cadence®

SpectreVerilog and UltraSimVerilog Migration to AMS Designer

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Contents

1

Setting Up the Migration Example

Important

SpectreVerilog and UltraSimVerilog are not available for 64-bit platforms. Hence, if you are using a 64-bit platform, and have set the `CDS_AUTO_64BIT` environment variable to `ALL`, unset the environment variable if you are using SpectreVerilog or UltraSimVerilog.

Before the Spectre AMS Designer simulator, the major mixed-signal solutions on the market were SpectreVerilog and UltraSimVerilog. The AMS Designer simulator provides faster simulation speed, increased capacity, and enhanced features for handling more complicated mixed-signal designs with new technologies. More and more chip designers use Spectre AMS Designer for mixed-signal simulation and verification.

This migration example shows you how you would simulate a PLL design using UltraSimVerilog, SpectreVerilog, and, finally, AMS Designer using the same `config` view. You will learn about the OSS netlister, the `ncverilog` flow, using `-v` and `-y` command-line options, compiled Verilog-A, fastcross, and other AMS Designer features.

Important

Use IC 6.1.3, MMSIM 6.2 or later, and IUS 6.11 or later for this example.

To set up the migration example, do the following in a terminal window:

1. Make and change to a directory for the migration example:

```
mkdir migrateToAMS
cd migrateToAMS
```

2. Copy the migration example files to this directory:

```
cp -r $CDSHOME/tools/dfII/samples/tutorials/AMS/MigrateFromCBNToOSSN.tar.gz .
```

3. Decompress the archive file:

```
gunzip MigrateFromCBNToOSSN.tar.gz
tar xf MigrateFromCBNToOSSN.tar
```

4. Change to the following directory:

```
cd MigrateFromCBNToOSSN
```

5. Source the setup file:

   ```
   source SETUP
   ```

   The `SETUP` file sets the `TUT_DIR` environment variable to your current directory:

   ```
   setenv TUT_DIR `pwd`
   ```

6. Start Cadence software:

   ```
   virtuoso &
   ```

See also:

- Features of the Migration Example, next
- Testbench for the PLL Design on page 4
- Inside the PLL_160MHZ Instance on page 5

Features of the Migration Example

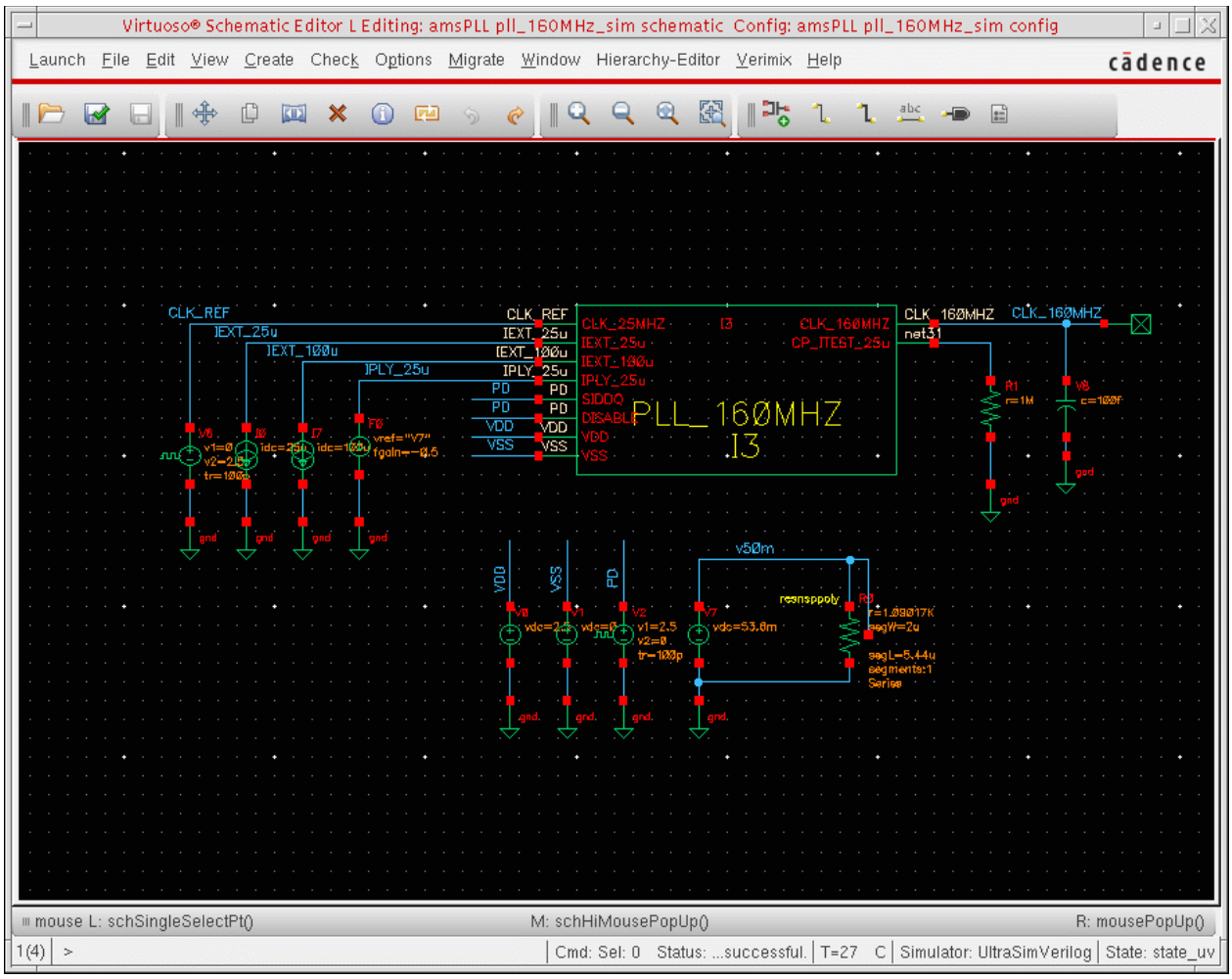
The migration example is a PLL design that has

- a 25 MHz input signal
- a 160 MHz output signal
- 305 MOSFETs
- 97 resistors
- 35 capacitors
- more than 30 behavioral modules

Testbench for the PLL Design

Here is the testbench schematic for the migration example (a PLL design).

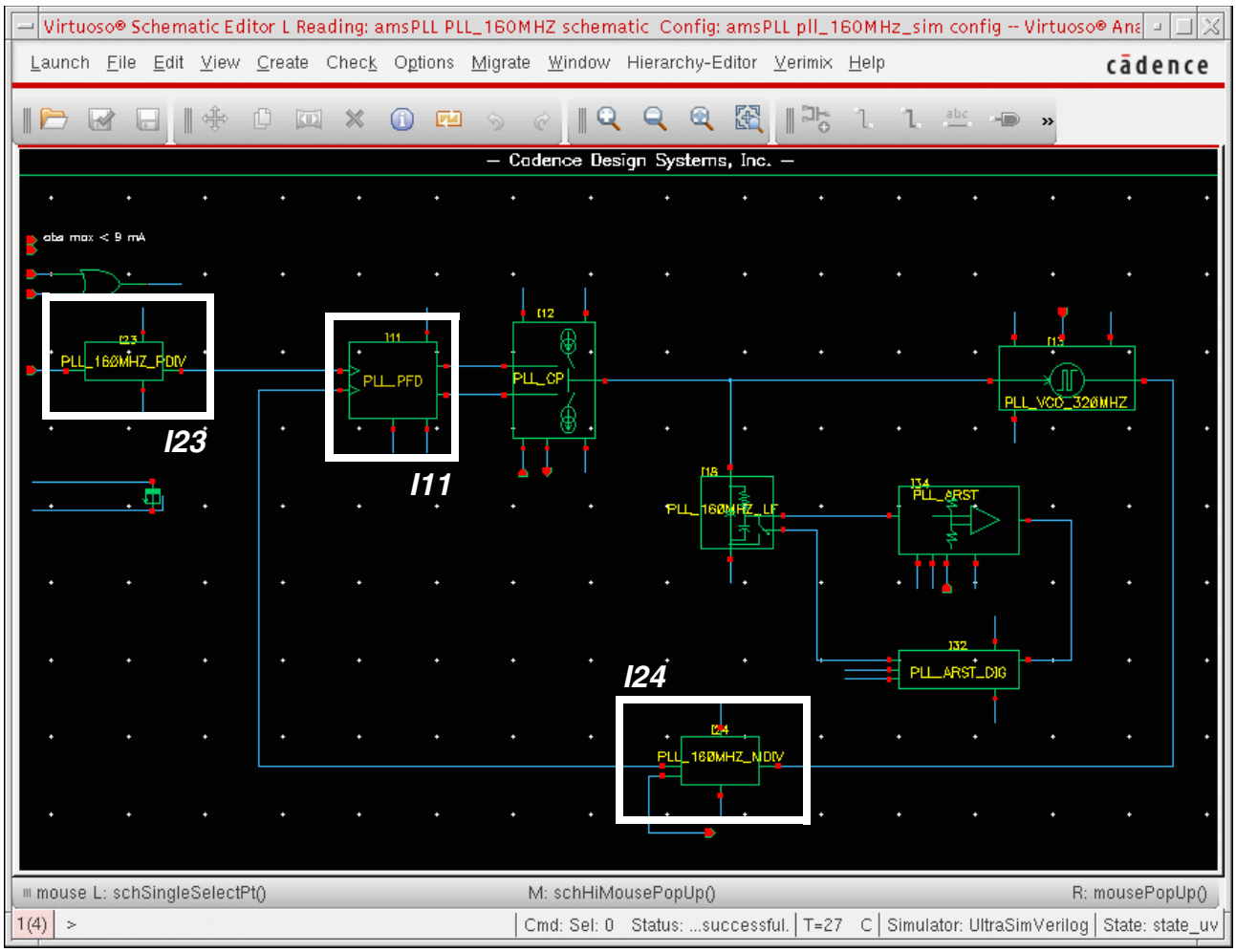
Figure 1-1 Testbench Schematic for PLL Design



Inside the PLL_160MHZ Instance

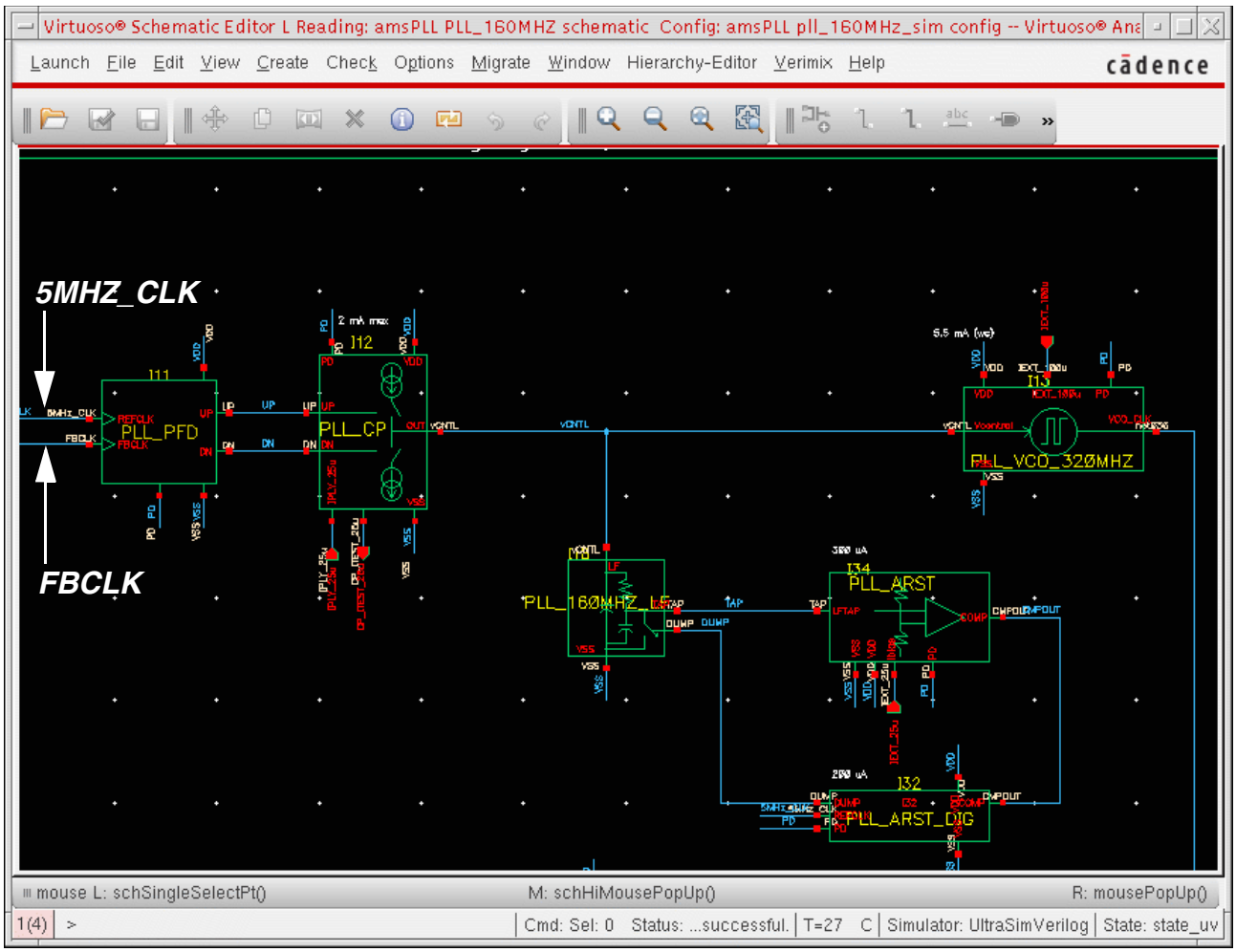
Inside the *I3* instance (*PLL_160MHZ*), the *I23* instance (*PLL_160MHZ_PDIV*) outputs a 5 MHz reference signal for the loop. The *I24* instance (*PLL_160MHZ_MDIV*) outputs a 160 MHz signal and a 5 MHz feedback signal for the *PLL_FPD* instance (*I11*).

Figure 1-2 Inside the I3 Instance



When the two *PD* input signals to *I3* (see Figure 1-1 on page 5) are out of sync, the PFD (*PLL_PFD*) generates corrective pulses (*UP*, *DN*) to adjust the charge pump output voltage (*vCNTL*) which controls the frequency of the VCO (*PLL_VCO_320MHZ*).

Figure 1-3 PFD Corrective Pulses, Charge Pump Output, VCO Input



Whenever the PLL is locked, the *FBCLK* and *5MHZ_CLK* signals are in phase and the VCO control signal (*vCNTL*) is stable.

2

Using the Spectre AMS Designer Simulator

Important

Use IC 6.1.3, MMSIM 6.2 or later, and IUS 6.11 or later for this example.

Spectre AMS Designer has many advantages:

- Better performance (33% for this particular example)
- More powerful digital solver (NC-Sim versus Verilog-XL)
- Powerful connect rules (CRs)
- Flexible discipline definitions
- Bidirectional CR support
- More language support (Verilog-AMS, VHDL-AMS, SystemVerilog, SystemC)

If you use the Spectre AMS Designer simulator in the Virtuoso Analog Design Environment (ADE), there are two netlisters:

- The cell-based netlister, which is the original netlister for AMS, requires `ams` simInfo (which contains information such as a parameter list and how to netlist each component) when it generates the individual `netlist.vams` netlist files in the library/cell/view directory structure. For more information, see "Netlisting" in the *Virtuoso AMS Environment User Guide*.
- The open simulation system (OSS) netlister is available in IC 5.1.41 USR4 and later. You can use this netlister when you migrate to AMS Designer. The OSS netlister uses existing `spectre` views. The OSS netlister generates a single netlist file (`netlist.vams`) that includes all the modules that need to be compiled. (The final netlist is also one file for Spectre and UltraSim.) The OSS netlister works the same way for the AMS Designer simulator as it does for the Spectre and UltraSim simulators.

If you are using the OSS netlister, you can use the same `config` view to run AMS Designer.

This tutorial illustrates how to use the OSS netlister and `ncverilog` so that you can benefit from the many advantages of AMS Designer. See the following topics for more information:

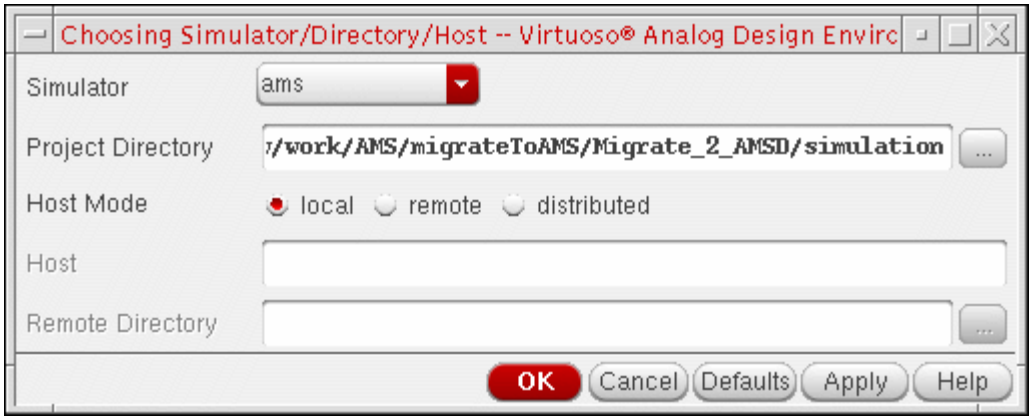
Changing the Simulator to AMS Designer

To change the simulator to AMS Designer, do the following:

1. In the Virtuoso® Analog Design Environment session window, choose *Setup – Simulator/Directory/Host*.

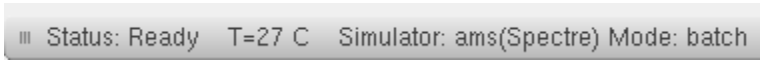
   The Choosing Simulator/Directory/Host form appears.

2. In the *Simulator* drop-down combo box, select *ams*.



3. Click *OK*.

   Simulator: ams appears on the status bar in the Virtuoso® Analog Design Environment session window. The name of the analog solver (*Spectre* or *UltraSim*) appears in parentheses after *ams*.

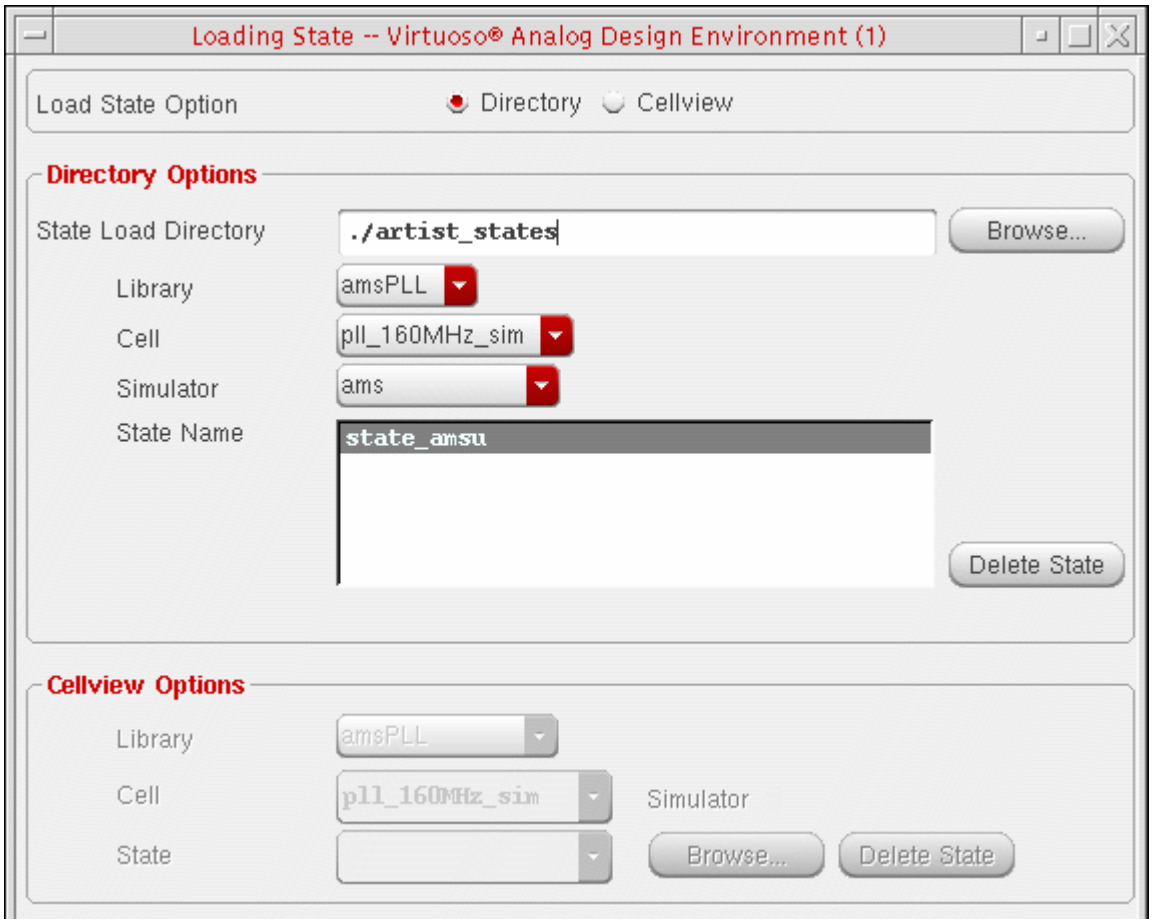


Loading the State File for AMS Designer

To load the state file for AMS Designer, do the following:

1. In the Virtuoso® Analog Design Environment window, choose *Session – Load State*.

   The Loading State form appears.

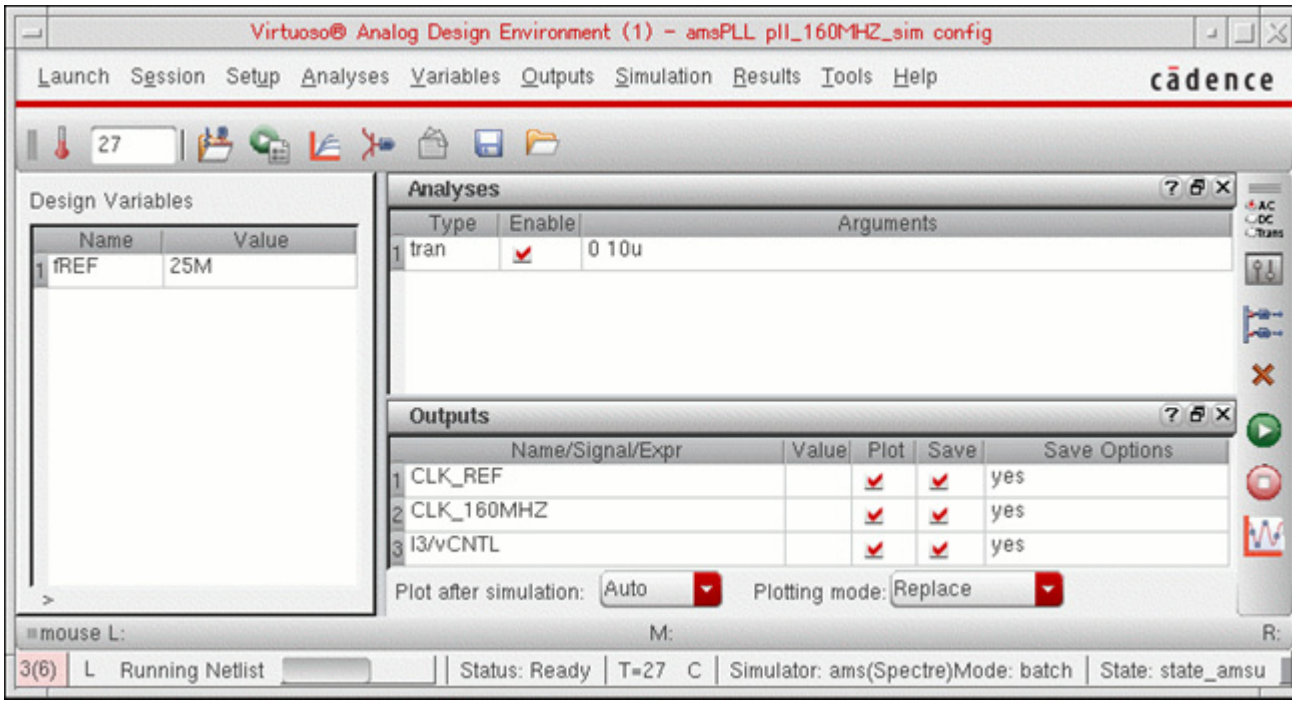


2. In the *State Name* area, select *state_amsu*.

   This state uses the UltraSim solver.

3. Click *OK*.

The state settings appear in the Virtuoso® Analog Design Environment session window, such as *tran … 10u* in the *Analyses* area and nodes to plot in the *Outputs* area. *Simulator: ams(UltraSim)* appears on the status bar in the ADE window.

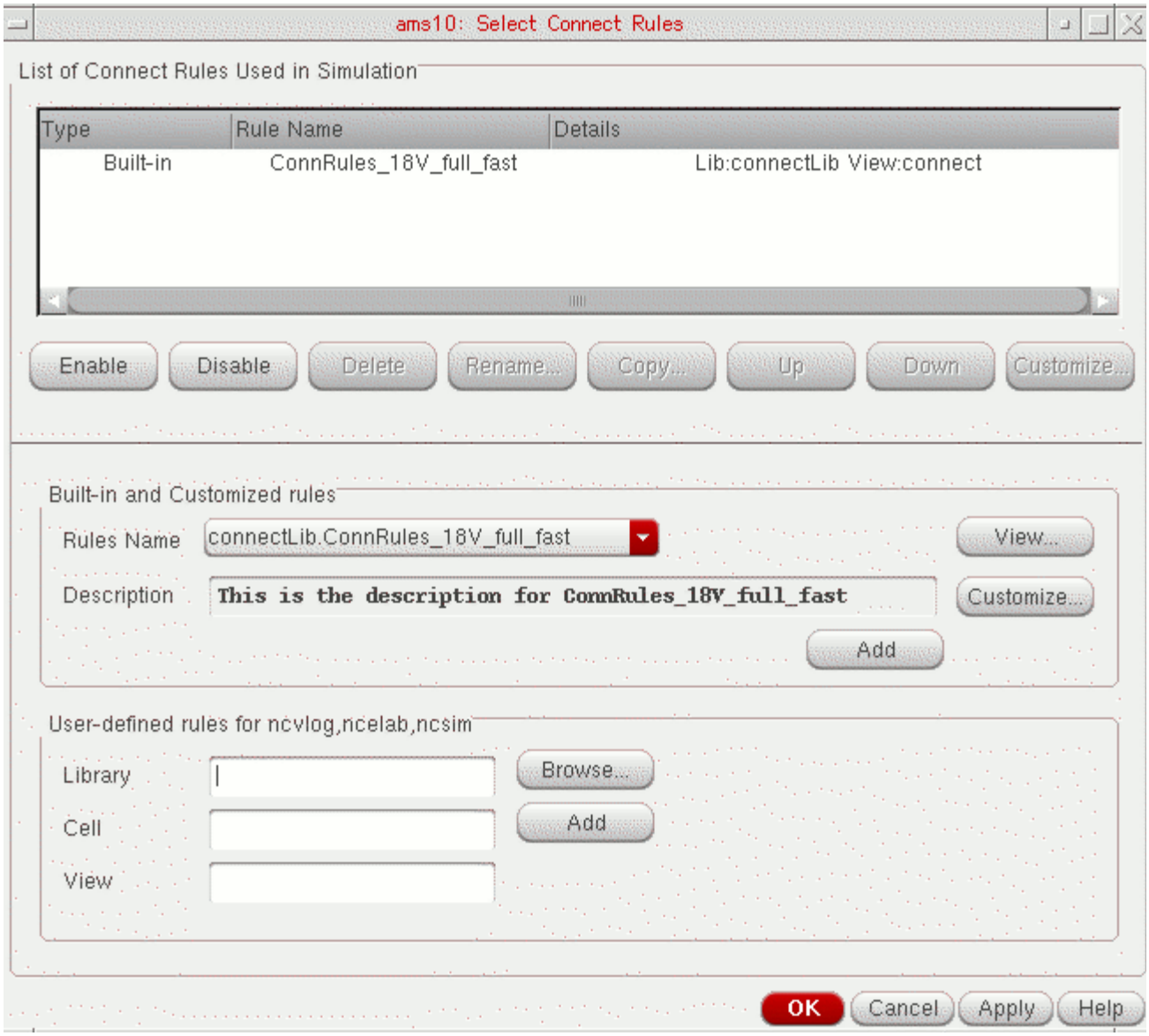


Selecting and Customizing Connect Rules for AMS Designer

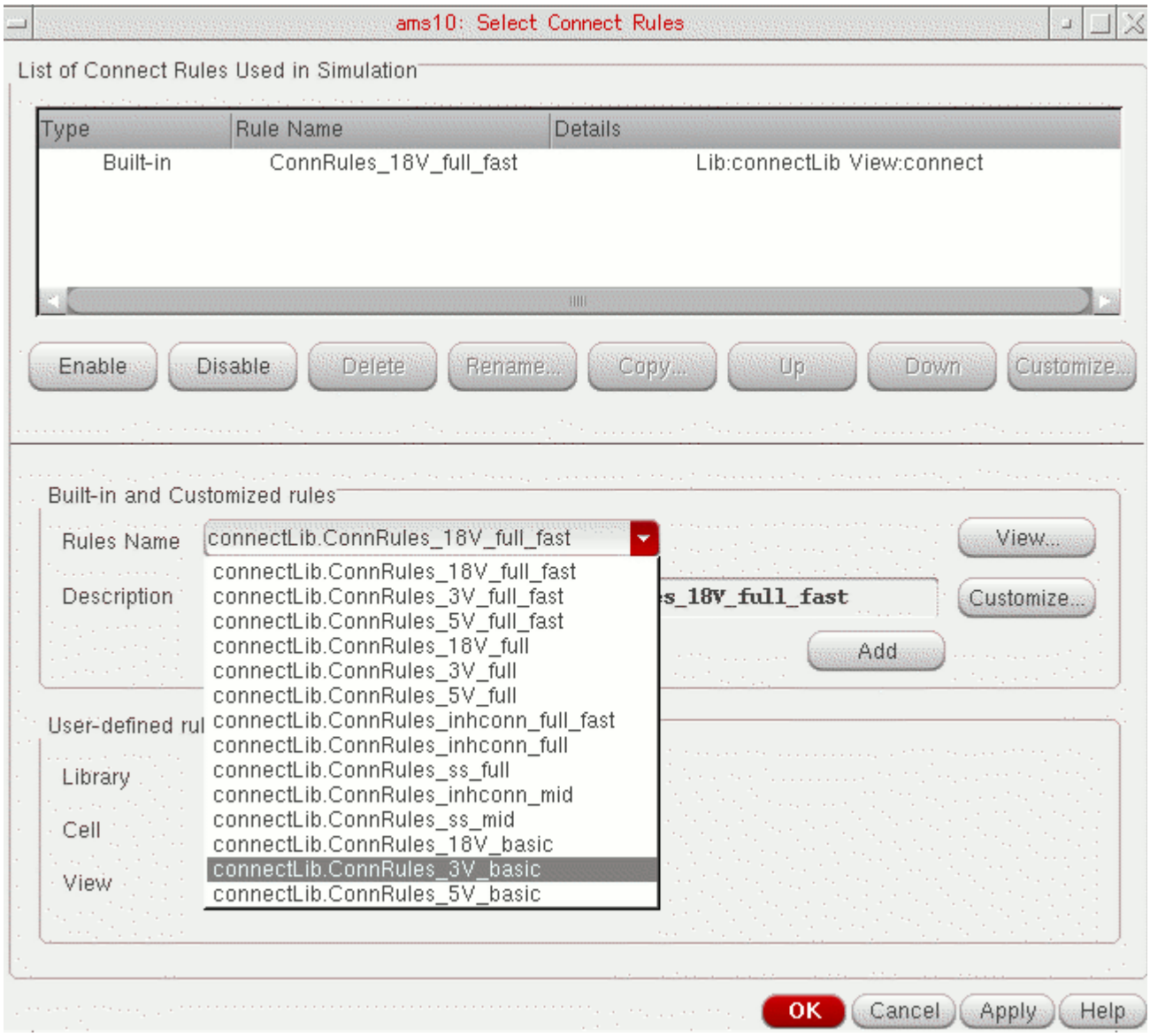
To specify and customize connect rules for the AMS Designer simulator, do the following:

1. In the Virtuoso® Analog Design Environment window, choose *Setup – Connect Rules*.

   The Select Connect Rules form appears.



2. In the *Rules Name* drop-down combo box, select *connectLib.ConnRules_3V_basic*.

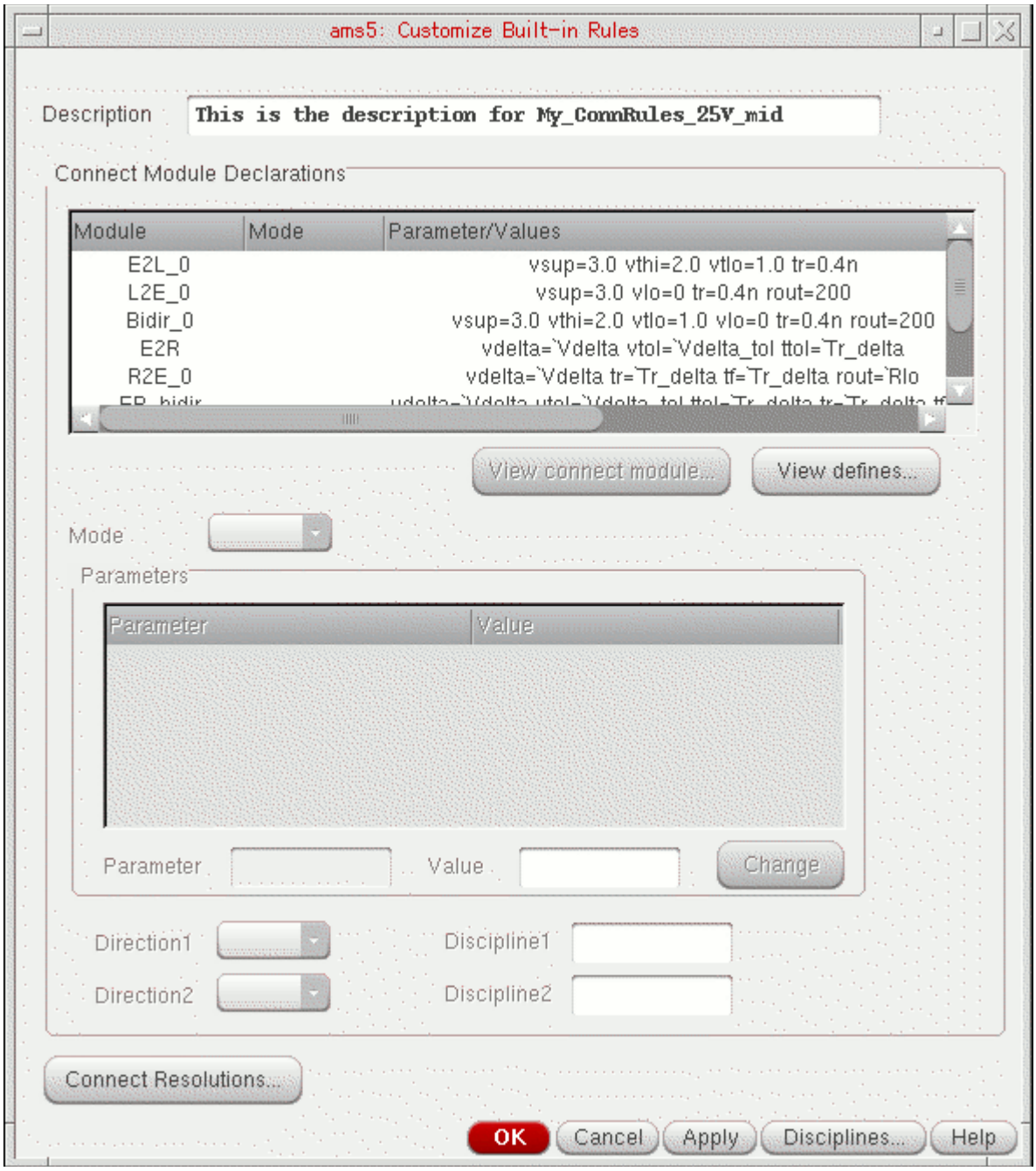


3. (Optional) To view the contents of the connect rule, click *View*.

   The connect rule file appears in a window. When you are finished viewing the file, you can choose *File – Close Window*.

4. To customize this connect rule, click *Customize*.

The Customize Built-in Rules form appears.

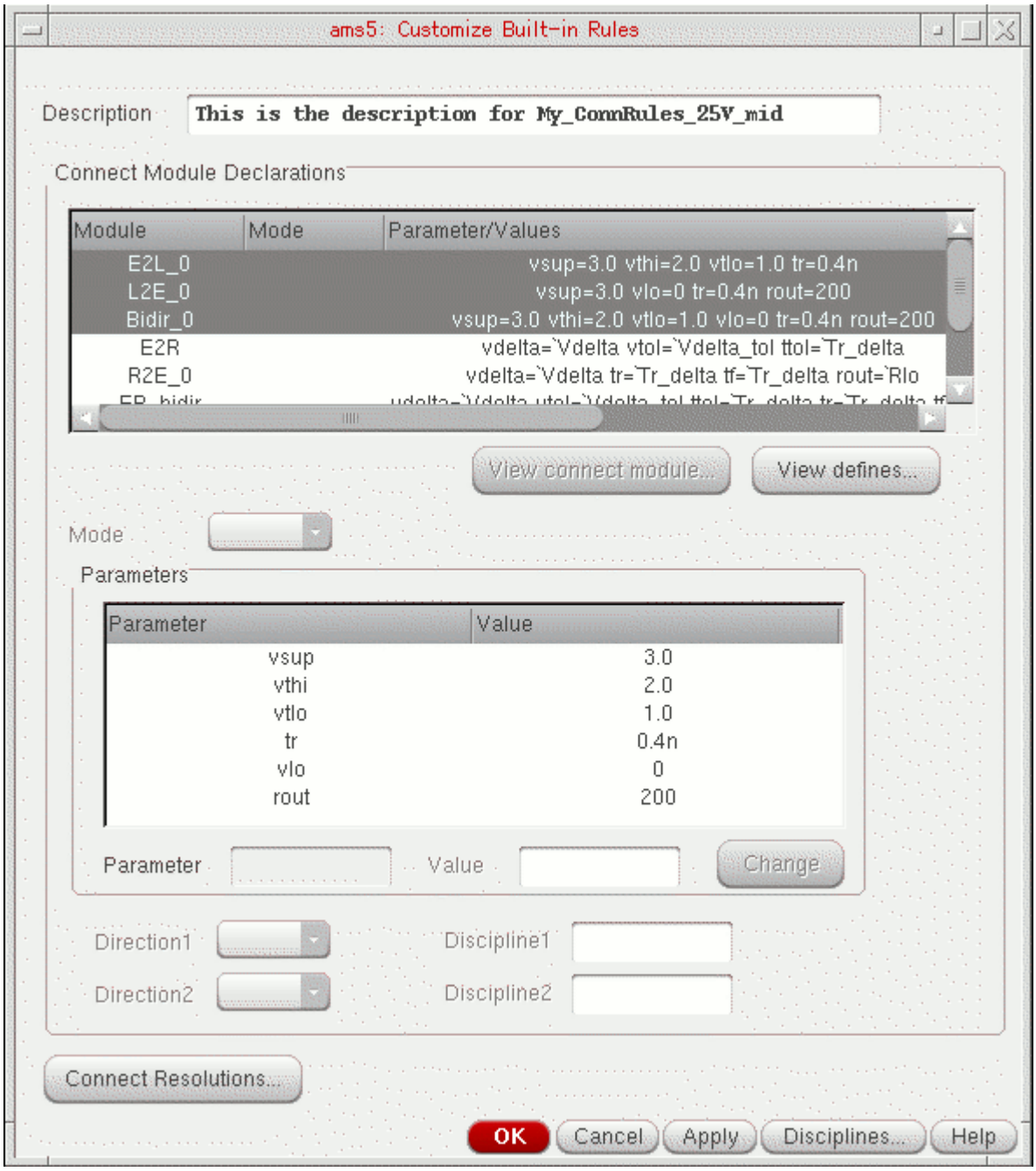


5. In the *Description* field, change the name of the rule to `My_ConnRules_25V_mid`:

```
This is the description for My_ConnRules_25V_mid
```

6. In the *Connect Module Declarations* group box, hilight the top three lines containing information for modules *E2L_0*, *L2E_0*, and *Bidir_0*.

   The shared parameters appear in the *Parameters* group box.



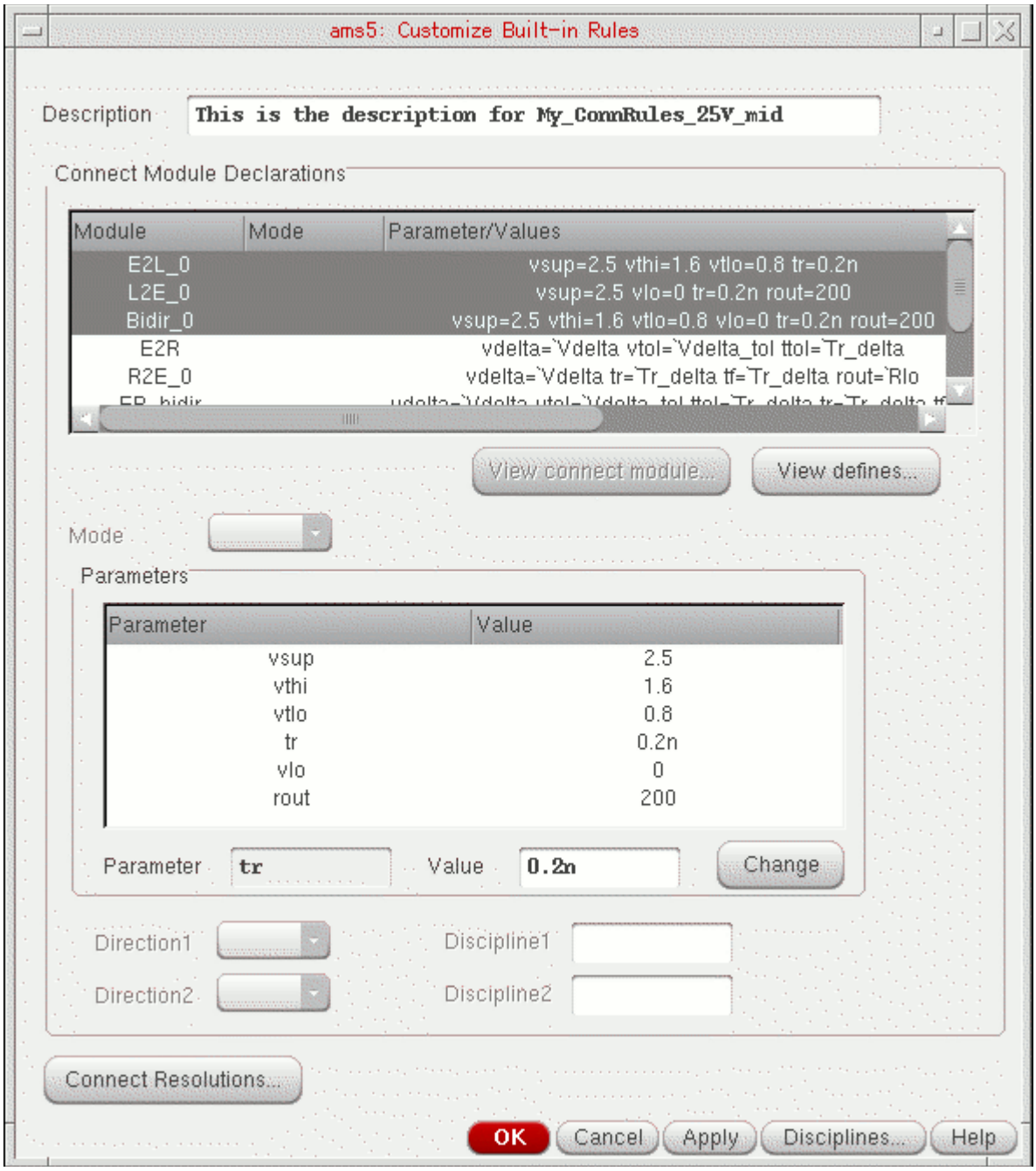
7. Change these values as follows:

Parameter	*Value*	Change it to
vsup	*3.0*	`2.5`
vthi	*2.0*	`1.6`
vtlo	*1.0*	`0.8`
tr	*0.4n*	`0.2n`

a. Select the parameter you want to change.

b. In the *Value* field, change its value.

c. Click *Change*.



8. Click *OK*.

9. On the Select Connect Rules form, click *Add*.

Modified built-in appears in the *Type* column.

10. Click *OK*.

The connect rules you specify on the Select Connect Rules form apply to the whole design.

Note: You might want to have several connect rules in the same design. You can set disciplines on a net, cell, instance, or library, and you can specify several connect rules accordingly.

Setting Netlister and Run Modes

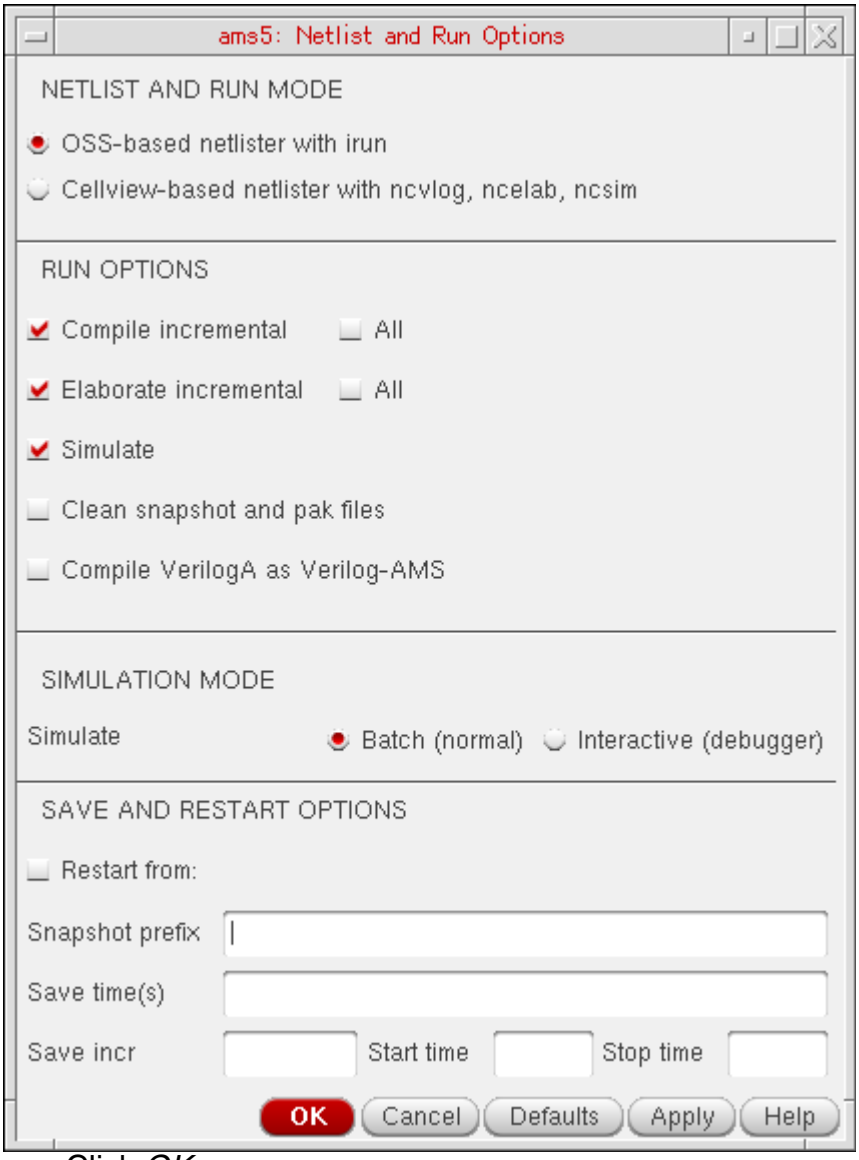
To set netlister and run modes, do the following:

1. In the Virtuoso® Analog Design Environment window, choose *Simulation – Netlist and Run Options*.

   The Netlister and Run Options form appears.

2. For *Netlister Mode*, select *OSS-based*.

   The *ncverilog* radio button appears as a *Run Mode* choice.

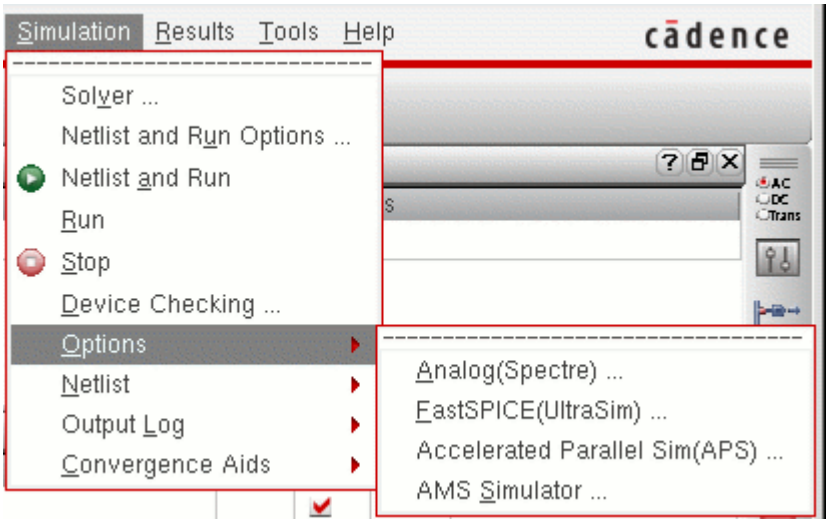


   Click *OK*.

You are ready to simulate.

Viewing Options

As you proceed through this next set of steps, you will notice several choices on the *Simulation – Options* menu in the Virtuoso® Analog Design Environment window:



You will not change any of these options during this example, but you will view some of the forms.

See

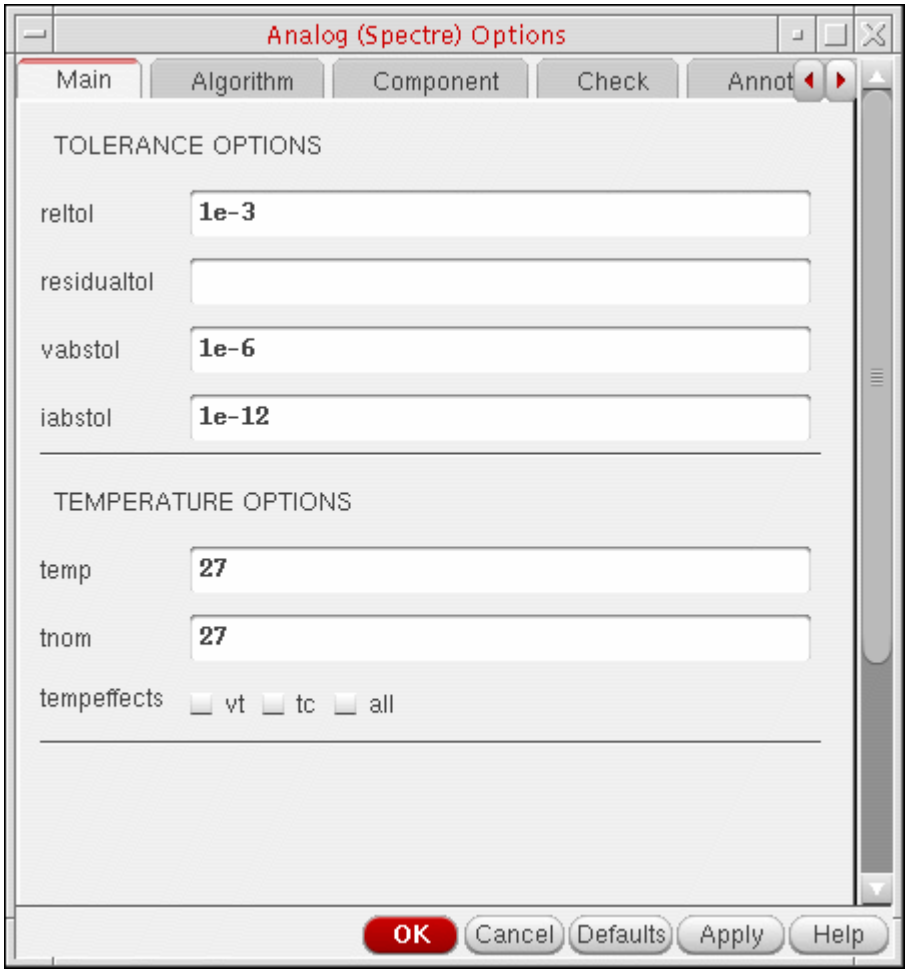
- Viewing Analog (Spectre) Options on page 24
- Viewing FastSPICE (UltraSim) Options on page 25
- Viewing AMS Options on page 26

Viewing Analog (Spectre) Options

To view Analog (Spectre) options, do the following:

1. In the Virtuoso® Analog Design Environment window, choose *Simulation – Options – Analog(Spectre)*.

   The Analog (Spectre) Options form appears.



   For information about the options you can set on this form, see the *Spectre Circuit Simulator and Accelerated Parallel Simulator User Guide*.

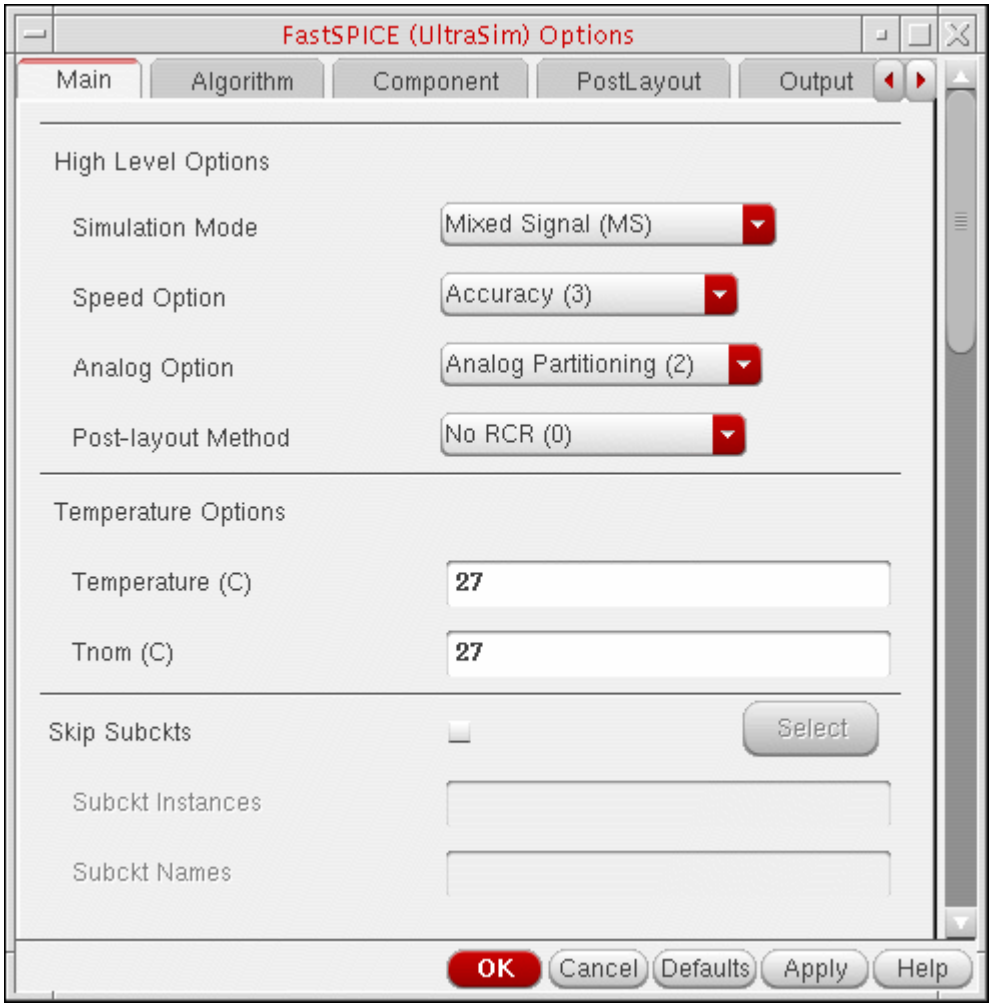
2. When you are finished viewing Spectre options, click *Cancel* to close the form.

Viewing FastSPICE (UltraSim) Options

To view FastSPICE (UltraSim) options, do the following:

1. In the Virtuoso® Analog Design Environment window, choose *Simulation – Options – FastSPICE(UltraSim)*.

   The FastSPICE (UltraSim) Options form appears.



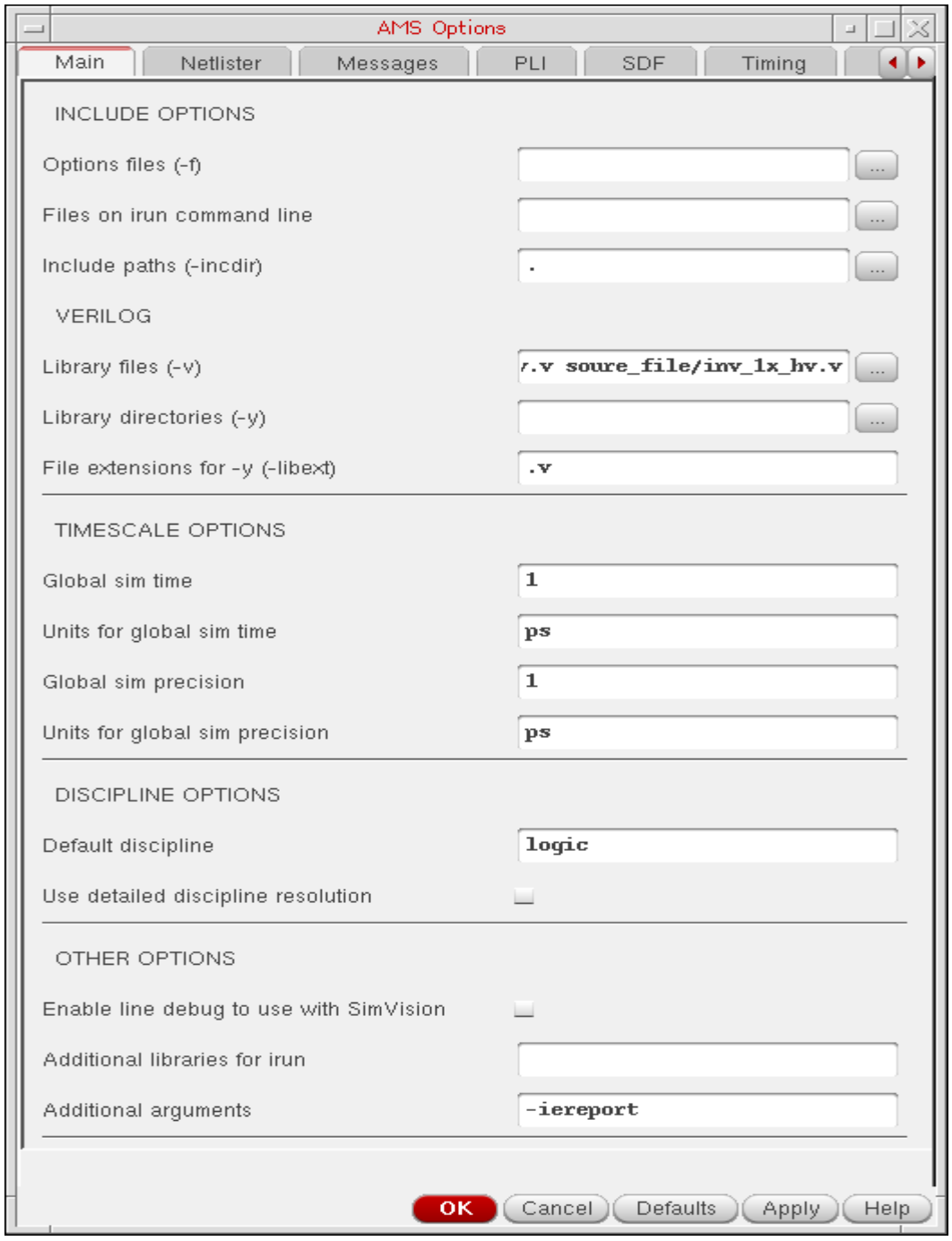
   For information about the options you can set on this form, see the *Virtuoso UltraSim Simulator User Guide*.

2. When you are finished viewing FastSPICE options, click *Cancel* to close the form.

Viewing AMS Options

To view AMS simulation options, do the following:

1. In the Virtuoso® Analog Design Environment window, choose *Simulation – Options – AMS Simulator*.



2. Scroll down to the bottom of this form to see that `-iereport` appears in the *Additional arguments* field.

   When you specify the `-iereport` option, the elaborator generates an interface element (IE) report. The IE report appears at the top of the simulation log file. This report contains information about each IE the software inserted into the design, such as its name, net, discipline, and so on.

3. When you are finished viewing options, click *Cancel* to close the form.

Netlisting and Running

To netlist and run, do the following:

➤ In the Virtuoso® Analog Design Environment window, choose *Simulation – Netlist and Run*.

Status appears in the upper left corner of the window. Simulation output information appears in the `ncverilog.log` file. The simulation time appears at the end of the file:

```
Time Usage:
  Total user time: 0:04:16 (256.980 sec), system time: 0:00:01 (1.100 sec),
real time: 0:04:26 (266.600 sec)
```

Note: This simulation ran for 5 minutes 47 seconds on our Solaris machine with a 1.6 G CPU.

Because *-iereport* appears in the *Additional arguments* field on the Main tab of the AMS tabbed window (see "Viewing AMS Options" on page 26), an IE report appears at the top of the log file. That report might look something like this:

```
----------IE report -------------

Automatically inserted instance: pll_160MHz_sim.I3.I11.I15.net18__E2L__logic
(merged):
        connectmodule name: E2L,
        inserted across signal: net18
        and ports of discipline: logic
        Sensitivity infomation:
                No Sensitivity info
        Discipline of Port (Ain): electrical, Analog port
        Discipline of Port (Dout): logic, Digital port
        Drivers of port Dout: No drivers
        Loads of port Dout: No loads
```

As you scroll down past UltraSim version and build time information, you will notice messages related to the compiled C flow for Verilog-A. Those messages might look something like this:

```
File read: .../Migrate_2_AMSD/models/spectre/resd_va.va
Created directory amsControl.ahdlSimDB/ (775)
Created directory
```

```
        amsControl.ahdlSimDB/
2143_migrateToAMS_Migrate_2_AMSD_models_spectre_resd_va.va.ahdlcmi/
        (775)
Created directory
        amsControl.ahdlSimDB/
2143_migrateToAMS_Migrate_2_AMSD_models_spectre_resd_va.va.ahdlcmi/
Linux2.4.21-37.ELsmp+gcc/
        (775)
Compiling ahdlcmi module library.
Finished compilation in 2 s (elapsed).
Installed compiled interface for resd_va.
```

You can use the compiled C flow to boost performance particularly when you are using Verilog-A to model bsources or CMOS devices such as MOSFETs, resistors, and capacitors. See “Using the Compiled C Code Flow” in the *Cadence Verilog-A Language Reference* for more information.

The IUS 5.83 release supports a feature called FastCross that speeds up the simulation by reducing the number of global time steps. Information about the total global time steps appears near the end of the log file:

```
Total Accepts: 1.452 M
```

You can close each window by choosing *File – Close Window*.

Viewing Waveforms

When the simulation finishes, a graph window appears in Virtuoso Visualization and Analysis XL. For derails on using this waveform tool, see the *Virtuoso Visualization and Analysis XL User Guide*.

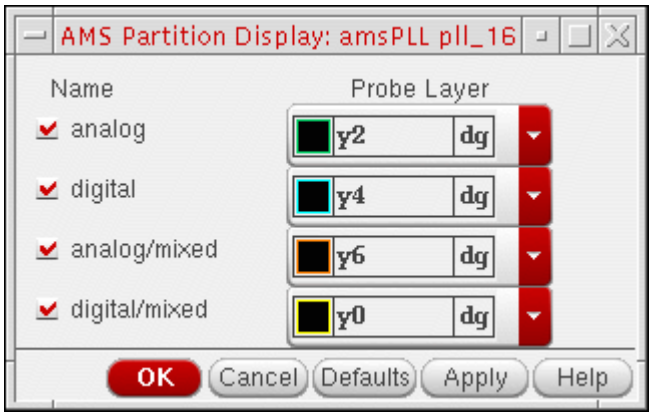
Displaying Partitions

Note: You can view partitions only after you have completed simulation and elaboration.

You can verify the partitions for AMS Designer:

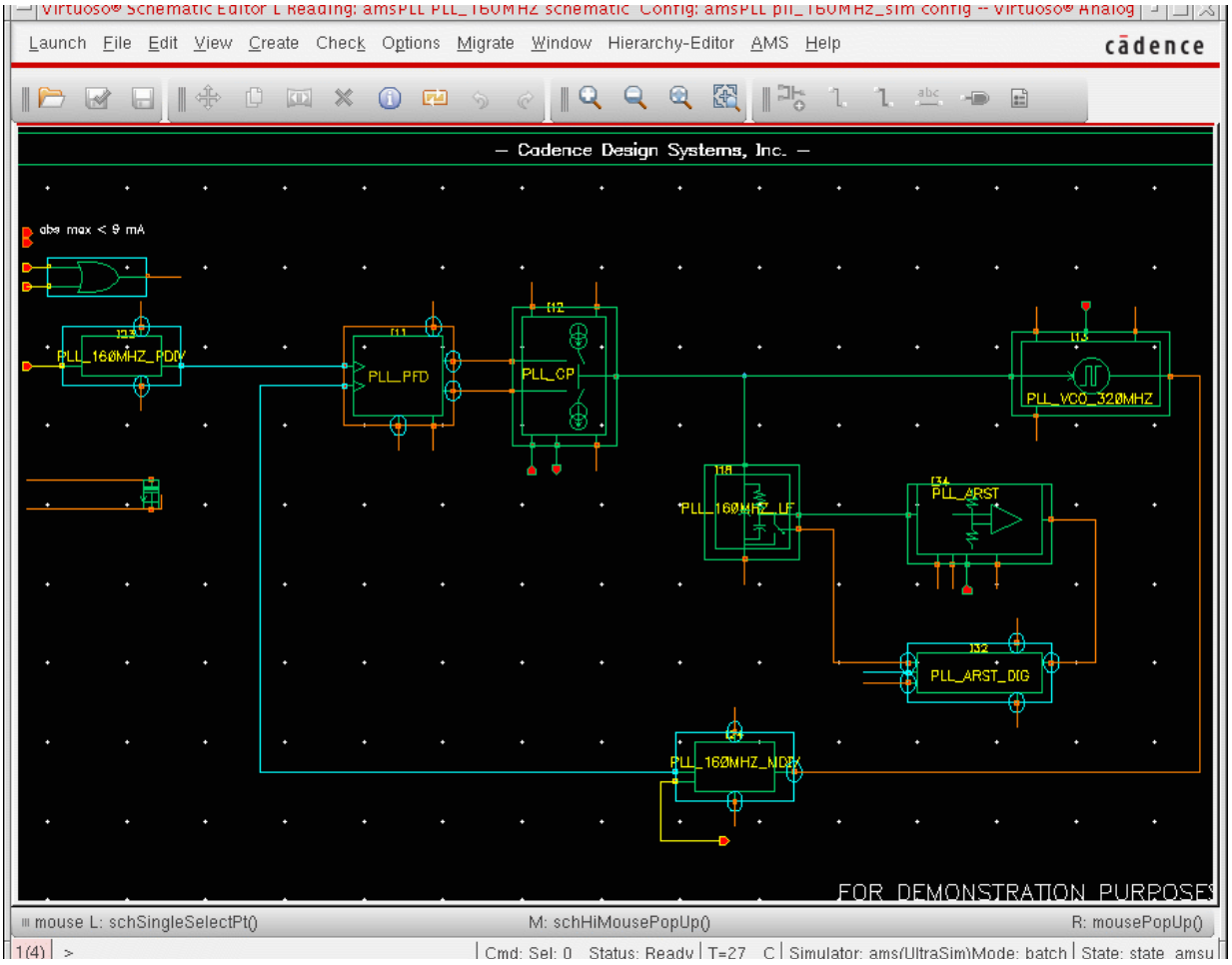
1. Make the *AMS* menu available in the menu bar. For this, choose *Launch – Plug-ins – Mixed Signal – Options – AMS*.
2. In the schematic window, descend into *I3* :
   a. Select I3.
   b. Type `e`.
   c. Click *OK*.
3. In the schematic window, choose *AMS – Display Partition – Initialize*.
4. In the schematic window, choose *AMS – Display Partition – Interactive*.

   The AMS Partition Display form appears.



5. Click *OK*.

On the schematic, mixed-signal items appear in orange and yellow.



You can see the set up for connect rules and disciplines both from the *AMS* menu in the schematic window and by choosing *Setup – Connect Rules* in the Virtuoso® Analog Design Environment window.

Understanding Connect Rules and Disciplines in AMS Designer

The AMS Designer simulator uses disciplines, connect modules, and connect rules in place of A2D and D2A interface elements. A discipline denotes an object as analog or digital (with, for example, an `electrical` or `logic` discipline). When you connect objects of different disciplines, connect rules determine which connect modules to insert between the objects. The inserted connect modules convert signals to values that are appropriate for each discipline. You can modify connect rule parameters such as supply voltage and rise time in your connect modules to tailor conversion of your design.

Note: For more information about disciplines, connect rules, and connect modules, see "Mixed-Signal Aspects of Verilog-AMS" in the *Cadence Verilog-AMS Language Reference*.

Cadence provides sample connect rules in the following directory:

```
$AMSHOME/tools/affirma_ams/etc/connect_lib
```

The sample connect rules (CRs) here are built in and ready for use in the Virtuoso® Analog Design Environment (ADE). Built-in CRs work for a certain set of voltage supplies only (such as 1.8V, 3V, and 5V). You can modify the parameters to customize a built-in CR for your design needs. Advanced designers can write customized CRs and include them in the simulation.

For this example, the voltage supply is 2.5 V. We can customize the 3V built-in CR to fit our simulation.

Note: Cadence provides full-fast, full, mid, and basic built-in CRs. You can speed up the simulation for complicated designs using the full-fast CRs. For this example, we do not need a bidirectional CR; we can choose a simpler CR.

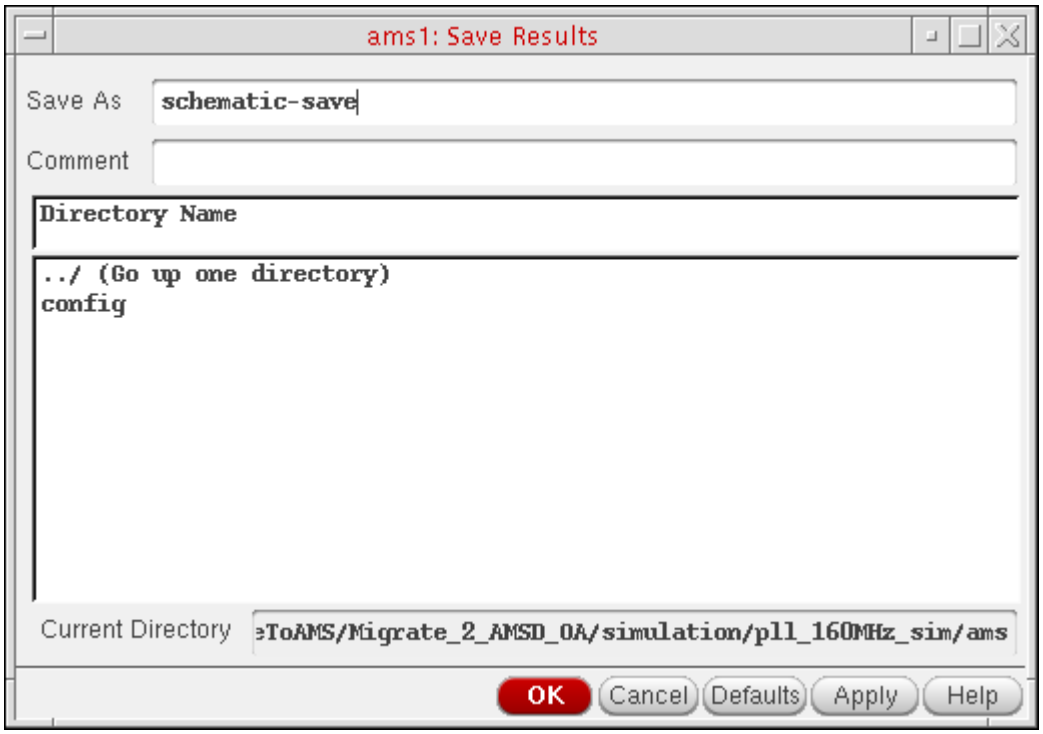
Simulating the Design Using the Spectre Solver

The AMS Designer simulator has two analog solvers: UltraSim and Spectre. To simulate the example design using the Spectre solver, you can do the following:

1. Save the results from the previous simulation as follows:

   a. In the Virtuoso® Analog Design Environment window, choose *Results – Save*.

      The Save Results form appears.

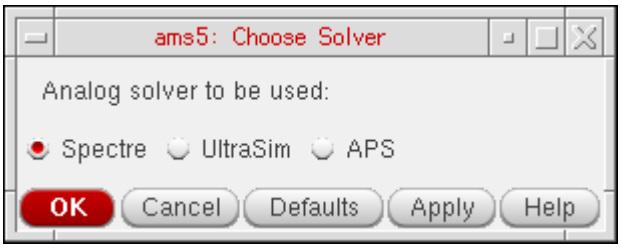


   b. In the *Save As* field, type a name for your results.

   c. Click *OK*.

2. Choose *Simulation – Solver*.

The Choose Solver form appears.



3. Select *Spectre* as the *Analog solver to be used*.
4. Click *OK*.
5. In the Virtuoso® Analog Design Environment window, choose *Simulation – Netlist and Run*.

   Status appears in the upper left corner of the window. Simulation output information appears in the `ncverilog.log` file. The simulation time appears at the end of the file.

   ```
   Total time required for tran analysis `tran' was 3.11407 ks (51m  54.1s).
   ```

   You can compare these results to those from the simulation using AMS Designer with the UltraSim solver.

   Note: This simulation ran for 60 minutes on our Solaris machine with a 1.6 G CPU.

   When the simulation finishes, a graph window appears. For derails on using this waveform tool, see the *Virtuoso Visualization and Analysis XL User Guide*. .