cadence®

Spectre Circuit Simulator Components and Device Models Reference

Product Version 23.1
June 2023

© 2023 Cadence Design Systems, Inc. All rights reserved.
Printed in the United States of America.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

MMSIM contains technology licensed from, and copyrighted by: C. L. Lawson, R. J. Hanson, D. Kincaid, and F. T. Krogh © 1979, J. J. Dongarra, J. Du Croz, S. Hammarling, and R. J. Hanson © 1988, J. J.Dongarra, J. Du Croz, I. S. Duff, and S. Hammarling © 1990; University of Tennessee, Knoxville, TN andOak Ridge National Laboratory, Oak Ridge, TN © 1992-1996; Brian Paul © 1999-2003; M. G. Johnson,Brisbane, Queensland, Australia © 1994; Kenneth S. Kundert and the University of California, 1111 FranklinSt., Oakland, CA 94607-5200 © 1985-1988; Hewlett-Packard Company, 3000 Hanover Street, Palo Alto,CA 94304-1185 USA © 1994, Silicon Graphics Computer Systems, Inc., 1140 E. Arques Ave., Sunnyvale,CA 94085 © 1996-1997, Moscow Center for SPARC Technology, Moscow, Russia © 1997; Regents of theUniversity of California, 1111 Franklin St., Oakland, CA 94607-5200 © 1990-1994, Sun Microsystems, Inc.,4150 Network Circle Santa Clara, CA 95054 USA © 1994-2000, Scriptics Corporation, and other parties ©1998-1999; Aladdin Enterprises, 35 Efal St., Kiryat Arye, Petach Tikva, Israel 49511 © 1999 and Jean-loupGailly and Mark Adler © 1995-2005; RSA Security, Inc., 174 Middlesex Turnpike Bedford, MA 01730 ©2005

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522. All other trademarks are the property of their respective holders.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Patents: Cadence product described in this document, is protected by U.S. Patents 5,610,847; 5,790,436; 5,812,431; 5,859,785; 5,949,992; 5,987,238; 6,088,523; 6,101,323; 6,151,698; 6,181,754; 6,260,176; 6,278,964; 6,349,272; 6,374,390; 6,493,849; 6,504,885; 6,618,837; 6,636,839; 6,778,025; 6,832,358; 6,851,097; 7,035,782; 7,085,700.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information. Cadence is committed to using respectful language in our code and communications. We are also active in the removal and/or replacement of

inappropriate language from existing content. This product documentation may however contain material that is no longer considered appropriate but still reflects long-standing industry terminology. Such content will be addressed at a time when the related software can be updated without end-user impact.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Contents

Preface . . . 51
Related Documents . . . 52
Typographic and Syntax Conventions . . . 52

1
Circuit Components . . . 55
Current Sources . . . 56
Linear Current Controlled Current Source (cccs) . . . 57
Sample Instance Statement . . . 57
Instance Syntax . . . 57
Instance Parameters . . . 58
Output Parameters . . . 60
Linear Current Controlled Voltage Source (ccvs) . . . 60
Sample Instance Statement . . . 61
Instance Syntax . . . 61
Instance Parameters . . . 62
Output Parameters . . . 64
Independent Current Source (isource) . . . 64
Sample Instance Statement . . . 64
Instance Syntax . . . 64
Instance Parameters . . . 65
PWL Type Waveform . . . 75
Bit Type Waveform . . . 75
PRBS Type Waveform . . . 76
LFSR Modes . . . 76
Triggering Mode . . . 76
Jitter . . . 77
Noise of the source . . . 77
Output Parameters . . . 77
Operating-Point Parameters . . . 77

© 2023 Cadence Design Systems, Inc.

Polynomial Current Controlled Current Source (pcccs) . . . 78
Sample Instance Statement . . . 78
Instance Syntax . . . 78
Instance Parameters . . . 79
Operating-Point Parameters . . . 79
Polynomial Voltage Controlled Current Source (pvccs) . . . 80
Instance Syntax . . . 80
Instance Parameters . . . 81
Operating-Point Parameters . . . 81
s-Domain Linear Current Controlled Current Source (scccs) . . . 82
Sample Instance Statement . . . 83
Instance Syntax . . . 83
Instance Parameters . . . 84
Operating-Point Parameters . . . 84
s-Domain Linear Voltage Controlled Current Source (svccs) . . . 85
Sample Instance Statement . . . 86
Instance Syntax . . . 86
Instance Parameters . . . 86
Operating-Point Parameters . . . 86
Linear Voltage Controlled Current Source (vccs) . . . 87
Sample Instance Statement . . . 87
Instance Syntax . . . 88
Instance Parameters . . . 89
Output Parameters . . . 91
Operating-Point Parameters . . . 91
z-Domain Linear Current Controlled Current Source (zcccs) . . . 91
Notes on gain and gainfactor . . . 92
Sample Instance Statement . . . 93
Instance Syntax . . . 93
Instance Parameters . . . 94
Operating-Point Parameters . . . 94
z-Domain Linear Voltage Controlled Current Source (zvccs) . . . 95
Instance Syntax . . . 96
Instance Parameters . . . 97
Operating-Point Parameters . . . 97
Voltage Sources . . . 98

© 2023 Cadence Design Systems, Inc.

Polynomial Current Controlled Voltage Source (pccvs) . . . 98
Sample Instance Statement . . . 98
Instance Syntax . . . 99
Instance Parameters . . . 100
Operating-Point Parameters . . . 100
Polynomial Voltage Controlled Voltage Source (pvcvs) . . . 101
Sample Instance Statement . . . 101
Instance Syntax . . . 101
Instance Parameters . . . 102
Operating-Point Parameters . . . 102
s-Domain Voltage Controlled Voltage Source (svcvs) . . . 103
Notes on gain and gainfactor . . . 103
Sample Instance Statement . . . 104
Instance Syntax . . . 104
Instance Parameters . . . 104
Operating-Point Parameters . . . 104
Linear Voltage Controlled Voltage Source (vcvs) . . . 105
Sample Instance Statement . . . 105
Instance Syntax . . . 105
Instance Parameters . . . 106
Output Parameters . . . 107
Operating-Point Parameters . . . 107
Independent Voltage Source (vsource) . . . 107
Sample Instance Statement . . . 108
Instance Syntax . . . 108
Instance Parameters . . . 108
Output Parameters . . . 122
Operating-Point Parameters . . . 122
z-Domain Current Controlled Voltage Source (zccvs) . . . 122
Sample Instance Statement . . . 123
Instance Syntax . . . 123
Instance Parameters . . . 124
Operating-Point Parameters . . . 125
z-Domain Voltage Controlled Voltage Source (zvcvs) . . . 125
Instance Syntax . . . 127
Instance Parameters . . . 127

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters . . . 128
Behavioral Source (bsource) . . . 128
Sample Instance Statement . . . 128
Multiplicity factor . . . 129
Temperature Parameters . . . 130
Clipping Parameters . . . 130
Noise Parameters . . . 130
DC Mismatch Parameters . . . 131
Other Parameters . . . 131
Instance Parameters . . . 132
Mathematical Definitions . . . 132
Noise Model for bsource . . . 134
Temperature Effect on bsource . . . 136
Independent Resistive Source (port) . . . 137
Sample Instance Statement . . . 137
Instance Syntax . . . 137
Instance Parameters . . . 138
PWL Type Waveform . . . 149
Bit Type Waveform . . . 150
PRBS Type Waveform . . . 150
LFSR Modes: . . . 150
Triggering Mode: . . . 151
Jitter: . . . 151
Linear N Port (nport) . . . 152
Sample Instance Statement . . . 153
Sample Model Statement . . . 153
Synopsis . . . 154
Model Synopsis . . . 154
Instance Parameters . . . 154
Passivity checking and enforcement parameters . . . 155
Model Syntax . . . 160
Model Parameters . . . 161
Important note about spline and linear interpolation parameters . . . 164
Current Probe (iprobe) . . . 170
Sample Instance Statement . . . 170
Instance Syntax . . . 170

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters . . . 170
Circuit Reduced Order Model (cktrom) . . . 171
Sample Instance Statement . . . 171
Instance Syntax . . . 172
Instance Parameters . . . 172
Operating-Point Parameters . . . 172
Analog-to-Logic Converter (a2d) . . . 172
device checker (assert) . . . 173
Instance Syntax . . . 173
Instance Parameters . . . 174
Logic-to-Analog Converter (d2a) . . . 176
Sample Instance Statement . . . 176
Instance Syntax . . . 176
Instance Parameters . . . 177
Ideal Switch (switch) . . . 177
Sample Instance Statement . . . 178
Instance Syntax . . . 178
Instance Parameters . . . 179
Output Parameters . . . 179
Ratiometric Fourier Analyzer (fourier) . . . 179
Sample Instance Statement . . . 180
Sample Model Statement . . . 180
Instance Syntax . . . 180
Instance Parameters . . . 181
Model Syntax . . . 182
Model Parameters . . . 182
IBIS I/O buffer (ibis_buffer) . . . 182
Driver Equations . . . 183
Receiver Equations . . . 183
Switching Coefficients . . . 184
Sample Instance Statement . . . 184
Sample Model Statement . . . 184
Instance Syntax . . . 185
Instance Parameters . . . 187
Model Syntax . . . 188
Model Parameters . . . 189

© 2023 Cadence Design Systems, Inc.

2
Passive Components

Passive Components . . . 195
Two Terminal Resistor (resistor) . . . 196
Two Terminal Resistor . . . 196
Wire RC Model . . . 198
Scaling Effects . . . 199
Component Statements . . . 200
Sample Instance Statement . . . 202
Sample Model Statement . . . 202
Sample behavior Statement . . . 202
Instance Syntax . . . 202
Instance Parameters . . . 203
Model Syntax . . . 204
Model Parameters . . . 205
Output Parameters . . . 210
Operating-Point Parameters . . . 210
Physical Resistor (phy_res) . . . 211
Thermal Noise . . . 213
Shot Noise for the Junctions . . . 213
Flicker Noise for the Resistor . . . 213
Flicker Noise for the Junctions . . . 214
Sample Instance Statement . . . 215
Sample Model Statement . . . 215
Instance Syntax . . . 215
Instance Parameters . . . 215
Model Syntax . . . 216
Model Parameters . . . 216
Output Parameters . . . 221
Operating-Point Parameters . . . 221
R2 Model (r2) . . . 222
Usage . . . 222
Equivalent Circuit . . . 223
Bias Dependence . . . 223
Geometry Dependence . . . 225
Temperature Dependence . . . 229

© 2023 Cadence Design Systems, Inc.

Noise . . . 230
Description and Details . . . 231
Component Statements . . . 232
Instance Syntax . . . 232
Instance Parameters . . . 233
Model Syntax . . . 233
Model Parameters . . . 234
Operating-Point Parameters . . . 235
Fractional Impedance/Admittance Pole (fracpole) . . . 236
Instance Syntax . . . 238
Instance Parameters . . . 239
Model Syntax . . . 239
Model Parameters . . . 240
Operating-Point Parameters . . . 240
Two-Terminal Capacitor (capacitor) . . . 240
Sample Instance Statement . . . 241
Sample Model Statement . . . 242
Sample Behavior Statement . . . 242
Instance Syntax . . . 242
Instance Parameters . . . 243
Model Syntax . . . 244
Model Parameters . . . 245
Output Parameters . . . 246
Two Terminal Capacitor with the specified Q factor (capq) . . . 247
Description . . . 247
Instance Syntax . . . 248
Instance Parameters . . . 249
Model Syntax . . . 250
Interconnect Capacitance (intcap) . . . 250
Instance Syntax . . . 251
Instance Parameters . . . 252
Model Syntax . . . 253
Model Parameters . . . 254
Output Parameters . . . 254
Junction Capacitor (juncap) . . . 255
Instance Syntax . . . 255

© 2023 Cadence Design Systems, Inc.

Instance Parameters . . . 256
Model Syntax . . . 256
Model Parameters . . . 257
Output Parameters . . . 259
Operating-Point Parameters . . . 260
JUNCAP2 Model (juncap200) . . . 260
Instance Syntax . . . 261
Instance Parameters . . . 261
Model Syntax . . . 261
Model Parameters . . . 262
Operating-Point Parameters . . . 265
Junction Capacitor (juncap_eldo) . . . 265
Sample Instance Statement . . . 266
Sample Model Statement . . . 266
Instance Syntax . . . 266
Instance Parameters . . . 266
Model Syntax . . . 266
Model Parameters . . . 267
Output Parameters . . . 269
Operating-Point Parameters . . . 270
Two Terminal Inductor (inductor) . . . 271
Sample Instance Statement . . . 271
Sample Model Statement . . . 272
Sample Behavior Statement . . . 272
Instance Syntax . . . 272
Instance Parameters . . . 273
Model Syntax . . . 273
Model Parameters . . . 273
Output Parameters . . . 275
Operating-Point Parameters . . . 275
Mutual Inductor (mutual_inductor) . . . 275
Sample Instance Statement with Two Inductors . . . 276
Instance Syntax . . . 276
Instance Parameters . . . 276
Magnetic Core with Hysteresis (core) . . . 277
Sample Instance Statement . . . 278

© 2023 Cadence Design Systems, Inc.

Sample Model Statement . . . 278
Instance Syntax . . . 278
Instance Parameters . . . 279
Model Syntax . . . 279
Model Parameters . . . 280
Winding for Magnetic Core (winding) . . . 281
Sample Instance Statement . . . 282
Instance Syntax . . . 282
Instance Parameters . . . 282
Linear Inductance, Reluctance, Resistance, and Capacitance Matrix (rlck_matrix) . . . 283
Sample Instance Statement . . . 283
Instance Syntax . . . 283
Instance Parameters . . . 284

3
Parameters Common to All Devices . . . 285
Multiplication Factor (m) . . . 286
Scaling Factors (scale and scalem) . . . 286
imelt and imax . . . 287
SPICE Compatibility Flag (compatible) . . . 289

4
Diode Model (diode) . . . 291
Device Regions . . . 292
Level-1 Model . . . 293
DC Current . . . 293
Junction Capacitance . . . 295
Peripheral Junction Capacitance . . . 295
Diffusion Capacitance . . . 295
Total Capacitance . . . 295
Breakdown Current . . . 296
Temperature Effect . . . 297
Noise Model . . . 301
Series Resistance Thermal Noise . . . 301
Diode Shot and Flicker Noise . . . 301

© 2023 Cadence Design Systems, Inc.

Scaling Effects . . . 301
Level-2 Model . . . 302
DC Current . . . 303
Linear Capacitance . . . 303
Scaling Effects . . . 303
Level-3 Model . . . 304
Component Statements . . . 305
Sample Instance Statement . . . 305
Sample Model Statement . . . 305
Instance Definition . . . 305
Instance Parameters . . . 306
Model Definition . . . 306
Model Parameters . . . 307
Output Parameters . . . 315
Operating-Point Parameters . . . 315

5
BJT Model (bjt) . . . 317
Device Regions . . . 322
DC Current . . . 322
Nonlinear Base Resistance . . . 324
Nonlinear Collector Resistance (If rcv Is Specified) . . . 325
Collector Leakage Current . . . 325
Substrate Leakage Current . . . 326
Charge and Capacitance . . . 326
Excess Phase . . . 327
Temperature Effect . . . 328
Energy Gap . . . 328
Saturation Current . . . 329
Current Gains (B_f, B_r) . . . 332
Junction Capacitors (cjc, cje, and cjs) . . . 334
Parasitic Resistors (rb, rc, and re) . . . 336
Noise Model . . . 337
Base Resistance Thermal Noise . . . 337
Collector Resistance Thermal Noise . . . 337

© 2023 Cadence Design Systems, Inc.

Emitter Resistance Thermal Noise . . . 337
Collector Shot Noise Source . . . 337
Base Shot, Flicker, and Burst Noise Sources . . . 338
Scaling Effects . . . 338
Sample Instance Statement: . . . 338
Sample Model Statement: . . . 338
Instance Definition . . . 339
Instance Parameters . . . 339
Model Definition . . . 339
Model Parameters . . . 339
Shrink Parameters . . . 350
Output Parameters . . . 351
Operating Point Parameters . . . 351

6
HiCUM Model (bht) . . . 353
Spectre HICUM Model Compared to Public HICUM Model . . . 354
Self-Heating . . . 354
Parameter flcomp . . . 354
Model Description . . . 355
DC Equations . . . 356
Charge and Capacitance Equations . . . 359
Noise Model . . . 362
Temperature Effect . . . 363
Self-Heating . . . 364
NQS effect . . . 365
Lateral NQS . . . 365
Vertical NQS . . . 365
HiCUM Model Version 2.2 . . . 367
Temperature Dependent Bandgap Voltage . . . 367
Transfer current . . . 368
Base Currents . . . 369
Depletion Capacitances and Charges . . . 370
Minority Charge . . . 372
Temperature Dependence . . . 373

© 2023 Cadence Design Systems, Inc.

Base-emitter Tunnelling Component . . . 375
Parasitic Base-Emitter Capacitance Partitioning . . . 376
Substrate Transistor . . . 376
HiCUM Model Version 2.3 . . . 377
Improvements in the model equations . . . 377
HiCUM Model Version 2.31 . . . 383
Improvements in Model Equations . . . 383
HiCUM Model Version 2.32 . . . 384
HiCUM Model Version 2.33 . . . 385
HiCUM Model Version 2.34 . . . 385
HiCUM Model Version 2.40 . . . 386
Improvised Strong Collector Avalanche Formula . . . 386
Conditional Statement for Weak Avalanche . . . 387
Backward Compatibility and Application . . . 388
Improvised Vciei Calculation . . . 388
Scaling Effects . . . 389
Component Statements . . . 389

7
HiCUM Level-0 Model (bht0) . . . 403
Model Version Updates . . . 404
Version 1.2: . . . 404
Version 1.3 . . . 404
Version 1.3.1 . . . 404
Version 1.3.2 . . . 405
Equivalent Circuit . . . 406
Charge formulation of the internal transistor . . . 407
Derivation of the simplified transfer current equation . . . 408
Static Base Current Components . . . 411
Depletion Charges And Capacitances . . . 411
Minority Charges And Capacitances . . . 412
Low current densities . . . 412
Medium and high current densities . . . 412
Series Resistance . . . 413
Internal base resistance . . . 413

© 2023 Cadence Design Systems, Inc.

External series resistances . . . 414
Temperature Dependence . . . 414
Noise Model . . . 416
DC Characteristics . . . 417
Charge Storage Elements . . . 418
Series Resistance . . . 419
Temperature Effects . . . 419
Noise Model . . . 420
Other Effects . . . 421
Models and Equations in Version 1.30 . . . 421
Improved model formulations for the HICUM/L0 transfer current . . . 421
Component Statements . . . 425
Instance Definition . . . 425
Instance Parameters . . . 425
Model Definition . . . 425
Model Parameters . . . 425
Output Parameters . . . 430
Operating Point Parameters . . . 430

8
VBIC Model (vbic) . . . 433
VBIC 1.1 . . . 435
DC Current . . . 435
Charge Equations . . . 437
Excess Phase . . . 440
Small Signal Parameters . . . 440
Temperature Equations . . . 442
Noise Equations . . . 444
VBIC 1.2 . . . 446
DC Current . . . 446
Charge Equations . . . 448
Temperature Equations . . . 450
Scaling Effects . . . 451
Component Statements . . . 452
Sample Instance Statement . . . 452

© 2023 Cadence Design Systems, Inc.

Sample Model Statement . . . 452
Instance Definition . . . 452
Instance Parameters . . . 453
Model Definition . . . 453
Model Parameters . . . 454
Operating-Point Parameters . . . 463

9
HBT Model (ucsd_hbt) . . . 467
DC Current . . . 468
Junction Capacitance . . . 470
Total Charge . . . 471
Thermal Current Equations . . . 474
Temperature Equations . . . 474
Scaling Effects . . . 476
Component Statements . . . 477

10
HBT Model (version 2) . . . 489
Component Statements . . . 490

11
JFET Model (jfet) . . . 499
Drain Current for the Subthreshold Region . . . 500
Drain Current for the Triode Region . . . 501
Drain Current for the Saturation Region . . . 501
Substrate Leakage Currents . . . 502
Gate Junction Currents . . . 502
Gate Junction Capacitance . . . 503
Temperature Effect . . . 503
Noise Model . . . 505
Scaling Effects . . . 506
Component Statements . . . 506

© 2023 Cadence Design Systems, Inc.

12
Philips Models

Philips Models . . . 515
Diode Level 500 (dio500) . . . 517
Lateral PNP Transistor (bjt301) . . . 520
Lateral PNP Transistor (bjt500) . . . 526
Lateral PNP Transistor (bjt500t) . . . 533
Vertical NPN/PNP Transistor (bjt503) . . . 541
Compact Bipolar-Transistor Model (bjt504) . . . 549
Compact Bipolar-Transistor Model (bjt504t) . . . 560
Compact Bipolar-Transistor Model (bjt505) . . . 571
Compact Bipolar-Transistor Model (bjt505t) . . . 583
Compact Bipolar-Transistor Model (bjtd504) . . . 595
Compact Bipolar-Transistor Model (bjtd504t) . . . 605
Compact Bipolar-Transistor Model (bjtd505) . . . 615
Compact Bipolar-Transistor Model (bjtd505t) . . . 625
Compact Bipolar-Transistor Model (bjtd3500) . . . 635
Compact Bipolar-Transistor Model (bjtd3500t) . . . 646
JFETIDG Model (jfetidg) . . . 656
Terminology and Notation . . . 658
Model Version . . . 660
Component Statements . . . 660
Long Channel JFET/MOSFET Model (mos30) . . . 673
MOS Model 40, Level 40 (mos40t) . . . 678
Long Channel JFET/MOSFET Model (mos3002) . . . 683
Compact MOS-Transistor Model (mos705) . . . 686
Compact MOS-Transistor Model (mos902) . . . 694
Compact MOS-Transistor Model (mos903) . . . 706
Compact MOS-Transistor Distortion Model (mos1000) . . . 717
Compact MOS-Transistor Distortion Model (mos1100) . . . 726
Compact MOS-Transistor Distortion Model (mos1100e) . . . 737
MOS Model 11, Level 1101 (mos11010) . . . 745
MOS Model 11, Level 1101 (mos11010t) . . . 755
MOS Model 11, Level 1101 (mos11011) . . . 765
MOS Model 11, Level 1101 (mos11011t) . . . 780
MOS Model 11, Level 1101 (mos1101e) . . . 795

© 2023 Cadence Design Systems, Inc.

MOS Model 11, Level 1101 (mos1101et) . . . 803
MOS Model 11, Level 1102 (mos11020) . . . 811
MOS Model 11, Level 1102 (mos11020t) . . . 821
MOS Model 11, Level 1102 (mos11021) . . . 833
MOS Model 11, Level 1102 (mos11021t) . . . 848
MOS Model 11, Level 1102 (mos1102e) . . . 862
MOS Model 11, Level 1102 (mos1102et) . . . 870
Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001) . . . 877
Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e) . . . 885
Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et) . . . 893
Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t) . . . 901
Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002) . . . 910
Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e) . . . 919
Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et) . . . 927
Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t) . . . 936
MOS Model 31, Level 3100 (mos3100) . . . 945
MOS Model 31, Level 3100 (mos3100t) . . . 949

13
Common MOSFET Equations . . . 955
Parameters Common to BSIM1 and BSIM2 Models . . . 956
Channel Width and Length . . . 956
Parameters Common to Levels 1-3 Only . . . 956
Source/Drain Bulk Junction Models . . . 958
Junction Leakage Current . . . 958
Bulk-Junction Bottom (Sidewall) Capacitance . . . 960
Drain and Source Area . . . 960
Drain and Source Perimeters . . . 961
Drain and Source Squares . . . 962
Junction Saturation Current . . . 963
Junction Capacitance . . . 963
Drain and Source Parasitic Resistance . . . 963
Temperature Effect on Model Parameters . . . 967
Mobility and Transconductance Parameters . . . 968
Energy Band Gap . . . 968

© 2023 Cadence Design Systems, Inc.

Surface Potential . . . 969
Built-in Voltage of Source/Drain Junctions . . . 970
Junction Leakage Currents . . . 972
Junction Capacitances . . . 972
Channel Length Modulation . . . 975
Threshold Voltage . . . 975
Drain and Source Parasitic Resistance . . . 976
Critical Field . . . 976
Noise Model . . . 978
Drain Resistance Thermal Noise . . . 978
Source Resistance Thermal Noise . . . 978
Channel Thermal and Flicker Noise . . . 978

14
MOS Capacitance Model . . . 981

Modified Meyer Model . . . 982
Accumulation Region . . . 983
Subthreshold Region . . . 983
Saturation Region . . . 984
Triode Region . . . 985
Yang-Chatterjee Model . . . 987
Accumulation Region . . . 988
Subthreshold Region . . . 988
Saturation Region . . . 989
Triode Region . . . 990
BSIM Charge Model with 0/100 Partitioning (xpart=1) . . . 992
BSIM Charge Model with 40/60 Partitioning (xpart=0) . . . 992
Accumulation Region . . . 993
Subthreshold Region . . . 993
Saturation Region . . . 994
Triode Region . . . 996
BSIM Charge Model with 50/50 Partitioning (xpart=0.5) . . . 998
Accumulation Region . . . 999
Subthreshold Region . . . 999
Saturation Region . . . 999

© 2023 Cadence Design Systems, Inc.

Triode Region . . . 1001
Scaling Effects . . . 1002

15
MOS Level-1 Model (mos1) . . . 1005
Channel Width and Length . . . 1006
Threshold Voltage . . . 1007
Drain Saturation Voltage . . . 1007
Drain Current for the Subthreshold Region . . . 1007
Drain Current for the Triode Region . . . 1008
Drain Current for the Saturation Region . . . 1009
Drain Saturation Voltage (Modified Level-1 Model) . . . 1009
Drain Current for the Triode Region (Modified Level-1 Model) . . . 1010
Drain Current for the Saturation Region (Modified Level-1 Model) . . . 1010
Substrate Current . . . 1011
Scaling Effects . . . 1011
Component Statements . . . 1011

16
MOS Level-2 Model (mos2) . . . 1025
Channel Width and Length . . . 1026
Threshold Voltage . . . 1027
Drain Saturation Voltage . . . 1028
Drain Current for the Subthreshold Region . . . 1029
Drain Current for the Triode Region . . . 1030
Drain Current for the Saturation Region . . . 1031
Substrate Current . . . 1032
Scaling Effects . . . 1032
Component Statements . . . 1032

17
MOS Level-3 Model (mos3) . . . 1047
Channel Width and Length . . . 1048
Threshold Voltage . . . 1049

© 2023 Cadence Design Systems, Inc.

Drain Saturation Voltage . . . 1050
Drain Current for the Subthreshold Region . . . 1051
Drain Current for the Triode Region . . . 1052
Drain Current for the Saturation Region . . . 1052
Substrate Current . . . 1053
Scaling Effects . . . 1054
Component Statements . . . 1054

18
BSIM1 Level-4 Model (bsim1) . . . 1073
Parameter Calculation . . . 1075
Drain Current Model . . . 1076
Scaling Effects . . . 1080
Component Statements . . . 1080

19
BSIM2 Level-5 Model (bsim2) . . . 1107
Parameter Calculation . . . 1110
Drain Current Model . . . 1110
Drain Current for the Subthreshold Region . . . 1112
Drain Current for the Triode Region . . . 1113
Scaling Effects . . . 1116
Component Statements . . . 1116

20
BSIM3v2 Level-10 Model (bsim3) . . . 1145
Threshold Voltage . . . 1146
Subthreshold Current . . . 1147
Drain Saturation Voltage . . . 1150
Drain Current for the Saturation Region . . . 1152
Default Model Parameter Value Calculation . . . 1154
Scaling Effects . . . 1158
New Features in BSIM3 Version 3.2.4 . . . 1158
Component Statements . . . 1158

© 2023 Cadence Design Systems, Inc.

21
BSIM3v3 Level-11 Model (bsim3v3) 1177

Spectre-Specific Parameters 1178
- Instance Parameters 1178
- Model Parameters 1179

Drain and Source Area 1182
Drain and Source Perimeters 1182
Drain and Source Parasitic Resistance 1182
I-V Model 1184
- Threshold Voltage 1184
- Effective Vgs-Vthc 1185
- Mobility 1186
- Drain Saturation Voltage 1187
- Effective Vds 1188
- Drain Current Expression 1188
- Substrate Current 1190
- Junction Saturation Current 1190
- Polysilicon Depletion Effect 1191
- Effective Channel Length and Width 1191
- Drain/Source Resistance 1192
- Temperature Effects 1193

Capacitance Model 1194
- Dimension Dependence 1194
- Junction Capacitance 1195
- Overlap Capacitance (for NMOS) 1195
- Intrinsic Charges 1199
- Intrinsic Capacitances (with Body Bias and DIBL) 1217

Nonquasi-static (NQS) Model 1219
SPICE3 Junction Diode Model 1220
Flicker Noise 1221
- For noimod = 1 and 4 1221
- For noimod = 2 and 3 1221

Channel Thermal Noise 1223
Default Model Parameter Value Calculation 1224
Gate Leak Currents 1227

© 2023 Cadence Design Systems, Inc.

Instance Parameters . . . 1227
Model Parameters . . . 1227
Leak current between Gate and Drain . . . 1227
Leak current between Gate and Source . . . 1228
Igs and Igd . . . 1230
Igb . . . 1230
LOD Model . . . 1232
Stress Effect . . . 1233
Well Proximity Effect . . . 1234
Differences between BSIM3v3 Subversions . . . 1236
Parameter Differences between BSIM3v3 Levels . . . 1239
Scaling Effects (BSIM3v3) . . . 1241
Instance Parameters . . . 1241
Component Statements . . . 1242
Binning Parameters . . . 1279

22
BSIM4 Level-14 Model (bsim4) . . . 1291

Instance . . . 1293
Instance syntax . . . 1293
Model . . . 1293
Model syntax . . . 1293
Auto Model Selection . . . 1293
Equivalent Circuit . . . 1294
Device Regions . . . 1294
Global Control Options . . . 1295
JUNCAP Model . . . 1296
TMI 1.0 Model . . . 1296
TMI 2.0 Model . . . 1296
Flexible device topology with customized model formulations . . . 1297
Support for reliability aging modeling and analysis for simulators with and without aging capability . . . 1297
Model Version Update . . . 1297
Version 4.30 . . . 1297
Version 4.40 . . . 1298

© 2023 Cadence Design Systems, Inc.

Version 4.50 . . . 1298
Version 4.60 . . . 1298
Version 4.61 . . . 1299
Version 4.62 . . . 1299
Version 4.63 . . . 1300
Version 4.64 . . . 1300
Version 4.65 . . . 1300
Version 4.70 . . . 1300
Version 4.80 . . . 1301
Version 4.81 . . . 1302
Model Equations . . . 1302
Effective Oxide Thickness, Channel Length and Channel Width . . . 1302
Threshold Voltage Model . . . 1306
Channel Charge and Subthreshold Swing Models . . . 1307
Gate Direct Tunneling Current Model . . . 1307
Drain Current Model . . . 1309
Body Current Model . . . 1317
Capacitance Model . . . 1319
High Speed/RF Models . . . 1332
Noise Models . . . 1339
Asymmetric MOS Junction Diode Models . . . 1343
Layout Dependent Parasitics Models . . . 1351
Temperature Effects Models . . . 1353
Stress Effects Models . . . 1360
Well Proximity Effect Model . . . 1363
TMIBSIM4 Model (tmibsim4) . . . 1363
Models and Equations in Version Updates . . . 1364
BSIM4 Version 4 . . . 1364
BSIM4 Version 5 . . . 1367
Mobility Model . . . 1367
Scalable Substrate Resistance Model . . . 1368
Temperature Dependence for VOFF, VFBSDOFF . . . 1369
New Temperature Mode (TempMod = 2) . . . 1369
DELVTO: An Instance Parameter . . . 1370
Well-Proximity Effect Modeling . . . 1370
Gate Current Vbs Dependence . . . 1371

© 2023 Cadence Design Systems, Inc.

BSIM4 Version 6 . . . 1371
GISL and GIDL Leakage Module . . . 1371
Junction Diode I-V . . . 1371
Gate Tunneling Current . . . 1372
Mobility Model . . . 1372
Improvement to NOIMOD = 2 . . . 1373
BSIM4 Version 6.1 . . . 1373
C-V Model . . . 1373
New Material Model . . . 1373
Improved Mobility Model . . . 1376
Improved GIDL/GISL Model . . . 1376
BSIM4 Version 6.2 . . . 1377
Width Dependent TAT Model . . . 1377
High K Mobility . . . 1378
BSIM4 Version 7.0 . . . 1380
GIDL/GISL Model . . . 1380
DIBL/Rout Model . . . 1380
Temperature Dependence of Subthreshold Leakage Current . . . 1381
New Model Selector for MTRLMOD=0 and MTRLMOD=1 Compatibility . . . 1382
Enhanced Thermal Noise Model . . . 1382
Mobility Models . . . 1384
Component Statements . . . 1384

23
BSIM6 Model (bsim6) . . . 1439
Instance . . . 1440
Instance Syntax . . . 1440
Model . . . 1440
Model Syntax . . . 1440
TMI Support . . . 1441
OMI Support . . . 1441
Version Update and Enhancements . . . 1442
Version 107 Enhancements . . . 1442
Version 106.2 Enhancements . . . 1443
Version 6.1.1 Enhancements . . . 1445

© 2023 Cadence Design Systems, Inc.

Model Equations . . . 1446
Effective Channel Length and Width . . . 1446
Binning Calculations . . . 1447
Global Geometrical Scaling . . . 1447
Terminal Voltages . . . 1447
Pinch-Off Potential and Normalized Charge Calculation . . . 1449
Short Channel Effects . . . 1450
Drain Saturation Voltage . . . 1450
Mobility Degradation with Vertical Field . . . 1452
Parasitic Series Resistance . . . 1452
Output Conductance . . . 1454
Velocity Saturation . . . 1455
Effective Mobility . . . 1455
Drain Current Model . . . 1455
Impact Ionization Model . . . 1455
GIDL/GISL Current Model . . . 1456
Gate Tunneling Current Model . . . 1456
Equations for Tunneling Currents . . . 1456
Gate Resistance and Body Resistance Model . . . 1458
Substrate Resistance Network . . . 1459
Noise Modeling . . . 1460
Self Heating Model . . . 1469
Asymmetric MOS Junction Diode Models . . . 1469
Layout Dependent Parasitic Models . . . 1471
Temperature Dependence Models . . . 1474
Stress Effect Model Development . . . 1476
Well Proximity Effect Model . . . 1477
C-V Model . . . 1477
Component Statements for BSIM6 . . . 1481
Instance Parameters . . . 1482
Model Definition . . . 1484
Model Parameters . . . 1485
Output Parameters . . . 1564

© 2023 Cadence Design Systems, Inc.

24
PSP102 Model

PSP102 Model . . . 1565
Model Usage . . . 1566
Instance Syntax . . . 1566
Model Syntax . . . 1566
Version and Master Name . . . 1566
Sample Model Statements . . . 1567
History and Development . . . 1568
PSP100 . . . 1568
PSP101 (SiMKit2.3) . . . 1568
PSP102.0 (SiMKit2.3.2) . . . 1568
PSP102.1 (SiMKit2.4) . . . 1569
PSP102.1.1 (SiMKit2.5) . . . 1569
PSP102.2 . . . 1569
PSP102.2.1 (SiMKit4.0.1) . . . 1570
PSP102.3 (SiMKit3.1.2) . . . 1570
PSP102.3.2 (SiMKit3.2) . . . 1570
PSP102.3.3 (SiMKit3.3) . . . 1571
PSP102.3.4 (SiMKit3.4) . . . 1571
PSP102.4 (SiMKit4.01) . . . 1571
PSP102.5 . . . 1572
Structure of PSP102 . . . 1572
Geometrical Scaling and Stress Model for Intrinsic MOSFET . . . 1575
Geometrical Scaling Rules . . . 1575
Calculation of Geometry-Dependent Parameters using Physical Scaling Rules . . . 1577
Parameter Modification due to Stress Effects . . . 1582
Model Equations . . . 1590
Calculation of Internal Parameters (including Temperature Scaling) . . . 1590
Conditioning of Terminal Voltages . . . 1595
Bias-Dependent Body Factor . . . 1595
Lateral Gradient Factor . . . 1596
Surface Potential at Source Side and Related Variables . . . 1597
Drain Saturation Voltage . . . 1599
Surface Potential at Drain Side and Related Variables . . . 1601
Mid-Point Surface Potential and Related Variables . . . 1603

© 2023 Cadence Design Systems, Inc.

Polysilicon Depletion . . . 1603
Potential Mid-Point Inversion Charge and Related Variables . . . 1604
Series Resistance . . . 1605
Mobility Reduction . . . 1605
Drain-Source Channel Current . . . 1605
Impact Ionization or Weak-Avalanche . . . 1607
Gate Current . . . 1610
Noise Model . . . 1616
Non-Quasi-Static (NQS) RF Model . . . 1619
Parasitics Circuit . . . 1620
Additional NQS and RF Parameters . . . 1621
Geometrical Scaling Rules for the NQS RF Model . . . 1621
Equations for the NQS RF Model . . . 1622
Component Statements for PSP102 Models . . . 1630
PSP MOSFET Model (PSP102) . . . 1630
PSP MOSFET Model (psp1020) . . . 1672
PSP MOSFET Model (psp1021) . . . 1696
PSP local MOSFET Model (psp102e) . . . 1724
PSP NQS MOSFET Model (pspnqs1020) . . . 1745
PSP NQS MOSFET Model (pspnqs1021) . . . 1770
PSP NQS local MOSFET Model (pspnqs102e) . . . 1798

25
PSP103 Model . . . 1819

Model Usage . . . 1821
Instance Syntax . . . 1821
Model Syntax . . . 1821
Model History and Development . . . 1822
PSP103.0 (SiMKit3.2) . . . 1822
PSP103.1 (SiMKit3.3) . . . 1822
PSP103.1.1 (SiMKit3.4) . . . 1822
PSP103.2 (SiMKit4.0.1) . . . 1823
PSP103.3 . . . 1823
PSP103.4 . . . 1824
PSP103.5 . . . 1824

© 2023 Cadence Design Systems, Inc.

PSP103.6 . . . 1824
PSP103.7 . . . 1825
Reference . . . 1825
Model Description . . . 1825
Geometry Scaling and Stress Model for Intrinsic MOSFET . . . 1825
PSP 103 Model Equations . . . 1855
Current Model . . . 1863
Charge Model . . . 1884
Noise Model . . . 1887
Self Heating . . . 1890
Non-quasi-static RF model . . . 1891
PSP NQS MOSFET Model (pspnqs103) . . . 1976

26
PSP-Based MOS Varactor Model (mosvar) . . . 2053
Device Structure . . . 2053
Model Equations . . . 2055
RC Circuit Model for Inversion Charge . . . 2055
Parameter Initializing . . . 2055
Static Evaluations . . . 2065
Calculation of Surface Potential at the Channel Side . . . 2066
Calculation of Surface Potential at the Overlap Regions . . . 2069
Surface Potential Without Poly Effect . . . 2071
Surface Potential With Poly Effect . . . 2071
Static Inversion Charge Calculations . . . 2071
Time-Dependent Silicon Surface Potential Without Poly Effect . . . 2074
Time-Dependent Poly Surface Potential Calculation Correction . . . 2074
Quantum Mechanical Corrections . . . 2075
Accumulation Resistance Bias Dependence . . . 2076
Calculation of Gate Tunneling Current . . . 2076
Gate Tunneling Current . . . 2078
Terminal Currents . . . 2079
Terminal Charges . . . 2079
Noise . . . 2080
Parameter Extraction . . . 2081

© 2023 Cadence Design Systems, Inc.

Auxiliary Equations . . . 2083
Model Version Updates . . . 2084
Version 1.2.0 . . . 2084
Version 1.3.0 . . . 2084
Model Usage . . . 2085
Instance Syntax . . . 2085
Model Syntax . . . 2085
Component Statements . . . 2085

27
EKV MOSFET Model (ekv) . . . 2091
Coherence of Static and Dynamic Models . . . 2091
Bulk Reference and Symmetry . . . 2092
Equivalent Circuit . . . 2093
Model Equations . . . 2094
Static Intrinsic Model . . . 2094
Quasi-static Model . . . 2106
Nonquasi-static (NQS) Model . . . 2109
Intrinsic Noise Model . . . 2111
Model Usage . . . 2113
Instance Syntax . . . 2113
Model Syntax . . . 2113
Component Statements . . . 2113
Instance Parameters . . . 2114
Model Parameters . . . 2114

28
EKV3 MOSFET Model (ekv3) . . . 2125
Modes . . . 2126
Model Equations . . . 2129
Instance Level . . . 2129
Effective Geometry . . . 2129
Matching . . . 2129
Long and wide channel correction of VTO and GAMMA . . . 2130
Parameter width and length scaling . . . 2130

© 2023 Cadence Design Systems, Inc.

Reverse short channel effect (RSCE) . . . 2131
Inverse narrow width effect (INWE) . . . 2131
Mobility Scaling . . . 2132
Instance level parameters . . . 2132
Temperature scaling . . . 2132
Normalizing . . . 2133
Slope factor nQ0 . . . 2133
Quantum mechanic effect . . . 2134
Normalization factor for charges . . . 2134
Normalization of potentials . . . 2134
Charge sharing effect . . . 2135
Flat-band voltage . . . 2135
Effective gate-voltage . . . 2136
Pinch-off surface potential . . . 2136
Pinch-off voltage . . . 2137
Velocity saturation . . . 2137
Normalized drain inversion charge . . . 2138
Slope factor n_v . . . 2138
Drain induced barrier lowering effect . . . 2139
Normalized source inversion charge . . . 2139
Slope factor n_Q . . . 2140
Charge model . . . 2140
Mobility effects . . . 2142
Specific current . . . 2143
Denormalizing . . . 2143
Edge Conductance . . . 2144
Normalization Factors (Edge Device) . . . 2144
Scaling - Normalizing . . . 2144
Normalized Inversion Charges (Edge Device) . . . 2144
Normalized Currents (Edge Device) . . . 2145
Drain Current (Edge Device) . . . 2145
Edge Device: Charge Model . . . 2145
Overlap Capacitances . . . 2146
Denormalizing (Overlap) . . . 2148
Fringing Capacitance . . . 2149
Bias-Independent Overlap Capacitances . . . 2149

© 2023 Cadence Design Systems, Inc.

Gate Induced Drain and Source Current . . . 2149
Gate Current . . . 2150
Overlap Gate Current . . . 2152
Impact Ionization Current . . . 2153
Noise . . . 2153
Thermal Noise . . . 2153
Flicker Noise . . . 2154
Induced Gate Noise . . . 2154
Shot and Flicker Gate Noise . . . 2155
Diodes . . . 2156
Temperature Dependence . . . 2156
Area and Perimeter . . . 2157
Junction Current . . . 2158
Junction Capacitance . . . 2158
External Resistors (Gate, Series, Bulk) . . . 2159
Temperature Dependence . . . 2161
Model Usage . . . 2162
Instance Syntax . . . 2162
Model Syntax . . . 2162
Component Statements . . . 2163
Device ekv3_nqs (ekv3_nqs) . . . 2180
Device ekv3_r4 (ekv3_r4) . . . 2198
Device ekv3_rf (ekv3_rf) . . . 2215
Device ekv3_s (ekv3_s) . . . 2233

29
BSIMSOI MOSFET Model (bsimsoi) . . . 2253
Device Structure . . . 2254
Equivalent Circuit . . . 2255
Device Regions . . . 2256
Global Control Options . . . 2256
Model Equations . . . 2258
DC current . . . 2258
Body current . . . 2259
Leakage current . . . 2262

© 2023 Cadence Design Systems, Inc.

Charge and Capacitance . . . 2265
Selfheating . . . 2269
RF model . . . 2270
Noise . . . 2272
Model Version Updates . . . 2277
Version 3.2 . . . 2277
Version 4.0 . . . 2277
Version 4.1 . . . 2278
Version 4.2 . . . 2278
Version 4.3 . . . 2279
Version 4.31 . . . 2279
Version 4.4 . . . 2279
Version 4.5 . . . 2279
Version 4.6.0 . . . 2280
Version 4.6.1 . . . 2281
Special Bugfixes . . . 2281
Rth thermal resistance . . . 2281
Cth thermal capacity . . . 2281
ExpVgst bug handling . . . 2281
Temperature node tolerance and quantity . . . 2282
I_{ji} (substrate current) . . . 2282
Bugfix control methodology . . . 2282
TMI Support . . . 2283
Model Usage . . . 2284
Instance Syntax . . . 2284
Model Syntax . . . 2284
Component Statements . . . 2285
Instance Parameters . . . 2286
Model Parameters . . . 2289

30
HiSIM2 Model (hisim2) . . . 2359
Model Concepts . . . 2361
Model Usage . . . 2362
Instance Syntax . . . 2362

© 2023 Cadence Design Systems, Inc.

Model Syntax . . . 2362
Model Version and Development . . . 2362
Version Update and Enhancement . . . 2363
Version 3.2.1 Enhancement . . . 2363
Version 3.1.1 Enhancement . . . 2364
Version 3.1.0 Enhancement . . . 2364
Version 3.0.0 Enhancement . . . 2365
Version 2.91 Enhancement . . . 2365
Version 2.90 Enhancement . . . 2365
Version 2.80 Enhancement . . . 2366
Version 2.70 Enhancement . . . 2366
Version 2.61 Enhancement . . . 2367
Version 2.60 Enhancement . . . 2367
Reference . . . 2368
Model Equations . . . 2368
Component Statements . . . 2406

31
HISIM_HV Model (hisim_hv) . . . 2441
Model Concepts . . . 2443
Model Usage . . . 2446
Instance Syntax . . . 2446
Model Syntax . . . 2447
Model Version and Development . . . 2447
Version Update and Enhancement . . . 2449
Version 2.41 Enhancement . . . 2449
Version 2.40 Enhancement . . . 2450
Version 2.33 Enhancement . . . 2451
Version 2.32 Enhancement . . . 2451
Version 2.31 Enhancement . . . 2451
Version 2.30 Enhancement . . . 2452
Version 2.20 Enhancement . . . 2452
Version 1.24 Enhancement . . . 2454
Version 2.10 Enhancement . . . 2454
Version 2.01 Enhancement . . . 2455

© 2023 Cadence Design Systems, Inc.

Version 1.23 Enhancement . . . 2455
Version 2.00 Enhancement . . . 2455
Version 1.22 Enhancement . . . 2457
Version 1.12 Enhancement . . . 2458
Version 1.21 Enhancement . . . 2458
Version 1.20 Enhancement . . . 2458
Reference . . . 2460
Model Equations . . . 2460
Component Statements . . . 2477

32
HISIM_SOI Model (hisimsoi) . . . 2531
Model Concepts . . . 2532
Model Usage . . . 2533
Version Update and Enhancements . . . 2535
Version 1.50 Enhancements . . . 2535
Version 1.40 Enhancements . . . 2536
Version 1.30 Enhancements . . . 2536
Reference . . . 2537
Model Equations . . . 2537
Component Statements . . . 2553

33
HiSIM_IGBT Model (hisim_igbt) . . . 2565
Model Concepts . . . 2566
Model Usage . . . 2567
Instance Syntax . . . 2567
Model Syntax . . . 2567
Sample Model Statement . . . 2567
Component Statements . . . 2568

34
HiSIM_Diode Model (hisim_diode) . . . 2609
Model Usage . . . 2610

© 2023 Cadence Design Systems, Inc.

Instance Syntax . . . 2610
Model Syntax . . . 2610
Component Statements . . . 2611
Instance Parameters . . . 2611
Model Parameters . . . 2611

35
Surface Potential Based Compact MOSFET Model (spmos) .

2615

Equivalent Circuit . . . 2617
Core Model . . . 2617
Lateral Gradient Factor . . . 2617
Effective Drain-Source Voltage . . . 2618
Surface Potential . . . 2619
Quantum Mechanical Corrections . . . 2624
Polysilicon Depletion . . . 2626
Drain Current . . . 2628
Intrinsic Charges . . . 2629
Bias-Dependent Body Factor . . . 2630
Extrinsic Model . . . 2630
Charge Model . . . 2633
Gate Current Model . . . 2634
Substrate Current Model . . . 2637
Total Terminal Currents . . . 2638
Noise Model . . . 2638
Gate Induced Drain/Source Leakage Current Model . . . 2641
Scaling Equations . . . 2642
Temperature Dependence (-55°°° to 150°°°) . . . 2645
Parameter Descriptions . . . 2647
New Parameters for SPMOS Version 34 . . . 2653
Parameters with Different Default Values for SPMOS Version 34 . . . 2655

© 2023 Cadence Design Systems, Inc.

36
MOS Level-0 Transistor (mos0) 2657

37
MOS Level-15 Transistor (mos15) 2661

38
GaAs Model (gaas) 2671
Model Equations 2672
Drain Current for the Subthreshold Region 2672
Drain Current for the Triode Region 2673
Drain Current for the Saturation Region 2673
Gate Junction Currents 2673
Gate Junction Capacitance 2675
Temperature Effect 2676
Noise Model 2678
Scaling Effects 2679
Component Statements 2680
Instance 2680
Model 2681

39
TriQuint Owned Models (tom2 and tom3/tom3v1) 2685
Circuit Diagrams 2685
TOM2 2685
TOM3 2686
Model Equations 2687
Channel Current Ids 2687
TOM2 2687
TOM3/TOM3V1 2688
Gate Current Ig 2689
TOM2 2689
TOM3/TOM3V1 2689

© 2023 Cadence Design Systems, Inc.

Gate Capacitance . . . 2690
TOM2 . . . 2690
TOM3/TOM3V1 . . . 2692
TOM3V1 . . . 2695
Temperature Effect . . . 2695
TOM2 . . . 2696
TOM3/TOM3V1 . . . 2696
Noise Model . . . 2696
Source Resistance Thermal Noise . . . 2696
Drain Resistance Thermal Noise . . . 2696
Channel Conductance Thermal and Flicker Noise . . . 2697
Gate Resistance Thermal Noise (TOM3V1) . . . 2697
Channel Conductance Thermal and Flicker Noise (TOM3V1) . . . 2697
Scaling Effects . . . 2698
New features from TOM3 to TOM3v1 . . . 2698
Model Usage (tom2) . . . 2699
Instance Syntax . . . 2699
Model Syntax . . . 2699
Component Statements . . . 2701
GaAs MESFET (tom3) . . . 2705
GaAs MESFET (TOM3V1) . . . 2710

40
RPI TFT Models . . . 2715
Poly-Si TFT Model (PSITFT) . . . 2717
Equivalent Circuit . . . 2717
Model Features . . . 2717
Channel Width and Length . . . 2718
Drain and Source Parasitic Resistance . . . 2718
Threshold Voltage . . . 2720
Effective Mobility . . . 2720
Unified Electron Sheet Charge Density Per Unit Area . . . 2721
Channel Conductance . . . 2722
Saturation Voltage . . . 2722
Channel Current . . . 2723

© 2023 Cadence Design Systems, Inc.

Kink Effect Current . . . 2724
Subthreshold Leakage Current . . . 2725
Parasitic Resistance Dependence . . . 2727
Gate-Drain/Source Resistance . . . 2728
Temperature Dependence . . . 2728
Capacitance . . . 2729
ACM Option . . . 2735
Scaling Effects . . . 2736
Component Statements . . . 2736
Amorphous-Si TFT Model (ATFT) . . . 2744
Equivalent Circuit . . . 2744
Model Features . . . 2744
Drain Current . . . 2746
Drain and Source Parasitic Resistance . . . 2748
Temperature Dependence . . . 2751
Capacitance . . . 2751
Component Statements . . . 2752

41
Three-Terminal Nonlinear (Diffused and Poly-Silicon) Resistor Model and JFET Model (r3) . . . 2759
Usage . . . 2760
Bias Dependence of Resistor Body Current . . . 2761
. . . Bias Dependence of Parasitics 2765
Geometry Dependence . . . 2766
. . . Temperature Dependence 2771
Noise . . . 2774
Operating Point Information . . . 2776
Statistical Variation . . . 2776
Notes on Parameter Extraction . . . 2779
Reference . . . 2786
Component Statements . . . 2786

© 2023 Cadence Design Systems, Inc.

42
IGBT0 Model (igbt0) 2793

Model Concepts 2794
Component Statements 2796
- Instance Syntax 2796
- Model Syntax 2796

Reference 2797
- Model Equations 2797

43
Distributed Components 2803

Microstrip Line (msline) 2804
- Instance Syntax 2804
- Instance Parameters 2804

Multi-Conductor Transmission Line (mtline) 2805
- Constant RLGC Matrices 2805
- Skin Effect and Dielectric Loss 2806
- Frequency-Dependent RLGC Data 2807
- 2-D Field Solver Information 2808
- Line Configuration (linetype) 2808
- Model Type (modeltype) 2808
- Ground Plane (numgnd) 2809
- Dielectric Layer (numlayer) 2809
- Signal Line 2809
- RLGC Reuse 2810
- Stackup-based Input of Cross-section Geometry and Material Properties 2810
- S-Parameter Data File 2811
- Old TLINE Parameters 2811
- Sample Instance Statement 2812
- Sample Model Statement 2813
- Rational Fitting 2821
- Modeling Frequency Dependent Effects 2821

Delay Line (delay) 2822
- Related Topics 2822

© 2023 Cadence Design Systems, Inc.

Four Terminal Relay (relay) . . . 2823
Related Topics . . . 2825
Linear Two Winding Ideal Transformer (transformer) . . . 2826
Related Topics . . . 2827

44
Other Models . . . 2829

High-Voltage MOSFET Model (hvmos) . . . 2830
MISN Field Effect Transistor (misnan) . . . 2858
Diffusion Resistor Model (rdiff) . . . 2867

45
BSIM-CMG . . . 2871

Model Overview . . . 2873
TMI Support . . . 2873
OMI Support . . . 2874
BSIM-CMG Model Equations . . . 2875
Bias Independent Calculations . . . 2875
Terminal Voltages . . . 2878
Short Channel Effects . . . 2879
Surface Potential Calculation . . . 2880
Drain Saturation Voltage . . . 2880
Average Potential and Charge . . . 2883
Quantum Mechanical Effects . . . 2884
Mobility Degradation and Series Resistance . . . 2886
Lateral Non-uniform Doping Model . . . 2887
Body Effect Model . . . 2887
Output Conductance . . . 2887
Velocity Saturation . . . 2888
Drain Current Model . . . 2889
Intrinsic Capacitance Model . . . 2889
Parasitic resistances and capacitance models . . . 2891
Impact Ionization and GIDL/GISL Model . . . 2898
Gate Tunneling Current . . . 2900
Non Quasi-static Models . . . 2901

© 2023 Cadence Design Systems, Inc.

Generation-recombination Component . . . 2903
Junction Current and Capacitances . . . 2904
Self-heating Model . . . 2904
Noise Models . . . 2904
Model Version Update . . . 2906
Version 105.02 Update . . . 2906
Version 105.03 update . . . 2906
Version 105.031 update . . . 2907
Version 105.04 update . . . 2908
Version 106.0.0 update . . . 2909
Version 106.1.0 update . . . 2910
Version 107.0.0 update . . . 2911
Version 108.0.0 update . . . 2912
Version 110.0.0 update . . . 2912
Version 111.0.0 update . . . 2914
Component tatements . . . 2915

46
BSIMSOI_S Model . . . 3063
Synopsis . . . 3063
Model Synopsis . . . 3066

47
BSIM-IMG . . . 3149
Model Overview . . . 3151
BSIM-IMG Model Equations . . . 3152
Bias Independent Calculations . . . 3152
Terminal Voltages and Pre-Conditioning . . . 3155
Short Channel Effects . . . 3156
Body Doping Effects . . . 3157
Surface Potential Calculation . . . 3157
Drain Saturation Voltage . . . 3159
Calculate Average Field, Potential, and Charge . . . 3162
Mobility Degradation . . . 3163
Output Conductance . . . 3164

© 2023 Cadence Design Systems, Inc.

Veolocity Saturation . . . 3165
Drain Current Model . . . 3165
C-V Model . . . 3166
Parasitic Resistance and Capacitance Models . . . 3166
Impact Ionization and GIDL/GISL Model . . . 3169
Gate-Induced-Drain/Source-Leakage Current . . . 3170
Gate Tunneling Current . . . 3171
Self Heating Model . . . 3172
Noise Modeling . . . 3173
Model Version Update . . . 3176
Version 102.94 . . . 3176
Version 102.92 . . . 3176
Version 102.90 . . . 3176
Version 102.80 . . . 3177
Version 102.70 . . . 3177
Version 102.61 . . . 3177
Component Statements . . . 3178
Sample Model Statement . . . 3178
Sample Instance Statement . . . 3178

48
Angelov Model . . . 3245

Model Equations . . . 3246
Equivalent Circuit . . . 3246
Ids Equations . . . 3246
Igs and Igd Equations . . . 3249
Temperature Equations . . . 3249
Charge Equations . . . 3250
Excess Phase . . . 3251
Self Heating Model . . . 3252
Noise Model . . . 3252
Igs, Igd Shot Noise and Flicker Noise . . . 3253
Ids Flicker Noise . . . 3254
Thermal Noise . . . 3254
Release History and Version . . . 3255

© 2023 Cadence Design Systems, Inc.

Model Usage . . . 3256
Instance Syntax . . . 3256
Model Syntax . . . 3256
Component Statements . . . 3256
Instance Parameters . . . 3257
Model Parameters . . . 3257

49
Angelov GaN Model . . . 3263

Model Equations . . . 3264
Equivalent Circuit . . . 3264
Ids Equations . . . 3264
Igs and Igd Equations . . . 3268
Temperature Equations . . . 3269
Charge Equations . . . 3269
Excess Phase . . . 3271
Self Heating Model . . . 3272
Noise Model . . . 3272
Igs, Igd Shot Noise and Flicker Noise . . . 3273
Ids Flicker Noise . . . 3274
Thermal Noise . . . 3274
Release History and Version . . . 3275
Model Usage . . . 3276
Instance Syntax . . . 3276
Model Syntax . . . 3276
Component Statements . . . 3276
Instance Parameters . . . 3277
Model Parameters . . . 3277

50
DIODE_CMC Model . . . 3283

Model Equations . . . 3283
Junction Charge . . . 3283
Ideal Current . . . 3284
Ideal Current with High Injection . . . 3284

© 2023 Cadence Design Systems, Inc.

Shockley-Read-Hall current . . . 3285
Trap-Assisted Tunneling Current . . . 3286
Band-to-band tunneling current . . . 3289
Avalanche and Breakdown . . . 3290
Total Current . . . 3290
Thermal Voltage . . . 3290
Band Gap . . . 3291
Intrinsic Carrier Concentration . . . 3291
Saturation Current Density . . . 3292
Determination of Vmax . . . 3292
Built-In Voltages . . . 3293
Determination of VF, min and Vch . . . 3294
Voltage Difference VAK . . . 3294
Final Junction Current . . . 3294
Auxiliary Equations . . . 3295
Model Version and Development . . . 3295
Version Update and Enhancement . . . 3295
Model Usage . . . 3296
Instance Syntax . . . 3296
Model Syntax . . . 3296
Component Statements . . . 3297
Instance Parameters . . . 3297
Model Parameters . . . 3297

51
JFET100 Model . . . 3305

52
UTSOI2 Model . . . 3331
Model Overview . . . 3333
Model Structure . . . 3333
Version Update and Enhancement . . . 3334
Version 2.3.0 Enhancement . . . 3334
Geometrical dependences, stress effects and junction asymmetry . . . 3335
Scaling Equations . . . 3335

© 2023 Cadence Design Systems, Inc.

Stress Model . . . 3344
Asymmetric Junctions . . . 3345
Model Equations . . . 3346
Internal Parameters Including Temperature Dependencies . . . 3346
Terminal Voltage Conditioning . . . 3355
Backplane Depletion . . . 3357
Channel Current . . . 3360
Gate Current, Intrinsic Charges and Overlap Related Variables . . . 3384
Gate Current . . . 3386
Gate Induced Drain/Source Leakage (GIDL/GISL) . . . 3391
Charge Model . . . 3391
Self-Heating . . . 3393
Noise Model . . . 3393
Total Current and Charges . . . 3396
Operating Point Output . . . 3398
Voltages . . . 3398
Component Statements . . . 3398
Model Definition . . . 3398
Instance Definition . . . 3399

53
ASM-HEMT Model . . . 3425

Model Overview . . . 3426
Model Equations . . . 3426
Physical Constants . . . 3426
Voltages Calculation and Pre Conditioning . . . 3427
Temperature Dependence . . . 3429
Surface Potential Calculation . . . 3430
Intrinsic Charge Calculation . . . 3434
Drain Current Model . . . 3436
Self Heating Model . . . 3437
Short Channel Effects . . . 3437
Access Region and Parasitic Resistances . . . 3438
Parasitic Capacitances . . . 3440
Trap Model . . . 3441

© 2023 Cadence Design Systems, Inc.

Gate Current Model . . . 3443
Field Plate Model . . . 3444
Noise Model . . . 3446
Component Statements . . . 3448
Model Definition . . . 3448
Instance Definition . . . 3448

54
MVSG Model . . . 3461
Model Equations . . . 3462
Transistor drain current formulation . . . 3462
Transistor channel charge formulation . . . 3466
Gate current formulation . . . 3468
Charge trapping effects . . . 3468
Device-noise: RF- and phase-noise modeling . . . 3468
Component Statements . . . 3470
Model Definition . . . 3470
Instance Definition . . . 3470

55
Josephson Junction Model (jj) . . . 3483
Model Overview . . . 3484
Equivalent Circuit . . . 3485
Model Equations . . . 3486
Component Statements . . . 3489
Instance . . . 3489
Model . . . 3489

56
LUTSOI Model . . . 3491
Model Structure . . . 3493
Version Update and Enhancements . . . 3494
L-UTSOI 102.7 Enhancements . . . 3494
L-UTSOI 102.6 Enhancements . . . 3495

© 2023 Cadence Design Systems, Inc.

Geometrical dependences, stress effects and junction asymmetry 3496
Scaling Equations 3496
Stress model for SWSTRESS = 1 3508
Stress model for SWSTRESS = 2 3510
Asymmetric junctions 3512
Model Equations 3513
Internal parameters including temperature dependences 3513
Terminal voltage conditioning 3523
Backplane depletion 3524
Channel current 3528
Gate current, intrinsic charges and overlap related variables 3539
Gate current 3542
Gate Induced Drain/Source Leakage (GIDL/GISL) 3546
Impact ionization current 3547
Charge model 3547
Self-heating 3550
Noise model 3550
Total currents and charges 3554
Component Statements 3556
Model Definition 3556
Instance Definition 3556

© 2023 Cadence Design Systems, Inc.

Preface

This manual assumes that you are familiar with the development, design, and simulation of integrated circuits and that you have some familiarity with SPICE simulation.

This manual describes equations and parameters for models supported by the Spectre® circuit simulator.

Spectre is an advanced circuit simulator that simulates analog and digital circuits at the differential equation level. The simulator uses improved algorithms that offer increased simulation speed and greatly improved convergence characteristics over SPICE. Besides the basic capabilities, the Spectre circuit simulator provides significant additional capabilities over SPICE. Verilog®-A uses functional description text files (modules) to model the behavior of electrical circuits and other systems. Spectre RF Simulation Option adds several new analyses that support the efficient calculation of the operating point, transfer function, noise, and distortion of common RF and communication circuits, such as mixers, oscillators, sample holds, and switched-capacitor filters.

This preface discusses the following topics:

? Related Documents on page 52

? Typographic and Syntax Conventions on page 52

© 2023 Cadence Design Systems, Inc.

Related Documents

The following can give you more information about the Spectre circuit simulator and related products:

- The Spectre circuit simulator is often run within the Virtuoso® analog design environment, under the Cadence® design framework II. To see how the Spectre circuit simulator is run under the analog circuit design environment, read the *Cadence Analog Design Environment User Guide.*
- To learn more about specific parameters of components and analyses, consult the Spectre online help (`spectre -h`) or the *Spectre Circuit Simulator Reference* manual.
- For more information about using the Spectre circuit simulator with Verilog-A, see the *Verilog-A Language Reference* manual.
- If you want to see how SpectreRF is run under the analog circuit design environment, read *SpectreRF Simulation Option User Guide*.
- For more information about RF theory, see *SpectreRF Simulation Option Theory*.
- For more information about how you work with the design framework II interface, see *Design Framework II Help*.
- For more information about specific applications of Spectre analyses, see *The Designer's Guide to SPICE & Spectre*[1].

Typographic and Syntax Conventions

This list describes the syntax conventions used for the Spectre circuit simulator.

`literal`	Nonitalic words indicate keywords that you must enter literally. These keywords represent command (function, routine) or option names, file names and paths, and any other sort of type-in commands.
`argument`	Words in italics indicate user-defined arguments for which you must substitute a name or a value. (The characters before the underscore (_) in the word indicate the data types that this argument can take. Names are case sensitive.

1. Kundert, Kenneth S. *The Designer's Guide to SPICE & Spectre.* Boston: Kluwer Academic Publishers, 1995.

© 2023 Cadence Design Systems, Inc.

|	Vertical bars (OR-bars) separate possible choices for a single argument. They take precedence over any other character.
[ ]	Brackets denote optional arguments. When used with OR-bars, they enclose a list of choices. You can choose one argument from the list.
{ }	Braces are used with OR-bars and enclose a list of choices. You must choose one argument from the list.
. . .	Three dots (...) indicate that you can repeat the previous argument. If you use them with brackets, you can specify zero or more arguments. If they are used without brackets, you must specify at least one argument, but you can specify more.

The language requires many characters not included in the preceding list. You must enter required characters exactly as shown.

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

1

Circuit Components

Click these links to view the component statements for the following:

- Current Sources
- Voltage Sources
- Behavioral Source (bsource)
- Independent Resistive Source (port)
- Linear N Port (nport)
- Current Probe (iprobe)
- Circuit Reduced Order Model (cktrom)
- Analog-to-Logic Converter (a2d)
- device checker (assert)
- Logic-to-Analog Converter (d2a)
- Ideal Switch (switch)
- Ratiometric Fourier Analyzer (fourier)
- IBIS I/O buffer (ibis_buffer)

© 2023 Cadence Design Systems, Inc.

Current Sources

Click the following topics to read about the types of current sources:

- Linear Current Controlled Current Source (cccs)
- Linear Current Controlled Voltage Source (ccvs)
- Independent Current Source (isource)
- Polynomial Current Controlled Current Source (pcccs)
- Polynomial Voltage Controlled Current Source (pvccs)
- s-Domain Linear Voltage Controlled Current Source (svccs)
- Linear Voltage Controlled Current Source (vccs)
- z-Domain Linear Current Controlled Current Source (zcccs)
- z-Domain Linear Voltage Controlled Current Source (zvccs)

© 2023 Cadence Design Systems, Inc.

Linear Current Controlled Current Source (cccs)

A current-controlled source senses the current with a probe device. A valid probe is a component instance in the circuit that naturally computes current. For example, probes can be voltage sources (independent or controlled), inductors, transmission lines, microstrip lines, N-ports, and transformers. If the probe device computes more than one current (such as transmission lines, microstrip lines, and N-ports), the index of the probe port through which the controlling current flows needs to be specified. Positive current exits the source node and enters the sink node of the controlled source.

This device can also model ideal digital gates.

This device is supported within altergroups.

Sample Instance Statement

```
vcs (pos gnd) cccs gain=2.5 probe=v1 m=1 //Note that v1 is an instance of a voltage
source
```

Instance Syntax

```
Name  sink  src cccs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

m	1	Multiplicity factor.
probe		Device through which the current that control, flows.
mprobe		mprobe functions the same way as probe except that it devides the input current by the mfactor.
port	0	Index of the probe port through which the controlling current flows.
probes	[...]	Devices through which the current that control, flows. For multi-input digital gates only.
mprobes	[...]	mprobes function the same way as probes except that they devide the input currents by mfactor.
ports	[...]	Indices of the probe ports through which the currents that control, flow. For multi-input digital gates only.
type	cccs	Type of the source.Possible values are cccs, and, nand, or and nor.
delta	0	Smoothing parameter. This may lead to convergency problems. Its value should be in the range between 0 and 0.5, both ends included. The smaller the delta is, the sharper the corner is.

Linear source parameters

gain	0 A/A	Current gain.
td	0.0 s	Time delay.
min	(A)	Minimum output current.

© 2023 Cadence Design Systems, Inc.

max	(A)	Maximum output current.
abs	off	Output current is absolute value if abs is set to on.Possible values are off and on.

PWL source parameters

file		Name of file containing current/current pairs that define the PWL transfer function.
pwl	[...]	Vector of current/current pairs that defines the PWL transfer function. The format of the vector is [in1 out1 in2 out2 ...].
scale	1	Scale factor for the PWL output current.
stretch	1	Scale factor for the PWL controlling current.

Temperature effects parameters

tc1	0 1/C	Linear temperature coefficient.
tc2	0 C^{-2}	Quadratic temperature coefficient.
trise	0.0 K	Temperature rise from ambient.

The Smoothing Factor

The parameter delta is the smoothing factor. When it is nonzero, a curve is introduced to smooth the corner. The value of delta defines the position of the starting and ending points of the curve that is used to smooth the corner. The minimum value 0 means no smoothing curve is introduced. The maximum value 0.5 means the distance between the starting point of the curve and the corner point is half of the shortest distance. The shortest distance is the length of the shortest segment of the piecewise linear function. When there is no shortest segment

© 2023 Cadence Design Systems, Inc.

in the controlling function, that is, only `abs=on` is specified, Spectre uses 1 as the shortest distance.

When `abs=on`, an absolute value is returned and `max` , `min`, and all temperature effct parameters work on their absolute values.

The `port` parameter specifies which current branch of the device specified by parameter `probe` is used as the controlling current flow. If the device specified by `probe` only has one current branch, `port` must be set to `0`, which is also the default value. If there are multiple current branches, then the port specifies the index of the current branch of the device, starting with 0.

Output Parameters

`islinear`

Related Topics

Linear Current Controlled Voltage Source (ccvs)

Independent Current Source (isource)

Circuit Components

Linear Current Controlled Voltage Source (ccvs)

A current-controlled source senses the current with a probe device. A valid probe is a component instance in the circuit that naturally computes current. For example, probes can be voltage sources (independent or controlled), inductors, transmission lines, microstrip lines, N-ports, and transformers. If the probe device computes more than one current (such as transmission lines, microstrip lines, and N-ports), the index of the probe port through which the controlling current flows needs to be specified. Current through the controlled voltage source is calculated and is defined to be positive if it flows from the positive terminal, through the source, to the negative terminal.

This device can also model ideal digital gates.

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

```
vvs (pos gnd) ccvs rm=1 probe=v1 m=1   //Note that v1 is an instance of a voltage
source
```

Instance Syntax

```
Name  p  n ccvs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

m	1	Multiplicity factor.
probe		Device through which the current that control, flows.
mprobe		mprobe functions the same way as probe except that it devides the input current by mfactor.
port	0	Index of the probe port through which the controlling current flows.
probes	[...]	Devices through which the current that control, flows. For multi-input digital gates only.
mprobes	[...]	mprobes function the same way as probes except that they devide the input currents by mfactor.
ports	[...]	Indices of the probe ports through which the currents that control, flow. For multi-input digital gates only.
type	ccvs	Type of the source.Possible values are ccvs, and, nand, or and nor.
delta	0	Smoothing parameter. This may lead to convergency problems. Its value should be in the range between 0 and 0.5, both ends included. The smaller the delta is, the sharper the corner is.

Linear source parameters

rm	0 Ω	Transresistance.
td	0.0 s	Time delay.
min	(V)	Minimum output voltage.

© 2023 Cadence Design Systems, Inc.

max	(V)	Maximum output voltage.
abs	off	Output voltage is absolute value if abs is set to on.Possible values are off and on.

PWL source parameters

file		Name of file containing current/voltage pairs that define the PWL transfer function.
pwl	[...]	Vector of current/voltage pairs that defines the PWL transfer function. The format of the vector is [in1 out1 in2 out2 ...].
scale	1	Scale factor for the PWL output voltage.
stretch	1	Scale factor for the PWL controlling current.

Temperature effects parameters

tc1	0 1/C	Linear temperature coefficient.
tc2	0 C^{-2}	Quadratic temperature coefficient.
trise	0.0 K	Temperature rise from ambient.

The Smoothing Factor

The parameter delta is the smoothing factor. When it is nonzero, a curve is introduced to smooth the corner. The value of delta defines the position of the starting and ending points of the curve that is used to smooth the corner. The minimum value 0 means no smoothing curve is introduced. The maximum value 0.5 means the distance between the starting point of the curve and the corner point is half of the shortest distance. The shortest distance is the length of the shortest segment of the piecewise linear function. Or, when there is no shortest

© 2023 Cadence Design Systems, Inc.

segment in the controlling function, i.e. only `abs=on` is specified, spectre uses 1 as the shortest distance.

Output Parameters

`islinear`

Related Topics

Linear Current Controlled Current Source (cccs)

Independent Current Source (isource)

Current Sources

Circuit Components

Independent Current Source (isource)

The value of the DC current as a function of the temperature is given by:

```
I(T) = I(tnom) * [1 + tc1 * (T - tnom) + tc2 * (T - tnom)^2].
```

Sample Instance Statement

```
i1 (in 0) isource dc=0 type=pulse delay=10n val0=0 val1=500u period=500n rise=1n
fall=1n width=250n
```

Instance Syntax

```
Name  sink  src  [ctlp]  [ctln] isource parameter=value ...
```

Positive current exits the source node and enters the sink node.The third node `ctl` is used as a switch only for prbs source.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

`dc=0 A`	DC value.

General waveform parameters

`type=dc`	Waveform type. Possible values are `dc`, `pulse`, `pwl`, `sine`, `exp`, `bit`, `prbs`, `pwlz`, `sigbus` and `oscmacro`.
`fundname`	Name of the fundamental frequency. The parameter must be specified if the source is active during qpss analysis or if the source is an active clock during an envlp analysis.
`delay=0 s`	Waveform delay time.
`edgetype=linear`	Type of rising and falling edges; effective for pulse, pulse-like piecewise linear, bit, and prbs sources. Possible values are `linear` and `halfsine`.

Pulse waveform parameters

`val0=0 A`	Zero value used in pulse and exponential waveforms.
`val1=1 A`	One value used in pulse and exponential waveforms.
`period=infinity s`	Period of waveform. When `type=prbs`, period defines the bit duration.
`rise (s)`	Rise time for pulse waveform (time for transition from `val0` to `val1`). If the rise parameters is not specified, the rise time is the same as fall time. If the fall time is also not specified, the rise time is 1/100 of the waveform period. If the waveform is not periodic, the rise time is 1/100 of the simulation interval. If type=prbs, the rise time is 1/10 of the bit duration.
`fall (s)`	Fall time for pulse waveform (time for transition from `val1` to `val0`). If the fall parameter is not specified, the fall time is the same as rise time. If the rise time is also not specified, the fall time is 1/100 of the waveform period. If the waveform is not periodic, the fall time is 1/100 of the simulation interval. If type=prbs, the fall time is 1/10 of the bit duration.
`width=infinity s`	Pulse width (duration of `val1`).

© 2023 Cadence Design Systems, Inc.

PWL waveform parameters

`file`	Name of the file containing the waveform.
`wave=[...]`	Vector of time/value pairs that defines the waveform.
`offset=0 A`	DC offset for the PWL waveform.
`scale=1`	Scale factor for the PWL waveform.
`stretch=1`	Scale factor for time given for the PWL waveform.
`rms`	Desired rms (root of mean square) value of the PWL waveform.
`pwlfilter=none`	Add filter for pwl source, where the pwl data should be equal space sampled. Possible values are `nrc` (normal raised cosine filter) and `none`.
`rolloff`	Desired rolloff factor for the raised cosine filter. The default value is 0.2. This parameter is valid only when `pwlfilter` is set to `nrc`.
`pwlbandwidth`	Bandwidth of the pwl input signal. This parameter is used when `pwlfilter` is set to `nrc`.
`allbrkpts`	If set to `yes`, all points in the PWL waveform are breakpoints. Default is `yes` if the number of points is less than 20. Possible values are `yes` and `no`.
`pwlperiod (s)`	Period of the periodic PWL waveform.
`pwlperiodstart (s)`	Period start time of the periodic PWL waveform.
`pwlperiodstop (s)`	Period stop time of the periodic PWL waveform.
`pwlperiodstopvalue`	Value of the source at the time of pwlperiodstop.
`pwlperiodstopslope=30p s`	Switching time from the last PWL value to the stopvalue.
`twidth=pwlperiod /1000 s`	Transition width used when making PWL waveforms periodic.
`highz=1e12`	The impedance of high z state.
`min_z_transition _width=10e-12 s`	Minimum width of transition from z-state to non z-state. The width of transition is set as 1e-3*(z-state duration).

© 2023 Cadence Design Systems, Inc.

`min_zx_transition_width=DBL_MAX s`	Minimum width of transition from z-state.
`min_xz_transition_width=DBL_MAX s`	Minimum width of transition to z-state.
`zx_transition_width=DBL_MAX s`	Width of transition from z-state.
`xz_transition_width=DBL_MAX s`	Width of transition to z-state.
`max_zx_transition_width=DBL_MAX s`	Maximal width of transition from z-state.
`max_xz_transition_width=DBL_MAX s`	Maximal width of transition to z-state.
`max_z_transition_width=DBL_MAX s`	Maximal width of transition related to z-state.
`tdvalue`	PWL wave value before time=td.
`abstime=1`	Possible value is '0' or '1'. if set to 0, then the time specified by wave or file is time increase compared with last point.

© 2023 Cadence Design Systems, Inc.

Sinusoidal waveform parameters

`sinedc=dc A`	DC level for sinusoidal waveforms.
`ampl=1 A`	Amplitude of sinusoidal waveform.
`freq=0 Hz`	Frequency of sinusoidal waveform.
`sinephase=0 ·`	Phase of sinusoid when `t=delay`.
`ampl2=1 A`	Amplitude of second sinusoidal waveform.
`freq2=0 Hz`	Frequency of second sinusoidal waveform.
`sinephase2=0 ·`	Phase of second sinusoid when `t=delay`.
`fundname2`	Name of the fundamental frequency associated with freq2. Must be specified if freq2 is used in a qpss analysis.
`iqmodfiles=[...]`	Two file names that contain pwl I/Q source waveform.
`fmmodindex=0`	FM index of modulation for sinusoidal waveform.
`fmmodfreq=0 Hz`	FM modulation frequency for sinusoidal waveform.
`fmmodfiles=[...]`	One or two file names: containing FM waveform for one file case, and FM I/Q signals for two files with I file first.
`ammodindex=0`	AM index of modulation for sinusoidal waveform.
`ammodoffset=1`	AM offset of modulation for sinusoidal waveform.
`ammodfreq=0 Hz`	AM modulation frequency for sinusoidal waveform.
`ammodphase=0 ·`	AM phase of modulation for sinusoidal waveform.
`damp=0 1/s`	Damping factor for sinusoidal waveform.
`freqvec=[...] Hz`	Vector of support frequency of sinusoidal channel source.
`amplvec=[...] A`	Vector of amplitude of sinusoidal channel source.
`phasevec=[...] ·`	Vector of phase of sinusoidal channel source.
`maxharms=[...]`	Array of the number of harmonics of each frequency.

Exponential waveform parameters

`td1=0 s`	Rise start time for exponential wave.
`tau1 (s)`	Rise time constant for exponential wave.
`td2 (s)`	Fall start time for exponential wave.

© 2023 Cadence Design Systems, Inc.

`tau2 (s)`	Fall time constant for exponential wave.
`expperiod (s)`	Period of the periodic exponential waveform.
`expvec=[...]`	Vector of rise start time, rise time constant, fall start time, fall time constant, rise start time.

© 2023 Cadence Design Systems, Inc.

Pattern parameters

`data`	The bit string that contains a series of the four states, 1 0 m z. For `prbs`, it can contain only 0 and 1. m and z are not supported.
`rptstart=1`	The position of the bit which is used as the starting bit while repeating the string. The string is repeated from the bit specified by this parameter till the last bit present in the string. The parameter should be an integer greater than 1. It can go up to the length of the bit string.
`rpttimes=0`	The number of times the string is to be repeated. The output will maintain the state of the last bit after the last repeat. The parameter should be a non-negative integer.
`td01=0 s`	Time delay for 0 to 1 transition.
`td10=0 s`	Time delay for 1 to 0 transition.

Prbs parameters

`ref (V)`	Sets the crossing reference for the control node. This parameter applies only when the Prbs source operates as a 3- or a 4- terminal device. When the voltage across terminals 3 and 4 drops below ref, the output of the source is set to 0. If terminal 4 is not specified, it is assumed to be connected to ground.
`jitter (s)`	The parameter jitter is obsolete. It has no effect on the output.
`rjseed=1`	The seed for random number generator, which is used in generating random jitter for PRBS sources. The default value is 1.
`rjrms (s)`	When set for PRBS source or Bit source, the source has a normally distributed random jitter whose mean is zero and standard deviation is rjrms.
`pjamp=[...] s`	When set for PRBS source or Bit source, the source has multiple periodic jitters whose amplitudes are defined by pjamp and frequencies are defined by pjfreq.
`pjfreq=[...] Hz`	When set for PRBS source or Bit source, the source has multiple periodic jitters whose amplitudes are defined by pjamp and frequencies are defined by pjfreq.

© 2023 Cadence Design Systems, Inc.

`pjtype="sine"`	For PRBS source or Bit source, pjtype defines the types of periodic jitters. Possible values are `sine`, `sawtooth`, and `square`.
`seed`	This parameter is obsolete, however, is retained for backward compatibility. Set registerlength=[2 ... 32] to choose a Maximum Length Sequence or define a custom PRBS by using the lfsrtaps and lfsrseed parameters.
`taps=[...]`	For PRBS source, taps is an integer array that sets the location of the LFSR taps. For more information about the PRBS operation, see the 'PRBS Type Waveform' section. Note: The use of taps is not recommended. Use lfsrtaps instead.
`lfsrtaps=[...]`	For PRBS source, lfsrtaps is an integer array that sets the location of LFSR taps. Locations are 1-based and ordered from MSB to LSB of the LFSR. The largest element of the taps array is equal to the width of the LFSR. For more information about the PRBS source operation, see the 'PRBS Type Waveform' section.
`lfsrseed=[...]`	For PRBS source, lfsrseed is an integer array that sets the initial state of an LFSR. Array elements set the location of non-zero bits. Locations are 1-based and ordered from MSB to LSB of the LFSR. For example, assume lfsrtaps=[6] and lfsrseed=[1 3 5]. The width of the register is then 6 bits and the initial state is '101010'.
`registerlength`	When set for PRBS source, the registerlength parameter defines the width of the LFSR that works in the Maximum Length Sequence mode. For more information about MLS setting, see the 'PRBS Type Waveform' section.
`triggerthreshold (A)`	For PRBS, when the triggerthreshold parameter is set and the source is instantiated with optional control terminals (terminals 3 and 4; if terminal 4 is unspecified it is assumed to be connected to ground), the parameter defines the crossing threshold for the trigger event. The event causes the emission of the next PRBS pulse.

© 2023 Cadence Design Systems, Inc.

`triggerdelthresh (A)`	For PRBS in external triggering mode, the triggerdelthresh parameter is used with the triggerthreshold parameter to define the crossing threshold. For rising edge triggering, the threshold is (triggerthreshold + triggerdelthresh); for falling edge triggering, the threshold is (triggerthreshold - triggerdelthresh). The default value is zero.
`triggerdirection ="both"`	For PRBS in external triggering mode, `triggerdirection` defines the direction of the control signal at the crossing event. Possible values are `rise`, `fall`, and `both`.
`transitionrefere nce`	Defines the voltage swing for the duration of rise and fall time as a percentage of val1 - val0. For example, transitionreference =100 means that the output voltage transitions from val0 to val1 in rise seconds. 90 means that it transitions from 0.1*(val1-val0) to 0.9*(val1-val0) in rise seconds, 80 means that it transitions from 0.2*(val1-val0) to 0.8*(val1-val0) in rise seconds, and so on. Possible values are 100, 90, 80, 70 and 60.
`modulation=none`	Type of amplitude modulation; effective for bit and prbs sources. Possible values are `none` and `pam4`.
`pam4_mapping=0132`	The PAM4 mapping string specifies the mapping from a pair of bits to 4-level voltages. Possible values are: 123, 132, 213, 231, 312, 321, 0123, 0132, 0213, 0231, 0312, 0321, 1023, 1032, 1203, 1230, 1302, 1320, 2013, 2031, 2103, 2130, 2301, 2310, 3012, 3021, 3102, 3120, 3201, and 3210.

Osc Macro Parameters

`oscmacrofile`	Name of the file containing the harmonic balance steady-state solution with/without phase noise data.
`freqscale`	Frequency scale factor
`amplscale`	Amplitude scale factor.

© 2023 Cadence Design Systems, Inc.

Noise Parameters

`noisefile`
: Name of the file containing excess spot noise data in the form of frequency-noise pairs. The noise can be specified as the spectral density in V^2/Hz, or as single-sideband phase noise in dBc. The parameter noisetype determines how Spectre interprets the noise data. Noisetype parameter in data file has identical definition to same parameter noisetype and supersedes it. It is intended to prevent misuse of the datafile.

`noisevec=[...]` A^2/Hz
: Excess spot noise as a function of frequency in the form of frequency-noise pairs. The parameter noisetype determines how Spectre interprets the noise data.

`noisetype=noisevoltage`
: `noisetype` parameter specifies the units and source of noise data. When this parameter is set to `noisevoltage`, the noise data represents the noise spectral density in V^2/Hz of noise measured at the output of a driven circuit. When set to `ssbphasenoise`, the noise data represents the single-sideband phase noise in dBc measured at the output of a free oscillator. When set to `edgephasenoise`, the noise data represents the single-sideband phase noise in dBc measured at the output of a driven or oscillator circuit in sampled pnoise/hbnoise jitter analysis. For `noisetype=noisevoltage`, the frequencies are taken as absolute. For `ssbphasenoise` and `edgephasenoise`, the frequencies are offset from the carrier. Note that `Noisetype=edgephasenoise` is tied to a specific sampling edge position and should be used only for simulating jitter at that given edge position. `Noisetype=ssbphasenoise` can be used only with pnoise, qpnoise, hbnoise analyses, the noise source will be ignored in transient noise and AC noise analyses.

  Possible values are `noisevoltage` and `ssbphasenoise`.

© 2023 Cadence Design Systems, Inc.

`noiseinterp=linear`	Determines how the specified noise data is interpolated. This parameter only applies to noisetype=noisevoltage. When set to linear, interpolation is linear over both axes. When set to loglog, Spectre uses log interpolation over both axes. Possible values are `linear` and `loglog`.
`isnoisy=yes`	Should isource generate noise. Possible values are `yes` and `no`.

Small signal parameters

`mag=0 A`	Small signal current.
`phase=0 ·`	Small signal phase.
`xfmag=1 A/A`	Transfer function analysis magnitude.
`pacmag=0 A`	Periodic AC analysis magnitude.
`pacphase=0 ·`	Periodic AC analysis phase.

Multiplication factor parameters

`m=1`	Multiplicity factor.

Temperature effects parameters

`tc1=0 1/C`	First order temperature coefficient.
`tc2=0` C^{-2}	Second order temperature coefficient.
`tnom=27 C`	Parameter measurement temperature. The default value is set by the options statement.
`trise=0.0 C`	Temperature rise from ambient.

If you do not specify the DC value, it is assumed to be the `time`=0 value of the waveform.

Sinusoidal waveform in the time interval `0<t<delay` has constant value equal to the value at `t=delay`.

In DC analyses, the only active parameters are `dc`, `m`, and the temperature coefficient parameters. In AC analyses, the only active parameters are `m`, `mag`, and `phase`. In transient analyses, all parameters are active except small-signal parameters and noise parameters.

© 2023 Cadence Design Systems, Inc.

The `type` parameter selects the type of waveform to be generated. You may specify parameters for more than one waveform type and use the `alter` statement to change the waveform type between analyses. However, you cannot change `bit` type to other types or other types to `bit`.

PWL Type Waveform

A vector of time-value pairs describes the piecewise linear waveform. As an alternative, you can read the waveform from a file. In this case, you give time-value pairs one pair per line with a space or tab between time and value.

The input file may also contain design variables. For example, the input file can have time, value, or both time and value as variables. The expressions may also contain empty spaces.

If you set `allbrkpts` to `yes`, you force the simulator to place the time points at each point specified in a PWL waveform during transient analysis. This can be expensive for waveforms with many points. If you set `allbrkpts` to `no`, Spectre looks for abrupt changes in the waveform and forces the time points only at those changes.

The PWL waveform is periodic if you specify `pwlperiod`, `pwlperiodstart` and `pwlperiodstop`. If both `pwlperiod` and `pwlperiodstart` are specified, `pwlperiod` should be greater than `wavelength` - `pwlperiodstart`, where `wavelength` means the last time point. If only `pwlperiod` is specified and `pwlperiodstart` is undefined, the period starts at the first time point or `wavelength` - `pwlperiod`, whichever is greater. If only `pwlperiodstart` is specified and `pwlperiod` is undefined, the period ends at the last time point in the waveform vector. If `pwlperiodstop` is defined, the waveform stops the repeat at the specified time, and the source value changes to `pwlperiodstopvalue` at the time period specified by `pwlperiodstopslope`. If the value of the waveform specified is not the same at both the period beginning and the period end, you must provide a non-zero value for`twidth`. Before repeating, the waveform changes linearly in an interval of `twidth` from its value at `period` - `twidth` to its value at the beginning of the waveform. Therefore, `twidth` must always be less than `period`.

Bit Type Waveform

Bit type waveform is the analog waveform of a series of digital logic states. It uses the pattern parameters to provide the digital state sequence, and some pulse waveform parameters to define the waveform characteristics.

To define the waveform characteristics, use parameters: `val1`, `val0`, `rise`, `fall`, and `period`. The general parameter `delay` can also be used for bit type to define the delay time

© 2023 Cadence Design Systems, Inc.

from the beginning of the transient interval to the beginning of the first bit. The state during the delay time is the same as the first state specified in data.

Note: It is mandatory to specify the parameter `period`, which defines the length of a bit.

Pattern parameters are used to specify the digital bit string. The pattern parameters of sources are the same as those of a pattern, except that you can set `rpttimes` to a negative value for sources but not for patterns. For more information on how to use pattern parameters, run the `spectre -h pattern` command.

PRBS Type Waveform

When `type=prbs`, the source generates a pseudo-random bit sequence. The sequence is defined by the LSB of a Fibonacci Linear Feedback Shift Register (LFSR) at trigger events.

LFSR is initially loaded by a `seed`. The value fed back to the input (MSB) is given by `feedback=tap_1 ^ tap_2 ^...^ tap_N`, where `^` represents an exclusive-or operation, and `tap_i` represents the i-th bit of the register, counting from 1 and starting from MSB. At a trigger event, the LFSR is shifted to the right and MSB is given by `feedback`.

LFSR Modes

The sequence can be defined by custom values of seeds and taps. Alternatively, you can specify a maximum length sequence by setting the length of LFSR. To specify custom seeds and taps, use the `lfsrseed` and `lfsrtaps` arrays. To specify a maximum length sequence, use the parameter `registerlength=[2 ... 32]`. Spectre sets the seeds and taps automatically. You can optionally set lfsrseed to override the automatically chosen seed.

Triggering Mode

By default, the sequence is triggered by an internal clock and pulses are generated every `period` seconds, excluding the optional jitter. Alternatively, you can apply an external clock to the optional third and fourth terminals. In external trigger mode, the pulses are generated when the clock crosses the specified threshold in the specified direction. The threshold is defined by the `triggerthreshold` parameter and the direction is specified by the `triggerdirection` parameter. In external trigger mode, `jitter` and `bit` period parameters are ignored.

© 2023 Cadence Design Systems, Inc.

Jitter

Let `{s_i}` be a sequence of ones and zeros whose transitions occur at intervals given by `n*T + j(t)`, where `T` is the bit duration. Then, according to the Verilog-A terminology, the jittered output is given by `s(t+j(t)) = transition(s_i? Vhigh : Vlow, rise, fall). j(t) = rj(t) + pj(t)`, where `rj` (random jitter) is a normally distributed random variable whose mean is 0 and standard deviation is given by the parameter `rjrms`. `pj` is the periodic jitter whose amplitude is `pjamp` and frequency is `pjfreq`. The parameter `pjtype` defines the type of jitter waveform. For sine, the periodic jitter is given by `pj(t) = pjamp*cos(2*pi*pjfreq*t)`. Other types are square and sawtooth.

Noise of the source

You can give the excess noise of the source as a file or specify it with a vector of frequency-noise pairs. For a file, give the frequency-noise pairs one pair per line with a space or tab between the frequency and noise values.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.

Operating-Point Parameters

`i (A)`	Current through the source.
`v (V)`	Voltage across the source.
`pwr (W)`	Power dissipation.

Related Topics

Linear Current Controlled Current Source (cccs)

Linear Current Controlled Voltage Source (ccvs)

Current Sources

Circuit Components

© 2023 Cadence Design Systems, Inc.

Polynomial Current Controlled Current Source (pcccs)

A vector of coefficients specifies the polynomial function that defines the relationship between the output current and the controlling currents. You must specify at least one coefficient.

This device is supported within altergroups.

For a polynomial in M variables a1, a2, ... am, the polynomial function F(a0,a1,...,am) is given by

F = c0 + c1 * a1 + c2 * a2 + ...

+ c(m+1) * a1^2 + c(m+2) * a1 * a2 +...

+ c(2m+1) * a2^2 + c(2m+2) * a2 * a3 +...

where the cs are coefficients of the polynomial terms.

Sample Instance Statement

```
vpc (net1 0) pcccs probes=[vb vc ve vlp vpn] coeffs=[0 8.8e6 -8.8e6 9e6 8e6 -9e6]
```

Instance Syntax

```
Name  sink  src pcccs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1`	Multiplicity factor.
`gain=1`	Gain Parameter.
`probes=[...]`	Devices through which the controlling currents flow.
`mprobes=[...]`	The mprobes function the same as probes except that they will divide the input currents by the mfactor.
`ports=[...]`	Indexes of the probe ports through which the controlling currents flow.
`coeffs=[...]`	Polynomial coefficients. At least one must be given.
`file`	File that contains nonzero polynomial coefficients.
`min (A)`	Minimum output current.
`max (A)`	Maximum output current.
`abs=off`	Absolute output current. Possible values are `off` or `on`.
`delta=0`	Smoothing parameter. This may lead to circuit convergence. The smaller the delta is, the sharper the corner is.

Temperature effects parameters

`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

Polynomial Voltage Controlled Current Source (pvccs)

© 2023 Cadence Design Systems, Inc.

Current Sources

Circuit Components

Polynomial Voltage Controlled Current Source (pvccs)

A vector of coefficients specifies the polynomial function that defines the relationship between the output current and the controlling voltages. You must specify at least one coefficient. Current exits the source node and enters the sink node.

This device is supported within altergroups.

For a polynomial in M variables a1, a2, ... am, the polynomial function F(a0,a1,...,am) is given by

F = c0 + c1 * a1 + c2 * a2 + ...

+ c(m+1) * a1^2 + c(m+2) * a1 * a2 +...

+ c(2m+1) * a2^2 + c(2m+2) * a2 * a3 +...

where the cs are coefficients of the polynomial terms.

Sample Instance Statement

v2 (net1 0 net2 0) pvccs coeffs=[0 -2e-3 - 10e-3] gain=2 m=1

Instance Syntax

```
Name  sink  src  ps1  ns1 ... pvccs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1`	Multiplicity factor.
`type=pvccs`	Type of the source. Possible values are `pvccs`, `vcr` or `vccap`.
`gain=1`	Gain Parameter.
`coeffs=[...]`	Polynomial coefficients. At least one must be given.
`file`	File that contains nonzero polynomial coefficients.
`min (A)`	Minimum output current.
`max (A)`	Maximum output current.
`abs=off`	Absolute output current. Possible values are `off` or `on`.
`delta=0`	Smoothing parameter. This may lead to circuit convergence. The smaller the delta is, the sharper the corner is.

Temperature effects parameters

`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0 C`	Temperature rise from ambient.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.
`rclamp=0.0` Ω	Used for PVCR only. When rclamp is positive, small resistor will be clamped to this value.
`rcut=1e100` Ω	Used for PVCR only. When resistor is larger than this value, it will be cut to this value.
`maxIrGain=100` Ω	Used for PVCR only. When abs(Ir * dR/dVr) is larger than this value, it will be clamped to this value.

© 2023 Cadence Design Systems, Inc.

Related Topics

Polynomial Current Controlled Current Source (pcccs)

Current Sources

Circuit Components

s-Domain Linear Current Controlled Current Source (scccs)

The device output is defined through a transfer function given as a ratio of two polynomials in the complex variable `s`. Polynomials can be specified in terms of either coefficients or roots. The roots of the numerator are the zeros of the transfer function and the roots of the denominator are the poles.

To specify the polynomial in terms of the coefficients, you enter them as a vector in ascending order of the power of the variable `s`, starting from the constant term. For example, to specify a denominator of 3s^2 + 4s + 1, use `denom=[1 4 3]`.

To specify a polynomial in terms of its roots, give the roots as a vector of complex frequencies (frequencies should be in radians/seconds). You must give both the real and imaginary parts of the root, even when the root is real. For the transfer function to be stable, all poles must have negative real values. When specifying a complex root, you should also specify its complex conjugate. However, if you omit the conjugate root, Spectre will supply the missing root and print a warning that a missing root was supplied. The roots can be in any order. For example, to specify poles of s = -1, s = 4j, s = -4j, s = -2 + 2j, and s = -2 - 2j; use `poles=[-1 0 0 4 0 -4 -2 2 -2 -2]`.

Either the numerator or the denominator specification can be omitted. An omitted denominator or numerator is taken to be 1.

Notes on gain and gainfactor

The parameter `gain` is interpreted either as the DC gain or, if the function has zeros or poles at the origin, as a constant factor. `gain` has a default value of 1, so if you do not want to specify the DC gain, you should always use parameter `gainfactor` to disable parameter `gain`. When `gainfactor` is specified, `gain` is not valid any more. For example, if the instant statement is:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4]

© 2023 Cadence Design Systems, Inc.

the transfer function will be 2*(2s+1)/(4s+3). Factor 2 is applied to make the DC gain of the transfer function to be 1. If you just want the transfer function to be (2s+1)/(4s+3), specify `gainfactor=1` to disable the default value of `gain`. In this example, the statement will be:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4] gainfactor=1

where the transfer function is 1*(2s+1)/(4s+3). 1 is the gainfactor.

This device is not supported within altergroup.

Sample Instance Statement

l1 (2 1) inductor l=15

sc1 (1 0) scccs probe=l1 zeros=[0 6 0 -6 2 -8 2 8] poles=[-1 0 0 64 0 -64 -2 8 -2 -8]

Instance Syntax

```
Name  sink  src scccs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`probe`	Device through which the controlling current flows.
`mprobe`	The mprobe functions the same as probe except that it will divide the input current by the mfactor.
`port=0`	Index of the probe port through which the controlling current flows.
`gain=1`	DC gain or constant transfer function factor. See `notes on gain and gainfactor` for details.
`gainfactor`	Constant factor applied to transfer function. It disables the parameter gain.
`numer=[...]`	Vector of numerator coefficients.
`denom=[...]`	Vector of denominator coefficients.
`zeros=[...]`	Vector of complex zeros.
`poles=[...]`	Vector of complex poles.
`m=1`	Multiplicity factor.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature frise from ambient.

Operating-Point Parameters

`i (A)`	Input current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

Linear Voltage Controlled Current Source (vccs)

Current Sources

Circuit Components

© 2023 Cadence Design Systems, Inc.

s-Domain Linear Voltage Controlled Current Source (svccs)

The device output is defined through a transfer function given as a ratio of two polynomials in the complex variable `s`. Polynomials can be specified in terms of either coefficients or roots. The roots of the numerator are the zeros of the transfer function and the roots of the denominator are the poles.

To specify the polynomial in terms of the coefficients, you enter them as a vector in ascending order of the power of the variable `s`, starting from the constant term. For example, to specify a denominator of 3s^2 + 4s + 1, use `denom=[1 4 3]`.

To specify a polynomial in terms of its roots, give the roots as a vector of complex frequencies (frequencies should be in radians/seconds). You must give both the real and imaginary parts of the root, even when the root is real. For the transfer function to be stable, all poles must have negative real values. When specifying a complex root, you should also specify its complex conjugate. However, if you omit the conjugate root, Spectre will supply the missing root and print a warning that a missing root was supplied. The roots can be in any order. For example, to specify poles of s = -1, s = 4j, s = -4j, s = -2 + 2j, and s = -2 - 2j; use `poles=[-1 0 0 4 0 -4 -2 2 -2 -2]`.

Either the numerator or the denominator specification can be omitted. An omitted numerator or denominator is taken to be 1.

Notes on gain and gainfactor

The parameter `gain` is interpreted either as the DC gain or, if the function has zeros or poles at the origin, as a constant factor. `gain` has a default value of 1, so if you do not want to specify the DC gain, you should always use parameter `gainfactor` to disable parameter `gain`. When `gainfactor` is specified, `gain` is not valid any more. For example, if the instant statement is:

s1 (1 0 control 0) svccs numer=[1 2] denom=[3 4]

the transfer function will be 2*(2s+1)/(4s+3). Factor 2 is applied to make the DC gain of the transfer function to be 1. If you just want the transfer function to be (2s+1)/(4s+3), specify `gainfactor=1` to disable the default value of `gain`. In this example, the statement will be:

s1 (1 0 control 0) svccs numer=[1 2] denom=[3 4] gainfactor=1

where the transfer function is 1*(2s+1)/(4s+3). 1 is the gainfactor.

This device is not supported within altergroup.

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

```
s2 (1 0 control 0) svccs gain=0.4 numer=[2 3] denom=[4 5 1]
```

Instance Syntax

```
Name  sink  src  ps  ns svccs parameter=value ...
```

Instance Parameters

`gain=1`	DC gain or constant transfer function factor. See `notes on gain and gainfactor` for details.
`gainfactor`	Constant factor applied to transfer function. It disables the parameter gain.
`numer=[...]`	Vector of numerator coefficients.
`denom=[...]`	Vector of denominator coefficients.
`zeros=[...]`	Vector of complex zeros.
`poles=[...]`	Vector of complex poles.
`m=1`	Multiplicity factor.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

Linear Voltage Controlled Current Source (vccs)

Current Sources

Circuit Components

© 2023 Cadence Design Systems, Inc.

Linear Voltage Controlled Current Source (vccs)

Positive current exits the source node and enters the sink node.

This device can also model ideal digital gates, voltage controlled resistors and voltage controlled capacitors.

Type of vccs:

You can use vccs to model three types of devices.

When `type=vccs`, the device is a regular voltage controlled current source. This is also the default type.When `type=vcr`, the device is a voltage controlled resistor. When `type=vccap`, the device is a voltage controlled capacitor.

Input type of vccs:

You can use vccs to model ideal digital gates. Ideal digital gates have more than one inputs. The parameter `inputtype` is used to specify which input is going to control the vccs (or vcr, or vccap, specified by parameter type).

When `inputtype=single`, the device has only one input. This is also the default `inputtype`. When `inputtype=and/nand`, the smallest input controls the device. When `inputtype=or/nor`, the largest input controls the device. When `inputtype=npwl`, node ns should be connected to either src or sink. if v(src,sink)>0, then the controlling voltage would be v(ps,sink). Otherwise, the controlling voltage is v(ps,src). When `inputtype=ppwl`, node ns should be connected to either src or sink. if v(src,sink)>0, then the controlling voltage would be v(ps,src). Otherwise, the controlling voltage is v(ps,sink). If `inputtype` is `npwl` or `ppwl` but node ns is not connected to src or sink, then spectre change `inputtype` to `pwl`.

When you are using regular vccs, you can specify and/nand/or/nor in either type parameter of `inputtype` parameter.

Note: Spectre does not check if the gate behaves like an and or an nand, it just takes the smallest input as the controlling voltage. And so is the case for or/nor.

This device is supported within altergroups.

Sample Instance Statement

```
v1 (1 0 2 3) gm=-1 m=2
```


© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  sink  src  ps  ns ... vccs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1`	Multiplicity factor.
`type=vccs`	Type of the source. Possible values are `vccs`, `vcr`, `vccap`, `and`, `nand`, `or`, `nor`, or `vcrspice`.
`inputtype=single`	Type of the input of the source. Possible values are `single`, `and`, `nand`, `or`, `nor`, `npwl`, or `ppwl`.
`delta=0`	Smoothing parameter. This may lead to circuit convergence. Its value should be in the range between 0 and 0.5, both ends included. The smaller the delta is, the sharper the corner is.

Linear source parameters

`gm=0 S`	Transconductance.
`td=0.0 s`	Time delay.
`min (A)`	Minimum output current.
`max (A)`	Maximum output current.
`abs=off`	Output current is absolute value if abs is set to on. Possible values are `off` or `on`.

PWL source parameters

`file`	Name of file containing voltage/current pairs that define the PWL transfer function.
`pwl=[...]`	Vector of voltage/current pairs that defines the PWL transfer function. The format of the vector is [in1 out1 in2 out2 ...].
`scale=1`	Scale factor for the PWL output current.
`stretch=1`	Scale factor for the PWL controlling voltage.
`logslope=1e3`	Used for PWL VCR only. If the slope between PWL points is larger than logslope, then log scale interpolation is used between the points.
`rclamp=0.0`	Used for VCR only. When `rclamp` is positive, a small resistor will be clamped to this value.

© 2023 Cadence Design Systems, Inc.

`rcut=1e100`	Used for VCR only. When resistor is larger than this value, it will be rcut to this value.

Temperature effects parameters

`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

The Smoothing Factor

The parameter delta is the smoothing factor. When it is nonzero, a curve is introduced to smooth the corner. The value of delta defines the position of the starting and ending points of the curve that is used to smooth the corner. The minimum value 0 means no smoothing curve is introduced. The maximum value 0.5 means the distance between the starting point of the curve and the corner point is half of the shortest distance. The shortest distance is the length of the shortest segment of the piecewise linear function. Or, when there is no shortest segment in the controlling function, i.e. only abs=on is specified, spectre uses 1 as the shortest distance.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`islinear`

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.
`lx0 (A)`	Output current for VCCS; resistance value for VCR; capacitance value for VCCAP.
`lx1 (A)`	Controlling voltage for VCCS or VCR; capacitance charge for VCCAP.
`lx3 (A)`	Voltage across capacitance for VCCAP.

Related Topics

s-Domain Linear Voltage Controlled Current Source (svccs)

Current Sources

Circuit Components

z-Domain Linear Current Controlled Current Source (zcccs)

The output is defined with a transfer function given as the ratio of two polynomials in the complex variable z. Each polynomial can be specified using either its coefficients or its roots. The roots of the numerator are the zeros of the transfer function and the roots of the denominator are the poles.

You may specify polynomials either in the complex variable z or 1/z by setting optional parameter `polyarg` to `z` or `inversez` respectively. By default, it is set to `inversez`. If you choose to provide the coefficients of a polynomial, enter them as a vector in ascending order of the power of the variable z or 1/z, starting from the constant term. For example, to specify a denominator of 3z^-2 + 4z^-1 + 1, use `denom=[1 4 3]`. Or to specify a denominator of 4z^2 + 3z - 2, use `polyarg=z denom=[2 3 4]`.

© 2023 Cadence Design Systems, Inc.

To specify transfer function in terms of its zeros and poles in z-plane, give them as vectors of complex numbers. You must always give the real and imaginary portions of the root, even when the root is real. You may give either both roots of a complex-conjugate pair or only one. In the latter case the conjugate complex root will be generated automatically. The order of the roots is not important. For example, to specify poles of z = 1, z = 4j, z = -4j, z = 2 + 2j, and z = 2 - 2j, use `poles=[1 0 0 4 0 -4 2 2 2 -2]` or, omitting conjugate poles, `poles=[1 0 0 4 2 2 ]`.

Either the numerator or the denominator specification can be omitted. An omitted denominator or numerator is taken to be 1.

Transition time (`tt`) is an optional parameter that at each sampling point forces linear transition of the output to a new value within the specified time range. By default, it is set to one percent of the sampling period.

The sampling delay (`td`) is another optional parameter, with the default value of 0, that lets you set asynchronous sampling rates.

To use the `s` to `z` transformation, set the optional `sxz` parameter to one of the transformation methods - forward differences, backward differences, or bilinear. When the `sxz` parameter is specified, the transfer function specification is assumed to be given in the complex variable s and it will be transformed to the complex variable z using the indicated method.

Notes on gain and gainfactor

The parameter `gain` is interpreted either as the DC gain or, if the function has zeros or poles at the origin, as a constant factor. `gain` has a default value of 1, so if you do not want to specify the DC gain, you should always use parameter `gainfactor` to disable parameter `gain`. When `gainfactor` is specified, `gain` is not valid any more. For example, if the instant statement is:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4]

the transfer function will be 2*(2s+1)/(4s+3). Factor 2 is applied to make the DC gain of the transfer function to be 1. If you just want the transfer function to be (2s+1)/(4s+3), specify `gainfactor=1` to disable the default value of `gain`. In this example, the statement will be:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4] gainfactor=1

where the transfer function is 1*(2s+1)/(4s+3). 1 is the gainfactor.

This device is not supported within altergroup.

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

```
va (1 0) vsource type=sine freq=10K
z2 (2 0) zcccs probe=va gain=1 ts=4.9e-5 tt=1e-5 polyarg=inservez
numer=[1 -1] denom=[1 0]
```

Instance Syntax

```
Name  sink  src zcccs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`probe`	Device through which the controlling current flows.
`mprobe`	The mprobe functions the same as probe except that it will divide the input current by the mfactor.
`port=0`	Index of the probe port through which the controlling current flows.
`ts=1 s`	Sampling period.
`td=0 s`	Sampling delay.
`tt=0.01 ts s`	Transition time.
`gain=1`	DC gain or constant transfer function factor. See `notes on gain and gainfactor` for details.
`gainfactor`	Factor applied to transfer function. It overwrites the parameter gain.
`polyarg=inversez`	Polynomial argument. Possible values are `z` or `inversez`.
`sxz=none`	s to z transformation. Possible values are `none`, `backward`, `forward`, or `bilinear`.
`numer=[...]`	Vector of numerator coefficients.
`denom=[...]`	Vector of denominator coefficients.
`zeros=[...]`	Vector of complex zeros.
`poles=[...]`	Vector of complex poles.
`m=1`	Multiplicity factor.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

Operating-Point Parameters

`i (A)`	Input current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

© 2023 Cadence Design Systems, Inc.

Related Topics

z-Domain Linear Voltage Controlled Current Source (zvccs)

Current Sources

Circuit Components

z-Domain Linear Voltage Controlled Current Source (zvccs)

The output is defined with a transfer function given as the ratio of two polynomials in the complex variable z. Each polynomial can be specified using either its coefficients or its roots. The roots of the numerator are the zeros of the transfer function and the roots of the denominator are the poles.

You may specify polynomials either in the complex variable z or 1/z by setting optional parameter `polyarg` to `z` or `inversez` respectively. By default, it is set to `inversez`. If you choose to provide the coefficients of a polynomial, enter them as a vector in ascending order of the power of the variable z or 1/z, starting from the constant term. For example, to specify a denominator of 3z^-2 + 4z^-1 + 1, use `denom=[1 4 3]`. Or to specify a denominator of 4z^2 + 3z - 2, use `polyarg=z denom=[2 3 4]`.

To specify transfer function in terms of its zeros and poles in z-plane, give them as vectors of complex numbers. You must always give the real and imaginary portions of the root, even when the root is real. You may give either both roots of a complex-conjugate pair or only one. In the latter case the conjugate complex root will be generated automatically. The order of the roots is not important. For example, to specify poles of z = 1, z = 4j, z = -4j, z = 2 + 2j, and z = 2 - 2j, use `poles=[1 0 0 4 0 -4 2 2 2 -2]` or, omitting conjugate poles, `poles=[1 0 0 4 2 2 ]`.

Either the numerator or the denominator specification can be omitted. An omitted denominator or numerator is taken to be 1.

Transition time (`tt`) is an optional parameter that at each sampling point forces linear transition of the output to a new value within the specified time range. By default, it is set to one percent of the sampling period.

The sampling delay (`td`) is another optional parameter, with the default value of 0, that lets you set asynchronous sampling rates.

To use the `s` to `z` transformation, set the optional `sxz` parameter to one of the transformation methods - forward differences, backward differences, or bilinear. When the `sxz` parameter is

© 2023 Cadence Design Systems, Inc.

specified, the transfer function specification is assumed to be given in the complex variable s and it will be transformed to the complex variable z using the indicated method.

Notes on gain and gainfactor

The parameter `gain` is interpreted either as the DC gain or, if the function has zeros or poles at the origin, as a constant factor. `gain` has a default value of 1, so if you do not want to specify the DC gain, you should always use parameter `gainfactor` to disable parameter `gain`. When `gainfactor` is specified, `gain` is not valid any more. For example, if the instant statement is:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4]

the transfer function will be 2*(2s+1)/(4s+3). Factor 2 is applied to make the DC gain of the transfer function to be 1. If you just want the transfer function to be (2s+1)/(4s+3), specify `gainfactor=1` to disable the default value of `gain`. In this example, the statement will be:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4] gainfactor=1

where the transfer function is 1*(2s+1)/(4s+3). 1 is the gainfactor.

This device is not supported within altergroup.

Sample Instance Statement:

va (1 0) vsource type=sine freq=10K

z1 (2 0 1 0) zvccs gain=2 ts=4.5e-5 tt=1e-5 zeros=[-1 0] poles=[0 0]

Instance Syntax

```
Name sink  src  ps  ns zvccs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`ts=1 s`	Sampling period.
`td=0 s`	Sampling delay.
`tt=0.01 ts s`	Transition time.
`gain=1`	DC gain or constant transfer function factor. See `notes on gain and gainfactor` for details.
`gainfactor`	Factor applied to transfer function. It overwrites the parameter gain.
`polyarg=inversez`	Polynomial argument. Possible values are `z` or `inversez`.
`sxz=none`	s to z transformation. Possible values are `none`, `backward`, `forward`, or `bilinear`.
`numer=[...]`	Vector of numerator coefficients.
`denom=[...]`	Vector of denominator coefficients.
`zeros=[...]`	Vector of complex zeros.
`poles=[...]`	Vector of complex poles.
`m=1`	Multiplicity factor.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

z-Domain Linear Current Controlled Current Source (zcccs)

Current Sources

© 2023 Cadence Design Systems, Inc.

Circuit Components

Voltage Sources

Click the following topics to read about the types of voltage sources:

- Polynomial Current Controlled Voltage Source (pccvs)
- Polynomial Voltage Controlled Voltage Source (pvcvs)
- s-Domain Voltage Controlled Voltage Source (svcvs)
- Linear Voltage Controlled Voltage Source (vcvs)
- Independent Voltage Source (vsource)
- z-Domain Current Controlled Voltage Source (zccvs)
- z-Domain Voltage Controlled Voltage Source (zvcvs)

Polynomial Current Controlled Voltage Source (pccvs)

The polynomial function defining the relationship between the output voltage and the controlling currents is specified by a vector of coefficients. At least one coefficient must always be specified. Current through the voltage source is calculated and is defined to be positive if it flows from the positive terminal, through the source, to the negative terminal.

This device is supported within altergroups.

For a polynomial in M variables a1, a2, ... am, the polynomial function F(a0,a1,...,am) is given by

$$F = c0 + c1 * a1 + c2 * a2 + ...$$

$$+ c(m+1) * a1^2 + c(m+2) * a1 * a2 +...$$

$$+ c(2m+1) * a2^2 + c(2m+2) * a2 * a3 +...$$

where the `c`s are coefficients of the polynomial terms.

Sample Instance Statement

```
ixy (net1 0) pccvs coeffs=[0 1 0 1] probes=[vin1 vin2] gain=2
```


© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  p  n pccvs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1`	Multiplicity factor.
`gain=1`	Gain Parameter.
`probes=[...]`	Devices through which the controlling currents flow.
`mprobes=[...]`	The mprobes function the same as probes except that they will divide the input currents by the mfactor.
`ports=[...]`	Indexes of the probe ports through which the controlling currents flow.
`coeffs=[...]`	Polynomial coefficients. At least one must be given.
`file`	File that contains nonzero polynomial coefficients.
`min (V)`	Minimum output voltage.
`max (V)`	Maximum output voltage.
`abs=off`	Absolute output voltage. Possible values are `off` or `on`.
`delta=0`	Smoothing parameter. This may lead to circuit convergence. The smaller the delta is, the sharper the corner is.

Temperature effects parameters

`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

Polynomial Voltage Controlled Voltage Source (pvcvs)

© 2023 Cadence Design Systems, Inc.

Voltage Sources

Circuit Components

Polynomial Voltage Controlled Voltage Source (pvcvs)

A vector of coefficients specifies the polynomial function that defines the relationship between the output voltage and the controlling voltages. You must specify at least one coefficient. Current through the voltage source is calculated and is defined to be positive if it flows from the positive terminal, through the source, to the negative terminal.

This device is supported within altergroups.

For a polynomial in M variables a1, a2, ... am, the polynomial function F(a0,a1,...,am) is given by

F = c0 + c1 * a1 + c2 * a2 + ...

+ c(m+1) * a1^2 + c(m+2) * a1 * a2 +...

+ c(2m+1) * a2^2 + c(2m+2) * a2 * a3 +...

where the cs are coefficients of the polynomial terms.

Sample Instance Statement

```
v1 (p 0 c1 0) pvcvs coeffs=[0 0 0 0.1 1 1] gain=1
```

Instance Syntax

```
Name  p  n  ps1  ns1 ... pvcvs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1`	Multiplicity factor.
`gain=1`	Gain Parameter.
`coeffs=[...]`	Polynomial coefficients. At least one must be given.
`file`	File that contains nonzero polynomial coefficients.
`min (V)`	Minimum output voltage.
`max (V)`	Maximum output voltage.
`abs=off`	Absolute output voltage. Possible values are `off` or `on`.
`delta=0`	Smoothing parameter. This may lead to circuit convergence. The smaller the delta is, the sharper the corner is.

Temperature effects parameters

`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

Polynomial Voltage Controlled Voltage Source (pvcvs)

Voltage Sources

Circuit Components

© 2023 Cadence Design Systems, Inc.

s-Domain Voltage Controlled Voltage Source (svcvs)

The device output is defined through a transfer function given as a ratio of two polynomials in the complex variable `s`. Polynomials can be specified in terms of either coefficients or roots. The roots of the numerator are the zeros of the transfer function and the roots of the denominator are the poles.

To specify the polynomial in terms of the coefficients, you enter them as a vector in ascending order of the power of the variable `s`, starting from the constant term. For example, to specify a denominator of 3s^2 + 4s + 1, use `denom=[1 4 3]`.

To specify a polynomial in terms of its roots, give the roots as a vector of complex frequencies (frequencies should be in radians/seconds). You must give both the real and imaginary parts of the root, even when the root is real. For the transfer function to be stable, all poles must have negative real values. When specifying a complex root, you should also specify its complex conjugate. However, if you omit the conjugate root, Spectre will supply the missing root and print a warning that a missing root was supplied. The roots can be in any order. For example, to specify poles of s = -1, s = 4j, s = -4j, s = -2 + 2j, and s = -2 - 2j; use `poles=[-1 0 0 4 0 -4 -2 2 -2 -2]`.

Either the numerator or the denominator specification can be omitted. An omitted numerator or denominator is taken to be 1.

Notes on gain and gainfactor

The parameter `gain` is interpreted either as the DC gain or, if the function has zeros or poles at the origin, as a constant factor. `gain` has a default value of 1, so if you do not want to specify the DC gain, you should always use parameter `gainfactor` to disable parameter `gain`. When `gainfactor` is specified, `gain` is not valid any more. For example, if the instant statement is:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4]

the transfer function will be 3*(2s+1)/(4s+3). Factor 3 is applied to make the DC gain of the transfer function to be 1. If you just want the transfer function to be (2s+1)/(4s+3), specify `gainfactor=1` to disable the default value of `gain`. In this example, the statement will be:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4] gainfactor=1

where the transfer function is 1*(2s+1)/(4s+3). 1 is the gainfactor.

This device is not supported within altergroup.

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

```
e1 (1 0 control 0) svcvs gain=5 poles=[-1 0 1 0] zero=[0 0 1 0]
```

Instance Syntax

```
Name  p  n  ps  ns svcvs parameter=value ...
```

Instance Parameters

`gain=1`	DC gain or constant transfer function factor. See `notes on gain and gainfactor` for details.
`gainfactor`	Factor applied to transfer function. It disables the parameter gain.
`numer=[...]`	Vector of numerator coefficients.
`denom=[...]`	Vector of denominator coefficients.
`zeros=[...]`	Vector of complex zeros.
`poles=[...]`	Vector of complex poles.
`m=1`	Multiplicity factor.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

Polynomial Current Controlled Voltage Source (pccvs)

Voltage Sources

Circuit Components

© 2023 Cadence Design Systems, Inc.

Linear Voltage Controlled Voltage Source (vcvs)

Current through the voltage source is calculated and is defined as positive if it flows from the positive terminal to the negative terminal through the source.

This device can also model ideal digital gates.

This device is supported within altergroups.

Sample Instance Statement

```
e1 (out1 0 pos neg) vcvs gain=10
```

Instance Syntax

```
Name  p  n  ps  ns ... vcvs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1`	Multiplicity factor.
`type=vcvs`	Type of the source. Possible values are `vcvs`, `and`, `nand`, `or`, or `nor`.
`delta=0`	Smoothing parameter. This parameter can lead to circuit convergence. Its value should be between 0 and 0.5, both ends included. The smaller the delta is, the sharper the corner is.

Linear source parameters

`gain=0 V/V`	Voltage gain.
`td=0.0 s`	Time delay.
`min (V)`	Minimum output voltage.
`max (V)`	Maximum output voltage.
`abs=off`	When abs is set to on, the output voltage is an absolute value. Possible values are `off` or `on`.

PWL source parameters

`file`	Name of the file that contains the voltage or voltage pairs that define the PWL transfer function.
`pwl=[...]`	Vector of the voltage or voltage pairs that defines the PWL transfer function. The format of the vector is [in1 out1 in2 out2 ...].
`scale=1`	Scale factor for the PWL output voltage.
`stretch=1`	Scale factor for the PWL controlling voltage.

Temperature effects parameters

`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

© 2023 Cadence Design Systems, Inc.

The Smoothing Factor

The parameter delta is the smoothing factor. When its value is non-zero, a curve is introduced to smooth the corner. The value of delta defines the starting and ending points of the curve that is used to smooth the corner. The minimum value, 0, means no smoothing curve is introduced. The maximum value, 0.5, means the distance between the starting point of the curve to the corner point is half of the shortest distance. The shortest distance is the length of the shortest segment of the piecewise linear function. Or, when there is no shortest segment in the controlling function, that is, only `abs=on` is specified, Spectre uses 1 as the shortest distance.

Output Parameters

`islinear`

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.
`lx0 (V)`	Output voltage.
`lx1 (A)`	Output current.
`lx2 (A)`	Controlling voltage.

Related Topics

Independent Voltage Source (vsource)

Voltage Sources

Circuit Components

Independent Voltage Source (vsource)

Current through the source is computed and is defined as positive if it flows from the positive node to the negative node through the source. The third node (ctl) is used as a switch only for prbs.

© 2023 Cadence Design Systems, Inc.

This device is supported within altergroups.

The value of the DC voltage as a function of the temperature is given by:

```
V(T) = V(tnom) * [1 + tc1 * (T - tnom) + tc2 * (T - tnom)^2]
```

Sample Instance Statement

```
vpulse1 (1 0) vsource type=pulse val0=0 val1=5 period=100n rise=10n fall=10n
width=40n
vpwl1 (1 0) vsource type=pwl wave=[1n 0 1.1n 2 1.5n 0.5 2n 3 5n 5] pwlperiod=5n
vpwlz1 (1 0) vsource type=pwlz wave=[1n 0 1.1n z 1.5n 0.5 2n z 5n 5] pwlperiod=5n
```

Instance Syntax

```
Name ( p  n [ctlp]  [ctln] ) vsource parameter=value ...
```

Instance Parameters

`dc=0 V`	DC value.

General waveform parameters

`type=dc`	Waveform type. Possible values are `dc`, `pulse`, `pwl`, `sine`, `exp`, `bit`, `prbs`, `pwlz`, `sigbus`, `oscmacro`, and `pwr`.
`fundname`	Name of the fundamental frequency. The parameter must be specified if the source is active during qpss analysis or if the source is an active clock during an envlp analysis.
`delay=0 s`	Waveform delay time.
`edgetype=linear`	Type of the rising and falling edges, effective for pulse, pulse-like piecewise linear, bit, and prbs sources. Possible values are `linear` and `halfsine`.

© 2023 Cadence Design Systems, Inc.

Pulse waveform parameters

`val0=0 V`	Zero value used in pulse and exponential waveforms.
`val1=1 V`	One value used in pulse and exponential waveforms.
`period=infinity s`	Period of waveform. When `type=prbs`, period defines the bit duration.
`rise (s)`	Rise time for pulse waveform (time for transition from `val0` to `val1`). If the parameter `rise` is not given, then the rise time will be the same as the fall time; if the fall time is not given either, then the rise time will be 1/100 of the waveform period; if the waveform is not periodic, then the rise time will be 1/100 of the simulation interval; if `type=prbs`, the rise time is 1/10 of the bit duration.
`fall (s)`	Fall time for pulse waveform (time for transition from `val1` to `val0`). If the parameter `fall` is not given, then the fall time will be the same as the rise time; if the rise time is not given either, then the fall time will be 1/100 of the waveform period; if the waveform is not periodic, then the fall time will be 1/100 of the simulation interval; if `type=prbs`, the fall time is 1/10 of the bit duration.
`width=infinity s`	Pulse width (duration of `val1`).

PWL waveform parameters

`file`	Name of the file containing the waveform.
`wave=[...]`	Vector of time/value pairs that defines the waveform.
`offset=0 V`	DC offset for the PWL waveform.
`scale=1`	Scale factor for the PWL waveform.
`stretch=1`	Scale factor for time given for the PWL waveform.
`rms`	Desired rms(root of mean squre) value of the PWL waveform.
`pwlfilter=none`	Add filter to pwl source, where the pwl data should be equal space sampled. Possible values are 'nrc' (normal raised cosine filter) and 'none'.
`rolloff`	Desired rolloff factor for the raised cosine filter, default value is 0.2. Valid only when `pwlfilter` is set to `nrc`.

© 2023 Cadence Design Systems, Inc.

`pwlbandwidth`	Bandwidth of the pwl input signal. This parameter is used when `pwlfilter` is set to `nrc`.
`allbrkpts`	If set to `yes`, all the points in the PWL waveform are breakpoints. Default is `yes` if the number of points is less than 20. Possible values are `yes` and `no`.
`pwlperiod (s)`	Period of the periodic PWL waveform.
`pwlperiodstart (s)`	Period start time of the periodic PWL waveform.
`pwlperiodstop (s)`	Period stop time of the periodic PWL waveform.
`pwlperiodstopvalue`	Value of the source at the time of pwlperiodstop.
`pwlperiodstopslope=30p s`	Switching time from the last PWL value to the stopvalue.
`twidth=pwlperiod/1000 s`	Transition width used when making PWL waveforms periodic.
`highz=1e12`	The impedance of high z state.
`min_z_transition_width=10e-12 s`	Minimum width of transition from z-state to non z-state. The width of transition is set as 1e-3*(z-state duration).
`min_zx_transition_width=DBL_MAX s`	Minimum width of transition from z-state.
`min_xz_transition_width=DBL_MAX s`	Minimum width of transition to z-state.
`zx_transition_width=DBL_MAX s`	Width of transition from z-state.
`xz_transition_width=DBL_MAX s`	Width of transition to z-state.
`max_zx_transition_width=DBL_MAX s`	Maximal width of transition from z-state.
`max_xz_transition_width=DBL_MAX s`	

© 2023 Cadence Design Systems, Inc.

	Maximal width of transition to z-state.
`max_z_transition_width=DBL_MAX s`	
	Maximal width of transition related to z-state.
`tdvalue`	PWL wave value before time=td.
`abstime=1`	Possible value is '0' or '1'. if set to 0, then the time specified by wave or file is time increase compared with last point.

Sinusoidal waveform parameters

`sinedc=dc V`	DC level for sinusoidal waveforms.
`ampl=1 V`	Amplitude of sinusoidal waveform.
`freq=0 Hz`	Frequency of sinusoidal waveform.
`sinephase=0 ·`	Phase of sinusoid when `t=delay`.
`ampl2=1 V`	Amplitude of second sinusoidal waveform.
`freq2=0 Hz`	Frequency of second sinusoidal waveform.
`sinephase2=0 ·`	Phase of second sinusoid when `t=delay`.
`fundname2`	Name of the fundamental frequency associated with freq2. Must be specified if freq2 is used in a qpss analysis.
`iqmodfiles=[...]`	Two file names that contain pwl I/Q source waveform.
`fmmodindex=0`	FM index of modulation for sinusoidal waveform.
`fmmodfreq=0 Hz`	FM modulation frequency for sinusoidal waveform.
`fmmodfiles=[...]`	One or two file names containing FM waveform for one file case, and FM I/Q signals for two files with I file first.
`ammodindex=0`	AM index of modulation for sinusoidal waveform.
`ammodoffset=1`	AM offset of modulation for sinusoidal waveform.
`ammodfreq=0 Hz`	AM modulation frequency for sinusoidal waveform.
`ammodphase=0 ·`	AM phase of modulation for sinusoidal waveform.
`damp=0 1/s`	Damping factor for sinusoidal waveform.
`freqvec=[...] Hz`	Vector of support frequency of sinusoidal channel source.

© 2023 Cadence Design Systems, Inc.

`amplvec=[...] V`	Vector of amplitude of sinusoidal channel source.
`phasevec=[...] ·`	Vector of phase of sinusoidal channel source.
`maxharms=[...]`	Array of the number of harmonics of each frequency.

Exponential waveform parameters

`td1=0 s`	Rise start time for exponential wave.
`tau1 (s)`	Rise time constant for exponential wave.
`td2 (s)`	Fall start time for exponential wave.
`tau2 (s)`	Fall time constant for exponential wave.
`expperiod (s)`	Period of the periodic EXP waveform.
`expvec=[...]`	Vector of rise start time, rise time constant, fall start time, fall time constant and so on.

© 2023 Cadence Design Systems, Inc.

Pattern parameters

`data`	The bit string. A string that contains a series of the four states, 1 0 m z. For prbs, it can contain only 0 and 1; m and z are supported.
`rptstart=1`	The starting bit when repeating. The data repeats from the specified bit to the end of the bit string. The parameter should be an integer from 1 to the length of the bit string.
`rpttimes=0`	The repeat times. The output will maintain the state of the last bit after the last repeat. If its value is negative, the string repeats forever.
`td01=0 s`	Time delay for 0 to 1 transition.
`td10=0 s`	Time delay for 1 to 0 transition.

Prbs parameters

`ref (V)`	Sets the crossing reference for the control node. This parameter applies only when the Prbs source operates as a 3 or 4 terminal device. When the voltage across terminals 3 and 4 drops below ref, the output of the source is set to 0. If terminal 4 is not specified, it is assumed to be connected to ground.
`jitter (s)`	The parameter jitter is obsolete. It has no effect on the output.
`rjseed=1`	The seed for random number generator, used in generating random jitter for PRBS sources. The default value is 1.
`rjrms (s)`	When set for PRBS source or Bit source, the source has a normally distributed random jitter, whose mean is zero and whose standard deviation is rjrms.
`pjamp=[...] s`	When set for PRBS source or Bit source, the source has multiple periodic jitters, whose amplitudes are defined by pjamp and frequencies are defined by pjfreq.
`pjfreq=[...] Hz`	When set for PRBS source or Bit source, the source has multiple periodic jitters, whose amplitudes are defined by pjamp and frequencies are defined by pjfreq.

© 2023 Cadence Design Systems, Inc.

`pjtype="sine"`	For PRBS source or Bit source, pjtype defines the types of periodic jitters. Possible valudes are `sine`, `sawtooth`, and `square`.
`seed`	This parameter is obsolete, however, it is retained for backward compatability. Set `registerlength=[2 ... 32]` to choose a Maximum Length Sequence or define a custom PRBS by using lfsrtaps and lfsrseed parameters.
`taps=[...]`	For PRBS, taps is an integer array that sets the locations of the LFSR taps. For more information about the PRBS operation, see 'PRBS Type Waveform' section below. **Note**: The use of taps is discouraged, use lfsrtaps instead.
`lfsrtaps=[...]`	For PRBS source, lfsrtaps is an integer array that sets the location of LFSR taps. Locations are 1-based and ordered from MSB to LSB of the LFSR. The largest element of the taps array is equal to the width of the LFSR. For more information abput prbs source operation, see the 'PRBS Type Waveform' section below.
`lfsrseed=[...]`	For PRBS source, lfsrseed is an integer array that sets the initial state of an LFSR. Array elements set the location of non-zero bits. Locations are 1-based and ordered from MSB to LSB of the LFSR. For example, assume lfsrtaps=[6] and lfsrseed=[1 3 5]. The width of the register is then 6 bits and the initial state is '101010'.
`registerlength`	When set for PRBS, the registerlength parameter defines the width of the LFSR that works in Maximum Length Sequence mode. For more information about MLS setting see the 'PRBS Type Waveform' section below.
`triggerthreshold (V)`	For PRBS, when the triggerthreshold parameter is set and the source is instantiated with optional control terminals (terminals 3 and 4; if terminal 4 is unspecified, it is assumed to be connected to ground), the parameter defines the crossing threshold for the trigger event. The event causes the emission of the next PRBS pulse.
`triggerdelthresh (V)`	

© 2023 Cadence Design Systems, Inc.

	For PRBS in external triggering mode, the triggerdelthresh parameter is used with the triggerthreshold parameter to define the crossing threshold. For rising edge triggering, the threshold is (triggerthreshold + triggerdelthresh); for falling edge triggering, the threshold is (triggerthreshold - triggerdelthresh). The default value is zero.
`triggerdirection="both"`	For PRBS in external triggering mode, trigger direction defines the direction of the control signal at the crossing event. Possible values are 'rise', 'fall', and 'both'.
`transitionreference`	Defines the voltage swing for the duration of rise and fall time, as a percentage of val1 - val0. For example, transitionreference =100 means that the output voltage transitions from val0 to val1 in rise seconds. 90 means that it transitions from 0.1*(val1-val0) to 0.9*(val1-val0) in rise seconds, 80 means from 0.2*(val1-val0) to 0.8*(val1-val0), in rise seconds etc. Possible values are 100, 90, 80, 70 and 60.
`modulation=none`	Type of amplitude modulation; effective for bit and prbs sources. Possible values are `none` and `pam4`.
`pam4_mapping=0132`	The PAM4 mapping string specifies the mapping from a pair of bits to 4-level voltages. Possible values are: 123, 132, 213, 231, 312, 321, 0123, 0132, 0213, 0231, 0312, 0321, 1023, 1032, 1203, 1230, 1302, 1320, 2013, 2031, 2103, 2130, 2301, 2310, 3012, 3021, 3102, 3120, 3201, and 3210.

© 2023 Cadence Design Systems, Inc.

Osc Macro parameters

`oscmacrofile`	Name of the file containing the harmonic balance steady-state solution with/without phase noise data..
`freqscale`	Frequency scale factor.
`amplscale`	Amplitude scale factor.

Noise Parameters

`noisefile`	Name of the file containing excess spot noise data in the form of frequency-noise pairs. The noise can be specified as the spectral density in V^2/Hz, or as single-sideband phase noise in dBc. The parameter noisetype determines how Spectre interprets the noise data. Noise data file contains an optional parameter noisetype. Noisetype parameter in data file has identical definition to same parameter noisetype and supersedes it. It is intended to prevent misuse of the datafile.
`noisevec=[...]` V^2/Hz	Excess spot noise as a function of frequency in the form of frequency-noise pairs. The parameter noisetype determines how Spectre interprets the noise data.

`noisetype=noisevoltage`

© 2023 Cadence Design Systems, Inc.

	`noisetype` parameter specifies the units and source of noise data. When this parameter is set to `noisevoltage`, the noise data represents the noise spectral density in V^2/Hz of noise measured at the output of a driven circuit. When set to `ssbphasenoise`, the noise data represents the single-sideband phase noise in dBc measured at the output of a free oscillator. When set to `edgephasenoise`, the noise data represents the single-sideband phase noise in dBc measured at the output of a driven or oscillator circuit in sampled pnoise/hbnoise jitter analysis. For `noisetype=noisevoltage`, the frequencies are taken as absolute. For `ssbphasenoise` and `edgephasenoise`, the frequencies are offset from the carrier. Note that `Noisetype=edgephasenoise` is tied to a specific sampling edge position and should be used only for simulating jitter at that given edge position. `Noisetype=ssbphasenoise` can be used only with pnoise, qpnoise, hbnoise analyses, the noise source will be ignored in transient noise and AC noise analyses. Possible values are `noisevoltage`, `ssbphasenoise` and `edgephasenoise`.
`noiseinterp=linear`	
	Determines how the specified noise data is interpolated. This parameter only applies to noisetype=noisevoltage. When set to linear, interpolation is linear over both axes. When set to loglog, Spectre uses log interpolation over both axes. Possible values are `linear` and `loglog`.
`isnoisy=yes`	Determines whether vsource should generate noise. Possible values are `yes` and `no`.

© 2023 Cadence Design Systems, Inc.

Small signal parameters

`mag=0 V`	Small signal voltage.
`phase=0 ·`	Small signal phase.
`xfmag=1 V/V`	Transfer function analysis magnitude.
`pacmag=0 V`	Periodic AC analysis magnitude.
`pacphase=0 ·`	Periodic AC analysis phase.

Multiplication factor parameters

`m=1`	Multiplicity factor.

Temperature effects parameters

`tc1=0 1/C`	First-order temperature coefficient.
`tc2=0 C`$^{-2}$	Second-order temperature coefficient.
`tnom=27 C`	Parameter measurement temperature. Default set by options.
`trise=0.0 C`	Temperature rise from ambient.

If you do not specify the DC value, it is assumed to be the `time`=0 value of the waveform.

Sinusoidal waveform in the time interval `0<t<delay` has constant value equal to that at `t=delay`.

In DC analyses, the only active parameters are `dc`, `m`, and the temperature coefficient parameters. In AC analyses, the only active parameters are `m`, `mag` and `phase`. In transient analyses, all parameters are active except the small signal parameters and the noise parameters. The `type` parameter selects which type of waveform is generated. You may specify parameters for more than one waveform type, and use the `alter` statement to change the waveform type between analyses. There is one exception for type `bit`. You cannot change the type `bit` to other types or other types to the type `bit`.

© 2023 Cadence Design Systems, Inc.

PWL Type Waveform

A vector of time-value pairs describes the piecewise linear waveform. Alternatively, you can read the waveform from a file. In this case, you can specify the time-value pairs, one pair per line with a space or tab between the time and the value.

The input file may also contain design variables. For example, the input file can have time, value, or both time and value as variables. The expressions may also contain empty spaces.

If you set `allbrkpts` to `yes`, you force the simulator to place time points at each point specified in a PWL waveform during a transient analysis. This can be expensive for waveforms with many points. If you set `allbrkpts` to `no`, Spectre inspects the waveform, looking for abrupt changes, and forces time points only at those changes.

The PWL waveform is periodic if you specify `pwlperiod`, `pwlperiodstart` and `pwlperiodstop`. If both `pwlperiod` and `pwlperiodstart` are specified, `pwlperiod` should be greater than `wavelength` - `pwlperiodstart`, where `wavelength` means the last time point. If only `pwlperiod` is specified and `pwlperiodstart` is undefined, the period starts at the first time point or `wavelength` - `pwlperiod`, whichever is greater. If only `pwlperiodstart` is specified and `pwlperiod` is undefined, the period ends at the last time point in the waveform vector. If `pwlperiodstop` is defined, the waveform stops the repeat at the specified time, and the source value changes to `pwlperiodstopvalue` at the time period specified by `pwlperiodstopslope`. If the value of the waveform specified is not the same at both the period beginning and the period end, you must provide a non-zero value for`twidth`. Before repeating, the waveform changes linearly in an interval of `twidth` from its value at `period` - `twidth` to its value at the beginning of the waveform. Therefore, `twidth` must always be less than `period`.

Bit Type Waveform

Bit type waveform is the analog waveform of a series of digital logic state. It uses the pattern parameters to provide the digital state sequence, and some pulse waveform parameters to define the waveform characteristics.

To define the waveform characteristics, use the following parameters: val1, val0, rise, fall, and period. The parameter period defines the length of a bit and it must be given. The general parameter delay can also be used for bit type to define the delay time from the beginning of the transient interval to the beginning of the first bit. The state during the delay time is the same as the first state specified in data.

Pattern parameters are used to specify the digital bit string. The pattern parameters of sources are the same as those of a pattern, except that you can specify rpttimes to a negative number for sources but not for patterns. For more information on how to use pattern parameters run the `spectre -h pattern` command.

© 2023 Cadence Design Systems, Inc.

Prbs Type Waveform

When `type=prbs`, the source emits a pseudo-random bit sequence. The sequence is defined by the LSB of a Fibonacci Linear Feedback Shift Register (LFSR) at trigger events.

The LFSR is initially loaded by a 'seed'. The value fed back to the input (MSB) is given by feedback=tap_1 ^ tap_2 ^...^ tap_N, where ^ represents an exclusive-or operation, and tap_i represents the i-th bit of the register, counting from 1 and starting from the MSB. At a trigger event, the LFSR is shifted to the right and the MSB is given by the 'feedback'.

LFSR Modes

The sequence can be defined by custom values of seeds and taps. Alternatively, you can specify a maximum length sequence by setting the length of the LFSR. To specify custom seeds and taps, use the lfsrseed and lfsrtaps arrays. To specify a maximum length sequence, use the parameter, registerlength=[2 ... 32]. Spectre sets the seeds and taps automatically. You can optionally set lfsrseed to override the automatically chosen seed.

Triggering Mode

By default, the sequence is triggered by an internal clock and pulses are emitted every 'period' seconds, excluding the optional jitter. Alternatively, you can apply an external clock to the optional 3rd and 4th terminals. In external trigger mode, the pulses are emitted when the clock crosses the specified threshold in the specified direction. The threshold is defined by the triggerthreshold parameter and the direction is specified by triggerdirection. In external trigger mode, the jitter and bit period parameters are ignored.

Jitter

Let {s_i} be a sequence of ones and zeros whose transitions occur at intervals given by n*T + j(t), where T is the bit duration. Then, borrowing Verilog-A terminology, the jittered output is given by s(t+j(t)) = transition(s_i? Vhigh : Vlow, rise, fall). j(t) = rj(t) + pj(t), where rj (random jitter) is a normally distributed random variable whose mean is 0 and standard deviation is given by the parameter rjrms; and pj is the periodic jitter whose amplitude is pjamp and whose frequency is pjfreq. The parameter, pjtype, defines the type of jitter waveform. For sine, the periodic jitter is given by pj(t) = pjamp*cos(2*pi*pjfreq*t). Other types are square and sawtooth.

Exponential Type Waveform

There are two types of definitions for an exponential function that result in different waveforms:

© 2023 Cadence Design Systems, Inc.

1. Define the exponential function with `val0`, `val`, `td1`, `tau1`, `td2`, and `tau2` parameters. For example:

```
V1 (n1 0) vsource type=exp val0=0 val1=5 td1=1u tau1=30u td2=40u tau2=60u
```

The waveform is calculated, as shown below.

Time	Value
0 to td1	val0
td1 to td2	val0 + (val1 - val0) * (1 - exp (- (Time - td1) / tau1))
td2 to tstop	val0 + (val1 - val0) * (1 - exp (- (Time - td1) / tau1)) + (val0 - val1) * (1 - exp (- (Time - td2) / tau2))

2. Define the exponential function with `val0`, `val1`, and `expvec` parameters. For example:

```
V2 (n2 0) vsource type=exp val0=0 val1=5 expvec=[1u 30u 40u 60u 100u 30u 140u
60 u]
```

The waveform is calculated, as shown below.

Time	Value
0 to td1	val0
td1 to td2	val0 + (val1 - val0) * (1 - exp (- (Time - td1) / tau1))
td2 to td3	val0 + (val1 - val0) * (1 - exp (- (td2 - td1) / tau1)) + (val0 - val1) * (1 - exp (- (Time - td2) / tau2))
td3 to td4	val0 + (val1 - val0) * (1 - exp (- (td2 - td1) / tau1)) + (val0 - val1) * (1 - exp (- (td3 - td2) / tau2))+ (val1 - val0) * (1 - exp (- (Time - td3) / tau3))

Here, `tstop` is the transient stop time and `Time` is the transient time.

If only one pair of `td` and `tau` parameters is specified, the waveforms for both the definitions are the same. However, if more than one pair of `td` and `tau` parameters are specified, the waveforms for both the definitions are different.

The `expperiod` parameter defines the period of repeating waveform; waveform from `td1` to `td1+expperiod` is repeated.

Noise of the source

You can specify the excess noise of the source as a file or specify it with a vector of frequency-noise pairs. In the file, specify the frequency-noise pairs as pair per line with a space or a tab between the frequency and noise values.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.

Operating-Point Parameters

`v (V)`	Voltage across the source.
`i (A)`	Current through the source.
`pwr (W)`	Power dissipation.

Related Topics

Linear Voltage Controlled Voltage Source (vcvs)

Voltage Sources

Circuit Components

z-Domain Current Controlled Voltage Source (zccvs)

The output is defined with a transfer function given as the ratio of two polynomials in the complex variable z. Each polynomial can be specified using either its coefficients or its roots. The roots of the numerator are the zeros of the transfer function and the roots of the denominator are the poles.

You may specify polynomials either in the complex variable z or 1/z by setting optional parameter `polyarg` to `z` or `inversez` respectively. By default, it is set to `inversez`. If you choose to provide the coefficients of a polynomial, enter them as a vector in ascending order of the power of the variable z or 1/z, starting from the constant term. For example, to specify a denominator of 3z^-2 + 4z^-1 + 1, use `denom=[1 4 3]`. Or to specify a denominator of 4z^2 + 3z - 2, use `polyarg=z denom=[2 3 4]`.

To specify transfer function in terms of its zeros and poles in z-plane, give them as vectors of complex numbers. You must always give the real and imaginary portions of the root, even when the root is real. You may give either both roots of a complex-conjugate pair or only one. In the latter case the conjugate complex root will be generated automatically. The order of the roots is not important. For example, to specify poles of z = 1, z = 4j, z = -4j, z = 2 + 2j, and z = 2 - 2j, use `poles=[1 0 0 4 0 -4 2 2 2 -2]` or, omitting conjugate poles, `poles=[1 0 0 4 2 2 ]`.

© 2023 Cadence Design Systems, Inc.

Either the numerator or the denominator specification can be omitted. An omitted denominator or numerator is taken to be 1.

Transition time (`tt`) is an optional parameter that at each sampling point forces linear transition of the output to a new value within the specified time range. By default, it is set to one percent of the sampling period.

The sampling delay (`td`) is another optional parameter, with the default value of 0, that lets you set asynchronous sampling rates.

To use the `s` to `z` transformation, set the optional `sxz` parameter to one of the transformation methods - forward differences, backward differences, or bilinear. When the `sxz` parameter is specified, the transfer function specification is assumed to be given in the complex variable s and it will be transformed to the complex variable z using the indicated method.

Notes on gain and gainfactor

The parameter `gain` is interpreted either as the DC gain or, if the function has zeros or poles at the origin, as a constant factor. `gain` has a default value of 1, so if you do not want to specify the DC gain, you should always use parameter `gainfactor` to disable parameter `gain`. When `gainfactor` is specified, `gain` is not valid any more. For example, if the instant statement is:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4]

the transfer function will be 2*(2s+1)/(4s+3). Factor 2 is applied to make the DC gain of the transfer function to be 1. If you just want the transfer function to be (2s+1)/(4s+3), specify `gainfactor=1` to disable the default value of `gain`. In this example, the statement will be:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4] gainfactor=1

where the transfer function is 1*(2s+1)/(4s+3). 1 is the gainfactor.

This device is not supported within altergroup.

Sample Instance Statement

```
va (1 0) vsource type=sine freq=10K
z2 2 0 zccvs probe=va gain=-2 ts=5e-5 tt=1.1e-5 numer=[1 -1]
```

Instance Syntax

```
Name  p  n zccvs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`probe`	Device through which the controlling current flows.
`mprobe`	The mprobe functions the same as probe except that it will divide the input current by the mfactor.
`port=0`	Index of the probe port through which the controlling current flows.
`ts=1 s`	Sampling period.
`td=0 s`	Sampling delay.
`tt=0.01 ts s`	Transition time.
`gain=1`	DC gain or constant transfer function factor. See `notes on gain and gainfactor` for details.
`gainfactor`	Factor applied to transfer function. It overwrites the parameter gain.
`polyarg=inversez`	Polynomial argument. Possible values are `z` or `inversez`.
`sxz=none`	s to z transformation. Possible values are `none`, `backward`, `forward`, or `bilinear`.
`numer=[...]`	Vector of numerator coefficients.
`denom=[...]`	Vector of denominator coefficients.
`zeros=[...]`	Vector of complex zeros.
`poles=[...]`	Vector of complex poles.
`m=1`	Multiplicity factor.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

z-Domain Voltage Controlled Voltage Source (zvcvs)

Voltage Sources

Circuit Components

z-Domain Voltage Controlled Voltage Source (zvcvs)

The output is defined with a transfer function given as the ratio of two polynomials in the complex variable z. Each polynomial can be specified using either its coefficients or its roots. The roots of the numerator are the zeros of the transfer function and the roots of the denominator are the poles.

You may specify polynomials either in the complex variable z or 1/z by setting optional parameter `polyarg` to `z` or `inversez` respectively. By default, it is set to `inversez`. If you choose to provide the coefficients of a polynomial, enter them as a vector in ascending order of the power of the variable z or 1/z, starting from the constant term. For example, to specify a denominator of 3z^-2 + 4z^-1 + 1, use `denom=[1 4 3]`. Or to specify a denominator of 4z^2 + 3z - 2, use `polyarg=z denom=[2 3 4]`.

To specify transfer function in terms of its zeros and poles in z-plane, give them as vectors of complex numbers. You must always give the real and imaginary portions of the root, even when the root is real. You may give either both roots of a complex-conjugate pair or only one. In the latter case the conjugate complex root will be generated automatically. The order of the roots is not important. For example, to specify poles of z = 1, z = 4j, z = -4j, z = 2 + 2j, and z = 2 - 2j, use `poles=[1 0 0 4 0 -4 2 2 2 -2]` or, omitting conjugate poles, `poles=[1 0 0 4 2 2 ]`.

Either the numerator or the denominator specification can be omitted. An omitted denominator or numerator is taken to be 1.

© 2023 Cadence Design Systems, Inc.

Transition time (`tt`) is an optional parameter that at each sampling point forces linear transition of the output to a new value within the specified time range. By default, it is set to one percent of the sampling period.

The sampling delay (`td`) is another optional parameter, with the default value of 0, that lets you set asynchronous sampling rates.

To use the `s` to `z` transformation, set the optional `sxz` parameter to one of the transformation methods - forward differences, backward differences, or bilinear. When the `sxz` parameter is specified, the transfer function specification is assumed to be given in the complex variable s and it will be transformed to the complex variable z using the indicated method.

Notes on gain and gainfactor

The parameter `gain` is interpreted either as the DC gain or, if the function has zeros or poles at the origin, as a constant factor. `gain` has a default value of 1, so if you do not want to specify the DC gain, you should always use parameter `gainfactor` to disable parameter `gain`. When `gainfactor` is specified, `gain` is not valid any more. For example, if the instant statement is:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4]

the transfer function will be 2*(2s+1)/(4s+3). Factor 2 is applied to make the DC gain of the transfer function to be 1. If you just want the transfer function to be (2s+1)/(4s+3), specify `gainfactor=1` to disable the default value of `gain`. In this example, the statement will be:

s1 (1 0 control 0) svcvs numer=[1 2] denom=[3 4] gainfactor=1

where the transfer function is 1*(2s+1)/(4s+3). 1 is the gainfactor.

This device is not supported within altergroup.

Sample Instance Statement:

va (1 0) vsource type=sine freq=10K

z3 (3 0 1 0) zvcvs gain=-1 ts=4e-5 tt=1e-5 numer=[-1 -1]

© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  p  n  ps  ns zvcvs parameter=value ...
```

Instance Parameters

`ts=1 s`	Sampling period.
`td=0 s`	Sampling delay.
`tt=0.01 ts s`	Transition time.
`gain=1`	DC gain or constant transfer function factor. See `notes on gain and gainfactor` for details.
`gainfactor`	Factor applied to transfer function. It overwrites the parameter gain.
`polyarg=inversez`	Polynomial argument. Possible values are `z` or `inversez`.
`sxz=none`	s to z transformation. Possible values are `none`, `backward`, `forward`, or `bilinear`.
`numer=[...]`	Vector of numerator coefficients.
`denom=[...]`	Vector of denominator coefficients.
`zeros=[...]`	Vector of complex zeros.
`poles=[...]`	Vector of complex poles.
`m=1`	Multiplicity factor.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`trise=0.0K`	Temperature rise from ambient.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`i (A)`	Output current.
`v (V)`	Output voltage.
`pwr (W)`	Power dissipation.

Related Topics

z-Domain Current Controlled Voltage Source (zccvs)

Voltage Sources

Circuit Components

Behavioral Source (bsource)

Behavioral source enables you to model a resistor, inductor, capacitor, voltage or current source as a behavioral component. Using bsource, you can express the value of a resistance, capacitance, voltage or current as a combination of device operating points, node voltages, branch currents, and built in Spectre® circuit simulator expressions. `bsource` simulation performance has now been improved by compiling the bsource devices.

Bsource simulation performance has been improved by compiling the bsource devices. This is explained in more detail in the bsource compilation section below.

Sample Instance Statement

```
name (node1 node2) bsource behav_param param_list
```

where behav_param can be

`c=simple_expr`	Capacitance between the nodes
`g=simple_expr`	Conductance between the nodes
`i=generic_expr`	Current through bsource
`l=simple_expr`	Inductance between the nodes
`phi=simple_expr`	Flux in the bsource device
`q=simple_expr`	Charge in bsource device

© 2023 Cadence Design Systems, Inc.

`r=simple_expr`	Resistance between the nodes
`v=generic_expr`	Voltage across the nodes

A simple_expr is defined as a spectre expression containing,

1. netlist parameters
2. current simulation time, $time
3. node voltages, v(a,b), where a and b are nodes in the spectre netlist or v(a), which is voltage between node a and ground
4. branch currents, i("inst_id:index"), where inst_id is an instance name given in the netlist and index is the port index. The default value for index is 0.

A generic_expr is defined as a simple_expr or ddt() or idt() of simple_expr. The param_list is param_name=value.

Multiplicity factor

`m`	The value of m will be default to1.

© 2023 Cadence Design Systems, Inc.

Temperature Parameters

`tc1`	Linear temperature co-efficient. Valid for all behavioral elements. Default value is 0 1/C.
`tc2`	Quadratic temperature co-efficient. Valid for all behavioral elements. Default value is 0 C^-2
`tnom`	Parameters measurement temperature. Valid for all behavioral elements. Default value is 27.0.
`trise`	Temperature rise for ambient. Valid for all behavioral elements. Default value is 0.0.
`T`	Effective value of temperature. Valid for all behaviroal elements. Default value is `temp+trise-tnom`.
`tc1c`	Linear temperature coefficient of capacitor. valid for transistor type behavioral element. Default is 0 1/C
`tc2c`	Quadratic temperature coefficient of capacitor. valid for transistor type behavioral element. Default is 0 C^{-2}

Clipping Parameters

`max_val`	Maximum value of bsource expression. Valid for all behavioral elements, but mostly used with i and v elements for clipping the current or voltage between the specified values.
`min_val`	Minimum value of bsource expression. Valid for all behavioral elements, but mostly used with i and v elements for clipping the current or voltage between the specified values.
`bv_max`	Generate a warning when bsource voltage of two terminals exceeds the value specified by `bv_max`.

Noise Parameters

`af`	Flicker noise exponent, Valid for r and g elements Default value is 2.
`fexp`	Flicker noise frequency exponent. Valid for r, g, v, and i elements. Default value is 1.

© 2023 Cadence Design Systems, Inc.

`ef`	Alias of `fexp`.
`ldexp`	Flicker (1/f) noise L component. Valid for r and g elements. Default value is 1.0.
`lf`	Alias of `ldexp`.
`wdexp`	Flicker (1/f) noise W component. Valid for r and g elements. Default value is 1.0.
`wf`	Alias of `wdexp`.
`isnoisy`	Specifies whether to generate noise. Valid for r, g, i, and v elements Valid values are yes and no. Default value is yes.
`kf`	Flicker noise co-efficient. Valid for r and g elements.
`white_noise`	White noise expression. Valid for v and i elements.
`flicker_noise`	Flicker noise expression. Valid for v and i elements.

DC Mismatch Parameters

`mr`	DC-Mismatch parameter. Valid only for r.

Other Parameters

`scale/scaleb/ scaler/scalei/ scalec`	Bsource scaling factor. Default value is 1.0.
`ctype`	Different implementations of a capacitor. When the value is 1, bsource current is `ddt(cap*V(node1, node2))`, where `cap` is the bsource capacitor value with temp effect, mfactor effect, scale effect and so on. `V(node1, node2)` is the voltage between the bsource terminals. When the value is 2, the current is `ddt(cap)`. When the value is 0, or any other value, the current value is `cap*ddt(V(node1, node2))`.

Note: All the parameters in the param_name table are instance parameters. `white_noise` and `flicker_noise` may be assigned behavioral expressions; the other parameters must be assigned constant or parametric expressions.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

`bsource` supports the following instance parameters for the Spectre primitives.

`Resistor`	isnoisy, m, r, tc1, tc2, trise, kf, af, fexp, ldexp, wdexp, l, w, mr.
`Capacitor`	c, m, tc1, tc2, trise, ic.
`Inductor`	l, m, tc1, tc2, trise.

Related Topics

Mathematical Definitions

Noise Model for bsource

Circuit Components

Mathematical Definitions

The i and v elements are current and voltage sources respectively with the current and voltage values specified by the generic_expression.

The `q` and `phi` elements are defined as:

(1-1)

$$i = ddt(q)) = ddt(simple_\text{expr})$$

(1-2)

$$v = ddt(phi) = ddt(simple_\text{expr})$$

The `r`, `g`, `c`, and `l` elements are defined as:

(1-3)

$$v = i \times r = i \times (simple_\text{expr})$$

(1-4)

$$i = g \times v = (simple_\text{expr}) \times v$$

© 2023 Cadence Design Systems, Inc.

(1-5)

$$i = c \times ddt(v) = (simple_\text{expr}) \times ddt(v)$$

(1-6)

$$v = l \times ddt(i) = (simple_\text{expr}) \times ddt(i)$$

The elements `r`, `g`, `c`, and `l` are provided for compatibility reasons. The correct resistance, conductance, capacitance, and inductance are different from the expressions you specify. For example, a non-linear conductance is defined as:

(1-7)

$$g(v) = \frac{di}{dv}$$

where i and v are the conductance branch current and voltage respectively. If we use the conductance element (equation 5-4), and specify the conductance as a function of the branch voltage:

(1-8)

$$g = g_s(v)$$

then the true conductance is given by:

(1-9)

$$g(v) = \frac{d}{dv}(g_s(v) \times v)$$

(1-10)

$$g(v) = g_s(v) + v\left(\frac{d}{dv} g_s v\right)$$

Note: The true conductance is different from the specified conductance. The correct way to implement a conductance $g_s(v)$ is to use the `i` element and specify the current expression as:

(1-11)

$$i = \int g_s(v) dv$$

© 2023 Cadence Design Systems, Inc.

Related Topics

Behavioral Source (bsource)

Noise Model for bsource

Temperature Effect on bsource

Circuit Components

Noise Model for bsource

Noise sources are implemented for the elements i, v, r, and g.

Noise for Elements i and v

You need to specify the expression for Power Spectrel Density (PSD) using the *white_noise* and *flicker_noise* parameters.

(1-12)

$$white_\text{noise} = simple_\text{expr}$$

(1-13)

$$flicker_\text{noise} = simple_\text{expr} \qquad \text{fexp} = constant_\text{expr}$$

where *simple_expr* is the power of the flicker noise (or white noise) source at 1Hz and *fexp* is the exponent of the frequency.

(1-14)

$$noisePSD = \frac{simple_\text{expr}}{f^{fexp}}$$

The noise source unit is A^2/Hz for `i` and V^2/Hz for `v`. The following is an example of a noise parameter specification for a current source:

(1-15)

$$white_\text{noise} = 4 \times k \times T \times g$$

where k is the Boltzman constant (1.380626e-23) and

© 2023 Cadence Design Systems, Inc.

T is the temperature.

(1-16)

$$flicker_\text{noise} = kf \times pow((g \times V(p,n)), af)\ fexp = 2$$

where $V(p,n)$ is the voltage across the `i` element.

The following is an example of a noise parameter specification for a voltage source:

(1-17)

$$white_\text{noise} = 4 \times k \times T \times r$$

(1-18)

$$flicker_\text{noise} = kf \times (r \times pow(i(\text{""inst_name:0}), af))fexp = 2$$

Noise for elements g and r

The syntax is:

```
name (node1 node2) bsource { r | g }=simple_expr kf=value af=value fexp=value
     isnoisy={ yes | no }
```

The white_noise and flicker_noise values are calculated from the above expression. When `isnoisy=no`, noise contributions are turned off. By default the white noise source is on and the flicker noise source is off (default is `kf=0`).

The noise source for g is a current source in parallel with the g element and the noise power is in units of A^2/Hz. If x is the expression for the g element,

(1-19)

$$white_\text{noise} = 4 \times k \times T \times x$$

(1-20)

$$flicker_\text{noise} = \frac{kf \times (x \times v(p,n))^{af}}{freq^{fexp}}$$

where kf, af, and $fexp$ are the values specified for these parameters

k is the Boltzman constant (1.380626e-23)

© 2023 Cadence Design Systems, Inc.

T is the temperature and

v(p,n) is the voltage across the g element.

The noise source for r is a current source in parallel with the r element and the noise power is in units of V^2/Hz. If x is the expression for the r element,

(1-21)

$$white_\text{noise} = 4 \times k \times T \times x$$

(1-22)

$$flicker_\text{noise} = \frac{kf \times (x \times I(relement))^{af}}{freq^{fexp}}$$

where *kf*, *af*, and *fexp* are the values specified for these parameters

k is the Boltzman constant (1.380626e-23)

T is the temperature and

I(relement) is the current through r element.

Temperature Effect on bsource

The equation for calculating temperature effect is:

(1-23)

$$tempFactor = [1 + tc1 \times (temp + trise - tnom) + tc1 \times (temp + trise - tnom)^2]$$

Related Topics

Behavioral Source (bsource)

Mathematical Definitions

Circuit Components

© 2023 Cadence Design Systems, Inc.

Independent Resistive Source (port)

In time-domain, a port is a resistive source that is tied between `pos` and `neg`. It is equivalent to a voltage source in series with a resistor, and the reference resistance of the port is the value of the resistor. The DC value given for the port voltage specifies the DC voltage across the port when it is terminated in its reference resistance (in other words, the DC voltage of the internal voltage source is double the user specified DC value, `dc`). The same is true for the values for the transient, and PAC signals of the port. However, the amplitude of the sine wave in the transient and PAC analyses can alternatively be specified as the power in dBm delivered by the port when terminated with the reference resistance. In frequency-domain, a port can have complex reference impedance. The value of AC signal of the port specifies the voltage across the port when it is terminated in its complex conjugate reference impedance. The reactance part of the impedance is ignored when the port is used in time-domain analyses.

While useful as a stimulus in high frequency circuits, the port has three unique capabilities. First, it acts to define the ports of the circuit to the S-parameter analysis. Second, it has an intrinsic noise source, and so allows the noise analysis to directly compute the noise figure of the circuit. And finally, it is the only source for which the amplitude can be specified in terms of power.

You can define 2 or 3 terminal port. if you define 2-terminal port it operates like was described above. In case of 3-terminal port it also includes internal ideal choke inductor and ideal blocking capacitor. They are work like switches to terminate or connect appropriate branch dependent on type of analysis

This device is not supported within altergroup.

The value of the DC voltage as a function of the temperature is given by:

$$V(T) = V * [1 + tc1 * (T - tnom) + tc2 * (T - tnom)^2].$$

Sample Instance Statement

```
p20 (2 0) port num=2 r=50 type=pulse period=1e-9 rise=1e-10 fall=1e-10 val1=1
width=0.5n mag=1
 p30 (2 0 choke) port num=1 r=50 lchoke=0.1 cblock=0.00001 type=pulse period=1e-9
rise=1e-10 fall=1e-10
```

Instance Syntax

```
Name  p  n ... port parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`dc=0 V`	DC value.

General waveform parameters

`type=dc`	Waveform type. Possible values are `dc`, `pulse`, `pwl`, `sine`, `exp`, `bit`, `prbs`, `pwlz`, `sigbus`, `oscmacro`, and `pwr`.
`fundname`	Name of the fundamental frequency. Must be specified if the source is active during a qpss analysis or it is the active clock during an envlp analysis.
`delay=0 s`	Waveform delay time.
`edgetype=linear`	Type of the rising and falling edges. This is for pulse waveform and pulse-like piecewise linear waveform. Possible values are `linear` or `halfsine`.

Pulse waveform parameters

`val0=0 V`	Zero value used in pulse and exponential waveforms.
`val1=1 V`	One value used in pulse and exponential waveforms.
`period=∞ s`	Period of waveform.
`rise (s)`	Rise time for pulse waveform (time for transition from `val0` to `val1`). If parameter rise is not given, then the rise time will be the same as fall time; if fall time is not given either, then the rise time will be 1/100 of the waveform period; if the waveform is not periodic, then the rise time will be 1/100 of the simulation interval.
`fall (s)`	Fall time for pulse waveform (time for transition from `val1` to `val0`). If parameter fall is not given, then the fall time will be the same as rise time; if rise time is not given either, then the fall time will be 1/100 of the waveform period; if the waveform is not periodic, then the fall time will be 1/100 of the simulation interval.
`width=∞ s`	Pulse width (duration of `val1`).

© 2023 Cadence Design Systems, Inc.

PWL waveform parameters

`file`	Name of file containing waveform.
`wave=[...]`	Vector of time/value pairs that defines waveform.
`offset=0 V`	DC offset for the PWL waveform.
`scale=1`	Scale factor for the PWL waveform.
`pwldbm (dBm)`	Power of PWL waveform in dBm (alternative to `scale`).
`stretch=1`	Scale factor for time given for the PWL waveform.
`rms`	Desired rms(root of mean squre) value of the PWL waveform.
`pwlfilter=none`	Add filter to pwl source, where the pwl data should be equal space sampled. Possible values are 'nrc'(normal raised cosine filter) and 'none'. Possible values are `none` and `nrc`.
`rolloff`	Desired rolloff factor for the raised cosine filter, default value is 0.2. Only valid when 'pwlfilter' is set to nrc.
`pwlbandwidth`	Bandwidth of the pwl input signal. Be used when 'pwlfilter' is set to nrc.
`allbrkpts`	All the points in the PWL waveform are breakpoints if set to yes. Default is yes if the number of points is less than 20. Possible values are `yes` and `no`.
`pwlperiod (s)`	Period of the periodic PWL waveform.
`pwlperiodstart (s)`	Period start time of the periodic PWL waveform.
`pwlperiodstop (s)`	Period stop time of the periodic PWL waveform.
`pwlperiodstopvalue`	Value of the source at the time of pwlperiodstop.
`pwlperiodstopslope=30p s`	Switching time from the last PWL value to the stopvalue.
`twidth=pwlperiod/1000 s`	Transition width used when making PWL waveforms periodic.
`highz=1e12`	The impedance of high z state.

© 2023 Cadence Design Systems, Inc.

`min_z_transition_width=10e-12 s`	Minimum width of transition from z-state to non z-state. The width of transition is set as 1e-3*(z-state duration).
`min_zx_transition_width=DBL_MAX s`	Minimum width of transition from z-state.
`min_xz_transition_width=DBL_MAX s`	Minimum width of transition to z-state.
`zx_transition_width=DBL_MAX s`	Width of transition from z-state.
`xz_transition_width=DBL_MAX s`	Width of transition to z-state.
`max_zx_transition_width=DBL_MAX s`	Maximal width of transition from z-state.
`max_xz_transition_width=DBL_MAX s`	Maximal width of transition to z-state.
`max_z_transition_width=DBL_MAX s`	Maximal width of transition related to z-state.
`tdvalue`	PWL wave value before time=td.
`abstime=1`	Possible value is '0' or '1'. if set to 0, then the time specified by wave or file is time increase compared with last point.

© 2023 Cadence Design Systems, Inc.

Sinusoidal waveform parameters

`sinedc=dc V`	DC level for sinusoidal waveforms.
`ampl=1 V`	amplitude of sinusoidal waveform.
`dbm (dBm)`	Amplitude of sinusoidal waveform in dBm (alternative to `ampl`).
`freq=0 Hz`	Frequency of sinusoidal waveform.
`sinephase=0 ·`	Phase of sinusoid when `t=delay`.
`ampl2=1 V`	amplitude of second sinusoidal waveform.
`dbm2 (dBm)`	Amplitude of second sinusoidal waveform in dBm (alternative to `ampl2`).
`freq2=0 Hz`	Frequency of second sinusoidal waveform.
`sinephase2=0 ·`	Phase of second sinusoid when `t=delay`.
`fundname2`	Name of the fundamental frequency associated with freq2. Must be specified if freq2 is used in a qpss analysis.
`iqmodfiles=[...]`	Two file names which containing pwl I/Q source waveform.
`fmmodindex=0`	FM index of modulation for sinusoidal waveform.
`fmmodfreq=0 Hz`	FM modulation frequency for sinusoidal waveform.
`fmmodfiles=[...]`	One or two file names: containing FM waveform for one file case, and FM I/Q signals for two files with I file first.
`ammodindex=0`	AM index of modulation for sinusoidal waveform.
`ammodoffset=1`	AM offset of modulation for sinusoidal waveform.
`ammodfreq=0 Hz`	AM modulation frequency for sinusoidal waveform.
`ammodphase=0 ·`	AM phase of modulation for sinusoidal waveform.
`damp=0 1/s`	Damping factor for sinusoidal waveform.
`freqvec=[...] Hz`	Vector of support frequency of sinusoidal channel source.
`amplvec=[...] V`	Vector of amplitude of sinusoidal channel source.
`dbmvec=[...] dBm`	Vector of amplitude of sinusoidal waveform in dBm (alternative to `amplvec`).
`phasevec=[...] ·`	Vector of phase of sinusoidal channel source.
`maxharms=[...]`	Array of number of harmonics of each frequency.

© 2023 Cadence Design Systems, Inc.

Exponential waveform parameters

`td1=0 s`	Rise start time for exponential wave.
`tau1 (s)`	Rise time constant for exponential wave.
`td2 (s)`	Fall start time for exponential wave.
`tau2 (s)`	Fall time constant for exponential wave.
`expperiod (s)`	Period of the periodic EXP waveform.
`expvec[...]`	Vector of rise start time, rise time constant, fall start time, fall time constant, rise start time.

Pattern parameters

`data`	The bit string. A string that contains a series of the four states, 1 0 m z. For prbs, it can contain only 0 and 1, and m, z is not supported.
`rptstart=1`	The starting bit when repeating. The data repeats from the specified bit to the end of the bit string. The parameter should be an integer from 1 to the length of the bit string.
`rpttimes=0`	The repeat times. The output will maintain the state of the last bit after the last repeat. If its value is negative, the string repeats forever.
`td01=0 s`	Time delay for 0 to 1 transition.
`td10=0 s`	Time delay for 1 to 0 transition.

Prbs parameters

`ref (V)`	Sets the crossing reference for the control node. This parameter applies only when the Prbs source operates as a 3 or 4 terminal device. When the voltage across terminals 3 and 4 drops below ref, the output of the source is set to 0. If terminal 4 is not specified, it is assumed to be connected to ground.
`jitter (s)`	The parameter jitter is obsolete. It has no effect on the output.

© 2023 Cadence Design Systems, Inc.

`rjseed=1`	The seed for random number generator, used in generating random jitter for PRBS sources. The default value is 1.
`rjrms (s)`	When set for PRBS source or Bit source, the source has a normally distributed random jitter, whose mean is zero and whose standard deviation is rjrms.
`pjamp=[...] s`	When set for PRBS source or Bit source, the source has multiple periodic jitters, whose amplitudes are defined by pjamp and frequencies are defined by pjfreq.
`pjfreq=[...] Hz`	When set for PRBS source or Bit source, the source has multiple periodic jitters, whose amplitudes are defined by pjamp and whose frequency are defined by pjfreq.
`pjtype="sine"`	For PRBS source or Bit source, pjtype defines the types of periodic jitters. Possible valudes are 'sine', 'sawtooth', or 'square'.
`seed`	This parameter is obsolete but retained for backward compatability. Set registerlength=[2 ... 32] to choose a Maximum Length Sequence or define a custom PRBS by use of the parameters, lfsrtaps and lfsrseed.
`taps=[...]`	The use of taps is discouraged. For PRBS, taps is an integer array which sets the locations of the LFSR taps. Use lfsrtaps instead. See section, 'PRBS Type Waveform' below for details of the PRBS operation.
`lfsrtaps=[...]`	For PRBS source, lfsrtaps is an integer array which sets the location of LFSR taps. Locations are 1-based and ordered form MSB to LSB of the LFSR. The largest element of the taps array is equal to the width of the LFSR. See section, 'PRBS Type Waveform' for details of PRBS source operation.
`lfsrseed=[...]`	For PRBS source, lfsrseed is an integer array which sets the initial state of the LFSR. Array elements sets the locations of non-zero bits. Locations are 1-based and ordered from MSB to LSB of the LFSR. For example, assume lfsrtaps=[6] and lfsrseed=[1 3 5]. The width of the register is then 6 bits and the initial state is '101010'.

© 2023 Cadence Design Systems, Inc.

`registerlength`	When set for PRBS, the registerlength defines the width of the LFSR and the LFSR works in Maximum Length Sequence mode. See section 'PRBS Type Waveform' below for details of MLS setting.
`triggerthreshold (V)`	For PRBS, when triggerthreshold is set and the source is instantiated with optional control terminals (terminals 3 and optionally 4; if terminal 4 is unspecified it is assumed to be connected to ground), triggerthreshold defines the crossing threshold for the trigger event. The event causes the emission of the next PRBS pulse.
`triggerdelthresh (V)`	For PRBS in external triggering mode, triggerdelthresh is used with triggerthreshold to define the crossing threshold. For rising edge triggering, the threshold is (triggerthreshold + triggerdelthresh); for falling edge triggering, the threshold is (triggerthreshold - triggerdelthresh). The default value is zero.
`triggerdirection="both"`	For PRBS in external triggering mode, trigger direction defines the direction of the control signal at the crossing event. Possible values are 'rise', 'fall', or 'both'.
`transitionreference`	Defines the voltage swing for the duration of rise and fall time, as a percentage of val1 - val0. For example, transitionreference =100 means that the output voltage transitions from val0 to val1 in rise seconds. 90 means that it transitions from 0.1*(val1-val0) to 0.9*(val1-val0) in rise seconds, 80 means from 0.2*(val1-val0) to 0.8*(val1-val0), etc. Possible values are 100, 90, 80, 70 and 60.
`modulation=none`	Type of amplitude modulation; effective for bit and prbs sources. Possible values are `none` and `pam4`.
`pam4_mapping=0132`	

© 2023 Cadence Design Systems, Inc.

	The PAM4 mapping string specifies the mapping from a pair of bits to 4-level voltages. Possible values are: 123, 132, 213, 231, 312, 321, 0123, 0132, 0213, 0231, 0312, 0321, 1023, 1032, 1203, 1230, 1302, 1320, 2013, 2031, 2103, 2130, 2301, 2310, 3012, 3021, 3102, 3120, 3201, and 3210.

Osc Macro Parameters

`oscmacrofile`	Name of the file containing the harmonic balance steady-state solution with/without phase noise data..
`freqscale`	Frequency scale factor.
`amplscale`	Amplitude scale factor.

Noise Parameters

`noisefile`	Name of file containing excess spot noise data in the form of frequency-noise pairs. The noise can be specified as the spectral density in V^2/Hz, or as single-sideband phase noise in dBc. The parameter noisetype determines how Spectre interprets the noise data. Noise data file contains an optional parameter noisetype. Noisetype parameter in data file has identical definition to same parameter noisetype and supersedes it. It is intended to prevent misuse of the datafile.
`noisevec=[...]` V^2/Hz	Excess spot noise as a function of frequency in the form of frequency-noise pairs. The parameter noisetype determines how Spectre interprets the noise data.

`noisetype=noisevoltage`

© 2023 Cadence Design Systems, Inc.

	`noisetype` parameter specifies the units and source of noise data. When this parameter is set to `noisevoltage`, the noise data represents the noise spectral density in V^2/Hz of noise measured at the output of a driven circuit. When set to `ssbphasenoise`, the noise data represents the single-sideband phase noise in dBc measured at the output of a free oscillator. When set to `edgephasenoise`, the noise data represents the single-sideband phase noise in dBc measured at the output of a driven or oscillator circuit in sampled pnoise/hbnoise jitter analysis. For `noisetype=noisevoltage`, the frequencies are taken as absolute. For `ssbphasenoise` and `edgephasenoise`, the frequencies are offset from the carrier. Note that `Noisetype=edgephasenoise` is tied to a specific sampling edge position and should be used only for simulating jitter at that given edge position. `Noisetype=ssbphasenoise` can be used only with pnoise, qpnoise, hbnoise analyses, the noise source will be ignored in transient noise and AC noise analyses. Possible values are `noisevoltage`, `ssbphasenoise` and `edgephasenoise`.
`noiseinterp=linear`	
	Determine how the specified noise data is interpolated. This parameter only applies to `noisetype=noisevoltage`. When set to linear, interpolation is linear over both axes. When set to loglog, Spectre uses log interpolation over both axes. Possible values are `linear` and `loglog`.
`noisetemp (C)`	Noise temperature of port. If not specified, the noise temperature is taken to be 290 K.
`isnoisy=yes`	Should port generate noise. Possible values are `yes` and `no`.

Port parameters

`r=50 Ω`	Reference resistance.
`x=0 Ω`	Reference reactance, ignored for time domain analyses.
`lchock=0.1 H`	Choke inductor for network analyser.

© 2023 Cadence Design Systems, Inc.

`lchoke=0.1 H`	Choke inductor for network analyser.
`cblock=0.0001 F`	Blocking capacitance for network analyser.
`num`	Port number.
`m=1`	Multiplicity factor.

Small signal parameters

`mag=0 V`	Small signal voltage.
`phase=0 ·`	Small signal phase.
`xfmag=1 V/V`	Transfer function analysis magnitude.
`pacmag=0 V`	Periodic AC analysis magnitude.
`pacdbm (dBm)`	Periodic AC analysis magnitude in dBm (alternative to `pacmag`).
`pacphase=0 ·`	Periodic AC analysis phase.

© 2023 Cadence Design Systems, Inc.

Temperature effects parameters

`tc1=0 1/C`	First order temperature coefficient.
`tc2=0` C^{-2}	Second order temperature coefficient.
`tnom (C)`	Parameters measurement temperature. Default set by options.

Harmonic balance parameters

`harmvec=[...]`	Harmvec, rvec, and xvec are considered together, and are only applied in harmonic balance large-signal analyses. Harmvec is a list of harmonics to have impedances set manually. If the input to the circuit has a single frequency, then this is a list of harmonics like [1 3] which would set the first and third harmonic. When there are two inputs, then each harmonic has two indexes. An example would be [2 -1 -1 2] which would set the harmonics 2, -1, and -1, 2 manually. When there are three inputs, then each harmonic has three indexes, and so on.
`rvec=[...]` Ω	Rvec is the list of series resistance values that go with the list of harmonics to be set manually. If there are three harmonics in the harmvec, for example [1 4 5] in a single tone analysis, then there must be three resistance values in rvec, like [60 70 80]. The order in the list corresponds to the order of harmvec. In this example, harmonic 5 gets set to 80 Ohms. All values must be specified. There is no default.
`xvec=[...]` Ω	Xvec is the list of series reactance values that go with the list of harmonics to be set manually. If there are two harmonics in the harmvec, for example [2 -1 1 -2] in a two tone circuit, then xvec must have two values, like [0 25]. The order in the list corresponds to the order of harmvec. In this example, harmonic 1, -2 gets set to 25 Ohms. All values must be specified. There is no default.
`ro=50` Ω	Series resistance for all the harmonics that are not set manually. This is also the value used in time-domain (transient and shooting PSS) and AC analyses.

© 2023 Cadence Design Systems, Inc.

`xo=0` Ω	This is used for the frequency-domain analyses only. This specifies the series reactance for all the harmonics that are not set manually. This value is ignored in time-domain analyses. It is used to represent the port impedance at all frequencies in AC analysis.

If you do not specify the DC value, it is assumed to be the `time`=0 value of the waveform.

Sinusoidal waveform in the time interval `0<t<delay` has constant value equal to that at `t=delay`.

In DC analyses, the only active parameters are `dc`, `m`, and the temperature coefficient parameters. In AC analyses, the only active parameters are `m`, `mag` and `phase`. In transient analyses, all parameters are active except the small signal parameters and the noise parameters. The `type` parameter selects which type of waveform is generated. You may specify parameters for more than one waveform type, and use the alter statement to change the waveform type between analyses. There is one exception for type `bit`. You cannot change `bit` type to other types or other types to `bit`.

Related Topics

Independent Resistive Source (port)

Mathematical Definitions

Circuit Components

PWL Type Waveform

A vector of time-value pairs describes the piecewise linear waveform. As an alternative, you can read the waveform from a file. In this case, you give time-value pairs one pair per line with a space or tab between the time and the value.

If you set `allbrkpts` to `yes`, you force the simulator to place time points at each point specified in a PWL waveform during a transient analysis. This can be expensive for waveforms with many points. If you set `allbrkpts` to `no`, Spectre inspects the waveform, looking for abrupt changes, and forces time points only at those changes.

The PWL waveform is periodic if you specify `pwlperiod`, `pwlperiodstart` and `pwlperiodstop`. If both `pwlperiod` and `pwlperiodstart` are specified, `pwlperiod` should be greater than `wavelength` - `pwlperiodstart`, where `wavelength` means the last time point. If only `pwlperiod` is specified and `pwlperiodstart` is undefined, the

© 2023 Cadence Design Systems, Inc.

period starts at the first time point or `wavelength` - `pwlperiod`, whichever is greater. If only `pwlperiodstart` is specified and `pwlperiod` is undefined, the period ends at the last time point in the waveform vector. If `pwlperiodstop` is defined, the waveform stops the repeat at the specified time, and the source value changes to `pwlperiodstopvalue` at the time period specified by `pwlperiodstopslope`. If the value of the waveform specified is not the same at both the period beginning and the period end, you must provide a non-zero value for`twidth`. Before repeating, the waveform changes linearly in an interval of `twidth` from its value at `period` - `twidth` to its value at the beginning of the waveform. Therefore, `twidth` must always be less than `period`.

Bit Type Waveform

Bit type waveform is the analog waveform of a series of digital logic state. It uses the pattern parameters to provide the digital state sequence, and some pulse waveform parameters to define the waveform characteristics.

To define the waveform characteristics, use parameters: val1, val0, rise, fall, and period. The parameter `period` here defines the length of a bit and it must be given. The general parameter delay can also be used for bit type to define the delay time from the beginning of the transient interval to the beginning of the first bit. The state during the delay time is the same as the first state specified in data.

Pattern parameters are used to specify the digital bit string. The pattern parameters of sources are the same as those of a pattern, except that you can specify rpttimes to a negative number for sources but not for patterns. Type `spectre -h pattern` for details on how to use pattern parameters.

PRBS Type Waveform

When `type=prbs`, the source emits a pseudo-random bit sequence. The sequence is defined by the LSB of a Fibonacci Linear Feedback Shift Register (LFSR) at trigger events.

The LFSR is initially loaded by a `seed`. The value fed back to the input (MSB) is given by f`eedback=tap_1 ^ tap_2 ^...^ tap_N`, where `^` represents an exclusive-or operation, and `tap_i` represents the i-th bit of the register, counting from 1 and starting from the MSB. At a trigger event, the LFSR is shifted to the right and the MSB is given by the `feedback`.

LFSR Modes:

The sequence can be defined by custom values of seeds and taps. Alternatively, you can specify a maximum length sequence by setting the length of the LFSR. To specify custom

© 2023 Cadence Design Systems, Inc.

seeds and taps, use the `lfsrseed` and `lfsrtaps` arrays. To specify a maximum length sequence, use the parameter, `registerlength=[2 ... 32]`. Spectre sets the seeds and taps automatically. You can optionally set lfsrseed to override the automatically chosen seed.

Triggering Mode:

By default, the sequence is triggered by an internal clock and pulses are emitted every `period` seconds, excluding the optional jitter. Alternatively, you can apply an external clock to the optional 3rd and 4th terminals. In external trigger mode, the pulses are emitted when the clock crosses the specified threshold in the specified direction. The threshold is defined by the triggerthreshold parameter; and, the direction is specified by `triggerdirection`. In external trigger mode, the jitter and bit period parameters are ignored.

Jitter:

Let `{s_i}` be a sequence of ones and zeros whose transitions occur at intervals given by `n*T + j(t)`, where `T` is the bit duration. Then, borrowing Verilog-A terminology, the jittered output is given by `s(t+j(t)) = transition(s_i? Vhigh : Vlow, rise, fall). j(t) = rj(t) + pj(t)`, where `rj` (random jitter) is a normally distributed random variable whose mean is 0 and standard deviation is given by the parameter `rjrms`; and, `pj` is the periodic jitter whose amplitude is `pjamp` and whose frequency is `pjfreq`. The parameter, `pjtype`, defines the type of jitter waveform. For sine, the periodic jitter is given by `pj(t) = pjamp*cos(2*pi*pjfreq*t)`. Other types are `square` and `sawtooth`.

Noise of the source

You can give the excess noise of the source as a file or specify it with a vector of frequency-noise pairs. For a file, give the frequency-noise pairs one pair per line with a space or tab between the frequency and noise values.

When computing the noise figure of a circuit driven at its input by a port, the noise temperature (noisetemp) of the port should be set to 16.85C (290K) in order to match the standard IEEE definition of noise figure. In addition, all other sources of noise in the port (noisefile and noisevec) should be disabled. If a noiseless port is desired, set the noise temperature to absolute zero or below, and do not specify a noise file or noise vector.

Related Topics

Independent Resistive Source (port)

PWL Type Waveform

© 2023 Cadence Design Systems, Inc.

Circuit Components

Linear N Port (nport)

An N-port takes its characteristics from an S, Y, or Z-parameter data file. An N-port can have as many ports as described in the data file. Each pair of terminals in the `nport' instance statement represents one port. Because there is no limit to the number of ports, there is no limit to the number of terminals. However, the terminals must be specified in pairs and you must specify at least one pair. The order of the pairs is the same as the order of the ports in the data file. Any missing ports are ignored.

The S, Y, or Z-parameter data file specifies the characteristics of the N-port. You can scale the frequency axis with the `scale` parameter. The frequencies in the data file are then multiplied by `scale` before the simulator uses them. The default scale factor is unity. In addition to Spectre's native format, the S, Y, or Z-parameters can be in Touchstone or CITIfile format, and the data can be given as: real-imag, mag-deg, mag-rad, db-deg, or db-rad.

An internal thermal noise model is used in noise analysis. However, if you provide frequency-dependent noise data, this data is used to build a noise model. Currently, the Touchstone format accepts the two-port noise parameters (NFmin, Gamma (Gopt, Bopt) and Rn), while Spectre's native format accepts both two-port noise parameters and noise correlation matrix.

If `interp=linear` or `spline` is specified, the impulse response is calculated and the convolution-based method is used for simulation in the time domain. It is assumed that the S, Y, or Z-parameter data is complete and smooth enough to be safely interpolated or extrapolated in the frequency range from fdelta to fmax, and to DC. N-port can be used to model different kinds of systems. The default setting of the impulse response and convolution algorithm is made for typical N-port applications. See the notes below on when and how to set some of the controlling parameters.

Linear interpolation or cubic spline is used for data in polar form. A simple algorithm removes 2 pi jumps in the phase data. Frequency points where the data is measured must therefore be close enough to avoid an excessive number of jumps. Unfortunately, noisy phase data can cause unnecessary warning messages. The number of frequency domain samples used for FFT is `fmax`/`fdelta` with the upper limit of `maxn`. It might be necessary to increase `maxn` for extremely large average group delays. When `usewindow` is set to `yes`, the data in the frequency domain is multiplied by the Kaiser-Bessel window function with smoothing parameter set to one.

If `interp=rational` is specified, the data is interpolated and extrapolated using a rational function fit to the data. The degree of rational interpolation is automatically selected based on the values of `abserr` and `relerr`, unless `ratorder` is given, in which case `relerr` and

© 2023 Cadence Design Systems, Inc.

`abserr` are ignored in selecting the order of the rational function interpolation. It is recommended to allow the simulator to automatically select the rational interpolation order.

When `interp=bbspice` and `nport_bbspice_to_linear=yes` are specified, then if:

- bbspice fails, interpolation method will switch to linear for all analysis.
- bbspice gives large fitting error, interpolation method will switch to linear for dc, ac, xf, sp, noise, stb analyses, and hb analysis on HB Newton stage.

If the S, Y, or Z-parameter data contains noise, `abserr` and `relerr` should be set so that the fitting procedure can ignore the noise, for example, by setting `abserr` above the noise floor and/or relaxing `relerr` as necessary.

Because the fitting procedure can take a long time for complicated data, the reduced order model (ROM) file option is available to store and re-use the rational interpolation function in subsequent simulations.

It is not practical to rely on extrapolated data.

If the `matrixform` parameter is set to `yes`, nport becomes a state-space model. A state-space model is a set of state space equations in matrix form describing a linear system. The equations are in the following form:

$E(dx/dt) = Ax + Bu$

$y = Cx + K(du/dt) + Du$

where u is the input vector, y is the output vector, and x is the internal-state vector. A, B, C, D, E, and K are coefficient matrices.

Refer to the notes on state-space models for detailed information on how to use the parameters.

Sample Instance Statement

```
x1 (a1 0 b1 0 b3 0) ndata file="sparam2.data"
```

Sample Model Statement

```
model ndata nport file="sparam.data" scale=1
```

This device is not supported within altergroup.

© 2023 Cadence Design Systems, Inc.

Synopsis

```
Name  t1  b1  [t2]  [b2] ... ModelName <parameter=value> ...
Name  t1  b1  [t2]  [b2] ... nport <parameter=value> ...
```

Terminals must be given in pairs.

Model Synopsis

```
model ModelName nport <parameter=value> ...
```

Instance Parameters

`m=1`	Multiplicity factor.
`file`	S-parameter data file name.
`com_file`	S-parameter data compress file name.
`datafmt`	The format of the S-parameter data file. If this parameter is not specified, Spectre detects the format by itself. Possible values are `spectre`, `touchstone`, `citi`, `rfm`, and `bnp`.
`scale=1`	Frequency scale factor.
`interp=nport_default_interp`	Method to interpolate S-parameter data, only valid for datafmt=spectre/touchstone/citi/bnp. Where 'interp' is not specified, by default it adheres to the global option nport_default_interp. Possible values are `spline`, `rational`, `linear` and `bbspice`.
`matrixform=no`	Flag for matrix form input. Possible values are `yes` and `no`.
`isnoisy=yes`	Should nport generate noise. Possible values are `yes` and `no`.

© 2023 Cadence Design Systems, Inc.

Spline/Linear interpolation parameters

`fmax (Hz)`	Maximum frequency of interest. Default is three times the highest frequency found in the S-parameter file.
`fdelta (Hz)`	Frequency sampling interva, automatically calculated by the simulator. If you specify the parameter explicitly, adaptive sampling is disabled.
`maxn=131072`	Maximal order of impulse response. Cannot exceed 262144.
`impnoiselevel=1.0e-4`	Noise level threshold for impulse responses used in causality enforcement.
`imptrunc=1.0e-4`	Impulse response truncation threshold relative to the maximum absolute value. The head and tail of the impulse response below imptrunc is removed to speed up the simulation.
`gmin=1.0e-9`	Adding gmin (minimum conductance) to nport terminals for tran and hb analysis.
`datatrunc=1.0e-4`	Relative truncation threshold for the S-parameter data.
`usewindow=no`	Use smooth data windowing function. Possible values are `yes` and `no`.
`dcextrap=constant`	Long delay DC extrapolation method. dcextrap = bbspice is valid only for freq-domain analysis. Possible values are `constant`, `unwrap`, `hpunwrap` and `bbspice`.
`hfextrap=constant`	High-frequency extrapolation method for frequency-domain simulation. hfextrap = bbspice is valid only for freq-domain analysis. Possible values are `constant`, `linear` and `bbspice`.

Passivity checking and enforcement parameters

`passivity=check`	Check and enforce passivity of S parameters. For `interp=bbspice`, default value is `fit_enforce`. For more information, see passivity. Possible values are `no`, `check`, `enforce`, `fit_weak_enforce`, and `fit_enforce`

© 2023 Cadence Design Systems, Inc.

`pabstol=-1.0e-6`	Absolute tolerance of passivity criteria for original s-parameter data.

© 2023 Cadence Design Systems, Inc.

Causality correction parameters

`causality=fmax`	Correct the S-parameter data to ensure that the system is causal. `auto` takes long time to perform causality correction. `fmax_active` can be used for active data. Possible values are `no`, `fmax`, `auto`, `fmax_active`, and `bbspice`.

Rational interpolation parameters

`relerr=0.01`	Maximum relative allowed tolerance for rational interpolation errors. Deviations of the nport model from the supplied S-parameter data of relative magnitude less than `relerr` are mostly ignored.
`abserr=1e-4`	Maximum absolute allowed tolerance for rational interpolation errors. Deviations of the nport model from the supplied S-parameter data of absolute magnitude less than `abserr` are ignored.
`romdatfile`	File used for storing time-domain reduced order model (ROM).
`ratorder`	Order of rational function to use in fitting the S-parameter data. If this argument is given, `relerr` and `abserr` are ignored in selecting the order of the rational function interpolation. If `ratorder` is not specified, the simulator attempts to select an order of rational interpolation that satisfies the criteria implied by `abserr` and `relerr`.

Noise parameters

`trise (C)`	Temperature rise from ambient.
`thermalnoise=yes`	Should nport generate noise. Possible values are `yes` and `no`.
`noisemodel`	Use either the internal thermal noise model or the externally supplied noise data in the S-parameter data file. The default behavior is to use external data whenever it is available. When `interp=bbspice`, externally supplied noise data is ignored and the broadbandspice rational fitting model is used to get the noise model. Possible values are `internal` and `external`.

© 2023 Cadence Design Systems, Inc.

`noisecorr=complex`	Setting `noisecorr` to `real` forces the nport noise correlation matrix to be real-valued. The parameter is used for backward compatibility only. Its value is determined automatically and its use is not recommended because it can lead to an incorrect answer. The simulator generates a warning if the noise correlation matrix is complex while the value of `noisecorr` is set to `real`. Possible values are `real` and `complex`.

© 2023 Cadence Design Systems, Inc.

Matrixform state-space model parameter

`porttypes=[...]`	A vector of integers that defines the types of ports. Use 0 for input port, 1 for output port, and 2 for both input and output ports.
`portquantities=[...]`	A vector of integers that defines the quantities of ports. Use 0 for voltage and 1 for current.
`matrixfile`	Matrix entry data file name.
`matrixA=[...]`	Non-zero entries in coefficient matrix A. Its format is [... row_i col_j value_ij ...].
`matrixB=[...]`	Non-zero entries in coefficient matrix B. Its format is [... row_i col_j value_ij ...].
`matrixC=[...]`	Non-zero entries in coefficient matrix C. Its format is [... row_i col_j value_ij ...].
`matrixD=[...]`	Non-zero entries in coefficient matrix D. Its format is [... row_i col_j value_ij ...].
`matrixE=[...]`	Non-zero entries in coefficient matrix E. Its format is [... row_i col_j value_ij ...].
`matrixK=[...]`	Non-zero entries in coefficient matrix K. Its format is [... row_i col_j value_ij ...].
`acmodel=freqdomain`	Alters nport behavior in small signal analyses: sp, ac, and xf. The default value is `freqdomain`. Possible values are `freqdomain` and `timedomain`.
`outfile`	File used for storing the equivalent S-parameter data based on corresponding time-domain model. The file format is touchstone. The instance name is added as a suffix and the file extension is added automatically.
`bbsfreqband=[...]`	The frequency band of interest. More weight will be added to this frequency band to increase the accuracy of BBspice fitting at this band. The parameter takes a vector with the first element is the start frequency point and the second element is the end freq point..
`maxdelay (C)`	

Related Topics

© 2023 Cadence Design Systems, Inc.

Model Syntax

Important note about spline and linear interpolation parameters

Circuit Components

Model Syntax

```
model modelName nport parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`file`	S-parameter data file name.
`datafmt`	The format of the S-parameter data file. If this parameter is not specified, Spectre detects the format by itself. Possible values are `spectre`, `touchstone`, `citi`, `rfm`, and `bnp`.
`scale=1`	Frequency scale factor.
`dcextrap=constant`	Long delay DC extrapolation method, dcextrap = bbspice is valid only for freq-domain analysis. Possible values are `constant`, `unwrap`, `hpunwrap` and `bbspice`.
`matrixform=no`	Flag for matrix form input. Possible values are `yes` and `no`.

Spline/Linear interpolation parameters

`interp=linear`	Method to interpolate S-parameter data, only valid for datafmt=spectre/touchstone/citi/bnp. Possible values are `spline`, `rational`, `linear` and `bbspice`.
`fmax (Hz)`	Maximum frequency of interest. Default is three times the highest frequency provided in the S-parameter file.
`fdelta (Hz)`	Frequency sampling interval automatically calculated by the simulator. If you specify the parameter explicitly, adaptive sampling is disabled.
`maxn=131072`	Maximal order of impulse response. Cannot exceed 262144.
`impnoiselevel=1.0e-4`	Noise level threshold for the impulse responses used in causality enforcement.
`imptrunc=1.0e-4`	Relative truncation threshold for the impulse response.
`gmin=1.0e-9`	Adding gmin (minimum conductance) to nport terminals for tran and hb analysis.
`datatrunc=1.0e-4`	Relative truncation threshold for the S-parameter data.

© 2023 Cadence Design Systems, Inc.

`usewindow=no`	Use smooth data windowing function. Possible values are `yes` and `no`.
`hfextrap=constant`	Long delay high-frequency extrapolation method. hfextrap = bbspice is valid only for freq-domain analysis. Possible values are `constant`, `linear` and `bbspice`.

© 2023 Cadence Design Systems, Inc.

Passivity checking and enforcement parameters

`passivity=check`	Check and enforce passivity of s parameters. For `interp=bbspice`, default value is `fit_enforce`. For more information, see `passivity`. Possible values are `no`, `check`, `enforce`, `fit_weak_enforce`, and `fit_enforce`.
`pabstol=-1.0e-6`	Absolute tolerance of passivity criteria.

Causality correction parameters

`causality=fmax`	Correct the S-parameter data to ensure that the system is causal. The default value is `fmax`. `auto` takes a long time to perform causality correction. Possible values are `no`, `fmax`, and `auto`.

Noise parameters

`trise=0 C`	Default temperature rise from ambient.
`thermalnoise=yes`	Should nport generate noise. Possible values are `yes` and `no`.
`isnoisy=yes`	Should nport generate noise. Possible values are `yes` and `no`.
`noisemodel`	Use either the internal thermal noise model or the externally supplied noise data in the S-parameter data file. The default behavior is to use external data whenever it is available. When `interp=bbspice`, externally supplied noise data is ignored and broadbandspice rational fitting model is used to get the noise model. Possible values are `internal` and `external`.
`noisecorr=complex`	Setting `noisecorr` to `real` forces the nport noise correlation matrix to be real-valued. The parameter is used for backward compatibility only. Its value is determined automatically and its use is not recommended because it can lead to an incorrect answer. The simulator generates a warning if the noise correlation matrix is complex while the value of `noisecorr` is set to `real`. Possible values are `real` and `complex`.

© 2023 Cadence Design Systems, Inc.

Matrixform state-space model parameter

`porttypes=[...]`	A vector of integers that defines the types of ports. Use 0 for input port, 1 for output port, and 2 for both input and output ports.
`portquantities=[...]`	A vector of integers that defines the quantities of ports. Use 0 for voltage and 1 for current.
`matrixfile`	Matrix entry data file name.
`matrixA=[...]`	Non-zero entries in coefficient matrix A. Its format is [... row_i col_j value_ij ...].
`matrixB=[...]`	Non-zero entries in coefficient matrix B. Its format is [... row_i col_j value_ij ...].
`matrixC=[...]`	Non-zero entries in coefficient matrix C. Its format is [... row_i col_j value_ij ...].
`matrixD=[...]`	Non-zero entries in coefficient matrix D. Its format is [... row_i col_j value_ij ...].
`matrixE=[...]`	Non-zero entries in coefficient matrix E. Its format is [... row_i col_j value_ij ...].
`matrixK=[...]`	Non-zero entries in coefficient matrix K. Its format is [... row_i col_j value_ij ...].

Related Topics

Linear N Port (nport)

Important note about spline and linear interpolation parameters

Circuit Components

Important note about spline and linear interpolation parameters

`interp`

To calculate impulse response, either linear or spline interpolation is used to sample data points in the frequency domain, based on the S-parameter data file. When the input data points are sufficient, linear and spline interpolation produce comparable model accuracy. However, when the input data points are scarce, linear interpolation is preferred to bound jumps between data points. Interpolation/extrapolation can be avoided all together if the S-

© 2023 Cadence Design Systems, Inc.

parameter data is provided from zero frequency to fmax with uniform step fdelta, and number of samples is a power of 2.

`fmax`

The default value of fmax is three times the highest frequency in the S-parameter data file. Impulse response is calculated by sampling frequency points between DC and `fmax'. The purpose of this extrapolation is to preserve high-frequency model accuracy. However, if you have enough bandwidth in the S-parameter data file, `fmax' needs to be set to the original highest frequency in the S-parameter data file. In general, fmax must be larger than the expected signal bandwidth.

`fdelta`

Frequency sampling interval automatically calculated by the simulator. If `causality=no`, it is the default of `fmax`/4096. If `causality=fmax/auto`, it is adaptively optimized. This interval is also limited by `fmax`/`maxn`. If you specify the parameter explicitly, adaptive sampling is disabled.

Note: `fdelta` can be further reduced so that `fmax`/`fdelta` is a power of 2. This is required by the FFT algorithm.

`maxn`

Maximal order of impulse response, or the maximum number of sampling points in the frequency domain. You should increase this value only when modeling a system with large average group delay, such as transmission line. Setting this parameter to an unnecessarily large value slows down the time-domain simulation. The absolute upper limit for `maxn` is 262144.

`impnoiselevel`

Noise level threshold for impulse responses used in causality enforcement.

`imptrunc`

Relative truncation threshold for impulse response. The head and tail of the impulse response with absolute values below `imptrunc` is removed to speed up the simulation.

`datatrunc`

S-parameter data truncation threshold relative to the maximum element in the same row. The S-parameter data below datatrunc is dropped. This improves the capability and performance for simulating large-scale nport systems. Set `datatrunc=0` to keep all S-parameter data.

`usewindow`

© 2023 Cadence Design Systems, Inc.

Kaiser-Bessel window with smoothing parameter 1 is used to regulate the stability of S-parameter data. This parameter trades off model accuracy with model stability and is particularly useful for S-parameter data with insufficient bandwidth. Window must be used for all-pass type systems, where S-parameters are non-zero for frequencies beyond `fmax`.

`dcextrap`

For long delay, the DC extrapolation method can be set to `constant`, `unwrap`, or `hpunwrap`. The default is `constant`, where, without a dc point, the low-frequency magnitude is held at the lowest data point and the dc phase is set to the real axis near the lowest-frequency data point and interpolated elsewhere. If the parameter is set to `unwrap` and there is no dc point, the DC magnitude is set based on a regression of some low-frequency data, and the DC phase is set by unwrapping the phase and then setting it onto the real axis. If the dc point is specified, the magnitude is interpolated while the phase is still determined using the unwrapped estimate. `hpunwrap` is similar to `unwrap` for DC phase extrapolation but provides an alternative approach for DC magnitude extrapolation, which may be preferred for high-pass characteristics.

`hfextrap`

For an all-pass system or nearly all-pass system, the high frequency extrapolation method can be set to `constant` or `linear`. The default is `constant`, which causes the out-of-band frequency magnitude and phase to be held at the highest data point. For the 'linear' case, the out-of-band frequency magnitude is still held at the highest data point, but the phase is linearly extrapolated based on the phase of the in-band high frequency data.

`passivity`

Due to poor measurement accuracy, the S-parameter data may be non-passive. Non-passive S-parameter data may lead to non-converging or even unstable time domain simulations. . The `passivity` option controls the detection and enforcement of S-parameter simulation model passivity. The `passivity` option can be set to `no`, `check`, or `enforce` for `interp=spline|linear`. The default is `check`, which causes the simulator to check the S-parameter data at each frequency point and report non-passive data. If the parameter is set to `enforce`, the simulator corrects the data to ensure passivity, if the original data is non-passive. This can cause accuracy loss.

For `interp=bbspice`, `passivity` may be set to `fit_weak_enforce` or `fit_enforce`, The default value is `fit_enforce`. With `passivity=fit_enforce`, the simulator always attempts to create a passive simulation model and favors passivity over accuracy. With `passivity=fit_weak_enforce`, the simulator does not create a passive model if the passivity enforcement phase results in a significant accuracy loss.

For i`nterp=bbspice`, the simulator always checks if the S-parameter data is passive. Passivity options `fit_weak_enforce` and `fit_enforce` are only available for

© 2023 Cadence Design Systems, Inc.

`interp=bbspice` and are interpreted as `passivity=check` for `interp=linear|spline`. Passivity options `no`, `check`, and `enforce` are only available for `interp=linear|spline` and are interpreted as `passivity=fit_enforce` for `interp=bbspice`.

`pabstol`

When checking or enforcing passivity, the default tolerance of the passivity criteria is -1.0e-6. If the parameter is set to a higher value, the passivity checking criteria loosens.

`causality`

For convolution-based time-domain simulation, causality is an important factor that affects the simulation accuracy. If `causality=fmax`, the simulator corrects the S-parameter causality up to `fmax`, as specified by the existing parameter. If `causality=auto`, the simulator corrects the S-parameter causality up to the automatically optimized fmax and ignores the existing parameter `fmax`. The parameters `usewindow` and `hfextrap` are ignored when `causality=fmax` or `causality=auto`.

It is recommended to use `causality=fmax` to obtain good simulation accuracy. For certain cases, if `causality=fmax` does not provide the expected accuracy, you can try `causality=auto`. However, it is slow to perform causality correction for large systems if `causality=auto`.

Important note about parameters for validation tool

An S-parameter time-domain validation tool is used to compare the original S-parameter data with the equivalent S-parameter data based on the corresponding time-domain model. The simulator uses the equivalent S-parameter data instead of the original S-parameter data in small signal analyses: sp, ac, and xf.

`acmodel`

This parameter alters the nport behavior in small signal analyses: sp, ac, and xf. The default value is `freqdomain`. When `acmodel=freqdomain`, the frequency domain data is used directly in small signal analysis after interpolation/extrapolation to a set of frequency sweep points. When `acmodel=timedomain`, frequency domain data is converted to a time-domain model in the same way it is done in the transient initialization step. Then, the time-domain model is converted back to the frequency domain, which is used in small signal analysis.

`outfile`

This parameter is used to specify the name of the file used for storing the equivalent S-parameter data based on the corresponding time-domain model. The file format is

© 2023 Cadence Design Systems, Inc.

touchstone. The instance name is added as a suffix and the file extension is added automatically. If the corresponding impulse responses are not generated, this parameter is ignored.

You can run ac analysis with `acmodel=timedomain` and compare the results with `acmodel=freqdomain` to see if the time-domain model is accurate. In addition, you can plot the equivalent S-parameters (outfile) and compare the results with the original S-parameter data using VIVA.

If `interp=bbspice`, this file is the same as the fitted sp file in the cache directory.

Important note about impulse responses (IR) reuse feature

Spectre checks there is a corresponding IR file. If yes, it loads the data from the IR file. If an IR file is not found, Spectre computes it and saves the IR file to the directory specified by the global option `nportirfiledir`. If the directory name is not specified, the file is written to `/home/<username>/.cadence/mmsim/`. To store the file in a location other than the default, you must specify either an absolute or a relative path. If a relative path is specified, the path is relative to the current working directory.

The global option `nportirreuse={yes|no}` can be used to enable or disable the IR reuse feature for all nport instances.

`nportirreuse` and `nportirfiledir` also work for `interp=bbspice`. The stored file named with '_encrypt' is the encrypted rational fitting model (RFM) from bbspice. The stored file named with '_save' is the fitting error report, it is created only when large fitting errors show up.

With `interp=bbspice`, there are some output files from bbspice run, they are located in `BBSpiceOutput` directory. This directory is under the current working directory unless the `-outdir` command line option is specified.

Important note about parameters for state-space models

`porttype` and `portquantities`

Both parameters have the same number of entries as the number of ports, and each entry corresponds to a port. The entries are in the same order as the port order in the terminal specification of the instance. The `porttype` parameter specifies the type of each port of nport. A port can be of type input, output, or both. The `portquantities` parameter specifies whether each input/output is a voltage or current. Each entry in `portquantities` corresponds to one entry in `porttypes`. It specifies the quantity of input for input and both

© 2023 Cadence Design Systems, Inc.

ports and the quantity of output for the output port. For both input and output ports, if the input quantity is set to voltage, the output quantity will be current and vice-versa.

`matrixfile`

Matrix entry data file name.

File format:

Any line beginning with ";", "#", or "%" is treated as a comment and discarded.

Remaining lines should have a first character as A, B, C, D, E, or K, two integers, and a floating-point number. Such a line denotes an entry in the appropriate matrix with given row column indexes and matrix element.

For example, a file may look like this:

```
;matrix A, 3x3
A 1 1 1234.5678
...
;
;matrix E, 3x3
E 1 1 1.0
...
;
;matrix B, 3x1
B 2 1 4.28
...
;
;matrix C, 2x3
C 2 1 3.14
...
```

If a matrix is not specified in the file, it is treated as a zero matrix for A, B, C, D, and K. Matrix E is treated as an identity matrix, if it is not specified in the file.

matrixA matrixB matrixC matrixD matrixE matrixK

Coefficient matrices of the state-space model. The syntax of the vector is in sparse form, that is:

```
[ Row_1, Column_1, Value_11,
  ...
  Row_i, Column_j, Value_ij,
  ... ]
```


© 2023 Cadence Design Systems, Inc.

If a matrix is not specified, it is treated as a zero matrix for A, B, C, D, and K. Matrix E is treated as an identity matrix, if it is not specified.

Related Topics

Model Syntax

Linear N Port (nport)

Circuit Components

Current Probe (iprobe)

Current through the probe is computed and is defined to be positive if it flows from the input node, through the probe, to the output node. The current variable is given the name of the `iprobe` instance, so you cannot create an `iprobe` with the same name as a circuit node.

This device is supported within altergroups.

Sample Instance Statement

ip (1 0) iprobe

Instance Syntax

```
Name  in  out iprobe
```

Operating-Point Parameters

`i (A)`	Current through iprobe.

Related Topics

Circuit Reduced Order Model (cktrom)

Circuit Components

© 2023 Cadence Design Systems, Inc.

Circuit Reduced Order Model (cktrom)

The circuit reduced order model is described by a set of partial differential equations in the form of:

$$\dot{x} = Ax + Bu \qquad (1)$$

$$y = Cx + Du \qquad (2)$$

where Eqn.(1) is the state equation, Eqn.(2) is the output equation, A is nxn matrix, B is nxm, C is mxn, and D is an mxm matrix. x is a vector of state variables. Input u is a vector of voltages at all the ports and output y is a vector of electric current at all the ports. The number of inputs is always equal to the number of outputs. The order of the terminals in the input must be consistent with the matrix equations. In the input file, the matrices A, B, C and D are in the form of long vectors with row order.

This device is not supported within altergroup.

Sample Instance Statement

```
rom3 (net11 0) cktrom a=[ -2.022852e+14  2.583012e+13  9.553125e+13  9.627727e+13
1.533971e+13 9.987851e+13 4.592012e+13 -1.671024e+14  2.296589e+13 -2.719915e+14
7.668472e+12 -1.564519e+14  8.543123e+13  3.395689e+13 -3.863150e+14 -
1.101618e+14 -5.415116e+14 -2.303841e+14  9.627728e+13 -1.711915e+14 -
1.001818e+14 -8.123120e+14 -2.272715e+14 -9.965181e+14 1.514961e+14
7.668372e+12 -6.415116e+14 -3.272715e+14 -2.852751e+15 -3.564466e+14
9.999851e+13 -1.761619e+14 -1.312841e+14 -8.967181e+14 -4.563456e+14 -
4.068747e+15 ]

b=[3.366776e+06  5.932470e+05 -1.508475e+06  4.349182e+06 -3.128869e+06 -
2.995677e+06 -2.831481e+06  2.708942e+06 -4.968876e+06 -3.338945e+06 -
3.278564e+06  3.925648e+06 ]

c=[-3.111296e+06  1.593292e+06  3.324594e+06  3.083731e+06  5.887179e+06
3.766094e+06 -5.049263e+05 -4.275158e+06  3.035578e+06 -3.666385e+06
3.424639e+06 -3.832285e+06]

d=[1.254627e-01  0.000000e+00 0.000000e+00  1.236790e-01 ]
```


© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name sink0 src0 [sink1] [src1] [sink2] [src2] [sink3] [src3] ... cktrom
parameter=value ...
```

Instance Parameters

m	1	Multiplicity factor.
a	[...]	Coefficient matrix A of state equations.
b	[...]	Coefficient Matrix B of state equations.
c	[...]	Coefficient matrix C of output equations.
d	[...]	Coefficient matrix D of output equations.

Operating-Point Parameters

i	[...] A	Port currents.
v	[...] V	Port voltages.
pwr	(W)	Power dissipation.

Related Topics

Current Probe (iprobe)

Circuit Components

Analog-to-Logic Converter (a2d)

The analog-to-logic converter transfers analog waveforms to a logic simulator.

This device is not supported within altergroup.

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

da99 (cmp_out 0) a2d dest=”99991” vl=0 vh=5 timex=200u

// 99991 is a digital net in the Verilog netlist.

Instance Syntax

```
Name  p  n a2d parameter=value ...
```

Instance Parameters

`dest`	The foreign simulator name for the destination of the signal.
`nestlev=0`	Number of nesting levels to be ignored in the hierarchical name. This should be used to skip over extra levels that do not exist in the co-simulator.
`vl=0 V`	Voltages below this will be logical 0.
`vh=5 V`	Voltages above this will be logical 1.
`timex=1 s`	Time signal can linger between `vl` and `vh` before the state becomes X.

Related Topics

device checker (assert)

Logic-to-Analog Converter (d2a)

Circuit Components

device checker (assert)

The assert statement cannot be altered using the alter statement.

This device is supported within altergroups.

Instance Syntax

```
Name assert parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

Scope parameters

`sub`	Subcircuit master or subcircuit master pattern to be checked. Pattern can have any wildcard symbols and should be in quotation marks.
`subs=[...]`	Array of subcircuit masters or subcircuit master patterns to be checked. Patterns can have any wildcard symbols.
`mod`	Model to be checked.
`dev`	Device, subcircuit instance, or instance pattern to be checked. Pattern can have any wildcard symbols and should be in quotation marks.
`primitive`	Primitive to be checked.

Checked parameters

`expr`	Expression to be checked for violation (in MDL syntax).
`modelparam`	Model parameter to be checked.
`param`	Any one of input, output, operating point, subcircuit instance parameter, or V() and I() probe functions to be checked.

Behavior parameters

`max=infinity`	Upper bound of the parameter to be checked.
`min=infinity`	Lower bound of the parameter to be checked.
`duration=0 s`	Time period over which the check has been in violation before a message is flagged.
`message`	Message to be printed when assertion fails.
`level=warning`	Severity used when assertion fails. Possible values are `none`, `notice`, `warning`, `error`, and `fatal`.
`info=no`	When `info=yes`, parameter will not be checked against min/max; only its value will be printed. Possible values are `yes` and `no`.

© 2023 Cadence Design Systems, Inc.

`values=[...]`	List of values for the enumerated type parameters. If `boolean=true` and the parameter value is specified other than the listed ones or if `boolean=false` and the parameter value is specified as one of the listed ones, violations are issued.
`boolean=true`	Choose behavior and report style for boolean violations. If `boolean=true`, asserts are reported in old style. If `boolean=false`, asserts are reported in new style. Possible values are `false` and `true`.
`anal_types=[...]`	List of analysis types for which the assert instance will be checked. By default, the check is performed for all analyses. Possible values are `ac`, `dc`, `noise`, `pz`, `sp`, `tran`, and `pss`.
`check_windows=[...]`	Time windows for which the check is enabled or disabled. The array should contain an even number of values [`b_begin1 b_end1 b_begin2 b_end2 ...`]. If the parameter is defined in both assert and checklimit statements, the parameter defined in the assert statement takes higher priority.
`maxvio_perinst`	Maximum number of violations per checked instance.
`maxvio_all`	Maximum number of all violations.
`group="default"`	Specify the group which this assert belongs to.
`safecheck=none`	Assert type for fault detection. When the parameter is set to 'func', it checks the functional module. When set to 'check', the parameter checks the diagnostic module. In addition, a functional safety report is generated for both 'func' and 'check' asserts. Set the value of the safecheck parameter to 'none' to perform regular assert checking. Possible values are `none`, `func`, and `check`
`extreme=no`	When `extreme=yes`, extreme information of boolean check assert is reported. Possible values are `yes` and `no`.
`skip_dev_inside_subckt=[...]`	

© 2023 Cadence Design Systems, Inc.

	Skip subcircuit or device instances inside a given subcircuit. `skip_dev_inside_subckt=[pll.M1 pll.inv1]` will not perform the assert on the device model instance `M1` and the subckt instance `inv1` inside the subckt definition of `pll`.
`max_peak=infinity`	Maximum threshold to decide whether to report a violation.
`min_peak=infinity`	Minimum threshold to decide whether to report a violation.

Related Topics

Analog-to-Logic Converter (a2d)

Logic-to-Analog Converter (d2a)

Circuit Components

Logic-to-Analog Converter (d2a)

The logic-to-analog converter converts a binary signal from a logic simulator to an analog waveform.

This device is not supported within altergroup.

Sample Instance Statement

```
d2a_1 (net1 net2) d2a src=”99991” val0=0 val1=2.5 valx=1.25 rise=200p fall=200p m=2
//99991 is an analog net
```

Instance Syntax

```
Name  p  n d2a parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

src		The foreign simulator's name for the source of the analog signal.
nestlev	0	Number of nesting levels to be ignored in the hierarchical name. This should be used skip over extra levels that do not exist in the co-simulator.
val0	0 V	Final value for logical 0.
val1	5 V	Final value for logical 1.
valx	(V)	Final value for logical X.
valz	(V)	Final value for logical Z.
rise	1ns s	Time for transition from val0 to val1.
fall	1ns s	Time for transition from val1 to val0.
ron	100 Ω	Output resistance when in active state.
m	1	Multiplicity factor.

Related Topics

device checker (assert)

Logic-to-Analog Converter (d2a)

Circuit Components

Ideal Switch (switch)

Ideal switch is a single-pole multiple-throw switch with infinite off resistance and zero on resistance. The switch is provided to allow you to reconfigure your circuit between analyses. You can only change the switch state between analyses (using the alter statement), not during an analysis.

© 2023 Cadence Design Systems, Inc.

When the switch is set to position 0 it is open. In other words, no terminal is connected to any other. When the switch is set to position 1, terminal 1 is connected to terminal 0, and all others are unconnected. When the position is set to 2, terminal 2 is connected to terminal 0, etc.

An offset voltage is supported. It is placed in series with the common terminal. The negative side of the source is connected to the common terminal.

The switch can change its position based on which analysis type is being performed using the `xxx_position` parameters. This feature should be used carefully. Careless use can generate discontinuities that result in convergence problems. Once an analysis specific position has been specified using `xxx_position`, it will always dominate over a position given with the `position` parameter. To disable an analysis specific position, alter it to its default value of unspecified.

This device is not supported within altergroup.

Sample Instance Statement

```
sw1 (t1 t2 t3) switch dc_position=0 ac_position=1 tran_position=2
```

Instance Syntax

```
Name  t0  t1 ... switch parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`position=0`	Switch position (0, 1, 2, ...).
`dc_position`	Position to which switch is set at start of DC analysis.
`ac_position`	Position to which switch is set at start of AC analysis.
`tran_position`	Position to which switch is set at start of transient analysis.
`ic_position`	Position to which switch is set at start of IC analysis (precedes transient analysis).
`offset=0`	Offset voltage in series with common terminal.
`m=1.0`	Multiplicity factor.

Output Parameters

`present_position`	Current switch position.

Related Topics

Ratiometric Fourier Analyzer (fourier)

IBIS I/O buffer (ibis_buffer)

Circuit Components

Ratiometric Fourier Analyzer (fourier)

The ratiometric Fourier analyzer measures the Fourier coefficients of two different signals at a specified fundamental frequency without loading the circuit. The algorithm used is based on the Fourier integral rather than the discrete Fourier transform and therefore is not subject to aliasing. Even on broad-band signals, it computes a small number of Fourier coefficients accurately and efficiently. Therefore, this Fourier analyzer is suitable on clocked sinusoids generated by sigma-delta converters, pulse-width modulators, digital-to-analog converters, sample-and-holds, and switched-capacitor filters as well as on the traditional low-distortion sinusoids produced by amplifiers or filters.

The analyzer is active only during transient analysis. For each signal, the analyzer prints the magnitude and phase of the harmonics along with the total harmonic distortion at the end of the transient analysis. The total harmonic distortion is found by adding the power in all of the

© 2023 Cadence Design Systems, Inc.

computed harmonics except DC and fundamental. Consequently, the distortion is not accurate if you request an insufficient number of harmonics The Fourier analyzer also prints the ratio of the spectrum of the first signal to the fundamental of the second, therefore, you can use the analyzer to compute large signal gains and immittances directly.

If you are concerned about accuracy, perform an additional Fourier transform on a pure sinusoid generated by an independent source. Because both transforms use the same time points, the relative errors measured with the known pure sinusoid are representative of the errors in the other transforms. In practice, this second Fourier transform is performed on the reference signal. To increase the accuracy of the Fourier transform, use the `points` parameter to increase the number of points. Tightening `reltol` and setting `errpreset=conservative` are two other measures to consider.

The accuracy of the magnitude and phase for each harmonic is independent of the number of harmonics computed. Therefore, increasing the number of harmonics (while keeping `points` constant) does not change the magnitude and phase of the low-order harmonics, but it does improve the accuracy of the total harmonic distortion computation. However, if you do not specify `points`, you can increase accuracy by requesting more harmonics, which creates more points.

The large number of points required for accurate results is not a result of aliasing. Many points are needed because a quadratic polynomial interpolates the waveform between the time-points. If you use too few time-points the polynomials deviate slightly from the true waveform between the time-points and all of the computed Fourier coefficients are slightly in error. The algorithm that computes the Fourier integral does accept unevenly spaced time-points, but because it uses quadratic interpolation, it is usually more accurate using time-steps that are small and nearly evenly spaced.

This device is not supported within altergroup.

Sample Instance Statement

```
four1 (1 0) fourmod harms=50
```

Sample Model Statement

```
model fourmod fourier fund=900M points=2500 order=2
```

Instance Syntax

```
Name  [p]  [n]  [pr]  [nr] ModelName parameter=value ...
Name  [p]  [n]  [pr]  [nr] fourier parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

The signal between terminals `p` and `n` is the test or numerator signal. The signal between terminals `pr` and `nr` is the reference or denominator signal. Fourier analysis is performed on terminal currents by specifying the `term` or `refterm` parameters. If both `term` and `p` or `n` are specified, the terminal current becomes the numerator and the node voltages become the denominator. By mixing voltages and currents, it is possible to compute large signal immittances.

Instance Parameters

`fund (Hz)`	Fundamental frequency.
`points=20 maxharm`	Minimum number of time points.
`active=yes`	Whether Fourier analysis should be performed or skipped. Possible values are `no` or `yes`.
`order=2`	Order of interpolation.
`term`	Terminal used to measure current for the test (numerator) channel.
`refterm`	Terminal used to measure current for the reference (denominator) channel.
`harmsvec=[...]`	Array of desired harmonics for the test (numerator) channel.
`harms=9`	Number of harmonics for test (numerator) channel, if an array is not given. The harmonics start from `firstharm` and go up to `firstharm` + `harms` - 1.
`refharmsvec=[...]`	Array of desired harmonics for the reference (denominator) channel.
`refharms=9`	Number of harmonics for the reference (denominator) channel, if an array is not given. The harmonics start from `reffirstharm` and go up to `reffirstharm` + `harms` - 1.
`scale=1`	Scale factor for the ratio results.
`firstharm=1`	First harmonic computed for the test (numerator) channel.
`reffirstharm=1`	First harmonic computed for the reference (denominator) channel.
`normharm=1`	Normalizing harmonic for test the (numerator) channel.

© 2023 Cadence Design Systems, Inc.

`refnormharm=1`	Normalizing harmonic for the reference (denominator) channel.
`where=logfile`	Location where the fourier results should be printed. Possible values are `screen`, `logfile`, and `both`.

Model Syntax

```
model modelName fourier parameter=value ...
```

Model Parameters

`fund (Hz)`	Fundamental frequency.
`points=20 maxharm`	Minimum number of time points.
`harms=9`	Desired number of harmonics.
`active=yes`	Specify whether fourier analysis should be performed or skipped. Possible values are `no` or `yes`.
`order=2`	Order of interpolation.
`firstharm=1`	First harmonic computed for the test (numerator) channel.
`reffirstharm=1`	First harmonic computed for the reference (denominator) channel.

Related Topics

Ideal Switch (switch)

IBIS I/O buffer (ibis_buffer)

Circuit Components

IBIS I/O buffer (ibis_buffer)

IBIS buffer model is based on IBIS (I/O Buffer Information Specification) standard, version 7.0. Package and board models, are not included in the buffer, and have to be added as separate subcircuits.

This device is not supported within altergroup.

© 2023 Cadence Design Systems, Inc.

Driver Equations

Current at the `die` terminal is a function of time and voltage:

```
I(die) = Ipd(V(die)-V(gnd))*Wd(t) + Icd(V(die)-V(gnd_c))
         + Ipu(V(die)-V(pwr))*Wu(t) + Icu(V(die)-V(pwr_c))
```

`Ipd(V)`, `Ipu(V)`, `Icd(V)`, and `Icu(V)` are peace-wise linear transfer functions of pull-down, pull-up, ground clamp, and power clamp voltage controlled current sources. `Wd(t)` and `Wu(t)` are switching coefficient functions for pull-up and pull-down sources, defined as follows.

When the buffer is in the high state,

```
Wd(t)=0, Wu(t)=1
```

When the state of the buffer is low,

```
Wd(t)=1, Wu(t)=0
```

During a transition from low to high state

```
Wd(t)=Wdr(t-t0), Wu(t)=Wur(t-t0)
```

During a hi-lo transition,

```
Wd(t)=Wdf(t-t0), Wu(t)=Wuf(t-t0)
```

where `t0` - is a time when transition was initiated.

For the 3-state or I/O buffer types, driver can be disabled by `en` signal, then both `Wu(t)`=`Wd(t)`=0.

`Wdr(t)`, `Wur(t)`, `Wdf(t)`, and `Wuf(t)` are pwl functions of time, derived from the rising and falling test waveforms and loads.

State of the buffer is defined by the voltage on the `out` terminal, and buffer polarity. During DC analysis buffer can be either in high, or low state. For non-inverting buffer, the state is high when `V(out)>0.5`, and low when `V(out)>=0.5`. For inverting buffer it is other way around. During transient analysis the buffer is turned into transition state at the time t0, when `V(out)` crosses the midpoint `V(out)=0.5`. When both `Wd(t)` and `Wu(t)` switching coefficient functions reach their final 1 or 0 values, the buffer returns to the static high or low state.

Receiver Equations

Voltage at the `in` terminal is a controlled by voltage at the `die` node.

© 2023 Cadence Design Systems, Inc.

If `V(die) > Vth_hi`, then `V(in) = 1`, if `V(die) < Vth_lo`, then `V(in) = 0`.

In between `Vth_hi >= V(die) >= Vth_lo`, `V(in)` keeps previously assigned voltage.

For differential input buffers the voltage difference between non-inverting and inverting pins: `V(die)-V(inv_die)` is used instead of `V(die)`

Switching Coefficients

Switching coefficients, if not given, are calculated from the test waveforms and loads. If two waveforms are available for rising transition (`V1r, V2r`) and two for falling (`V1f, V2f`), then linear system of equations is solved for pairs of switching coefficients (`Wdr, Wur`) and (`Wdf, Wuf`) at each time t:

```
Ipd(Vr1-Vgnd)*Wdr + Ipu(Vr1-Vpwr)*Wur = I0(Vr1)
Ipd(Vr2-Vgnd)*Wdr + Ipu(Vr2-Vpwr)*Wur = I0(Vr2)
Ipd(Vf1-Vgnd)*Wdf + Ipu(Vf1-Vpwr)*Wuf = I0(Vf1)
Ipd(Vf2-Vgnd)*Wdf + Ipu(Vf2-Vpwr)*Wuf = I0(Vf2)
```

Where `Ipd(V)`, `Ipu(V)` are pull-down and pull-up current source fonctions. Load current `I0(V)` for each load resistance `Rl`, voltage `Vl`, and capacitance `Cl` is calculated as:

```
I0(V) = (Ccomp+Cl)*dV/dt - (V-Vl)/Rl - Igc(V-Vgndc) - Ipc(V-Vpwrc)
```

If only one waveform is available for each transition, additional equations are used:

```
Wdr + Wur = 1
Wdf + Wuf = 1
```

If no waveforms are given, then `ramp` parameters are used to determine the coefficients. In this case they will be linear functions of time with the slope equal to `ramp` value.

Sample Instance Statement

```
pin1 (die in out en gnd vdd gnd_c vdd_c) iobuff1
pin2 (die out en) ibis_buffer file="models.ibs" model="out2"
```

Sample Model Statement

```
model iobuff1 ibis_buffer type=io vrange=3 ccomp=1p polarity=noninv enable=high
    pullup=[-3 30m -2 25m -1 15m 0 0 1 -15m 2 -24m 3 -30m 4 -35m 5 -36m 6 -37m]
     pulldown=[6 40m 5 38m 4 35m 3 30m 2 25m 1 15m 0 0 -1 -15m -2 -24m -3 -30m]
     uprise=[0 0 3n 1]
```


© 2023 Cadence Design Systems, Inc.

```
downrise=[0 1 3n 0]
upfall=[0 1 3n 0]
downfall=[0 0 3n 1]
gndclamp=[-4 -40 -0.4 0 0 0]
```

Instance Syntax

```
Name die [inp] [out] [en] [gnd] [pwr] [gnd_c] [pwr_c] [inv_die] ModelName
parameter=value ...
Name die [inp] [out] [en] [gnd] [pwr] [gnd_c] [pwr_c] [inv_die] ibis_buffer
parameter=value ...
```

Terminal comments

Number of terminals depend on the type of the buffer.

Only one terminal - `die` - is required for terminator.

Terminals `out` and `die` are required for output buffer. They connect to digital signals, which control pullup and pulldown current sources driving the `die`.

Input buffer must have `in` terminal, which is digital signal received from the `die`.

Terminals `gnd`, `pwr`, `gnd_c`, `pwr_c` provide optional ground and power connections for pull-down, pull-up, ground clamp, and power clamp current sources. Opendrain buffers do not require power connections. Opensource have no groun connections. Either none, or all possible reference voltage terminals have to be specified.

For differential input buffers `inv_die` terminal provides input voltage reference. It have to be connected to the die pad of the inverse pin.

Buffer type	Terminals (y= required, n=not, o=optional)								
	die	in	out	en	gnd	pwr	gnd_c	pwr_c	inv_die
terminator	y	n	n	n	n	n	o	o	n
input	y	y	n	n	n	n	o	o	o
output	y	n	y	n	o	o	o	o	n
tristate	y	n	y	y	o	o	o	o	n
io	y	y	y	y	o	o	o	o	o
opendrain	y	n	y	n	o	n	o	n	n
ioopendrain	y	y	y	y	o	n	o	n	o

© 2023 Cadence Design Systems, Inc.

`opensource`	y	y	y	y	n	o	n	o	n
`ioopensource`	y	y	y	y	n	o	n	o	o

Buffer type `opensink` is same as `opendrain`, and `ioopensink` is same as `ioopendrain`. Buffer types ending with ecl (inputecl, outputecl, ioecl, tristateecl) have same terminals as their normal counterparts (input, output, io, tristate).

© 2023 Cadence Design Systems, Inc.

Instance Parameters

`file`	Name of ibis file containing buffer model information.
`model`	Name of the model section in ibis file.
`corner=0`	IBIS model corner. Allowed values are: 0 or `typical`, 1 or `minimal`, 2 or `maximal`, 3 or `slow`, 4 or `fast`. Possible values are `typical`, `minimal`, `maximal`, `slow`, and `fast`.
`power=on`	SPECTRE format netlist: ■ `on` means Spectre will use the internal reference. ■ `off` means Spectre will use the external reference. ■ `pwr` means Spectre will use the internal reference for pullup and power clamp, while the pulldown and gnd clamp must be connected to the external reference. ■ `gnd` means Spectre will use the internal reference for pulldown and gnd clamp, while the pullup and power clamp must be connected to the external reference. Possible values are `on`, `off`, `pwr`, and `gnd`.

Differential buffer parameters

`polarity=inv`	Polarity of the buffer. Possible values are `inv` and `noninv`.
`delay (s)`	Relative delay for differential output buffer.
`vdiff (V)`	Threshold voltage for differential input buffer.

SPICE compatibility parameters. Ignored in Spectre mode

`compatible=spectre`	Selects buffer format - terminal order, parameters.

© 2023 Cadence Design Systems, Inc.

`buffer`	IBIS model type. If given, must correspond to the buffer model type in the IBIS file. Allowed values are: 1 or `input`, 2 or `output`, 3 or `input_output`, 4 or `three_state`, 5 or `open_drain`, 6 or `io_open_drain`, 7 or `open_sink`, 8 or `io_open_sink`, 9 or `open_source`, 10 or `io_open_source`, 11 or `input_ecl`, 12 or `output_ecl`, 13 or `io_ecl`, 14 or `three_state_ecl`, 17 or `terminator`. Possible values are `input`, `output`, `input_output`, `three_state`, `open_drain`, `io_open_drain`, `open_source`, `io_open_source`, `terminator`, `input_ecl`, `output_ecl`, `io_ecl`, `three_state_ecl`, `open_sink`, `io_open_sink`, `series`, and `series_switch`.
`ramp_rwf=2`	Use the rising waveform or ramp data. Value 2 (default) means use the first two rising waveforms. Value 1 means use the first rising waveform. Value 0 means use ramp data. Possible values are `0`, `1`, and `2`.
`ramp_fwf=2`	Use the falling waveform or ramp data. Value 2 (default) means use the first two falling waveforms. Value 1 means use the first falling waveform. Value 0 means use ramp data. Possible values are `0`, `1`, and `2`.

Model Syntax

```
model modelName ibis_buffer parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`type=tristate`	Type of the buffer. Possible values are `input`, `output`, `io`, `tristate`, `opendrain`, `ioopendrain`, `opensource`, `ioopensource`, `terminator`, `inputecl`, `outputecl`, `ioecl`, `tristateecl`, `opensink`, and `ioopensink`.
`enable=high`	Polarity of the enable signal. Possible values are `low` and `high`.
`polarity=inv`	Polarity of the buffer. Possible values are `inv` and `noninv`.
`ccomp=0 F`	Node capacitance on the die pad.
`ccomp_pu=0 F`	Node capacitance between the die pad and pullup reference.
`ccomp_pd=0 F`	Node capacitance between the die pad and pulldown reference..
`ccomp_pc=0 F`	Node capacitance between the die pad and power clamp reference.
`ccomp_gc=0 F`	Node capacitance between the die pad and gnd clamp reference.
`rgnd (Ω)`	Resistor between the die pad and gnd clamp reference; only for terminator.
`rpower (Ω)`	Capacitance between the die pad and power clamp reference; only for terminator.
`rac (Ω)`	rac and cac are series R and C between the die pad and gnd; only for terminator.
`cac (F)`	rac and cac are series R and C between the die pad and gnd; only for terminator.

Multistage buffer parameters

`drvsh_model=[...]`	Driver Schedule name.
`drvsh_delay=[...] s`	Driver Schedule delay time. Format: [`rise_on_dly rise_off_dly fall_on_dly fall_off_dly`].

© 2023 Cadence Design Systems, Inc.

`drvsh_num`	Number of models in the Driver Schedule.
`drvsh_typ`	The type of models in the Driver Schedule.
`drvsh_file`	The ibis file where the Driver Schedule is in.
`drvsh_topname`	The top level model name.

© 2023 Cadence Design Systems, Inc.

Voltage reference parameters

`vrange=5.0 V`	Reference voltage.
`vref=[...] V`	Reference voltage, format [gnd pwr gnd_c pwr_c].

Voltage controlled current sources (I/V tables)

`pullup=[...]`	Pull-up current source, format [v1 i1 ...].
`pulldown=[...]`	Pull-down current source, format [v1 i1 ...].
`powerclamp=[...]`	Power clamp current source, format [v1 i1 ...].
`gndclamp=[...]`	Gnd clamp current source, format [v1 i1 ...].
`issopu=[...]`	ISSO PU, format [v1 i1 ...].
`issopd=[...]`	ISSO PD, format [v1 i1 ...].

Switching coefficients (W/T tables)

`uprise=[...]`	Pull-up source, rising edge, format [t1 w1 ...].
`upfall=[...]`	Pull-up source, falling edge, format [t1 w1 ...].
`downrise=[...]`	Pull-down source, rising edge, format [t1 w1 ...].
`downfall=[...]`	Pull-down source, falling edge, format [t1 w1 ...].

Test waveforms (V/T tables and I/T tables) and loads

`loadrise1=[...]`	Load for the rising waveform, format [v r c l].
`vtrise1=[...]`	Rising waveform, format [t1 v1 ...].
`iccrise1=[...]`	Composite Current after rising waveform1, format [t1 i1 ...].
`loadfall1=[...]`	Load for the falling waveform, format [v r c l].
`vtfall1=[...]`	Falling waveform, format [t1 v1 ...].
`iccfall1=[...]`	Composite Current after falling waveform1, format [t1 i1 ...].
`loadrise2=[...]`	Test load for the rising waveform, format [v r c l].

© 2023 Cadence Design Systems, Inc.

`vtrise2=[...]`	Rising waveform, format [t1 v1 ...].
`iccrise2=[...]`	Composite Current after rising waveform2, format [t1 i1 ...].
`loadfall2=[...]`	Test load for the falling waveform, format [v r c l].
`vtfall2=[...]`	Falling waveform, format [t1 v1 ...].
`iccfall2=[...]`	Composite Current after falling waveform2, format [t1 i1 ...].
`ramp=[...]`	Rise and fall time, format [dv_rise dt_rise dv_fall dt_fall].

Input logic parameters

`vth=[...] V`	Low and High switching threshold, format [vth_lo vth_hi].

When `file` and `model` parameters are given, buffer model information is read from the `model` section of the `file`. It is assumed that file has standard IBIS format if it has an extension `.ibs`.

If `vref` is not given, reference voltages are set according to `vrange` value: vref=[0 vrange 0 vrange]. If reference voltage terminals are provided for the buffer instance, then both vref and vrange are ignored.

Multistaged buffers can be modeled as multiple simple ibis buffers connected in parallel. Each stage may have different on and off switching delay relatively to the initial transition edge. Driver schedule has to be specified only for the instances, which are part of multistaged buffer.

Differential buffer can be modeled by a pair of buffers, one for inverting pin, and another for non-inverting pin. Instance parameter `polarity` is used to override the buffer model polarity. In the case of output buffer, `delay` sets transition delay for non-inverting pin relatively to the inverting one. For differential input buffer the inverse pin have to be specified, and `vdiff` instance parameter overrides threshold voltages defined in the model.

Note: SPECTRE supports `C_comp_pullup`, `C_comp_pulldown`, `C_comp_power_clamp`, and `C_comp_gnd_clamp` in the IBIS model only when `C_comp` is not specified in the same model. If `C_comp` and `C_comp_*` are specified simultaneously in the same model, then SPECTRE just uses `C_comp` and ignores the value of `C_comp_*`.

© 2023 Cadence Design Systems, Inc.

Slow/Fast Corners

Slow/fast corners are composition of minimal and maximal value of some parameters, as shown in the table below:

Parameter	**corner=slow**	**corner=fast**
Ccomp	maximal	minimal
Voltage_Range	minimal	maximal
Pullup_Ref	minimal	maximal
Pulldown_Ref	maximal	minimal
POWER_Clamp_Ref	minimal	maximal
GND_Clamp_Ref	maximal	minimal
Rpower	minimal	maximal
Rgnd	minimal	maximal
Pullup	minimal	maximal
Pulldown	minimal	maximal
POWER_Clamp	minimal	maximal
GND_Clamp	minimal	maximal
Ramp	minimal	maximal
Rising_Wave	minimal	maximal
Falling_Wave	minimal	maximal
Rac	minimal	maximal
Cac	maximal	minimal
ISSO_PU	minimal	maximal
ISSO_PD	minimal	maximal
Composite Current	minimal	maximal

Related Topics

Ideal Switch (switch)

© 2023 Cadence Design Systems, Inc.

Ratiometric Fourier Analyzer (fourier)

Circuit Components

© 2023 Cadence Design Systems, Inc.

2

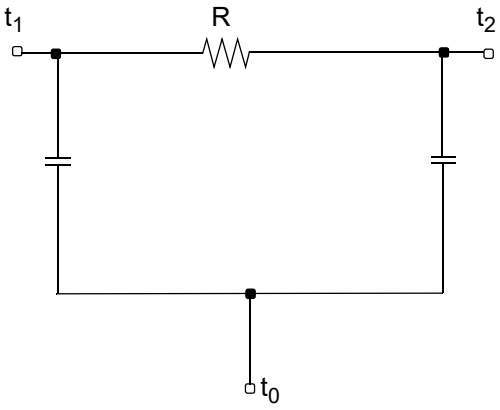
Passive Components

Click to view the details of the following passive components:

- Two Terminal Resistor
- Physical Resistor (phy_res)
- R2 Model (r2)
- Fractional Impedance/Admittance Pole (fracpole)
- Two-Terminal Capacitor (capacitor)
- Junction Capacitor (juncap)
- JUNCAP2 Model (juncap200)
- Junction Capacitor (juncap_eldo)
- Two Terminal Inductor (inductor)
- Mutual Inductor (mutual_inductor)
- Magnetic Core with Hysteresis (core)
- Winding for Magnetic Core (winding)
- Linear Inductance, Reluctance, Resistance, and Capacitance Matrix (rlck_matrix)

© 2023 Cadence Design Systems, Inc.

Two Terminal Resistor (resistor)



Two Terminal Resistor

If $R(inst)$ is not given and $R(model)$ is given,

$$R(inst) = R(model)$$

Otherwise,

$$R(inst) = Rsh \times \frac{(L - 2 \times etchl)}{(W - 2 \times etch)}$$

If the polynomial coefficients vector (*coeffs=[c1 c2 ...]*) is specified, the resistor is nonlinear. When `nonlinform` is set to `g`, the conductance is

$$G(V) = \frac{dI}{dV}$$
$$= \frac{(1 + c1 \times V + c2 \times V^2 + \ldots)}{R(inst)}$$

The branch current as a function of applied voltage is

$$I(V) = \left(\frac{V}{R(inst)}\right) \times \left(1 + \frac{1}{2} \times c1 \times V + \frac{1}{3} \times c2 \times V^2 + \ldots\right)$$

© 2023 Cadence Design Systems, Inc.

When `nonlinform` is set to `r`, the resistance is

$$R(V) = \frac{dV}{dI}$$
$$= R(inst) \times (1 + c1 \times V + c2 \times V^2 + \ldots)$$

where *ck* is the *k*th entry in the coefficient vector.

The value of the resistor as a function of the temperature is given by

$$R(T) = R(tnom) \times [1 + tc1 \times (T - tnom) + tc2 \times (T - tnom)^2]$$

where

$$T = trise(inst) + temp$$

if *trise(inst)* is given, and

$$T = trise(model) + temp$$

Rac is an instance or model parameter used in AC analysis.

If Rac(inst) is not given and Rac(model) is given,

$$Rac(inst) = Rac(model)$$

The final effective value of AC resistance is:

$$Rac_\text{eff} = Rac(inst) \times (1.0 + tc1 \times (T - tnom) + tc2 \times (T - tnom)^2)$$

If:

- *Rac* is not specified either in the instance or in the model, *Rac_eff* is the resistor value at operating point.
- *Rac_eff* is less than 1.0e-10 ohms, *Rac_eff*=1.0e-10 ohms.

© 2023 Cadence Design Systems, Inc.

Noise Model

Thermal Noise:

$$\overline{i_T} = \frac{4kT}{R} \cdot \Delta f$$

where

R is the resistor value and T is the temperature.

Flicker Noise:

$$\overline{i_f} = \frac{KF \cdot I^{AF}}{f^{FEXP}} \cdot \frac{1}{Weff^{WEEXP} \cdot Leff^{LEEXP} \cdot W^{WDEXP} \cdot L^{LDEXP}} \cdot \Delta f$$

where:

KF, AF, FEXP, WEEXP, LEEXP, WDEXP, and LDEXP are model parameters, I is the current, f is the frequency, and W and L are the device width and length.

`Weff=W-2ETCH` and `Leff=L-2ETCHL`.

Related Topics

Physical Resistor (phy_res)

Wire RC Model

Component Statements

Passive Components

Wire RC Model

If you specify the capacitance for a two terminal resistor, the model is a Wire RC model. If you do not specify the capacitance explicitly, it is computed from the physical length and width of the resistor using *Cj* and *Cjsw*. You can use the model parameter *cratio* to allocate the

© 2023 Cadence Design Systems, Inc.

parasitic capacitance of the wire element between the model's input capacitor and output capacitor.

If *C(inst)* is not given and *C(model)* is given

$$C(inst) = C(model)$$

Otherwise,

$$C(inst) = Cj \times (L - 2 \times etch1) \times (W - 2 \times etch) + 2 \times Cjsw \times (W + L - 2 \times etch - 2 \times etch1)$$

The parasitic capacitance assigned to the input and output nodes is given by

$$C(1) = C(inst) \times cratio$$

$$C(2) = C(inst) \times (1 - cratio)$$

If Cj is not given, but thick is given and is nonzero, Cj is calculated as follows:

If di is given and is nonzero,

$$Cj = \frac{di \cdot \varepsilon o}{thick}$$

otherwise

$$Cj = \frac{\varepsilon ox}{thick}$$

where

εo = 8.8542149e-12 F/meter

εox = 3.453148e-11 F/meter

The value of each capacitor as a function of the temperature is given by

$$C(T) = C(tnom) \times [1 + tc1c \times (T - tnom) + tc2c \times (T - tnom)^2]$$

Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem) on page 286.

© 2023 Cadence Design Systems, Inc.

The length and width of the Wire RC model are also scaled by the model parameter *shrink*.

Related Topics

Physical Resistor (phy_res)

Component Statements

Passive Components

Component Statements

You can give the resistance explicitly or allow it to be computed from the physical length and width of the resistor. In either case, the resistance can be a function of temperature or applied voltage.

This device is supported within altergroups.

If R(inst) is not given and R(model) is given

R(inst) = R(model)

otherwise,

R(inst) = Rsh * (L - 2 * etchl) / (W - 2 * etch)

If the polynomial coefficients vector (coeffs=[c1 c2 ...]) is specified, the resistor is nonlinear. When nonlinform is set to g, the conductance is

G(V) = dI / dV

= (1 + c1 * V + c2 * V^2 + ...) / R(inst).

The branch current as a function of applied voltage is

I(V) = (V / R(inst)) * (1 + 1/2 * c1 * V + 1/3 * c2 * V^2 + ...)

When nonlinform is set to r, the resistance is

R(V) = dV / dI

= R(inst) * (1 + c1 * V + c2 * V^2 + ...).

where ck is the kth entry in the coefficient vector.

© 2023 Cadence Design Systems, Inc.

For AC analysis, RAC(inst) AC resistance will be used.

If RAC(inst) is not given, and RAC(model) is given,

RAC(inst) = RAC(model)

otherwise,

RAC(inst) will use DC resistance.

The value of the resistor as a function of the temperature is given by:

R(T) = R(tnom) * [1 + tc1 * (T - tnom) + tc2 * (T - tnom)^2]

where

T = trise(inst) + temp

if trise(inst) is given, and

T = trise(model) + temp

otherwise.

If you specify capacitance the model is a wire RC model. You can give the capacitance explicitly or allow it to be computed from the physical length and width of the resistor. The model parameter `cratio` can be used to allocate the parasitic capacitance of the wire element between the models input capacitor and output capacitor.

If C(inst) is not given and C(model) is given,

C(inst) = C(model).

Otherwise,

C(inst) = Cj * (L - 2 * etchl) * (W - 2 * etch) + 2 * Cjsw * (W + L - 2 * etch - 2 * etchl).

The parasitic capacitance assigned to the input and output nodes is given by:

C(1) = C(inst) * cratio

C(2) = C(inst) * (1 - cratio).

The value of each capacitor as a function of the temperature is given by:

C(T) = C(tnom) * [1 + tc1c * (T - tnom) + tc2c * (T - tnom)^2].

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

without model:

```
r1 (1 2) resistor r=1.2K rac=100K m=2
```

with model:

```
r1 (1 2) resmod l=8u w=1u
```

Sample Model Statement

```
model resmod resistor rsh=150 l=2u w=2u etch=0.05u tc1=0.1 tnom=27 kf=1
```

This device support behavior expression

Sample behavior Statement

```
r1 (1 0) resistor r=rsh*(1 + v(1,2)*c1 + v(1,2)^2*c2)
r1 (1 0) resistor r= 100 + sqrt($freq)/1e6
```

Instance Syntax

```
Name  1  2  [0] ModelName parameter=value ...
Name  1  2  [0] resistor parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

r (Ω)	Resistance.
l (m)	The length of the resistor.
w (m)	The width of the resistor.
lvl=0	The metal layer of the resistor.
m=1	Multiplicity factor.
scale=1	Scale factor.
resform	Use the resistance form for this instance. Default is yes if r < thresh. Possible values are no or yes.
tc1=0 1/C	Linear temperature coefficient(alias=lv3,tc1r).
tc1r=0 1/C	Alias for tc1.
tc2=0 C^{-2}	Quadratic temperature coefficient(alias=lv4,tc2r).
tc2r=0 C^{-2}	Alias for tc2.
trise (C)	Temperature rise from ambient.
isnoisy=yes	Should resistor generate noise. Possible values are no or yes.
bv_max=∞	Maximum allowed voltage across two terminals.
c (F)	Capacitance.
tc1c=0 1/C	Linear temperature coefficient of capacitor.
tc2c=0 C^{-2}	Quadratic temperature coefficient of capacitor.
rac (Ω)	Default AC resistance, (alias=ac).
scaler	Resistance scaling factor.
scalec	Capacitance scaling factor.
dtemp (C)	Alias of Temperature rise from ambient.
cap (F)	Alias of capacitance.

The instance parameter scale, if specified, overrides the value given by the option parameter scale. The w and l parameters are scaled by the resulting scale, and the option parameter scalem. The parameters w and l are scaled also by the model parameter shrink.The values of w and l printed out by spectre are those given in the input, and these values might not have the correct units if the scaling factors are not unity. The correct effective resistor dimensions

© 2023 Cadence Design Systems, Inc.

are stored in the output parameters. You can obtain these dimensions by using the info statement.

Model Syntax

```
model modelName resistor parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Resistance parameters

`r=0.0` Ω	Default resistance.
`rsh=0.0` Ω/sqr	Sheet resistance.
`thresh=1.0e-3` Ω	Resistances smaller than this will use the resistance form, as opposed to the standard conductance form.
`rthresh=1.0e-3` Ω	Alias of thresh.
`rac=0.0` Ω	Default AC resistance.

Resistor size parameters

`l=0.0 m`	Default resistor length.
`w=1e-6 m`	Default resistor width.
`etch=0 m`	Width narrowing due to etching per side.
`etchl=0 m`	Length narrowing due to etching per side.
`scaler=1`	Resistance scaling factor.

Temperature effects parameters

`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0` C^{-2}	Quadratic temperature coefficient.
`tnom (C)`	Parameters measurement temperature. Default set by `options`.
`trise=0 C`	Default temperature rise from ambient.

Nonlinear resistance

`coeffs=[...]`	Vector of polynomial conductance coefficients.
`nonlinform=g`	The form of the nonlinear resistance. Possible values are `g` or `r`.

© 2023 Cadence Design Systems, Inc.

`symmetric=none`	Use symmetric resistor model. Possible values are `none`, `absolute` or `smooth`.

© 2023 Cadence Design Systems, Inc.

Noise model parameters

`kf=0`	Flicker (1/f) noise coefficient.
`af=2`	Flicker (1/f) noise exponent.
`wdexp=1`	Flicker (1/f) noise W exponent.
`ldexp=1`	Flicker (1/f) noise L exponent.
`weexp=0`	Flicker (1/f) noise W effective exponent.
`wf=0`	Alias of flicker (1/f) noise W effective exponent, default value=1 when spice compatible.
`leexp=0`	Flicker (1/f) noise L effective exponent.
`lf=0`	Alias of flicker (1/f) noise L effective exponent, default value=1 when spice compatible.
`fexp=1`	Flicker (1/f) noise frequency exponent.

DC-mismatch model parameters

`mr=0.0`	Resistor mismatch dependence.
`mrl=0.0 1/m^mrlp`	Resistor mismatch length dependence.
`mrlp=0.0`	Resistor mismatch length power dependence.
`mrw=0.0 1/m^mrwp`	Resistor mismatch width dependence.
`mrwp=0.0`	Resistor mismatch width power dependence.
`mrlw1=0.0 1/m^(2 mrlw1p)`	Resistor mismatch area 1 dependence.
`mrlw1p=0.0`	Resistor mismatch area 1 power dependence.
`mrlw2=0.0 1/m^(2 mrlw2p)`	Resistor mismatch area 2 dependence.
`mrlw2p=0.0`	Resistor mismatch area 2 power dependence.

Wire RC parameters

`c=0 F`	Default capacitance.
`cj=0 F/m`^{2}	Bottomwall capacitance.

© 2023 Cadence Design Systems, Inc.

`cjsw=0 F/m`	Sidewall fringing capacitance.
`thick=0 m`	Dielectric thickness.
`di=0`	Relative dielectric constant.
`cratio=0.5`	Cratio.
`tc1c=0 C`$^{-2}$	Linear temperature coefficient of capacitor.
`tc2c=0 C`$^{-2}$	Quadratic temperature coefficient of capacitor.
`shrink=1`	Shrink Factor.
`scalec=1`	Capacitance scaling factor.
`dtemp=0 C`	Alias of default temperature rise from ambient.
`cap=0 F`	Alias of default capacitance.
`dw=0 m`	Alias of width narrowing due to etching per side.
`dlr=0 m`	Alias of length narrowing due to etching per side.
`cox=0 F/m`^{2}	Alias of bottomwall capacitance.
`capsw=0 F/m`	Alias of sidewall fringing capacitance.
`res=0` Ω	Alias of default resistance.
`ef=1`	Alias of flicker (1/f) noise frequency exponent.

Safe operating areas parameters

`bv_max=`∞	Maximum allowed voltage across two terminals.

The instance parameter resform and the model parameter thresh control whether a resistor is formulated in the standard conductance form, or in the resistance form. If the value of the resistor is smaller than thresh, Spectre uses the resistance form; otherwise it uses the conductance form. If resform is set on an instance, it overrides the thresh parameter. The resistance form is appropriate for small resistances and the conductance form is intended for larger resistances. Using the conductance form for small resistances or the resistance form for large resistances can cause convergence problems.

With the resistance form, the resistance can be zero; with the conductance form, the resistance can be infinite. The resistance form is less efficient than the conductance form. You cannot change the formulation of a resistor once it has been determined. Spectre makes this choice by comparing the initial value of the resistance to thresh.

© 2023 Cadence Design Systems, Inc.

If the polynomial coefficients vector is specified and symmetric=absolute, the resistor model is symmetric. When nonlinform is set to g, the conductance is

G(V) = dI / dV

= (1 + c1 * |V| + c2 * |V|^2 + ...) / R(inst)

where |V| = ABS(V(1) - V(2)) and ck is the kth entry in the coefficient vector.

When nonlinform is set to r, the resistance is

R(V) = dV / dI

= R(inst) * (1 + c1 * |V| + c2 * |V|^2 + ...)

where |V| = ABS(V(1) - V(2)).

If symmetric=smooth the smoothing function f(V) is used:

f(V) = V * V / sqrt(V * V + 0.00001).

For nonlinform=g the conductance is

G(V) = dI / dV

= (1 + c1 * f(V) + c2 * f(V)^2 + ...) / R(inst).

Modeling AC resistance

In certain situations, a part of a circuit that is required to calculate the DC operating point needs to be removed during a subsequent AC analysis or visa versa. An example of a situation in which this occurs is when measuring the loop gain of a feedback amplifier. In this case the feedback loop must be removed when computing the AC response of the amplifier. In Spectre, the most accurate method of doing this is to use an ideal switch component (see `spectre -h switch`), e.g.

Vin (pin 0) vsource mag=1

OA1 (pin nin out) opamp

Sw1 (nin out 0) switch position=1 ac_position=2

LoopGain ac start=1 stop=1MHz

© 2023 Cadence Design Systems, Inc.

Another possibility is that the resistance of an instance changes from one analysis to another. The following subcircuit models a resistance whose value is given by the parameter `rac` during AC analyses, and `rdc` for all other analyses.

```
subckt ac_res (a b)
    parameters rdc=1 rac=2
    R1 (a i) resistor r=rdc
    Rac (i b) resistor r=rac-rdc
    Sw (i b) switch position=1 ac_position=0
ends ac_res
```

Output Parameters

`leff (m)`	Effective resistor length.
`weff (m)`	Effective resistor width.
`reff (Ω)`	Effective resistance.
`ceff (F)`	Effective capacitance.
`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`trise (C)`	Temperature rise from ambient.
`v (V)`	Voltage at operating point.
`i (A)`	Current through the resistor.
`res (Ω)`	Resistance at op point.
`pwr (W)`	Power dissipation.

Related Topics

Physical Resistor (phy_res)

© 2023 Cadence Design Systems, Inc.

Wire RC Model

Passive Components

Physical Resistor (phy_res)

A physical resistor consists of a two terminal resistor (tied between `t1` and `t2`) and two diodes (tied between `t1`-`t0` and `t2`-`t0`). The diodes are junction diodes. Under normal operation, the two diodes are reverse biased, but the parameter `subtype` can reverse the direction of the diodes. If you do not specify `t0`, ground is assumed. The instance parameters always override model parameters. If you do not specify the instance resistance value, it is calculated from the model parameters.

This device is supported within altergroups.

If R(inst) is not given and R(model) is given,

R(inst) = R(model).

Otherwise,

R(inst) = Rsh * (L - 2 * etchl) / (W - 2 * etch).

If the polynomial coefficients vector (coeffs=[c1 c2 ...]) is specified, the resistor is nonlinear. When `nonlinform` is set to `g`, the conductance is

G(V) = dI / dV

= (1 + c1 * V + c2 * V^2 + ...) / R(inst)

where

V = V(t1) - V(t2)

Here V is the controlling voltage across the resistor. It is also the controlling voltage when the model parameter `polyarg` is set to `diff`. In this form, the physical resistor is symmetric with respect to V(t1) and V(t2). The branch current as a function of the applied voltage is given by

I(V) = (V / R(inst)) * (1 + 1/2 * c1 * V + 1/3 * c2 * V^2 + ...)

where ck is the kth entry in the coefficient vector.

If the model parameter `polyarg` is set to `sum`, then the controlling voltage is defined as

© 2023 Cadence Design Systems, Inc.

Vsum = ((V(t1) - V(t0)) + (V(t2) - V(t0)))/2

Here, Vsum is the controlling voltage between the resistor and the substrate, `t0`. In this case, the device becomes asymmetric with respect to V(t1) and V(t2). The branch current as a function of the applied voltage for this case is given by

I(Vsum) = (V / R(inst)) * (1 + c1 * Vsum + c2 * Vsum^2 + ...)

The large-signal conductance is given by

G(Vsum) = I/V = (1 + c1 * Vsum + c2 * Vsum^2 + ...) / R(inst)

Note, since the device is asymmetrical, the small-signal model is more complicated then a simple conductance.

When `nonlinform` is set to `r`, the resistance is

R(V) = dV / dI

= R(inst) * (1 + c1 * V + c2 * V^2 + ...).

The resistance as a function of temperature is given by:

R(T) = R(tnom) * [1 + tc1 * (T - tnom) + tc2 * (T - tnom)^2].

where

T = trise(inst) + temp

if trise(inst) is given, and

T = trise(model) + temp

otherwise.

If you do not specify the junction leakage current (`is`) and `js` is specified, the leakage current is calculated from `js` and the device dimensions.

is = js * 0.5 * (L - 2 * etchl) * (W - 2 * etch)

If you specify the instance capacitance or the linear model capacitance, linear capacitors are used between `t1`-`t0` and `t2`-`t0`. Otherwise, nonlinear junction capacitors are used and the zero-bias capacitance values are calculated from the model parameters.

If C(inst) is not given and C(model) is given,

© 2023 Cadence Design Systems, Inc.

C(inst) = C(model).

Otherwise,

C(inst) = 0.5 * Cj * (L - 2 * etchlc) * (W - 2 * etchc) + Cjsw * (W + L - 2 * etchc - 2 * etchlc).

If the capacitance is nonlinear, the temperature model for the junction capacitance is used. Otherwise, the following equation is used.

C(T) = C(tnom) * [1 + tc1c * (T - tnom) + tc2c * (T - tnom)^2].

Thermal Noise

$$\overline{i_T} = \frac{4kT}{R} \cdot \Delta f$$

where:

R is the resistor value and T is the temperature.

Shot Noise for the Junctions

$$\overline{i_S} = 2 \cdot q \cdot I \cdot \Delta f$$

Where I is the current flow through the junction.

Flicker Noise for the Resistor

$$\overline{i_f} = \frac{KF \cdot I^{AF}}{f^{FEXP}} \cdot \frac{1}{Weff^{WEEXP} \cdot Leff^{LEEXP} \cdot W^{WDEXP} \cdot L^{LDEXP}} \cdot \Delta f$$

Where KF, AF, FEXP, WEEXP, LEEXP, WDEXP and LDEXP are model parameters, I is the current, W and L are the device width and length, `Weff=W-2ETCH` and `Leff=L-2ETCHL`.

© 2023 Cadence Design Systems, Inc.

Flicker Noise for the Junctions

$$\bar{i}_f = \frac{KF \cdot I^{AF}}{f^{FEXP}} \cdot \Delta f$$

Where:

Where KF, AF and FEXP are model parameters, I is the current, and f is the frequency.

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

```
res1 (net9 vcc) resphy l=1e-3 w=2e-6
```

Sample Model Statement

```
model resphy phy_res rsh=85 tc1=1.53e-3 tc2=4.67e-7 etch=0 cj=1.33e-3 cjsw=3.15e-10 tc1c=9.26e-4
```

Instance Syntax

```
Name  1  2  [0] ModelName parameter=value ...
```

Instance Parameters

r (Ω)	Resistance.
c (F)	Linear capacitance.
l (m)	Line length.
w (m)	Line width.
region=normal	Estimated operating region. Spectre generates output number (0-1) in a rawfile. Possible values are normal or breakdown.
tc1=0 1/C	Linear temperature coefficient of resistor.
tc2=0 C^{-2}	Quadratic temperature coefficient of resistor.
tc1c=0 1/C	Linear temperature coefficient of linear capacitor.
tc2c=0 C^{-2}	Quadratic temperature coefficient of linear capacitor.
trise (C)	Temperature rise from ambient.
isnoisy=yes	Should resistor generate noise. Possible values are no or yes.
m=1	Multiplicity factor.

The w and l parameters are scaled by the option parameters scale and scalem. The values of w and l printed by Spectre are those given in the input file. These values may not have the correct units if the scaling factors are not unity. The correct effective resistor dimensions are stored in the output parameters. You can obtain these dimensions with the info statement. You can delete the diodes from the device by either setting is=0 or subtype=poly. You can also set both mj and mjsw to zero to make the capacitance linear but still calculated from the

© 2023 Cadence Design Systems, Inc.

device geometry. If `subtype=poly`, the linear capacitors will always be used irrespective of the values of `mj` and `mjsw`.

Model Syntax

```
model modelName phy_res parameter=value ...
```

Model Parameters

Substrate type parameters

`subtype=p`	Substrate type. Possible values are `n`, `p` or `poly`.

© 2023 Cadence Design Systems, Inc.

Resistance parameters

`r=∞ Ω`	Default resistance.
`rsh=∞ Ω/sqr`	Sheet resistance.
`minr=0.1 Ω`	Minimum resistance.
`coeffs=[...]`	Vector of polynomial conductance or resistance coefficients.
`nonlinform=g`	The form of the nonlinear resistance. Possible values are `g` or `r`.
`polyarg=diff`	Polynomial model argument type. Possible values are `sum` or `diff`.

Temperature effects parameters

`tc1=0 1/C`	Linear temperature coefficient of resistor.
`tc2=0` C^{-2}	Quadratic temperature coefficient of resistor.
`tc1c=0` C^{-2}	Linear temperature coefficient of linear capacitor.
`tc2c=0` C^{-2}	Quadratic temperature coefficient of linear capacitor.
`tnom (C)`	Parameters measurement temperature. Default set by `options`.
`trise=0 C`	Temperature rise from ambient.

Junction diode model parameters

`is (A)`	Saturation current.
`js=0` A/m^2	Saturation current density.
`n=1`	Emission coefficient.
`eg=1.11 V`	Band gap.
`xti=3`	Saturation current temperature exponent.
`imelt=`imax' A`	Explosion current, diode is linearized beyond this current to aid convergence.
`jmelt=`jmelt' A/m`^{2}	

© 2023 Cadence Design Systems, Inc.

	Explosion current density, diode is linearized beyond this current to aid convergence.
`imax=1 A`	Maximum current, currents above this limit generate a warning.
`jmax=1e8 A/m`^{2}	Maximum current density, currents above this limit generate a warning.
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`. Possible values are `no` or `yes`.
`bvj=∞ V`	Junction reverse breakdown voltage.

© 2023 Cadence Design Systems, Inc.

Junction capacitance model parameters

`c=0 F`	Default linear capacitance.
`cj=0 F/m`^{2}	Zero-bias junction bottom capacitance density.
`cjsw=0 F/m`	Zero-bias junction sidewall capacitance density.
`mj=1/2`	Junction bottom grading coefficient.
`mjsw=1/3`	Junction sidewall grading coefficient.
`pb=0.8 V`	Junction bottom built-in potential.
`pbsw=0.8 V`	Junction sidewall built-in potential.
`fc=0.5`	Junction bottom capacitor forward-bias threshold.
`fcsw=0.5`	Junction sidewall capacitor forward-bias threshold.
`tt=0 s`	Transit time.

Device size parameters

`l=∞ m`	Default line length.
`w=1e-6 m`	Default line width.
`etch=0 m`	Narrowing due to etching.
`etchl=0 m`	Length reduction due to etching.
`etchc=etch m`	Narrowing due to etching for capacitances.
`etchlc=etchl m`	Length reduction due to etching for capacitances.
`scaler=1`	Resistance scaling factor.
`scalec=1`	Capacitance scaling factor.

Noise model parameters

`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`wdexp=1`	Flicker (1/f) noise W exponent.
`ldexp=1`	Flicker (1/f) noise L exponent.
`weexp=0`	Flicker (1/f) noise W effective exponent.

© 2023 Cadence Design Systems, Inc.

`leexp=0`	Flicker (1/f) noise L effective exponent.
`fexp=1`	Flicker (1/f) noise frequency exponent.

© 2023 Cadence Design Systems, Inc.

DC-mismatch model parameters

`mr=0.0` Ω^2	Resistor mismatch dependence.
`mrl=0.0` Ω^2`/m^mrlp`	Resistor mismatch length dependence.
`mrlp=0.0`	Resistor mismatch length power dependence.
`mrw=0.0` Ω^2`/m^mrwp`	Resistor mismatch width dependence.
`mrwp=0.0`	Resistor mismatch width power dependence.
`mrlw1=0.0` Ω^2`/m^(2 mrlw1p)`	Resistor mismatch area 1 dependence.
`mrlw1p=0.0`	Resistor mismatch area 1 power dependence.
`mrlw2=0.0` Ω^2`/m^(2 mrlw2p)`	Resistor mismatch area 2 dependence.
`mrlw2p=0.0`	Resistor mismatch area 2 power dependence.

Output Parameters

`leff (m)`	Effective line length.
`weff (m)`	Effective line width.
`iseff (A)`	Effective saturation current.
`reff (`Ω`)`	Effective resistance.
`ceff (F)`	Effective zero-bias capacitance.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`subtype=p`	Substrate type. Possible values are `n`, `p` or `poly`.
`region=normal`	Estimated operating region. Spectre generates output number (0-1) in a rawfile. Possible values are `normal` or `breakdown`.

© 2023 Cadence Design Systems, Inc.

`i (A)`	Current through the resistor.
`capd1 (F)`	Capacitance at the positive node.
`capd2 (F)`	Capacitance at the negative node.
`id1 (A)`	Current between nodes `t1` and `t0`.
`id2 (A)`	Current between nodes `t2` and `t0`.
`res (Ω)`	Resistance between nodes `t1` and `t2`.
`resd1 (Ω)`	Resistance between nodes `t1` and `t0`.
`resd2 (Ω)`	Resistance between nodes `t2` and `t0`.
`pwr (W)`	Power at op point.

Related Topics

Two Terminal Resistor (resistor)

R2 Model (r2)

Passive Components

R2 Model (r2)

The R2 model is a nonlinear 2-terminal resistor model. The model does not include parasitic capacitances. As an option, the model can include self-heating. The nonlinearity form is from Agere Systems, and effectively implements first and second order electric field coefficients of resistance. The R2 model does not have the numerical problems that can arise in polynomial models. Although empirical, the form of the nonlinearity can model data reasonably well, especially for velocity saturation effects which are important in short resistors.

Usage

With model card:

```
r<instanceName> (<node1> <node2> [dt]) <modelName> <instanceParameters> model
<modelName> r2 <modelParameters>
```

Without model card:

```
r<name> (<node1> <node2> [dt]) r2 r=<resistanceValue> [tc1=<tc1Value>]
[tc2=<tc2Value>]
```


© 2023 Cadence Design Systems, Inc.

The dt node is the rise above the local temperature caused by the thermal power dissipated by the device being modeled.

Examples

```
r137 (n1 n2) rnpoly1 w=1u l=10u
model rnpoly1 r2
+ rsh=100.0 xl=0.2u xw=-0.05u
+ p3=0.12 q3=1.63 p2=0.014 q2=3.79
```

Equivalent Circuit

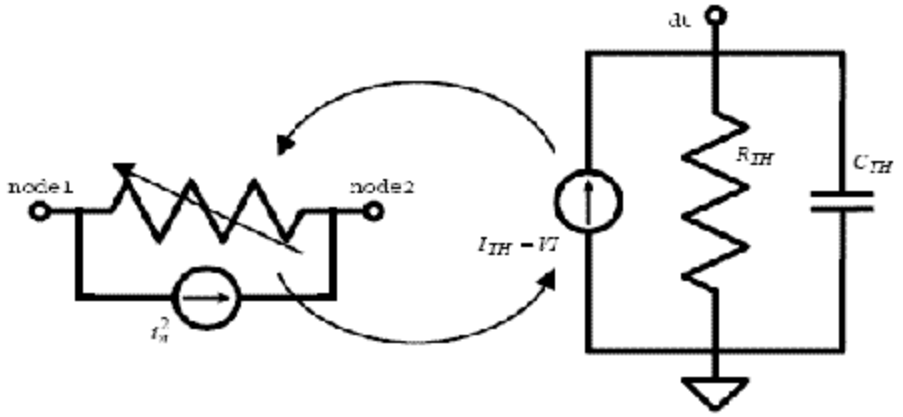


Figure 2-1 Model Equivalent Network (the thermal sub-network is optional)

Bias Dependence

If V is the voltage between the terminals node1 and node2, then the current flowing from node1 to node2 is

(2-1)

$$I = \frac{V}{r_\mathrm{dc}}$$

the DC bias dependent resistance is

(2-2)

$$r_\mathrm{dc} = R_0(T) \cdot rFactor$$

© 2023 Cadence Design Systems, Inc.

where $R_0(T)$ is the zero-bias resistance at the device temperature (which includes self-heating for the electrothermal version of the model), and the bias-dependent resistance factor is

(2-3)

$$rFactor = 1 - p2 - p3 + p2\sqrt{1 + (q2\mathrm{E})^2} + p3\sqrt[3]{1 + |q3\mathrm{E}|^3}$$

The electric field E can be calculated based on either the design length or the effective electrical length, depending on the switch parameter `sw_efgeo`. This is because, depending upon how the model is used and the model parameters are characterized, there can be effects in the value of `xl` (the parameter that defines the difference between the design length and the effective electrical length) that are not related to velocity saturation (e.g. if end spreading and/or contact resistance are included in xl). If `sw_efgeo` is `1` (`true`), the electric field is calculated from the effective geometry.

(2-4)

$$\mathrm{E} = \frac{V}{leff_\mathrm{um} + dxle}$$

otherwise it is calculated from the design geometry,

(2-5)

$$\mathrm{E} = \frac{V}{\mathrm{l_um} + dxle}$$

In both cases, an additional length offset `dxle` is included to allow flexibility and optimization in fitting data by separating the lengths used for resistance and field nonlinearity calculation. Although there is a singularity at $V = E = 0$ because of the absolute value operation in Equation 2-3 on page 224, the derivative of Equation 2-1 on page 223 with respect to voltage is defined and continuous up to third order. The fourth order derivative does not exist at $V = 0$ and its left limit does not equal its right limit there.

For the electrothermal version of the model, the thermal power is calculated as

(2-6)

$$I_{TH} = V \cdot I$$

and the powers that flow through the thermal resistance and thermal capacitance are

© 2023 Cadence Design Systems, Inc.

(2-7)

$$T(dt)*g_{TH}$$

and

(2-8)

$$ddt(T(dt)*c_{TH})$$

respectively, where *T*(dt) is the local temperature rise due to self-heating and the thermal conductance and capacitance are g_{TH} and c_{TH}, respectively. The thermal admittance is $y_{TH} = g_{TH} + j\omega c_{TH}$.

The thermal power after simulation convergence is:

(2-9)

$$I_{TH} = T(dt)*g_{TH} + ddt(T(dt)*c_{TH})$$

Geometry Dependence

The basic calculation for the (zero bias) resistance of a resistor is $R_0 = rsh L/W$. Because of several physical effects, the length and width used in this calculation differ from the design (or mask) length and width that define the resistor layout.

The r2 model incorporates a simple, fixed offset between design and effective (electrical) length and width. Because subcircuit models for resistors can consist of multiple resistance sections connected in series, it is desirable to be able to switch on and off the end corrections for length to facilitate implementation of such multi-section models. This is the function of the c1 and c2 instance parameters of the r2 model. The effective length offset is

(2-10)

$$xleff = xl(c1 + c2)/2$$

(which is zero if neither end is contacted, xl if both ends are contacted, and xl/2 if only one end is contacted).

The design length and width, in units of microns, are

© 2023 Cadence Design Systems, Inc.

(2-11)

$$l_\text{um} = l \cdot scale \cdot (1 - shrink/100) \cdot 10^6$$

(2-12)

$$w_\text{um} = l \cdot scale \cdot (1 - shrink/100) \cdot 10^6$$

where conversions from optical shrinking and unit scale conversion are included. If `scale` is `1` then `l` and `w` should be specified on model instances in meters. If scale is `1.0e-6` then `l` and `w` should be specified in units if microns. The effective electrical dimensions are

(2-13)

$$leff_\text{um} = l_\text{um} + xleff$$

(2-14)

$$weff_\text{um} = w_\text{um} + xw$$

There are three modes of geometric calculation based on the instance parameters `w`, `l`, and `r`. All modes are based on resistance being specified (or calculated), at zero applied bias and at the nominal device temperature specified by the parameter `tnom`. The order of importance of considering the instance parameters is (in order of from most to least important) width, length, and resistance. If all are specified, the instance `r` value is ignored, and resistance is calculated from the specified length and width.

(2-15)

$$R_{0,\,nom} = r$$

and the effective width is calculated

(2-16)

$$weff_\text{um} = \frac{rsh}{R_{0,\,nom}} leff_\text{um}$$

and possibilities of zero resistance or length, and error conditions of negative length or width, are handled.

If resistance is specified, and length is not specified, then

© 2023 Cadence Design Systems, Inc.

(2-17)

$$R_{0,\,nom} = r$$

(2-18)

$$leff_\mathrm{um} = \frac{R_{0,\,nom}}{rsh} weff_\mathrm{um}$$

and again possibilities of zero resistance and error conditions of negative length or width are handled.

For any other combination of instance parameter specification (resistance is not specified, or if it is then both width and length, which override resistance specification, are also specified), then the resistance is calculated from the geometry,

(2-19)

$$R_{0,\,nom} = rsh \frac{leff_\mathrm{um}}{weff_\mathrm{um}}$$

and zero resistance or conductance, and negative length or width errors, are handled.

Although end effects, such as spreading resistance and contact resistance, are assumed to be modeled via the `xl` parameter, the temperature coefficients of the end effects may differ from those of the body of the resistor. Simple analysis shows that these different temperature coefficients can be accounted for by introducing inverse length dependence to the temperature coefficients. A width dependence of temperature coefficients of resistance is also included in the model. Therefore in the R2 model,

(2-20)

$$T_{C1}^{eff} = tc1 + \frac{0.5(c1 + c2)tc1l}{leff_\mathrm{um}} + \frac{tc1w}{weff_\mathrm{um}}$$

(2-21)

$$T_{C2}^{eff} = tc2 + \frac{0.5(c1 + c2)tc2l}{leff_\mathrm{um}} + \frac{tc2w}{weff_\mathrm{um}}$$

where the length dependence is switched on, off, or halved, depending on whether the resistor is contacted at both ends, not contacted, or contacted at only one end, respectively. The dependence of the temperature coefficients on whether a resistor is contacted or not enables consistent modeling of temperature coefficients for single or multiple section models.

© 2023 Cadence Design Systems, Inc.

The thermal conductance and capacitance include area, perimeter, and fixed components. Asymptotically for a large area device, the heat flow is perpendicular to the plane of heat generation in the resistor, and the heat energy stored in a device depends on its volume, hence the area dependent component. For a long resistor, as it becomes narrower, more of the heat flow is conducted by a fringe path at the edges of the device, hence the perimeter dependent component. As both length and width decrease, the thermal conditions in the device asymptotically approach that of a point source in an infinite medium, hence the fixed component. The thermal conductance and capacitance are therefore

(2-22)

$$g_{TH} = gth0 + gthp \cdot p_\mathrm{um} + gtha \cdot a_\mathrm{um2}$$

(2-23)

$$c_{TH} = cth0 + cthp \cdot p_\mathrm{um} + ctha \cdot a_\mathrm{um2}$$

where the area and perimeter are calculated as

(2-24)

$$a_\mathrm{um2} = l_\mathrm{um} \cdot w_\mathrm{um}$$

(2-25)

$$p_\mathrm{um} = 2l_\mathrm{um} + (c1 + c2)w_\mathrm{um}$$

The calculated perimeter therefore depends on whether the ends are contacted or not. Often, the design dimensions of the body of a resistor differ from the overall dimensions of the device, for example if the design length is considered to be the unsolicited length of a poly resistor, the total resistor length will typically include silicided contact regions. So it is not readily apparent what dimension should be used in calculation of the thermal conductance and capacitance. That is why the design dimensions, rather than some effective dimensions (whose value is calculated to best fit DC electrical data), are used. This turns out to be fine (with the exception that differences between the perimeter components along length and width dimensions are ignored), because if there is some difference Δ between design and effective dimensions for thermal conductance modeling, then for a device contacted at both ends

(2-26)

$$\begin{aligned} g_{TH} &= gth0 + gthp(2l_\mathrm{um} + 2w_\mathrm{um} + 4\Delta) + gtha(l_\mathrm{um} + \Delta)(w_\mathrm{um} + \Delta) \\ &= (gth0 + 4gthp \cdot \Delta + gtha \cdot \Delta^2) + (gthp + 0.5gtha \cdot \Delta)p_\mathrm{um} + gtha \cdot a_\mathrm{um2} \end{aligned}$$

© 2023 Cadence Design Systems, Inc.

therefore, any difference between design and effective dimensions can be taken into account by appropriate characterization of the fixed, perimeter, and area component parameters.

Because the local thermal conductance differs between the edge of a device and the center of a device, it is higher at the edge because of fringing conductance, the temperature of a resistor undergoing self-heating is not spatially uniform, but is lower at the edges than in the middle. This is not taken into account in the R2 model.

Temperature Dependence

The zero-bias resistance $R0$ varies with temperature as

(2-27)

$$R_0(T) = R_{0,nom}(1 + T_{C1}^{eff} dT + T_{C2}^{eff} dT^2)$$

where $R_{0,nom}$ is the nominal value of the zero-bias resistance, at the nominal temperature `tnom`, dT is the temperature difference (including self-heating, if that form of the model is used) with respect to `tnom`, and

T_{c2}^{eff}

and

T_{c1}^{eff}

are first (linear) and second (quadratic) order temperature coefficients. These coefficients have both a width dependence and a length dependence, the latter to enable modeling of resistors that have different temperature coefficients for end resistance (which includes contacts and contact enhancement regions) compared to body resistance without having to implement a sectional (subcircuit) model with explicit end and body resistance components. The width and length dependency is detailed in the section on geometry dependence — see Equation 2-20 on page 227 and Equation 2-21 on page 227. Smooth limiting of the resistance temperature coefficient in (Equation 2-22 on page 228) is implemented to limit its lower value to 0.01.

For the isothermal version of the model the temperature difference dT is calculated statically based on the device temperature (which can vary from the circuit ambient temperature by setting the instance parameter `trise`, which is the local device temperature difference with respect to the circuit ambient temperature). For the electrothermal version of the model *dT* is calculated dynamically and self-consistently with the power dissipation of the device.

© 2023 Cadence Design Systems, Inc.

The flicker noise coefficient varies with temperature as

(2-28)

$$K_{FN}(T) = kfn(1 + tc1kfndT)$$

where `kfn` and `tc1kfn` are model parameters.

Noise

The noise model comprises two components, a thermal (white) noise component and a flicker ker ($1/f$) noise component. These components are noise current spectral density (in A^2/Hz) that are implemented as a noise current sources in parallel with the resistance element.

The thermal noise component is based on the DC conductance of the device,

(2-29)

$$i^2_{thermal} = 4kT_K G_0(T)/rFactor$$

where k is Boltzmann's constant, T_K is the device temperature (in Kelvin, including the effect of self-heating), G_0 is the zero-bias conductance of the resistor (at the temperature `T`), and $rFactor$ is the bias-dependent (DC) resistance factor (Equation 2-3 on page 224).

The flicker noise component is DC current dependent (Equation 2-2 on page 223), and scales with geometry per the physical restrictions noted in Equation 2-3 on page 224.

(2-30)

$$i^2_{flicker} = K_{FN}(T)\left(\frac{I}{W}\right)^{afn}\frac{W}{L}\frac{1}{f^{bfn}}$$

where f is frequency (in Hz), `afn` and `bfn` are model parameters, $K_{FN}(T)$ is the temperature dependent flicker noise coefficient (Equation 2-28 on page 230), I is the DC current in the resistor, and W and L are the resistor width and length, respectively, in units of micron. If the switch parameter for flicker noise geometry calculation `sw_fngeo` is 0 (`false`) then W and L are design geometries, w_um and l_um respectively, else if it is 1 (`true`) then W and L are effective geometries, $weff_um$ and $leff_um$ respectively.

Note: If self-heating is included, then possibly there is a frequency dependence to the flicker noise because of the thermal time constant. There is no data to verify this at present so a frequency independent noise current spectral density is used.

© 2023 Cadence Design Systems, Inc.

Description and Details

The voltage nonlinearity of the device resistance is

(2-31)

$$R(E) = R_0\left((1 - p2 - p3) + p3\sqrt[3]{1 + |q3\mathrm{E}|^3} + p2\sqrt{1 + (q2\mathrm{E})^2}\right)$$

where R_0 is the zero bias resistance of the resistor, $E=V/L$ is the electric field across the device, `p3` and `q3` are parameters of the effective first order (linear) electric field coefficient, and `p2` and `q2` are parameters of the effective second order (quadratic) electric field coefficient. Because the nonlinearity is based on field, rather than voltage, it scales with geometry.

For q3E somewhat greater than 1, the cubic component of the model becomes

(2-32)

$$R(E) = R_0(1 + p3(|q3\mathrm{E}| - 1))$$

therefore this term approximates a linear (first order) field dependence of resistance with a coefficient of value `p3.q3`.

For q2E somewhat less than 1, the quadratic component of the model becomes

(2-33)

$$R(E) = R_0(1 + 0.5p2 \cdot q2^2E^2)$$

therefore this term approximates a quadratic (second order) field dependence of resistance with a coefficient of value `0.5p2*q2`^{2}. For high fields this component becomes

(2-34)

$$R(E) = R_0(1 + p2(|q2\mathrm{E}| - 1))$$

and it turns out that the behavior embodied in Equation 2-33 on page 231 and Equation 2-34 on page 231 is quite accurate for modeling velocity saturation, which is a significant component of nonlinearity for shorter resistors.

To ensure that the resistance does not become negative,

© 2023 Cadence Design Systems, Inc.

(2-35)

$$0 \le p3 < 1$$

and

(2-36)

$$0 \le p2 < 1 - p3$$

are enforced. This also precludes the model exhibiting a negative differential resistance (NDR). NDR is observed in some devices, but this is from self-heating effects in resistors with positive temperature coefficients. This behavior should therefore be modeled using the electrothermal version of the model.

In SPICE-like simulators, which are based on modified nodal analysis (MNA), it is preferable to formulate models as voltage controlled current sources (VCCS's). This is the default for the R2 model. For small resistance values this can cause numerical problems, and the MNA formulation is not possible for zero valued resistors (which have infinite conductance). For small resistance values it is better to switch to a current controlled voltage source (CCVS) formulation. Implicitly, this increases the matrix size for MNA analysis, as the current through the CCVS becomes a system variable. The R2 model includes a parameter `rthresh`, and if the total (not per segment, but r/m) resistance at zero bias is less than `rthresh`, the model switches to a CCVS formulation for numerical stability and to be able to work properly for zero valued resistors. This makes the model implicit as the formulation is effectively $V=I \cdot R(V)$.

Related Topics

Two Terminal Resistor (resistor)

Physical Resistor (phy_res)

Component Statements

Passive Components

Component Statements

Instance Syntax

```
Name  1  2 ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

```
Name  1  2 r2 parameter=value ...
```

Instance Parameters

`m=1`	Multiply factor.
`w=1e-6 m`	Default width.
`l=1e-6 m`	Resistor length.
`r=100.0 Ω`	Resistance.
`c1=1`	Contact terminal.
`c2=1`	Contact terminal.
`trise=0.0 C`	Temperature rise.
`isnoisy=yes`	Should resistor generate noise. Possible values are `no` or `yes`.
`sw_et=yes`	switch for turning off self-heating.
`tc1=0.0 /K`	resistance linear.
`tc2=0.0 /K`	resistance linear.

Model Syntax

```
model modelName r2 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

version=1.0	Model version selector. The available versions are 1.0.
revision=0.0	Model sub-version selector. The available versions are 0.0.
shrink=0.0 %	Shrink factor.
tmin=-100 C	The minimal temperature.
tmax=500.0 C	The maximal temperature.
rthresh=1e-3 Ω	threshold.
level=1002	r2 model selector. The available level are 1002.
tnom=27.0 C	Reference temperature.
rsh=∞ Ω/sqr	Sheet resistance.
lmin=0.0 µm	Minimum channel length for which the model is valid.
lmax=9.9e99 µm	Maximum channel length for which the model is valid.
wmin=0.0 µm	Minimum channel width for which the model is valid.
wmax=9.9e99 µm	Maximum channel width for which the model is valid.
xw=0.0 µm	Width offset.
xl=0.0 µm	Length offset.
dxle=0.0 µm	Length delta.
sw_efgeo=no	Switch for electric field geometry calculation.
q3=0.0 µm/V	Threshold for the linear field coefficient activities.
p3=0	Coefficient for linear field.
q2=0.0 µm/V	Threshold for the quadratic field coefficient activities.
p2=0	Coefficient for quadratic field.
kfn=0	Coefficient for flicker noise.
afn=2.0	Flicker noise current exponent.
bfn=1.0	Coefficient for quadratic field.
sw_fngeo=no	Switch for flicker noise geometry calculation.
jmax=100.0 A/µm	Maximum allowable current density.
tminclip=-100.0 C	Clip minimum temperature.

© 2023 Cadence Design Systems, Inc.

`tmaxclip=500.0 C`	clip maximum temperature.
`tc1=0.0 /K`	Resistance linear.
`tc2=0.0 /K`^{2}	Resistance quadratic.
`tc1l=0.0 µm/K`	tc length coefficient for resistance linear.
`tc2l=0.0 µm/K`^{2}	tc length coefficient for resistance quadratic.
`tc1w=0.0 µm/K`	tc width coefficient for resistance linear.
`tc2w=0.0 µm/K`^{2}	tc width coefficient for resistance quadratic.
`tc1kfn=0`	Coefficient for flicker noise linear tc1.
`gth0=1.0e6 W/K`	Thermal conductance fixed component.
`gthp=0.0 W/Kµm`	Thermal conductance perimeter component.
`gtha=0.0 W/Kµm`^{2}	Thermal conductance area component.
`cth0=0.0 sW/K`	Thermal capacitance fixed component.
`cthp=0.0 sW/Kµm`	Thermal capacitance perimeter component.
`ctha=0.0 sW/Kµm`^{2}	Thermal capacitance area component.
`c1=1`	Resistance contact terminal.
`c2=1`	Resistance contact terminal.

Operating-Point Parameters

`v (V)`	Voltage at operating point.
`i (A)`	Current through the resistor.
`power (W)`	Power dissipated.
`pwr (W)`	Power dissipated.
`r0 (Ω)`	zero bias resistance.
`leff_um (µm)`	effective length in um.
`weff_um (µm)`	effective width in um.
`r_dc (Ω)`	DC Resistance.
`r_ac (Ω)`	AC Resistance.
`rth (K/W)`	Thermal Resistance.

© 2023 Cadence Design Systems, Inc.

0	`cth (sW/K)`	Thermal capacitance.
1	`dt_et (C)`	The self-heating temperature rise.

Related Topics

Two Terminal Resistor (resistor)

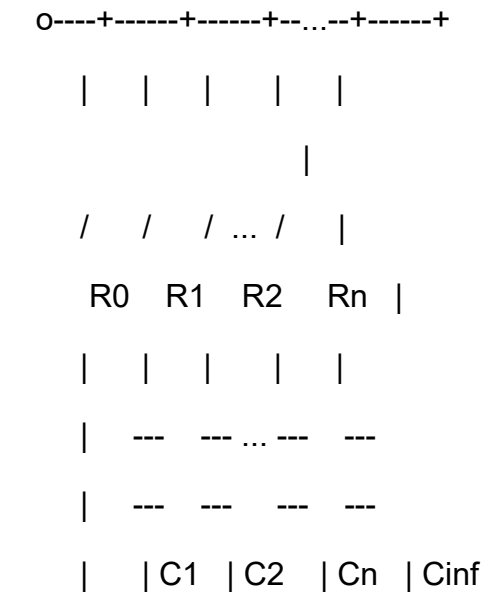
Physical Resistor (phy_res)

R2 Model (r2)

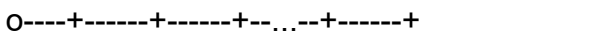
Passive Components

Fractional Impedance/Admittance Pole (fracpole)

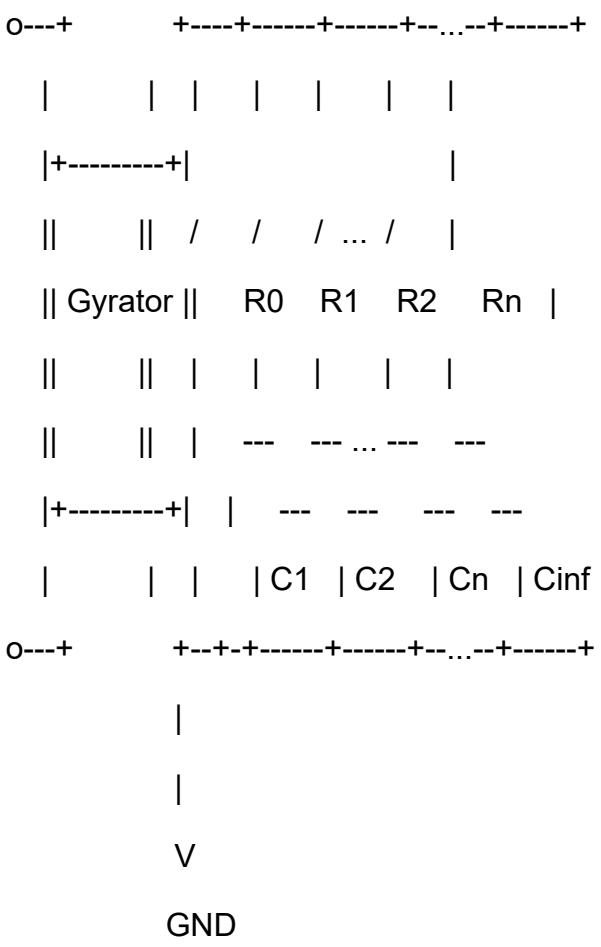
Fractional Impedance Pole takes as input a start frequency, a stop frequency, a negative slope, the unity intercept point, and the number of lumps, and synthesizes a RC circuit that models a fractional impedance pole over the given frequency range. The circuit is a one-port that exhibits poles and zeros that are real and that are spaced evenly in a logarithmic sense over the frequency range. The impedance exhibited by the one port approximates a fractional pole slope between -1 and 0 in the frequency range. In other words, if the impedance is plotted on a log-log scale, it will have a negative slope equal to the fraction specified. The user requested half a pole, the slope will be -1/2, etc. Of course it is a lumped approximation, so the slope will not be exact, but it will slowly oscillate about the desired value.



© 2023 Cadence Design Systems, Inc.



This model is converted to model a Fractional Admittance Pole by combining it with a gyrator.



It can be used to model skin-effect loss in an inductor and dielectric absorption in a capacitor, and can be used to shape white noise into flicker noise.

Profile

In both fractional impedance/admittance pole cases, what happens outside the range of the approximation is specifies the parameter `profiles` of fracpole. It is a code that consists of a pair of letters. The first letter represents the low frequency behavior and the second represents the high frequency behavior. The letters are either `f` or `d`, `f` represents flat or a zero-pole slope, and `d` represents down or a one-pole slope. Depending on the profile chosen, either R0 or Cinf may or may not be present in the synthesized RC circuit.

Internal Nodes

© 2023 Cadence Design Systems, Inc.

Internal nodes are created for each RC pair in the synthesized RC circuit, and they are labeled as InstanceName:int_1, InstanceName:int_2, ... In the case of fractional admittance pole, one more additional internal node, InstanceName:int_gyr, is created on the opposite side of gyrator from the terminals of the device.

Current

The current reported by fracpole device is the static terminal current. In the case of fractional impedance pole, this current does not include the dynamic part. To find the total current of fractional impedance pole, either use current probe in series with it or use the option useprobes=yes.

This device is supported within altergroups.

Fractional Impedance Pole approximates

$$Z(s) = Coef*s^{Slope}$$

for s=2*pi*freq*j with f0 < freq < f1, and -1 < Slope < 0.

Fractional Admittance Pole approximates

$$Z(s) = Coef*s^{Slope}$$

(or $Y(s) = s^{(-Slope)}/Coef$)

for s=2*pi*freq*j with f0 < freq < f1, and 0 < Slope < 1.

Sample Instance Statement

without model:

fp (1 2) fracpole f0=1 f1=1M coef=1k dec=1.0 slope=-0.5 profile=ff

with model:

fp (1 2) fpModel f0=1 f1=1M coef=1.5k lumps=12 slope=-0.5 profile=dd

Sample Model Statement

model fpModel fracpole f0=1 f1=1M coef=1k dec=1.0 slope=-0.5 profile=ff

Instance Syntax

```
Name  1  2 ModelName parameter=value ...
Name  1  2 fracpole parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`f0=1.0 Hz`	Low frequency limit for the approximation.
`f1=1.0e6 Hz`	High frequency limit for the approximation.
`coef=1.0 Ω`	Unity intercept point for ideal impedance at 2*pi*freq=1.
`slope=-0.5`	Slope of the impedance when plotted on a log-log scale.
`lumps`	Number of lumps used in the approximation.
`dec=1.0`	Number of lumps per decade used in the approximation.
`profile=dd if abs(slope)`	
`m=1.0`	Multiplicity factor.
`ic (V)`	Initial condition for fractional impedance pole devices with `df` or `dd` profile.
`rforce=1.0 Ω`	Resistance used when forcing initial conditions.

Model Syntax

```
model modelName fracpole parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`f0=1.0 Hz`	Low frequency limit for the approximation.
`f1=1.0e6 Hz`	High frequency limit for the approximation.
`coef=1.0 Ω`	Unity intercept point for ideal impedance at 2*pi*freq=1.
`slope=-0.5`	Slope of the impedance when plotted on a log-log scale.
`lumps`	Number of lumps used in the approximation.
`dec=1.0`	Number of lumps per decade used in the approximation.
`profile=dd if abs(slope)`	

Operating-Point Parameters

`v (V)`	Voltage at operating point.
`i (A)`	Current. See comment on current above.
`pwr (W)`	Power dissipation.

Related Topics

Two-Terminal Capacitor (capacitor)

Two Terminal Capacitor with the specified Q factor (capq)

Junction Capacitor (juncap)

JUNCAP2 Model (juncap200)

Junction Capacitor (juncap_eldo)

Passive Components

Two-Terminal Capacitor (capacitor)

You can assign the capacitance or let Spectre compute it from the physical length and width of the capacitor. In either case, the capacitance can be a function of temperature or applied voltage.

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

If the `C(inst)` is not given,

```
C(inst) = C(model)
```

if `C(model)` is given,

and if `Area(inst)` or `Perim(inst)` is given

```
Area_eff = Area - (Perim)*etch + 4*etch^2
Perim_eff = Perim - 8*etch
```

else

```
Area_eff  = (L - 2*etch)*(W - 2*etch)
Perim_eff = 2 *(W + L - 4*etch)
C(inst) = Cj*Area_eff +  Cjsw*Perim_eff
```

if `C(model)` is not given.

If the polynomial coefficients vector (`coeffs=[c1 c2 ...]`) is specified, the capacitor is nonlinear and the capacitance is

```
C(V) = dQ(V) / dV
     = C(inst)*(1 + c1*V + c2*V^2 + ...)
```

or

```
Q(V) = C(inst)*V*(1 + 1/2*c1*V + 1/3*c2*V^2 + ...)
```

where `ck` is the kth entry in the coefficient vector.

The value of the capacitor as a function of the temperature is given by:

```
C(T) = C(tnom)*[1 + tc1*(T - tnom) + tc2*(T - tnom)^2]
```

where

```
T = trise(inst) + temp
```

if `trise(inst)` is given, and

```
T = trise(model) + temp
```

if trise`(inst)` is not given.

Sample Instance Statement

without model:

```
c2 (1 0) capacitor c=2.5u tc1=1e-8
```

with model:

© 2023 Cadence Design Systems, Inc.

```
c2 (1 0) proc_cap c=2.5u tc1=1e-8
```

Sample Model Statement

```
model proc_cap capacitor c=2u tc1=1.2e-8 tnom=25
```

This device supports behavior expression

Sample Behavior Statement

```
c1 (1 0) capacitor c=c0*(1 + tanh(v(1,2)*c2))
c1 (1 0) capacitor c=1e-12/(1+($freq)/1e9)
```

Instance Syntax

```
Name  1  2 ModelName parameter=value ...
Name  1  2 capacitor parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

c	(F)	Capacitance.
c0	(F)	0th order value of polynomial capacitor.
w	(m)	Capacitor width.
l	(m)	Capacitor length.
m	1	Multiplicity factor.
scale	1	Scale factor.
trise	(C)	Temperature rise from ambient.
tc1	(1/C)	Linear temperature coefficient.
tc2	(C^{-2})	Quadratic temperature coefficient.
ic	(V)	Initial condition(alias=lv2).
area	1.0 m^2	Capacitor area.
perim	0.0 m	Capacitor perimeter.
coeffs	[...]	Vector of polynomial capacitance coefficients.
symmetric	none	Use symmetric capacitor model.Possible values are none and absolute.
bv_max	infinity V	Maximum allowed voltage cross two terminals.
scalec		Capacitance scaling factor.
bv_min	-infinity V	Minimum allowed voltage cross two terminals.

© 2023 Cadence Design Systems, Inc.

The instance parameter `scale`, if specified, overrides the value given by the option parameter `scale`. The `w` and `l` parameters are scaled by the resulting scale, and the option parameter `scalem`. The values of `w` and `l` printed by Spectre are those given in the input file, and these values might not have the correct units if the scaling factors are not unity. The correct capacitor dimensions are stored in the output parameters. You can obtain these dimensions with the `info` statement.

Model Syntax

```
model modelName capacitor parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`c`	`0 F`	Default capacitance.
`trise`	`0 C`	Default `trise` value for instance.
`tnom`	`(C)`	Parameter measurement temperature. The default value is set using the options statement.
`w`	`0 m`	Default capacitor width.
`l`	`0 m`	Default capacitor length.
`etch`	`0 m`	Narrowing due to side etching.
`cj`	`0` F/m^2	Bottom capacitance density.
`cjsw`	`0 F/m`	Sidewall capacitance.
`scalec`	`1`	Capacitance scaling factor.
`rforce`	`1` Ω	Resistance used when forcing initial conditions.
`di`	`0`	Relative dielectric constant.
`thick`	`0 m`	Dielectric thickness.

Polynomial capacitor *parameters*

`coeffs`	`[...]`	Vector of polynomial capacitance coefficients.
`symmetric`	`none`	Use symmetric resistor model.Possible values are none and absolute.
`min`	`(F)`	Minimum capacitance.
`max`	`(F)`	Maximum capacitance.

© 2023 Cadence Design Systems, Inc.

Temperature effects parameters

tc1	0 1/C	Linear temperature coefficient.
tc2	0 C^{-2}	Quadratic temperature coefficient.

Shrink Parameters

shrink	0.0	Linear shrink parameter.
shrink2	0.0	Area shrink parameter.

Safe Operating Areas Parameters

bv_max	infinity V	Maximum allowed voltage across two terminals.
bv_min	-infinity V	Minimum allowed voltage across two terminals.

Output Parameters

tempeff	(C)	Effective temperature for a single device.
meff		Effective multiplicity factor (m-factor).
leff	(m)	Effective capacitor length.
weff	(m)	Effective capacitor width.
ceff	(F)	Effective capacitance(alias=lv1).

© 2023 Cadence Design Systems, Inc.

Related Topics

Fractional Impedance/Admittance Pole (fracpole)

Two Terminal Capacitor with the specified Q factor (capq)

Junction Capacitor (juncap)

JUNCAP2 Model (juncap200)

Junction Capacitor (juncap_eldo)

Passive Components

Two Terminal Capacitor with the specified Q factor (capq)

Description

The 'capq' instance is a capacitor with the Q factor 'q' specified at a particular frequency 'fq'. The parameter 'mode' specifies the exact form of the frequency dependence of the real part of the admittance Re(Y).

mode=1: Constant real part of the admittance Re(Y)=const.

mode=2: Re(Y) increases proportional to sqrt(freq).

mode=3: Re(Y) increases linearly with frequency.

mode=4: Re(Y) decreases proportional to (freq/fq)^alph.

This device is supported within altergroups.

The capq instance is an RC parallel branch with R being frequency-dependent and C=const.

Instance parameters: c, mode, fq, q.

The equations are written in terms of admittance Y, with w=2*Pi*freq and wq=2*Pi*fq:

mode=1: Re(Y)=wq*c/q=const; Im(Y)=w*C.

mode=2: Re(Y)=c*sqrt(wq*w)/q; Im(Y)=w*C.

mode=3: Re(Y)=w*c/q; Im(Y)=w*C.

© 2023 Cadence Design Systems, Inc.

mode=4: Re(Y)=w*c/Qf; Im(Y)=w*c; Qf=q*(freq/fq)^alph.

Sample Instance Statement:

Without model:

cq2 (1 0) capq c=2.5u mode=2 fq=1.3G q=120

cq2 (1 0) capq c=2.5u mode=4 fq=1.3G q=120 alph=1

With model:

cq2 (1 0) proc_capq

Sample Model Statement:

model proc_capq capq c=2u mode=1 fq=1.3G q=100

model proc_capq capq c=2u mode=4 fq=1.3G q=100 alph=1

This device does not support behavioral expressions.

Instance Syntax

```
Name  1  2 ModelName parameter=value ...
Name  1  2 capq parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

c	(F)	Capacitance.
ic	(V)	Initial condition(alias=lv2).
m	1	Multiplicity factor.
trise	(C)	Temperature rise from ambient.
q	50.0	Quality factor measured at the frequency 'fq'.
fq	1.0e8 Hz	Frequency at which 'q' is measured.
mode	1	Integer parameter that selects the frequency dependence.
isnoisy	yes	Should capq resistance generate noise.Possible values are no and yes.
alph	0	Scaling factor for Q in 'capq', qf=q*(freq/fq)^alph, Y=2*pi*freq*c*(1/qf+j).

The instance parameter mode defaults to 1, if not specified.

The Q factor defaults to q=50, and fq defaults to fq=0.1 GHz.

In transient simulations, the DC values are used.

© 2023 Cadence Design Systems, Inc.

Model Syntax

```
model modelName capq parameter=value ...
```

Related Topics

Fractional Impedance/Admittance Pole (fracpole)

Two-Terminal Capacitor (capacitor)

Junction Capacitor (juncap)

JUNCAP2 Model (juncap200)

Junction Capacitor (juncap_eldo)

Passive Components

Interconnect Capacitance (intcap)

Intcap is a model that is used for calculation of the interconnect capacitance, which takes into account the local layer composition and the tracks spacing width.It is described in the Phillips MOST Modelbook (Dec.96) as INTCAP model.

(c) Phillips Electronics N.V. 1993,1996

The model is extended by the device parameters `lxbelps`, `lxbelin` and `lxbelins`, according to the specification by H.Okel (I&A Hamburg).

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Sample Instance Statement:

intc (net9 net12) intconcap m=1 ael=2.5e-15 ain=2e-15 aps=1.8e-15

Sample Model Statement:

model intconcap intcap cbps=1.5e-13 cebpsm=0.9e-15 cebpsi=0.83e-15 cbin=1.45e-13 cbins=1.4e-13

© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  n1  n2 ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1`	Multiplicity factor.
`ael=0.0` m^2	The common area of `EL` track of the reference electrode.
`ain=0.0` m^2	The common area of `IN` track of the reference electrode.
`ains=0.0` m^2	The common area of `INS` track of the reference electrode.
`aps=0.0` m^2	The common area of `PS` track of the reference electrode.
`lbel=0.0 m`	The sum of periphery length of `EL`-segments common to node n2 downwards.
`lbin=0.0 m`	The sum of periphery length of `IN`-segments to node n2 downwards.
`lbins=0.0 m`	The sum of periphery length of `INS`-segments common to node n2 downwards.
`lbps=0.0 m`	The sum of periphery length of `PS`-segments common to node n2 downwards.
`lfbel=0.0 m`	The sum of periphery length-factor products `EL` downwards.
`lfbin=0.0 m`	The sum of periphery length-factor products `IN` downwards.
`lfbins=0.0 m`	The sum of periphery length-factor products `INS` downwards.
`lfbps=0.0 m`	The sum of periphery length-factor products `PS` downwards.
`lftel=0.0 m`	The sum of periphery length-factor products `EL` upwards.
`lftin=0.0 m`	The sum of periphery length-factor products `IN` upwards.
`lftins=0.0 m`	The sum of periphery length-factor products `INS` upwards.
`lftps=0.0 m`	The sum of periphery length-factor products `PS` upwards.
`ltel=0.0 m`	The sum of periphery length of `EL`-segments common to node n2 upwards.
`ltin=0.0 m`	The sum of periphery length of `IN`-segments common to node n2 upwards.
`ltins=0.0 m`	The sum of periphery length of `INS`-segments common to node n2 upwards.

© 2023 Cadence Design Systems, Inc.

`ltps=0.0 m`	The sum of periphery length of `PS`-segments common to node n2 upwards.
`ldsel=0.0 m`	The sum of Li/Si quotients for `EL` tracks.
`ldsin=0.0 m`	The sum of Li/Si quotients for `IN` tracks.
`ldsins=0.0 m`	The sum of Li/Si quotients for `INS` tracks.
`ldsps=0.0 m`	The sum of Li/Si quotients for `PS` tracks.
`lxbinps=0.0 m`	The sum of Li/Si quotients for an `IN` track in parallel with an `PS` track.
`lxbinsin=0.0 m`	The sum of Li/Si quotients for an `INS` track in parallel with an `IN` track.
`lxbinsps=0.0 m`	The sum of Li/Si quotients for an `INS` track in parallel with an `PS` track.
`lxbelps=0.0 m`	The sum of Li/Si quotients for an `EL` track in parallel with an `PS` track.
`lxbelin=0.0 m`	The sum of Li/Si quotients for an `EL` track in parallel with an `IN` track.
`lxbelins=0.0 m`	The sum of Li/Si quotients for an `EL` track in parallel with an `INS` track.

The Spectre option `scale`, default value is 1.0, scales the geometric

parameters. The areas (parameters starting with letter `a`) are equal

axxx * scale ^ 2

The lengths (parameters starting with letter `l`) are equal

lxxx * scale

Model Syntax

```
model modelName intcap parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`cbps=0.0 F/m`^{2}	Bottom capacitance, `PS` to node n2.
`cebpsm=0.0 F/m`	Edge to bottom capacitance (`PS`), 1.0um spacing.
`cebpsi=0.0 F/m`	Edge to bottom capacitance (`PS`), single track.
`cetpsm=0.0 F/m`	Edge to top capacitance (`PS`), 1.0um spacing.
`cetpsi=0.0 F/m`	Edge to top capacitance (`PS`), single track.
`cbin=0.0 F/m`^{2}	Bottom capacitance, `IN` to node n2.
`cebinm=0.0 F/m`	Edge to bottom capacitance (`IN`), 1.0um spacing.
`cebini=0.0 F/m`	Edge to bottom capacitance (`IN`), single track.
`cetinm=0.0 F/m`	Edge to top capacitance (`IN`), 1.0um spacing.
`cetini=0.0 F/m`	Edge to top capacitance (`IN`), single track.
`cbins=0.0 F/m`^{2}	Bottom capacitance, `INS` to node n2.
`cebinsm=0.0 F/m`	Edge to bottom capacitance (`INS`), 1.0um spacing.
`cebinsi=0.0 F/m`	Edge to bottom capacitance (`INS`), single track.
`cetinsm=0.0 F/m`	Edge to top capacitance (`INS`), 1.0um spacing.
`cetinsi=0.0 F/m`	Edge to top capacitance (`INS`), single track.
`cbel=0.0 F/m`^{2}	Bottom capacitance, `EL` to node n2.
`cebelm=0.0 F/m`	Edge to bottom capacitance (`EL`), 1.0um spacing.
`cebeli=0.0 F/m`	Edge to bottom capacitance (`EL`), single track.
`cetelm=0.0 F/m`	Edge to top capacitance (`EL`), 1.0um spacing.
`ceteli=0.0 F/m`	Edge to top capacitance (`EL`), single track.
`cecps=0.0 F/m`	Lateral capacitance (`PS`), 1.0um spacing.
`cecin=0.0 F/m`	Lateral capacitance (`IN`), 1.0um spacing.
`cecins=0.0 F/m`	Lateral capacitance (`INS`), 1.0um spacing.
`cecel=0.0 F/m`	Lateral capacitance (`EL`), 1.0um spacing.

Output Parameters

`cap (F)`	Total Capacitance.

© 2023 Cadence Design Systems, Inc.

Related Topics

Fractional Impedance/Admittance Pole (fracpole)

Two-Terminal Capacitor (capacitor)

Junction Capacitor (juncap)

JUNCAP2 Model (juncap200)

Junction Capacitor (juncap_eldo)

Passive Components

Junction Capacitor (juncap)

This is SiMKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

Instance Syntax

```
Name  a  k ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`ab=1e-12` m^2	Diffusion area.
`ls=1e-06 m`	Length of the side-wall of the diffusion area AB which is not under the gate.
`lg=1e-06 m`	Length of the side-wall of the diffusion area AB which is under the gate.
`mult=1`	Number of devices in parallel.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `rev`, `fwd`, or `brk`.
`m=1`	Multiplicity factor.
`area=1.0e-12` m^2	Alias of `ab`.
`peri=0.0 m`	Alias of `ls`.
`pgate=0.0 m`	Alias of `lg`.
`pj=0.0 m`	Aias of `peri`.

Model Syntax

```
model modelName juncap parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1`	Level of this model.
`dta=0 K`	Temperature offset of the juncap element with respect to TA.
`tr=25 C`	Temperature at which the parameters have been determined.
`vr=0 V`	Voltage at which the parameters have been determined.
`jsgbr=0.001 Am`$^{-2}$	Bottom saturation-current density due to electron-hole generation at V=VR.
`jsdbr=0.001 Am`$^{-2}$	Bottom saturation-current density due to diffusion from back contact.
`jsgsr=0.001 Am^-1`	Sidewall saturation-current density due to electron-hole generation at V=VR.
`jsdsr=0.001 Am^-1`	Sidewall saturation-current density due to diffusion from back contact.
`jsggr=0.001 Am^-1`	Gate edge saturation-current density due to diffusion from back contact.
`jsdgr=0.001 Am^-1`	Gate edge saturation-current density due to diffusion from back contact.
`nb=1`	Emission coefficient of the bottom forward current.
`ns=1`	Emission coefficient of the sidewall forward current.
`ng=1`	Emission coefficient of the gate edge forward current.
`vb=0.9 V`	Reverse breakdown voltage.
`cjbr=1e-12 Fm`$^{-2}$	Bottom junction capacitance at V=VR.
`cjsr=1e-12 Fm^-1`	Sidewall junction capacitance at V=VR.
`cjgr=1e-12 Fm^-1`	Gate edge junction capacitance at V=VR.
`vdbr=1 V`	Diffusion voltage of the bottom junction at T=TR.
`vdsr=1 V`	Diffusion voltage of the sidewall junction at T=TR.
`vdgr=1 V`	Diffusion voltage of the gate edge junction at T=TR.
`pb=0.4`	Bottom junction grading coefficient.
`ps=0.4`	Sidewall junction grading coefficient.

© 2023 Cadence Design Systems, Inc.

`pg=0.4`	Gate edge junction grading coefficient.
`imax=1e+03 A`	Explosion current.
`shrink=0`	Linear shrink factor.
`shrink2=0`	Areal shrink factor.
`type=n`	Transistor gender. Possible values are `n`, `p`, `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, or `pnpl`.
`tnom (C)`	Alias of tnom.
`tref (C)`	Alias of tnom.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`dta (K)`	Temperature offset of the juncap element with respect to TA.
`tr (C)`	Temperature at which the parameters have been determined.
`vr (V)`	Voltage at which the parameters have been determined.
`isgb (Am^-2)`	Bottom saturation-current density due to electron-hole generation at V=VR.
`isdb (Am^-2)`	Bottom saturation-current density due to diffusion from back contact.
`isgs (Am^-1)`	Sidewall saturation-current density due to electron-hole generation at V=VR.
`isds (Am^-1)`	Sidewall saturation-current density due to diffusion from back contact.
`isgg (Am^-1)`	Gate edge saturation-current density due to electron-hole generation at V=VR.
`isdg (Am^-1)`	Gate edge saturation-current density due to diffusion from back contact.
`nb`	Emission coefficient of the bottom forward current.
`ns`	Emission coefficient of the sidewall forward current.
`ng`	Emission coefficient of the gate edge forward current.
`cjb (Fm^-2)`	Bottom junction capacitance at V=VR.
`cjs (Fm^-1)`	Sidewall junction capacitance at V=VR.
`cjg (Fm^-1)`	Gate edge junction capacitance at V=VR.
`vdb (V)`	Diffusion voltage of the bottom junction at T=TR.
`vds (V)`	Diffusion voltage of the sidewall junction at T=TR.
`vdg (V)`	Diffusion voltage of the gate edge junction at T=TR.
`pb`	Bottom junction grading coefficient.
`ps`	Sidewall junction grading coefficient.
`imax (A)`	Explosion current.
`vexpl (A)`	Explosion voltage.

© 2023 Cadence Design Systems, Inc.

`pg`	Gate edge junction grading coefficient.

Operating-Point Parameters

`g (S)`	Total differential conductance.
`c (F)`	Total capacitance.
`lx1 (A)`	Total current.
`lx3 (Coul)`	Total charge.
`lx5 (F)`	Total capacitance, identical to OP output c.
`ctotal (F)`	Total capacitance, identical to OP output c.
`vdio (V)`	Voltage across junction.
`pwr (W)`	Power for juncap.
`diode_region`	DIODE region. Possible values are `off` and `on`.

Related Topics

Fractional Impedance/Admittance Pole (fracpole)

Two-Terminal Capacitor (capacitor)

Two Terminal Capacitor with the specified Q factor (capq)

JUNCAP2 Model (juncap200)

Junction Capacitor (juncap_eldo)

Passive Components

JUNCAP2 Model (juncap200)

This is SiMKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  a  k ModelName parameter=value ...
```

Instance Parameters

`ab=1e-12` m^2	Junction area.
`ls=1e-06 m`	STI-edge part of junction perimeter.
`lg=1e-06 m`	Gate-edge part of junction perimeter.
`mult=1`	Number of devices in parallel.
`ifactor=1`	Multiplier for current.
`cfactor=1`	Multiplier for depletion capacitance.
`trise=0 K`	Temperature offset to the ambient temperature.
`region=off`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `rev`, `fwd` and `brk`.
`m=1`	Multiplicity factor.
`area=1.0e-12 for spice; 1 for spectre` m^2	Alias of ab for SPICE; alias of mult for Spectre.
`peri=0.0 m`	Alias of ls for SPICE.
`pgate=0.0 m`	Alias of lg for SPICE.
`pj=0.0 m`	Alias of peri for SPICE.

Model Syntax

```
model modelName juncap200 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=200`	Model level must be 200.
`type=n`	Type parameter, in output value 1 reflects n-type, -1 reflects p-type. Possible values are `n`, `p`, `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, or `pnpl`.
`trj=21 C`	Reference temperature.
`dta=0 C`	Temperature offset with respect to ambient temperature.
`imax=1e+03 A`	Maximum current up to which forward current behaves exponentially.
`cjorbot=0.001 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component.
`cjorsti=1e-09 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component.
`cjorgat=1e-09 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component.
`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component.
`pbot=0.5`	Grading coefficient of bottom component.
`psti=0.5`	Grading coefficient of STI-edge component.
`pgat=0.5`	Grading coefficient of gate-edge component.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component.

© 2023 Cadence Design Systems, Inc.

`idsatrbot=1e-12 Am^-2`

Saturation current density at the reference temperature of bottom component.

`idsatrsti=1e-18 Am^-1`

Saturation current density at the reference temperature of STI-edge component.

`idsatrgat=1e-18 Am^-1`

Saturation current density at the reference temperature of gate-edge component.

`csrhbot=100 Am^-3` Shockley-Read-Hall prefactor of bottom component.

`csrhsti=0.0001 Am^-2`

Shockley-Read-Hall prefactor of STI-edge component.

`csrhgat=0.0001 Am^-2`

Shockley-Read-Hall prefactor of gate-edge component.

`xjunsti=1e-07 m` Junction depth of STI-edge component.

`xjungat=1e-07 m` Junction depth of gate-edge component.

`ctatbot=100 Am^-3` Trap-assisted tunneling prefactor of bottom component.

`ctatsti=0.0001 Am^-2`

Trap-assisted tunneling prefactor of STI-edge component.

`ctatgat=0.0001 Am^-2`

Trap-assisted tunneling prefactor of gate-edge component.

`mefftatbot=0.25` Effective mass (in units of m0) for trap-assisted tunneling of bottom component.

`mefftatsti=0.25` Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component.

`mefftatgat=0.25` Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component.

`cbbtbot=1e-12 AV^-3`

Band-to-band tunneling prefactor of bottom component.

`cbbtsti=1e-18 AV^-3m`

Band-to-band tunneling prefactor of STI-edge component.

© 2023 Cadence Design Systems, Inc.

`cbbtgat=1e-18 AV^-3m`	Band-to-band tunneling prefactor of gate-edge component.
`fbbtrbot=1e+09 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component.
`fbbtrsti=1e+09 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component.
`fbbtrgat=1e+09 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component.
`stfbbtbot=-0.001 K^-1`	Temperature scaling parameter for band-to-band tunneling of bottom component.
`stfbbtsti=-0.001 K^-1`	Temperature scaling parameter for band-to-band tunneling of STI-edge component.
`stfbbtgat=-0.001 K^-1`	Temperature scaling parameter for band-to-band tunneling of gate-edge component.
`vbrbot=10 V`	Breakdown voltage of bottom component.
`vbrsti=10 V`	Breakdown voltage of STI-edge component.
`vbrgat=10 V`	Breakdown voltage of gate-edge component.
`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component.
`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component.
`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component.
`swjunexp=0`	Flag for JUNCAP-express; 0=full model, 1=express model.
`vjunref=2.5`	Typical maximum junction voltage; usually about 2*VSUP.
`fjunq=0.03`	Fraction below which junction capacitance components are considered negligible.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

1	`vak (V)`	Voltage between anode and cathode.
2	`cj (F)`	Total source junction capacitance.
3	`cjbot (F)`	Junction capacitance (bottom component).
4	`cjgat (F)`	Junction capacitance (gate-edge component).
5	`cjsti (F)`	Junction capacitance (STI-edge component).
6	`ij (A)`	Total source junction current.
7	`ijbot (A)`	Junction current (bottom component).
8	`ijgat (A)`	Junction current (gate-edge component).
9	`ijsti (A)`	Junction current (STI-edge component).
10	`si (A`^{2}`/Hz)`	Total junction current noise spectral density.

Related Topics

Fractional Impedance/Admittance Pole (fracpole)

Two-Terminal Capacitor (capacitor)

Two Terminal Capacitor with the specified Q factor (capq)

Junction Capacitor (juncap)

Junction Capacitor (juncap_eldo)

Passive Components

Junction Capacitor (juncap_eldo)

The juncap model is intended to describe the behavior of the juncaps that are formed by the source, drain or well-to-bulk junctions in MOS devices. It is described in the Phillips MOST Modelbook (Dec.93) as JUNCAP model. Information on how to obtain this document can be found on Source Link by searching for Phillips (c) Phillips Electronics N.V. 1994

In extension to the model book description a minimum conductance `gmin` is inserted between the juncap nodes, to aid convergence. The value of `gmin` is set by an options statement, default = 1e-12 S.

© 2023 Cadence Design Systems, Inc.

The `imax` parameter is used to aid convergence and to prevent numerical overflow. The junction characteristics of the junction capacitor are accurately modeled for currents up to `imax`. For currents above `imax`, the junction is modeled as a linear resistor and a warning is printed.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

Sample Instance Statement

```
c2 (1 2) capmod ab=7e-12 lg=5e-6 region=rev
```

Sample Model Statement

```
model capmod juncap type=n cjbr=0.2 cjgr=0.2 cjsr=0.2 tref=25 jsgbr=2e-3
jsdbr=0.28e-3 jsggr=1e-5 jsdgr=0.33e-6 vdsr=0.8 vdgr=0.8 vdbr=0.8
```

Instance Syntax

```
Name  n  [b] ModelName parameter=value ...
```

Instance Parameters

`ab=1.0 scale`^{2} `m`^{2}	Diffusion area. Scale set by option scale.
`ls=1.0 scale m`	Length of the sidewall of the diffusion area ab which is not under the gate. Scale set by option scale.
`lg=1.0 scale m`	Length of the sidewall of the diffusion area ab which is under the gate. Scale set by option scale.
`m=1.0`	Multiplicity factor.
`region=rev`	Estimated DC operating region, used as a convergence aid. Possible values are `fwd` or `rev`.

Model Syntax

```
model modelName juncap_eldo parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Structural parameters

`type=n`	Type of the juncap device. Possible values are `n` or `p`.
`vb (V)`	Not used for juncap model.
`bv (V)`	Alias of `vb`.
`level`	Not used for juncap model.

© 2023 Cadence Design Systems, Inc.

Current parameters

`jsgbr=1.0e-3 A/m`^{2}	Bottom saturation-current density due to electron-hole generation at reference voltage.
`jsdbr=1.0e-3 A/m`^{2}	Bottom saturation-current density due to diffusion from back contact.
`jsgsr=1.0e-3 A/m`	Sidewall saturation-current density due to electron-hole generation at reference voltage.
`jsdsr=1.0e-3 A/m`	Sidewall saturation-current density due to diffusion from back contact.
`jsggr=1.0e-3 A/m`	Gate edge saturation-current density due to electron-hole generation at reference voltage.
`jsdgr=1.0e-3 A/m`	Gate edge saturation-current density due to diffusion from back contact.
`imax=1.0 A`	Explosion current.

Temperature effects parameters

`dta=0.0 K`	Temperature offset of the juncap element with respect to ambient temperature.
`trise=0.0 K`	Alias of `dta`.
`tr (C)`	Temperature at which the parameters have been determined. Default set by option `tnom`.
`tref (C)`	Alias of tr. Default set by option `tnom`.
`tnom (C)`	Alias of tr. Default set by option `tnom`.

Junction capacitance parameters

`cjbr=1.0e-12 F/m`^{2}	Bottom junction capacitance at reference voltage.
`cjsr=1.0e-12 F/m`	Sidewall junction capacitance at reference voltage.
`cjgr=1.0e-12 F/m`	Gate edge junction capacitance at reference voltage.

© 2023 Cadence Design Systems, Inc.

Emission coefficient parameters

`nb=1.0`	Emission coefficient of the bottom forward current.
`ns=1.0`	Emission coefficient of the sidewall forward current.
`ng=1.0`	Emission coefficient of the gate-edge forward current.

Voltage parameters

`vr=0.0 V`	Voltage at which parameters have been determined.
`vdbr=1.0 V`	Diffusion voltage of the bottom junction at reference temperature.
`vdsr=1.0 V`	Diffusion voltage of the sidewall junction at reference temperature.
`vdgr=1.0 V`	Diffusion voltage of the gate edge junction at reference temperature.

Grading coefficient parameters

`pb=0.4`	Bottom-junction grading coefficient.
`ps=0.4`	Sidewall-junction grading coefficient.
`pg=0.4`	Gate edge-junction grading coefficient.

Compatibility model parameters

`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, or `spiceplus`.

Output Parameters

`cjb (F)`	Capacitance of bottom area `ab`.
`cjs (F)`	Capacitance of locos-edge `ls`.

© 2023 Cadence Design Systems, Inc.

`cjg (F)`	Capacitance of gate-edge `lg`.
`isdb (A)`	Diffusion saturation-current of bottom area `ab`.
`isds (A)`	Diffusion saturation-current of locos-edge `ls`.
`isdg (A)`	Diffusion saturation-current of gate-edge `lg`.
`isgb (A)`	Generation saturation-current of bottom area `ab`.
`isgs (A)`	Generation saturation-current of locos-edge `ls`.
`isgg (A)`	Generation saturation-current of gate-edge `lg`.
`vdb (V)`	Diffusion voltage of bottom area `ab`.
`vds (V)`	Diffusion voltage of locos-edge `ls`.
`vdg (V)`	Diffusion voltage of gate-edge `lg`.

Operating-Point Parameters

`v (V)`	juncap bias voltage (v = va - vk).
`i (A)`	Total resistive current from anode to cathode (i = ia = -ik).
`gm (S)`	Total differential conductance.
`q (Coul)`	Total junction charge (q = qa = -qk).
`c (F)`	Total capacitance.
`pwr (W)`	Power.

Related Topics

Fractional Impedance/Admittance Pole (fracpole)

Two-Terminal Capacitor (capacitor)

Two Terminal Capacitor with the specified Q factor (capq)

JUNCAP2 Model (juncap200)

Junction Capacitor (juncap)

Passive Components

© 2023 Cadence Design Systems, Inc.

Two Terminal Inductor (inductor)

The inductance of this component can be a function of temperature or branch current. If you do not specify the inductance in the instance statement, it is taken from the model statement.

The inductor component can also have the frequency-dependent Q-factor with three modes of frequency dependence. This mode `indq` has four optional parameters `mode`, `q`, `fq`, `rdc` and `alph`.

This device is supported within altergroups.

If the polynomial coefficients vector (coeffs=[c1 c2 ...]) is specified, the inductor is nonlinear and the inductance is

L(I) = L(inst) * (1 + c1 * I + c2 * I^2 + ...).

The branch flux as a function of current is

Flux(I) = L(inst) * I * (1 + 1/2 * c1 * I + 1/3 * c2 * I^2 + ...)

where ck is the kth entry in the coefficient vector.

The value of the inductor as a function of the temperature is given by:

L(T) = L(tnom) * [1 + tc1 * (T - tnom) + tc2 * (T - tnom)^2].

where

T = trise(inst) + temp

if trise(inst) is given, and

T = trise(model) + temp

otherwise.

Sample Instance Statement

without model:

```
l33 (0 net29) inductor l=10e-9 r=1 m=1
```

with model:

```
l33 (0 net29) ind l=10e-9 r=1 m=1
```


© 2023 Cadence Design Systems, Inc.

Sample Model Statement

```
model ind inductor l=6e-9 r=1 tc1=1e-12 tc2=1e-12 tnom=25
```

This device support behavior expression

Sample Behavior Statement

```
l33 (0 net29) inductor l=l0*(1 + v(net27, net28)*c1)
l33 (0 net29) inductor l=1e-9+1e-9/(1+($freq)/1e9)
```

Instance Syntax

```
Name  1  2 ModelName parameter=value ...
Name  1  2 inductor parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`l (H)`	Inductance value.
`r (Ω)`	Resistance value.
`m=1`	Multiplicity factor.
`trise (C)`	Temperature rise from ambient.
`ic (A)`	Initial condition (alias=lv2).
`isnoisy=yes`	Should inductor resistance generate noise. Possible values are `yes` and `no`.
`coeffs=[...]`	Vector of polynomial inductance coefficients.
`symmetric=none`	Use symmetric inductor model. Possible values are `none` and `absolute`.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0 C`$^{-2}$	Quadratic temperature coefficient.
`scalei`	Inductance scaling factor.
`mode=0`	Integer parameter used in 'indq' model.
`q=50.0`	Quality factor measured at the frequency 'fq'.
`fq=1e8 Hz`	Frequency at which 'l' and 'q' are measured.
`rdc=0.0 Ω`	DC resistance used in mode=2 and mode=3.
`alph=0`	Scaling factor for Q in 'indq', qf=q*(freq/fq)^alph, Z=2*pi*freq*L*(1/qf+j).

Model Syntax

```
model modelName inductor parameter=value ...
```

Model Parameters

`l=0 H`	Default inductance.
`r=0 Ω`	Default resistance.
`tc1=0 1/C`	Linear temperature coefficient.
`tc2=0 C`$^{-2}$	Quadratic temperature coefficient.

© 2023 Cadence Design Systems, Inc.

`trise=0 C`	Default `trise` value for instance.
`tnom (C)`	Parameter measurement temperature. The default value is set by the `options` statement.
`rforce=1e9` Ω^2	Resistance used when forcing nodesets and initial conditions.
`coeffs=[...]`	Vector of polynomial inductance coefficients.
`symmetric=none`	Use symmetric inductor model. Possible values are `none` and `absolute`.
`scalei=1`	Inductance scaling factor.
`mode=0`	Integer parameter used in 'indq' model.
`q=50.0`	Quality factor measured at the frequency 'fq'.
`fq=1.0e8 Hz`	Frequency at which 'l' and 'q' are measured.
`rdc=0.0` Ω	DC resistance used in mode=2 and mode=3.
`alph=0`	Scaling factor for Q in 'indq', qf=q*(freq/fq)^alph, Z=2*pi*freq*L*(1/qf+j).

© 2023 Cadence Design Systems, Inc.

Noise model parameters

`kf=0`	Flicker (1/f) noise coefficient.
`af=2`	Flicker (1/f) noise exponent.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`indeff (H)`	Effective inductance(alias=lv1).

Operating-Point Parameters

`trise (C)`	Temperature rise from ambient.
`ind (H)`	Inductance at operating point.
`i (A)`	Current at operating point (alias=lx2).
`pwr (W)`	Power dissipation.

Related Topics

Mutual Inductor (mutual_inductor)

Magnetic Core with Hysteresis (core)

Winding for Magnetic Core (winding)

Linear Inductance, Reluctance, Resistance, and Capacitance Matrix (rlck_matrix)

Passive Components

Mutual Inductor (mutual_inductor)

The mutual inductor couples two previously specified inductors. There is no limit to the number of inductors that you can couple or to the number of couplings to a particular inductor, but you must specify separate mutual inductor statements for each coupling. Using the `dot` convention, place a `dot` on the first terminal of each inductor.

© 2023 Cadence Design Systems, Inc.

This device is supported within altergroups.

The mutual inductor modifies the constitutive equations of two isolated inductors to

v1 = L11*di1/dt + M*di2/dt

v2 = M*di1/dt + L22*di2/dt

where the mutual inductance, M, is computed from the coupling coefficient, k, using k = |M|/ sqrt(L11*L22).

Sample Instance Statement with Two Inductors

```
l1 (1 0) inductor
l2 (2 0) inductor
ml1 mutual_inductor coupling=1 ind1=l1 ind2=l2
```

Instance Syntax

```
Name mutual_inductor parameter=value ...
```

Instance Parameters

`coupling=0`	Coupling coefficient.
`k=0`	Alias to coupling.
`ind1`	Inductor to be coupled.
`ind2`	Inductor to be coupled.

Output Parameters

`islinear`

Operating-Point Parameters

`mind (H)`	Mutual inductance between the inductors(alias=lv1).

Related Topics

Two Terminal Inductor (inductor)

© 2023 Cadence Design Systems, Inc.

Magnetic Core with Hysteresis (core)

Winding for Magnetic Core (winding)

Linear Inductance, Reluctance, Resistance, and Capacitance Matrix (rlck_matrix)

Passive Components

Magnetic Core with Hysteresis (core)

This component models the magnetic hysteresis, with air gap, frequency, and temperature effects. The model is based on the AWB model for magnetic cores and windings. The user has to specify the cores material and geometric parameters to model the hysteresis.

The material parameters to specify are the `Br`, `Bm` and `Hc` of the core. The geometric parameters are the area, magnetic path length and the air gap of the core.

You can specify the magnetic path length in one of the following ways:

Give the length directly in cm.

Or give the outer and inner diameter of the core.

Cores without terminals represent complete magnetic loops. Cores with terminals are fragments that you can use as building blocks to build models of complicated core structures. For example, you can use the following set of core fragments to model an `E` core:

```
W1  e1p  e1m  winding turns=80 core=C1

W3a e2p  e2c  winding turns=80 core=C3

W3b e2c  e2m  winding turns=80 core=C3

C1  m1   0    permalloy area=1 len=2

C2  m1   0    permalloy area=2 len=2

C3  m1   0    permalloy area=1 len=2

model permalloy core ...
```

There are three parallel core fragments representing each of the three fingers on the `E`. One 80 turn winding is connected to core fragment `C1`. A center-tapped 160 turn winding

© 2023 Cadence Design Systems, Inc.

(implemented as a pair of windings) is wrapped around core fragment `C3`. Node `m1` is a `magnetic` node whose value is in magnetomotive force and flow is flux.

You can calculate the frequency and temperature dependency of the core model by specifying the frequency loss parameters and the temperature effects parameters. You can make all the core parameters vary in temperature, including the permeability, saturation flux, and core loss. For frequency losses, a static model refers to a value that you type in for frequency. This model does not adjust the shape of the B-H loop in response to power dissipation or rate of rise of the applied currents and voltages during transient analysis.

This device is not supported within altergroup.

The hysteresis is modeled by different regions whose equations are:

phi = phir + (phis - phir) F/(F + Ha) for region number 1

phi = phis * (F - Fc)/(F - Hb) for region number 2

where phi = flux density

F = magnetomotive force

phir = residual flux density

phis = Saturated flux density

Fc = Coercive magnetic force

Ha and Hb are shape parameters.

Sample Instance Statement

```
c1 (1 0) core_mod area=1.2 len=8.1 id=0.55 gap=0.25
```

Sample Model Statement

```
model core_mod core len=7.7 area=0.85 br=1e3 bm=5e3 hc_t1=0.2 p1_f1=2.08 f1=10e3
p2_f2=50 f2=100K bflux=1e3 density=4.75
```

Instance Syntax

```
Name  [1]  [2] ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

area	(cm^2)	Effective magnetic cross-sectional area of core.
len	(cm)	Effective length of magnetic path.
id	(cm)	Inner diameter of toroidal core.
od	(cm)	Outer diameter of toroidal core.
gap	(cm)	Gap length.
m	1	Multiplicity factor.

Model Syntax

```
model modelName core parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`br`	`1 gauss`	Residual flux density.
`bm`	`1 gauss`	Saturation flux density.
`hc`	`1 oersteds`	Coercive magnetizing force (value of H where B equals 0).
`area`	`1 cm`^{2}	Effective magnetic cross-sectional area of core.
`len`	`1 cm`	Effective length of magnetic path.
`id`	`(cm)`	Inner diameter of toroidal core.
`od`	`(cm)`	Outer diameter of toroidal core.
`gap`	`0.0 cm`	Gap length.

Initial Conditions

`b0`	`(gauss)`	Initial condition for core.

Frequency Loss Parameters

`freq`	`(Hz)`	Core operating frequency.
`p1_f1`	`(W/Kg)`	Core power loss at frequency `f1`.
`f1`	`(Hz)`	Reference frequency for power loss.
`p2_f2`	`(W/Kg)`	Core power loss at frequency `f2`.
`f2`	`(Hz)`	Reference frequency for power loss.

© 2023 Cadence Design Systems, Inc.

`bflux`	`(gauss)`	Reference flux density.
`density`	`(g/cm`^{3}`)`	Core density.

Temperature Effects Parameters

`temp`	`(C)`	Core operating temperature.
`bm_t1`	`(gauss)`	Saturated flux density `Bm` at `T1`.
`br_t1`	`(gauss)`	Residual flux density `Br` at `T1`.
`hc_t1`	`(oersteds)`	Coercive force `Hc` at `T1`.
`t1`	`(C)`	Reference temperature.

Related Topics

Two Terminal Inductor (inductor)

Mutual Inductor (mutual_inductor)

Winding for Magnetic Core (winding)

Linear Inductance, Reluctance, Resistance, and Capacitance Matrix (rlck_matrix)

Passive Components

Winding for Magnetic Core (winding)

Winding is used in conjunction with magnetic cores to model coils and transformers with hysteresis. Each winding must be associated with a single core, though a core may have any number of windings.

Winding connects terminals `t1` and `b1`. Current through the winding is computed.

© 2023 Cadence Design Systems, Inc.

This device is not supported within altergroup.

Sample Instance Statement

```
c1 (1 0) core_mod area=1.2 len=8.1 id=0.45 id=0.55 gap=0.25
y1 (2 0) winding turn=5 core=c1 resis=1m
```

Instance Syntax

```
Name  t  b winding parameter=value ...
```

Instance Parameters

`turn=1`	Number of turns on a winding.
`resis (Ω)`	Resistance of the winding.
`m=1`	Multiplicity factor.
`core`	Name of the core around which the winding is wrapped.

Initial Conditions

`ic=0.0 A`	Initial condition on the winding.

Related Topics

Two Terminal Inductor (inductor)

Magnetic Core with Hysteresis (core)

Mutual Inductor (mutual_inductor)

Linear Inductance, Reluctance, Resistance, and Capacitance Matrix (rlck_matrix)

Passive Components

© 2023 Cadence Design Systems, Inc.

Linear Inductance, Reluctance, Resistance, and Capacitance Matrix (rlck_matrix)

Matrix device allows to specify a set of coupled inductors, resistors and capacitors in a single device, as opposed to a netlist of individual two-terminal devices and pair couplings. Reluctance matrix can be given instead of inductance matrix.

This device is supported within altergroups.

Device equations can be formulated in terms of inductance matrix L, or reluctance matrix K, defined as inverse of L

Inductance form

$$Vp - Vn = R*I + L*ddt(I)$$

Reluctance form

$$K*Vp - K*Vn = K*R*I + ddt(I)$$

where R is resistance matrix, I - vector of branch currents, ddt - time differentiation operator, Vp and Vn are vectors of positive and negative terminal voltages.

Capacitance equations

$$Ip = I + Cp*ddt(Vp)$$

$$In = -I + Cn*ddt(Vn)$$

where Ip and In are vectors of terminal currents, Cp, Cn are capacitance matrices for positive and negative terminals.

Sample Instance Statement

```
l33 (p1 n1 p2 n2) rlck_matrix l=[1 1 10n 1 2 -1n 2 2 5n] r=[1 1 100m 2 2 50m]
```

Instance Syntax

```
Name  1  2 ... rlck_matrix parameter=value ...
```

Number of terminals is two times dimension of matrix. When capacitance matrix is given, additional terminal can be specified to provide a reference for diagonal capacitors.

© 2023 Cadence Design Systems, Inc.

Sparse format is used for matrix input. Each matrix element is preceded by its row and column indexes. All matrices should have the same dimensions. Matrices are symmetric, so that only upper or lower triangular elements should be specified. At least one of R, L, K matrices must be given. Either L, or K, but not both can be specified.

Instance Parameters

`l=[...] H`	Inductance matrix.
`r=[...] Ω`	Resistance matrix.
`k=[...] 1/H`	Reluctance matrix.
`c1=[...] F`	Capacitance matrix for positive terminals.
`c2=[...] F`	Capacitance matrix for negative terminals.
`ignore_coupling=no`	Ignore coupling elements in r, l, k, and c matrices. Possible values are `no` or `yes`.
`file`	rlck matrix data file name.
`m=1`	Multiplicity factor.

Matrix data file may have several sections - one for each matrix. Each section starts with keyword: inductance (l), reluctance (k), resistance (r), capacitance1 (c1), capacitance2 (c2). If the keyword is not given, the data is assumed to be reluctance matrix. Matrix data is in sparse format, same as on the instance statement. Character + in the first column, as well as =, [, and] are treated as blank space.

Related Topics

Two Terminal Inductor (inductor)

Mutual Inductor (mutual_inductor)

Magnetic Core with Hysteresis (core)

Winding for Magnetic Core (winding)

Passive Components

© 2023 Cadence Design Systems, Inc.

3

Parameters Common to All Devices

Click to view the details of the following parameters:

- Multiplication Factor (m)
- Scaling Factors (scale and scalem)
- imelt and imax
- SPICE Compatibility Flag (compatible)

© 2023 Cadence Design Systems, Inc.

Multiplication Factor (m)

The multiplication factor (`m`) puts `m` devices in parallel. `m` is an instance parameter and need not be an integer. All devices have the multiplication factor capability.

If you specify `m` in an instance statement, all currents and capacitances of that device are multiplied by `m`, and all resistances are divided by `m`. The multiplication factor, however, does not affect short-channel or narrow-gate effects in MOSFETs. For example, the following two statements might not give you the same simulation results:

```
m1 d g s b my_model w=10u l=1u m=10
m1 d g s b my_model w=100u l=1u m=1
```

You can also specify the multiplication factor on subcircuits. If a multiplication factor is specified in a subcircuit, it applies to all elements in that subcircuit. For example, if the multiplication factor of the subcircuit is 2 and the multiplication factor of an element in the subcircuit is 3, the effective multiplication factor for that element is 6.

Some devices—such as BJT, JFET, and diode—have an area factor parameter (`area`). The `area` parameter has identical effect on devices as the multiplication factor.

Related Topics

Scaling Factors (scale and scalem)

imelt and imax

SPICE Compatibility Flag (compatible)

Parameters Common to All Devices

Scaling Factors (scale and scalem)

`scale` and `scalem` are options that set the scaling factors for instance and model parameters, respectively. You can specify the scaling factors in the `.options` statement. The following devices are affected by `scale` or `scalem`:

- Capacitors
- Diodes
- Resistors
- Physical resistors (`phy_res`)

© 2023 Cadence Design Systems, Inc.

- All levels of MOSFET models

These scaling factors affect capacitors, resistors, and physical resistors with specified device length (`l`) or width (`w`). `scale` and `scalem` are global options and apply to all instance and model statements for the preceding list of devices.

Parameters are scaled according to the following rules:

- Model (instance) parameters containing units of *m* (meters) are multiplied by `scalem` (`scale`).
- Model (instance) parameters containing units of m^n are multiplied by $\texttt{scalem}^n$ ($\texttt{scale}^n$), where *n* can be a positive integer or a positive real number.
- Model (instance) parameters containing units of 1/*m* are divided by `scalem` (`scale`).
- Model (instance) parameters containing units of $1/m^n$ are divided by $\texttt{scalem}^n$ ($\texttt{scale}^n$), where *n* can be a positive integer or a positive real number.
- Parameters that use the units *cm* (1/*cm*, cm^2, ...) and µ*m* (1/µ*m*, μm^2, ...) are not scaled. For example, `vmax`, which contains the unit *m*/*sec*, is scaled by `scalem`, but `ucrit`, which has the unit *V*/*cm*, is not scaled. Similarly, `nsub`, which has the unit $1/cm^3$, is not scaled by `scalem`.
- Parameters with other units are not scaled.

Note: The `diode` model is not scaled by default. To scale the `diode` model, set `allow_scaling` in the model card to `yes`.

Related Topics

Multiplication Factor (m)

imelt and imax

SPICE Compatibility Flag (compatible)

Parameters Common to All Devices

imelt and imax

`imelt` and `imax` are used on devices containing p-n junctions. These devices include

- JFETs

© 2023 Cadence Design Systems, Inc.

- GaAs FETs
- Physical resistors (`phy_res`)
- All MOSFET models
- Diodes
- All BJTs (G-P, VBIC, and HBT)

`imelt` is used to help convergence and to prevent numerical problems. The Spectre® circuit simulator uses `imelt` to linearize the junction current. When the junction current is larger than `imelt` (a model parameter), the junction current is calculated as a linear function instead of an exponential function of the junction voltage. Therefore, if the junction current is larger than `imelt`, the current calculated by the Spectre circuit simulator is not what the original junction current model predicts, and the Spectre circuit simulator issues a warning.

`imax` is a warning control parameter. Normally, `imax` does not affect the simulation results. Whenever the junction current is larger than `imax`, the Spectre circuit simulator issues a warning. The default value of `imax` is `1A`, and the default value of `imelt` is `imax`. Therefore, `imax` can affect the simulation results only when `imelt` is not specified and takes its value from `imax`.

Typically, the junction current is much less than 1 A. When `imelt` is `1A`, the conductance of the junction at room temperature is about 40 siemens, which is much larger than those of typical semiconductor devices. The Spectre circuit simulator issues a warning message telling you the junction current is linearized when

- The `imelt` value is set too small
- The connection to devices is incorrect
- Temporary voltage overshoot due to capacitive coupling at fast transient transition

  If this happens, the warnings can be ignored in most cases unless the voltage overshoot is purposely designed to trigger some circuit functions.

`imelt` and `imax` have current density counterparts, `jmelt` and `jmax`, which can be specified if you want the absolute current values to depend on the device area.

If the `is` parameter is not specified, its value is calculated as `area*js`, and `imax` and `imelt` values will also be calculated as `area*jmax` and `area*jmelt`. In this condition, values of `imax` and `imelt` given in the model card will have no effect.

In MOSFETs, you can use `jmelt` instead of `imelt`. The function of `jmelt` is identical to that of `imelt`, except that the junction current is linearized based on the current density specified by `jmelt`. If both `imelt` and `jmelt` are specified, `imelt` takes precedence.

© 2023 Cadence Design Systems, Inc.

For BJTs, `imelt` and `imax` are used to control the base-emitter and the substrate junctions. `imelt1` and `imax1` are used to control the base-collector junction.

Related Topics

Scaling Factors (scale and scalem)

Multiplication Factor (m)

SPICE Compatibility Flag (compatible)

Parameters Common to All Devices

SPICE Compatibility Flag (compatible)

The SPICE compatibility flag (`compatible`) is a parameter you can specify in an `.options` statement. This parameter solves some SPICE compatibility issues. The valid values for `compatible` are `spectre`, `spice2`, `spice3`, and `cdsspice`. This parameter affects two areas:

- Energy band gap

  If you set `compatible` to `spectre`, the Spectre simulator uses a more physics-based temperature equation to calculate the energy band gap. For all other values, the Spectre simulator uses the SPICE temperature equation. This different energy gap calculation affects only devices that use the common junction codes such as MOSFET, diode, JFET, and GaAs. BJT is not affected.

- MOSFET Level-2

  The MOSFET Level-2 model includes a model parameter `smooth`, which chooses an improved (smoother and faster) model (`smooth = yes`) or the original SPICE Level-2 model (`smooth = no`). The default value of `smooth` is `yes`. If `compatible` is set to a value other than `spectre`, the Spectre simulator sets `smooth` to `no` regardless of the value you specify.

Related Topics

Scaling Factors (scale and scalem)

imelt and imax

Multiplication Factor (m)

© 2023 Cadence Design Systems, Inc.

Parameters Common to All Devices

© 2023 Cadence Design Systems, Inc.

4

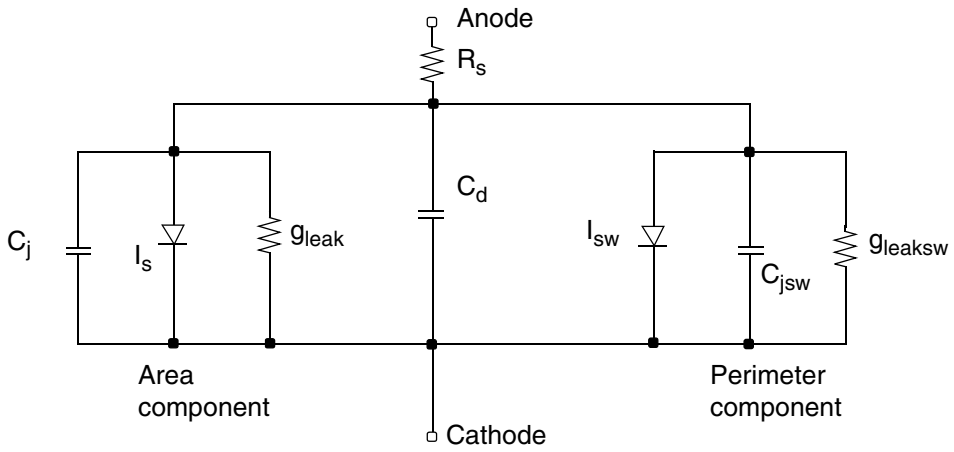
Diode Model (diode)

The DIODE level-1 model is based on the junction (Berkeley-spice) model and the level-2 model is based on the Fowler-Nordheim model. Click to view the following details about the DIODE model:

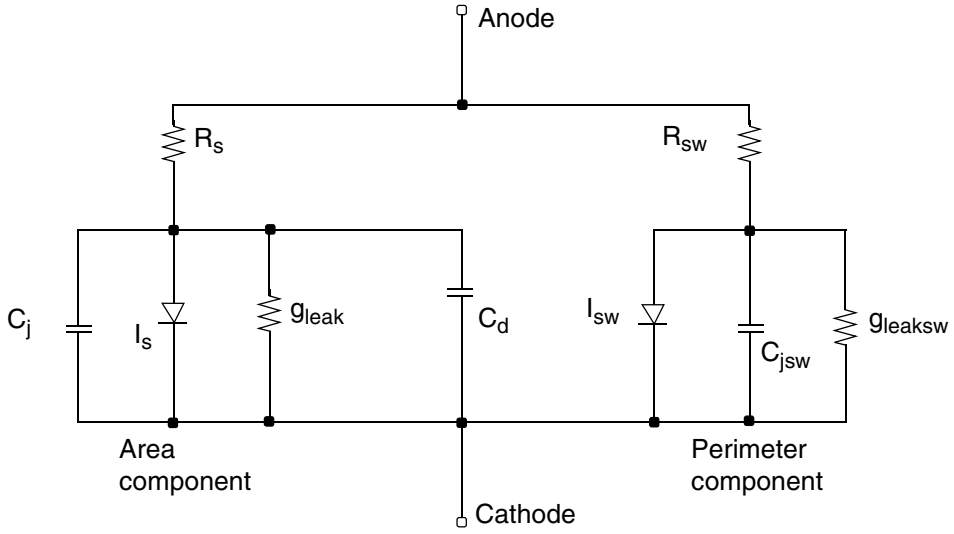
- Level-1 Model
- Noise Model
- Level-2 Model
- Level-3 Model
- Component Statements

© 2023 Cadence Design Systems, Inc.

If R_{sw} is not given, the diode model schematic is given by



If R_{sw} is given, the diode model schematic is given by



Device Regions

This section describes device regions for the Diode model.

The device region is	If

© 2023 Cadence Design Systems, Inc.

`Breakdown`	bvj is given and Vd<= -bvj
	ZenerV is given and Vd <= -ZenerV
`OFF`	Vd <= -10kT/q
`ON`	Vd > -10kT/q

Level-1 Model

The following effects are included in the junction diode model: forward characteristics, reverse leakage current, breakdown, parasitic resistance, diffusion capacitance, depletion capacitance, and overlap capacitance.

To achieve better scaling, a sidewall (peripheral) diode can also be specified. The peripheral diode shares most model parameters with the main diode except for the following parameters: `isw`, `ns`, `cjsw`, `mjsw`, `fcsw`, `rsw`, `gleaksw`, `ctp`, and `ptp`. If the sidewall parasitic resistance (`rsw`) is not specified, the peripheral diode shares the same parasitic resistance with the main diode. That is, both the main and the peripheral diodes are connected to the same internal nodes. If `rsw` is specified, the peripheral diode creates its own internal node. In this case, the peripheral and main diode are equivalent to connecting two diodes in parallel.

The leakage currents are modeled by putting two small conductances (`gleak` and `gleaksw`) in parallel with the intrinsic diodes.

DC Current

$$I_{jtot} = I_j + I_{jsw}$$

where V_t is the thermal voltage given by

$$V_t = \frac{kT}{q}$$

$$I_j = \begin{cases} is\left(e^{\frac{V}{nV_t}} - 1\right) & \text{if } V \le V_{Expl} \\ I_{offset} + G_{Expl}V & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$V_{Expl} = nV_t \ln\left[1 + \frac{imelt}{is}\right]$$

is the forward explosion voltage,

$$G_{Expl} = \frac{(imelt + is)}{nV_t}$$

is the conductance at V_{Expl}, and

$$I_{offset} = imelt - V_{Expl} G_{Expl}$$

is the current linearly extrapolated to $V = 0$ from V_{Expl}.

$$Ij+ = -JTUNeff \times \left(e^{\frac{-vd}{NTUN \times vt}} - 1 \right)$$

If I_j>0 and I_k>0,

$$I_j = I_j / (1 + \sqrt{I_j / (I_k \times Area)})$$

$$I_{jsw} = \begin{cases} isw\left(e^{\frac{V}{n_s V_t}} - 1 \right) & \text{if } V \le V_{Explsw} \\ I_{offsetsw} + G_{Explsw} V & \text{otherwise} \end{cases}$$

$$V_{Explsw} = n_s V_t \ln\left[1 + \frac{imelt}{is}\right]$$

$$G_{Explsw} = \frac{(imelt + isw)}{n_s V_t}$$

$$I_{offsetsw} = imelt - V_{Explsw} G_{Explsw}$$

If I_{jsw}>0 and I_{kp}>0,

© 2023 Cadence Design Systems, Inc.

$$I_{jsw} = I_{jsw} / (1 + \sqrt{I_{jsw} / (I_{kp} \times AreaSW)})$$

Junction Capacitance

$$C_j(V) = \begin{cases} \dfrac{cjo}{\left[1 - \dfrac{V}{vj}\right]^m} & \text{if } V \le fc * vj \\ \dfrac{cjo}{(1-fc)^m}\left[1 + \dfrac{m(V - vj*fc)}{vj(1-fc)}\right] & \text{otherwise} \end{cases}$$

Peripheral Junction Capacitance

$$C_{jsw}(V) = \begin{cases} \dfrac{cjsw}{\left[1 - \dfrac{V}{vjsw}\right]^{mjsw}} & \text{if } V \le fcsw * vjsw \\ \dfrac{cjsw}{(1-fcsw)^{mjsw}}\left[1 + \dfrac{mjsw(V - vjsw*fcsw)}{vjsw(1-fcsw)}\right] & \text{otherwise} \end{cases}$$

Diffusion Capacitance

$$C_{diff} = \frac{tt[I_j + is]}{nV_t} + \frac{tt[I_{jsw} + isw]}{n_s V_t}$$

Total Capacitance

$$C_{tot} = C_j + C_{jsw} + C_{diff} + C_d$$

© 2023 Cadence Design Systems, Inc.

Breakdown Current

$$I_{zener} = \begin{cases} -ibv \exp\left[-\frac{(V+bv)}{n_z V_t}\right] & \text{if } -(bv + V_{ZenerExpl}) \le V \\ -[I_{ZenerOffset} - G_{ZenerExpl}(V+bv)] & \text{otherwise} \end{cases}$$

where

$$V_{ZenerExpl} = n_z V_t \ln\left[\frac{imelt}{ibv}\right]$$

is the zener explosion voltage,

$$G_{ZenerExpl} = \frac{(imelt + ibv)}{n_z V_t}$$

is the conductance at $V_{ZenerExpl}$,

and

$$I_{ZenerOffset} = imelt - V_{ZenerExpl} G_{ZenerExpl}$$

is the current linearly extrapolated to $V = 0$ from $V_{ZenerExpl}$. The breakdown current is not modeled in the peripheral diode.

© 2023 Cadence Design Systems, Inc.

Temperature Effect

Energy Band Gap

$$E_g(T) = \begin{cases} eg - \dfrac{gap1 * T^2}{T + gap2} & \text{if } tlev = 2 \\ \left(1.17 - \dfrac{4.73 \times 10^{-4} T^2}{T + 636}\right) & \text{if } tlev = 0 \text{ or } 1 \text{ and } compatible{=}spectre \\ \left(1.16 - \dfrac{7.02 \times 10^{-4} T^2}{T + 1108}\right) & \text{otherwise} \end{cases}$$

Junction Currents

$$is = \begin{cases} is_{nom}\left(\dfrac{T}{Tnom}\right)^{\frac{xti}{n}} \exp\left[\dfrac{eg}{nV_{t,\,nom}} - \dfrac{eg}{nV_t}\right] & \text{if } tlev = 0 \text{ or } 1 \text{ and } eg \text{ is given, or } compatible{\neq}spectre \\ is_{nom}\left(\dfrac{T}{Tnom}\right)^{\frac{xti}{n}} \exp\left[\dfrac{E_g(Tnom)}{nV_{t,\,nom}} - \dfrac{E_g(T)}{nV_t}\right] & \text{if } tlev = 2 \text{ or } eg \text{ is not given} \end{cases}$$

Note: in the above equation, when eg is not specified, the default band gap is temperature dependent as specified by $E_g(T)$. The temperature dependence can be turned off by specifying eg in the model card or by setting the option *compatible* to something other than Spectre® circuit simulator (for example *compatible = spice*).

© 2023 Cadence Design Systems, Inc.

$$isw = \begin{cases} isw_{nom}\left(\frac{T}{Tnom}\right)^{\frac{xti}{n_s}} \exp\left[\frac{eg}{V_{t,\,nom}} - \frac{eg}{V_t}\right] & \text{if } tlev = 0 \text{ or } 1 \\ isw_{nom}\left(\frac{T}{Tnom}\right)^{\frac{xti}{n_s}} \exp\left[\frac{E_g(Tnom)}{V_{t,\,nom}} - \frac{E_g(T)}{V_t}\right] & \text{if } tlev = 2 \end{cases}$$

Breakdown Voltage

$$bv = bv_{nom}(1 + tbv*\Delta T + tbv2*\Delta T^2)$$

Parasitic Resistance

$$rs = rs_{nom}(1 + trs*\Delta T + trs2*\Delta T^2)$$

$$rsw = rsw_{nom}(1 + trs*\Delta T + trs2*\Delta T^2)$$

Leakage Conductance

$$gleak = gleak_{nom}(1 + tgs*\Delta T + tgs2*\Delta T^2)$$

$$gleaksw = gleaksw_{nom}(1 + tgs*\Delta T + tgs2*\Delta T^2)$$

© 2023 Cadence Design Systems, Inc.

Junction Potential

$$vj = \begin{cases} vj_{nom}\left(\frac{T}{Tnom}\right) - \Delta V_j & \text{if } tlevc = 0 \\ vj_{nom} - pta\Delta T & \text{if } tlevc = 1 \text{ or } 2 \\ vj_{nom} - \frac{dV_j}{dT}\Delta T & \text{if } tlevc = 3 \end{cases}$$

$$vjsw = \begin{cases} vjsw_{nom}\left(\frac{T}{Tnom}\right) - \Delta V_j & \text{if } tlevc = 0 \\ vjsw_{nom} - ptp\Delta T & \text{if } tlevc = 1 \text{ or } 2 \\ vjsw_{nom} - \frac{dV_{jsw}}{dT}\Delta T & \text{if } tlevc = 3 \end{cases}$$

where

$$\Delta V_j = V_t\left[3\ln\left(\frac{T}{Tnom}\right) + \frac{E_g(Tnom)}{V_{t,\,nom}} - \frac{E_g(T)}{V_t}\right]$$

$$\frac{dV_j}{dT} = \begin{cases} \frac{\left[E_g(Tnom) + 3V_{t,\,nom} + (1.16 - E_g(Tnom))\left(2 - \frac{Tnom}{Tnom + 1108}\right) - vj\right]}{Tnom} \\ \frac{\left[E_g(Tnom) + 3V_{t,\,nom} + (eg - E_g(Tnom))\left(2 - \frac{Tnom}{Tnom + gap2}\right) - vj\right]}{Tnom} \end{cases}$$

$$\frac{dV_{jsw}}{dT} = \begin{cases} \frac{\left[E_g(Tnom) + 3V_{t,\,nom} + (1.16 - E_g(Tnom))\left(2 - \frac{Tnom}{Tnom + 1108}\right) - vjsw\right]}{Tnom} & \text{if } tlev = 0, 1 \\ \frac{\left[E_g(Tnom) + 3V_{t,\,nom} + (eg - E_g(Tnom))\left(2 - \frac{Tnom}{Tnom + gap2}\right) - vjsw\right]}{Tnom} & \text{if } tlev = 2 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Junction Capacitance

$$cjo = \begin{cases} cjo_{nom}\left[1 + m\left(0.0004\Delta T - \frac{vj}{vj_{nom}} + 1\right)\right] & \text{if } tlevc = 0 \\ cjo_{nom}(1 + cta\Delta T) & \text{if } tlevc = 1 \\ cjo_{nom}\left(\frac{vj_{nom}}{vj}\right)^{m} & \text{if } tlevc = 2 \\ cjo_{nom}\left(1 - 0.5\frac{dV_j}{dT}\frac{\Delta T}{vj_{nom}}\right) & \text{if } tlevc = 3 \end{cases}$$

$$cjsw = \begin{cases} cjsw_{nom}\left[1 + m\left(0.0004\Delta T - \frac{vjsw}{vjsw_{nom}} + 1\right)\right] & \text{if } tlevc = 0 \\ cjsw_{nom}(1 + ctp\Delta T) & \text{if } tlevc = 1 \\ cjsw_{nom}\left(\frac{vjsw_{nom}}{vjsw}\right)^{mjsw} & \text{if } tlevc = 2 \\ cjsw_{nom}\left(1 - 0.5\frac{dV_{jsw}}{dT}\frac{\Delta T}{vjsw_{nom}}\right) & \text{if } tlevc = 3 \end{cases}$$

Related Topics

Noise Model

Level-2 Model

Level-3 Model

Component Statements

Diode Model (diode)

© 2023 Cadence Design Systems, Inc.

Noise Model

Series Resistance Thermal Noise

$$\overline{i_{R_s}^2} = \frac{4kT}{rs}\Delta f$$

Diode Shot and Flicker Noise

$$\overline{i_D^2} = 2qI_D\Delta f + kf\frac{I_D^{af}}{f}\Delta f$$

where kf and af are constants for a given device. The Spectre® circuit simulator defaults for these constants are 0.0 and 1.0, respectively.

Scaling Effects

The following are the Spectre scaling effects:

- is, cjo, cd, and ibv are multiplied by $area$ and m.
- rs is divided by $area$ and m.
- All noises are multiplied by $area$ and m.
- isw and $cjsw$ are multiplied by $perim$ and m for the peripheral diode.
- rsw is divided by $perim$ and m.
- If $area$ is not specified and l and w are specified, $area$ is calculated from l and w as

  $$area = L_{eff} \times W_{eff}$$

  where

  $$W_{eff} = w - etch$$

  $$L_{eff} = l - etchl$$

  If $area$, w, and l are not specified on the instance line, and $area$ is specified on the model card, then $area = area_{model}$.

© 2023 Cadence Design Systems, Inc.

Otherwise, $area$ defaults to 1.

- If $perim$ is not specified and l and w are specified, $perim$ is calculated from l and w as

  $$perim = 2 \times (L_{eff} + W_{eff})$$

  If $perim$, l, and w are not specified on the instance line, and $perim$ is specified on the model card, then $perim = perim_{model}$.

  Otherwise, $perim$ defaults to 0.

  The model parameter $allow_scaling$ controls scaling of diode geometry parameters ($area$, $perim$, l, and w) by the scale option. If $allow_scaling$ is set to yes, then the l, w, and $perim$ device parameters are multiplied by $scale$, while $area$ is multiplied by $scale^2$. By default, $allow_scaling$ is no.

  If $scale$ is specified on the diode instance line, then this value overrides the value of the scale option for this particular instance, although it is still only used if $allow_scaling$ is yes on the corresponding diode model card.

Related Topics

Level-1 Model

Level-2 Model

Level-3 Model

Component Statements

Diode Model (diode)

Level-2 Model

The level-2 diode model is used to model the Fowler-Nordheim tunneling current in thin insulators, such as silicon dioxide, commonly seen in nonvolatile memory. The peripheral diode is not supported for the level-2 model. If $perim$ is specified, it is ignored.

© 2023 Cadence Design Systems, Inc.

DC Current

$$I_j = \begin{cases} if\left(\frac{V^{nf}}{tox^2}\right) e^{\frac{-ecrf \times tox}{V}} & \text{if } V \geq 0 \\ ir\left(\frac{V^{nr}}{tox^2}\right) e^{\frac{ecrr \times tox}{V}} & \text{otherwise} \end{cases}$$

Linear Capacitance

$$C_d = cd + \frac{\varepsilon_{ox}}{tox}$$

Scaling Effects

The following are the Spectre scaling effects:

- if, ir, and cd are multiplied by $area$ and m.
- rs is divided by $area$ and m.
- If $area$ is not specified and l and w are specified, $area$ is calculated from l and w as follows:

  $$area = L_{eff} \times W_{eff}$$

  where

  $$W_{eff} = w - etch$$

  $$L_{eff} = l - etchl$$

  Otherwise, $area$ defaults to 1.

Related Topics

Noise Model

© 2023 Cadence Design Systems, Inc.

Level-2 Model

Level-3 Model

Component Statements

Diode Model (diode)

Level-3 Model

The level-3 model shares the level-1 model parameters. In addition, the level-3 model supports the following parameters: LM, LP, WM, XM, XP, XOI and XOM.

The poly metal capacitor is calculated by:

If xoi is given:

$$C_{poly} = (oxide \text{ permittivity} | xoi \times 1.0E-10) \times (wp + xp) \times (lp + xp)$$

otherwise,

$$C_{poly} = (oxide \text{ permittivity} | 7.0E) \times (wp + xp) \times (lp + xp)$$

The metal capacitor is calculated by:

If xom is given:

$$C_{metal} = (oxide \text{ permittivity} | xoi \times 1.0E-10) \times (wm + xm) \times (lm + xm)$$

otherwise,

$$C_{metal} = (oxide \text{ permittivity} | 1.0E6) \times (wm + xm) \times (lm + xm)$$

Related Topics

Level-1 Model

Noise Model

Level-2 Model

© 2023 Cadence Design Systems, Inc.

Component Statements

Diode Model (diode)

Component Statements

The junction diode model includes nonlinear junction capacitance and reverse breakdown.

This device is supported within altergroups.

Sample Instance Statement

```
d0 (dp dn) pdiode l=3e-4 w=2.5e-4 area=1
```

Sample Model Statement

```
model pdiode diode is=1.8e-5 rs=1.43 n=1.22 nz=2.31 gleak=6.2e-5 rsw=10 isw=6.1e-
10 ibv=0.95e-3 tgs=2 ik=1.2e7 fc=0.5 cj=1.43e-3 pb=0.967 mj=0.337 cjsw=2.76e-9
vjsw=0.94 jmax=1e20
```

Instance Definition

```
Name  a  c ModelName parameter=value ...
```

In forward operation, the voltage on the anode (a) is more positive than the voltage on the cathode (c).

© 2023 Cadence Design Systems, Inc.

Instance Parameters

area	Junction area factor (alias=lv1).
perim	Junction perimeter factor. pj is an alias of perim.
l=1e-6 m	Drawn length of junction.
w=1e-6 m	Drawn width of junction.
m=1	Multiplicity factor.
scale=1	Scale factor.
region=on	Estimated operating region. Spectre generates output number (0-2) in a rawfile. Possible values are off, on, and breakdown.
trise (C)	Temperature rise from ambient.
lm=0.0 m	Length of metal capacitor.
lp=0.0 m	Length of polysilicon capacitor.
wm=0.0 m	Width of metal capacitor.
wp=0.0 m	Width of polysilicon capacitor.
isnoisy=yes	Should device generate noise. Possible values are yes and no.

The instance parameter scale, if specified, overrides the value given by the option parameter scale. If the model parameter allow_scaling is set to yes, then, the area, perim, l, and w parameters are scaled by scale. By default, allow_scaling is set to no and no scaling of geometry parameters occurs. The values of area, perim, l, and w parameters printed by Spectre are those given in the input, and these values might not have the correct units if the scaling factors are not unity.

Model Definition

```
model modelName diode parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Model selector parameters

`level=1`	Model selector. 1 = Junction, 2 = Fowler-Nordheim, 3 = Junction + additional metal and polysilicon capacitances.
`dcap=2`	Depletion capacitance equations selector.
`bv_enable=1`	Flag to enable the breakdown of diode. 1=breakdown effect enabled, 0=breakdown effect disabled.
`compatible=spectre`	Spice compatibility flag. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, `tispice`, and `pspice`.

Process parameters

`etch=0 m`	Narrowing due to etching per side.
`etchl=0 m`	Length reduction due to etching per side.
`l=1e-6 m`	Drawn length of junction.
`w=1e-6 m`	Drawn width of junction.

Junction diode parameters

`js=1e-14 A/Area`	Saturation current.
`is=`jsA'`	Alias to `js`.
`jsw=0 A/Perim`	Sidewall saturation current.
`isw=`jswA'`	Alias to `jsw`.
`isp=`jswA'`	Alias to `jsw`.
`n=1`	Emission coefficient.
`ns=1`	Sidewall emission coefficient.
`ik=0.0 A/Area`	High-level injection knee current, alias to ikf.
`ikf=0.0 A/Area`	High-level injection knee current, alias to ik.
`ikp=`ikA/Area'`	High-level injection knee current for sidewall.

© 2023 Cadence Design Systems, Inc.

`ikr=0.0 A/Area`	Reverse high-level injection knee current.
`area=1`	Junction area factor.
`perim=0`	Junction perimeter factor.
`allow_scaling=no`	Allow scale option and instance scale parameter to affect diode instance geometry parameters. Possible values are `yes` and `no`.

Capacitive parameters

`tt=0 s`	Transit time.
`cd=0 F/Area`	Linear capacitance.
`cjo=0 F/Area`	Zero-bias junction capacitance.
`vj=1 V`	Junction potential.
`pb=`vjV'`	Alias to 'vj'.
`m=0.5`	Grading coefficient.
`cjsw=0 F/Perim`	Zero-bias sidewall junction capacitance.
`cjp=`cjswF'`	Alias to `cjsw`.
`vjsw=1 V`	Sidewall junction potential.
`php=`vjswV'`	Alias of `vjsw`.
`mjsw=0.33`	Sidewall grading coefficient.
`fc=0.5`	Forward-bias depletion capacitance threshold.
`fcs=`fc'`	Coefficient for forward-bias depletion sidewall capacitance.
`lm=0.0 m`	Length of metal capacitor (level=3 only).
`lp=0.0 m`	Length of polysilicon capacitor(level=3 only).
`wm=0.0 m`	Width of metal capacitor(level=3 only).
`wp=0.0 m`	Width of polysilicon capacitor(level=3 only).
`xm=0.0 m`	XM accounts for masking and etching effects (level=3 only).

© 2023 Cadence Design Systems, Inc.

`xp=0.0 m`	XP accounts for masking and etching effects (level=3 only).
`xoi=0.0 m`	Thickness of the polysilicon-to-bulk oxide. Units - nAngstram (level=3 only).
`xom=0.0 m`	Thickness of the metal-to-bulk oxide. Units - nAngstram (level=3 only).
`xw=0.0 m`	Accounts for masking and etching effects(level=3 only).
`vjmin=0.1`	Lowest value for built-in junction potential.

© 2023 Cadence Design Systems, Inc.

Breakdown parameters

`bv=infinity V`	Reverse breakdown voltage. Note: bv=0 is not the same as bv=infinity.
`vb=`bvV'`	Alias to `bv`.
`ibv=0.001 A/Area`	Current at breakdown voltage.
`nz=1`	Emission coefficient for Zener diode.
`bvj=infinity V`	Voltage at which junction breakdown warning is issued.
`isr=0` A/m^2	Recombination current parameter.
`ibvl=0` A/m^2	Low-level reverse breakdown current.
`nbv=1`	Reverse breakdown ideality factor.
`nbvl=1`	Reverse breakdown ideality factor.

Parasitic resistance parameters

`rs=0` Ω	Series resistance (/area).
`rsw=0` Ω	Sidewall series resistance (/perim).
`gleak=0 S`	Bottom junction leakage conductance (*area).
`gleaksw=0 S`	Sidewall junction leakage conductance (*perim).
`minr=0.1` Ω	Minimum series resistance.

Temperature effects parameters

`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eglev=0`	DC temperature selector.
`eg=1.11 V`	Band gap. **Note**: When bandgap is not specified, the default value is dependent on temperature. It is 1.11 at temp=27C.
`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.

© 2023 Cadence Design Systems, Inc.

`xti=3`	Saturation current temperature exponent.
`tbv1=0 1/C`	Linear temperature coefficient for `bv`.
`tcv=`tbv11/C'`	Linear temperature coefficient for `bv`.
`tbv2=0 C`$^{-2}$	Quadratic temperature coefficient for `bv`.
`tikf=0 1/C`	IKF temperature coefficient (linear).
`tnom (C)`	Parameter measurement temperature. The default value is set by the `options` statement.
`trise=0 C`	Temperature rise from ambient.
`trs=0 1/C`	Linear temperature coefficient for parasitic resistance.
`trs1=0 1/C`	Alias of trs.
`tmod=tnom C`	Model temperature.
`trs2=0 C`$^{-2}$	Quadratic temperature coefficient for parasitic resistance.
`tgs=0 1/C`	Linear temperature coefficient for leakage conductance.
`tgs2=0 C`$^{-2}$	Quadratic temperature coefficient for leakage conductance.
`cta=0 1/C`	Junction capacitance temperature coefficient.
`ctp=0 1/C`	Sidewall junction capacitance temperature coefficient.
`pta=0 V/C`	Junction potential temperature coefficient.
`ptp=0 V/C`	Sidewall junction potential temperature coefficient.
`ttt1=0.0 1/C`	First order temperature coefficient for tt.
`ttt2=0.0 C`$^{-2}$	Second order temperature coefficient for tt.
`tm1=0.0 1/C`	First order temperature coefficient for Mj.
`tm2=0.0 C`$^{-2}$	Second order temperature coefficient for Mj.

© 2023 Cadence Design Systems, Inc.

Junction diode model control parameters

`jmelt=1.0 A/Area`	Explosion current.
`imelt=`jmeltA'`	Alias to `jmelt`.
`expli=`jmeltA'`	Alias to `jmelt`.
`jmax=1 A/Area`	Maximum allowable current.
`imax=`jmaxA'`	Alias to `jmax`.
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`. Possible values are `yes` and `no`.

Fowler-Nordheim diode parameters

`if=1e-10 A/V^nf`	Forward Fowler-Nordheim current coefficient (*area).
`ir=`ifA/V^nr'`	Reverse Fowler-Nordheim current coefficient (*area).
`ecrf=2.55e10 V/m`	Forward critical field.
`ecrr=`ecrfV/m'`	Reverse critical field.
`ef=`ecrfV/m'`	Alias of `ecrf`.
`er=`ecrrV/m'`	Alias of `ecrr`.
`nf=2`	Forward voltage power.
`nr=`nf'`	Reverse voltage power.
`tox=1e-8 m`	Thickness of insulating layer.

TSMC Stand Alone model parameters

`rod=`rs'`Ω	Alias for Rs (Ohmic series resistance).
`jts=0 A/m`^{2}	Bottom trap-assisted saturation current density (with Level=1 and StAlone flag=1).
`jtssw=0 A/m`^{2}	Sidewall trap-assisted saturation current density (with Level=1 and StAlone flag=1).
`mrs=0.4`	Fitting parameter for Rseff (with Level=1 and StAlone flag=1).
`njts=60`	Non-ideality factor for Jts (with Level=1 and StAlone flag=1).

© 2023 Cadence Design Systems, Inc.

`njtssw=60`	Non-ideality factor for Jtssw (with Level=1 and StAlone flag=1).
`xts=0.055`	Power dependence of Jts on temperature (with Level=1 and StAlone flag=1).
`xtssw=0.055`	Power dependence of Jtssw on temperature (with Level=1 and StAlone flag=1).
`tnjts=0.15`	Temperature coefficient for Njts (with Level=1 and StAlone flag=1).
`tnjtssw=0.15`	Temperature coefficient for Njtssw (with Level=1 and StAlone flag=1).
`trod=0`	Temperature coefficient for Rod(Rs) (with Level=1 and StAlone flag=1).

© 2023 Cadence Design Systems, Inc.

Noise model parameters

`kf=0`	Flicker noise (1/f) coefficient.
`af=1`	Flicker noise (1/f) exponent.

Shrink Parameters

`shrink=1.0`	Shrink factor.
`shrink2=0.0`	Area shrink parameter.

Trap-assisted tunneling current parameters

`jtun=0 A`	Tunneling saturation current per area.
`jtunsw=0 A`	Sidewall tunneling saturation current per unit junction periphery.
`ntun=30`	Tunneling emission coefficient.
`xtitun=3.0`	Exponent for the tunneling current temperature.
`egtun=eg V`	Parameter for tunneling current at reverse region.

Safe Operating Areas Parameters

`bv_max=infinity V`	Maximum allowed voltage across two terminals.
`fv_max=infinity V`	Maximum allowed forward voltage across two terminals.
`keg=1.0 V`	The factor that is multiplied by EG to calculate the tunneling bandgap.
`gmin_m_scaling=no`	Allow gmin to be scaled by m or not. Possible values are `yes` and `no`.

Both of these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`bveff (V)`	Effective reverse breakdown voltage.
`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`region=on`	Estimated operating region. Spectre generates output number (0-2) in a rawfile. Possible values are `off`, `on`, and `breakdown`.
`region0`	Estimated operating region. Spectre outputs number (0-2) in a rawfile. Possible values are `off`, `on` and `breakdown`.
`v (V)`	Extrinsic diode voltage.
`i (A)`	Resistive diode current (alias=lx1).
`pwr (W)`	Power dissipation.
`res (Ω)`	Resistance of intrinsic diode.
`resp (Ω)`	Resistance of intrinsic sidewall diode.
`cap (F)`	Junction capacitance.
`capp (F)`	Sidewall junction capacitance.
`cd (F)`	Total junction capacitance (alias=lx5).
`ctotal (F)`	Total junction capacitance (alias=lx5).
`trise (C)`	Temperature rise from ambient.
`gd (S)`	Equivalent conductance (alias=lx2).
`qd (Coul)`	Charge of diode capacitor (alias=lx3).
`vdio (V)`	Voltage across diode (VD), excluding RS (alias=lx0).

Related Topics

Level-1 Model

© 2023 Cadence Design Systems, Inc.

Noise Model

Level-2 Model

Level-3 Model

Diode Model (diode)

© 2023 Cadence Design Systems, Inc.

5

BJT Model (bjt)

The BJT model is based on the Berkeley-Spice Gummel-Poon model. It defaults to the simpler Ebers-Moll model if certain parameters are left unspecified. This model also includes a substrate junction that connects either to the collector or to the base to model vertical and lateral structures.

Click to view the following information about the BJT model:

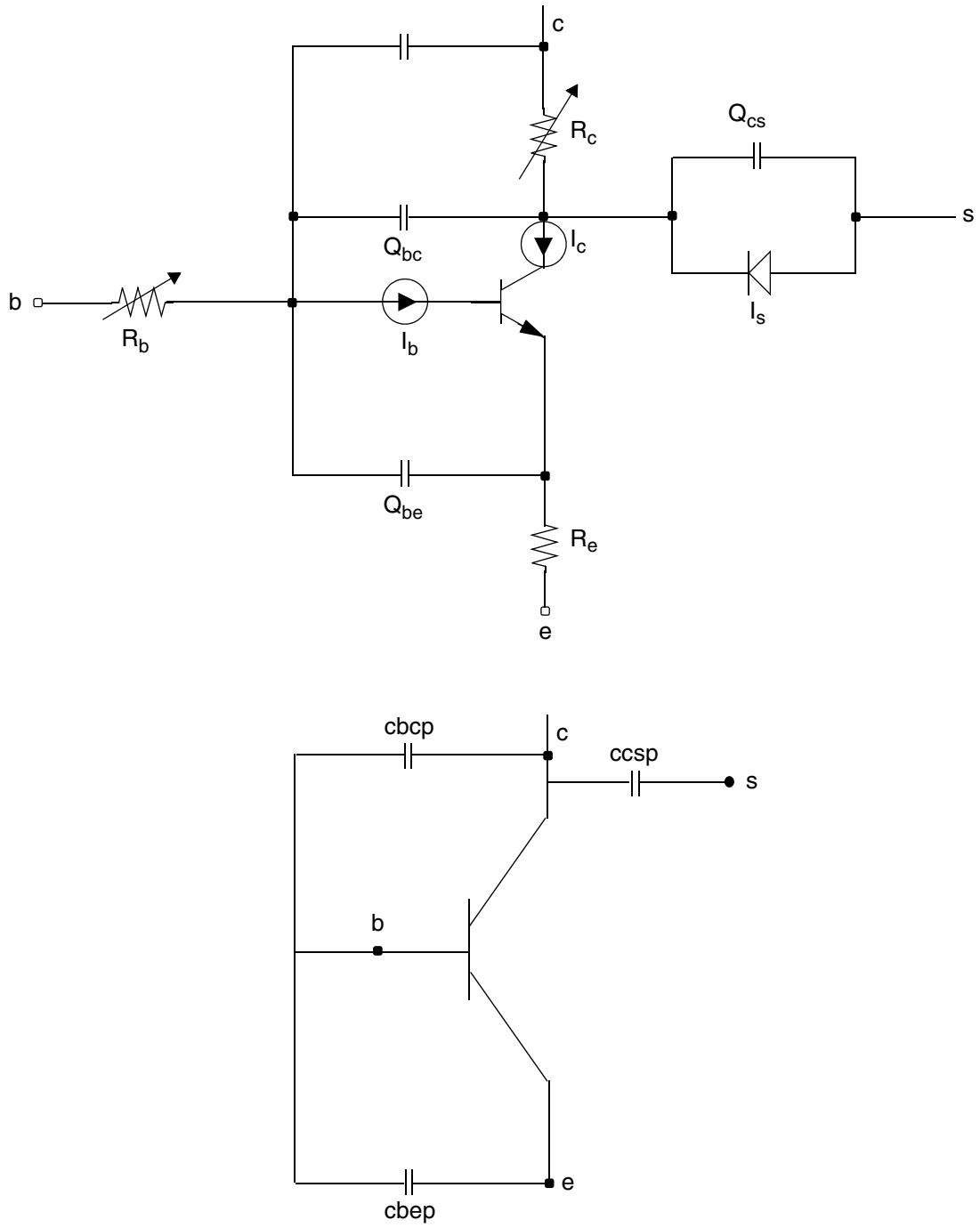
- Device Regions
- DC Current
- Nonlinear Base Resistance
- Nonlinear Collector Resistance (If rcv Is Specified)
- Collector Leakage Current
- Substrate Leakage Current
- Charge and Capacitance
- Excess Phase
- Temperature Effect
- Noise Model
- Scaling Effects

Note: When the Spectre® circuit simulator option `approx` is set to `yes`, `pow()` in the junction depletion capacitance calculation and `sqrt()` in the BJT and MOSFET level 1-5 models are replaced by a spline-function approximation. For more information, see `spectre -h options`.

© 2023 Cadence Design Systems, Inc.

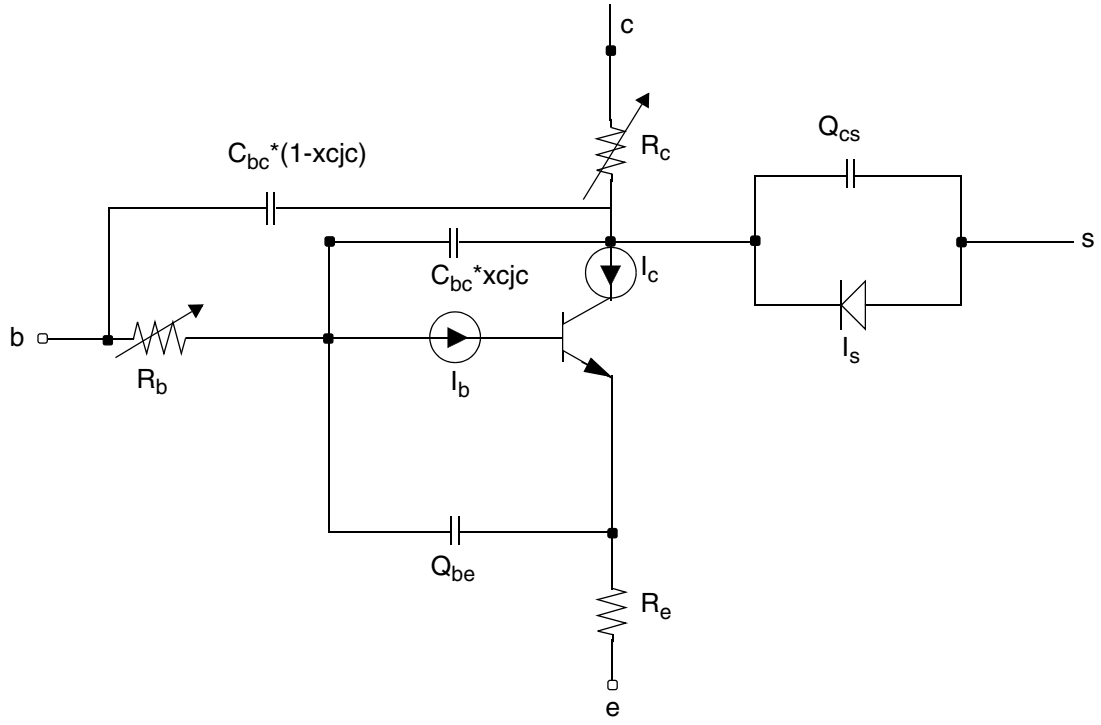
If `struct=vertical` (the default for NPN), the schematic of the model is given by one of the following figures:

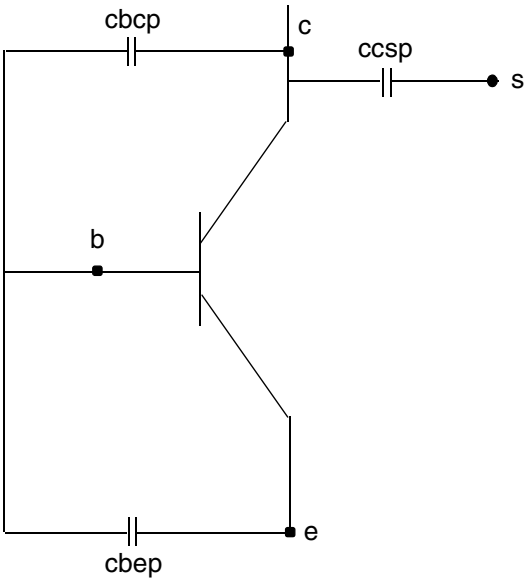
If Cbcsplit2 or Cbcsplit is not specified:



© 2023 Cadence Design Systems, Inc.

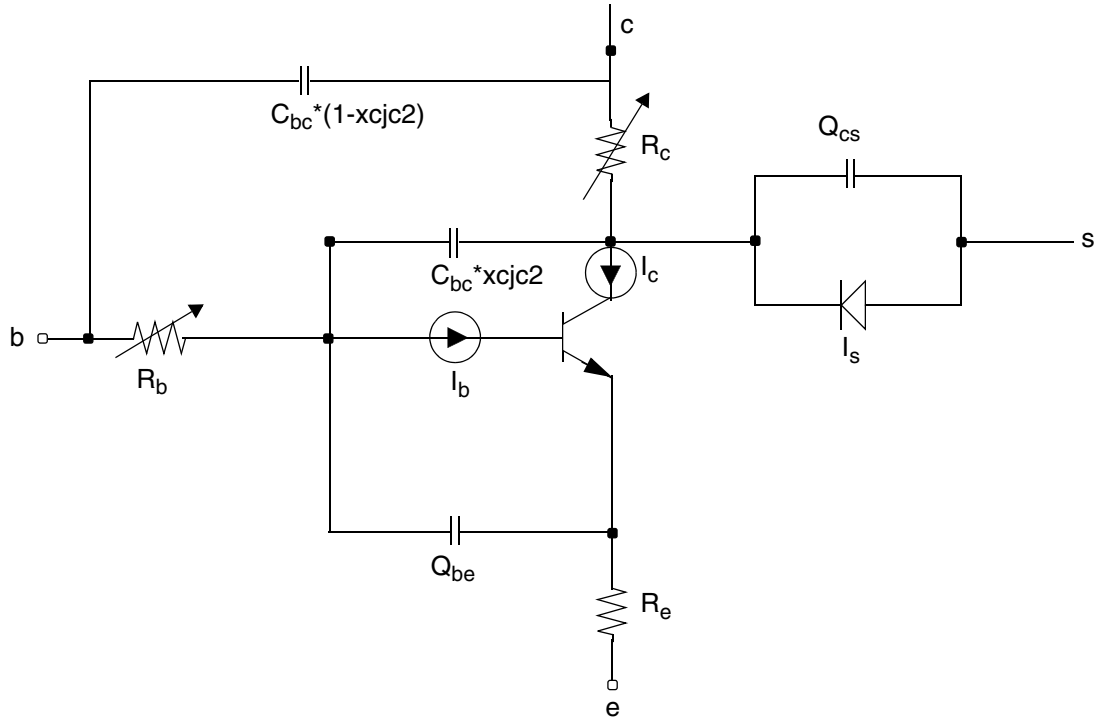
If Cbcsplit=xcjc:

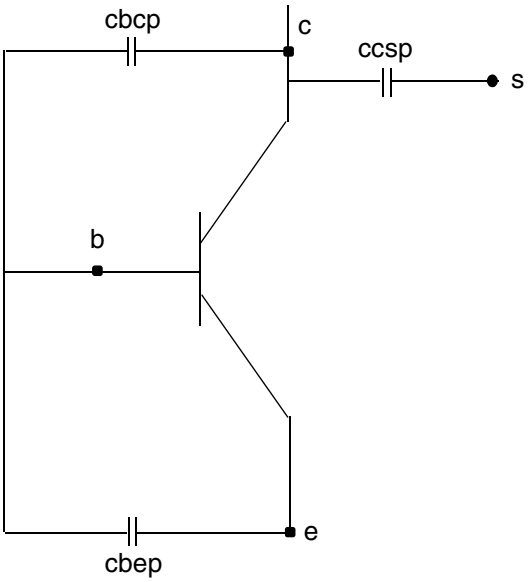




© 2023 Cadence Design Systems, Inc.

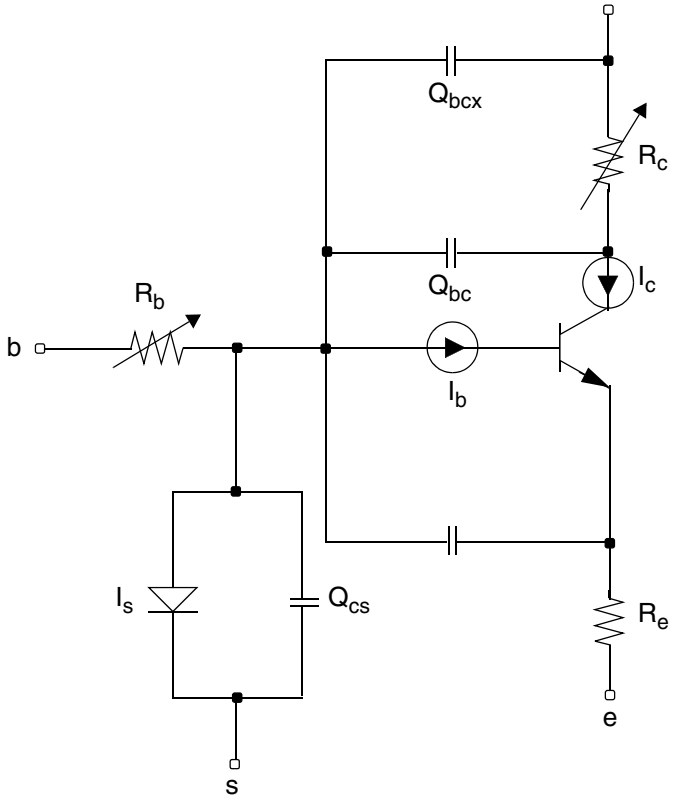
If Cbcsplit2=xcjc2

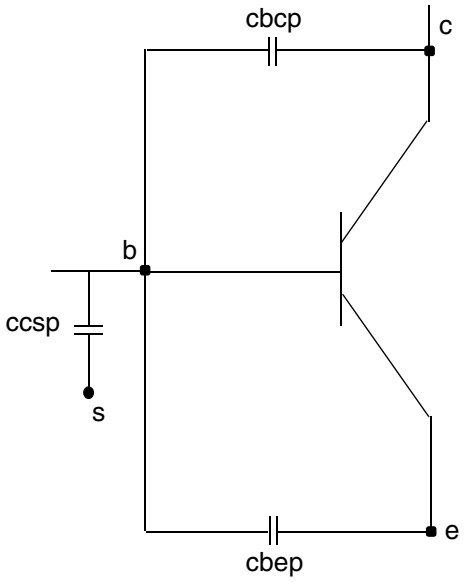




© 2023 Cadence Design Systems, Inc.

If `struct=lateral` (the default for PNP), the schematic of the model is given by





© 2023 Cadence Design Systems, Inc.

Device Regions

This section describes device regions for the BJT model.

The device region is	If
`breakdown`	■ bvsub is given and V_{CS} >= bvsub ■ bvbe is given and V_{BE} <= bvbe ■ bvce is given and V_{CE} >= bvce
`saturation`	V_{BE} > vbefwd and V_{BC} > vbcfwd
`reverse`	V_{BC} > vbcfwd and V_{BE} <= Vbefwd
`off`	none of the above conditions are true

Related Topics

DC Current

Collector Leakage Current

Substrate Leakage Current

BJT Model (bjt)

DC Current

$$I_c = \frac{is}{Q_B}\left(e^{\frac{V_{BE}}{nfV_t}} - e^{\frac{V_{BC}}{nrV_t}}\right) - I_{CB}$$

$$I_b = \frac{is}{bf}\left(e^{\frac{V_{BE}}{nfV_t}} - 1\right) + ise\left(e^{\frac{V_{BE}}{neV_t}} - 1\right) + I_{CB}$$

where V_t is the thermal voltage given by

© 2023 Cadence Design Systems, Inc.

$$V_t = \frac{kT}{q}$$

$$I_{CB} = \frac{is}{br}\left(e^{\frac{V_{BC}}{nrV_t}} - 1\right) + isc\left(e^{\frac{V_{BC}}{ncV_t}} - 1\right)$$

The intact equation for QB and nkf is:

$$Q_B = \frac{Q_1}{2}(1 + (1 + 4Q_2)^{nkf})$$

When nkf=0.5, the QB equation is:

$$Q_B = \frac{Q_1}{2}(1 + \sqrt{1 + 4Q_2})$$

$$Q_1 = \begin{cases} \dfrac{1}{1 - \dfrac{V_{BC}}{vaf} - \dfrac{V_{BE}}{var}} & \text{if neither ke or kc is specified} \\ \left(1 + \displaystyle\int_0^{V_{BE}} f_{cj}(\text{ke, vje, mje})dv + \int_0^{V_{BC}} f_{cj}(\text{kc, vjc, mjc})dv\right) & \text{otherwise} \end{cases}$$

where f_{cj} is defined as follows:

$$f_{cj}(C, P, M) = \begin{cases} \dfrac{C}{\left(1 - \dfrac{v}{P}\right)^M} & \text{if v } \le \text{fc * P} \\ \dfrac{C}{(1 - fc)^{1+M}}\left[1 - fc(1 + M) + \dfrac{M}{P}v\right] & \text{otherwise} \end{cases}$$

$$Q_2 = \frac{is}{ikf}\left(e^{\frac{V_{BE}}{nfV_t}} - 1\right) + \frac{is}{ikr}\left(e^{\frac{V_{BC}}{nrV_t}} - 1\right)$$

If ise (isc) is not given and $C2$ ($C4$) is specified, ise (isc) is calculated from

© 2023 Cadence Design Systems, Inc.

$$ise = C2 \times is$$

$$isc = C4 \times is$$

Related Topics

Device Regions

Collector Leakage Current

Substrate Leakage Current

BJT Model (bjt)

Nonlinear Base Resistance

$$R_B = rbm + \frac{rb - rbm}{Q_B} \qquad \text{if irb is not given}$$

If *irb* is given and `rbmod = spice` or SPICE compatibility is required,

$$R_B = rbm + 3(rb - rbm)\frac{\tan(z) - z}{z\tan^2(z)}$$

where

$$z = \frac{-1 + \sqrt{1 + \frac{144 I_b}{irb\pi^2}}}{\frac{24}{\pi^2}\sqrt{\frac{I_b}{irb}}}$$

If *irb* is given and `rbmod = spectre`,

$$R_B = rbm + \frac{rb - rbm}{\sqrt{1 + 3\left(\frac{I_b}{irb}\right)^{0.852}}}$$

© 2023 Cadence Design Systems, Inc.

Nonlinear Collector Resistance (If rcv Is Specified)

$$R_C = rcv\left[1+\left(\frac{n_i}{dope}\right)^2\left(e^{\frac{V_{BC}}{V_t}}\right)\right]^{-1}\left[1+\left(\frac{I_c}{cco}\right)^{cex}\right]+rcm$$

Related Topics

DC Current

Collector Leakage Current

Substrate Leakage Current

BJT Model (bjt)

Collector Leakage Current

If vbo is specified, the collector leakage current I_{CB} for $V_{BC} \le 0$ is modeled by

$$I_{CB} = (-cbo + gboV_{BC})\left[1-e^{\frac{V_{BC}}{vbo}}\right]$$

Note: To make the transition at $V_{BC} = 0$ smooth, vbo must satisfy

$$\frac{cbo}{vbo} = \frac{is}{br}\left(\frac{1}{nrV_t}\right)+\frac{isc}{ncV_t} \quad .$$

Related Topics

Substrate Leakage Current

BJT Model (bjt)

© 2023 Cadence Design Systems, Inc.

Substrate Leakage Current

$$I_S = iss\left(e^{\frac{V_{SC}}{nsV_t}} - 1\right)$$

where V_{SC} is the substrate-to-collector voltage if `struct=vertical` or the base-to-substrate voltage if `struct=lateral`.

Related Topics

Collector Leakage Current

BJT Model (bjt)

Charge and Capacitance

$$Q_{be} = \frac{tfI_{Fwd}}{Q_B}\left\{1 + (xtf)e^{\frac{V_{BC}}{\sqrt{2}vtf}}\left[\frac{I_{Fwd}}{I_{Fwd} + itf}\right]^2\right\} + \int_0^{V_{BE}} f_{cj}(\text{cje, vje, mje})dv$$

where

$$I_{Fwd} = is\left(e^{\frac{V_{BE}}{nfV_t}} - 1\right)$$

Note: If `compatible()spectre`, the equation is as follows

$$Q_{be} = \frac{tfI_{Fwd}}{Q_B}\left\{1 + (xtf)e^{\frac{V_{BC}}{1.44vtf}}\left[\frac{I_{Fwd}}{I_{Fwd} + itf}\right]^2\right\} + \int_0^{V_{BE}} f_{cj}(\text{cje, vje, mje})dv$$

© 2023 Cadence Design Systems, Inc.

$$Q_{bc} = tr*is\left(e^{\frac{V_{BC}}{nrV_t}} - 1\right) + xcjc\int_0^{V_{BC}} f_{cj}\,(\text{cjc, vjc, mjc})dv$$

$$Q_{bcx} = (1 - xcjc)\int_0^{V_{BCX}} f_{cj}\,(\text{cjc, vjc, mjc})dv$$

$$Q_{cs} = \begin{cases} \int_0^{V_{CS}} f_{cj}\,(\text{cjs, vjs, mjs,})dv & \text{if } mjs \text{ is specified} \\ \text{cjs}V_{CS} & \text{otherwise} \end{cases}$$

Related Topics

Charge and Capacitance

BJT Model (bjt)

Excess Phase

In an actual device, the measured phase shift is often larger than the shift predicted by the lumped model. The excess-phase parameter *ptf* accounts for this extra phase shift at high frequencies. An all-pass, second-order Bessel function filter creates this extra phase shift. The frequency response of this filter is

$$\phi(s) = \frac{3\omega_0^2}{s^2 + 3\omega_0 s + 3\omega_0^2}$$

where

$$\omega_0 = \frac{180}{ptf \times tf \times \pi}$$

and the phase shift due to this filter is

$$\theta = \tan^{-1}(H)$$

© 2023 Cadence Design Systems, Inc.

$$H = \frac{3\omega\omega_0}{3\omega_0^2 - \omega^2}$$

The value of *ptf* is usually the excess phase shift of transconductance measured at frequency $f = 1/(2\pi tf)$. The value of *ptf* should not be less than zero. SPICE does not implement the actual Bessel filter, which requires two more internal nodes for each BJT device. Instead, SPICE uses second-order numerical integration in the device code. This approach sometimes causes convergence problems. However, to remain compatible with SPICE, the Spectre® circuit simulator follows the SPICE method.

Related Topics

Temperature Effect

Noise Model

Scaling Effects

BJT Model (bjt)

Temperature Effect

Energy Gap

For tlev=0, 1, or 3

$$E_{g,\,ref} = 1.16 - 7.02 \cdot 10^{-4} \cdot \frac{T_{nom}^2}{T_{nom} + 1108}$$

$$E_{g,\,t} = 1.16 - 7.02 \cdot 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$dV_{je}dT = -\frac{E_{g,\,ref} + 3V_{T,\,nom} + (1.16 - E_{g,\,ref})\left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - V_{je}}{T_{nom}}$$

© 2023 Cadence Design Systems, Inc.

$$dV_{jc}dT = -\frac{E_{g,ref} + 3V_{T,nom} + (1.16 - E_{g,ref})\left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - V_{jc}}{T_{nom}}$$

$$dV_{js}dT = -\frac{E_{g,ref} + 3V_{T,nom} + (1.16 - E_{g,ref})\left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - V_{js}}{T_{nom}}$$

For tlev=2

$$E_{g,ref} = E_g - Gap_1 \cdot \frac{T_{nom}^2}{T_{nom} + Gap_2}$$

$$E_g = E_g - Gap_1 \cdot \frac{T^2}{T + Gap_2}$$

$$dV_{je}dT = -\frac{E_{g,ref} + 3V_{T,nom} + (E_g - E_{g,ref})\left(2 - \frac{T_{nom}}{T_{nom} + Gap_2}\right) - V_{je}}{T_{nom}}$$

$$dV_{jc}dT = -\frac{E_{g,ref} + 3V_{T,nom} + (E_g - E_{g,ref})\left(2 - \frac{T_{nom}}{T_{nom} + Gap_2}\right) - V_{jc}}{T_{nom}}$$

$$dV_{js}dT = -\frac{E_{g,ref} + 3V_{T,nom} + (E_g - E_{g,ref})\left(2 - \frac{T_{nom}}{T_{nom} + Gap_2}\right) - V_{js}}{T_{nom}}$$

Saturation Current

For tlev=0 and tlev=2

© 2023 Cadence Design Systems, Inc.

$$I_{set} = \frac{I_{se}}{\left(\frac{T}{Tnom}\right)^{X_{TB}}} \cdot e^{LsT/Ne}$$

$$I_{sct} = \frac{I_{sc}}{\left(\frac{T}{Tnom}\right)^{X_{TB}}} \cdot e^{LsT/Nc}$$

$$I_{sst} = \frac{I_{ss}}{\left(\frac{T}{Tnom}\right)^{X_{TB}}} \cdot e^{LsT/Ns}$$

$$Ibet = Ibe \cdot e^{LsT/Nf}$$

$$Ibct = Ibc \cdot e^{LsT/Nr}$$

$$I_{sT} = I_s e^{L_{sT}}$$

For tlev=1

$$Iset = \frac{Ise}{1 + X_{TB} \cdot \Delta T} \cdot e^{LsT/Nc}$$

$$Isct = \frac{Isc}{1 + X_{TB} \cdot \Delta T} \cdot e^{LsT/N_c}$$

$$Isst = \frac{Iss}{1 + X_{TB} \cdot \Delta T} \cdot e^{LsT/Ns}$$

$$Ibet = Ibe \cdot e^{LsT/Nf}$$

$$Ibct = Ibc \cdot e^{LsT/Nr}$$

© 2023 Cadence Design Systems, Inc.

$$Ist = Is \cdot e^{LsT}$$

For tlev=3

$$Iset = Ise^{(1 + t_{ise1} \cdot \Delta T + t_{ise2} \cdot \Delta T^2)}$$

$$Isct = Isc^{(1 + t_{isc1} \cdot \Delta T + t_{isc2} \cdot \Delta T^2)}$$

$$Isst = Iss^{(1 + t_{iss1} \cdot \Delta T + t_{iss2} \cdot \Delta T^2)}$$

$$Ibet = Ibe^{(1 + t_{is1} \cdot \Delta T + t_{is2} \cdot \Delta T^2)}$$

$$Ibct = Ibc^{(1 + t_{is1} \cdot \Delta T + t_{is2} \cdot \Delta T^2)}$$

$$Ist = Is^{(1 + t_{is1} \cdot \Delta T + t_{is2} \cdot \Delta T^2)}$$

Parameters $\mathtt{I_{kf}}$, $\mathtt{I_{kr}}$, and $\mathtt{I_{rb}}$ are modified as follows.

For tlev=0, 1, or 2

$$I_{kfT} = I_{kf} \cdot (1 + t_{ikf1}\Delta T + t_{ikf2}\Delta T^2)$$

$$I_{krT} = I_{kr} \cdot (1 + t_{ikr1}\Delta T + t_{ikr2}\Delta T^2)$$

$$I_{rbT} = I_{rb} \cdot (1 + t_{irb1}\Delta T + t_{irb2}\Delta T^2)$$

For tlev=3

$$I_{kfT} = I_{kf}^{1 + t_{ikf1}\Delta T + t_{ikf2}\Delta T^2}$$

$$I_{krT} = I_{kr}^{1 + t_{ikr1}\Delta T + t_{ikr2}\Delta T^2}$$

© 2023 Cadence Design Systems, Inc.

$$I_{rbT} = I_{rb}^{1 + t_{irb1}\Delta T + t_{irb2}\Delta T^2}$$

Degree Factor

For tlev=0, 1, or 3

$$L_{sT} = \frac{Eg}{V_{Tnom}} - \frac{Eg}{V_T} + X_{TI} \cdot \ln\left(\frac{T}{Tnom}\right)$$

For tlev=2

$$LsT = \frac{Eg, ref}{V_{Tnom}} - \frac{Eg}{V_T} + X_{TI} \cdot \ln\left(\frac{T}{Tnom}\right)$$

Current Gains (B_f, B_r)

For tlev=0, 2, or 3

$$B_{fT} = B_f \cdot \left(\frac{T}{T_{nom}}\right)^{X_{TB}}$$

$$B_{rT} = B_r \cdot \left(\frac{T}{T_{nom}}\right)^{X_{TB}}$$

For tlev=1

$$B_{fT} = B_f \cdot (1 + X_{TB}\Delta T)$$

$$B_{rT} = B_r \cdot (1 + X_{TB}\Delta T)$$

If coefficients are specified,

$$B_f(T) = B_{fT} \cdot (1 + t_{Bf1}\Delta T + t_{Bf2}\Delta T^2)$$

© 2023 Cadence Design Systems, Inc.

$$B_r(T) = B_{rT} \cdot (1 + t_{Br1}\Delta T + t_{Br2}\Delta T^2)$$

$$V_{afT} = V_{af} \cdot (1 + t_{vaf1}\Delta T + t_{vaf2}\Delta T^2)$$

$$V_{arT} = V_{ar} \cdot (1 + t_{var1}\Delta T + t_{var2}\Delta T^2)$$

$$t_{fT} = t_f \cdot (1 + t_{tf1}\Delta T + t_{tf2}\Delta T^2)$$

$$t_{rT} = t_r \cdot (1 + t_{tr1}\Delta T + t_{tr2}\Delta T^2)$$

$$N_{fT} = N_f \cdot (1 + t_{nf1}\Delta T + t_{nf2}\Delta T^2)$$

$$N_{rT} = N_r \cdot (1 + t_{nr1}\Delta T + t_{nr2}\Delta T^2)$$

$$N_{eT} = N_e \cdot (1 + t_{ne1}\Delta T + t_{ne2}\Delta T^2)$$

$$N_{cT} = N_c \cdot (1 + t_{nc1}\Delta T + t_{nc2}\Delta T^2)$$

$$N_{sT} = N_s \cdot (1 + t_{ns1}\Delta T + t_{ns2}\Delta T^2)$$

$$M_{jeT} = M_{je} \cdot (1 + t_{mje1}\Delta T + t_{mje2}\Delta T^2)$$

$$M_{jcT} = M_{jc} \cdot (1 + t_{mjc1}\Delta T + t_{mjc2}\Delta T^2)$$

$$M_{jsT} = M_{js} \cdot (1 + t_{mjs1}\Delta T + t_{mjs2}\Delta T^2)$$

$$t_{dT} = t_d \cdot (1 + t_{tf1}\Delta T + t_{tf2}\Delta T^2)$$

© 2023 Cadence Design Systems, Inc.

$$I_{tfT} = I_{tf} \cdot (1 + t_{itf1}\Delta T + t_{itf2}\Delta T^2)$$

$$X_{tfT} = X_{tf} \cdot (1 + t_{xtf1}\Delta T + t_{xtf2}\Delta T^2)$$

$$V_{tfT} = V_{tf} \cdot (1 + t_{vtf1}\Delta T + t_{vtf2}\Delta T^2)$$

Junction Capacitors (cjc, cje, and cjs)

For tlevc=0

$$C_{jeT} = C_{je}\left[1 + M_{je} \cdot \left(400 \cdot 10^{-6}\Delta T + 1 - \frac{V_{jeT}}{V_{je}}\right)\right]$$

where

$$V_{jeT} = V_{je}\frac{T}{T_{nom}} - 3V_T \cdot \ln\frac{T}{T_{nom}} + E_{g,ref}\frac{T}{T_{nom}} - E_g$$

$$C_{jcT} = C_{jc}\left[1 + M_{jc} \cdot \left(400 \cdot 10^{-6}\Delta T + 1 - \frac{V_{jcT}}{V_{jc}}\right)\right]$$

where

$$V_{jcT} = V_{jc}\frac{T}{T_{nom}} - 3V_T \cdot \ln\frac{T}{T_{nom}} + E_{g,ref}\frac{T}{T_{nom}} - E_g$$

$$C_{jsT} = C_{js}\left[1 + M_{js} \cdot \left(400 \cdot 10^{-6}\Delta T + 1 - \frac{V_{jsT}}{V_{js}}\right)\right]$$

where

$$V_{jsT} = V_{js}\frac{T}{T_{nom}} - 3V_T \cdot \ln\frac{T}{T_{nom}} + E_{g,ref}\frac{T}{T_{nom}} - E_g$$

For tlevc=1

© 2023 Cadence Design Systems, Inc.

$$C_{jeT} = C_{je} \cdot (1 + C_{te}\Delta T)$$

where

$$V_{jeT} = V_{je} - t_{vje}\Delta T$$

$$C_{jcT} = C_{jc} \cdot (1 + C_{tc}\Delta T)$$

where

$$V_{jcT} = V_{jc} - t_{vjc}\Delta T$$

$$C_{jsT} = C_{js} \cdot (1 + C_{ts}\Delta T)$$

where

$$V_{jsT} = V_{js} - t_{vjs}\Delta T$$

For tlevc=2

$$C_{jeT} = C_{je} \cdot \left(\frac{V_{je}}{V_{jeT}}\right)^{M_{je}}$$

where

$$V_{jeT} = V_{je} - t_{vje}\Delta T$$

$$C_{jcT} = C_{jc} \cdot \left(\frac{V_{jc}}{V_{jcT}}\right)^{M_{jc}}$$

where

$$V_{jcT} = V_{jc} - t_{vjc}\Delta T$$

$$C_{jsT} = C_{js} \cdot \left(\frac{V_{js}}{V_{jsT}}\right)^{M_{js}}$$

where

© 2023 Cadence Design Systems, Inc.

$$V_{jsT} = V_{js} - t_{vjs}\Delta T$$

For tlevc=3

$$C_{jeT} = C_{je} \cdot \left(1 - 0.5 \cdot dV_{je}dT\frac{\Delta T}{V_{je}}\right)$$

where

$$V_{jeT} = V_{je} + dV_{je}dT\Delta T$$

$$C_{jcT} = C_{jc} \cdot \left(1 - 0.5 \cdot dV_{jc}dT\frac{\Delta T}{V_{jc}}\right)$$

where

$$V_{jcT} = V_{jc} + dV_{jc}dT\Delta T$$

$$C_{jsT} = C_{js} \cdot \left(1 - 0.5 \cdot dV_{js}dT\frac{\Delta T}{V_{js}}\right)$$

where

$$V_{jsT} = V_{js} + dV_{js}dT\Delta T$$

Parasitic Resistors (rb, rc, and re)

$$R_{eT} = R_e \cdot (1 + t_{re1}\Delta T + t_{re2}\Delta T^2)$$

$$R_{cT} = R_c \cdot (1 + t_{rc1}\Delta T + t_{rc2}\Delta T^2)$$

$$R_{sT} = R_s \cdot (1 + t_{rs1}\Delta T + t_{rs2}\Delta T^2)$$

$$R_{bmT} = R_{bm} \cdot (1 + t_{rm1}\Delta T + t_{rm2}\Delta T^2)$$

© 2023 Cadence Design Systems, Inc.

Related Topics

Excess Phase

Noise Model

Scaling Effects

BJT Model (bjt)

Noise Model

Base Resistance Thermal Noise

$$\overline{i_{R_B}^2} = \begin{cases} \frac{4kT}{R_B}\frac{rbnoi}{R_B}\Delta f & \text{if } rbnoi \text{ is specified} \\ \frac{4kt}{R_B}\Delta f & \text{otherwise} \end{cases}$$

Collector Resistance Thermal Noise

$$\overline{i_{R_C}^2} = \frac{4kT}{R_C}\Delta f$$

Emitter Resistance Thermal Noise

$$\overline{i_{R_E}^2} = \frac{4kT}{R_E}\Delta f$$

Collector Shot Noise Source

$$\overline{i_C^2} = 2qI_C\Delta f$$

© 2023 Cadence Design Systems, Inc.

Base Shot, Flicker, and Burst Noise Sources

$$\overline{i_B^2} = 2qI_B\Delta f + kf\frac{I_B^{af}}{f}\Delta f + kb\frac{I_B}{1+(f/f_c)^2}\Delta f$$

where kf, af, kb, and fc are constants for a given device. The Spectre defaults for these constants are 0.0, 1.0, 0.0, and 1.0 respectively.

Related Topics

Excess Phase

Temperature Effect

Scaling Effects

BJT Model (bjt)

Scaling Effects

This model has the following enhancements over SPICE2G.6:

1. Two base resistance models are provided.

2. Nonlinear collector resistance is implemented.

3. The integral form of the Early voltage effect is available.

4. The substrate junction includes both the diode and the capacitor.

This device is supported within altergroups.

Sample Instance Statement:

```
q1 (vcc net3 minus) npn_mod region=fwd area=1 m=1
```

Sample Model Statement:

```
model npn_mod bjt type=npn is=10e-13 bf=200 va=58.8 ikf=5.63e-3 rb=700 rbm=86
re=3.2 cje=0.352e-12 pe=0.76 me=0.34 tf=249e-12 cjc=0.34e-12 pc=0.55
```


© 2023 Cadence Design Systems, Inc.

Instance Definition

```
Name  c  b  e  [s] ModelName parameter=value ...
```

You do not have to specify the substrate terminal. If you do not specify it, the substrate is connected to ground.

Instance Parameters

`area=1`	Transistor area factor (alias=lv1).
`areab=1`	Transistor areab factor.
`areac=1`	Transistor areac factor.
`m=1`	Multiplicity factor.
`trise`	Temperature rise from ambient.
`region=fwd`	Estimated operating region. Spectre outputs a number (0-4) in a rawfile. Possible values are `off`, `fwd`, `rev`, `sat`, or `breakdown`.
`isnoisy=yes`	Should device generate noise. Possible values are `no` or `yes`.

Model Definition

```
model modelName bjt parameter=value ...
```

Model Parameters

© 2023 Cadence Design Systems, Inc.

Structural parameters

`type=npn`	Transistor type. Possible values are `npn` and `pnp`.
`struct=vertical`	Transistor structure. For pnp, the default is `lateral`. Possible values are `vertical` and `lateral`.
`subs=1`	Transistor structure. `1` for vertical structure and `-1` for lateral structure. For NPN, default = `1` and for PNP, default = `-1`.

Saturation current parameters

`is=1e-16 A`	Saturation current (*area).
`ise=0 A`	B-E leakage saturation current. Set to `c2*is` if not given. (*area). If ise is greater than or equal to 1e-4, ise will be multiplied by is.
`isc=0 A`	B-C leakage saturation current. Set to `c4*is` if not specified (*area). If isc is greater than or equal to 1e-4, isc will be multiplied by is.
`iss=0 A`	Substrate leakage saturation current (*area).
`c2=0`	Forward leakage saturation current coefficient.
`c4=0`	Reverse leakage saturation current coefficient.
`nkf=0.5`	Qb exponent parameter.
`nk=nkf`	Qb exponent parameter. It is an alias of nkf.

B-C leakage model parameters

`cbo=0 A`	Extrapolated 0-volt B-C leakage current (*area).
`gbo=0 S`	Slope of `Icbo` comapred to `Vbc` above `Vbo` (*area).
`vbo=0 V`	Slope of `Icbo` compared to `Vbc` at `Vbc`=0.
`tcbo=0 1/C`	Temperature coefficient for cbo.
`tgbo=0 1/C`	Temperature coefficient for gbo.

© 2023 Cadence Design Systems, Inc.

Emission coefficient parameters

`nf=1`	Forward emission coefficient.
`nr=1`	Reverse emission coefficient.
`ne=1.5`	B-E leakage emission coefficient.
`nc=2`	B-C leakage emission coefficient.
`ns=1`	Substrate junction emission coefficient.

Current gain parameters

`bf=100 A/A`	Forward current gain (`beta`).
`bfm (A/A)`	Forward current gain (`beta`).
`br=1 A/A`	Reverse current gain (`beta`).
`brm (A/A)`	Reverse current gain (`beta`).
`ikf=∞ A`	High current corner for forward `beta` (*area).
`ik=∞ A`	High current corner for forward `beta` (*area).
`jbf=∞ A`	High current corner for forward `beta` (*area).
`ikr=∞ A`	High current corner for reverse `beta` (*area).
`jbr (A)`	High current corner for reverse `beta` (*area).

Early voltage parameters

`vaf=∞ V`	Forward Early voltage.
`va=∞ V`	Forward Early voltage.
`var=∞ V`	Reverse Early voltage.
`vb=∞ V`	Reverse Early voltage.
`ke=0 1/V`	B-E space-charge integral multiplier.
`kc=0 1/V`	B-C space-charge integral multiplier.

Parasitic resistance parameters

`rb=0 Ω`	Zero-bias base resistance (/area).

© 2023 Cadence Design Systems, Inc.

`rbm=rb` Ω	Minimum base resistance for high currents (/area).
`irb=∞ A`	Current at base resistance midpoint (*area).
`jrb (A)`	Current at base resistance midpoint (*area).
`iob (A)`	Current at base resistance midpoint (*area).
`rbmod=spice`	Nonlinear `Rb` model. Possible values are `spectre` and `spice`.
`rc=0` Ω	Collector resistance (/area).
`rcv=0` Ω	Variable collector resistance (/area). It works only when its value is specified.
`rcm=0` Ω	Minimum collector resistance (/area).
`dope=1e15` cm^{-3}	Collector background doping concentration.
`cex=1`	Current crowding exponent.
`cco=1 A`	Current crowding normalization constant (*area).
`re=0` Ω	Emitter resistance (/area).
`minr=0.1` Ω	Minimum parasitic resistance.

© 2023 Cadence Design Systems, Inc.

Junction capacitance parameters

`dcap=2`	Depletion capacitance model selector.
`cje=0 F`	B-E zero-bias junction capacitance (*area).
`vje=0.75 V`	B-E built-in junction potential.
`mje=1/3`	B-E junction exponent.
`pe=0.75 V`	B-E built-in junction potential.
`me=1/3`	B-E junction exponent.
`cjc=0 F`	B-C zero-bias junction capacitance (*area).
`vjc=0.75 V`	B-C built-in junction potential.
`mjc=1/3`	B-C junction exponent.
`pc=0.75 V`	B-C built-in junction potential.
`mc=1/3`	B-C junction exponent.
`xcjc=1`	Fraction(xcjc) of B-C capacitance tied to internal base and internal collector. (1-xcjc)*(B-C capacitance) tied to external base and internal collector.
`xcjc2=1`	Fraction(xcjc2) of B-C capacitance tied to external base and external collector. (1-xcjc2)*(B-C capacitance) tied to external base and external collector.
`cjs=0 F`	B-S zero-bias junction capacitance (*area).
`ccs=0 F`	B-S zero-bias junction capacitance (*area).
`csub (F)`	B-S zero-bias junction capacitance (*area).
`vjs=0.75 V`	B-S built-in junction potential.
`mjs=0`	B-S junction exponent.
`ps=0.75 V`	B-S built-in junction potential.
`psub (V)`	B-S built-in junction potential.
`ms=0`	B-S junction exponent.
`esub`	B-S junction exponent.
`fc=0.5`	Junction capacitor forward-bias threshold.
`cbcp=0 F`	B-C parasitic capacitance.
`cbep=0 F`	B-E parasitic capacitance.

© 2023 Cadence Design Systems, Inc.

`ccsp=0 F`	C-S parasitic capacitance.

© 2023 Cadence Design Systems, Inc.

Transit time and excess phase parameters

`tf=0 s`	Ideal forward transit time.
`td=0 s`	Intrinsic base delay time.
`xtf=0`	Coefficient for bias dependence of `tf`.
`vtf=∞ V`	Voltage describing Vbc dependence of `tf`.
`itf=0 A`	High current parameter for effect on `tf` (*area).
`jtf (A)`	High current parameter for effect on `tf` (*area).
`tr=0 s`	Ideal reverse transit time.
`ptf=0 °`	Excess phase at freq = 1.0/(`tf`*2 pi) Hz.

Temperature effects parameters

`tnom (C)`	Measurement temperature for the parameter. The default value is set by using the `options` statement.
`tref (C)`	TNOMs alias.
`trise=0 C`	Temperature rise from ambient.
`eg=1.11 V`	Band-gap voltage.
`xtb=0`	`Beta` temperature exponent.
`xti=3`	Temperature exponent for effect on `is`.
`pt`	Temperature exponent for effect on `is`. It is an alias of `xti`.
`trb1=0 1/C`	Linear temperature coefficient for the base resistor.
`trb2=0` C^{-2}	Quadratic temperature coefficient for the base resistor.
`trm1=0 1/C`	Linear temperature coefficient for the minimum base resistor.
`trm2=0` C^{-2}	Quadratic temperature coefficient for the minimum base resistor.
`trc1=0 1/C`	Linear temperature coefficient for the collector resistor.
`trc2=0` C^{-2}	Quadratic temperature coefficient for the collector resistor.
`tre1=0 1/C`	Linear temperature coefficient for the emitter resistor.
`tre2=0` C^{-2}	Quadratic temperature coefficient for the emitter resistor.

© 2023 Cadence Design Systems, Inc.

`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eglev=0`	DC temperature selector.
`gap1=7.02e-4 V/C`	Band-gap temperature coefficient.
`gap2=1108 C`	Band-gap temperature offset.
`tikf1=0 1/C`	Linear temperature coefficient for `ikf`.
`tikf2=0` C^{-2}	Quadratic temperature coefficient for `ikf`.
`tikr1=0 1/C`	Linear temperature coefficient for `ikr`.
`tikr2=0` C^{-2}	Quadratic temperature coefficient for `ikr`.
`tirb1=0 1/C`	Linear temperature coefficient for `irb`.
`tirb2=0` C^{-2}	Quadratic temperature coefficient for `irb`.
`tis1=0 1/C`	Linear temperature coefficient for `is`.
`tis2=0` C^{-2}	Quadratic temperature coefficient for `is`.
`tise1=0 1/C`	Linear temperature coefficient for `ise`.
`tise2=0` C^{-2}	Quadratic temperature coefficient for `ise`.
`tisc1=0 1/C`	Linear temperature coefficient for `isc`.
`tisc2=0` C^{-2}	Quadratic temperature coefficient for `isc`.
`tiss1=0 1/C`	Linear temperature coefficient for `iss`.
`tiss2=0` C^{-2}	Quadratic temperature coefficient for `iss`.
`tbf1=0 1/C`	Linear temperature coefficient for `bf`.
`tbf2=0` C^{-2}	Quadratic temperature coefficient for `bf`.
`tbr1=0 1/C`	Linear temperature coefficient for `br`.
`tbr2=0` C^{-2}	Quadratic temperature coefficient for `br`.
`tvaf1=0 1/C`	Linear temperature coefficient for `vaf`.
`tvaf2=0` C^{-2}	Quadratic temperature coefficient for `vaf`.
`tvar1=0 1/C`	Linear temperature coefficient for `var`.
`tvar2=0` C^{-2}	Quadratic temperature coefficient for `var`.
`titf1=0 1/C`	Linear temperature coefficient for `itf`.
`titf2=0` C^{-2}	Quadratic temperature coefficient for `itf`.

© 2023 Cadence Design Systems, Inc.

`ttf1=0 1/C`	Linear temperature coefficient for `tf`.
`ttf2=0 C`$^{-2}$	Quadratic temperature coefficient for `tf`.
`ttr1=0 1/C`	Linear temperature coefficient for `tr`.
`ttr2=0 C`$^{-2}$	Quadratic temperature coefficient for `tr`.
`tnf1=0 1/C`	Linear temperature coefficient for `nf`.
`tnf2=0 C`$^{-2}$	Quadratic temperature coefficient for `nf`.
`tnr1=0 1/C`	Linear temperature coefficient for `nr`.
`tnr2=0 C`$^{-2}$	Quadratic temperature coefficient for `nr`.
`tne1=0 1/C`	Linear temperature coefficient for `ne`.
`tne2=0 C`$^{-2}$	Quadratic temperature coefficient for `ne`.
`tnc1=0 1/C`	Linear temperature coefficient for `nc`.
`tnc2=0 C`$^{-2}$	Quadratic temperature coefficient for `nc`.
`tns1=0 1/C`	Linear temperature coefficient for `ns`.
`tns2=0 C`$^{-2}$	Quadratic temperature coefficient for `ns`.
`tmje1=0 1/C`	Linear temperature coefficient for `mje`.
`tmje2=0 C`$^{-2}$	Quadratic temperature coefficient for `mje`.
`tmjc1=0 1/C`	Linear temperature coefficient for `mjc`.
`tmjc2=0 C`$^{-2}$	Quadratic temperature coefficient for `mjc`.
`tmjs1=0 1/C`	Linear temperature coefficient for `mjs`.
`tmjs2=0 C`$^{-2}$	Quadratic temperature coefficient for `mjs`.
`cte=0 1/C`	Temperature coefficient for `cje`.
`ctc=0 1/C`	Temperature coefficient for `cjc`.
`cts=0 1/C`	Temperature coefficient for `cjs`.
`tvje=0 V/C`	Temperature coefficient for `vje`.
`tvjc=0 V/C`	Temperature coefficient for `vjc`.
`tvjs=0 V/C`	Temperature coefficient for `vjs`.
`tvtf1=0 1/C`	Linear temperature coefficient for `vtf`.
`tvtf2=0 C`$^{-2}$	Quadratic temperature coefficient for `vtf`.
`txtf1=0 1/C`	Linear temperature coefficient for `xtf`.

© 2023 Cadence Design Systems, Inc.

`txtf2=0` C^{-2}	Quadratic temperature coefficient for `xtf`.

© 2023 Cadence Design Systems, Inc.

Junction diode model control parameters

`dskip=yes`	Skip junction calculations if they are reverse-saturated. Possible values are `yes` and `no`.
`imelt=imax A`	Junction explosion current (*area).

Operating region warning control parameters

`bvbe=∞ V`	B-E breakdown voltage.
`bvbc=∞ V`	B-C breakdown voltage.
`bvce=∞ V`	C-E breakdown voltage.
`bvsub=∞ V`	Substrate junction breakdown voltage.
`vbefwd=0.2 V`	B-E forward voltage.
`vbcfwd=0.2 V`	B-C forward voltage.
`vsubfwd=0.2 V`	Substrate junction forward voltage.
`imax=1e3 A`	Maximum allowable base current (*area).
`imax1=imax A`	Maximum allowable collector current (*area).
`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `fwd`, `rev`, and `sat`.

Noise model parameters

`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`kb=0`	Burst noise coefficient.
`bnoisefc=1`	Burst noise cutoff frequency.
`rbnoi=rb Ω`	Effective base noise resistance.

DC-mismatch model parameters

`mvt0=0.0 V`	Threshold mismatch intercept.

© 2023 Cadence Design Systems, Inc.

Compatibility model parameters

`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`updatelevel=0`	Model update selector. The available versions are 0, 1.

Shrink Parameters

Safe Operating Areas Parameters

`vbe_max=∞ V`	Maximum allowed voltage across base and emitter.
`vbc_max=∞ V`	Maximum allowed voltage across base and collector.
`vce_max=∞ V`	Maximum allowed voltage across collector and emitter.
`vcs_max=∞ V`	Maximum allowed voltage across collector and substrate.

Auto Model Selector parameters

`areamax=0`	Maximum transistor area factor for which the model is valid.
`areamin=1`	Minimum transistor area factor for which the model is valid.

`imax` and `imelt`

The`imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax'. If `imax' is exceeded during iterations, the linear model is substituted until the current drops below 'imax' or until convergence is achieved. If convergence is achieved with the current exceeding `imax', the results are inaccurate, and a warning is printed out.

A separate model parameter, `imelt', is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt', the base and collector currents are composed of many exponential terms, a warning will be issued and the results become inaccurate. The junction current is linearized above the value of `imelt' to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt'.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`ibeeff (Ohm)`	The effective reverse saturation current of BE.
`ibceff (Ohm)`	The effective reverse saturation current of BC.
`iseeff (Ohm)`	The effective leakage saturation current of BE.
`isceff (Ohm)`	The effective leakage saturation current of BC.
`isseff (Ohm)`	The effective reverse saturation current of bulk-collector or bulk-base.

Operating Point Parameters

`type=npn`	Transistor type. Possible values are `npn` and `pnp`.
`struct=vertical`	Transistor structure. For pnp, default is `lateral`. Possible values are `vertical` and `lateral`.
`trise (C)`	Temperature rise from ambient.
`region=fwd`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `fwd`, `rev`, `sat`, and `breakdown`.
`vbe (V)`	Base-emitter voltage (alias=lx0).
`vbc (V)`	Base-collector voltage (alias=lx1).
`vce (V)`	Collector-emitter voltage.
`vsub (V)`	Substrate junction voltage (alias=lx24).
`ic (A)`	Resistive collector current (alias=lx2).
`ib (A)`	Resistive base current (alias=lx3).
`isub (A)`	Resistive substrate current (alias=lv6).
`pwr (W)`	Power dissipation.
`betadc (A/A)`	Ratio of resistive collector current to resistive base current (alias=lv10).
`betaac (A/A)`	Small-signal common-emitter current gain.
`gm (S)`	Common-emitter transconductance (alias=lx6).
`rpi (Ω)`	Common-emitter input resistance.
`ro (Ω)`	Common-emitter output resistance.

© 2023 Cadence Design Systems, Inc.

rb (Ω)	Parasitic base resistance.
rc (Ω)	Parasitic collector resistance.
cpi (F)	Common-emitter input capacitance (alias=lx19).
cmu (F)	Common-base output capacitance (alias=lx20).
cmux (F)	External common-base output capacitance (alias=lx22).
csub (F)	Substrate capacitance (alias=lx21).
ft (Hz)	Unity small-signal current-gain frequency (alias=lv5).
gpi (S)	Gpi=ib/vbe constant vbc (alias=lx4).
gmu (S)	Gmu=ib/vbc constant vbe (alias=lx5).
g0 (S)	G0=ic/vce constant vbe (alias=lx7).
gb (S)	1/Rbeff internal conductance (alias=lx16).
qbe	Base emitter charge (alias=lx8).
qbc	Base collector charge (alias=lx10).
qsc	Collector substrate charge.
grc (S)	Collector conductance (alias=lv16).
rbb (Ω)	Base resistance (alias=lv14).
log_ic (A)	Log(Ic) (alias=lv8).
log_ib (A	Log(Ib) (alias=lv9).
gre (S)	Emitter conductance (alias=lv15).
re (Ω)	

Related Topics

Excess Phase

Temperature Effect

Noise Model

BJT Model (bjt)

© 2023 Cadence Design Systems, Inc.

6

HiCUM Model (bht)

The HiCUM model was developed by Professor M. Schroter. Click the following links to know the details about the HiCUM Model:

- Spectre HICUM Model Compared to Public HICUM Model
- Model Description
- DC Equations
- Charge and Capacitance Equations
- Noise Model
- Temperature Effect
- Self-Heating
- NQS effect
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.

Spectre HICUM Model Compared to Public HICUM Model

MMSIM supports HICUM model version = 1.0, 2.1, 2.20, 2.21, 2.22, 2.23, 2.24, 2.3, 2.31, 2.32, 2.33, 2.34, 2.40, and 3.00. Model parameter “updatelevel” is added by Cadence in order to include some enhancement. The detail information is in the below:

- **updatelevel = 0:** The model is compatible with the original HICUM Fortran code. Temperature dependence is ignored in the model. No fix or enhancement is added to updatelevel=0. The model may show convergence issue. It is not suggested to use it.
- **updatelevel = 1 / 2:** This level has better temperature dependence. It includes some fixes and enhancements. Version1.0, 2.1, 2.20, 2.21 and 2.22 supports this level.
- **updatelevel = 3:** This level has complete derivatives for current and charge model. And the simulation result is fully compatible with the result from HICUM Verilog-A model (released from TU Dresden, Germany). This level supports version = 2.1, 2.20, 2.21, 2.22, 2.23, 2.24, 2.3, 2.31, 2.32, 2.33, 2.34, and 2.40. It is recommended to use this level. Further enhancement will be focusing on this level. Version = 2.23 and 2.24 support NQS effects.

Self-Heating

You can set `self_heating=fast` to enable the fast self-heating which has high performance. The result should be identical or close to normal self-heating result.

Parameter flcomp

When updatelevel=3, if `flcomp`=0 or 2.1 the result is consistent with version2.1, irrespective of the version used in the netlist.

Related Topics

Model Description

HiCUM Model Version 2.2

HiCUM Model Version 2.3

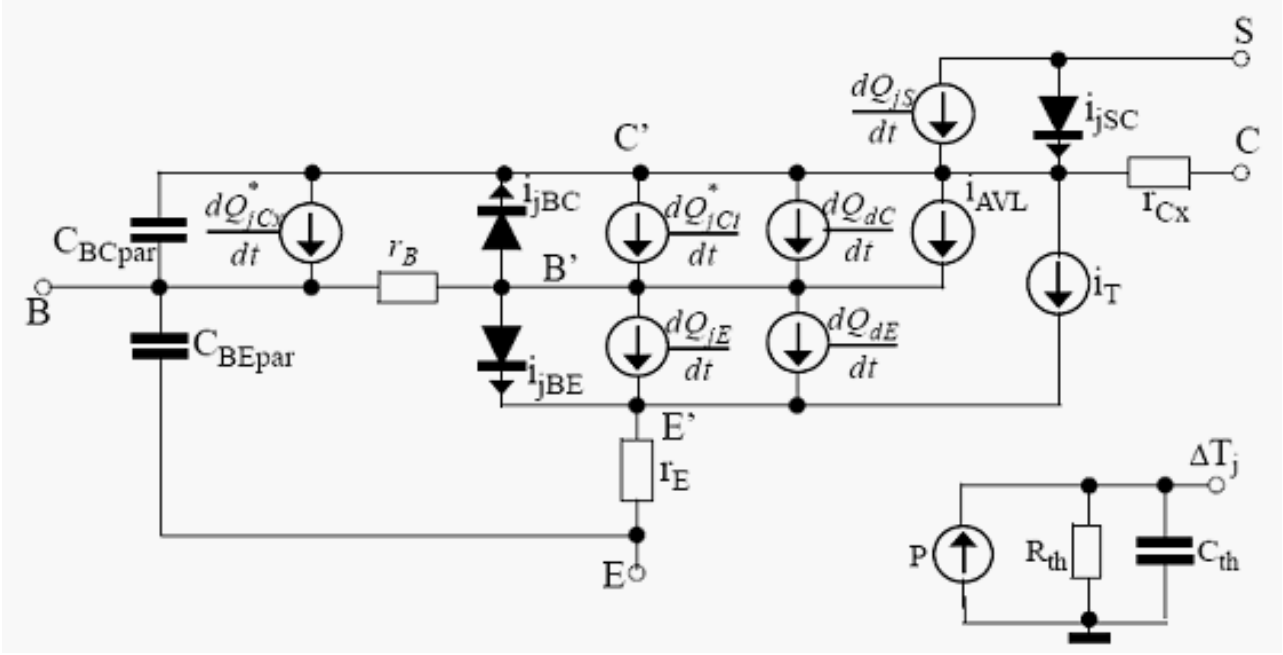
Component Statements

HiCUM Model (bht)

© 2023 Cadence Design Systems, Inc.

Model Description

The HICUM model is a semi-physical compact bipolar transistor model. Semi-physical means that for arbitrary transistor configurations, a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data. This model was developed with special emphasis on modeling the operating region at high current densities. The modularity and physics-based approach of this model allows the construction of a model hierarchy without additional effort in parameter extraction.



Large-signal HICUM Equivalent Circuit

Thermal Network

© 2023 Cadence Design Systems, Inc.

DC Equations

$$i_T = i_{Tf} - i_{Tr}$$

$$i_{Tf1} = \frac{C_{10}}{Q_{p,T}} \exp\left(\frac{V_{B'E'}}{m_{cf} V_T}\right)$$

$$i_{Tf} = i_{Tf1}\left(1 + \frac{i_{Tf1}}{i_{ch}}\right)$$

$$i_{Tr} = \frac{C_{10}}{Q_{p,T}} \exp\left(\frac{V_{B'C'}}{V_T}\right)$$

$$Q_{p,T} = \frac{Q_{p,low}}{2} + \sqrt{\left(\frac{Q_{p,low}}{2}\right)^2 + \tau_{f0} C_{10} \exp\left(\frac{V_{B'E'}}{V_T}\right) + \tau_r C_{10} \exp\left(\frac{V_{B'C'}}{V_T}\right)}$$

$$Q_{p,1} = Q_{p0} + Q_{jEi} h_{jei} + h_{jci} Q_{jci}$$

$$I_{CK} = \frac{V_{ceff}}{r_{cio}} \frac{1}{\sqrt{1 + \left(\frac{V_{ceff}}{V_{lim}}\right)^2}} \left[1 + \frac{x + \sqrt{x^2 + 10^{-3}}}{2}\right]$$

$$X = (V_{ceff} - V_{lim}) / V_{PT}$$

$$r_{cio} = \frac{w_c}{q \mu_{nC0} N_{ci} A_E} \frac{1}{f_{cs}}$$

$$V_{lim} = \frac{V_{sn}}{\mu_{nc0}} w_c$$

$$V_{PT} = \frac{q N_{ci}}{2E} w_c^2$$

© 2023 Cadence Design Systems, Inc.

$$i_{jBEi} = I_{BEis}\left[\exp\left(\frac{V_{B'E'}}{m_{BEi}V_T}\right)-1\right]+I_{REis}\left[\exp\left(\frac{V_{B'E'}}{m_{BEi}V_T}\right)-1\right]$$

$$i_{jBEp} = I_{BEps}\left[\exp\left(\frac{V_{B'E'}}{m_{BEp}V_T}\right)-1\right]+I_{REps}\left[\exp\left(\frac{V_{B'E'}}{m_{REp}V_T}\right)-1\right]$$

$$i_{jBCi} = I_{BCis}\left[\exp\left(\frac{V_{B'C'}}{m_{BCi}V_T}\right)-1\right]$$

$$i_{jBCx} = I_{BCxs}\left[\exp\left(\frac{V_{B'C'}}{M_{BCx}V_T}\right)-1\right]$$

$$r_{Bi} = r_{Bi0}\frac{C_i}{C_i + C_{dEp}}$$

$$r_{Bi0} = r_{SBi0}\frac{b_E}{l_E n_E}g_i$$

$$C_i = C_{jEi} + C_{dEi} + C_{dci}$$

$$C_{dEp} = C_{dE}(1-f_{Qi})$$

$$i_{AVL} = I_T\frac{f_{AVL}V_{DCi}}{C_c^{1/z_{ci}}}\exp\left(-\frac{q_{AVL}}{C_{jCi0}V_{DCi}}C_c^{(1/z_{ci}-1)}\right)$$

$$C_c = \frac{C_{jci}(V_{B'C'})}{C_{jci}0}$$

*

$$i_{BEt} = I_{BEts}(-V_e)C_e^{1-1/z_E}\exp\left[-a_{BEt}C_e^{1/z_E-1}\right]$$

© 2023 Cadence Design Systems, Inc.

$$I_{BEts} = 2\frac{\sqrt{2m^*/E_G}q^3V_{DE}^2}{h^2\varepsilon_{Si}}C_{jE0}$$

$$a_{BEt} = \frac{8\pi\sqrt{2m^*E_G}E_G}{3qh}\frac{W_{BE0}}{2V_{DE}}$$

$$C_e = \frac{C_{jE(V)}}{C_{jE0}}$$

$$i_{TS} = I_{TSf} - I_{TSr} = I_{TSS}\left[\exp\left(\frac{V_{B^*C'}}{m_{Sf}V_T}\right) - \exp\left(\frac{V_{S'C'}}{m_{Sr}V_T}\right)\right]$$

$$i_{SC} = I_{SCS}\left[\exp\left(\frac{V_{S'C'}}{m_{SC}V_T}\right) - 1\right]$$

© 2023 Cadence Design Systems, Inc.

Charge and Capacitance Equations

$$Q_{P,T} = Q_{p0} + h_{jEi}Q_{jEi} + h_{jCi}Q_{jCi} + Q_{f,T} + Q_{r,T}$$

$$Q_{f,T} = Q_{f0} + \Delta Q_{Ef} + \Delta Q_{fh}$$

$$Q_{f0} = \tau_{f0} i_{Tf}$$

$$\Delta Q_{Ef} = \Delta\tau_{Ef} \frac{i_{Tf}}{1 + g_{\tau E}}$$

$$\Delta\tau_{Ef} = \tau_{Ef0} \left(\frac{i_{Tf}}{I_{CK}} \right)^{g_{\tau E}}$$

$$\tau_{Ef0} = \frac{1}{\beta_0} \left(\frac{W_E}{V_{Ke}} + \frac{W_E^2}{2\mu_{PE} V_T} \right)$$

$$\Delta Q_{fh} = \Delta Q_{Bf} + Q_{cf} = \tau_{hcS} i_{Tf} W^2$$

$$Q_{r,T} = \tau_r i_{Tr}$$

$$C_{jEi} = \frac{C_{jEi0}}{\left(1 - V_j / V_{DEi}\right)^{2_{Ei}}} \cdot \frac{e}{1 + e} + a_{jEi} C_{jEi0} \frac{1}{1 + e}$$

$$e = \exp\left(\frac{V_f - V_{B'E'}}{V_T} \right)$$

$$V_j = V_f - V_T \ln[1 + e] < V_f$$

$$V_f = V_{DEi} \left[1 - a_{jEi}^{-(1/(z_{Ei}))} \right]$$

© 2023 Cadence Design Systems, Inc.

$$Q_{jEi} = \frac{C_{jEi0}V_{DEi}}{1-Z_{Ei}}\left[1-\left(1-\frac{V_j}{V_{DEi}}\right)^{(1/(z_{Ei}))}\right] + a_{jEi}C_{jEi0}(V_{B'E'}-V_j)$$

$$C_{jci} = C_{jci,cl} + C_{jci,PT} + C_{jci,fb}$$

$$C_{jci,cl} = \frac{C_{jci0}}{(1-V_{j,m}/V_{DCi})^{z_{ci}}} \cdot \frac{Q_{j,r}}{1+e_{j,r}} \frac{e_{j,m}}{1+e_{j,m}}$$

$$C_{jci,fb} = a_{jci}C_{jci0}\frac{1}{e_{j,r}+1}$$

$$C_{jci,PT} = \frac{C_{jci0,r}}{(1-V_{j,r}/V_{DCi})^{Z_{ci,r}}} \cdot \frac{1}{1+e_{j,m}}$$

$$Q_{jCi} = Q_{jCi,m} + Q_{jci,r} + a_{jci}C_{jci0}(V_{B'C'}-V_{j,r}) - Q_{jci,c}$$

$$Q_{jCi,m} = \frac{C_{jCi0}V_{DCi}}{1-z_{Ci}}\left[1-\left(1-\frac{V_{j,m}}{V_{DCi}}\right)^{1-z_{Ci}}\right]$$

$$Q_{jCi,r} = \frac{C_{jCi,r}V_{DCi}}{1-z_{Ci,r}}\left[1-\left(1-\frac{V_{j,r}}{V_{DCi}}\right)^{1-z_{Ci,r}}\right]$$

$$Q_{jCi,c} = \frac{C_{jCi,r}V_{DCi}}{1-z_{ci,r}}\left[1-\left(1-\frac{V_{j,m}}{V_{DCi}}\right)^{1-z_{Ci,r}}\right]$$

$$C_{jCi0,r} = C_{jCi0} \cdot \left(\frac{V_{DCi}}{V_{PTCi}}\right)^{(Z_{ci}-Z_{ci,r})}$$

$$C_i = C_{jEi} + C_{jCi} + C_{dE} + C_{dC}$$

$$Q_{dS} = \Upsilon_{Sf}{}^{i}{}_{TSf}$$

© 2023 Cadence Design Systems, Inc.

$$C_{dE} = \tau_f S_{fb}$$

$$C_{dC} = \tau_r S_{rC} + \tau_f S_{fC}$$

$$C_{dS} = \tau_{Sf} S_{TSu,\,b}$$

$$S_{fb} = \left.\frac{dI_{Tf}}{dV_{B'E'}}\right|_{V_{B'C'}} = \frac{I_{Tf1}}{V_{Tf}} \cdot \frac{Q_{P,\,T} + \tau_r I_{Tr} - h_{jei} C_{jEi} V_{Tf}}{Q_{P,\,T} + \tau_r I_{Tr} + \tau_{fT} I_{Tf1} d_{ch}} d_{ch}$$

$$d_{Ch} = 1 + 2 I_{Tf1} / I_{Ch}$$

$$S_{fC} = \left.\frac{dI_{Tf}}{dV_{C'E'}}\right|_{V_{B'E'}} = \frac{I_{Tf1}}{V_{Af}} \cdot \frac{d}{1 + d\tau_{f,\,T} I_{Tf1} / Q_{p,\,T}}$$

$$V_{Af} = \frac{Q_{P,T}}{h_{jci} C_{jCi} - \left.\frac{dQ_f}{dV_{C'E'}}\right|_{V_{B'E'}}}$$

$$d = d_{ch} \frac{e}{1 + e}$$

$$e = \exp\left(\frac{V_c}{V_T} - 1\right)$$

$$S_{rc} = \left.\frac{dI_{Tr}}{dV_{C'E'}}\right|_{V_{B'E'}} = -\frac{I_{Tr}}{V_T} \cdot \frac{Q_{P,\,T} + (\tau_{f,\,T} S_{fc} - h_{jci} C_{jci}) V_T}{Q_{p,\,T} + \tau_r I_{Tr}}$$

$$S_{Tsu,\,b} = \frac{I_{TsS}}{m_{sf} V_T} \exp\left(\frac{V_{B*C'}}{m_{sf} V_T}\right)$$

© 2023 Cadence Design Systems, Inc.

Noise Model

$$\overline{i_{RE}^2} = \frac{4K_B T\Delta f}{r_E}$$

$$\overline{i_{Rcx}^2} = \frac{4K_B T\Delta f}{r_{cx}}$$

$$\overline{i_{Bx}^2} = \frac{4K_B T\Delta f}{r_{Bx}}$$

$$\overline{i_{Bin}^2} = \frac{4K_B T\Delta f}{r_{Bin}}$$

$$\overline{i_T^2} = 2qI_T\Delta f$$

$$\overline{i_{AVL}^2} = 2qI_{AVL}\Delta f$$

Diode currents I_{jdiode}={BEi, BCi, BEp, BCx, CS}:

$$\overline{i_{jdiode}^2} = 2qI_{jdiode}\Delta f$$

$$\overline{i_{BE}^2} = k_F(I_{jBEi} + I_{jBEp})^{\alpha_F}\frac{\Delta f}{f}$$

Correlation between base and collector noise spectral density S_{incinb}:

$$S_{incinb} \approx -2qI_T \times (j\omega\tau_{Bf} \times alit)$$

$$\tau_{Bf} = \frac{I_T}{I_{BEi}}$$

© 2023 Cadence Design Systems, Inc.

Temperature Effect

$$r_{ci}(T) = r_{ci}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{ci}}$$

$$V_{lim}(T) = V_{lim}(T_0)(1-\alpha_{VS}\Delta T)\left(\frac{T}{T_0}\right)^{\zeta_{Ci}}$$

$$V_{C'E's}(T) = V_{C'E's}(T_0)[1+\alpha_{CEs}\Delta T]$$

$$\tau_0(T) = \tau_0(T_0)[1+\alpha_{\tau 0}\Delta T + K_{\tau 0}\Delta T^2]$$

$$\tau_{hcs}(T) = \tau_{hcs}(T_0)\left(\frac{T}{T_0}\right)^{(\tau_{ci}-1)}$$

$$\tau_{Ef0}(T) = \tau_{Ef}(T_0)\frac{T/T_0}{1+\alpha_B\Delta T}$$

$$V_D(T) = V_D(T_0)\frac{T}{T_0} - V_{Gj}\left(\frac{T}{T_0}-1\right) - 3V_T\ln\left(\frac{T}{T_0}\right)$$

$$C_{j0}(T) = C_{j0}(T_0)\left(\frac{V_D(T_0)}{V_D(T)}\right)^2$$

$$\alpha_J(T) = \alpha_j(T_0)\frac{V_D(T)}{V_D(T_0)}$$

$$r_{Bi0}(T) = r_{Bi0}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{rBi}}$$

$$f_{AVL}(T) = f_{AVL}(T_0)\exp(\alpha_{fav}\Delta T)$$

$$q_{AVL}(T) = q_{AVL}(T_0)\exp(\alpha_{qav}\Delta T)$$

© 2023 Cadence Design Systems, Inc.

$$I_{BEtsS}(T) = I_{BEtS}(T_0)\sqrt{\frac{V_G(T_0)}{V_G(T)}}\left(\frac{V_{DEp}(T)}{V_{DEp}(T_0)}\right)^2\frac{C_{jEp0}(T)}{C_{jEp0}(T_0)}$$

$$a_{BEt}(T) = a_{BEt}(T_0)\left(\frac{V_G(T)}{V_G(T_0)}\right)^{3/2}\frac{V_{DEp}(T)}{V_{DEp}(T_0)}$$

When `updatelevel=0`,

$Itss(T) = Itss(T0)$ (No temperature dependence)

$$TEF0(T0) = TEF0(T0)\times(T/T0)/(0.5\times(A+\sqrt{A\times A+0.01}))$$

When `updatelevel=1`,

$$Itss(T) = Itss(T0)\times(T/T0)^{3/Msf}\times\exp(VGB/(Msf\times Vt)\times(T/T0-1))$$

$$TEF0(T0) = TEF0(T0)\times(T/T0)/(0.5\times(A+\sqrt{A\times A+le-6}))$$

$Cdci = Tr\times Src$

where

$A = 1.0 + Alb\times DeltaT$

The original HICUM model had simple derivatives for some currents and charges, which sometimes caused convergence issues. There have been some enhancements made to solve this problem, especially for AC analyses.

Self-Heating

You can set `self_heating=fast` to enable the fast self-heating, which is faster than the full self-heating but gives similar results in most cases.

Self-heating for parasitic resistor is given by the following equation:

$Pwr = Vcei\times It - Vbci\times lavl$

If updatelevel=2,

© 2023 Cadence Design Systems, Inc.

$$Pwr = Pwr + (Vbp - Vb) \times \frac{(Vbp - Vb)}{Rbi}$$ if Rbi0 is given

$$Pwr = Pwr + (Vbx - Vbp) \times \frac{(Vbx - Vbp)}{Rbx}$$ if Rbx is given

$$Pwr = Pwr + (Vcx - Vc) \times \frac{(Vcx - Vc)}{Rcx}$$ if Rcx is given

$$Pwr = Pwr + (Ve - Vex) \times \frac{(Ve - Vex)}{Re}$$ if Re is given

NQS effect

Lateral NQS

The lateral NQS effect is implemented by an adequate capacitance C_{rBi} in parallel to the resistance r_{Bi}.

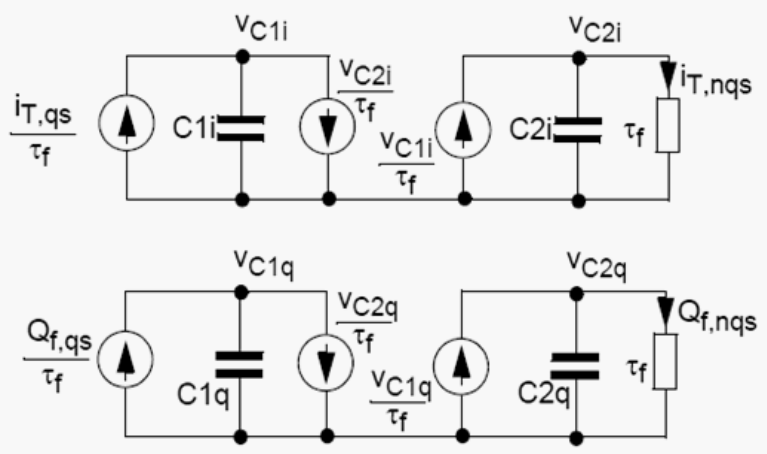
$$C_{rBi} = f_{crBi} \times C_{jei} \times C_{jci} \times C_{dei} \times C_{dci}$$

$$Q_{rBi} = C_{rBi} \times V_{B \times B''''}$$

Vertical NQS

Vertical NQS effects are implemented through “additional delay times” for both minority charge Q_f and forward transfer current i_{Tf}. The figure below shows the adjunct NQS networks for Transfer Current i_T and Minority Charge Q_r.

© 2023 Cadence Design Systems, Inc.



$$\frac{I_{T,qs} - V_{C2i}}{\tau_f} = \frac{d \times (alit \times V_{C1i})}{dt}$$

$$\frac{V_{C1i} - V_{C2i}}{\tau_f} = \frac{d \times (alit \times V_{C2i}/3)}{dt}$$

$$I_{T,nqs} = \frac{V_{C2i}}{\tau_f}$$

$$\frac{Q_{T,qs} - V_{C2q}}{\tau_f} = \frac{d \times (alqf \times V_{C1i})}{dt}$$

$$\frac{V_{C1q} - V_{C2q}}{\tau_f} = \frac{d \times (alqf \times V_{C2q}/3)}{dt}$$

$$Q_{T,nqs} = \frac{V_{C2q}}{\tau_f}$$

Related Topics

Spectre HICUM Model Compared to Public HICUM Model

© 2023 Cadence Design Systems, Inc.

HiCUM Model Version 2.2

HiCUM Model Version 2.3

Component Statements

HiCUM Model (bht)

HiCUM Model Version 2.2

Temperature Dependent Bandgap Voltage

$$V_g(T) = V_g(0) + K_1 T 1n(T) + K_2 T$$

$$V_g(T) = V_{g,cq}(0) - \frac{\alpha_g T^2}{T + T_g}$$

For compact model and application purposes, it is sometimes more convenient to re-write the above equation in terms of a reference temperature T_0 (e.g. for parameter extraction), which gives

$$V_g(T) = V_g(T_0) + k1\frac{T}{T_0}\ln\left(\frac{T}{T_0}\right) + k_2\left(\frac{T}{T_0} - 1\right)$$

with the definitions

$$k_1 = k_1 T_0$$

$$k_2 = k_2 T_0 + k_1 1n(T_0)$$

and the bandgap voltage at the measurement reference temperature,

$$V_g(T_0) = k_2 + V_g(0)$$

The choice of the bandgap description also influences the formulation of the effective intrinsic carrier density, which now reads

© 2023 Cadence Design Systems, Inc.

$$n_{ie}^2(T) = n_{ie}^2(T_0)\left(\frac{T}{T_0}\right)^{m_g}\exp\left[\frac{V_{geff}(0)}{V_T}\left(\frac{T}{T_0}-1\right)\right]$$

with the constant

$$m_g = 3-\frac{k_1}{V_{T0}} = 3-\frac{qK_1}{K_B}$$

Transfer current

Base Region Reach-Through

$$Q_{pT,j} = Q_{p0}+h_{jEi}Q_{jEi}+h_{jCi}Q_{jCi}$$

$$Q_{pT,low} = Q_{B,rt}\left(1+\frac{x+\sqrt{x^2+a}}{2}\right)$$

and a = 1.921812.

$$x = \frac{Q_{pT,j}}{Q_{B,rt}}-1$$

Temperature Dependence

Prefactor

$$c_{10}(T) = c_{10}(T_0)\left(\frac{T}{T_0}\right)^{\varsigma_{CT}}\exp\left[\frac{V_{gBeff}(0)}{V_T}\left(\frac{T}{T_0}-1\right)\right]$$

$$\varsigma_{CT} = m_g+1-\zeta_{\mu mB}$$

© 2023 Cadence Design Systems, Inc.

Zero-Bias Hole Charge

$$Q_{p0}(T) = Q_{p0}(T_0)\left[2 - \left(\frac{V_{DEi}(T)}{V_{DEi}(T_0)}\right)^{Z_{Ei}}\right]$$

Base Currents

Excess Base Current from Recombination at the BC Barrier

$$i_{Bhrec} = \frac{\Delta Q_{Bf}}{\tau_{Bhrec}}$$

Temperature Dependent Junction Current Components

$$I_{BEiS}(T) = I_{BEiS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{BET}} \exp\left[\frac{V_{gEeff}(0)}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$$

$$V_{gEeff}(0) = V_{gBeff}(0) - \alpha_{Bf} T_0 V_{T0}$$

$$I_j = I_{jS}\exp\left(\frac{V}{mV_T}\right)$$

$$I_{jS}(T) = I_{jS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_T} \exp\left[\frac{V_{geff}(0)}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$$

$$V_{gBEeff} = \frac{V_{gBEeff} + V_{gEeff}}{2}$$

$$\mu_{Ci}(T) = \mu_{Ci}(T_0)\left(\frac{T}{T_0}\right)^{-\zeta_{Ci}}$$

$$\zeta_{BCiT} = m_g + 1 - \zeta_{Ci}$$

© 2023 Cadence Design Systems, Inc.

$$\zeta_{BCxT} = m_g + 1 - \zeta_{Cx}$$

$$\zeta_{SCT} = m_g + 1 - \zeta_{\mu pS}$$

Depletion Capacitances and Charges

Bias Dependence of Base-Emitter Component

$$v_j = V_f - V_T \frac{x + \sqrt{x^2 + a_{fj}}}{2} < V_f$$

$$x = \frac{V_f - v_{B'E'}}{V_T}$$

$$a_{fj} = 4 \ln^2(2) = 1.921812$$

$$C_{jEi} = \frac{C_{jEi0}}{(1 - v_j / V_{DEi})^{z_{Ei}}} \cdot \frac{dv_j}{dv_{B'E'}} + a_{jEi} C_{jEi0} \left(1 - \frac{dv_j}{dv_{B'E'}}\right)$$

$$\frac{dv_j}{dv_{B'E'}} = \frac{x + \sqrt{x^2 + a_{fj}}}{2\sqrt{x^2 + a_{fj}}}$$

External Depletion Capacitances

The formulation for the depletion capacitances C_{jEp} also has been changed from exponential to hyperbolic smoothing functions.

© 2023 Cadence Design Systems, Inc.

Temperature Dependence of Built-in Voltages

$$V_{Dj}(T_0) = 2V_{T0}\ln\left[\exp\left(\frac{V_D(T_0)}{2V_{T0}}\right) - \exp\left(\frac{V_D(T_0)}{2V_{T0}}\right)\right]$$

$$V_{Dj}(T) = V_{Dj}(T_0)\frac{T}{T_0} - 3V_T\ln\left(\frac{T}{T_0}\right) + V_{geff}(T) - V_{geff}(T_0)\left(\frac{T}{T_0}\right)$$

For the bandgap voltage formulation, the above equation reads

$$V_{Dj}(T) = V_{Dj}(T_0)\frac{T}{T_0} - m_g V_T\ln\left(\frac{T}{T_0}\right) - V_{geff}(0)\left(\frac{T}{T_0} - 1\right)$$

which reduces to the classical equation (that assumes a linear temperature dependence of V_{geff}) if $m_g = 3$. Finally, the new built-in voltage is calculated as

$$V_D(T) = V_{Dj}(T) + 2V_T\ln\left(\frac{1}{2}\left[1 + \sqrt{1 + 4\exp\left(-\frac{V_{Dj}(T)}{V_T}\right)}\right]\right)$$

$$V_{geff} \rightarrow V_{g(x,y)eff} = \frac{V_{gxeff} + V_{gyeff}}{2}$$

$$\left.\frac{dV_D(T)}{dT}\right|_{T_0} \cong \left.\frac{dV_{Dj}(T)}{dT}\right|_{T_0}$$

$$\left.\frac{dV_{Dj}(T)}{dT}\right|_{T_0} = \frac{V_{Dj}(T_0) - V_{geff}(0) - m_g V_T)}{T_0}$$

© 2023 Cadence Design Systems, Inc.

Minority Charge

Effective Collector Voltage and Critical Current

$$v_{ceff} = V_T\left[1 + \frac{u + \sqrt{u^2 + a_{vceff}}}{2}\right]$$

$$u = \frac{v_c - V_T}{V_T}$$

$$x = \frac{v_{ceff} - V_{lim}}{V_{PT}}$$

Diffusion Capacitances

$$C_{dCi} = \tau_r S_{rc} + \tau_f S_{fc}$$

has been changed to

$$C_{dCi} = \tau_r S_{rc}$$

$$C_{dEi}^{C} = \tau_f S_{fc} + \left.\frac{dQ_f}{dV_{CE}}\right|_{T_{Tf},\, T}$$

$$C_{dEi}^{B} = \tau_r S_{rb}$$

© 2023 Cadence Design Systems, Inc.

Temperature Dependence

Critical Voltage Vlim

$$V_{lim}(T) = \frac{v_s(T)}{\mu_{nCi0}(T)}$$

$$v_s(T) = v_{s0}(T_0)\left(\frac{T}{T_0}\right)^{-a_{vs}}$$

$$a_{vs} = a_{vs}T_0$$

Inserting the temperature dependence of the collector electron mobility into the $V_{lim}(T)$ equation gives the physics-based formulation

$$V_{lim}(T) = V_{lim}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{Cl} - a_{vs}}$$

The following equation replaces the formulation used in version 2.1:

$$V_{lim}(T) = V_{lim}(T_0)(1 - a_{vs}\Delta T)\left(\frac{T}{T_0}\right)^{\zeta_{Cl}}$$

Emitter Transit Time

$$\tau_{Ef0}(T) = \tau_{Ef0}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\tau Cl}} \exp\left[-\frac{\Delta V_{geff}(0)}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$$

$$\Delta V_{geff}(0) = V_{gBeff}(0) - V_{gEeff}(0)$$

$$\zeta_{\tau Ef} = \zeta_{BET} - \zeta_{CT} - 0.5$$

© 2023 Cadence Design Systems, Inc.

Collector Current Spreading

$$f_{ccs} = \frac{\tau_f(I_{CK})}{\tau_{f,ID}(I_{CK})}$$

$$\tau_{hcs} = f_{ccs}\tau_{pCs} + \tau_{Bfvs} = f_{ccs}\frac{w_C^2}{4\mu_{nC0}V_T} + \frac{w_{Bm}w_C}{2G_{\zeta i}\mu_{nC0}V_T}$$

The original model parameter τ_{hcs} is be extracted from measurements together with the partitioning factor

$$f_{thc} = \frac{\tau_{pCs}}{\tau_{hcs,x}}$$

Thus, during preprocessing for model card generation, the modified extracted time constant

$$\tau_{hcs} = (1-f_{thc})\tau_{hcs,x} + f_{ccs}\tau_{pCs} = [(1-f_{thc}) + f_{ccs}f_{thc}]\tau_{hcs,x}$$

is calculated and used as a model parameter.

Internal Base Resistance

In Version 2.1, the impact of the minority charge at the emitter periphery during large-signal switching on the lumped internal base resistance was taken into account by the equation

$$r^*_{Bi} = r_{Bi}\frac{\Delta Q_i}{\Delta Q_p} = r_{Bi}\frac{\Delta Q_i}{\Delta Q_i + \Delta Q_{fp}}$$

with

$$\Delta Q_i = Q_{jEi} + Q_{jCi} + Q_{fi}$$

For the case of a large negative BC voltage and a low forward BE voltage

$$\Delta Q_i = Q_{jEi} + Q_{jCi}$$

© 2023 Cadence Design Systems, Inc.

can become zero, causing a division by zero and a pole in the bias dependent r_{Bi} characteristic. Although this case is rare and is mostly likely caused by bad (non-physical) parameter combinations, it needs to be avoided under any circumstances. Therefore, to ensure numerical stability Q_{jCi} is dropped, leading to the modified formulation of the charge difference

$$\Delta Q_i = Q_{jEi} + Q_{fi}$$

In the corresponding small-signal equation,

$$r^*_{Bi} = r_{Bi}\frac{C_i}{C_i + C_{dEp}}$$

the internal capacitance has also to be modified to

$$C_i = C_{jEi} + C_{dEi}$$

Another change of the formulation for the internal base resistance is that the parameter KRBI is dropped. It was introduced about 10 years ago and intended to be used for changing during h.f. noise analysis due to the many uncertainties in bipolar transistor noise mechanisms and theory. With a better understanding of noise in bipolar transistors and many experimental investigations performed recently for advanced processes, this empirical parameter does not seem to be required anymore.

Base-emitter Tunnelling Component

Location of the Current Source

$$i_{BEt} = I_{BEtS}(-V_e)C_e^{\,1-1/z_g}\exp\left[-a_{BEt}C_e^{\,1/z_g-1}\right]$$

Temperature Dependence

$$I_{BEtS}(T) = I_{BEtS}(T_0)\sqrt{\frac{V_g(T_0)}{V_g(T)}}\left(\frac{V_{DE}(T)}{V_{DE}(T_0)}\right)^2\left(\frac{C_{jE0}(T)}{C_{jE0}(T_0)}\right)$$

© 2023 Cadence Design Systems, Inc.

$$a_{BEt}(T) = a_{BEt}(T_0)\left(\frac{V_g(T)}{V_g(T_0)}\right)^{3/2}\frac{V_{DE}(T_0)}{V_{DE}(T)}\frac{C_{jE0}(T_0)}{C_{jE0}(T)}$$

$$V_g(T) = V_{gBEeff}(T) = \frac{V_{gBeff}(0T) + V_{gEeff}(T)}{2}$$

Parasitic Base-Emitter Capacitance Partitioning

$$C_{BEpar} = C_{Eox} + C_{BE,\,metal}$$

$$f_{BEpar'} = \frac{C_{BEpar,\,2}}{C_{BEpar}} = \frac{C_{Eox,\,2} + C_{BE,\,metal}}{C_{Eox} + C_{BE,\,metal}}$$

Substrate Transistor

$$I_{TS}(T) = I_{TSS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{BCxT}}\exp\left[\frac{V_{gCeff}(0)}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$$

$$\tau_{Sf}(T) = \tau_{Sf}(T_0)\left(\frac{T}{T_0}\right)^{(\zeta_{Cx} - 1)}$$

Related Topics

Spectre HICUM Model Compared to Public HICUM Model

Model Description

HiCUM Model Version 2.3

Component Statements

HiCUM Model (bht)

© 2023 Cadence Design Systems, Inc.

HiCUM Model Version 2.3

HICUM/L2 version 2.30 has been developed to a large extent within the framework of the European DOTFIVE project. This HICUM/L2 version has been improved from its present official version (v2.24) in order to meet the requirements for emerging mm-wave applications. Following is a brief overview of the new improvements and additions in the new model.

Improvements in the model equations

Formulation for the critical current (ICK)

$$I_{ck} = \frac{V_{ceff}}{r_{ci0}} \frac{1}{\left(1+\left(\frac{V_{ceff}}{V_{lim}}\right)^{\delta_{ck}}\right)^{1\delta_{ck}}} \left[1+\frac{\chi+\sqrt{\chi^2-a_{ickpt}}}{2}\right]$$

where δ_{ck} is the new mode parameter.

Weight factors

Weight factor for low current transit time

A new weight factor hf0 for the low current minority charge has been introduced.

$$Q_{fT} = h_{f0}Q_{f0} + h_{fE}\Delta Q_{Ef} + \Delta Q_{Bf} + h_{fc}\Delta Q_{cf}$$

Note: The default value of hf0 (=1) makes it compatible with the previous version. The temperature dependence of hf0 is given by

$$h_{f0}(T) = h_{f0}(T_0)\exp\left[\frac{\Delta V_{gBE}}{V_T}\left(\frac{T}{T_0}-1\right)\right]$$

© 2023 Cadence Design Systems, Inc.

where, ΔVgBE is the new model parameter and defined as the bandgap difference between base and BE-junction, used for hjEi0 and hf0.

Weight factor of BE depletion charge

In this version, the BE-depletion charge weight factor hjEi is modeled as bias dependent with the following equations:

$$h_{jEi} = h_{jEi0}\frac{\exp(u)-1}{1}$$

With,

$$u = a_{hjEi}\left(1-\left(1-\frac{V_j}{V_{DEi}}\right)^{Z_{Ei}}\right)$$

Where, ahjEi is the new model parameter.

The junction voltage is limited to V_{DEi} and 0 by:

$$\chi_{upp} = \frac{V_{DEi}-V_{BEi}}{r_{h_{jEi}}V_t}$$

and

$$V_{j,\,upp} = V_{DEi} - r_{h_{jEi}}V_T\frac{\chi_{upp}+\sqrt{\chi^2{}_{upp}-a_{fi}}}{2}$$

where, rhjEi is the newly introduced model parameter.

The voltage has been further limited to values greater than zero using the following equations:

$$\chi_{low} = \frac{v_{j,\,upp}-V_T}{V_T}$$

© 2023 Cadence Design Systems, Inc.

$$v_j = V_T\left(1 + \frac{\chi_{low} + \sqrt{\chi^2_{low} + a_{fi}}}{2}\right)$$

The temperature dependence of h_{JEi} and r_{hjEi} is given by:

$$a_{hjEi}(T) = a_{hjEi}(T_0)\left(\frac{T}{T_0}\right)^{\xi_{h_{jEi}}}$$

$$h_{jEi0}(T) = h_{jEi}(T_0)\exp\left[\left(-\frac{\Delta V_{gBe}}{V_T}\right)\left(\left(\frac{T}{T_0}\right)^{\zeta_{VgBE}} - 1\right)\right]$$

Where,

ζ_{hjEi} and ζ_{VgBE} are the fitting parameters.

High current weight factors

Temperature dependences for hfE and hfC have been considered in the new model.

$$h_{fE}(T) = h_{fE}(T_0)\exp\left[\frac{V_{gb} - V_{ge}}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$$

$$h_{fc}(T) = h_{fc}(T_0)\exp\left[\frac{V_{gb} - V_{gc}}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$$

To enable full backward compatibility to previous versions of HICUM, the parameter `flcomp` needs to be set to 2.3, or more to turn on these models.

© 2023 Cadence Design Systems, Inc.

Transit Times

Barrier voltage

The barrier related term is calculated by the bias dependent barrier voltage:

$$\Delta V_{cBar} = V_{cBar}\exp\left(-\frac{2}{i_{Bar}+\sqrt{i^2_{Bar}+a_{cBar}}}\right)$$

$$i_{Bar} = \frac{i_{Tf}-I_{CK}}{i_{cBar}}$$

Barrier related minority charge

The high current minority charge expression has been extended by adding the barrier related part:

$$Q_{f,h} = \Delta Q_{Ef}+\Delta Q_{Bf,b}+\Delta Q_{Bf,c}+\Delta Q_{cf,c}$$

The new formulation for the barrier related minority charge reads as follows:

$$\Delta Q_{Bf,b} = \tau_{Bfvs} i_{Tf}\left[\exp\left(\frac{\Delta V_{cBar}}{V_T}\right)-1\right]$$

With the already existing parameter:

$$\tau_{Bfvs} = (1-f_{\tau hc})\tau_{hCs}$$

High current charges

Considering the “Kirk effect” the following expression can be obtained:

$$\Delta Q_{f_{h,c}} = \tau_{hCs} i_{Tf} w^2 \exp\left(\frac{\Delta V_{cBar}-V_{cBar}}{V_T}\right)$$

© 2023 Cadence Design Systems, Inc.

The high current collector charge including current spreading can be expressed as:

$$\Delta Q_{Cf,\,c} \;=\; \tau_{pCs} i_{Tf} \exp\left(\frac{\Delta V_{cBar} - V_{cBar}}{V_T}\right) \begin{cases} 2\dfrac{f_{Ci} ln\left(\dfrac{1+\zeta_b w}{1+\zeta_l w}\right) - f_{Cb} + f_{Cl}}{\zeta_b - \zeta_l} & l_{E0} > b_{E0} \\ \dfrac{1+\zeta_{bw/3}}{1+\zeta_b w} w^2 & l_{E0} \;=\; b_{E0} \end{cases}$$

Emitter transit time

The temperature dependence of the emitter transit time has been removed. However, by setting `flcomp` to 2.2 or lower, the former existing equation will still be available.

Lateral non-quasi-static (NQS) effect

The formulation has been switched back to that of HICUM/L2 version 2.23.

Temperature dependence of thermal resistance

In this version, the thermal resistance (Rth) has been modeled as temperature dependent.

$$R_{th}(T) \;=\; R_{th}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{rth}}$$

where, ζ_{rth} is the temperature coefficient of Rth and a new model parameter.

Temperature dependence of internal BE recombination current

The current equation has been modified, within the existing simplifying assumptions, by replacing “1/2” with “1/m_{REi}”

$$I_{REiS}(T) \;=\; I_{REiS}(T0)\left(\frac{T}{T_0}\right)^{\frac{m_g}{m_{REi}}} \exp\left[\frac{1}{m_{REi}} \cdot \frac{V_{gBEeff}}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$$

© 2023 Cadence Design Systems, Inc.

Temperature dependence of peripheral BE recombination current

In the same way the with peripheral BE recombination current has been modified:

$$I_{REpS}(T) = I_{REpS}(T0)\left(\frac{T}{T_0}\right)^{\frac{m_g}{m_{REp}}} \exp\left[\frac{1}{m_{REp}} \cdot \frac{V_{gBEeff}}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$$

Note: Setting mREi =2 and mREp=2 yields the formulation of previous model versions.

Noise source of the emitter resistance

Based on measurements presented in an additional flicker noise contribution has been introduced for the series emitter resistance RE. The total noise contribution becomes:

$$\overline{I^2_{rE}} = \frac{Kf_{rE} \cdot T_E^{Af_{rE}}}{f} + \frac{4KT}{r_E}$$

where, the first component represents the flicker noise and second the thermal noise.

Related Topics

Spectre HICUM Model Compared to Public HICUM Model

Model Description

HiCUM Model Version 2.2

HiCUM Model Version 2.3

Component Statements

HiCUM Model (bht)

© 2023 Cadence Design Systems, Inc.

HiCUM Model Version 2.31

Improvements in Model Equations

Temperature Dependence of Thermal Resistance

In this version, the temperature dependence of thermal resistance (R_{th}) has been changed as follows:

$$R_{th}(T) = R_{th}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{rth}}(1 + alrth \cdot \Delta t)$$

Lateral Non-Quasi-Static (NQS) Effect

In this version, the lateral NQS modeling has been simplified to reduce the number of calculated derivatives.

$$Cdei = T(f0) \cdot itf / V_t$$
$$Cdci = tr \cdot itr / V_t$$

Vertical NQS Effect Parameters

The default value of the vertical NQS effect parameters has been changed as follows:

$$alqf = 0.167$$
$$alit = 0.333$$

Noise Correlation

A new noise correlation model has been introduced, which is valid at all frequencies.

Related Topics

Spectre HICUM Model Compared to Public HICUM Model

© 2023 Cadence Design Systems, Inc.

HiCUM Model Version 2.3

HiCUM Model Version 2.32

HiCUM Model Version 2.33

HiCUM Model Version 2.34

HiCUM Model Version 2.40

Component Statements

HiCUM Model (bht)

HiCUM Model Version 2.32

Improvements in Model Equations

The conditional statement for the barrier term has been changed to transistor-specific values. The original conditional statement `if(icbar<1e-10)` has been changed to `if(icbar<0.05*(vlim/rci0))` where `vlim/rci0` is a rough bias and temperature-independent estimation of `ICK`.

Related Topics

Spectre HICUM Model Compared to Public HICUM Model

HiCUM Model Version 2.3

HiCUM Model Version 2.31

HiCUM Model Version 2.33

HiCUM Model Version 2.34

HiCUM Model Version 2.40

Component Statements

HiCUM Model (bht)

© 2023 Cadence Design Systems, Inc.

HiCUM Model Version 2.33

Following updates have been made in Version 2.33:

- Two operating point values `TK` and `DTSH` have been added.
  - `TK` - actual device temperature in Kelvin
  - `DTSH` - temperature increase due to self heating
- Bugs related to `white_noise` have been fixed.
- Code for tunneling current blocks has been optimized.

elated Topics

Spectre HICUM Model Compared to Public HICUM Model

HiCUM Model Version 2.3

HiCUM Model Version 2.31

HiCUM Model Version 2.32

HiCUM Model Version 2.34

HiCUM Model Version 2.40

Component Statements

HiCUM Model (bht)

HiCUM Model Version 2.34

Following updates have been made in Version 2.34:

- Branch added from Substrate to Collect.
- Five new model parameters, `cscp0`, `vdsp`, `zsp`, `vptsp`, and `aick` added.
- Bug related to avalanche breakdown fixed.
- Range of depletion capacitance grading factors changed to exclude 1.0. It applies to all grading factors: zEi, zEp, zCi, zCx, zS, and zSp.

© 2023 Cadence Design Systems, Inc.

- Code for critical current, depletion capacitance, and noise correlation evaluation optimized.

elated Topics

Spectre HICUM Model Compared to Public HICUM Model

HiCUM Model Version 2.3

HiCUM Model Version 2.31

HiCUM Model Version 2.33

HiCUM Model Version 2.32

HiCUM Model Version 2.40

Component Statements

HiCUM Model (bht)

HiCUM Model Version 2.40

Following updates have been made in Version 2.40:

- New CMC model versioning policy is adopted:

  <*version #*>.<*subversion #*>.<*revision#*>
- Improvised collector avalanche equation
- Backward compatibility and application
- Introduction of conditional statement for weak avalanche breakdown
- Addition of `Gmin` for operating point values
- Renamed the operating point value names of resistance, `RE` and `RCX` by `re_t` and `rcx_t`
- Improvised calculation of `Vciei`

Improvised Strong Collector Avalanche Formula

The new formulation for strong collector avalanche breakdown is given by:

© 2023 Cadence Design Systems, Inc.

$$I_{AVL} = I_T \frac{f_{AVL}(V_{DCi} - V_{B'C'})\exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - V_{B'C'})}\right)}{1 - f_{AVL}(V_{DCi} - V_{B'C'})\exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - V_{B'C'})}\right)}$$

Formula based on weak avalanche:

$$I_{AVL}^{weak} = I_T g$$

$$I_{AVL} = I_T \frac{g}{1 - k_{AVL} g}$$

With addition parameter α_{KAV}, `kAVL` is modeled temperature dependent by:

$$k_{AVL}(T) = k_{AVL}(T_0)\exp(\alpha_{KAV}\Delta T)$$

With the smoothening model parameter a_{AVL} fixed to 0.01, the denominator $1 - k_{AVL} g$ is limited to values greater than zero by the smoothening function:

$$h_1 = \frac{(1 - k_{AVL} g) + \sqrt{(1 - k_{AVL} g)^2 + a_{AVL}}}{2}$$

Parameter Extraction

You can extract `kAVL` as:

$$k_{AVL}(T) = k_{AVL}(T_0)\exp(\alpha_{KAV}\Delta T)$$

Conditional Statement for Weak Avalanche

Improvised conditional statement based on based on `favl` and `cjci0` and not `favl_t` and `cjci0_t`:

```
if ((favl > 0.0) && (cjci0 > 0.0)) begin
use_aval = 1;
```


© 2023 Cadence Design Systems, Inc.

```
end else begin
use_aval = 0;
iavl = 0.0;
end
```

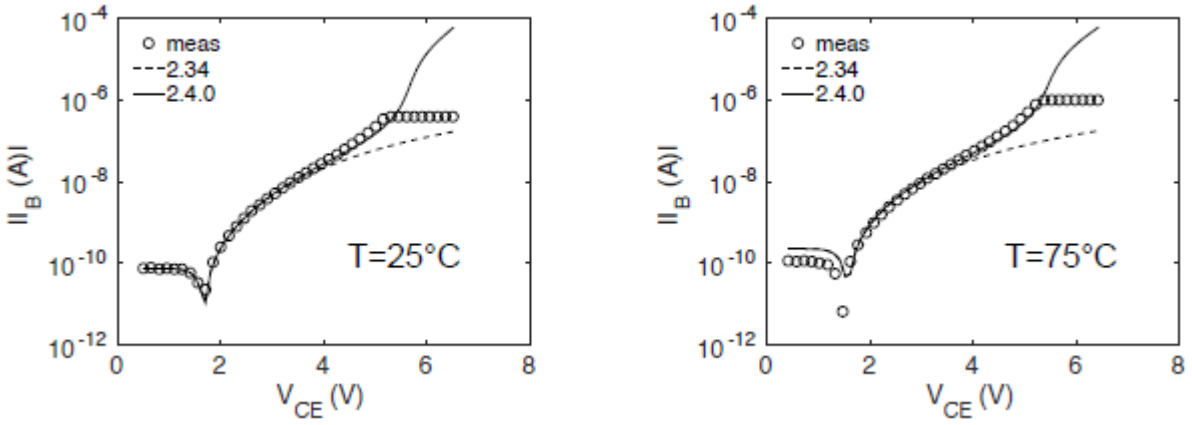
Usage of an integer flag results in faster evaluation of the if-statement:

```
if(use_aval == 1) begin : HICAVL
```

Setting `iavl = 0.0` during model initialization avoids the additional else block for this if-statement.

Backward Compatibility and Application

- Extension is completely compatible to previous HICUM versions.
- Values for weak avalanche model parameters `fAVL` and `qAVL` can be re-used to extend existing model cards by the new feature.
- Application of experimental data:
  - `favl` and `qavl` are used for 2.34 and 2.4.0
  - New parameters: `kavl = 0.088` and `alkav=0.0037`



Improvised Vciei Calculation

For model compilers with derivatives based on branches, variables for the high-current region dependent on four branches, `bi,ei`, `bi,ci`, `ci,ei`, and `t,gnd`, Vciei will be calculated as:

```
Vciei = Vbiei-Vbici
```

This calculation removes the dependence on the `ci,ei` branch and reduces number of derivatives for each variable to three.

© 2023 Cadence Design Systems, Inc.

Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem) on page 286.

elated Topics

Spectre HICUM Model Compared to Public HICUM Model

HiCUM Model Version 2.3

HiCUM Model Version 2.31

HiCUM Model Version 2.32

HiCUM Model Version 2.33

HiCUM Model Version 2.34

HiCUM Model Version 2.40

HiCUM Model (bht)

Component Statements

Instance Definition

```
Name  c  b  e  [s]  [t] ModelName parameter=value ...
```

Specifying the substrate terminal is optional. If not provided, the substrate is connected to ground.

Specifying the thermal node (`t`) is optional. However, if it is specified then:

- When it is connected, it is parallel with the internal Rth/Cth
- When it is shorted to ground, it disables the self heating effect
- When it is kept floated, it uses the internal Rth/Cth and is equivalent to not being specified.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

Parameters valid for both modes

`region=fwd`	Estimated operating region. Possible values are `off`, `fwd`, `rev`, and `sat`.
`trise (C)`	Temperature rise from ambient.
`self_heating=yes`	Control switch for self-heating. The value `fast` is Cadence's proprietary approach that is significantly faster than the full self-heating and generates similar results in most cases. Possible values are `no`, `yes`, or `fast`.
`m=1`	Multiplicity factor (number of devices in parallel).

Parameters for structure mode

`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Structural parameters

`area=1`	Transistor area factor.

Model Definition

```
model modelName bht parameter=value ...
```

Model Parameters

Major mode of operation

`mode=internal`	Mode for model parameter determination. Possible values are `internal`.

© 2023 Cadence Design Systems, Inc.

Parameters for internal mode

Structural parameters

`type=npn`	Transistor type. Possible values are `pnp` and `npn`.
`latb=0.0`	Parameter for lateral scaling (Zeta_b).
`latl=0.0`	Parameter for lateral scaling (Zeta_l).

Internal transistor

`c10=2.0e-30 A`^{2}`s`	Constant for ICCR.
`qp0=2.0e-14 Coul`	Zero-bias hole charge.
`ich=infinity A`	High current correction (multidimensional ICCR).
`hjci=1.0`	B-C depletion charge weighting factor.
`hf0=1.0`	Weight factor for the low current minority charge.
`ahjei=0.0`	Parameter describing the slope of hjEi (VBE).
`rhjei=1.0`	Smoothing parameter for hjEi (VBE) at high voltage.
`hjei=1.0`	B-E depletion charge weighting factor.
`hjei0=1.0`	B-E depletion charge weighting factor in HBTs at VBE=0.
`mcf=1.0`	Forward non-ideality factor of Su transfer current.
`tsf=0.0 s`	Transit time (forward operation).
`hfc=1.0`	Collector minority charge weighting factor.
`hfe=1.0`	Emitter minority charge weighting factor.
`alit=0.0`	Factor for additional delay time of iT.
`cjei0=0.0 F`	Internal zero-bias BE depletion capacitance.
`vdei=0.9 V`	Internal BE built-in voltage.
`zei=0.5`	Internal BE depletion coefficient.
`aljei=2.5`	Maximum internal depletion capacitance divided by Cjei0.
`cjci0=0.0 F`	Internal zero-bias BC depletion capacitance.
`vdci=0.7 V`	Internal BC built-in voltage.

© 2023 Cadence Design Systems, Inc.

zci=0.4	Internal BC depletion coefficient.
vptci=infinity V	Punch-through voltage of internal BC junction.
t0=0.0 s	Time constant (low current densities).
dt0h=0.0 s	Time constant for base and BC space charge layer width modulation.
tbvl=0.0 s	Time constant for modeling carrier jam.
tef0=0.0 s	Neutral emitter storage time.
gtfe=1.0	Current dependence factor for TEF0.
thcs=0.0 s	Saturation time constant.
alhc=0.1	Smoothing facor for base and collector transit time.
fthc=0.0	Partitioning factor for base and collector portion.
vces=0.1 V	Internal CE saturation voltage.
vdck=0.0 V	Built-In B-C voltage including voltage drop in B and epi-b.l.
rci0=150.0 Ω	Low-field resistance of epitaxial collector.
vlim=0.5 V	Limitation voltage.
vpt=infinity V	Punch-through voltage. The default value is 100V since version 2.24.
tr=0.0 s	Ideal reverse transit time.
vcbar=0.0 V	Barrier voltage.
icbar=0.0 A	Normalization parameter.
acbar=0.01	Smoothing parameter for barrier voltage.
delck=2.0	Fitting factor for critical current.
alqf=0.0	Factor for additional delay time of minority charge.
ibeis=1.0e-18 A	Internal BE saturation current.
mbei=1.0	Internal BE non-ideality factor.
ireis=0.0 A	Internal BE saturation current (recombination).
mrei=2.0	Internal BE non-ideality factor (recombination).
ibcis=1.0e-16 A	Internal BC saturation current.
mbci=1.0	Internal BC non-ideality factor.

© 2023 Cadence Design Systems, Inc.

favl=0.0 1/V	Avalanche current factor.
qavl=0.0 Coul	Exponent factor for Avalanche current.
rbi0=0.0 Ω	Internal base resistance at zero-bias.
fdqr0=0.0	Correction factor for modulation.
fgeo=0.6557	Geometry factor for current crowding.
fqi=1.0	Ratio of internal to total minority charge.
fcrbi=0.0	Ratio of h.f. shunt to total internal capacitance.
dvgbe=0.0 V	Bandgap difference between B and B-E junction used for hjEi0 and hf0.
zetahjei=1.0	Temperature coefficient for ahjEi.
zetavgbe=1.0	Temperature coefficient for hjEi0.
zetarth=0.0 K/W	Temperature coefficient for Rth.
flcono=no	Flag for turning on/off correlated noise implementation. Possible values are `yes` and `no`.
alrth=0.0 1/K	First order relative TC of parameter Rth.

Peripheral elements

cjep0=0.0 F	Peripheral zero-bias BE depletion capacitance.
vdep=0.9 V	Peripheral BE built-in voltage.
zep=0.5	Peripheral BE depletion coefficient.
aljep=2.5	Maximum per. depl. cap. divided by Cjep0.
ibeps=0.0 A	Peripheral BE saturation current.
mbep=1.0	Peripheral BE non-ideality factor.
ireps=0.0 A	Peripheral BE saturation current (recomb.).
mrep=2.0	Peripheral BE non-ideality factor (recomb.).

© 2023 Cadence Design Systems, Inc.

External elements

`cjcx0=0.0 F`	External zero-bias BC depletion capacitance.
`vdcx=0.7 V`	External BC built-in voltage.
`zcx=0.4`	External BC depletion coefficient.
`vptcx=infinity V`	Punch-through voltage of external BC junction.
`ccox=0.0 F`	BC overlap capacitance.
`fbc=0.0`	Partitioning factor for Cjcx and Ccox over rBx.
`ibcxs=0.0 A`	External BC saturation current.
`mbcx=1.0`	External BC non-ideality factor.
`ceox=0.0 F`	Emitter oxide (overlap) capacitance.
`rbx=0.0 Ω`	External base series resistance.
`re=0.0 Ω`	Emitter series resistance.
`rcx=0.0 Ω`	External collector series resistance.

Substrate transistor

`cjs0=0.0 F`	Zero-bias CS depletion capacitance.
`vds=0.6 V`	CS built-in voltage.
`zs=0.5`	CS depletion coefficient.
`vpts=infinity V`	Punch-through voltage of CS junction.
`rsu=0.0 Ω`	Substrate resistance.
`csu=0.0 F`	Substrate coupling capacitance.
`iscs=0.0 A`	CS diode saturation current.
`msc=1.0`	CS diode non-ideality factor.
`itss=0.0 A`	Transfer saturation current of Su transistor.
`msf=1.0`	Forward non-ideality factor of Su transfer current.
`msr=1.0`	Reverse non-ideality factor of Su transfer current.
`ibets=0.0 A`	BE tunneling saturation current.

© 2023 Cadence Design Systems, Inc.

`abet=40.0`	BE tunneling factor.

Noise parameters

`kf=0.0`	Flicker noise factor.
`af=2.0`	Flicker noise exponent factor.
`krbi=1.0`	Noise factor for internal base resistance.
`kfre=0.0`	Emitter resistance flicker noise coefficient.
`afre=2.0`	Emitter resistance flicker noise exponent facto.

Temperature effect parameters

`tnom (C)`	Parameters measurement temperature. Default set by options.
`vgb=1.17 V`	Bandgap-voltage.
`alb=5.0e-3 1/K`	Relative temperature coefficient of current gain.
`alfav=0.0 1/K`	Temperature coefficient for FAVL.
`alqav=0.0 1/K`	Temperature coefficient for QAVL.
`zetaci=0.0`	Temperature coefficient (mobility) for epi-collector.
`alvs=0.0 1/K`	Relative temperature coefficient of saturation drift velocity.
`alces=0.0 1/K`	Relative temperature coeff. of VCEs.
`aldck=0.0 1/K`	Relative TC of VDCK.
`zetarbi=0.0`	Temperature coefficient (mobility) for internal base resistance.
`zetarbx=0.0`	Temperature coefficient (mobility) for external base resistance.
`zetarcx=0.0`	Temperature coefficient (mobility) for external collector resistance.
`zetare=0.0`	Temperature coefficient (mobility) for emitter resistance.
`alt0=0.0 1/K`	Frist-order temperature coefficient of temperature T0.

© 2023 Cadence Design Systems, Inc.

`kt0=0.0`	Second-order temperature coefficient of temperature T0.
`rth=0.0 K/W`	Thermal resistance for self-heating.
`cth=0.0 J/K`	Thermal capacitance for self-heating.
`version=2.1`	The available versions are 1.0, 2.1, 2.20, 2.21, 2.22, 2.23, 2.24, 2.30, 2.31, 2.32, 2.33, 2.34, 2.40 and 3.00.

Operating region warning control parameters

`updatelevel=2.0`	Model update selector. The available versions are 0, 1 ,2 and 3. updatelevel = 0 : This level is compatible with the original HICUM Fortran code. Temperature dependence is ignored.Not suggested to use this level for convergence issue; updatelevel = 1 OR 2 : This level has better temperature dependence. It includes some fixes and enhancements. Version 1.0, 2.1, 2.21, and 2.22 support this level; updatelevel = 3 : This level has complete derivatives for current and charge model. The simulation result is fully compatible with HICUM Verilog-A model. Version 2.1, 2.20, 2.22, 2.23, 2.24, 2.30, 2.31, 2.32, 2.33, and 2.34 support this level.
`minr=0.001 Ω`	Minimum resistance.
`imax=1e3`	Maximum current.
`tmax=500 K`	Maximum device temperature.
`tmin=200 K`	Minimum device temperature.
`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `fwd`, `rev`, and `sat`.

DC-mismatch model parameters

`mvt0=0.0 V`	Threshold mismatch intercept.

© 2023 Cadence Design Systems, Inc.

Formally released Hicum 2.2 new parameters

`vgc=1.17 V`	Effective collector bandgap voltage.
`vge=1.17 V`	Effective emitter bandgap voltage.
`vgs=1.17 V`	Effective substrate bandgap voltage.
`zetact=3.0`	Exponent coefficient in transfer current temperature dependence.
`zetabet=3.5`	Exponent coefficient in B-E junction current temperature dependence.
`tbhrec=0.0 s`	Base current recombination time constant at B-C barrier for high forward injection.
`tunode=1`	Specifies the base node connection for the tunneling current, possible value are 0 and 1, 1 signifies perimeter node.
`cbepar=0.0 F`	Total parasitic B-E capacitance.
`fbepar=1.0`	Partitioning factor of parasitic B-E capacitance.
`f1vg=-1.02377e-4`	Coefficient K1 in T-dependent band-gap equation.
`f2vg=4.3215e-4`	Coefficient K2 in T-dependent band-gap equation.
`cfbe=-1`	Flag for determining where to tag the flicker noise source, Possible values are -1 and -2.
`zetacx=1.0`	Temperature exponent of mobility in substrate transistor transit time.
`cbcpar=0.0 F`	Total parasitic B-C capacitance.
`fbcpar=0.0`	Partitioning factor of parasitic B-C capacitance.
`ajei=2.5`	Ratio of maximum to zero-bias value of internal B-E capacitance.
`ajep=2.5`	Ratio of maximum to zero-bias value of peripheral B-E capacitance.
`ahc=0.1`	Smoothing factor for current dependence of base and collector transit time.
`flsh=1`	Flag for turning on/off self-heating effect. Possible values are 0, 1, and 2. 0 refers to turn off, 1 refers to partial turn on, and 2 refer to full selfheating.
`flcomp=0.0`	Flag for compatibility with v2.1 model (0=v2.1).

© 2023 Cadence Design Systems, Inc.

`flnqs=1`	Flag for allowing to turn on(1) or off(0) NQS effect in a given model parameter set, that included non-zero values for alit and alqf.
`cornoise_flag=no`	Flag for turning on/off corelated noise implementation. This parameter is an alias of `flcono`. Possible values are `yes` and `no`.
`compatible=spectre`	Compatiblity parameter. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`cscp=0.0 F`	Perimeter S-C zero-bias depletion capacitance.
`vdsp=0.6 V`	Perimeter S-C built-in potential.
`zsp=0.5`	Perimeter S-C grading coefficient.
`vptsp=100 V`	Perimeter S-C punch-through voltage.
`aick=1e-3`	Smoothing term for ICK.
`kavl=0.0`	Flag/factor for turning strong avalanche on.
`alkav=0.0 1/K`	Relative TC for KAVL.
`hcavl=0.0`	Factor for current dependent avalanche effect.
`hvdavl=0.0`	Ilim dependence for spatially varying collector doping.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`region=fwd`	Estimated operating region. Possible values are `off`, `fwd`, `rev`, and `sat`.
`temp (C)`	Temperature.
`tk (K)`	Temperature in Kelvin.
`dtsh (C)`	Temperature rise due to selfheating.

© 2023 Cadence Design Systems, Inc.

`ic (A)`	Collector current.
`ib (A)`	Base current.
`vbei (V)`	Internal base-emitter voltage.
`qjei (Coul)`	Internal base-emitter space charge.
`cjei (F)`	Internal base-emitter depletion capacitance.
`vbep (V)`	Peripheral base-emitter voltage.
`qjep (Coul)`	Peripheral base-emitter space charge.
`cjep (F)`	Peripheral base-emitter depletion capacitance.
`vbci (V)`	Internal base-collector voltage.
`qjci (Coul)`	Internal base-collector space charge.
`cjci (F)`	Internal base-collector depletion capacitance.
`vbcp (V)`	Voltage between Per_B and internal C.
`qjcp (Coul)`	Charge related to Cjcp capacitance.
`cjcp (F)`	Capacitance between Per_B and internal C.
`vbcx (V)`	Voltage between external B and internal C.
`qjcx (Coul)`	Charge on capacitance Cjcx.
`cjcx (F)`	Capacitance between external B and internal C.
`vsc (V)`	Voltage between internal S and internal C.
`qjs (Coul)`	Substrate space charge.
`cjs (F)`	Substrate capacitance.
`qdsu (Coul)`	Substrate diffusion charge.
`cdsu (F)`	Substrate diffusion capacitance.
`vcei (V)`	Internal collector emitter voltage.
`tf (s)`	Transit Time.
`qf (Coul)`	Minority charge.
`qdei (Coul)`	Internal base-emitter diffusion charge.
`cdei (F)`	Internal base-emitter diffusion capacitance.
`qdci (Coul)`	Internal base-collector diffusion charge.
`cdci (F)`	Internal base-collector diffusion capacitance.

© 2023 Cadence Design Systems, Inc.

qp (Coul)	Hole charge.
it (A)	Transfer current.
itf (A)	Transfer current.
itr (A)	Transfer current.
ibet (A)	Tunneling current.
gm (S)	Common-emitter transconductance.
si (S)	Common emitter output conductance.
sfb	Sfb variable.
srb	Srb variable.
sfc	Sfc variable.
src	Src variable.
rbi (Ω)	Internal base resistance.
rbx (Ω)	External base resistance.
rcx (Ω)	External collector resistance.
re (Ω)	Re variable.
rsu (Ω)	External collector resistance.
is (A)	Substrate current.
ft (Hz)	Unity small-signal current-gain frequency.
pwr (W)	Power dissipation.
iavl (A)	Avalanche current.
ibei (A)	Internal BE current.
ibci (A)	Internal BC current.
ibep (A)	Peripheral BE current.
ijbcx (A)	External BC junction current.
ijsc (A)	SC junction current.
ieei (A)	Current from internal E to external E.
ie (A)	Current flow through terminal E.
cbe (F)	BE capacitance.
cbc (F)	BC capacitance.

© 2023 Cadence Design Systems, Inc.

betar (A/A)	Common collector current gain.
beta (A/A)	Common emitter current gain.
betadc (A/A)	Common emitter current gain. The alias is beta.
betaac	Small signal current gain.
gmavl (S)	Transconductance for avalanche current.
gms (S)	Transconductance of the parasitic substrate PNP.
rpii (Ω)	Intrinsic input resistance.
rpix (Ω)	Extrinsic input resistance.
rmui (Ω)	Intrinsic feedback resistance.
rmux (Ω)	Extrinsic feedback resistance.
rmus (Ω)	Intrinsic substrate feedback resistance.
ro (Ω)	Output resistance.
ros (Ω)	Output resistance for the parasitic substrate PNP.
cpii (F)	Total intrinsic BE capacitance.
cpix (F)	Total extrinsic BE capacitance.
cmui (F)	Total intrinsic BC capacitance.
cmux (F)	Total extrinsic BC capacitance.
ccs (F)	CS junction capacitance.
crbi (F)	Shunt capacitance across RBI.
vef (V)	Effective Forward Early voltage.
ver (V)	Effective Inverse Early voltage.
vbe (V)	External BE voltage.
vbc (V)	External BC voltage.
vce (V)	External CE voltage.
gmi (S)	Internal transconductance, alias of gm.
roi (Ω)	Output resistance.
rb (Ω)	Total base resistance as calculated in the model.

© 2023 Cadence Design Systems, Inc.

Related Topics

Spectre HICUM Model Compared to Public HICUM Model

HiCUM Model Version 2.3

HiCUM Model Version 2.31

HiCUM Model Version 2.32

HiCUM Model Version 2.33

HiCUM Model Version 2.34

HiCUM Model Version 2.40

HiCUM Model (bht)

© 2023 Cadence Design Systems, Inc.

7

HiCUM Level-0 Model (bht0)

The HiCUM Level0 model was developed by Professor M. Schroter. It combines the simplicity of the Spice Gummel Poon Model (SGPM) in terms of equivalent circuit and some of its model equations with several important features of HiCUM Level2. As a result, BHT0 is a more physics-based and accurate model than the SGPM and also reduces parameter extraction efforts, especially for single transistor sizes, compared to HiCUM Level2 and SGPM. The latest version of this model is 1.32, and all of previous versions are supported with setting model parameter VERSION.

Click to view the following information about the BHT0 model:

- Model Version Updates
- Equivalent Circuit
- Charge formulation of the internal transistor
- Derivation of the simplified transfer current equation
- Static Base Current Components
- Depletion Charges And Capacitances
- Minority Charges And Capacitances
- Series Resistance
- Temperature Dependence
- Noise Model
- Charge Storage Elements
- Series Resistance
- Temperature Effects
- Models and Equations in Version 1.30
- Component Statements

© 2023 Cadence Design Systems, Inc.

Model Version Updates

Version 1.2:

- Upper limit of the model parameter FGEO is now infinity.
- Four or five terminals can be used with the latest version model, corresponding "tnode" is set as internal or external.
- Flag FLSH introduced for controlling self-heating calculation.
- All series resistors and RTH are limited to a minimum value.
- ddx() operator used with QJMOD and QJMODF wherever required.
- Substrate transistor transfer current has been added.
- Hyperbolic smoothing is used in rbi computation to a void divide-by-zero.

Version 1.3

- Modification done at TUD: Third order polynomial is solved for transfer current. It can be turned on by setting `IT_MOD=1`.
- Added voltage dependent Reverse Early voltage. Parameter `aver` describes voltage dependence.
- Parameters `ZETAVER`, `ZETAVGBE`, `VGBE` describe temperature dependence of `VER` and `IQF`.
- Added temperature dependence for `IQFH` and `TFH`. `ALIQFH` and `KIQFH` are used to model a second order temperature model. Parameter `TEF_TEMP=0` turns off the temperature dependence for `TEF0`.
- Corrected SPICE name for `AHQ` and `ZETAIQF`. The original name is `AHQX` and `ZETIQF`, which are also valid aliases.
- Implemented a `gmin` between nodes `CI` and `EI`.
- `qj` is now limited to positive values to improve convergence at negative bias.
- Resolved a convergence issue for cc a calculation of voltage dependence of t0

Version 1.3.1

- NQS effects have been added and can be activated by using the flag FLNQS=1.

© 2023 Cadence Design Systems, Inc.

- Some operating point outputs have been added to the Va code.

Version 1.3.2

- A new parameter `type` has been implemented to specify the transistor type. This parameter replaces the `pnp` and `npn` model parameters, which are not supported in version 1.32. In addition, the `type` parameter is not supported in previous versions.
- While lodading the parasitic substrate transistor transfer current, the current is multiplied by type in version 1.32.

Related Topics

Equivalent Circuit

Charge formulation of the internal transistor

HiCUM Level-0 Model (bht0)

© 2023 Cadence Design Systems, Inc.

Equivalent Circuit

Figure 7-1 Large signal equivalent circuit of the simplified HICUM version, HICUM/L0

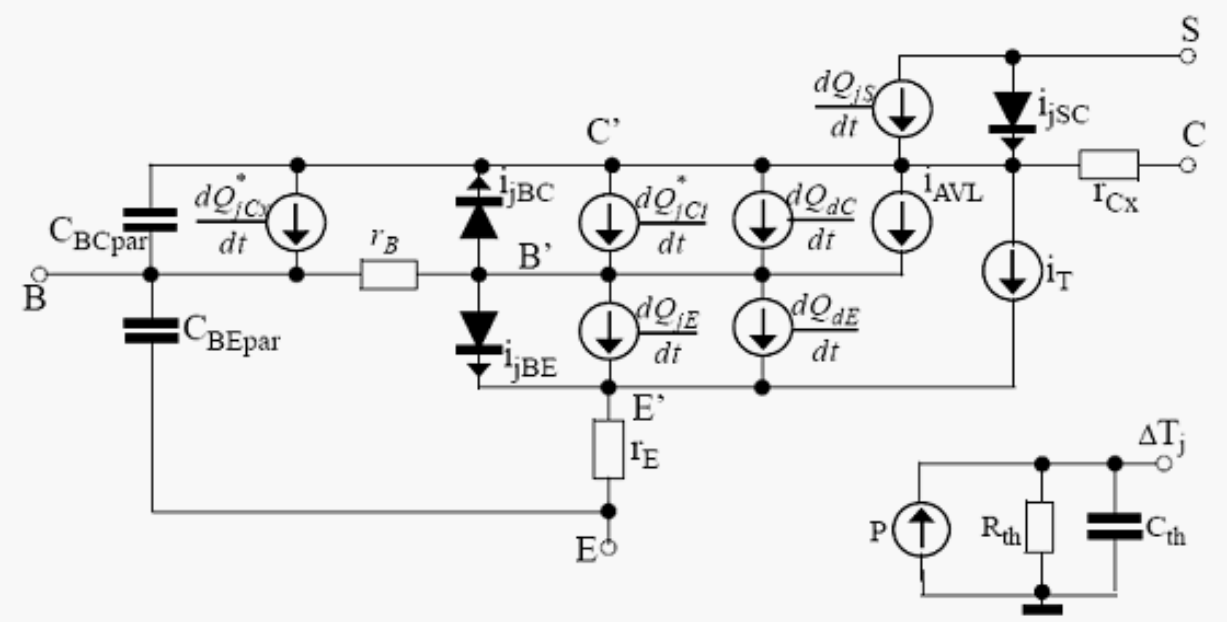
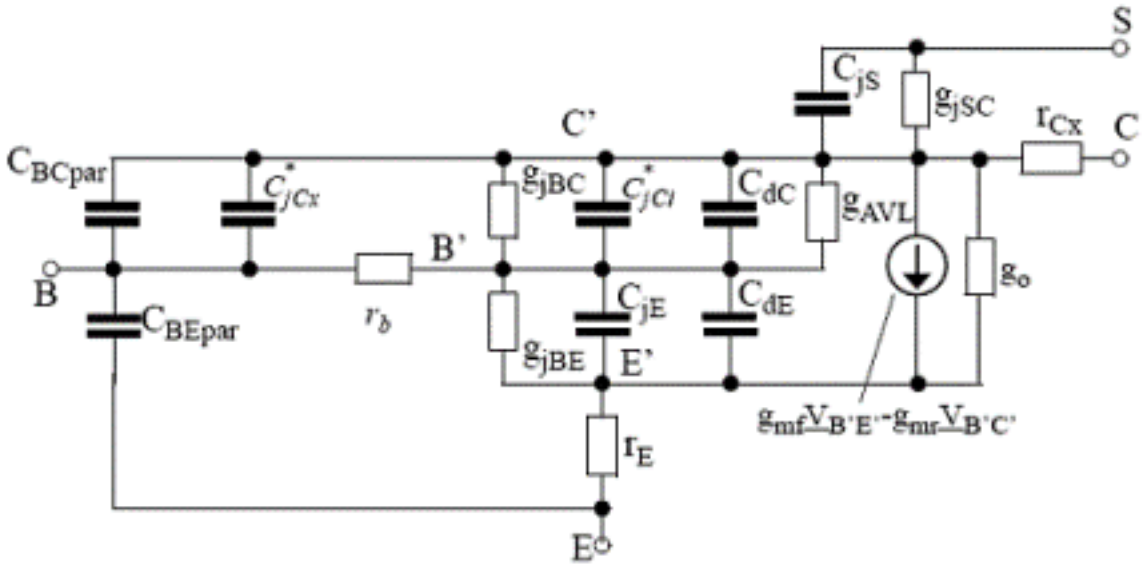
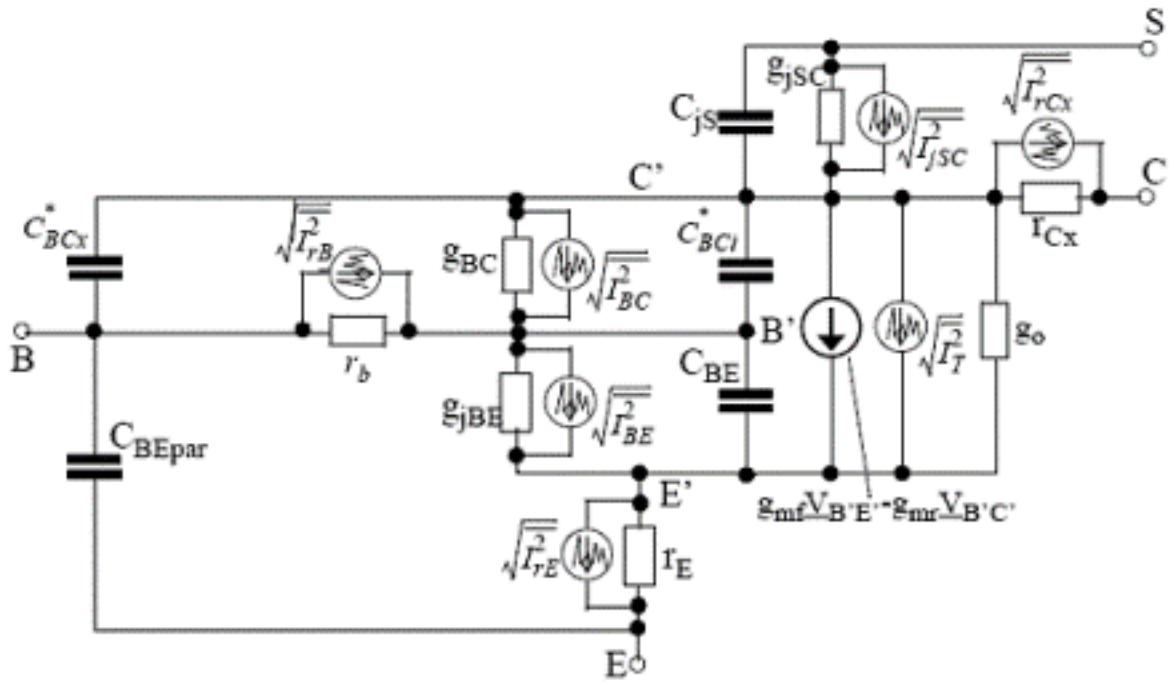


Figure 7-2 Small signal equivalent circuit of HICUM/L0



© 2023 Cadence Design Systems, Inc.

Figure 7-3 Small signal noise equivalent circuit of HICUM/L0 showing the noise sources with their RMS values used in a circuit simulator



Charge formulation of the internal transistor

All depletion charges and capacitances are described with the same equations as HICUM/L2. The formulation of forward minority charge Q_f is strongly based on the accurate description of the transit time τ_f. Like in HICUM/L2, the bias dependent of τ_f is modeled as

$$\tau = \tau_{f0}(v_{B'C'}) + \Delta\tau_{f0}(i_{Tf}, v_{C'E'})$$

© 2023 Cadence Design Systems, Inc.

with the low current component τ_{f0}, the high-current component $\Delta\tau_f$ and the i_{tf} as the forward transfer current. The formulation of τ_{f0} is same as in HICUM/L2.

$$\Delta\tau_f = \left(\tau_{hcs} w^2 \left(1 + \frac{2I_{CK}}{i_{Tf}\sqrt{\left(1 - \frac{I_{CK}}{i_{Tf}}\right)^2 + a_{hc}}} \right) + \tau_{fE0}\left(\frac{i_{Tf}}{I_{CK}}\right)^{g\tau E} \right) .$$

The minority charge Q_f used for dynamic transistor operation is then obtained analytically by integrating τ_f over i_{tf}.

$$Q_f = (\tau_{f0} i_{Tf} + \Delta Q_f) ,$$

Derivation of the simplified transfer current equation

$$i_T = \frac{c_{10}}{Q_{p,T}}\left[\exp\left(\frac{v_{B'E'}}{V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right)\right] ,$$

The derivation starts with the transport related charge for low bias:

$$Q_{p,T} = Q_{p0} + h_{jei}Q_{jEi} + h_{jci}Q_{jCi} = Q_{p0} + h_{jei}(Q_{jEi,op} + \Delta Q_{jEi}) + h_{jci}Q_{jCi} .$$

$$Q^*_{p0} = Q_{p0} + h_{jei}Q_{jEi,op} .$$

$$\frac{Q_{p,T}}{Q^*_{p0}} = 1 + \frac{h_{jei}\Delta Q_{jEi}}{Q^*_{p0}} + \frac{h_{jci}Q_{jCi}}{Q^*_{p0}} + \frac{Q_{f,T}}{Q^*_{p0}} + \frac{Q_{r,T}}{Q^*_{p0}}$$

© 2023 Cadence Design Systems, Inc.

The resulting transfer current expression reads

$$i_{Tf} = \frac{I_S^*}{Q_{p,I}/Q_{p0}^*}\exp\left(\frac{v_{B'E'}}{V_T}\right) ,$$

with a modified saturation current

$$I_S^* = c_{10}/Q_{p0}^* .$$

The forward transfer current equation can be written in a more familiar form:

$$i_{Tf} = \frac{I_S^*}{1+\frac{h_{jci}Q_{jCt}}{Q_{p0}^*}+\frac{Q_{f,I}}{Q_{p0}^*}+\frac{Q_{r,I}}{Q_{p0}^*}}\exp\left(\frac{v_{B'E'}}{m_{Cf}V_T}\right) .$$

Where

$$m_{Cf} = \frac{i_{Tf}/V_T}{g_m} \cong \left(1-\frac{h_{jei}C_{jEt,op}V_T}{Q_{p0}^*}\right)^{-1} \cong 1+\frac{h_{jei}C_{jEt,op}V_T}{Q_{p0}^*} ,$$

the low-current transconductance at the selected bias point $V_{B'E',op}$ is given by

$$g_m = \frac{di_{Tf}}{dv_{B'E'}} \cong i_{Tf}\left(\frac{1}{V_T}-\frac{h_{jei}C_{jEt,op}}{Q_{p0}^*}\right) = \frac{i_{Tf}}{V_T}\left(1-\frac{h_{jei}C_{jEt,op}V_T}{Q_{p0}^*}\right) .$$

© 2023 Cadence Design Systems, Inc.

The artificial Early Voltage is defined as:

$$V_{Ef} = \frac{Q^{*}_{p0}}{h_{jci} C_{jCi0}} \quad .$$

The critical (or knee) current of the D.C. forward transfer curve is defined as:

$$I_{Qf} = Q^{*}_{p0} / \tau_{f0} (v_{B'C'} = 0)$$

$$I_{Qr} = Q^{*}_{p0} / \tau_{f}$$

Quadratic equation for normalized charge:

$$q_{p,T} = \underbrace{1 + \frac{q_{jCi}}{V_{Ef}}}_{q_j} + \underbrace{\left(\frac{i_{Tfi}}{I_{Qf}} + \frac{i_{Tri}}{I_{Qr}} \right)}_{q_m} \cdot \frac{1}{q_{p,T}} \quad .$$

The final formulation for the HICUM/L0 transfer current components:

$$\boxed{i_{Tf} = \frac{i_{Tfi}}{1 + \frac{\Delta q_{fh}}{q_{p,T}}}} \quad \text{and} \quad \boxed{i_{Tr} = \frac{i_{Tri}}{1 + \frac{\Delta q_{fh}}{q_{p,T}}}}$$

The total transfer current in HICUM/L0 reads:

$$i_T = i_{Tf} - i_{Tr} \, .$$

© 2023 Cadence Design Systems, Inc.

Static Base Current Components

$$i_{jBE} = I_{BES}\left[\exp\left(\frac{v_{B'E'}}{m_{BE}V_T}\right)-1\right]+I_{RES}\left[\exp\left(\frac{v_{B'E'}}{m_{RE}V_T}\right)-1\right],$$

$$i_{jBC} = I_{jBCS}\left[\exp\left(\frac{v_{B'C}}{m_{BC}V_T}\right)-1\right]$$

$$i_{AVL} = k_{AVL}\frac{i_{Tf}}{C_c^{1/z_{Ci}}}\exp\left(-e_{AVL}\,C_c^{\left(\frac{1}{z_{Ci}}-1\right)}\right)$$

$$i_{jSC} = I_{SCS}\left[\exp\left(\frac{v_{SC}}{m_{SC}V_T}\right)-1\right]$$

Related Topics

Depletion Charges And Capacitances

Model Version Updates

HiCUM Level-0 Model (bht0)

Depletion Charges And Capacitances

$$C_{jE} = \frac{C_{jE0}}{\left(1-v_j/V_{DE}\right)^{z_E}}\frac{dv_j}{dv_{B'E'}} + a_{jE}C_{jE0}\left(1-\frac{dv_j}{dv_{B'E'}}\right)$$

$$Q_{jE} = \frac{C_{jE0}V_{DE}}{1-z_E}\left[1-\left(1-\frac{v_j}{V_{DE}}\right)^{(1-z_E)}\right] + a_{jE}C_{jE0}(v_{B'E'}-v_j)$$

© 2023 Cadence Design Systems, Inc.

Minority Charges And Capacitances

The transit time consists of two components:

$$\tau_f(v_{CE'}, i_{If}) = \tau_f(v_{B'C'}) + \Delta\tau_f(v_{CE'}, i_{If})$$

Low current densities

The transit time reads:

$$\tau_{f0}(v_{B'C'}) = \tau_0 + \Delta\tau_{0h}(c-1) + \tau_{Bfvl}\left(\frac{1}{c}-1\right)$$

The respective forward minority charge is given by:

$$Q_{f0} = \tau_{f0}\, i_{If}$$

Medium and high current densities

The total increase in the (forward) transit time is given by:

$$\Delta\tau_f(v_{CE'}, i_{If}) = \Delta\tau_{Ef} + \Delta\tau_{fh}$$

$$\Delta\tau_{fh} = \tau_{hcs} \cdot w^2 \left[1 + \frac{2I_{CK}}{i_{If}\sqrt{i^2 + a_{hc}}}\right]$$

$$w = \frac{w_i}{w_C} = \frac{i + \sqrt{i^2 + a_{hc}}}{1 + \sqrt{1 + a_{hc}}}$$

$$i = 1 - \frac{I_{CK}}{I_{If}}$$

© 2023 Cadence Design Systems, Inc.

The critical current $I_{CK}$is described by the same voltage dependence as for HICUM/L2.:

$$I_{CK} = \frac{v_{ceff}}{r_{Ci0}^{*}} \frac{1}{\sqrt{1+\left(\frac{v_{ceff}}{V_{lim}}\right)^2}} \left[1 + \frac{x + \sqrt{x^2 + 10^{-3}}}{2}\right]$$

$$v_{ceff} = V_T\left[1 + \frac{1}{2}\left\{u_{vc} + \sqrt{u_{vc}^2 + 1.921812}\right\}\right]$$

$$\Delta Q_{fh} = \tau_{hcs} i_{Tf} w^2$$

Series Resistance

Internal base resistance

$$r_{Bi} = r_i \; \psi(\eta)$$

$$\psi(\eta) = \frac{\ln(1+\eta)}{\eta}$$

$$\eta = f_{geo} \frac{r_i I_{BE}}{V_T}$$

$$r_i = \frac{r_{Bi0}}{f_{Qz}}$$

$$f_{Qz} = \frac{1}{2}\left\{Q_z + \sqrt{Q_z^2 + 0.01}\right\}$$

$$Q_z = \left(1 + \frac{q_{jE}}{V_{r0E}} + \frac{q_{jCi}^{*}}{V_{r0C}} + \frac{I_{Tf}}{I_{Qf}} + \frac{I_{Tr}}{I_{Qr}}\right)$$

© 2023 Cadence Design Systems, Inc.

External series resistances

$$r_B = r_{Bi} + r_{Bx}$$

Temperature Dependence

$$V_g(T) = V_g(T_0) + k_1 \frac{T}{T_0} \ln\left(\frac{T}{T_0}\right) + k_2\left(\frac{T}{T_0} - 1\right)$$

with the definitions

$$k_1 = K_1 T_0 \quad , \quad k_2 = K_2 T_0 + k_1 \ln(T_0)$$

© 2023 Cadence Design Systems, Inc.

and the bandgap voltage at the measurement reference temperature

$$V_g(T_0) = k_2 + V_g(0)$$

$$I_S^*(T) = I_S^*(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{CT}} \exp\left[\frac{V_{Gb}}{V_T(T)}\left(\frac{T}{T_0}-1\right)\right]$$

$$I_{BES}(T) = I_{BES}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{BET}} \exp\left[\frac{V_{Gb}}{V_T(T)}\left(\frac{T}{T_0}-1\right)\right]$$

$$I_{RES}(T) = I_{RES}(T_0)\left(\frac{T}{T_0}\right)^{m_g/2} \exp\left[\frac{V_{Gb}}{V_T(T)}\left(\frac{T}{T_0}-1\right)\right]$$

$$I_{BCS}(T) = I_{BCS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{BCT}} \exp\left[\frac{V_{Gbx}}{V_T(T)}\left(\frac{T}{T_0}-1\right)\right]$$

with $\zeta_{BET} = m_g + 1 - \zeta_{CT}$ and

$$I_{SCS}(T) = I_{SCS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{SCT}} \exp\left[\frac{V_{Gsc}}{V_T(T)}\left(\frac{T}{T_0}-1\right)\right]$$

$$I_{TSS}(T) = I_{TSS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{SCT}} \exp\left[\frac{V_{Gc}}{V_T(T)}\left(\frac{T}{T_0}-1\right)\right]$$

with $\zeta_{SCT} = m_g - 1.5$

$$C_{j0}(T) = C_{j0}(T_0)\left(\frac{V_D(T_0)}{V_D(T)}\right)^z$$

$$V_{Dj}(T_0) = 2V_{T0}\ln\left[\exp\left(\frac{V_D(T_0)}{2V_{T0}}\right) - \exp\left(-\frac{V_D(T_0)}{2V_{T0}}\right)\right]$$

$$V_{Dj}(T) = V_{Dj}(T_0)\left(\frac{T}{T_0}\right) + V_g\left(1-\frac{T}{T_0}\right) - m_g V_{T0}\ln\left(\frac{T}{T_0}\right)$$

© 2023 Cadence Design Systems, Inc.

$$V_D(T) = V_{Dj}(T) + 2V_T \ln\left(\frac{1+\sqrt{1+4\exp\left(-\frac{V_{Dj}(T)}{V_T}\right)}}{2}\right)$$

$$\tau_0(T) = \tau_0(T_0)[1 + alt0(T-T_0) + kt0(T-T_0)^2]$$

$$r_{Ci0}(T) = r_{Ci0}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{CI}}$$

$$V_{CEs}(T) = V_{CEs}(T_0)[1 + (T-T_0)\alpha_{CES}]$$

$$r_{Cx}(T) = r_{Cx}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{RCX}}$$

$$r_{Bx}(T) = r_{Bx}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{RBX}}$$

$$r_{Bi0}(T) = r_{Bi0}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{RBI}}$$

$$r_E(T) = r_E(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{RE}}$$

Noise Model

The equivalent noise current source is used for thermal noise in ohmic resistance:

$$\overline{I_r^2} = \frac{4kT\Delta f}{r}$$

© 2023 Cadence Design Systems, Inc.

For the transfer current, shot noise is assumes as:

$$\overline{I_T^2} = 2qI_T\,\Delta f$$

The noise resulting from the current injected across the BE junction into the emitter

$$\overline{I_{BE}^2} = 2qI_{jBE}\Delta f + k_F\, I_{jBE}^{a_F}\,\frac{\Delta f}{f}$$

The currents across the other junctions are assumed to have a shot noise component only

$$\overline{I_{jdiode}^2} = 2qI_{jdiode}\,\Delta f$$

Noise from avalanche generation within the internal BC depletion region is modelled as shot noise

$$\overline{I_{AVL}^2} = 2qI_{AVL}\,\Delta f$$

giving for the total noise contribution within the BC junction

$$\overline{I_{BC}^2} = \overline{I_{jBC}^2} + \overline{I_{AVL}^2}$$

DC Characteristics

$$i_T = c_{10}\cdot\frac{\exp(V_{B'E'}/V_T) - \exp(V_{B'C'}/V_T)}{Q_{p0} + h_{jei}Q_{jei} + h_{jci}Q_{jCi} + Q_{fT} + Q_{rT}}$$

$$i_{Tf} = \frac{I^*_S}{1 + \dfrac{h_{jci}Q_{jCi}}{Q_{p0}} + \dfrac{Q_{fT}}{Q_{p0}} + \dfrac{Q_{rT}}{Q_{p0}}}\cdot\exp\left(\frac{v_{B'E'}}{m_{Cf}V_T}\right)$$

$$I^*_S = (c_{10}/Q^*_{p0})\exp((h_{jei}C_{jei,\,op}v_{B'E',\,op})/Q^*_{p0})$$

© 2023 Cadence Design Systems, Inc.

$$V_{Ef} = \frac{Q^*_{p0}}{h_{jci} C_{jCi0}}$$

$$I_{Qf} = Q^*_{p0} / \tau_{f0} (v_{B'C'} = 0)$$

$$I_{Qr} = Q^*_{p0} / \tau_f$$

$$q_{pT} = \underbrace{\frac{1 + q_{jCi}/V_{Ef}}{q_j}} + \underbrace{\frac{i_{Tfl}/I_{Qf} + i_{Trl}/I_{Qr}}{q_m/q_{pT}}}$$

$$i_{Trl} = \frac{I^*_s}{q_{pT}} \exp\left(\frac{v_{B'C'}}{m_{Cr} V_T}\right)$$

$$\frac{Q_{fT} - \tau_{f0} i_{Tfl}}{Q^*_{p0}} \cong \Delta q_{fh} = \left(w^2 + t_{fh} \frac{i_{Tfl}}{I_{CK}}\right) \frac{i_{Tfl}}{I_{Qfh}}$$

$$i_T = \frac{i_{Tfl} - i_{Trl}}{1 + \Delta q_{fh}/q_{pT}}$$

Charge Storage Elements

$$\tau_f = \tau_{f0}(V_{B'C'}) + \Delta\tau_f(i_{Tf}, V_{C'E'})$$

The current dependence of $\Delta\tau_f$ is simplified by neglecting the bias dependent collector current spreading formulation. However, the bias independent collector current spreading factor *fcs* remains included in the critical current ICK, resulting in a more physical geometry dependence of the low-field internal (epi-)collector resistance.

$$\Delta\tau_f = \tau_{hcs} w^2 \left(1 + \frac{2 l_{CK}}{i_{Tf} \sqrt{(1 - l_{CK}/i_{Tf})^2 + a_{hc}}}\right) + \tau_{fE0} \left(\frac{i_{Tf}}{l_{CK}}\right)^{g_{\tau fE}}$$

$$Qf = ((Qf0 + dQef) + dQfh)$$

$$Q_r = \tau_r i_{Tr}$$

© 2023 Cadence Design Systems, Inc.

Series Resistance

The internal base resistance can be strongly bias dependent and is modeled as

$$r_i = \frac{r_{Bi0}}{1 + \frac{q_{jE}}{V_{r0E}} + \frac{q_{jCi}}{V_{r0C}} + \frac{i_{Tf}}{I_{Qf}} + \frac{l_{Tf}}{I_{Qr}}}$$

where *rBi0* is the geometry dependent zero-bias value, and the denominator represents the conductivity modulation. The above equation has been derived from HICUM level-2 by introducing certain simplifications. Note, that *VroC* is close to the Early voltage V_{Ef} for BJTs but generally differs from V_{Ef} for HBTs.

Temperature Effects

$$qtt0 = Tdev/Tnom$$

$$Is(t) = IS*\exp(ZETACT*\ln(qtt0) + VGB/VT*(qtt0 - 1))$$

$$Ibes(t) = IBES*\exp(ZETABET*\ln(qtt0) + VGE/VT*(qtt0 - 1))$$

$$Ires(t) = IRES*\exp(ZETABET*\ln(qtt0) + vgbe/VT*(qtt0 - 1))$$

$$Ibcs(t) = IBCS*\exp(ZETABCI*\ln(qtt0) + VGC/VT*(qtt0 - 1))$$

$$Iscs(t) = ISCS*\exp(ZETASCT*\ln(qtt0) + VGS/VT*(qtt0 - 1))$$

$$vdj0 = 2*VT0*\ln(\exp(0.5*vd/VT0) - \exp(-0.5*vd/VT0))$$

$$vdjt = vdj0*qtt0 + vg*(1 - qtt0) - mg*VT*\ln(qtt0)$$

$$vd_t = vdjt + 2*VT*\ln(0.5*(1 + sqrt(1 + 4*\exp(-vdjt/VT))))$$

where *vg* can be replaced with *vgbe*, *vgbc*, or *vgsc*

$$Cje0(t) = CJE0*\exp(ZE*\ln(VDE/vd_t))$$

© 2023 Cadence Design Systems, Inc.

$$Cjci0(t) = CJCI0*\exp(ZCI*\ln(VDCI/vd_t))$$

$$Cjcx0(t) = CJCX0*\exp(ZCX*\ln(VDCX/vd_t))$$

$$Cjs0(t) = CJS0*\exp(ZS*\ln(VDS/vd_t))$$

$$Rci0(t) = RCI0*\exp(ZETACI*\ln(qtt0))$$

$$Vlim(t) = VLIM*\exp((ZETACI-avs)*\ln(qtt0))$$

$$Vces(t) = VCES*(1+ALCES*dt)$$

$$T0(t) = T0*(1+ALT0*dt+KT0*dT*dT)$$

$$Thcs(t) = THCS*\exp((ZETACI-1)*\ln_qtto)$$

$$zetatef = ZETABET-ZETACT-0.5$$

$$dvg = VGB-VGE$$

$$Tef0(t) = TEF0*\exp(ZETATEF*\ln(qtt0)-dvg/VT*(qtt0-1))$$

$$Rbx(t) = RBX*\exp(ZETARBX*\ln(qtt0))$$

$$Rcx(t) = RCX*\exp(ZETARCX*\ln(qtt0))$$

$$rbi0(t) = RBI0*\exp(ZETARBI*\ln(qtt0))$$

$$Re(t) = RE*\exp(ZETARE*\ln(qtt0))$$

$$Eavl(t) = EAVL*\exp(ALEAV*dT) \quad /$$

$$Kavl(t) = KAVL*\exp(ALKAV*dT)$$

Noise Model

The equivalent noise current source is used for thermal noise in ohmic resistance:

© 2023 Cadence Design Systems, Inc.

$$\overline{I_r^2} = \frac{4k_B T\Delta f}{r}, with\ \mathrm{r} \rightarrow r_E, r_{Cx}, r_B = r_{Bx} + R_{Bi}$$

Shot noise is assumed for transfer current

$$\overline{I_T^2} = 2qI_T\Delta f$$

Shot noise for current across BE junction is taken into account in the following equation

$$\overline{I_{jBE}^2} = 2qI_{jBE}\Delta f$$

A flicker noise source is implemented for the BE junction

$$\overline{I_{BE}^2} = k_f I_{jBE}^{a_f}\frac{\Delta f}{f}$$

Other Effects

Self-heating is included to overcome one of the most significant deficiencies of the SGPM for advanced processes including III-V HBTs.

Related Topics

Equivalent Circuit

Model Version Updates

HiCUM Level-0 Model (bht0)

Models and Equations in Version 1.30

Improved model formulations for the HICUM/L0 transfer current

The improvements can be categorized by:

- Bias Dependence
- Temperature Dependence

© 2023 Cadence Design Systems, Inc.

Bias Dependence

Low and Medium Current Range

The equation for reverse Early voltage is:

$$V_{Er} = \frac{V_{Er0}}{\left(\frac{\exp(u)-1}{u}\right)}$$

where

$$u = a_{VEr}\left(1-\left(1-\frac{v_j}{V_{DE}}\right)^{Z_E}\right)$$

Here, V_{Er0} is the Early voltage for zero volt and aV_{Er} the parameter describing the change of the Early voltage. The junction voltage is limited to the range (0, VDEi) as follows:

$$\chi_{upp} = \frac{V_{DE}-V_{BEi}}{r_{VEr}V_t}$$

$$v_{j,upp} = V_{DE} - r_{VEr}V_T\frac{\chi_{upp}-\sqrt{\chi^2_{upp}+a_{fi}}}{2}$$

$r_{VEr}V_T$ is used rather than V_T since it allows a smooth transition to voltages larger than V_{DE}.

The limitation to values larger zero is realized by:

$$\chi_{low} = \frac{v_{j,upp}-V_T}{V_T} \qquad \text{and} \qquad v_j = V_T\left(1+\frac{\chi_{low}+\sqrt{\chi^2_{low}+a_{fi}}}{2}\right)$$

The parameters V_{DE} and j used here are the same as for the electrostatic capacitance. For simplification, the parameter r_{VEr} is set to a fixed value of two, which is sufficient for all verifications. However, to allow full backward compatibility the parameter set for the DC charge VDEDC, zEDC and ajEDC is still kept separately from that of the AC charge, although the values may be the same. Therefore, the DC-charge formulation can still be used in the new version and the bias dependence of V_{Er} can be turned off by settings a_{VEr} to zero.

© 2023 Cadence Design Systems, Inc.

High Current

The transfer current equation for high current effects has been changed. In earlier versions, a second order polynomial (with bias dependent coefficients) was used for the whole range. However, a more physical description results in a third order polynomial function (resulting from $g_{\tau fE}$=1 in HICUM/L2). The third order polynomial reads:

$$q_{pT}^{3} - q_j q_{pT}^{2} - \left(\frac{I_{Tf0}}{I_{CKf}} + \frac{I_{Tr0}}{I_{CKr}} + \frac{I_{Tf0}}{I_{Qfh}} w^2 \right) q_{pT} - \frac{I_{Tf0}^2 t_{fh}}{I_{CK} I_{Qfh}} = 0$$

The above equation can be solved with respect to q_{pT}.

The following is the transfer current equation for modeling the high current effects:

$$i_{Tf} = \frac{I_s}{q_j + \frac{i_{Tf}}{I_{CKf}} + \frac{i_{Tr}}{I_{CKr}} + w^2 \frac{i_{Tf}}{I_{Qfh}} + \left(\frac{i_{Tf}}{I_{CK}} \right) \frac{i_{Tf}}{I_{QfE}}}$$

tfh can be calculated by:

$$t_{fh} = \frac{I_{Qfh}}{I_{QfE}}$$

Temperature Dependence

Medium Bias Range

The medium bias range is dominated by the temperature dependence of the saturation current and reverse Early voltage. The temperature dependence of the saturation current is kept untouched. The reverse Early voltage itself becomes temperature dependent. Two effects need to be taken into account.

First, the Early voltage at zero volt changes due to the different bandgap in the base and the BESCR. This bandgap difference is used as a parameter along with a non-idealitiy parameter. The equation itself reads:

$$V_{Er0}(T) = V_{Er0}(T_0) \exp\left[\frac{-\Delta V_{gBE}}{V_T} \left(\left(\frac{T}{T_o} \right)^{\zeta_{vgBE}} - 1 \right) \right]$$

© 2023 Cadence Design Systems, Inc.

Additional, the parameter describing the Early voltage change also changes due to the temperature voltage VT and the temperature induced moving of the SCR-boundary. Both effects are modelled using one temperature coefficient.

$$a_{VEr}(T) = a_{VEr}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{VEr}}$$

High Current Effects

The temperature dependence of I_{Qf} is given by:

$$I_{Qf}(T) = I_{Qf}(T0)\left(\frac{T}{T0}\right)^{\zeta_{IQf}} \exp\left(\frac{-\Delta V_{gBE}}{V_T}\left(\frac{T}{T0}-1\right)\right)$$

Due to different bandgap voltages in the transistor, high current effects may become also temperature dependent. Since for IQfh, minorities in different regions of the transistor are taken into account, a simple second order polynomial fit is applied, as follows:

$$I_{Qfh}(T) = I_{Qfh}(T0)\left(1+\alpha_{IQfh}\Delta T + k_{IQfh}\Delta T^2\right)$$

$$I_{Qfh} = \frac{Q_{p0}}{((1-f_{\tau hC})+f_{\tau hC}h_{fC})\tau_{hCs}}$$

The temperature dependence of t_{fh} is given by:

$$t_{fh}(T) = t_{fh}(T_0)\frac{I_{Qfh}(T)}{I_{Qfh}(T_0)}\exp\left(\frac{V_{gb}-V_{ge}}{V_T}\left(\frac{T}{T_0}-1\right)\right)$$

Related Topics

Equivalent Circuit

Model Version Updates

Depletion Charges And Capacitances

© 2023 Cadence Design Systems, Inc.

HiCUM Level-0 Model (bht0)

Component Statements

The device is supported within altergroups.

Instance Definition

```
Name  c  b  e  s  [tnode] ModelName parameter=value ...
```

Instance Parameters

`dt=0.0 K`	Temperature change for particular transistor.
`dtemp=0.0`	Alias for dt.
`trise=0.0`	Alias for dt.
`m=1`	Instance parameter Mfactor.
`exp_cr=80`	Instance parameter exp_cr for limitexp.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.
`self_heating=yes`	Control switch for self-heating. The value fast is Cadence's proprietary approach, which is significantly faster than full self-heating and generates similar results in most cases. Possible values are `no`, `yes` and `fast`.

Model Definition

```
model modelName bht0 parameter=value ...
```

Model Parameters

`is=1.0e-16 A`	(Modified) saturation current.
`it_mod=0`	Flag for using third order solution for transfer current.
`flitm=0`	Flag for using third order solution for transfer current.

© 2023 Cadence Design Systems, Inc.

mcf=1.00	Non-ideality coefficient of forward collector current.
mcr=1.00	Non-ideality coefficient of reverse collector current.
vef=1.0e6 V	Forward Early voltage (normalization volt.).
ver=1.0e6 V	Reverse Early voltage (normalization volt.).
aver=0.0	Bias dependence for reverse Early voltage.
iqf=1.0e6 A	Forward d.c. high-injection toll-off current.
fiqf=0	Flag for turning on base related critical current.
iqr=1.0e6 A	Inverse d.c. high-injection roll-off current.
iqfh=1.0e6 A	High-injection correction current.
tfh=0.0	High-injection correction factor.
ahq=0	Smoothing factor for the d.c. injection width.
rver=2.0	Smoothing parameter for VBE at high voltage.
bes=1e-18 A	BE saturation current.
mbe=1.0	BE non-ideality factor.
ires=0.0 A	BE recombination saturation current.
mre=2.0	BE recombination non-ideality factor.
ibcs=0.0 A	BC saturation current.
mbc=1.0	BC non-ideality factor.
favl=0.0	Avalanche current factor.
qavl=0.0	Exponent factor for avalanche current.
cje0=1.0e-20 F	Zero-bias BE depletion capacitance.
vde=0.9 V	BE built-in voltage.
ze=0.5	BE exponent factor.
aje=2.5	Ratio of maximum to zero-bias value.
vdedc=0.9 V	BE charge built-in voltage for d.c. transfer current.
zedc=0.5	BE charge exponent factor for d.c. transfer current.
ajedc=2.5	BE capacitance ratio. The ratio can be maximum to zero-bias value d.c. transfer current.
t0=0.0 s	Low current transit time at Vbici=0.

© 2023 Cadence Design Systems, Inc.

dt0h=0.0	Base width modulation contribution.
tbvl=0.0 s	SCR width modulation contribution.
tef0=0.0 s	Storage time in neutral emitter.
gte=1.0	Exponent factor for emitter transit time.
thcs=0.0 s	Saturation time at high current densities.
ahc=0.1	Smoothing factor for current dependence.
tr=0.0 s	Storage time at inverse operation.
rci0=150 Ω	Low-field collector resistance under emitter.
vlim=0.5 V	Voltage dividing ohmic and saturation region.
vpt=100 V	Punch-through voltage.
vdci=0.7 V	BC built-in voltage.
vdck=0.0	Build-In B-C voltage including voltage drop in B and epi-b.l..
aick=1e-3	Smoothing term for ICK.
delck=2.0	Fitting factor for critical current.
cjci0=1.0e-20 F	Total zero-bias BC depletion capacitance.
vdci=0.7 V	BC built-in voltage.
zci=0.333	BC exponent factor.
vptci=100 V	Punch-through voltage of BC junction.
cjcx0=1.0e-20 F	Zero-bias external BC depletion capacitance.
vdcx=0.7 V	External BC built-in voltage.
zcx=0.333	External BC exponent factor.
vptcx=100 V	Punch-through voltage.
fbc=1.0	Split factor = Cjci0/Cjc0.
rbi0=0.0 Ω	Internal base resistance at zero-bias.
vr0e=2.5 V	Forward early voltage (normalization voltage).
vr0c=1.0e6 V	Forward early voltage (normalization voltage).
fgeo=0.656	Geometry factor.
rbx=0.0 Ω	External base series resistance.

© 2023 Cadence Design Systems, Inc.

`rcx=0.0 Ω`	Emitter series resistance.
`re=0.0 Ω`	External collector series resistance.
`itss=0.0 A`	Substrate transistor transfer saturation current.
`msf=1.0`	Substrate transistor transfer current non-ideality factor.
`iscs=0.0 A`	SC saturation current.
`msc=1.0`	SC non-ideality factor.
`cjs0=1.0e-20 F`	Zero-bias SC depletion capacitance.
`vds=0.3 V`	SC built-in voltage.
`zs=0.3`	External SC exponent factor.
`vpts=100 V`	SC punch-through voltage.
`cbcpar=0.0 F`	Collector-base isolation (overlap) capacitance.
`cbepar=0.0 F`	Emitter-base oxide capacitance.
`eavl=0.0`	Exponent factor.
`kavl=0.0`	Prefactor.
`kf=0.0 M^(1-AF)`	Flicker noise coefficient.
`af=2.0`	Flicker noise exponent factor.
`alqf=0.167`	Factor for additional delay time of minority charge.
`alit=0.333`	Factor for additional delay time of transfer current.
`flnqs=0`	Flag for turning on and off of vertical NQS effect.
`vgb=1.2 V`	Bandgap-voltage.
`vge=1.17 V`	Effective emitter bandgap-voltage.
`vgc=1.17 V`	Effective collector bandgap-voltage.
`vgs=1.17 V`	Effective substrate bandgap-voltage.
`f1vg=(-1.02377e-4) V/K`	Coefficient K1 in T-dependent bandgap equation.
`f2vg=4.3215e-4 V/K`	Coefficient K2 in T-dependent bandgap equation.
`alt0=0.0 1/K`	First-order TC of tf0.

© 2023 Cadence Design Systems, Inc.

`kt0=0.0 1/K`^{2}	Second-order TC of tf0.
`zetact=3.0`	Exponent coefficient in transfer current temperature dependence.
`zetabet=3.5`	Exponent coefficient in BE junction current temperature dependence.
`zetaci=0.0`	TC of epi-collector diffusivity.
`alvs=0.0 1/K`	Relative TC of saturation drift velocity.
`alces=0.0 1/K`	Relative TC of vces.
`zetarbi=0.0`	TC of internal base resistance.
`zetarbx=0.0`	TC of external base resistance.
`zetarcx=0.0`	TC of external collector resistance.
`zetare=0.0`	TC of emitter resistances.
`zetaiqf=0.0`	TC of iqf.
`alkav=0.0 1/K`	TC of avalanche prefactor.
`aleav=0.0 1/K`	TC of avalanche exponential factor.
`zetarth=0.0`	Exponent factor for temperature dependent thermal resistance.
`tef_temp=1`	Flag for turning temperature dependence of tef0 on and off.
`zetaver=(-1.0)`	TC of Reverse Early voltage.
`zetavgbe=1.0`	TC of AVER.
`dvgbe=0.0`	Bandgap difference between base and BE-junction.
`aliqfh=0 1/K`	First-order TC of iqfh.
`kiqfh=0 1/K`^{2}	Second-order TC of iqfh.
`alfav=0.0`	Relative TC for FAVL.
`alqav=0.0`	Relative TC for QAVL.
`aldck=0.0`	Relative TC of VDCK.
`flteft=1`	Flag for turning temperature dependence of tef0 on and off.
`flsh=0`	Flag for self-heating calculation.

© 2023 Cadence Design Systems, Inc.

`rth=0.0 K/W`	Thermal resistance.
`cth=0.0 Ws/K`	Thermal capacitance.
`pnp=0`	Model type flag for pnp.
`npn=1`	Model type flag for npn.
`alrth=0.0`	First order relative TC of parameter Rth.
`type=1`	Transistor type. 1 for NPN and -1 for PNP. This parameter is available starting with version 1.32.
`tnom=27 C`	Temperature for which parameters are valid.
`version=1.2`	The available versions are 1.0, 1.11, 1.12, 1.2, 1.3, 1.31, 1.32 and 2.00.

Output Parameters

`meff`	Effective multiplicity factor (m-factor).

Operating Point Parameters

`qjci (C)`	B-C internal junction charge.
`qjei (C)`	B-E internal junction charge.
`cjei (F)`	B-E internal junction capacitance.
`it (A)`	Transfer Current.
`ijbc (A)`	Base-collector diode current.
`iavl (A)`	Avalanche current.
`ijsc (A)`	Substrate-collector diode current.
`ieei (A)`	Current through external to internal emitter node.
`icci (A)`	Current through external to internal collector node.
`ibbi (A)`	Current through external to internal base node.
`ibici (A)`	Base-collector diode current minus the avalanche current.

© 2023 Cadence Design Systems, Inc.

ijbe (A)	Base-emitter diode current.
vef (V)	Effective forward Early-voltage.
ver (V)	Effective inverse Early-voltage.
tempeff (C)	Effective temperature for a single device.
ib	Base terminal current.
ic	Collector terminal current.
is	Substrate current.
vbe	External BE voltage.
vbc	External BC voltage.
vce	External CE voltage.
vsc	External SC voltage.
betadc	Common emitter forward current gain.
gmi	Internal transconductance.
rpii	Internal input resistance.
rmui	Internal feedback resistance.
roi	Internal Output resistance.
cpii	Total BE capacitance.
cmui	Total internal BC capacitance.
cbcx	Total external BC capacitance.
ccs	CS junction capacitance.
rbi	Internal base resistance.
rb	Total base resistance.
rcx	External (saturated) collector series resistance.
re	Emitter series resistance.
betaac	Small signal current gain.
tf	Total forward transit time.
ft	Transit frequency.
pwr (W)	Power dissipation.

© 2023 Cadence Design Systems, Inc.

Related Topics

Equivalent Circuit

Model Version Updates

Depletion Charges And Capacitances

HiCUM Level-0 Model (bht0)

© 2023 Cadence Design Systems, Inc.

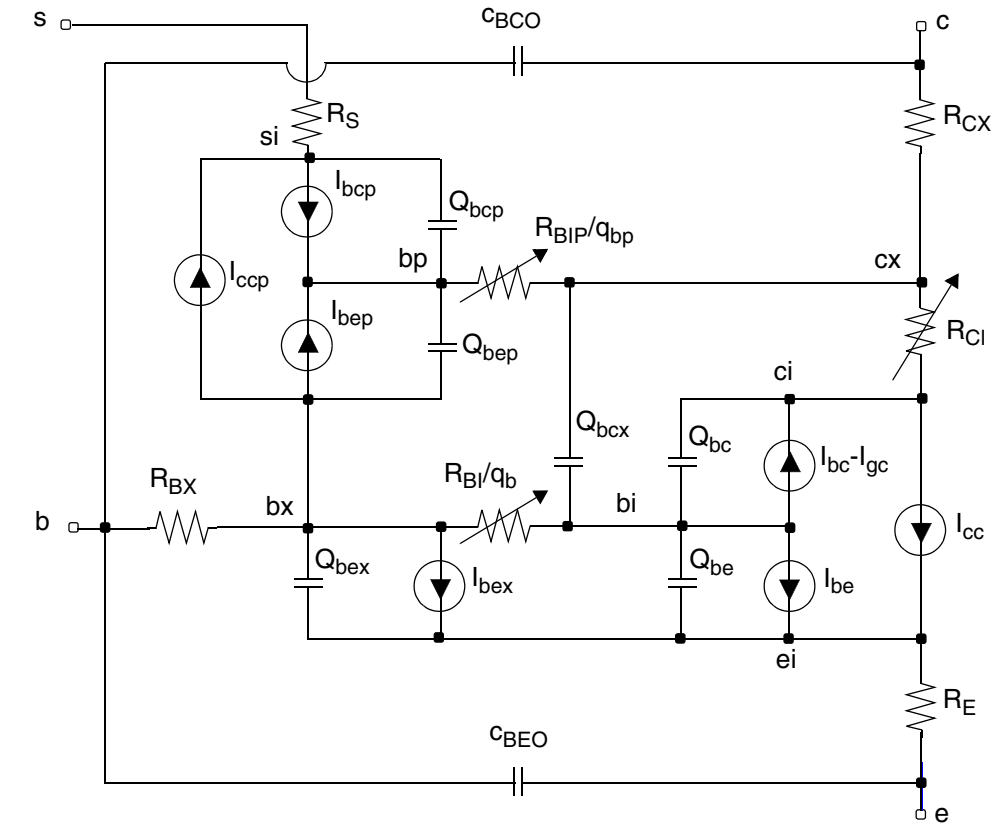
8

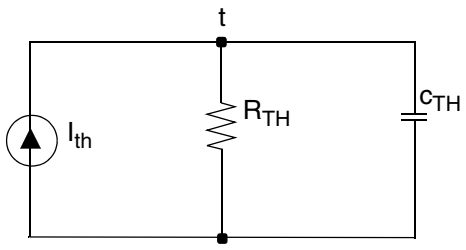
VBIC Model (vbic)

The VBIC model was developed by the Colin McAndrew team at Motorola as a replacement of the Gummel-Poon model. This chapter contains the following information for the VBIC model:

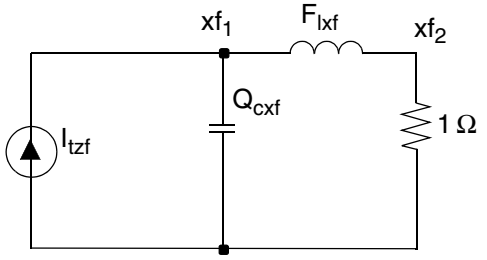
- VBIC 1.1
  - DC Current
  - Charge Equations
  - Excess Phase
  - Small Signal Parameters
  - Temperature Equations
  - Noise Equations
- VBIC 1.2
  - DC Current
  - Charge Equations
  - Temperature Equations
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.





Thermal network



Excess phase network

© 2023 Cadence Design Systems, Inc.

VBIC 1.1

DC Current

$$I_{cc} = \frac{I_{tf} - I_{tr}}{Q_b}$$

$$I_{tf} = I_s \ (e^{V_{bei}/N_f V_{tm}} - 1)$$

$$I_{tr} = I_s \ (e^{V_{bci}/N_r V_{tm}} - 1)$$

$$Q_b = \frac{1}{2}\left(Q_1 + \sqrt{Q_1^2 + 4Q_2}\right)$$

$$Q_1 = \frac{1}{2}\sqrt{\left(0.9999 + \frac{Q'_{je}}{V_{er}} + \frac{Q'_{jc}}{V_{ef}}\right)^2 + 10^{-8}} + \frac{1}{2}\left(0.9999 + \frac{Q'_{je}}{V_{er}} + \frac{Q'_{jc}}{V_{ef}}\right) + 10^{-4}$$

$$Q'_{je} = \frac{Q_{je}}{C_{je}}$$

$$Q'_{jc} = \frac{Q_{jc}}{C_{jc}}$$

$$Q_2 = \frac{I_{tf}}{I_{kf}} + \frac{I_{tr}}{I_{kr}}$$

$$I_{be} = W_{be}\left[I_{bei}(e^{V_{bei}/N_{ei}V_{tm}} - 1) + I_{ben}\ (e^{V_{bei}/N_{en}V_{tm}} - 1)\right]$$

$$I_{bex} = (1 - W_{be})\left[I_{bei}\ (e^{V_{bex}/N_{ei}V_{tm}} - 1) + I_{ben}\ (e^{V_{bex}/N_{en}V_{tm}} - 1)\right]$$

© 2023 Cadence Design Systems, Inc.

$$I_{bc} = I_{bci}\ (e^{V_{bci}/N_{ci}V_{tm}} - 1) + I_{bcn}\ (e^{V_{bci}/N_{cn}V_{tm}} - 1)$$

$$I_{gc} = (I_{cc} - I_{bc})\ A_{vc1}\ 1V_l\ e^{-A_{vc2}\ V_{lm}}$$

$$V_l = \frac{1}{2}\left[\sqrt{(P_c - V_{bc})^2 + 0.01} + (P_c - V_{bc})\right]$$

$$V_{lm} = V_l^{(M_c - 1)}$$

$$I_{bep} = I_{beip}\ (e^{V_{bep}/N_{ci}V_{tm}} - 1) + I_{benp}\ (e^{V_{bep}/(N_{cn}V_{tm})} - 1)$$

$$I_{bcp} = I_{bcip}\ (e^{V_{bcp}/(N_{cip}V_{tm})} - 1) + I_{bcnp}\ (e^{V_{bcp}/(N_{cnp}V_{tm})} - 1)$$

$$I_{ccp} = \frac{I_{tfp} - I_{trp}}{Q_{bp}}$$

$$I_{tfp} = W_{sp}\ I_{sp}\ (e^{V_{bep}/N_{fp}\ V_{tm}} - 1) + (1 - W_{sp})\ I_{sp}\ (e^{V_{bci}/N_{fp}\ V_{tm}} - 1)$$

$$I_{trp} = I_{sp}\ (e^{V_{bcp}/N_{fp}\ V_{tm}} - 1)$$

$$Q_{bp} = \frac{1}{2}(1 + \sqrt{1 + 4Q_{2p}})$$

$$Q_{2p} = \frac{I_{tfp}}{I_{kp}}$$

$$R_{bi} = \frac{R_{bi}}{Q_b}$$

$$R_{bp} = \frac{R_{bp}}{Qbp}$$

© 2023 Cadence Design Systems, Inc.

$$I_{rci} = \frac{V_{rci} + Vtm[Kbci - Kbcx - ln(Rxpi)]}{R_{ci}\sqrt{1 + (Derf)^2}}$$

$$D_{erf} = \frac{V_{rci} + V_{tm}\ [K_{bci} - K_{bcx} - \ln(R_{kp1})]}{V_o + \frac{\sqrt{V_{rci}^2 + 0.01}}{2H_{rcf}}}$$

If the backward compatibility flag imeltrci=no (the default value), K_{bci} and K_{bcx} are calculated as follows:

$$K_{bci} = \sqrt{1 + G_{amm}\ e^{V_{bc}/V_{tm}}}$$

$$K_{bcx} = \sqrt{1 + G_{amm}\ e^{V_{bcx}/V_{tm}}}$$

If imeltrci=yes, K_{bci} and K_{bcx} are limited.

$$R_{kp1} = \frac{K_{bci} + 1}{K_{bcx} + 1}$$

$$V_{bcx} = V_{bci} - V_{rci}$$

Charge Equations

$$Q_{be} = W_{be}\ Q_{je} + T_{ff}\ I_{tf}$$

$$T_{ff} = \begin{cases} T_f\ (1 + Q_{tf}\ Q_1)\left[1 + X_{tf}\ e^{V_{bci}/(1.44\ V_{tf})}\ \frac{\left(\frac{I_{tf}(current)}{I_{tf}(modelparameter)}\right)^2}{\left(1 + \frac{I_{tf}}{I_{tf}}\right)^2}\right] & \text{If } I_{tf} \text{ (model parameter)} > 0 \\ T_f\ (1 + Q_{tf}\ Q_1) & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Note: In the above equation, I_{tf} is the current calculated from the equation given under the section DC Current.

$$Q_{bc} = T_r \; I_{tr} + Q_{jc} + Q_{co} \; K_{bci}$$

$$Q_{bex} = (1 - W_{be}) \; Q_{jex}$$

$$Q_{bcx} = Q_{co} \; K_{bcx}$$

$$Q_{bep} = T_r \; I_{tfp} + Q_{jep}$$

$$Q_{bcp} = Q_{jcp}$$

$$Q_{je} = Q_j(C_{je}, P_e, M_e, A_{je}, V_{bei})$$

$$Q_{jc} = Q_j(C_{jc}, P_c, M_c, A_{jc}, V_{bci})$$

$$Q_{jex} = Q_j(C_{je}, P_e, M_e, A_{je}, V_{bex})$$

$$Q_{jep} = Q_j(C_{jep}, P_c, M_c, A_{jc}, V_{bep})$$

$$Q_{jcp} = Q_j(C_{jcp}, P_s, M_s, A_{js}, V_{bcp})$$

If $A_j > 0$, $Q_j(C_j, P, M, A_j, V)$ is calculated as

$$Q_j = \frac{C_j}{2}\left(1 - \frac{D_v}{M_v}\right)\left(1 - \frac{V_l}{P}\right)^{-M} + \frac{C_j}{(1 - F_c)^M}\left[1 - \frac{1}{2}\left(1 - \frac{D_v}{M_v}\right)\right]$$

$$D_v = V - P \; F_c$$

$$M_v = \sqrt{D_v^2 + A_j}$$

$$V_l = \frac{1}{2}(D_v - M_v) + P \; F_c$$

© 2023 Cadence Design Systems, Inc.

$$Q_j = -\frac{C_j \ P \ \left(1-\frac{V_l}{P}\right)\left(1-\frac{V_l}{P}\right)^{-M}}{1-M} - Q_0 + \frac{C_j \ (V - V_l + V_{l0})}{(1-F_c)^M}$$

$$Q_0 = -\frac{C_j \ P \ \left(1-\frac{V_{l0}}{P}\right)^{1-M}}{1-M}$$

$$V_{l0} = \frac{1}{2}(D_{v0} - M_{v0}) + P \ F_c$$

$$D_{v0} = -P \ F_c$$

$$M_{v0} = \sqrt{D_{v0}^2 + A_j}$$

If $A_j \le 0$, $Q_j(C_j, P, M, A_j, V)$ is calculated as

$$Q_j = \begin{cases} C_j P\left[\dfrac{1-\left(1-\frac{V}{P}\right)^{1-M}}{1-M}\right] & \text{If } V \le F_c P \\ \dfrac{[1-F_c \ (1+M)] \ (V - F_c \ P) + \dfrac{M \ (V^2 - F_c^2 \ P^2)}{2P}}{(1-F_c)^{M+1}} + \dfrac{P}{1-M}\left[1 - \dfrac{1}{(1-F_c)^{M-1}}\right] & \text{otherwise} \end{cases}$$

otherwise

$$C_j = \begin{cases} \dfrac{C_j}{\left(1-\frac{V}{P}\right)^M} & \text{If } \quad V \le F_c P \\ \dfrac{1}{(1-F_c)^M\left[1+\dfrac{M \ (V - F_c \ P)}{P - F_c \ P}\right]} & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Excess Phase

In an actual device, the measured phase shift is often larger than the shift predicted by the lumped model. The excess-phase parameter *td* accounts for this extra phase shift at high frequencies. An all-pass, second-order Bessel function filter creates this extra phase shift. The frequency response of this filter is

$$\phi(s) = \frac{3\omega_0^2}{s^2 + 3\omega_0 s + 3\omega_0^2}$$

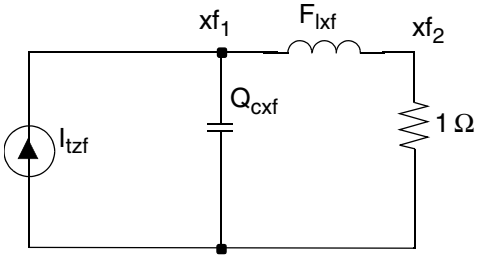
where

$$\omega_0 = \frac{1}{td}$$

and the phase shift due to this filter is

$$\theta = tan^{-1}\frac{3\omega\omega_0}{3\omega_0^2 - \omega^2}$$

The Bessel filter is implemented with the excess phase network shown below.



Excess phase network

where $L_{xf} = \frac{td}{3}$ and $C_{xf} = td$.

Small Signal Parameters

$$g_m = \frac{dI_{cc}}{dV_{be}} + \frac{dI_{cc}}{dV_{bc}}$$

© 2023 Cadence Design Systems, Inc.

$$g_{pi} = \frac{dI_{be}}{dV_{be}}$$

$$g_o = -\frac{dI_{cc}}{dV_{bc}}$$

$$g_{mu} = \frac{dI_{bc}}{dV_{bc}}$$

$$betaAC = \frac{g_m}{g_{pi}}$$

$$c_{pi} = \frac{dQ_{be}}{dV_{be}}$$

$$c_{mu} = \frac{dQ_{bc}}{dV_{bc}}$$

$$C_{bcx} = \frac{dQ_{bcx}}{dV_{bcx}}$$

If R_{ci} is given,

$$F_t = \frac{g_m}{2\pi(c_{pi} + g_m \cdot tf + cb_{cx} + cmu(g_m R_{ci} + 1))}$$

where

$$R_{ci} = \frac{dI_{rci}}{dV_{rci}}$$

and `tf` is the model parameter.

If R_{ci} is not given,

© 2023 Cadence Design Systems, Inc.

$$F_t = \frac{g_m}{2\pi(c_{pi} + c_{bcx} + c_{mu})}$$

Temperature Equations

$$\Delta T = T - Tnom$$

$$R_t = \frac{T}{Tnom}$$

$$R_{cx} = R_{cxnom}\ R_t^{X_{rc}}$$

$$R_{ci} = R_{cinom}\ R_t^{X_{rc}}$$

$$R_{bp} = R_{bpnom}\ R_t^{X_{rc}}$$

$$R_{bx} = R_{bxnom}\ R_t^{X_{rb}}$$

$$R_{bi} = R_{binom} R_t^{X_{rb}}$$

$$R_e = R_{enom}\ R_t^{X_{re}}$$

$$R_s = R_{snom}\ R_t^{X_{rs}}$$

$$I_s = I_{snom}\ R_t^{X_{is}/NF_{nom}}\ e^{-E_a(1-R_t)/NF_{nom}\ V_{tm}}$$

$$I_{sp} = I_{spnom}\ R_t^{X_{is}/N_{fp}}\ e^{-E_a(1-R_t)/N_{fp}\ V_{tm}}$$

$$I_{bei} = I_{beinom}\ R_t^{X_{ii}/N_{ei}}\ e^{-E_{aie}(1-R_t)/N_{ei}\ V_{tm}}$$

© 2023 Cadence Design Systems, Inc.

$$I_{ben} = I_{bennom} \; R_t^{X_{in}/N_{en}} \; e^{-E_{ane}(1-R_t)/N_{en} \; V_{tm}}$$

$$I_{bci} = I_{bcinom} \; R_t^{X_{ii}/N_{ci}} \; e^{-E_{aic}(1-R_t)/N_{ci} \; V_{tm}}$$

$$I_{bcn} = I_{bcnnom} \; R_t^{X_{in}/N_{cn}} \; e^{-E_{anc}(1-R_t)/N_{cn} \; V_{tm}}$$

$$I_{beip} = I_{beipnom} \; R_t^{X_{ii}/N_{ci}V_{tm}} \; e^{-E_{aic}(1-R_t)/N_{ci} \; V_{tm}}$$

$$I_{benp} = I_{benpnom} \; R_t^{X_{in}/N_{cn}} \; e^{-E_{anc}(1-R_t)/N_{cn} \; V_{tm}}$$

$$I_{bcip} = I_{bcipnom} \; R_t^{X_{ii}/N_{cip}} \; e^{-E_{ais}(1-R_t)/N_{cip} \; V_{tm}}$$

$$I_{bcnp} = I_{bcnpnom} \; R_t^{X_{in}/N_{cnp}} \; e^{-E_{ans}(1-R_t)/N_{cnp} \; V_{tm}}$$

$$N_f = N_{fnom}(1 + T_{nf} \; \Delta T)$$

$$N_r = N_{rnom}(1 + T_{nf} \; \Delta T)$$

$$A_{vc2} = A_{vc2nom}(1 + T_{avc} \; \Delta T)$$

$$G_{amm} = G_{ammnom} \; R_t^{X_{is}} \; e^{-E_a\left(1 - \frac{T}{Tnom}\right)/V_{tm}}$$

$$V_o = V_{onom} \; R_t^{X_{vo}}$$

$$C_{je} = C_{jenom}\left(\frac{P_{enom}}{P_e}\right)^{M_e}$$

© 2023 Cadence Design Systems, Inc.

$$C_{jc} = C_{jcnom}\left(\frac{P_{cnom}}{P_c}\right)^{M_c}$$

$$C_{jep} = C_{jepnom}\left(\frac{P_{cnom}}{P_c}\right)^{M_c}$$

$$C_{jcp} = C_{jcpnom}\left(\frac{P_{snom}}{P_s}\right)^{M_s}$$

$$P_e = A_e + 2V_{tm}\ln\left[\frac{1}{2}\left(1+\sqrt{1+4e^{-A_e/V_{tm}}}\right)\right]$$

$$A_e = 2V_{tm}\ln(e^{PE_{nom}/2V_{tm}} - e^{-PE_{nom}/2V_{tm}})\ R_t - 3V_{tm}\ln(R_t) - E_{aie}(R_t-1)$$

$$P_c = A_c + 2V_{tm}\ln\left[\frac{1}{2}\left(1+\sqrt{1+4e^{-A_c/V_{tm}}}\right)\right]$$

$$A_c = 2V_{tm}\ln(e^{PC_{nom}/2V_{tm}} - e^{-PC_{nom}/2V_{tm}})\ R_t - 3V_{tm}\ln(R_t) - E_{aic}(R_t-1)$$

$$P_s = A_s + 2V_{tm}\ln\left[\frac{1}{2}\left(1+\sqrt{1+4e^{-A_s/V_{tm}}}\right)\right]$$

$$A_s = 2V_{tm}\ln(e^{PS_{nom}/2V_{tm}} - e^{-PS_{nom}/2V_{tm}})\ R_t - 3V_{tm}\ln(R_t) - E_{ais}(R_t-1)$$

Noise Equations

$$\overline{i_{Icc}^2} = 2\ q\ I_{cc}\Delta f$$

I_{be} shot and flicker noises:

© 2023 Cadence Design Systems, Inc.

$$\overline{i_{Ibe}^2} = 2\ q\ I_{be} + \frac{K_{fn}\ I_{be}^{A_{fn}}}{f^{B_{fn}}}\Delta f$$

R_{cx} thermal noise:

$$\overline{i_{Rcx}^2} = \frac{4K_t}{R_{cx}}$$

R_{ci} thermal noise:

$$\overline{i_{Rci}^2} = \frac{4K_t}{dI_{rci}}/(dV_{rci})$$

R_{bx} thermal noise:

$$\overline{i_{Rbx}^2} = \frac{4K_t}{R_{bx}}$$

R_{bi} thermal noise:

$$\overline{i_{Rbi}^2} = \frac{4K_t}{dI_{rbi}}/(dV_{rbi})$$

R_e thermal noise:

$$\overline{i_{RE}^2} = \frac{4K_t}{R_e}$$

R_s thermal noise:

$$\overline{i_{RS}^2} = \frac{4K_t}{R_e}$$

I_{ccp} shot noise:

$$\overline{i_{Rccp}^2} = 2\ q\ I_{ccp}$$

© 2023 Cadence Design Systems, Inc.

I_{bep} shot and flicker noises:

$$\overline{i_{Rbep}^2} = 2\ q\ I_{bep} + \frac{K_{fn}\ I_{bep}^{A_{fn}}}{f_{B_{fn}}}$$

R_{bp} thermal noise:

$$\overline{i_{Rbp}^2} = \frac{4K_t}{dI_{rbp}} / (dV_{rbp})$$

Related Topics

VBIC Model (vbic)

VBIC 1.2

Component Statements

VBIC 1.2

This section lists equations new for VBIC 1.2. The rest of the equations remain the same as VBIC 1.15 (previous section).

DC Current

$$I_{tr} = I_s(T) \cdot I_{srr}(T) \cdot \left(e^{V_{bci}/(N_r \cdot V_{tm})} - 1 \right)$$

If $Q_{bm} < \frac{1}{2}$

then

$$Q_b = \frac{1}{2} \cdot \left(Q_1 + \left(Q_1^{1/N_{kf}} + 4 \cdot Q_2 \right)^{N_{kf}} \right)$$

otherwise

© 2023 Cadence Design Systems, Inc.

$$Q_b = \frac{1}{2} \cdot Q_1 \cdot \left(1 + (1 + 4 \cdot Q_2)^{N_{kf}}\right)$$

If $(V_{be} > 0)$

$$I_{bei} = I_{bei(T)}\left(e^{V_{bei}/(N_{en} \cdot V_{tm})} - 1\right)$$

$$I_{ben} = I_{ben(T)}\left(e^{V_{bei}/(N_{en} \cdot V_{tm})} - 1\right)$$

$$I_{bbe} = I_{bbe(T)_{nom}} \cdot \left(e^{(-V_{bbe}(T) - V_{bei})/(N_{bbe}(T) \cdot V_{tm})} - E_{bbe}(T)\right)$$

then

$$I_{be} = W_{be} \cdot I_{bei(T)} + I_{ben(T)} - I_{bbe(T)}$$

If $V_{bex} > 0$

$$I_{bexi} = I_{bexi(T)}\left(e^{V_{bex}/(N_{en} \cdot V_{tm})} - 1\right)$$

$$I_{bexn} = I_{bexn(T)}\left(e^{V_{bex}/(N_{en} \cdot V_{tm})} - 1\right)$$

$$I_{bbex} = I_{bbex(T)_{nom}} \cdot \left(e^{(-V_{bbe}(T) - V_{bex})/(N_{bbe}(T) \cdot V_{tm})} - E_{bbe}(T)\right)$$

then

$$I_{bex} = (1 - W_{be}) \cdot (I_{bexi(T)} + I_{bexn(T)} - I_{bbex(T)})$$

If $V_{be} \leq 0$

```
{
    Ibei = - Ibei(T);
    Iben = - Iben(T);
    Ibbe =  0;
}
```


© 2023 Cadence Design Systems, Inc.

If $V_{bex} \le 0$

```
{
    Ibexi = - Ibexi(T);
    Ibexn = - Ibexn(T);
    Ibbex =  0;
}
```

Charge Equations

If $(A_{je} \le 0)$

{

If $V \le F_c P$

$$Q_j = \frac{P}{1-M}\left[1-\left(1-\frac{V}{P}\right)^{1-M}\right]$$

Else

$$Q_j = \frac{[1-Fc(1+M)]\cdot(V-FcP)+\frac{M\cdot(V^2-Fc^2p^2)}{2P}}{(1-Fc)^{M+1}}+\frac{P}{1-M}\left[1-\frac{1}{(1-Fc)^{M-1}}\right]$$

}

Else

{

$$Q_j = -\frac{P}{1-M}\cdot\left[\left(1-\frac{T1}{P}\right)^{1-M}-\left(1+\frac{1}{2P}\cdot\left(-FcP+\sqrt{Fc^2P^2+4Aj^2}\right)\right)^{1-M}\right]+$$
$$\frac{Vbe-T1-\frac{1}{2}\cdot\left(-FcP+\sqrt{Fc^2P^2+4Aj^2}\right)}{(1-Fc)^{M}}$$

and

© 2023 Cadence Design Systems, Inc.

$$T1 = \frac{1}{2}\left(V - FcP - \sqrt{(V - FcP)^2 + 4Aj^2}\right) + FcP$$

}

If $(A_{jc} > 0)$

If $(V_{rt}>0)\wedge(A_{rt}>0)$

then

$$dv0 = -(F_c \cdot P)$$

$$vn0 = \frac{V_{rt} + dv0}{V_{rt} - dv0}$$

$$v_{nl0} = \frac{2 \cdot vn0}{\sqrt{(vn0 - 1)^2 + 4 \cdot A_j^2} + \sqrt{(vn0 + 1)^2 + 4 \cdot A_{rt}^2}}$$

$$v_{l0} = \frac{1}{2} \cdot (v_{nl0} \cdot (V_{rt} - dv0) - V_{rt} - dv0)$$

$$Q_{l0} = P \cdot \frac{\left(1 - \left(1 - \frac{V_{l0}}{P}\right)^{1-M}\right)}{1 - M}$$

$$vn = \frac{2 \cdot V + V_{rt} + dv0}{V_{rt} - dv0}$$

$$vnl = \frac{2 \cdot vn}{\sqrt{(vn - 1)^2 + 4 \cdot A \cdot A} + \sqrt{(vn + 1)^2 + 4 \cdot A_{rt} \cdot A_{rt}}}$$

$$vl = \frac{1}{2} \cdot (vnl \cdot (V_{rt} - dv0) - V_{rt} - dv0)$$

$$Q_{jc0} = P \cdot \frac{\left(1 - \left(1 - \frac{vl}{P}\right)^{1-M}\right)}{1 - M}$$

© 2023 Cadence Design Systems, Inc.

$$sel = \frac{1}{2} \cdot (vnl + 1)$$

$$crt = \left(1 + \frac{V_{rt}}{P}\right)^{-M}$$

$$cl = (1 - sel) \cdot crt + sel \cdot cmx$$

$$Q_l = (V - vl + vl0) \cdot cl$$

$$Q_{jc} = Q_l + Q_{jc0} - Q_{l0}$$

else

$$vl = \frac{1}{2} \cdot \left(V - F_c \cdot P - \sqrt{(V - (F_c \cdot P))^2 + 4 \cdot A \cdot A}\right) + F_c \cdot P$$

$$vl0 = -\frac{1}{2} \cdot \left(-Fc \cdot P + \sqrt{(F_c \cdot P)^2 + 4 \cdot A \cdot A}\right)$$

$$Q_{j0} = -P \cdot \frac{\left(1 - \frac{vl0}{P}\right)^{1-M}}{1 - M}$$

$$Q_{lo} = -P \cdot \frac{\left(1 - \frac{vl}{P}\right)^{1-M}}{1 - M}$$

$$Q_{jc} = Q_{lo} + (1 - F_c)^{-M} \cdot (V - vl + vlo) - Q_{jo}$$

Temperature Equations

If self-heating is on, the device temperature is calculated by

$$T = T_{op} + DTEMP + V(rth)$$

If self-heating is off, the device temperature is calculated by

$$T = T_{op} + DTEMP$$

© 2023 Cadence Design Systems, Inc.

The model parameter extraction temperature is calculated by

$$T_{nom} = TNOM$$

$$R_t = \frac{T}{T_{nom}}$$

$$V_{tm} = \frac{K_B \cdot T}{Q_e}$$

$$\Delta T = T - T_{nom}$$

$$R_{cx}(T) = R_{cx} \cdot R_t^{X_{rcx}}$$

$$R_{bx}(T) = R_{bx} \cdot R_t^{X_{rbx}}$$

$$R_{bp}(T) = R_{bp} \cdot R_t^{X_{rbp}}$$

$$I_{sp}(T) = I_{sp} \cdot R_t^{X_{is}/N_{fp}} \cdot e^{-E_{ap}/N_{fp} \cdot (1 - R_t)/(V_{tm} \cdot N_{fp})}$$

Scaling Effects

For scaling effects, Scaling Factors (scale and scalem).

Related Topics

VBIC Model (vbic)

VBIC 1.1

Component Statements

© 2023 Cadence Design Systems, Inc.

Component Statements

The VBIC model was developed as a replacement for the SPICE G-P model. The model has four electrical terminals, two thermal terminals, and up to nine internal nodes, depending on the model parameters that the user specifies. VBIC 1.1.5 and VBIC 1.2 are implemented and controlled by model parameter version. Default is version=1.1.5. For more information about the model and the equations, refer to the Spectre Circuit Simulator Device Model Equations manual.

This device is supported within altergroups.

Sample Instance Statement

```
q1 (1 2 0 0 0) vbjt area=1
```

Sample Model Statement

```
model vbjt vbic type=npn is=2e-16 iben=4.5e-15 isp=1e-15 gamm=1.55e-11 ikf=0.0021
ikr=0.0021 vef=15 ver=7 rbi=35 rbx=7 re=3 rs=15 cje=1.5e-14 tf=15e-12 selft=yes
rth=1K
```

Instance Definition

```
Name  c  b  e  [s]  [dt]  [tl] ModelName parameter=value ...
```

`tl` node is the local temperature and the `dt` node is the rise above the local temperature caused by the thermal power dissipated by the device being modeled by VBIC. Consequently, the `tl` node can be connected to a thermal network that models heat flow through the substrate and/or between devices. It is not necessary to specify the substrate and the two thermal terminals. If unspecified, the substrate and the `tl` thermal terminal are connected to ground. However, if the self-heating flag is turned on and `dt` is not specified, an internal node is created for self-heating. You must specify the substrate terminal if you specify `dt`, and both substrate and `dt` must be specified if `tl` needs to be specified.

It is recommended not to use the `tl` node because it is not fully supported and using it will degrade the convergence properties. This node was removed in the VBIC 1.2 version. All thermal effects can be modeled with just the `dt` node.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

`area=1`	The area factor of the transistor.
`m=1`	Multiplicity factor.
`region=fwd`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `fwd`, `rev`, `sat`, or `breakdown`.
`trise`	Temperature rise from ambient.
`dtmp`	Alias to trise.
`dtemp`	Alias to trise.
`isnoisy=yes`	Determines if the device should generate noise. Possible values are `no` or `yes`.

small-signal model parameters

Model Definition

```
model modelName vbic parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Structural parameters

`type=npn`	The type of transistor. Possible values are `npn` or `pnp`.
`compatible=spectre`	Encourages device equations to be compatible with a foreign simulator. This option does not affect the input syntax. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, or `mica`.

Saturation current parameters

`is=1e-16 A`	Transport saturation current (*area).
`ibei=1e-18 A`	Ideal B-E saturation current. (*area).
`iben=0 A`	Nonideal B-E saturation current (*area).
`ibci=1e-16 A`	Ideal B-C saturation current. (*area).
`ibcn=0 A`	Nonideal B-C saturation current (*area).
`isp=0 A`	Parasitic transport saturation current. (*area).
`ibeip=0 A`	Ideal parasitic B-E saturation current (*area).
`ibenp=0 A`	Nonideal parasitic B-E saturation current (*area).
`ibcip=0 A`	Ideal parasitic B-C saturation current (*area).
`ibcnp=0 A`	Non-ideal parasitic B-C saturation current (*area).
`vo=0 V`	Epi drift saturation voltage.
`gamm=0 V`	Epi doping parameter.
`hrcf=1`	High current RC factor.
`wbe=1`	Portion of Ibei from Vbei.
`wsp=1`	Portion of Iccp from Vbep.

Emission coefficient parameters

`nf=1`	Forward emission coefficient.

© 2023 Cadence Design Systems, Inc.

`nr=1`	Reverse emission coefficient.
`nei=1`	Ideal B-E emission coefficient.
`nen=2`	Nonideal B-E emission coefficient.
`nci=1`	Ideal B-C emission coefficient.
`ncn=2`	Nonideal B-C emission coefficient.
`nfp=1`	Parasitic forward emission coefficient.
`ncip=1`	Ideal parasitic B-C emission coefficient.
`ncnp=2`	Nonideal parasitic B-C emission coefficient.

© 2023 Cadence Design Systems, Inc.

Current gain parameters

`ikf=∞ A`	Forward knee current (*area).
`ikr=∞ A`	Reverse knee current (*area).
`ikp=∞ A`	Parasitic knee current (*area).

Early voltage parameters

`vef=∞ V`	Forward Early voltage.
`ver=∞ V`	Reverse Early voltage.

Breakdown voltage parameters

`avc1=0`	B-C weak avalanche parameter.
`avc2=0`	B-C weak avalanche parameter.

Parasitic resistance parameters

`rbi=0 Ω`	Intrinsic base resistance (/area).
`rbx=0 Ω`	Extrinsic base resistance (/area).
`re=0 Ω`	Emitter resistance (/area).
`rs=0 Ω`	Substrate resistance (/area).
`rbp=0 Ω`	Parasitic base resistance (/area).
`rcx=0 Ω`	Extrinsic collector resistance (/area).
`rci=0 Ω`	Intrinsic collector resistance (/area).
`minr=0.01 Ω`	Minimum parasitic resistance.

Junction capacitance parameters

`cje=0 F`	B-E zero-bias capacitance (*area).
`pe=0.75 V`	B-E built-in potential.
`me=0.33`	B-E grading coefficient.

© 2023 Cadence Design Systems, Inc.

`aje=-0.5`	B-E capacitance smoothing factor.
`fc=0.9`	Forward-bias depletion capacitance limit.
`cbeo=0 F`	Extrinsic B-E overlap capacitance (*area).
`cjc=0 F`	B-C zero-bias capacitance (*area).
`cjep=0 F`	B-C extrinsic zero-bias capacitance (*area).
`pc=0.75 V`	B-C built-in potential.
`mc=0.33`	B-C grading coefficient.
`ajc=-0.5`	B-C capacitance smoothing factor.
`cbco=0 F`	Extrinsic B-C overlap capacitance (*area).
`qco=0 Coul`	Epi charge parameter.
`cjcp=0 F`	S-C zero-bias capacitance (*area).
`ps=0.75 V`	S-C built-in potential.
`ms=0.33`	S-C grading coefficient.
`ajs=-0.5`	S-C capacitance smoothing factor.

© 2023 Cadence Design Systems, Inc.

Transit time and excess phase parameters

`tf=0 s`	Forward transit time.
`tr=0 s`	Reverse transit time.
`td=0 s`	Forward excess-phase delay time.
`qtf=0`	Variation of `tf` with base width modulation.
`xtf=0`	Coefficient of `tf` with bias dependence.
`vtf=0`	Coefficient of `tf` dependence on Vbc.
`itf=0`	Coefficient of `tf` dependence on Ic.

Temperature effects parameters

`selft=no`	Flag denoting self-heating. Possible values are `no` or `yes`.
`tnom (C)`	Parameters measurement temperature. Default set by options.
`trise=0 C`	Temperature rise from ambient.
`rth=0 Ω`	Thermal resistance, must be given for self-heating.
`cth=0 F`	Thermal capacitance.
`xis=3 V`	Temperature exponent of Is.
`xii=3 V`	Temperature exponent of Ibei, Ibci, Ibeip, and Ibcip.
`xin=3 V`	Temperature exponent of Iben, Ibcn, Ibenp, and Ibcnp.
`tnf=0 V`	Temperature coefficient of Nf.
`tavc=0 V`	Temperature coefficient of Avc2.
`ea=1.12 V`	Activation energy for `is`.
`eaie=1.12 V`	Activation energy for Ibei.
`eaic=1.12 V`	Activation energy for Ibci/Ibeip.
`eais=1.12 V`	Activation energy for Ibcip.
`eane=1.12 V`	Activation energy for Iben.
`eanc=1.12 V`	Activation energy for Ibcn/Ibenp.

© 2023 Cadence Design Systems, Inc.

`eans=1.12 V`	Activation energy for Ibcnp.
`xre=0`	Temperature exponent of `re`.
`xrb=0`	Temperature exponent of `rb`.
`xrc=0`	Temperature exponent of `rc`.
`xrs=0`	Temperature exponent of `rs`.
`xvo=0`	Temperature exponent of `vo`.
`dtmax=226.85 C`	Maximum expected device temperature. (500 K).

© 2023 Cadence Design Systems, Inc.

Noise model parameters

`kfn=0`	B-E flicker (1/f) noise coefficient.
`afn=1`	B-E flicker (1/f) noise exponent.
`bfn=1`	B-E flicker (1/f) noise dependence.

Junction diode model control parameters

`dskip=yes`	Skip junction calculations if they are reverse-saturated. Possible values are `no` or `yes`.
`imelt=10 A`	Explosion current (*area).

Operating region warning control parameters

`bvbe=∞ V`	B-E breakdown voltage.
`bvbc=∞ V`	B-C breakdown voltage.
`bvce=∞ V`	C-E breakdown voltage.
`bvsub=∞ V`	Substrate junction breakdown voltage.
`vbefwd=0.2 V`	B-E forward voltage.
`vbcfwd=0.2 V`	B-C forward voltage.
`vsubfwd=0.2 V`	Substrate junction forward voltage.
`imax=1 A`	Maximum allowable base current (*area).
`imax1=`imax' A`	Maximum allowable collector current (*area).
`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `fwd`, `rev`, or `sat`.

DC-mismatch model parameters

`mvt0=0.0 V`	Threshold mismatch intercept.

New model parameter for Vbic 1.2

`vrt=0 V`	B-C reach-through limiting voltage.

© 2023 Cadence Design Systems, Inc.

art=0.1 V	B-C reach-through limiting smoothing factor .
ccso=0 F	Fixed collector-substrate capacitance.
qbm=0	Parameter to select SGP qb formulation.
nkf=0.5	High current beta rolloff parameter.
xikf=0	Parameter of temperature dependence to ikf.
xrcx=0	Parameter of temperature dependence to rcx.
xrbx=0	Parameter of temperature dependence to rbx.
xrbp=0	Parameter of temperature dependence to rbp.
isrr=1	Parameter to separate is for forward and reversed parts.
xisr=0	Temperature exponent coefficient of isrr.
dear=0 V	Activation energy for isrr.
eap=1.12 V	Activation energy for isp.
vbbe=0 V	B-E breakdown voltage.
nbbe=1.0	B-E breakdown emission coefficient.
ibbe=1.0e-6 A	B-E breakdown current.
tvbbe1=0	First temperature coefficient of vbbe.
tvbbe2=0	Second temperature coefficient of vbbe.
tnbbe=0	Temperature coefficient for nbbe.
vers=1.15	Version control parameter.
vrev=0	Revision control parameter.
dtmp (C)	Alias to trise.
dtemp (C)	Alias to trise.
version	Alias to vers.
rev	Alias to vrev.
xrbi	Alias to xrb.
xrci	Alias to xrc.

© 2023 Cadence Design Systems, Inc.

Shrink Parameters

`shrink=0.0`	Linear shrink parameter.
`shrink2=0.0`	Area shrink parameter.

Imax and Imelt

The `imax` parameter aids in convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for the value of current up to `imax`. If the value of `imax` exceeds during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and a warning message is displayed.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, given that the base and collector currents are composed of many exponential terms, the results become inaccurate and a warning message is displayed. The junction current is linearized to above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`type=npn`	The type of transistor. Possible values are `npn` and `pnp`.
`region=fwd`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `fwd`, `rev`, `sat`, and `breakdown`.
`trise (C)`	Temperature rise from ambient.
`vbe (V)`	Base-emitter voltage.
`vbc (V)`	Base-collector voltage.
`vce (V)`	Collector-emitter voltage.
`vcs (V)`	Collector-substrate voltage.
`temp (C)`	Device temperature.
`ith (A)`	Thermal source.
`ic (A)`	Intrinsic DC collector current. (Icc - Ibc + Igc).
`ib (A)`	Intrinsic DC base current. (Ibe + Ibc - Igc).
`icc (A)`	C-E current.
`ibe (A)`	Intrinsic B-E junction current.
`ibc (A)`	Intrinsic B-C junction current.
`ibex (A)`	BX-E junction current.
`igc (A)`	Breakdown current.
`iccp (A)`	Parasitic transport C-E current.
`ibep (A)`	Parasitic transport B-E current.
`ibcp (A)`	Parasitic transport B-C current.
`betadc (A/A)`	Ratio of external collector current to external base current. (ic_ext/ib_ext).
`rcx_t (Ω)`	Temperature-dependent extrinsic collector resistance (/area).
`rci_t (Ω)`	Temperature-dependent intrinsic collector resistance (/area).
`rbp_t (Ω)`	Temperature-dependent parasitic transistor base resistance (/area).

© 2023 Cadence Design Systems, Inc.

`rbx_t (Ω)`	Temperature-dependent extrinsic base resistance (/ area).
`rbi_t (Ω)`	Temperature-dependent intrinsic base resistance (/ area).
`re_t (Ω)`	Temperature-dependent emitter resistance (/area).
`rs_t (Ω)`	Temperature-dependent substrate resistance (/ area).
`gm (S)`	Intrinsic small-signal transconductance. (gm = dIcc_dVbe + dIcc_dVbc).
`gpi (S)`	Intrinsic small-signal input conductance. (gpi = dIbe_dVbe).
`go (S)`	Intrinsic small-signal output conductance. (go = -dIcc_dVbc).
`gmu (S)`	Intrinsic small-signal Collector-Base conductance. (gmu = dIbc_dVbc).
`cpi (F)`	Intrinsic small-signal B-E capacitance. Same as cje.
`cmu (F)`	Intrinsic small signal B-C capacitance. Same as cjc.
`betaac (A/A)`	Small-signal common-emitter current gain. (gm/ gpi).
`ft (Hz)`	Unity small-signal current-gain frequency.
`dic_dvbe (S)`	Intrinsic dIc/dVbe.
`dic_dvbc (S)`	Intrinsic dIc_dVbc.
`dib_dvbe (S)`	Intrinsic dIb_dVbe.
`dib_dvbc (S)`	Intrinsic dIb_dVbc.
`rbi (Ω)`	Intrinsic base resistance.
`rci (Ω)`	Intrinsic collector resistance.
`rbp (Ω)`	Parasitic transistor base resistance.
`cje (F)`	Intrinsic B-E capacitance.
`cjc (F)`	Intrinsic B-C capacitance.
`cbex (F)`	BX-E junction capacitance.
`cbcx (F)`	B-CX junction capacitance.

© 2023 Cadence Design Systems, Inc.

`cbep (F)`	Parasitic B-E junction capacitance.
`cbcp (F)`	Parasitic B-C junction capacitance.
`pwr (W)`	Power dissipation.

Related Topics

VBIC Model (vbic)

VBIC 1.2

VBIC 1.1

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

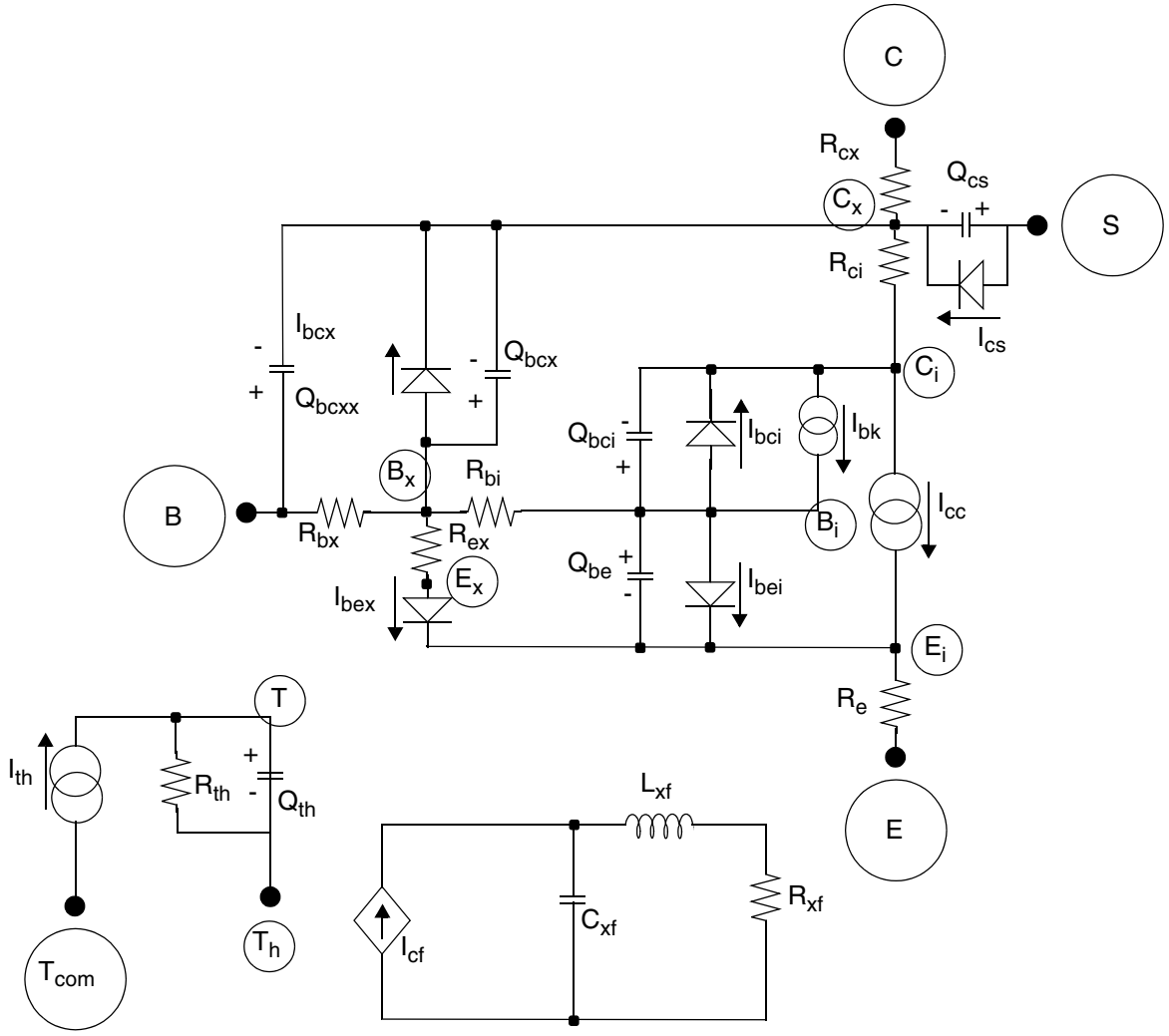
9

HBT Model (ucsd_hbt)

This topic contains the following information for the UCSD HBT model:

- DC Current
- Junction Capacitance
- Total Charge
- Thermal Current Equations
- Temperature Equations
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.



Thermal network Excess phase

DC Current

$$I_{cc} = I_{cf} - I_{cr}$$

$$I_{cf} = \frac{I_s}{\Delta}(e^{V_{be}/N_r(V_{tm})} - 1)$$

© 2023 Cadence Design Systems, Inc.

$$I_{cr} = \frac{I_s}{\Delta}(e^{V_{bc}/N_r(V_{tm})} - 1)$$

$$\Delta = Q_b + \frac{I_s}{I_{sa}}e^{V_{be}/N_a(V_{tm})} + \frac{I_s}{I_{sb}}e^{V_{bc}/N_b(V_{tm})}$$

$$Q_b = \frac{Q_1}{2}(1 + \sqrt{1 + 4Q_2})$$

$$Q_1 = \frac{1}{1 - \frac{V_{bc}}{V_{af}} - \frac{V_{be}}{V_{ar}}}$$

$$Q_2 = \frac{I_s}{I_k}(e^{V_{be}/N_f(V_{tm})} - 1)$$

$$I_{be} = \frac{I_{cf}}{B_f} + I_{se}(e^{V_{be}/N_e(V_{tm})} - 1)$$

$$I_{bex} = I_{sex}(e^{V_{bex}/N_{ex}(V_{tm})} - 1)$$

$$I_{bc} = \frac{I_{cr}}{B_r} + I_{sc}(e^{V_{be}/N_c(V_{tm})} - 1)$$

$$I_{bcx} = I_{scx}(e^{V_{bcx}/N_{cx}(V_{tmop})} - 1)$$

$$I_{cs} = I_{cs}(e^{-V_{cs}/N_{cs}(V_{tmop})} - 1)$$

$$I_{bk} = \begin{cases} 0 & \text{if } B_{kdn} = 0 \\ (M_f - 1)I_{cf} & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$M_f = \begin{cases} \dfrac{1}{1-\left(\dfrac{-V_{bc}}{B_{vc}}\right)^{N_{bc}}} & \text{if } V_{tm} < -V_{bc} < F_a(B_{vc}) \\ 1 & \text{if } -V_{bc} < V_{tm} \\ M_{f1} + g_1(-V_{bc} - F_a(B_{vc})) & -V_{bc} < F_a(B_{vc}) \end{cases}$$

$$M_{f1} = \frac{1}{1 - F_a^{N_{bc}}}$$

$$g_1 = M_{f1}(M_{f1} - 1)\frac{N_{bc}}{F_a(B_{vc})}$$

Junction Capacitance

Define

$$V_{min} = V_j\left[1 - \left(\frac{C_j}{C_{min}}\right)^{1/M_j}\right]$$

If $V < V_{min}$,

$$C_j = C_{min}$$

$$Q_j = C_{min}(V - V_j) + C_{min}(V_j)\left(\frac{M_j}{M_j - 1}\right)\left(\frac{C_j}{C_{min}}\right)^{1/M_j}$$

If $V < F_c(V_j)$,

$$C_j = \frac{C_j}{\left(1 - \dfrac{V}{V_j}\right)^{M_j}}$$

© 2023 Cadence Design Systems, Inc.

If $V > F_c(V_j)$ and $C_j \geq C_{min}(1 - F_c)^{Mj}$,

$$C_j = \frac{C_j}{(1 - F_c)^{M_j}}[1 + M_j(V_R)]$$

$$Q_j = \frac{-C_j}{(1 - F_c)^{M_j}}\left[\frac{1}{1 - M_j} - V_r - \frac{M_j(V_R^2)}{2}\right]$$

where

$$V_R = \frac{V - F_c(V_j)}{V_j - F_c(V_j)}$$

If $V > F_c(V_j)$ and $C_j < C_{min}(1 - F_c)^{Mj}$,

$$C_j = C_{min} + \frac{C_j(M_j)(V_R)}{(1 - F_c)^{M_j}}$$

$$Q_j = C_{min}\left(V - V_{min} - \frac{V_j - V_{min}}{1 - M_j}\right) + \frac{C_j(M_j)(V - F_c(V_j))(V_R)}{2(1 - F_c)^{M_j}}$$

Total Charge

$$Q_{be} = Q_{je} + (1 - F_{ex})Q_{fdiff}$$

where Q_{je} is the junction charge Q_j with $V = V_{be}$.

$$Q_{bc} = Q_{jc} + T_r(I_{cr}) + F_{ex}(Q_{fdiff})$$

$$Q_{bcx} = T_{rx}(I_{bcx}) + X_{cjc}(Q_{jcx})$$

© 2023 Cadence Design Systems, Inc.

$$Q_{bcxx} = (1 - X_{cjc})Q_{jcxx}$$

$$Q_{cs} = Q_{js}$$

$$Q_{fdiff} = I_{cf}(F_{tt})\left(T_{fbt} + \frac{T_{fco}}{Q_{cc}} + Q_{bcm} + Q_{krk}\right)$$

where

$$F_{tt} = R_{td}^{X_{ttf}}$$

$$T_{fbt} = T_{fb}\left(1 + \frac{V_{bc}}{V_{af}} + \frac{V_{be}}{V_{ar}}\right) + T_{bexs}(e^{-(V_{be} - V_{je})/N_a(V_{tm})}) + T_{bcxs}(e^{-(V_{bc} - V_{jc})/N_b(V_{tm})})$$

$$Q_{cc} = \frac{1 + (I_{cf})^2}{1 + \left(\frac{I_{cf}}{I_{tc2}}\right)^3 + \left(\frac{V_{jc} - V_{bc}}{V_{tc}}\right)}$$

$$Q_{krk} = T_{krk}(I_{cj})e^{(V_{bc}/V_{krk} + I_{cf}/I_{krk})}$$

$$Q_{bcm} = Q_{bcf} - Q_{jc}$$

where Q_{bcf} is calculated according to the following rules:

Define

$$I_o = \frac{I_{cf}}{I_{crit}}$$

where

$$I_{crit} = I_{crito}\left(\frac{Q_{cc}}{F_{tt}}\right)$$

© 2023 Cadence Design Systems, Inc.

$$C_{jch} = \begin{cases} C_{jc}\left((1-I_o)^{M_{jc}}\right) & \text{If } I_o < 1 \\ -C_{jc}\left((I_o-1)^{M_{jc}}\right) & \text{otherwise} \end{cases}$$

If $C_{jch} < 0$,

$$Q_{bcf} = C_{cmin}(V_{bc}-V_{jc}) - \frac{C_{cmin}(V_{jc})(M_{jc})}{M_{jc}-1}\left(-\frac{C_{jch}}{C_{cmin}}\right)^{1/M_{jc}}$$

If $C_{jch} \geq 0$, define

$$V_{min1} = V_{jc}\left[1-\left(\frac{C_{jch}}{C_{cmin}}\right)^{1/M_{jc}}\right]$$

If $V_{bc} < F_c(V_{jc})$ and $V_{bc} < V_{min1}$,

$$Q_{bcf} = C_{cmin}(V_{bc}-V_{jc}) + \frac{C_{cmin}(V_{jc})(M_{jc})}{M_{jc}-1}\left(\frac{C_{jch}}{C_{cmin}}\right)^{1/M_{jc}}$$

If $V_{bc} < F_c(V_{jc})$ and $V_{bc} \geq V_{min1}$,

$$Q_{bcf} = -\frac{C_{jch}(V_{jc})}{1-M_{jc}}\left(1-\frac{V_{bc}}{V_{jc}}\right)^{1-M_{jc}}$$

If $V_{bc} \geq F_c(V_{jc})$ and $C_{jch} > C_{min}(1-F_c)^{Mjc}$,

$$Q_{bcf} = \frac{-C_{jch}(V_{jc}-F_c(V_{jc}))}{(1-F_c)^{M_{jc}}}\left[\frac{1}{1-M_{jc}} - V_{RC} - \frac{M_{jc}(V_{RC}^2)}{2}\right]$$

where

$$V_{RC} = \frac{V_{bc}-F_c(V_j)}{V_j-F_c(V_j)}$$

© 2023 Cadence Design Systems, Inc.

If $V_{bc} \geq F_c(V_{jc})$ and $C_{jch} \leq C_{min}(1 - F_c)^{Mjc}$,

$$Q_{bcf} = C_{cmin}\left(V_{bc} - V_{min1} - \frac{V_{jc} - V_{min1}}{1 - M_{jc}}\right) + \frac{C_{jch}(M_{jc})(V_{bc} - F_c(V_{jc}))V_{R_c}}{2(1 - F_c)^{M_{jc}}}$$

Thermal Current Equations

$$I_{th} = I_{cc}(V_{ce}) + I_{be}(V_{be}) + I_{bex}(V_{bex}) + I_{bcx}(V_{bcx}) + (I_{bc} - I_{bk})(V_{bc} - I_{cs})(V_{cs})$$
$$+ \frac{V_{bbx}^2}{R_{bx}} + \frac{V_{bxex}^2}{R_{ex}} + \frac{V_{bxbi}^2}{R_{bi}} + \frac{V_{eei}^2}{R_e} + \frac{V_{ccx}^2}{R_{cx}} + \frac{V_{cxci}^2}{R_{ci}}$$

Temperature Equations

$$\Delta T = T - Tnom$$

$$V_{tm} = \frac{kT}{q}$$

$$V_{tmop} = \frac{kT_{op}}{q}$$

$$V_{tmnom} = \frac{kTnom}{q}$$

$$R_{td} = \frac{T}{Tnom}$$

$$R_{top} = \frac{T_{op}}{Tnom}$$

$$R_{th} = R_{thnom}\left(R_{td}^{X_{rt}}\right)$$

© 2023 Cadence Design Systems, Inc.

$$R_{cx} = R_{cxnom}\left(R_{t_op}^{X_{rc}}\right)$$

$$R_{ci} = R_{cinom}\left(R_{t_op}^{X_{rc}}\right)$$

$$R_{bx} = R_{bxnom}\left(R_{t_op}^{X_{rb}}\right)$$

$$R_{bi} = R_{binom}\left(R_{t_op}^{X_{rb}}\right)$$

$$R_{e} = R_{enom}\left(R_{t_op}^{X_{re}}\right)$$

$$R_{ex} = R_{exnom}\left(R_{t_op}^{X_{rex}}\right)$$

$$I_s = I_{snom}\left(R_{td}^{X_{ti}}\right)\left(e^{E_g(R_{td}-1)/V_{tm}}\right)$$

$$I_{sa} = I_{sanom}\left(R_{td}^{X_{ti}}\right)\left(e^{(E_g+E_{aa})(R_{td}-1)/V_{tm}}\right)$$

$$I_{sb} = I_{sbnom}\left(R_{td}^{X_{ti}}\right)\left(e^{(E_g+E_{ab})(R_{td}-1)/V_{tm}}\right)$$

$$B_f = B_{fnom}\left(R_{td}^{X_{tb}}\right)$$

$$B_r = B_{rnom}\left(R_{td}^{X_{tb}}\right)$$

$$I_{se} = I_{senom}\left(R_{td}^{(X_{ti}/N_e - X_{tb})}\right)\left(e^{(E_g+E_{ae})/N_e(V_{tm}) - (E_g+E_{ae})/N_{enom}(V_{tmnom})}\right)$$

© 2023 Cadence Design Systems, Inc.

$$N_e = N_{enom} + T_{ne}(\Delta T)$$

$$I_{sc} = I_{scnom}\left(R_{td}^{(X_{ti}/N_c - X_{tb})}\right)\left(e^{(E_g + E_{ac})/N_c(V_{tm}) - (E_g + E_{ac})/N_{cnom}(V_{tmnom})}\right)$$

$$N_c = N_{cnom} + T_{nc}(\Delta T)$$

$$I_{sex} = I_{sexnom}\left(R_{td}^{X_{ti}/N_{ex} - X_{tb}}\right)\left(e^{(E_g + E_{ax})/N_{ex}(V_{tm}) - (E_g + E_{ax})/N_{exnom}(V_{tmnom})}\right)$$

$$N_{ex} = N_{exnom} + T_{nex}(\Delta T)$$

$$V_j = V_{jnom} - T_{vj}(T_{op} - Tnom)$$

$$C_j = C_{jnom}\left(\frac{V_{jnom}}{V_j}\right)^{M_j}$$

$$I_{tc} = I_{tcnom}\left(R_{td}^{X_{titc}}\right)$$

$$I_{tc2} = I_{tc2nom}\left(R_{td}^{X_{titc2}}\right)$$

$$T_{krk} = T_{krknom}\left(R_{top}^{X_{ttkrk}}\right)$$

$$V_{krk} = V_{krknom}\left(R_{top}^{X_{tvkrk}}\right)$$

$$I_{krk} = I_{krknom}\left(R_{top}^{X_{tikrk}}\right)$$

Scaling Effects

For scaling effects, Scaling Factors (scale and scalem).

© 2023 Cadence Design Systems, Inc.

Component Statements

Sample Instance Statement

```
q7 (net5 net2 0) hbtmod m=1 top=25
```

Sample Model Statement

```
model hbtmod hbt type=npn bf=500 br=1000 xtb=-2.4 xti=0 xcjc=0.83 mje=0.34 fc=0.5
eg=1.2 ise=5.5e-15 vjc=0.84 vaf=40 cjc=5.1e-15
```

Instance Syntax

```
Name  c  b  e  s [t] ModelName parameter=value ...
```

The thermal node is an optional node. If it is specified, then it is the external thermal terminal. If it is not specified, and self heating effect is turned on by using `selft=1`, then an internal thermal node will be created.

Instance Parameters

`area=1`	Transistor area factor.
`m=1`	Multiplicity factor.
`isnoisy=yes`	Should resistor generate noise. Possible values are `yes` or `no`.
`trise=0 C`	Variability in device temperature.
`selft=0`	Self-Heating flag as an instance parameter.

Model Syntax

```
model modelName hbt parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`version=2`	Model Version.
`level=2`	Model Level.
`compatible=0`	Possible values are `SPECTRE` and `NI`.
`abel=0.0 A`	Base-Emitter current: Portion of base-emitter current allocated to extrinsic region.
`af=1.5`	Flicker noise exponent.
`area=1.0`	Device area factor (Does not scale parasitic inductors or capacitors).
`cjc=0.0 F`	Base-collector capacitance: zero-bias capacitance.
`cje=0.0 F`	Base-emitter capacitance: zero-bias capacitance.
`cjs=0.0 F`	Substrate depletion capacitance at zero voltage.
`cpbc=0.0 F`	Parasitic / fringing base-collector capacitance.
`cpbe=0.0 F`	Parasitic / fringing base-emitter capacitance.
`cpce=0.0 F`	Parasitic / fringing collector-emitter capacitance.
`dtmax=500 C`	Alias of ETMAXTEMP. Maximum temperature rise above heatsink in Celsius degrees.
`etmaxtemp=500 C`	Maximum temperature rise above heatsink in Celsius degrees.
`eaa=0.0 V`	Temperature dependence of ISA.
`eab=0.0 V`	Temperature dependence of ISB.
`ffe=1.0`	Flicker noise frequency exponent.
`ics=1.0e-30 A`	Saturation value for collector-substrate current.
`ik=1e10 A`	High current roll-off in Beta.
`ikrk=1e3 A`	Kirk effect: critical current for Kirk effect at Vbc=0.
`imax=10.0 A`	Explosion current.
`is=1e-25 A`	Collector-Emitter current: Forward collector saturation current.
`isa=1e10 A`	Base-emitter heterojunction saturation current (BE barrier effects).

© 2023 Cadence Design Systems, Inc.

`isb=1e10 A`	Base-collector heterojunction saturation current (BC barrier effects).
`isc=1e-30A`	Base-Collector current: Non-ideal base-collector saturation current.
`ise=1e-30 A`	Base-Emitter current: Non-ideal base-emitter current.
`itc=0 A`	Collector transit time: midpoint in collector current between TFC0 and TCMIN.
`itc2=0 A`	Collector transit time: transition width in collector current between TFC0 and TCMIN.
`kf=0`	Flicker noise coefficient.
`lpb=0 H`	Parasitic base inductance.
`lpc=0 H`	Parasitic collector inductance.
`lpe=0 H`	Parasitic emitter inductance.
`mjc=0.33`	Base-collector capacitance: grading factor (0.1<MJC).
`mje=0.5`	Base-emitter capacitance: grading factor (0.1<MJE).
`mjs=0.5`	Exponent for voltage variation of C-S Cj.
`na=2`	Base-emitter heterojunction ideality factor.
`nb=2`	Base-collector heterojunction ideality factor.
`nc=2`	Base-Collector current: Non-ideal base-collector current ideality factor.
`ncs=2`	Ideality factor for collector-substrate current.
`ne=2`	Base-Emitter current: Non-ideal base-emitter current ideality factor.
`nf=1`	Collector-Emitter current: Forward collector current ideality factor.
`nr=1`	Collector-Emitter current: Reverse emitter current ideality factor.
`rbi=0 W`	Intrinsic base resistance.
`rbx=0 W`	Extrinsic base resistance.

© 2023 Cadence Design Systems, Inc.

`rci=0 W`	Intrinsic collector resistance.
`rcx=0 W`	Extrinsic collector resistance.
`re=0 W`	Emitter resistance.
`tbp=298.15 K`	Base-plate temperature. Specifying this parameter enables partial Self Heating. Self-consistent (or dynamic) temperature is obtained by adding temperature rise due to power dissipation and TBP.
`tfb=0 s`	Base transit time: delay through the base.
`tfc0=0 s`	Collector transit time: low current transit time.
`tkrk=0 s`	Kirk effect: Kirk effect delay time.
`tnom=27 C`	Parameters measurement temperature. Default value is set by options.
`tr=0.35e-9 s`	Reverse transit time.
`tvjc=0 V/K`	Rate of change in temperature of VJC (Volt/K).
`tvje=0 V/K`	Rate of change in temperature of VJE (Volt/K).
`tvjs=0 V/K`	Coefficient for VJS temperature dependence.
`vaf=1000 V`	Forward Early voltage.
`var=1000 V`	Reverse Early voltage.
`vjc=1.4 V`	Base-collector capacitance: built-in voltage.
`vje=1.6 V`	Base-emitter capacitance: built-in voltage.
`vjs=1.4 V`	Built-in potential for substrate capacitance.
`vkrk=10.0 V`	Kirk effect: rate of change of IKRK with Vcb.
`xrb=0`	Temperature exponent for RBI and RBX.
`xrc=0`	Temperature exponent for RCI and RCX.
`xre=0`	Temperature exponent for RE.
`xikrk=0`	Alias of XTIKRK. Temperature exponent for IKRK.
`xtikrk=0`	Temperature exponent for IKRK.
`xitc=0`	Alias of XTITC. Temperature exponent for ITC.
`xtitc=0`	Temperature exponent for ITC.
`xitc2=0`	Alias of XTITC2. Temperature exponent for ITC2.

© 2023 Cadence Design Systems, Inc.

`xtitc2=0`	Temperature exponent for ITC2.
`xttkrk=0`	Temperature exponent for TKRK.
`xtkrk=0`	Alias of XTTKRK. Temperature exponent for TKRK.
`xtvkrk=0`	Temperature exponent for VKRK.
`xvkrk=0`	Alias of XTVKRK. Temperature exponent for VKRK.
`selft=0`	Self-Heating flag.
`bkdn=0`	Breakdown current flag.
`ext_flag=0`	ADS-Extensions flag.
`compat=0`	Compatible flag.
`partialsh=0`	Partial self-heating flag.
`nflag=0`	Noise flag.
`type=1`	Transistor type. Possible values are `pnp` and `npn`.
`bf=10000 A/A`	Forward ideal current gain (beta).
`br=10000 A/A`	Reverse ideal current gain.
`isex=1e-30 A`	Saturation current for emitter leakage diode.
`nex=2`	Ideality factor for emitter leakage diode.
`iscx=1e-30 A`	Saturation current for extrinsic BC junction current.
`ncx=2`	Ideality factor for extrinsic BC junction current.
`fa=0.9`	Factor to specify avalanche voltage.
`bvc=1000 V`	C-B breakdown voltage (BVcb0); positive.
`nbc=8`	Exponent for BC multiplication factor vs. voltage.
`rex=1e-3 W`	Extrinsic emitter leakage diode series resistance.
`cemin=1e-40 F`	Min value of intrinsic BE capacitance.
`fce=0.8`	Factor for BE capacitance approximation near Vbi.
`ccmin=1e-40 F`	Min value of intrinsic BC capacitance.
`fc=0.8`	Factor for BC capacitance approximation near Vbi.
`cjcx=0.0 F`	Extrinsic BC capacitance at zero voltage.
`vjcx=1.4 V`	Extrinsic BC capacitance Vbi.

© 2023 Cadence Design Systems, Inc.

`mjcx=0.33`	Extrinsic base-collector capacitance: grading factor (0.1<MJCX).
`cxmin=1e-40 F`	Minimum extrinsic BC capacitance.
`xcjc=1`	Factor for partitioning BC capacitance.
`tbcxs=0`	Excess BC transit time.
`tbexs=0`	Excess BE transit time.
`icrit0=1e3 A`	Critical current for junction capacitance.
`vtc=1e3 V`	Characteristic voltage for TFC.
`trx=0 s`	Reverse storage time for extrinsic BC diode.
`fex=0 s`	Excess phase factor.
`rth=1e-8 W`	Thermal resistance of device.
`cth=1e-6 F`	Thermal capacitance of device.
`xti=2`	Exponent for IS temperature dependence.
`xtb=2`	Exponent for beta temperature dependence.
`tnc=0`	Coefficient for NC temperature dependence.
`tne=0`	Coefficient for NE temperature dependence.
`tnex=0`	Coefficient for `nex` temperature dependence.
`eg=1.5 V`	Activation energy for IS temperature dependence.
`eac=0 V`	Activation energy for ISC temperature dependence.
`eae=0 V`	Activation energy for ISE temperature dependence.
`eax=0 V`	Activation energy for ISEX temperature dependence.
`xrex=0`	Coefficient for REX temperature dependence.
`tvjcx=0 V/C`	Coefficient for VJCX temperature dependence.
`xttf=0`	Coefficient for TF temperature dependence.
`xrt=0`	Coefficient for RTH temperature dependence.
`tvpe=0 V/K`	Rate of change in temperature of VPTE (Volt/K).
`tvpc=0 V/K`	Rate of change in temperature of VPTC (Volt/K).
`ege=1.55 V`	Effective emitter bandgap parameter.

© 2023 Cadence Design Systems, Inc.

`tnf=0`	Rate of change in temperature of NF.
`xtis=3`	Temperature exponent for IS.
`xtih=4`	Temperature exponent for ISH.
`xtie=3`	Temperature exponent for ISE.
`egc=1.5 V`	Effective collector bandgap parameter.
`tnr=0`	Rate of change in temperature of NR.
`xtir=3`	Temperature exponent for ISR.
`xtic=3`	Temperature exponent for ISC.
`xtirh=4`	Temperature exponent for ISRH.
`xtik3=0`	Temperature exponent for IKDC3.
`xtfb=0`	Temperature exponent for TFB.
`xtcmin=0`	Temperature exponent for TCMIN.
`xtfc0=0`	Temperature exponent for TFC0.
`rth1=1000 W`	Thermal resistance #1 (Kelvin/Watt).
`rth2=0 W`	Thermal resistance #2 (Kelvin/Watt).
`cth1=5e-10 F`	Thermal capacitance #1 (Sec-Amp/Volt).
`cth2=0 F`	Thermal capacitance #2 (Sec-Amp/Volt).
`xth1=0`	Temperature exponent for RTH1.
`xth2=0`	Temperature exponent for RTH2.
`kb=0`	Burst noise coefficient.
`ab=1`	Burst noise exponent.
`fb=1 Hz`	Burst noise corner frequency.
`vtc0inv=0.3 1/V`	Collector transit time: rate of change of TFC0 with Vcb (in inverse voltage) (1/Volt).
`vtr0=2.0`	Collector transit time: transition width in Vcb to VMX0 (models velocity saturation).
`vmx0=2.0`	Collector transit time: maximum Vcb for TFC0 (models velocity saturation).
`vtcmininv=0.5 1/V`	Collector transit time: rate of change of TCMIN with Vbc (in inverse voltage) (1/Volt).

© 2023 Cadence Design Systems, Inc.

`vtrmin=1`	Collector transit time: transition width in Vcb to VMX-MIN (models velocity saturation).
`vmxmin=1`	Collector transit time: maximum Vcb for TCMIN (models velocity saturation).
`vtc2inv=0.1 1/V`	Collector transit time: rate of change of ITC2 with Vcb (in inverse voltage) (1/Volt).
`vtcinv=0.1 1/V`	Collector transit time: rate of change of ITC with Vcb (in inverse voltage) (1/Volt).
`fextc=0.8`	Collector transit time: fraction of the collector transit time charge allocated to the base-collector junction.
`ikrktr=1.0e-6`	Kirk effect: transition width to prevent Ikirk=0 (use sparingly).
`vkrk2inv=0.2 1/V`	Kirk effect: rate of change of TKRK with Vcb (in inverse voltage) (1/Volt).
`gkrk=4`	Kirk effect: exponent of Kirk effect delay.
`vktr=1.0`	Kirk effect: transition width in Vcb to VKMX.
`vkmx=1.0 V`	Kirk effect: maximum Vcb for TKRK.
`fexke=0.2`	Kirk effect: fraction of the Kirk effect charge allocated to the base-collector junction.
`tcmin=5.0e-13`	Collector transit time: high current transit time.
`fextb=0.2`	Base transit time: fraction of base transit time charge allocated to the base-collector junction.
`ccmax=9.0e-14 F`	Base-collector capacitance: maximum value in forward bias.
`vptc=3.0 V`	Base-collector capacitance: punchthrough voltage.
`mjcr=0.03`	Base-collector capacitance: grading factor beyond punchthrough.
`abcx=0.75`	Ratio between extrinsic and total base-collector regions.
`cemax=1.0e-13 F`	Base-emitter capacitance: maximum value in forward bias.
`vpte=1.0 V`	Base-emitter capacitance: punchthrough voltage.

© 2023 Cadence Design Systems, Inc.

`mjer=0.05`	Base-emitter capacitance: grading factor beyond punchthrough.
`abex=0`	Base-emitter capacitance: ratio between extrinsic and total base-emitter regions.
`ikdc1=1.0`	Soft knee effect: Transition width in Ic of q3 function.
`ikdc2inv=0.0`	Soft knee effect: Slope of q3 function (1/Amp).
`ikdc3=1.0 A`	Soft knee effect: Critical current at which soft knee effect occurs at Vcb=VJC.
`vkdcinv=0.1 1/V`	Soft knee effect: Transition width of Vcb (in inverse voltage) (1/Volt).
`nkdc=3.0`	Soft knee effect: maximum value of q3.
`gkdc=0.0`	Soft knee effect: Exponent of q3 factor in base current.
`isr=1e-15 A`	Collector-Emitter current: Reverse emitter saturation current.
`isrl=0 A`	
`ish=1e-27 A`	Base-Emitter current: Ideal base-emitter current.
`nh=1`	Base-Emitter current: Ideal base-emitter current ideality factor.
`isrh=1e-25 A`	Base-Collector current: Ideal base-collector saturation current.
`nrh=2`	Base-Collector current: Ideal base-collector current ideality factor.

© 2023 Cadence Design Systems, Inc.

Output parameters

`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`type=1`	Transistor type. Possible values are `npn` or `pnp`.
`temp (C)`	Average device operating temperature.
`ibe (A)`	Intrinsic B-E current.
`ibc (A)`	Intrinsic B-C current.
`ice (A)`	Intrinsic C-E current.
`ics (A)`	C-S junction current.
`ibei (A)`	B-E junction current.
`ibci (A)`	B-C junction current.
`ibex (A)`	XB-E junction current.
`ibcx (A)`	XB-C junction current.
`qbe (A))`	Intrinsic B-E charge.
`qbc (A)`	Intrinsic B-C charge.
`qbex (A)`	XB-E junction charge.
`qbcx (A`	XB-C junction charge
`vbc (V)`	Base-emitter voltage.
`vbe (V)`	Base-collector voltage.
`vce (V)`	Collector-emitter voltage.
`vcs (V)`	XC-substrate voltage.
`pwr (W)`	Power dissipation.

Related Topics

HBT Model (ucsd_hbt)

VBIC Model (vbic)

JFET Model (jfet)

© 2023 Cadence Design Systems, Inc.

Philips Models

© 2023 Cadence Design Systems, Inc.

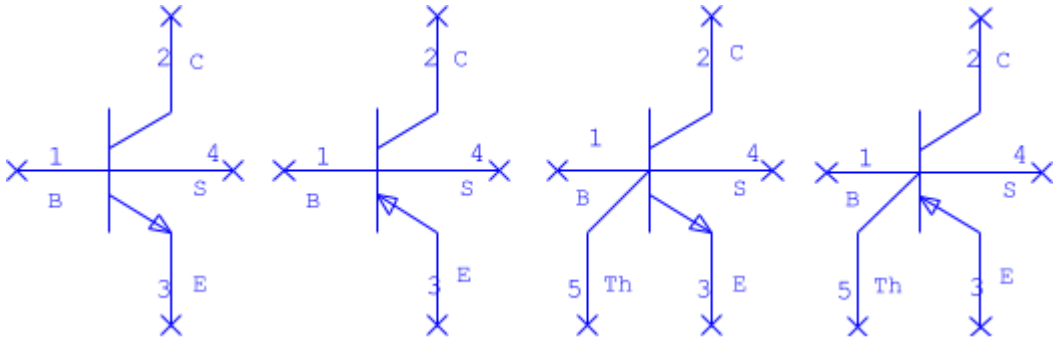
© 2023 Cadence Design Systems, Inc.

10

HBT Model (version 2)

The Cadence HBT (Hetero-junction Bipolar Transistor) element implements the HBT model, developed by University of California San Diego (UCSD) as part of the ARPA High Speed Circuit Design Program. The UCSD HBT model, like the Berkeley BSIM3 model, was conceived as an industry standard SPICE model. This model may be described as a revised version of the standard Gummel-Poon model, where some portions of the model have been enhanced or modified to support features not supported by the original Gummel-Poon model, while the remaining has been kept unchanged. Support for breakdown and self-heating are among the most important new features introduced by this model. The Cadence HBT model is fully compatible with the AWR HBT model.

The following diagram shows the symbol of this model.



Since this model supports both the UCSD original model and AWR extensions, the model has an extensive parameter set. Some parameters are shared by both modes of operation and some are exclusive to a particular one. The AWR extensions are enabled by choosing the appropriate setting of the `ext_flag` parameter. The `selft` parameter controls whether self-heating simulation is supported or not. The self-heating terminal is shown or hidden, accordingly. The extraction and device temperatures are controlled using the `tnom` and `temp` parameters, respectively. The temperature parameter `tbp` (Temperature of the Base Plate) enables partial self-heating simulation. This type of operation is not enabled when the model supports the AWR extensions. The `type` parameter controls whether the device is NPN or PNP.

© 2023 Cadence Design Systems, Inc.

Note: When self-heating effects are not to be considered, set the `selft` parameter to `off`. This removes unused self-heating associated branches from the model, resulting in faster execution time. The `dtmax` parameter limits the value of self-heating induced temperature changes during simulation. You should keep this value as small as possible, provided it does not affect the simulation results.

Component Statements

Sample Instance Statement

```
q7 (net5 net2 0) hbtmod m=1 top=25
```

Sample Model Statement

```
model hbtmod hbt type=npn bf=500 br=1000 xtb=-2.4 xti=0 xcjc=0.83 mje=0.34 fc=0.5
eg=1.2 ise=5.5e-15 vjc=0.84 vaf=40 cjc=5.1e-15
```

Instance Definition

```
Name  c  b  e s ModelName parameter=value ...
```

Instance Parameters

1	`area=1`	Transistor area factor.
2	`m=1`	Multiplicity factor.
3	`temp`	Ambient temperature.
4	`trise=0 C`	Variability in device temperature.
5	`isnoisy=yes`	Should resistor generate noise. Possible values are `no` or `yes`.

Model Definition

```
model modelName hbt parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

1	`nflag=on`	Noise Model.
2	`area=1`	Device area factor (Does not scale parasitic inductors or capacitors).
3	`tnom`	Reference (extraction) temperature.
4	`tbp=298.15`	Base-plate temperature.
5	`selft=off`	Self-Heating flag.
6	`ext_flag=0`	AWR-Extensions flag.
7	`re=0`	Emitter resistance.
8	`rci=0`	Intrinsic collector resistance.
9	`rcx=0`	Extrinsic collector resistance.
10	`rbi=0`	Intrinsic base resistance.
11	`rbx=0`	Extrinsic base resistance.
12	`is=1e-25`	Collector-Emitter current: Forward collector saturation current.
13	`nf=1`	Collector-Emitter current: Forward collector current ideality factor.
14	`isr=1e-15`	Collector-Emitter current: Reverse emitter saturation current.
15	`nr=1`	Collector-Emitter current: Reverse emitter current ideality factor.
16	`ish=1e-27`	Base-Emitter current: Ideal base-emitter current.
17	`nh=1`	Base-Emitter current: Ideal base-emitter current ideality factor.
18	`ise=1e-25`	Base-Emitter current: Non-ideal base-emitter current.
19	`ne=2`	Base-Emitter current: Non-ideal base-emitter current ideality factor.
20	`isrh=1-e25`	Base-Collector current: Ideal base-collector saturation current.
21	`nrh=2`	Base-Collector current: Ideal base-collector current ideality factor.

© 2023 Cadence Design Systems, Inc.

22	`isc=1e-20`	Base-Collector current: Non-ideal base-collector saturation current.
23	`nc=2`	Base-Collector current: Non-ideal base-collector current ideality factor.
24	`abel=0`	Base-Emitter current: Portion of base-emitter current allocated to extrinsic region.
25	`vaf=500`	Forward Early voltage.
26	`var=500`	Reverse Early voltage.
27	`isa=1e10`	Base-emitter heterojunction saturation current (BE barrier effects).
28	`na=2`	Base-emitter heterojunction ideality factor.
29	`isb=1e10`	Base-collector heterojunction current (BC barrier effects).
30	`nb=2`	Base-collector heterojunction ideality factor.
31	`ikdc1=1`	Soft knee effect: Transition width in Ic of q3 function.
32	`ikdc2inv=0`	Soft knee effect: slope of q3 function (1/Amp).
33	`ikdc3=1`	Soft knee effect: Critical current at which soft knee effect occurs at Vcb=VJC.
34	`vkdcinv=0.1`	Soft knee effect: Transition width of Vcb (in inverse voltage) (1/Volt).
35	`nkdc=3`	Soft knee effect: maximum value of q3.
36	`gkdc=0`	Soft knee effect: Exponent of q3 factor in base current.
37	`ik=1e10`	High current roll-off in Beta.
38	`cje=0`	Base-emitter capacitance: zero-bias capacitance.
39	`vje=1.6`	Base-emitter capacitance: built- in voltage.
40	`mje=0.5`	Base-emitter capacitance: grading factor (0.1<MJE).
41	`cemax=1e-13`	Base-emitter capacitance: maximum value in forward bias.
42	`vpte=1`	Base-emitter capacitance: punchthrough voltage.
43	`mjer=0.05`	Base-emitter capacitance: grading factor beyond punchthrough.

© 2023 Cadence Design Systems, Inc.

44	`abex=0`	Base-emitter capacitance: ratio between extrinsic and total base-emitter regions.
45	`cjc=0`	Base-collector capacitance: zero-bias capacitance.
46	`vjc=1.4`	Base-collector capacitance: built-in voltage.
47	`mjc=0.33`	Base-collector capacitance: grading factor (0.1<MJC).
48	`ccmax=9e-14`	Base-collector capacitance: maximum value in forward bias.
49	`vptc=3`	Base-collector capacitance: punchthrough voltage.
50	`mjcr=0.03`	Base-collector capacitance: grading factor beyond punchthrough.
51	`abcx=0.75`	Ratio between extrinsic and total base-collector regions.
52	`tfb=0`	Base transit time: delay through the base.
53	`fextb=0.2`	Base transit time: fraction of base transit time charge allocated to the base-collector junction.
54	`tfc0=0`	Collector transit time: low current transit time.
55	`tcmin=5e-13`	Collector transit time: high current transit time.
56	`itc=0`	Collector transit time: midpoint in collector current between TFC0 and TCMIN.
57	`itc2=0`	Collector transit time: transition width in collector current between TFC0 and TCMIN.
58	`vtc0ivn=0.3`	Collector transit time: rate of change of TFC0 with Vcb (in inverse saturation).
59	`vtr0=2`	Collector transit time: transition width in Vcb to VMX0 (models velocity saturation).
60	`vmx0=2`	Collector transit time: maximum Vcb for TFC0 (models velocity saturation).
61	`vtcmininv=0.5`	Collector transit time: rate of change of TCMIN with Vbc (in inverse voltage) (1/Volt).
62	`vtrmin=1`	Collector transit time: transition width in Vcb to VMXMIN (models velocity saturation).

© 2023 Cadence Design Systems, Inc.

63	`vmxmin=1`	Collector transit time: maximum Vcb for TCMIN (models velocity saturation).
64	`vtcinv=0.1`	Collector transit time: rate of change of ITC with Vcb (in inverse voltage) (1/Volt).
65	`vtc2inv=0.8`	Collector transit time: rate of change of ITC2 with Vcb (in inverse voltage) (1/Volt).
66	`fextc=0.8`	Collector transit time: fraction of the collector transit time charge allocated to the base-collector junction.
67	`tkrk=0`	Kirk effect: Kirk effect delay time.
68	`ikrk=1e3`	Kirk effect: critical current for Kirk effect at Vbc=0.
69	`ikrktr=1e-6`	Kirk effect: transition width to prevent Ikirk=0 (use sparingly).
70	`vkrk=10`	Kirk effect: rate of change of IKRK with Vcb.
71	`vkrk2inv=0.2`	Kirk effect: rate of change of TKRK with Vcb (in inverse voltage) (1/Volt).
72	`gkrk=4`	Kirk effect: exponent of kirk effect delay.
73	`vktr=1`	Kirk effect: transition width in Vcb to VKMX.
74	`vkmx=1`	Kirk effect: Maximum Vcb for TKRK.
75	`fexke=0.2`	Kirk effect: fraction of the Kirk effect charge allocated ti the base-collector junction.
76	`tr=3.5e-10`	Reverse transit time.
77	`cpce=0`	Parasitic/Fringing collector-emitter capacitance.
78	`cpbe=0`	Parasitic/Fringing base-emitter capacitance.
79	`cpbc=0`	Parasitic/Fringing base-collector capacitance.
80	`lpc=0`	Parasitic collector inductance.
81	`lpb=0`	Parasitic base inductance.
82	`lpe=0`	Parasitic emitter inductance.
83	`xrb=0`	Temperature exponent for RBI and RBX.
84	`xrc=0`	Temperature exponent for RCI and RCX.
85	`xre=0`	Temperature exponent for RE.
86	`tvje==0`	Rate of change in temperature of VJE (Volt/K).

© 2023 Cadence Design Systems, Inc.

87	`tvpe=0`	Rate of change in temperature of VPTE (Volt/K).
88	`tvjc=0`	Rate of change in temperature of VJC (Volt/K).
89	`tvpc=0`	Rate of change in temperature of VPTC (Volt/K).
90	`ege=1.55`	Effective emitter bandgap parameter.
91	`tnf=0`	Rate of change in temperature of NF.
92	`xtis=3`	Temperature exponent for IS.
93	`xtih=4`	Temperature exponent for ISH.
94	`xtie=3`	Temperature exponent for ISE.
95	`egc=1.5`	Effective collector bandgap parameter.
96	`tnr=0`	Rate of change in temperature of NR.
97	`xtir=3`	Temperature exponent for ISR.
98	`xtic=3`	Temperature exponent for ISC.
99	`xtirh=4`	Temperature exponent for ISRH.
100	`xtik3=0`	Temperature exponent for IKDC3.
101	`eaa=0`	Temperature dependence of ISA.
102	`eab=0`	Temperature dependence of ISB.
103	`xtfb=0`	Temperature exponent for TFB.
104	`xtcmin=0`	Temperature exponent for TCMIN.
105	`xtfc0=0`	Temperature exponent for TFC0.
106	`xtitc=0`	Temperature exponent for ITC.
107	`xtitc2=0`	Temperature exponent for ITC2.
108	`xttkrk=0`	Temperature exponent for TKRK.
109	`xtikrk=0`	Temperature exponent for IKRK.
110	`xtvkrk=0`	Temperature exponent for VKRK.
111	`rth1=1000`	Thermal resistance #1 (Kelvin/Watt).
112	`cth1=5e-10`	Thermal capacitance #1 (Sec-Amp/Volt).
113	`xth1=0`	Temperature exponent for Rth1.
114	`rth2=0`	Thermal resistance #2 (Kelvin/Watt).
115	`cth2=0`	Thermal capacitance #2 (Sec-Amp/Volt).

© 2023 Cadence Design Systems, Inc.

116	`xth2=0`	Temperature exponent for Rth2.
117	`kf=0`	Flicker noise coefficient.
118	`af=1`	Flicker noise exponent.
119	`ffe=1`	Flicker noise frequency exponent.
120	`kb=0`	Burst noise coefficient.
121	`ab=1`	Burst noise exponent.
122	`fb=1`	Burst noise corner frequency.
123	`imax=10`	Explosion current.
124	`bkdn=0`	Breakdown current flag.
125	`bf=1000`	Forward ideal current gain.
126	`br=1000`	Reverse ideal current gain.
127	`isex=1e-25`	Saturation current for emitter leakage diode.
128	`nex=2`	Ideality factor for emitter leakage diode.
129	`iscx=1e-30`	Saturation current for extrinsic BC junction current.
130	`ncx=2`	Ideality factor for extrinsic BC junction current.
131	`fa=0.9`	Factor to specify avalanche voltage.
132	`bvc=50`	C-B breakdown voltage (BVcb0); positive.
133	`nbc=8`	Exponent for BC multiplication factors versus voltage.
134	`ics=1e-30`	Saturation value for collector-substrate current.
135	`ncs=2`	Ideality factor for collector-substrate current.
136	`rex=1e-3`	Extrinsic emitter leakage diode series resistance.
137	`cemin=1e-40`	Min value for intrinsic BC capacitance.
138	`fce=0.8`	Factor for BE capacitance approximation near Vbi.
139	`ccmin=1e-40`	Min valuer of intrinsic BC capacitance.
140	`fc=0.8`	Factor for BC capacitance approximation near Vbi.
141	`cjcx=0`	Extrinsic BC capacitance at zero voltage.
142	`vjcx=1.4`	Extrinsic BC capacitance Vbi.

© 2023 Cadence Design Systems, Inc.

143	`mjcx=0.33`	Extrinsic base-collector capacitance: grading factor (0.1<MJCX).
144	`cxmin=1e-40`	Minimum extrinsic BC capacitance.
145	`xcjc=0`	Factor for partitioning BC capacitance.
146	`cjs=0`	Substrate depletion capacitance at zero voltage.
147	`vjs=1.4`	Built-in potential for substrate capacitance.
148	`mjs=0.5`	Substrate capacitance: grading factor (0.1<MJS).
149	`tbexs=0`	Excess BE transit time.
150	`tbcxs=0`	Excess BC transit time.
151	`icrit0=1e3`	Critical current for junction capacitance.
152	`vtc=1e3`	Characteristic voltage for TFC.
153	`trx=0`	Reverse storage time for extrinsic BC diode.
154	`fex=0`	Excess phase factor.
155	`rth=1e-8`	Thermal resistance.
156	`cth=1e-6`	Thermal capacitance.
157	`xti=2`	Exponent for IS temperature dependence.
158	`xtb=2`	Exponent for beta temperature dependence.
159	`tne=0`	Coefficient for NE temperature dependence.
160	`tnc=0`	Coefficient for NC temperature dependence.
161	`tnex=0`	Coefficient for NEX temperature dependence.
162	`eg=1.5`	Activation energy for IS temperature dependence.
163	`eae=0`	Activation energy for ISE temperature dependence.
164	`eac=0`	Activation energy for ISC temperature dependence.
165	`eax=0`	Activation energy for ISEX temperature dependence.
166	`xrex=0`	Coefficient for REX temperature dependence.
167	`tvjcx=0`	Coefficient for VJCX temperature dependence.
168	`tvjs=0`	Coefficient for VJS temperature dependence.
169	`xttf=0`	Coefficient for TF temperature dependence.

© 2023 Cadence Design Systems, Inc.

170	`xrt=0`	Coefficient for RTH temperature dependence.
171	`dtmax=500`	Maximum temperature rise above heatsink in Celsius degrees.
172	`compat=0`	Model compatibility selector.

Operating-Point Parameters

1	`pwr (Power)`	Dissipated power.
2	`temp (Temperature)`	Temperature.
3	`Ibe`	Intrinsic B-E current.
4	`Ice`	Intrinsic B-C current.
5	`Ics`	C-S junction current.
6	`Ibei`	B-E junction current.
7	`Ibci`	B-C junction current.
8	`Ibex`	XB-E junction current.
9	`Ibcx`	XB-C junction current.
10	`Qbe`	Intrinsic B-E charge.
11	`Qbc`	Intrinsic B-C charge.
12	`Qbex`	XB-E junction charge.
13	`Qbcx`	XB-C junction charge.
14	`Vbe`	Base-emitter voltage.
15	`Vbc`	Base-collector voltage.
16	`Vce`	Collector-emitter voltage.
17	`Vcs`	XC-substrate voltage.

© 2023 Cadence Design Systems, Inc.

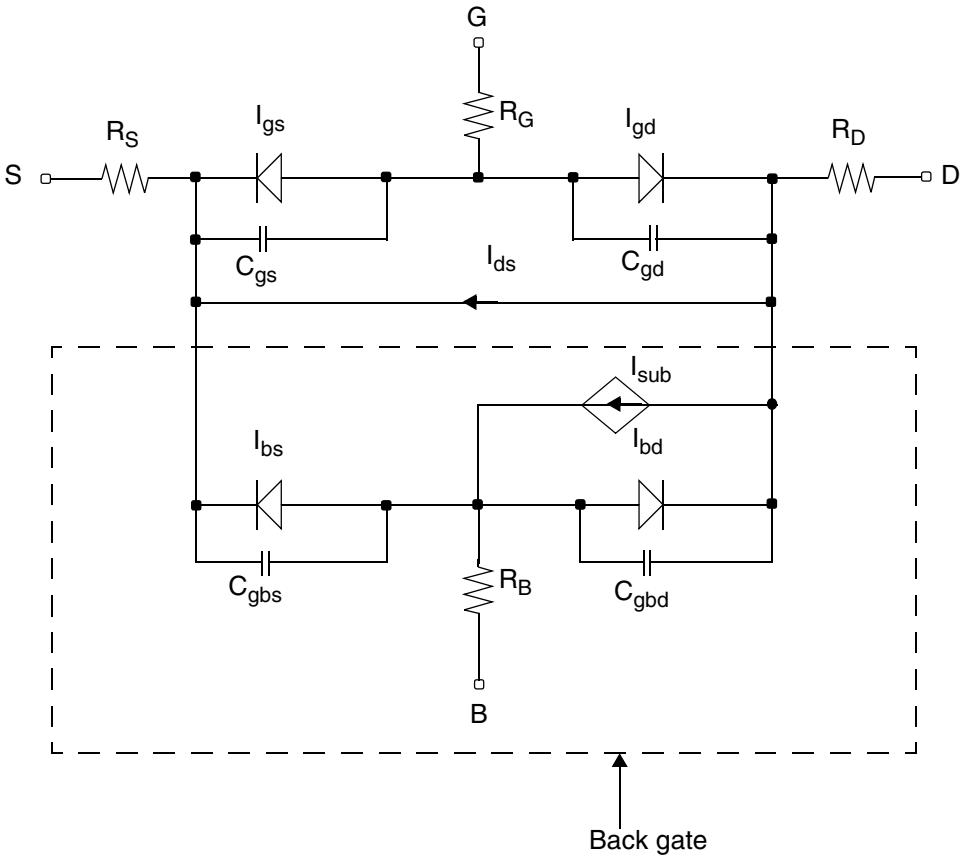
11

JFET Model (jfet)

The JFET model is derived from the FET model of Shichman and Hodges. This topic contains the following information for the JFET model:

- Drain Current for the Subthreshold Region
- Drain Current for the Triode Region
- Drain Current for the Saturation Region
- Gate Junction Currents
- Gate Junction Capacitance
- Temperature Effect
- Noise Model
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.



Note: The back gate (enclosed by dotted lines) is available for $level$ = 3 only.

$$V_{GST} = V_{GS} - V_{TH}$$

where

$$V_{TH} = \begin{cases} vto & \text{if } level = 1 \text{ or } 2 \\ V_{to4} & \text{if } level = 3 \end{cases}$$

$$V_{to4} = vtos(vtop - V_{BS})^{vtoe} + vtoc$$

Drain Current for the Subthreshold Region

Note: These equations apply when $V_{GST} \leq 0$.

© 2023 Cadence Design Systems, Inc.

$$I_{DS} = \begin{cases} 0 & \text{if } level = 1 \\ \dfrac{I_{EXP} I_{LIMIT}}{I_{EXP} + I_{LIMIT}} \left(1 - e^{-V_{DS}/V_t}\right) & \text{otherwise} \end{cases}$$

where

$$I_{LIMIT} = 2betaV_t^2$$

$$I_{EXP} = (io)e^{V_{GST}/nsV_t}$$

Drain Current for the Triode Region

Note: These equations apply when $V_{GST} \geq 0$ and $V_{DS} \leq V_{GST}$.

$$I_{DS} = \begin{cases} beta(2V_{GST} - V_{DS})V_{DS}(1 + \lambda V_{DS}) & level = 1 \\ betaV_{GST}^{np} \tanh\left(\dfrac{alphaV_{DS}}{V_{GST}}\right)(1 + \lambda V_{DS}) & level = 2 \\ \beta_4 V_{GST}^{np} \tanh\left(\dfrac{alphaV_{DS}}{V_{GST}}\right)(1 + \lambda V_{DS}) & level = 3 \end{cases}$$

where

$$\beta_4 = beta\left(\frac{vto + vtop}{V_{to4} + vtop}\right)$$

$$\lambda = lambda(1 + lambda1V_{GST})$$

Drain Current for the Saturation Region

Note: These equations apply when $V_{GST} \geq 0$ and $V_{DS} \geq V_{GST}$.

© 2023 Cadence Design Systems, Inc.

$$I_{DS} = \begin{cases} betaV_{GST}^2(1+\lambda V_{DS}) & level = 1 \\ betaV_{GST}^{np}\tanh\left(\frac{alphaV_{DS}}{V_{GST}}\right)(1+\lambda V_{DS}) & level = 2 \\ \beta_4 V_{GST}^{np}\tanh\left(\frac{alphaV_{DS}}{V_{GST}}\right)(1+\lambda V_{DS}) & level = 3 \end{cases}$$

Substrate Leakage Currents

If `ai` and `bi` are both greater than 0, and V_{DS}>V_{DSAT},

$$I_{sub} = I_{DS} \times (V_{DS} - V_{DSAT}) \times ai \times exp\left[\frac{-bi}{V_{DS} - V_{DSAT}}\right]$$

For information on bulk junction models I_{BS}, I_{BD}, C_{GBS}, and C_{GBD}, see Common MOSFET Equations

Gate Junction Currents

$$I_{GS(GD)} = \begin{cases} is\left(e^{\frac{V_{gs(gd)}}{nV_t}} - 1\right) & \text{if Vgs(gd)} \leq \text{VExpl} \\ I_{offset} + G_{Expl}V_{gs(gd)} & \text{otherwise} \end{cases}$$

where V_t is the thermal voltage given by

$$V_t = \frac{kT}{q},$$

$$V_{Expl} = nV_t\ln\left[1 + \frac{imelt}{is}\right]$$

is the forward explosion voltage,

© 2023 Cadence Design Systems, Inc.

$$G_{Expl} = \frac{(imelt + is)}{nV_t}$$

is the conductance at V_{Expl}, and

$$I_{offset} = imelt - V_{Expl}G_{Expl}$$

is the current linearly extrapolated to V = 0 from V_{Expl}.

Gate Junction Capacitance

$$C_{GS(GD)}(V_{GS(GD)}) = \begin{cases} \dfrac{cgs(cgd)}{\left[1 - \dfrac{V_{gsgd}}{pb}\right]^{mj}} & \text{if } V_{GS(GD)} \le fc*\text{pb} \\ \dfrac{cgs(cgd)}{(1-fc)^{mj}}\left[1 + \dfrac{mj(V_{gs(gd)} - pb*fc)}{pb(1-fc)}\right] & \text{otherwise} \end{cases}$$

Temperature Effect

Gate-Source and Gate-Drain Capacitance

$$C_{gs} = cgs_{nom}\left\{1 + mj\left[0.0004(T - Tnom) + \frac{(pb_{nom} - pb)}{pb_{nom}}\right]\right\}$$

$$C_{gd} = cgd_{nom}\left\{1 + mj\left[0.0004(T - Tnom) + \frac{(pb_{nom} - pb)}{pb_{nom}}\right]\right\}$$

Junction Potential

$$pb = pb_{nom}\left(\frac{T}{Tnom}\right) - 3V_t\ln\left[\frac{T}{Tnom}\right] - E_{g,nom}\left(\frac{T}{Tnom}\right) + E_g$$

© 2023 Cadence Design Systems, Inc.

Transconductance Temperature

$$Beta = Beta \times \left(\frac{T}{Tnom + bto}\right)^{bte}$$

$$Lambda = Lambda \times \left(\frac{T}{Tnom + lto}\right)^{lte}$$

$$Lambda1 = Lambda1 \times \left(\frac{T}{Tnom + lto}\right)^{lte}$$

Gate Junction Current

$$is = is_{nom}\left(\frac{T}{Tnom}\right)^{xti} \exp\left[\frac{E_{g,\,nom}}{V_{t,\,nom}} - \frac{E_g}{V_t}\right]$$

where, if SPICE-compatibility is required (set by the options),

$$E_g = 1.16 - \frac{7.02 \times 10^{-4} T^2}{1108 + T}$$

$$E_{g,\,nom} = 1.16 - \frac{7.02 \times 10^{-4} Tnom^2}{1108 + Tnom}$$

otherwise,

$$E_g = 1.17 - \frac{4.73 \times 10^{-4} T^2}{636 + T}$$

$$E_{g,\,nom} = 1.17 - \frac{4.73 \times 10^{-4} Tnom^2}{636 + Tnom}$$

For equations on parameters `tlev`, `tlevc`, `gap1`, and `gap2`, see Common MOSFET Equations

© 2023 Cadence Design Systems, Inc.

Threshold Voltage

For `tcv`,

$$V_{TO} = V_{TO}(model) - tcv \times deltaT$$

$$V_{TOC} = V_{TOC}(model) - tcv \times deltaT$$

Parasitic Resistors

$$tempfactor = 1.0 + deltaT \times (tc1 + deltaT \times tc2)$$

$$R_{geff} = tempfactor \times R_g$$

$$R_{deff} = tempfactor \times R_d$$

$$R_{seff} = tempfactor \times R_s$$

$$R_{beff} = tempfactor \times R_b$$

Noise Model

Source Series Resistance Thermal Noise

$$\overline{i_{Rs}^2} = \frac{4kT}{rs}\Delta f$$

Drain Series Resistance Thermal Noise

$$\overline{i_{RD}^2} = \frac{4kT}{rd}\Delta f$$

© 2023 Cadence Design Systems, Inc.

Channel Thermal and Flicker Noise

$$\overline{i_{DS}^2} = \frac{8kT(g_m + g_{ds})}{3}\left(\frac{3}{2} - \frac{V'_{DS}}{2V_{DSAT}}\right) + kf\frac{(I_{DS})^{af}}{f}\Delta f$$

where

$$V'_{DS} = MIN(V_{DS}, V_{DSAT})$$

g_m is the transconductance, g_{ds} is the channel conductance, kf and af are constants for a given device. The Spectre® circuit simulator defaults for kf and af are 0.0 and 1.0, respectively.

Gate Junction Noise

$$\overline{i_{gs}^2} = 2qI_{GS}\Delta f + kfd\frac{I_{GS}^{afg}}{f}\Delta f$$

$$\overline{i_{gd}^2} = 2qI_{GD}\Delta f + kfd\frac{I_{GD}^{afg}}{f}\Delta f$$

Scaling Effects

The following are the Spectre scaling effects:

- is, cgs, cgd, and $beta$ are multiplied by $area$.
- rs and rd are divided by $area$.
- All noises are multiplied by $area$.

Component Statements

Sample Instance Statement:

```
jf1 (net1 net2 0) jmod area=1
```


© 2023 Cadence Design Systems, Inc.

Sample Model Statement

```
model jmod jfet beta=9e-5 lambda=0 type=n vt0=-18.7 rd=10 rs=10 cgs=1.3e-13 pb=0.65
```

Instance Syntax

```
Name  d  g  s  [b] ModelName parameter=value ...
```

You do not have to specify the back gate terminal when you use the four-terminal model. If left unspecified, the substrate is connected to ground.

Instance Parameters

`area=1`	Junction area factor.
`m=1`	Multiplicity factor.
`region=triode`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, or `breakdown`.
`isnoisy=yes`	Should resistor generate noise. Possible values are `no` or `yes`.
`trise=0`	Temperature rise from ambient.
`dtemp=0`	Alias of trise.

Model Syntax

```
model modelName jfet parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

Drain current model parameters

`level=1`	Drain current model level selector.
`vto=-2 V`	Pinchoff voltage.
`beta=0.0001 A/V`^{2}	Transconductance parameter.
`lambda=0 1/V`	Channel length modulation parameter.
`lambda1=0 1/V`	Gate dependence of channel length modulation parameter.
`np=2`	Power-law exponent.
`alpha=2`	Triode-to-saturation transition parameter.
`io=0 A`	Subthreshold current parameter.
`ns=1`	Subthreshold swing parameter.
`ai=0 1/V`	Impact ionization current coefficient.
`bi=0 V`	Impact ionization current exponent.

Four terminal threshold voltage parameters

`vtop=0.6 V`	Back gate to channel junction potential.
`vtos=1.2 V`	Threshold voltage slope.
`vtoe=0.33`	Threshold voltage exponent.
`vtoc=-3.3 V`	Threshold voltage constant.

Parasitic resistance parameters

`rd=0 Ω`	Drain resistance (/area).
`rs=0 Ω`	Source resistance (/area).

© 2023 Cadence Design Systems, Inc.

`rg=0` Ω	Gate resistance (/area).
`rb=0` Ω	Back gate resistance (/area).
`minr=0.1` Ω	Minimum source/drain/gate resistance.

© 2023 Cadence Design Systems, Inc.

Junction diode model parameters

`is=1e-14 A`	Gate saturation current (*area).
`n=1`	Emission coefficient for G-D and G-S junctions.
`imelt=`imax' A`	Explosion current (*area).
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`. Possible values are `no` or `yes`.

Junction capacitance model parameters

`tt=0 s`	Transit time.
`cgs=0 F`	Gate-source zero-bias junction capacitance (*area).
`cgd=0 F`	Gate-drain zero-bias junction capacitance (*area).
`mj=1/2`	Junction grading coefficient.
`pb=1 V`	Gate-junction potential.
`fc=0.5`	Junction capacitor forward-bias threshold.

Four terminal junction parameters

`isb=1e-14 A`	Back gate-saturation current (*area).
`nb=1`	Emission coefficient for back gate-junctions.
`cgbs=0 F`	Back gate-source zero-bias junction capacitance (*area).
`cgbd=0 F`	Back gate-drain zero-bias junction capacitance (*area).
`mjb=1/2`	Back gate-junction grading coefficient.
`pbb=1 V`	Back gate-junction potential.

Temperature effect parameters

`tnom (C)`	Parameters measurement temperature. Default set by `options`.
`trise=0 C`	Temperature rise from ambient.
`xti=3`	Temperature exponent for effect on `is`.

© 2023 Cadence Design Systems, Inc.

`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eg=1.12452 V`	Energy band gap.
`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.
`eglev=0`	DC temperature selector.
`tcv=0 1/C`	Threshold voltage temperature coefficient.
`bto=0 C`	Transconductance parameter temperature offset.
`bte=0`	Transconductance parameter temperature exponent.
`lto=0 C`	Channel length modulation parameters temperature offset.
`lte=0`	Channel length modulation parameters temperature exponent.
`tc1=0 1/C`	Linear temperature coefficient for parasitic resistors.
`tc2=0` C^{-2}	Quadratic temperature coefficient for parasitic resistors.
`pta=0 V/C`	Junction potential temperature coefficient.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, or `rev`.
`imax=1 A`	Maximum allowable current (*area).
`bvj=∞ V`	Junction reverse breakdown voltage.

© 2023 Cadence Design Systems, Inc.

Noise parameters

`kf=0`	Flicker noise (1/f) coefficient.
`af=1`	Flicker noise (1/f) exponent.
`kfd=0`	Flicker noise (1/f) coefficient for gate diodes.
`afg=1`	Flicker noise (1/f) exponent for gate diodes.

Compatibility model parameters

`ldel=0 m`	Difference between drawn and actual or optical device length.
`wdel=0 m`	Difference between drawn and actual or optical device Width.
`rsh=0 Ω`	heavily doped region, sheet resistance (ohm/sq).
`rshg=0 Ω`	Gate sheet resistance (ohm/sq).
`rshl=0 Ω`	lightly doped region, sheet resistance (ohm/sq).
`hdif=0 m`	distance of the heavily diffused or low resistance region from source or drain contact to lightly doped region.
`ldif=0 m`	distance of the lightly doped region from heavily doped region to transistor edge.
`trd=0 1/C`	temperature coefficient for drain resistance.
`trs=0 1/C`	temperature coefficient for source resistance.
`acm=0`	area calculation method. acm=0 area=w/l, acm=1 area=w.l.

Imax and Imelt

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and Spectre prints a warning.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, the base and collector currents are composed of many

© 2023 Cadence Design Systems, Inc.

exponential terms, Spectre issues a warning and the results become inaccurate. The junction current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

The `bv` parameter is used to detect the junction breakdown only. The breakdown currents of the junctions are not modeled.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.
`region=triode`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, or `breakdown`.
`ids (A)`	Resistive drain current.
`id (A)`	Id drain current.
`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`vth (V)`	Threshold at op point.
`vdsat (V)`	Drain saturation voltage.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`ig (A)`	Resistive gate current.
`pwr (W)`	Power at op point.
`qd (V)`	Threshold at op point.
`qg (V)`	Threshold at op point.
`qs (V)`	Threshold at op point.
`qb (V)`	Threshold at op point.

© 2023 Cadence Design Systems, Inc.

Related Topics

HBT Model (ucsd_hbt)

VBIC Model (vbic)

Philips Models

© 2023 Cadence Design Systems, Inc.

12

Philips Models

This topic lists the component statements for the following models:

- Diode Level 500 (dio500)
- Lateral PNP Transistor (bjt301)
- Lateral PNP Transistor (bjt500)
- Lateral PNP Transistor (bjt500t)
- Vertical NPN/PNP Transistor (bjt503)
- Compact Bipolar-Transistor Model (bjt504)
- Compact Bipolar-Transistor Model (bjt504t)
- Compact Bipolar-Transistor Model (bjtd504)
- Compact Bipolar-Transistor Model (bjtd504t)
- Compact Bipolar-Transistor Model (bjt505)
- Compact Bipolar-Transistor Model (bjt505t)
- Compact Bipolar-Transistor Model (bjtd505)
- Compact Bipolar-Transistor Model (bjtd505t)
- Compact Bipolar-Transistor Model (bjtd3500)
- Compact Bipolar-Transistor Model (bjtd3500t)
- JFETIDG Model (jfetidg)
- Long Channel JFET/MOSFET Model (mos30)
- MOS Model 40, Level 40 (mos40t)
- Long Channel JFET/MOSFET Model (mos3002)
- Compact MOS-Transistor Model (mos705)

© 2023 Cadence Design Systems, Inc.

- Compact MOS-Transistor Model (mos902)
- Compact MOS-Transistor Model (mos903)
- Compact MOS-Transistor Distortion Model (mos1100)
- Compact MOS-Transistor Distortion Model (mos1100e)
- MOS Model 11, Level 1101 (mos11010)
- MOS Model 11, Level 1101 (mos11010t)
- MOS Model 11, Level 1101 (mos11011)
- MOS Model 11, Level 1101 (mos11011t)
- MOS Model 11, Level 1101 (mos1101e)
- MOS Model 11, Level 1101 (mos1101et)
- MOS Model 11, Level 1102 (mos11020)
- MOS Model 11, Level 1102 (mos11020t)
- MOS Model 11, Level 1102 (mos11021)
- MOS Model 11, Level 1102 (mos11021t)
- MOS Model 11, Level 1102 (mos1102e)
- MOS Model 11, Level 1102 (mos1102et)
- Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)
- Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)
- Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)
- Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)
- Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)
- Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)
- Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)
- Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)
- MOS Model 31, Level 3100 (mos3100)
- MOS Model 31, Level 3100 (mos3100t)

© 2023 Cadence Design Systems, Inc.

Diode Level 500 (dio500)

The `dio500` model provides a detailed description of the diode currents in forward and reverse biased Si-diodes. It is described in the Philips Bipolar Modelbook (Dec.93) as `Diode level 500`. Information on how to obtain this document can be found on Source Link by searching for Philips.

(c) Philips Electronics N.V. 1994

In extension to the model book description a minimum conductance `gmin` is inserted between the diode nodes to aid convergence. The value of `gmin` is set by an options statement, default is gmin = 1.0e-12 S.

The `imax` parameter is used to aid convergence and to prevent numerical overflow. The junction characteristics of the diode are accurately modeled for currents up to `imax`. For currents above `imax`, the junction is modeled as a linear resistor, and a warning is printed.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

Sample Instance Statement

```
d1 (pnode 0) phdiode area=2
```

Sample Model Statement

```
model phdiode dio500 is=3.5e-12 rs=26.3 n=2.7 imax=1e20 vlc=1.8 vbr=9.63 cj=2.65e-11 dta=12.88 tau=7.5e-10 tnom=25
```

Instance Syntax

```
Name  a  k ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

area=1.0	Multiplication factor.
mult	Alias of area factor.
m=1.0	Multiplicity factor.
region=fwd	Estimated DC operating region, which is used as a convergence aid. Possible values are fwd, rev or brk.
trise= (K)	Temperature rise from ambient

Model Syntax

```
model modelName dio500 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`is=7.13e-13 A`	Saturation current.
`n=1.044`	Junction emission coefficient.
`vlc=0.0 V`	Voltage dependence at low forward currents.
`vbr=7.459 V`	Breakdown voltage.
`emvbr=1.36e+06 V/cm`	Electric field at breakdown.
`csrh=7.44e-07 A/cm`	Shockley-Read-Hall generation.
`cbbt=3.255 A/V`	Band to band tunneling.
`ctat=3.31e-06 A/cm`	Trap assisted tunneling.
`rs=0.0 Ω`	Series resistance.
`tau=500.0e-12 s`	Transit time.
`cj=7.0e-12 F`	Zero-bias depletion capacitance.
`vd=0.9 V`	Diffusion voltage.
`p=0.4`	Grading coefficient.
`tref (C)`	Reference temperature. Default set by option `tnom`.
`tnom (C)`	Alias of `tref`.
`tr (C)`	Alias of `tref`.
`vg=1.206 V`	Bandgap voltage.
`ptrs=0.0`	Power for temperature dependence of `rs`.
`kf=0.0`	Flickernoise coefficient.
`af=1.0`	Flickernoise exponent.
`dta=0.0 K`	Difference between device temperature and ambient temperature.
`trise (K)`	Alias of `dta`.
`imax=1.0 A`	Explosion current.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`vak (V)`	Diode voltage, measured from anode to cathode (including `rs`).
`id (A)`	Total resistive diode current.
`qd (Coul)`	Diffusion charge.
`qt (Coul)`	Depletion charge.
`rst (Ω)`	Series resistance (temperature updated).
`rl (Ω)`	AC linearized resistance.
`cl (F)`	AC linearized capacitance.
`ctotal (F)`	AC linearized capacitance.
`lx5 (F)`	AC linearized capacitance.
`pwr (W)`	Power dissipation.

Related Topics

Philips Models

Lateral PNP Transistor (bjt301)

Lateral PNP Transistor (bjt500)

Lateral PNP Transistor (bjt500t)

Lateral PNP Transistor (bjt301)

The bjt301 model provides an extensive description of a lateral integrated circuit junction-isolated PNP transistor. It is described in the Philips Bipolar Modelbook (Dec.93) as TPL level 301.

(c) Philips Electronics N.V. 1993

In extension to the model book description a minimum conductance `gmin` is inserted between the internal base and internal collector node, between the internal base and the internal emitter node, and between the external base and the substrate node to aid convergence. The value of `gmin` is set by an options statement, default = 1e-12 S.

© 2023 Cadence Design Systems, Inc.

The imax parameter is used to aid convergence and to prevent numerical overflow. The junction characteristics of the transistor are accurately modeled for currents up to imax. For currents above imax, the junction is modeled as a linear resistor and a warning is printed.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Sample Instance Statement:

```
q2 (minus net3 vcc) pnp_mod region=fwd area=1 m=1
```

Sample Model Statement:

```
model pnp_mod bjt301 type=pnp struct=lateral is=1e-14 bf=85 ilf=11e-9 ikf=95e-6
re=3.2 cje=0.352e-12
```

Instance Syntax

```
Name  c  b  e  [s] ModelName parameter=value ...
```

Instance Parameters

area=1	Area factor.
mult=1	Alias of area factor.
m=1	Multiplicity factor.
region=fwd	Estimated DC operating region; used as a convergence aid. Possible values are off, fwd, rev, and sat.
trise=0.0 K	Temperature rise from ambient.

Model Syntax

```
model modelName bjt301 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Structural parameters

`type=pnp`	Transistor type. Possible values are `pnp` or `pnpl`.
`struct=lateral`	Transistor structure. Possible values are `lateral`.

Current parameters

`is=1.0e-15 A`	Saturation current.
`imax=1.0 A`	Explosion current.
`bf=100.0 A/A`	Ideal forward common-emitter current gain (beta).
`ilf=10.0e-9 A`	Low-level knee-current of forward beta.
`nlf=2.0`	Emission coefficient of non-ideal forward base current.
`ikf=100.0e-6 A`	High-injection knee-current of forward beta.
`nhf=1.0`	Base widening exponent.
`veaf=50.0 V`	Early voltage related to collector junction.
`br=10.0 A/A`	Ideal reverse common-collector current gain (beta).
`ilr=10.0e-9 A`	Low-level knee-current of reverse beta.
`nlr=2.0`	Emission coefficient of non-ideal reverse base current.
`ikr=100.0e-6 A`	High-injection knee-current of reverse beta.
`iks=100.0e-6 A`	High-injection current of substrate effect.
`xcs=1.0`	Current fraction of c-b-s transistor.
`xes=0.01`	Current fraction of e-b-s transistor.

Parasitic resistance parameters

`rc=1.0 Ω`	Collector resistance.
`rbc=10.0 Ω`	Constant part of base resistance.
`rbv=10.0 Ω`	Variable part of base resistance.
`re=1.0 Ω`	Emitter series resistance.

© 2023 Cadence Design Systems, Inc.

Junction capacitance parameters

`taub=25.0e-9 s`	Forward transit time related to neutral base.
`taune=1.0e-9 s`	Forward transit time related to neutral emitter in neutral e-b region.
`mtau=1.0`	Coefficient of current dependence of taune.
`cje=100.0e-15 F`	Zero bias emitter-base depletion capacitance.
`vde=0.55 V`	Emitter-base diffusion voltage.
`pe=0.333`	Emitter-base grading coefficient.
`taur=100.0e-9 s`	Ideal reverse transit time.
`cjc=200.0e-15 F`	Zero bias collector-base depletion capacitance.
`vdc=0.55 V`	Collector-base diffusion voltage.
`pc=0.333`	Collector-base grading coefficient.
`cjs=1.0e-12 F`	Zero bias substrate junction depletion capacitance.
`vds=0.55 V`	Substrate junction diffusion voltage.
`ps=0.333`	Substrate junction grading coefficient.
`exphi=0.3`	Excess phase shift.
`fc=0.95`	Coefficient for forward bias capacitance.

Temperature effects parameters

`tref (C)`	Reference temperature. Default set by option `tnom`.
`tnom (C)`	Alias of tref. Default set by option `tnom`.
`dta=0.0 K`	Difference between device temperature and ambient temperature.
`trise=0.0 K`	Alias of dta.
`ptbf=0.0`	Power for temperature dependence of `bf`.
`ptbr=0.0`	Power for temperature dependence of `br`.
`ptrc=0.0`	Power for temperature dependence of `rc`.
`ptrb=0.0`	Power for temperature dependence of `rbc` and `rbv`.
`vg=1.2 V`	Band-gap voltage.

© 2023 Cadence Design Systems, Inc.

`pt=1.2`	Power for temperature dependence of diffusion coefficient.

© 2023 Cadence Design Systems, Inc.

Noise model parameters

`kf=0.0`	Flickernoise coefficient.
`af=1.0`	Flickernoise exponent.

Operating-Point Parameters

`ib (A)`	Base current.
`ic (A)`	Collector current.
`ie (A)`	Emitter current.
`isub (A)`	Substrate current.
`vbe (V)`	Base-emitter voltage.
`vbc (V)`	Base-collector voltage.
`vce (V)`	Collector-emitter voltage.
`vsubj (V)`	Substrate voltage.
`betadc (A/A)`	Ratio of DC collector current to DC Base current.
`rb (Ω)`	Base resistance at operating point.
`rc (Ω)`	Collector resistance at operating point.
`re (Ω)`	Emitter resistance at operating point.
`icb (A)`	Collector-Base current.
`ieb (A)`	Emitter-Base current.
`icsub (A)`	Collector-Substrate current.
`iesub (A)`	Emitter-Substrate current.
`pwr (W)`	Power.
`gpi (S)`	Conductance emitter-base junction.
`gmu (S)`	Conductance collector-base junction.
`gf (S)`	Forward transconductance.
`gr (S)`	Reverse transconductance.
`gs (S)`	Conductance substrate-base junction.
`g3 (S)`	Transconductance (parasitic PNP) c-b-s transistor.

© 2023 Cadence Design Systems, Inc.

`g4 (S)`	Transconductance (parasitic PNP) e-b-s transistor.
`ced (F)`	Emitter diffusion capacitance.
`ccd (F)`	Collector diffusion capacitance.
`cet (F)`	Emitter junction depletion capacitance.
`cct (F)`	Collector junction depletion capacitance.
`cst (F)`	Substrate junction depletion capacitance.
`betaac (A/A)`	Small-signal common-emitter current gain.
`ft (Hz)`	Unity small-signal current-gain frequency.

Related Topics

Philips Models

Lateral PNP Transistor (bjt500)

Lateral PNP Transistor (bjt500t)

Lateral PNP Transistor (bjt500)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Instance Syntax

```
Name  c  b  e  s ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Area factor.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjt500 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=500`	Bipolar Level.
`paramchk=0`	Level of clip warning info.
`is=1.8e-16 A`	Collector-emitter saturation current.
`bf=131 A`	Ideal forward common-emitter current gain.
`ibf=2.6e-14 A`	Saturation current of non-ideal forward base current.
`vlf=0.54 V`	Cross-over voltage of non-ideal forward base current.
`ik=0.00011 A`	High injection knee current.
`xifv=0.43`	Vertical fraction of forward current.
`eaf1=20.5 V`	Early voltage of the lateral forward current component.
`eafv=75 V`	Early voltage of the vertical forward current component.
`br=25 A`	Ideal reverse common-emitter current gain.
`ibr=1.2e-13 A`	Saturation current of non-ideal reverse base current.
`vlr=0.48 V`	Cross-over voltage of non-ideal reverse base current.
`xirv=0.43`	Vertical fraction of reverse current.
`earl=13.1 V`	Early voltage of the lateral reverse current component.
`earv=104 V`	Early voltage of the vertical reverse current component.
`xes=0.0027`	Ratio between saturation current of e-b-s transistor and e-b-c transistor.
`xhes=0.7`	Fraction of substrate current of e-b-s transistor subject to high injection.
`xcs=3`	Ratio between saturation current of c-b-s transistor and c-b-e transistor.
`xhcs=1`	Fraction of substrate current of c-b-s transistor subject to high injection.
`iss=4e-13 A`	Saturation current of substrate-base diode.
`rcex=5 Ω`	External part of the collector resistance.
`rcin=47 Ω`	Internal part of the collector resistance.
`rbcc=10 Ω`	Constant part of the base resistance `rbc`.

© 2023 Cadence Design Systems, Inc.

`rbcv=10 Ω`	Variable part of the base resistance `rbc`.
`rbec=10 Ω`	Constant part of the base resistance `rbe`.
`rbev=50 Ω`	Variable part of the base resistance `rbe`.
`reex=27 Ω`	External part of the emitter resistance.
`rein=66 Ω`	Internal part of the emitter resistance.
`rsb=1e+15 Ω`	Substrate-base leakage resistance.
`tlat=2.4e-09 s`	Low injection (forward and reverse) transit time of charge stored in the epilayer between emitter and collector.
`tfvr=3e-08 s`	Low injection forward transit time due to charge stored in the epilayer under the emitter.
`tfn=2e-10 s`	Low injection forward transit time due to charge stored in the emitter and the buried layer under the emitter.
`cje=6.1e-14 F`	Zero-bias emitter-base depletion capacitance.
`vde=0.52 V`	Emitter-base diffusion voltage.
`pe=0.3`	Emitter-base grading coefficient.
`trvr=1e-09 s`	Low injection reverse transit time due to charge stored in the epilayer under the collector.
`trn=3e-09 s`	Low injection reverse transit time due to charge stored in the collector and the buried layer under the collector.
`cjc=3.9e-13 F`	Zero-bias collector-base depletion capacitance.
`vdc=0.57 V`	Collector-base diffusion voltage.
`pc=0.36`	Collector-base grading coefficient.
`cjs=1.3e-12 F`	Zero-bias substrate-base depletion capacitance.
`vds=0.52 V`	Substrate-base diffusion voltage.
`ps=0.35`	Substrate-base grading coefficient.
`tref=25 C`	Reference temperature. Default set by option `tnom`.
`dta=0 K`	Difference between the device temperature and the ambient analysis temperature.
`vgeb=1.21 V`	Bandgap voltage of the emitter-base depletion region.

© 2023 Cadence Design Systems, Inc.

`vgcb=1.21 V`	Bandgap voltage of the collector-base depletion region.
`vgsb=1.21 V`	Bandgap voltage of the substrate-base depletion region.
`vgb=1.21 V`	Bandgap voltage of the base between emitter and collector.
`vge=1.21 V`	Bandgap voltage of the emitter.
`vgje=1.12 V`	Bandgap voltage recombination emitter-base junction.
`ae=4.48`	Temperature coefficient of `bf`.
`spb=2.85`	SC.
`snb=2.6`	Temperature coefficient of the epitaxial base electron mobility.
`snbn=0.3`	Temperature coefficient of buried layer electron mobility.
`spe=0.73`	Temperature coefficient of emitter hole mobility.
`spc=0.73`	Temperature coefficient of collector hole mobility.
`sx=1`	Temperature coefficient of combined minority carrier mobility in emitter and buried layer.
`kf=0`	Flickernoise coefficient.
`af=1`	Flickernoise exponent.
`exphi=0`	Not used in model bjt500.
`type=npn`	Transistor gender. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`imax=1000 A`	Explosion current.
`tnom (C)`	alias of tnom.
`tr (C)`	alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

tempeff (C)	Effective temperature for a single device.
meff	Effective multiplicity factor (m-factor).

Operating-Point Parameters

ic (A)	External DC collector current.
ib (A)	External DC base current.
ie (A)	Resistive emitter current.
isub (A)	Resistive substrate current.
iflat (A)	Lateral forward current.
irlat (A)	Lateral reverse current.
ifver (A)	Vertical forward current.
irver (A)	Vertical reverse current.
ire (A)	ideal forward base current.
ile (A)	Non-ideal forward base current.
ise (A)	Forward substrate current.
irc (A)	Ideal reverse base current.
ilc (A)	Non-ideal reverse base current.
isc (A)	Reverse substrate current.
isf (A)	Reverse leakage current of the substrate-base junction.
ip (A)	Main current.
betadc	External DC current gain Ic/Ib.
vbc (V)	Base-collector voltage.
vbe (V)	Base-emitter voltage.
vce (V)	Collector-emitter voltage.
vsb (V)	Substrate-base voltage.
rcex (Ω)	External part of the collector resistance.
rcin (Ω)	Internal part of the collector resistance.

© 2023 Cadence Design Systems, Inc.

`reex (Ω)`	External part of the emitter resistance.
`rein (Ω)`	Internal part of the emitter resistance.
`rbc (Ω)`	Base resistance under the collector.
`rbe (Ω)`	Base resistance under the emitter.
`rsb (Ω)`	Ohmic leakage across the substrate-base junction.
`pwr (W)`	Power.
`gfl (S)`	Forward conductance, lateral path.
`grl (S)`	Reverse conductance, lateral path.
`g11 (S)`	Forward conductance, vertical path.
`g12 (S)`	Collector Early-effect on Ifver.
`g21 (S)`	Emitter Early-effect on Irver.
`g22 (S)`	Reverse conductance, vertical path.
`gpiv (S)`	Conductance emitter-base junction.
`gmuv (S)`	Conductance collector-base junction.
`gbe (S)`	Emitter-side: base conductance B1-B.
`gibe (S)`	Emitter Early-effect on Ib1b.
`gbc (S)`	Collector-side: base conductance B2-B.
`gibc (S)`	Collector Early-effect on Ib2b.
`gise (S)`	Transconductance (parasitic PNP) e-b-s transistor.
`gisc (S)`	Transconductance (parasitic PNP) c-b-s transistor.
`gsb (S)`	Conductance substrate-base junction.
`cpil (F)`	Forward diffusion capacitance, lateral path.
`cipil (F)`	Collector Early-effect on Qflat.
`cpiv (F)`	Forward total capacitance, vertical path.
`cmul (F)`	Reverse diffusion capacitance, lateral path.
`cimul (F)`	Emitter Early-effect on Qrlat.
`cmuv (F)`	Reverse total capacitance, vertical path.
`csb (F)`	Total capacitance substrate-base junction.
`irbe (A)`	Ideal total forward base current.

© 2023 Cadence Design Systems, Inc.

`irbc (A)`	Ideal total reverse base current.
`irsb (A)`	Substrate base leakage resistance current.
`jtype`	type: +1=npn and -1=pnp.

Related Topics

Philips Models

Lateral PNP Transistor (bjt301)

Lateral PNP Transistor (bjt500t)

Lateral PNP Transistor (bjt500t)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Instance Syntax

```
Name  c  b  e  s  dt ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Area factor.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjt500t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=500`	Bipolar Level.
`paramchk=0`	Level of clip warning info.
`is=1.8e-16 A`	Collector-emitter saturation current.
`bf=131 A`	Ideal forward common-emitter current gain.
`ibf=2.6e-14 A`	Saturation current of non-ideal forward base current.
`vlf=0.54 V`	Cross-over voltage of non-ideal forward base current.
`ik=0.00011 A`	High injection knee current.
`xifv=0.43`	Vertical fraction of forward current.
`eaf1=20.5 V`	Early voltage of the lateral forward current component.
`eafv=75 V`	Early voltage of the vertical forward current component.
`br=25 A`	Ideal reverse common-emitter current gain.
`ibr=1.2e-13 A`	Saturation current of non-ideal reverse base current.
`vlr=0.48 V`	Cross-over voltage of non-ideal reverse base current.
`xirv=0.43`	Vertical fraction of reverse current.
`earl=13.1 V`	Early voltage of the lateral reverse current component.
`earv=104 V`	Early voltage of the vertical reverse current component.
`xes=0.0027`	Ratio between saturation current of e-b-s transistor and e-b-c transistor.
`xhes=0.7`	Fraction of substrate current of e-b-s transistor subject to high injection.
`xcs=3`	Ratio between saturation current of c-b-s transistor and c-b-e transistor.
`xhcs=1`	Fraction of substrate current of c-b-s transistor subject to high injection.
`iss=4e-13 A`	Saturation current of substrate-base diode.
`rcex=5 Ω`	External part of the collector resistance.
`rcin=47 Ω`	Internal part of the collector resistance.
`rbcc=10 Ω`	Constant part of the base resistance `rbc`.

© 2023 Cadence Design Systems, Inc.

`rbcv=10 Ω`	Variable part of the base resistance `rbc`.
`rbec=10 Ω`	Constant part of the base resistance `rbe`.
`rbev=50 Ω`	Variable part of the base resistance `rbe`.
`reex=27 Ω`	External part of the emitter resistance.
`rein=66 Ω`	Internal part of the emitter resistance.
`rsb=1e+15 Ω`	Substrate-base leakage resistance.
`tlat=2.4e-09 s`	Low injection (forward and reverse) transit time of charge stored in the epilayer between emitter and collector.
`tfvr=3e-08 s`	Low injection forward transit time due to charge stored in the epilayer under the emitter.
`tfn=2e-10 s`	Low injection forward transit time due to charge stored in the emitter and the buried layer under the emitter.
`cje=6.1e-14 F`	Zero-bias emitter-base depletion capacitance.
`vde=0.52 V`	Emitter-base diffusion voltage.
`pe=0.3`	Emitter-base grading coefficient.
`trvr=1e-09 s`	Low injection reverse transit time due to charge stored in the epilayer under the collector.
`trn=3e-09 s`	Low injection reverse transit time due to charge stored in the collector and the buried layer under the collector.
`cjc=3.9e-13 F`	Zero-bias collector-base depletion capacitance.
`vdc=0.57 V`	Collector-base diffusion voltage.
`pc=0.36`	Collector-base grading coefficient.
`cjs=1.3e-12 F`	Zero-bias substrate-base depletion capacitance.
`vds=0.52 V`	Substrate-base diffusion voltage.
`ps=0.35`	Substrate-base grading coefficient.
`tref=25 C`	Reference temperature. Default set by option `tnom`.
`dta=0 K`	Difference between the device temperature and the ambient analysis temperature.
`vgeb=1.21 V`	Bandgap voltage of the emitter-base depletion region.

© 2023 Cadence Design Systems, Inc.

`vgcb=1.21 V`	Bandgap voltage of the collector-base depletion region.
`vgsb=1.21 V`	Bandgap voltage of the substrate-base depletion region.
`vgb=1.21 V`	Bandgap voltage of the base between emitter and collector.
`vge=1.21 V`	Bandgap voltage of the emitter.
`vgje=1.12 V`	Bandgap voltage recombination emitter-base junction.
`ae=4.48`	Temperature coefficient of `bf`.
`spb=2.85`	SC.
`snb=2.6`	Temperature coefficient of the epitaxial base electron mobility.
`snbn=0.3`	Temperature coefficient of buried layer electron mobility.
`spe=0.73`	Temperature coefficient of emitter hole mobility.
`spc=0.73`	Temperature coefficient of collector hole mobility.
`sx=1`	Temperature coefficient of combined minority carrier mobility in emitter and buried layer.
`kf=0`	Flickernoise coefficient.
`af=1`	Flickernoise exponent.
`exphi=0`	Not used in model bjt500.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`type=npn`	Transistor gender. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`imax=1000 A`	Explosion current.
`tnom (C)`	alias of tnom.
`tr (C)`	alias of tnom.
`compatible=spectre`	

© 2023 Cadence Design Systems, Inc.

	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`ic (A)`	External DC collector current.
`ib (A)`	External DC base current.
`ie (A)`	Resistive emitter current.
`isub (A)`	Resistive substrate current.
`iflat (A)`	Lateral forward current.
`irlat (A)`	Lateral reverse current.
`ifver (A)`	Vertical forward current.
`irver (A)`	Vertical reverse current.
`ire (A)`	ideal forward base current.
`ile (A)`	Non-ideal forward base current.
`ise (A)`	Forward substrate current.
`irc (A)`	Ideal reverse base current.
`ilc (A)`	Non-ideal reverse base current.
`isc (A)`	Reverse substrate current.
`isf (A)`	Reverse leakage current of the substrate-base junction.
`ip (A)`	Main current.
`betadc`	External DC current gain Ic/Ib.
`vbc (V)`	Base-collector voltage.
`vbe (V)`	Base-emitter voltage.
`vce (V)`	Collector-emitter voltage.
`vsb (V)`	Substrate-base voltage.
`rcex (Ω)`	External part of the collector resistance.
`rcin (Ω)`	Internal part of the collector resistance.

© 2023 Cadence Design Systems, Inc.

`reex (Ω)`	External part of the emitter resistance.
`rein (Ω)`	Internal part of the emitter resistance.
`rbc (Ω)`	Base resistance under the collector.
`rbe (Ω)`	Base resistance under the emitter.
`rsb (Ω)`	Ohmic leakage across the substrate-base junction.
`pwr (W)`	Power.
`gfl (S)`	Forward conductance, lateral path.
`grl (S)`	Reverse conductance, lateral path.
`g11 (S)`	Forward conductance, vertical path.
`g12 (S)`	Collector Early-effect on Ifver.
`g21 (S)`	Emitter Early-effect on Irver.
`g22 (S)`	Reverse conductance, vertical path.
`gpiv (S)`	Conductance emitter-base junction.
`gmuv (S)`	Conductance collector-base junction.
`gbe (S)`	Emitter-side: base conductance B1-B.
`gibe (S)`	Emitter Early-effect on Ib1b.
`gbc (S)`	Collector-side: base conductance B2-B.
`gibc (S)`	Collector Early-effect on Ib2b.
`gise (S)`	Transconductance (parasitic PNP) e-b-s transistor.
`gisc (S)`	Transconductance (parasitic PNP) c-b-s transistor.
`gsb (S)`	Conductance substrate-base junction.
`cpil (F)`	Forward diffusion capacitance, lateral path.
`cipil (F)`	Collector Early-effect on Qflat.
`cpiv (F)`	Forward total capacitance, vertical path.
`cmul (F)`	Reverse diffusion capacitance, lateral path.
`cimul (F)`	Emitter Early-effect on Qrlat.
`cmuv (F)`	Reverse total capacitance, vertical path.
`csb (F)`	Total capacitance substrate-base junction.
`irbe (A)`	Ideal total forward base current.

© 2023 Cadence Design Systems, Inc.

`irbc (A)`	Ideal total reverse base current.
`irsb (A)`	Substrate base leakage resistance current.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual device temperature.
`jtype`	Type +1=npn and -1=pnp.

Related Topics

Philips Models

Lateral PNP Transistor (bjt500)

Lateral PNP Transistor (bjt301)

Vertical NPN/PNP Transistor (bjt503)

The bjt503 model provides a detailed description of a vertical integrated NPN and PNP transistor. It is described in the Philips Bipolar Modelbook (Dec.95) as TN/TNS and TP/TPS level 503.

The NPN is also described in Nat.Lab. Unclassified Report Nr. 006/94 as Mextram Bipolar Transistor Model. Information on how to obtain this document can be found on Source Link by searching for Philips.

(c) Philips Electronics N.V. 1993,1996

In addition to the model description a `level` parameter is added. Via the `level` parameter the user can switch between Philips Bipolar Modelbook (Dec.95) and Philips Bipolar Modelbook (Dec.94).

The `imax` parameter is used to aid convergence and to prevent numerical overflow. The junction characteristics of the transistor are accurately modeled for currents up to `imax`. For currents above `imax`, the junction is modeled as a linear resistor and a warning is printed.

The descriptions of the operating point derivatives are given for the NPN type. For the PNP type the terminal voltage in the descriptions has to be exchanged. E.g.:

NPN: gx = dIn/dVb2e1

© 2023 Cadence Design Systems, Inc.

PNP: gx = dIn/dVe1b2

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Sample Instance Statement

```
q4 (vcc net3 minus) npn_mod region=fwd m=1 mult=1
```

Sample Model Statement:

```
model npn_mod bjt503 type=npn level=2 exmod=1 is=1e-14 bf=85 ik=95e-6 rbc=50
cje=0.352e-12
```

Instance Syntax

```
Name  c  b  e  [s] ModelName parameter=value ...
```

Instance Parameters

`area=1`	Area factor.
`mult=1`	Alias of area factor.
`m=1`	Multiplication factor.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `fwd`, `rev`, and `sat`.
`trise=0.0 K`	Temperature rise from ambient.
`lv1=1`	
`lv4=1`	

Model Syntax

```
model modelName bjt503 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`type=npn`	Transistor type. Possible values are `npn`, `npnv`, `pnp`, and `pnpv`.
`level=2.0`	Transistor Level. Possible values are `1` (Philips Bipolar Modelbook Dec.94) or `2` (Philips Bipolar Modelbook Dec.95).
`exmod=0`	Flag for extended modeling of the reverse current gain.
`exphi=0`	Flag for distributed high frequency effects.
`exavl=1`	Flag for extended modeling of avalanche currents.
`is=5.0e-17 A`	Collector-emitter saturation current.
`bf=140.0 A/A`	Ideal forward current gain.
`xibi=0.0`	Fraction of ideal base current that belongs to the sidewall.
`ibf=2.0e-14 A`	Saturation current of the non-ideal forward base current.
`vlf=0.5 V`	Cross-over voltage of the non-ideal forward base current.
`ik=15.0e-3 A`	High-injection knee current.
`bri=16.0 A/A`	Ideal reverse current gain.
`ibr=8.0e-15 A`	Saturation current of the non-ideal reverse base current.
`vlr=0.5 V`	Cross-over voltage of the non-ideal reverse base current.
`xext=0.5`	Part of `Iex`, `Qex`, `Qtex` and `Isub` that depends on `Vbc1`.
`qbo=1.2e-12 Coul`	Base charge at zero bias.
`eta=4.0`	Factor of the built-in field of the base.
`avl=50.0`	Weak avalanche parameter.
`efi=0.7`	Electric field intercept (with `exavl`=1.
`ihc=3.0e-3 A`	Critical current for hot carriers.
`rcc=25.0 Ω`	Constant part of the collector resistance.
`rcv=750.0 Ω`	Resistance of the unmodulated epilayer.

© 2023 Cadence Design Systems, Inc.

scrcv=1000.0 Ω	Space charge resistance of the epilayer.
sfh=0.6	Current spreading factor epilayer.
rbc=50.0 Ω	Constant part of the base resistance.
rbv=100.0 Ω	Variable part of the base resistance at zero bias.
re=2.0 Ω	Emitter series resistance.
taune=3.0e-10 s	Minimum delay time of neutral and emitter charge.
mtau=1.18	Non-ideality factor of the neutral and emitter charge.
cje=2.5e-13 F	Zero bias emitter-base depletion capacitance.
vde=0.9 V	Emitter-base diffusion voltage.
pe=0.33	Emitter-base grading coefficient.
xcje=0.5	Fraction of the e-b depletion cap. that belongs to the sidewall.
cjc=1.3e-13 F	Zero bias collector-base depletion capacitance.
vdc=0.6 V	Collector-base diffusion voltage.
pc=0.4	Collector-base grading coefficient variable part.
xp=0.2	Constant part of cjc.
mc=0.5	Collector current modulation coefficient.
xcjc=0.1	Fraction of the collector-base depletion cap. under the emitter area.
tref (C)	Reference temperature. Default set by option tnom.
tnom (C)	Alias of tref. Default set by option tnom.
tr (C)	Alias of tref. Default set by option tnom.
dta=0.0 K	Difference of the device temperature to the ambient temperature. It served as the default value of instance trise.
trise=0.0 K	Alias of dta.
vge=1.01 V	Band-gap voltage of the emitter.
vgb=1.18 V	Band-gap voltage of the base.
vgc=1.205 V	Band-gap voltage of the collector.
vgj=1.1 V	Band-gap voltage recombination emitter-base junction.

© 2023 Cadence Design Systems, Inc.

`vi=0.04 V`	Ionization voltage base dope.
`na=3.0e17 cm`$^{-3}$	Maximum base dope concentration.
`er=2.0e-3`	Temperature coefficient of `vlf` and `vlr`.
`ab=1.35`	Temperature coefficient resistivity base.
`aepi=2.15`	Temperature coefficient resistivity of the epilayer.
`aex=1.0`	Temperature coefficient resistivity of the extrinsic base.
`ac=0.4`	Temperature coefficient resistivity of the buried layer.
`kf=2.0e-16`	Flickernoise coefficient ideal base current.
`kfn=2.0e-16`	Flickernoise coefficient non-ideal base current.
`af=1.0`	Flickernoise exponent.
`iss=6.0e-16 A`	Base-substrate saturation current.
`iks=5.0e-6 A`	Knee current of the substrate.
`cjs=1.0e-12 F`	Zero bias collector-substrate depletion capacitance.
`vds=0.5 V`	Collector-substrate diffusion voltage.
`ps=0.33`	Collector-substrate grading coefficient.
`vgs=1.15 V`	Band-gap voltage of the substrate.
`as=2.15`	For a closed buried layer: `as=ac`. For an open buried layer: `as=aepi`.
`imax=1.0 A`	Explosion current.
`vers=503`	Version mextrem.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, and `spiceplus`.
`subs=1`	

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`ib (A)`	Base current.
`ic (A)`	Collector current.
`ie (A)`	Emitter current.
`is (A)`	Substrate current.
`vbe (V)`	Base-emitter voltage.
`vbc (V)`	Base-collector voltage.
`vce (V)`	Collector-emitter voltage.
`vsc (V)`	Substrate voltage.
`re (Ω)`	Constant emitter resistance.
`rcc (Ω)`	Constant collector resistance.
`rbc (Ω)`	Constant part of base resistance.
`betadc (A/A)`	DC current gain.
`pwr (W)`	Power.
`Vb1e1 (V)`	Internal voltage.
`Vb2e1 (V)`	Internal voltage.
`Vb2c1 (V)`	Internal voltage.
`Vb2c2 (V)`	Internal voltage.
`Vb1b2 (V)`	Internal voltage.
`Vb1c1 (V)`	Internal voltage.
`Vbc1 (V)`	Internal voltage.
`in (A)`	Main current.
`ic1c2 (A)`	Variable collector resistance current.
`ib1 (A)`	Bulk component of ideal base current.
`ib1s (A)`	Sidewall component of ideal base current.
`ib2 (A)`	Non-ideal base current.
`iavl (A)`	Weak avalanche current.
`ib1b2 (A)`	Variable base resistance current.
`ib3 (A)`	Non-ideal reverse base current.

© 2023 Cadence Design Systems, Inc.

`iex (A)`	Internal extrinsic base current.
`isub (A)`	Internal base-substrate current.
`isf (A)`	Substrate-collector current.
`xiex (A)`	External extrinsic base current.
`Xisub (A)`	External base-substrate current.
`gx (S)`	dIn/dVb2e1.
`gy (S)`	dIn/dVb2c2.
`gz (S)`	dIn/dVb2c1.
`grcvy (S)`	dIc1c2/dVb2c2.
`grcvz (S)`	dIc1c2/dVb2c1.
`gpi (S)`	Conductance floor base-emitter junction: dIb1/dVb2e1 + dIb2/dVb2e1.
`sgpi (S)`	Conductance sidewall base-emitter junction: dIb1S/dVb1e1.
`gmux (S)`	Dependence avalanche multiplication on internal b-e junction: -dIavl/dVb2e1.
`gmu (S)`	Dependence avalanche multiplication on internal b-c junction: -dIavl/dVb2c2.
`gmuz (S)`	Dependence avalanche multiplication on external b-c junction:-dIavl/dVb2c1.
`grbv (S)`	dIb1b2/dVb1b2.
`grbvx (S)`	Emitter Early-effect on Ib1b2: dIb1b2/dVb2e1.
`grbvy (S)`	Internal collector Early-effect on Ib1b2: dIb1b2/dVb2c2.
`grbvz (S)`	External collector Early effect on Ib1b2: dIb1b2/dVb2c1.
`gmuex (S)`	Conductance floor extrinsic b-c junction: dIex/dVb1c1 + dIsub/dVb1c1 + dIb3/dVb1c1.
`xgmuex (S)`	Conductance sidewall extrinsic b-c junction: dXIex/dVbc1 + dXIsub/dVbc1.
`gsub (S)`	Conductance s-c junction: dIsf/dVsc1.

© 2023 Cadence Design Systems, Inc.

`gpnp (S)`	Transconductance floor extrinsic PNP transistor: dIsub/dVb1c1.
`xgpnp (S)`	Transconductance sidewall extrinsic PNP transistor: dXIsub/dVbc1.
`cbex (F)`	Capacitance floor b-e junction: dQte/dVb2e1 + dQbe/dVb2e1 + dQn/dVb2e1.
`cbey (F)`	Internal collector Early-effect on Qbe: dQbe/dVb2c2.
`cbez (F)`	External collector Early-effect on Qbe: dQbe/dVb2c1.
`scte (F)`	Dependence of QteS on internal b-e junction: dQteS/dVb2e1.
`cbcx (F)`	Emitter Early-effect on Qbc: dQbc/dVb2e1.
`cbcy (F)`	Capacitance intrinsic b-c junction: dQtc/dVb2c2 + dQbc/dVb2c2 + dQepi/dVb2c2.
`cbcz (F)`	Collector Early-effect on Qtc: dQtc/dVb2c1 + dQbc/dVb2c1 + dQepi/dVb2c1.
`cb1b2 (F)`	Capacitance AC current crowding: dQb1b2/dVb1b2 = Cb.
`cb1b2x (F)`	Dependence of Qb1b2 on internal b-e junction voltage: dQb1b2/dVb2e1.
`cbcex (F)`	Capacitance floor extrinsic b-c junction: dQtex/dVb1c1 + dQex/dVb1c1.
`xcbcex (F)`	Capacitance sidewall extrinsic b-c junction: dXQtex/dVbc1 + dXQex/dVbc1.
`cts (F)`	Capacitance s-c junction: dQtex/dVb1c1 + dQex/dVb1c1.
`lv6 (A)`	
`lv7 (S)`	
`lv8 (A)`	
`lv9 (A)`	
`lv10 (A/A)`	
`lv11 (A/A)`	
`lv14 (Ω)`	

© 2023 Cadence Design Systems, Inc.

lv15 (Ω)	
lv16 (S)	
lx0 (V)	
lx1 (V)	
lx2 (A)	
lx3 (A)	
cbe (F)	Cbe.
cbc (F)	Cbc.
csc (F)	Csc.

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt504t)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd504t)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

Compact Bipolar-Transistor Model (bjtd3500t)

Compact Bipolar-Transistor Model (bjt504)

This is SimKit 5.2.

Compact Bipolar-Transistor Model

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Instance Syntax

```
Name  c  b  e  s ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjt504 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=504`	Bipolar Level.
`paramchk=0`	Level of clip warning info.
`mexlev=2`	flag for ELDO model.
`tref=25 deg. C`	Reference temperature.
`dta=0 K`	Difference between the local ambient and global ambient temperature.
`exmod=1`	Flag for extended modeling of reverse current gain.
`exphi=1`	Flag for the distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modeling of avalanche currents.
`exsub=0`	Flag for extended modeling of substrate currents.
`is=2.2e-17 A`	Collector-emitter saturation current.
`ik=0.1 A`	Collector-emitter high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`bf=215`	Ideal forward current gain.
`ibf=2.7e-15 A`	Saturation current of the non-ideal forward base current.
`mlf=2`	Non ideality factor of the non-ideal forward base current.
`xibi=0`	Part of ideal base current that belongs to the sidewall.
`izeb=0 A`	Pre-factor of emitter-base Zener tunneling current.
`nzeb=22`	Coefficient of emitter-base Zener tunneling current.
`bri=7`	Ideal reverse current gain.
`ibr=1e-15 A`	Saturation current of the non-ideal reverse base current.
`vlr=0.2 V`	Cross-over voltage of the non-ideal reverse base current.
`xext=0.63`	Part of Iex, Qtex, Qex and Isub that depends on Vbc3(Vbc3) instead of Vb1c4(Vb1c4).

© 2023 Cadence Design Systems, Inc.

`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.
`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model (when EXAVL=1).
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of the base resistance.
`rbv=18 Ω`	Zero-bias value of the variable part of the base resistance.
`rcc=12 Ω`	Collector contact resistance.
`rcblx=0`	Resistance of collector buried layer under the extrinsic transistor.
`rcbli=0`	Resistance of collector buried layer under the Intrinsic transistor.
`rcv=150 Ω`	Resistance of the un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of the epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in the epilayer.
`axi=0.3`	Smoothness parameter for the onset of quasi-saturation.
`cje=7.3e-14 F`	Zero-bias emitter-base depletion capacitance.
`vde=0.95 V`	Emitter-base diffusion voltage.
`pe=0.4`	Emitter-base grading coefficient.
`xcje=0.4`	Fraction of the emitter-base depletion capacitance that belongs to the sidewall.
`cbeo=0`	Emitter-base overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias collector-base depletion capacitance.
`vdc=0.68 V`	Collector-base diffusion voltage.
`pc=0.5`	Collector-base grading coefficient.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for the current modulation of the collector-base depletion capacitance.

© 2023 Cadence Design Systems, Inc.

`xcjc=0.032`	Fraction of the collector-base depletion capacitance under the emitter.
`cbco=0`	Collector-base overlap capacitance.
`mtau=1`	Non-ideality factor of the emitter stored charge.
`taue=2e-12 s`	Minimum transit time of stored emitter charge.
`taub=4.2e-12 s`	Transit time of stored base charge.
`tepi=4.1e-11 s`	Transit time of stored epilayer charge.
`taur=5.2e-10 s`	Transit time of reverse extrinsic base charge.
`deg=0 eV`	Bandgap difference over the base.
`xrec=0`	Pre-factor of the recombination part of Ib1.
`xqb=0.333`	Fraction of the total base charge supplied by the collector instead of the base (Base charge partitioning).
`aqbo=0.3`	Temperature coefficient of the zero-bias base charge.
`ae=0`	Temperature coefficient of the resistivity of the emitter.
`ab=1`	Temperature coefficient of the resistivity of the base.
`dais=0`	Parameter for fine tuning of temperature dependence of collector-emitter saturation current.
`aepi=2.5`	Temperature coefficient of the resistivity of the epilayer.
`aex=0.62`	Temperature coefficient of the resistivity of the extrinsic base.
`ac=2`	Temperature coefficient of the resistivity of the collector contact.
`acbl=2`	Temperature coefficient of the resistivity of the collector buried layer.
`dvgbf=0.05 V`	Bandgap voltage difference of forward current gain.
`dvgbr=0.045 V`	Bandgap voltage difference of reverse current gain.
`vgb=1.17 V`	Bandgap voltage of the base.
`vgc=1.18 V`	Bandgap voltage of the collector.
`vgj=1.15 V`	Bandgap voltage recombination emitter-base junction.

© 2023 Cadence Design Systems, Inc.

vgzeb=1.15 V	Band-gap at reference temperature relevant to the Zener effect in the emitter-base junction.
avgeb=0.000473 V/K	Temperature scaling coefficient of emitter-base Zener tunneling current.
tvgeb=636 K	Temperature scaling coefficient of emitter-base Zener tunneling current.
dvgte=0.05 V	Bandgap voltage difference of emitter stored charge.
af=2	Exponent of the Flicker-noise.
kf=2e-11	Flicker-noise coefficient of the ideal base current.
kfn=2e-11	Flicker-noise coefficient of the non-ideal base current.
kavl=0	Switch for white noise contribution due to avalanche.
kavlver=504	Switch for avalanche noise of 504.11 and 504.12.
kc=0	Switch for RF correlation noise model selection.
ke=0	Fraction of QE in excess phase shift.
ftaun=0	Fraction of noise transit time to total transit time.
iss=4.8e-17 A	Base-substrate saturation current.
icss=-1 A	Collector-substrate ideal saturation current.
iks=0.00025 A	Base-substrate high injection knee current.
cjs=3.15e-13 F	Zero-bias collector-substrate depletion capacitance.
vds=0.62 V	Collector-substrate diffusion voltage.
ps=0.34	Collector-substrate grading coefficient.
vgs=1.2 V	Band-gap voltage of the substrate.
as=1.58	For a closed buried layer: As=Ac: for an open buried layer: As=Aepi.
asub=2	Temperature coefficient for mobility of minorities in the substrate.
vexlim=400	Upper limit of exp() function argument for convergence.
subs=1	Flag of supporting substrate or not.

© 2023 Cadence Design Systems, Inc.

`type=npn`	Transistor type. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`imax=1000 A`	Explosion current.
`mvt0=0.0`	Threshold mismatch intercept.
`tnom (deg. C)`	Parameters measurement temperature.
`tr (deg. C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica` and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`Ic (A)`	External DC collector current.
`Ib (A)`	External DC base current.
`Ie (A)`	External DC emitter current.
`Is (A)`	External DC substrate current.
`BetaDC`	External DC current gain Ic/Ib.
`Vbe (V)`	External base-emitter bias.
`Vbc (V)`	External base-collector bias.
`Vce (V)`	External collector-emitter bias.
`Vse (V)`	External substrate-emitter bias.
`Vbs (V)`	External base-substrate bias.
`Vsc (V)`	External substrate-collector bias.
`Vb2e1 (V)`	Internal base-emitter bias.
`Vb2c2 (V)`	Internal base-collector bias.
`Vb2c1 (V)`	Internal base-collector bias including epilayer.
`Vb1c1 (V)`	External base-collector bias without contact resistances.
`Vb1c4 (V)`	External base-collector bias with contact resistance RCBLI.
`Vc3c4 (V)`	External collector-collector bias over contact resistance RCBLX.
`Vc4c1 (V)`	Bias over intrinsic buried layer.
`Ve1e (V)`	Bias over emitter resistance.
`In (A)`	Main current.
`Ic1c2 (A)`	Epilayer current.

© 2023 Cadence Design Systems, Inc.

`Ib1b2 (A)`	Pinched-base current.
`Ib1 (A)`	Ideal forward base current.
`SIb1 (A)`	Ideal side-wall base current.
`Izteb (A)`	Zener tunneling current in the emitter base junction.
`Ib2 (A)`	Non-ideal forward base current.
`Ib3 (A)`	Non-ideal reverse base current.
`Iex (A)`	Extrinsic reverse base current.
`XIex (A)`	Extrinsic reverse base current.
`Iavl (A)`	Avalanche current.
`IRE (A)`	Current through emitter resistance.
`IRBC (A)`	Current through constant base resistance.
`IRCC (A)`	Current through collector contact resistance.
`IRCBLX (A)`	Current through extrinsic collector resistance.
`IRCBLI (A)`	Current through intrinsic collector resistance.
`Qe (C)`	Emitter charge or emitter neutral charge.
`Qte (C)`	Base-emitter depletion charge.
`SQte (C)`	Sidewall base-emitter depletion charge.
`Qbe (C)`	Base-emitter diffusion charge.
`Qbc (C)`	Base-collector diffusion charge.
`Qtc (C)`	Base-collector depletion charge.
`Qepi (C)`	Epilayer diffusion charge.
`Qb1b2 (C)`	AC current crowding charge.
`Qtex (C)`	Extrinsic base-collector depletion charge.
`XQtex (C)`	Extrinsic base-collector depletion charge.
`Qex (C)`	Extrinsic base-collector diffusion charge.
`XQex (C)`	Extrinsic base-collector diffusion charge.
`gx (1/Ω)`	Forward transconductance.
`gy (1/Ω)`	Reverse transconductance.
`gz (1/Ω)`	Reverse transconductance.

© 2023 Cadence Design Systems, Inc.

`Sgpi (1/Ω)`	Conductance sidewall b-e junction.
`gpix (1/Ω)`	Conductance floor b-e junction.
`gpiy (1/Ω)`	Early effect on recombination base current.
`gpiz (1/Ω)`	Early effect on recombination base current.
`gmux (1/Ω)`	Early effect on avalanche current limiting.
`gmuy (1/Ω)`	Conductance of avalanche current.
`gmuz (1/Ω)`	Conductance of avalanche current.
`gmuex (1/Ω)`	Conductance extrinsic b-c junction.
`Xgmuex (1/Ω)`	Conductance extrinsic b-c junction.
`grcvy (1/Ω)`	Conductance of the epilayer current.
`grcvz (1/Ω)`	Conductance of the epilayer current.
`Rbv (Ω)`	Base resistance.
`grbvx (1/Ω)`	Early-effect on base resistance.
`grbvy (1/Ω)`	Early-effect on base resistance.
`grbvz (1/Ω)`	Early-effect on base resistance:.
`RE (Ω)`	Emitter resistance.
`RBC (Ω)`	Constant part of the base resistance.
`RCC (Ω)`	Collector contact resistance.
`RCBLX (Ω)`	Resistance of collector buried layer under the extrinsic transistor.
`RCBLI (Ω)`	Resistance of collector buried layer under the Intrinsic transistor.
`SCbe (F)`	Capacitance sidewall b-e junction.
`Cbex (F)`	Capacitance floor b-e junction.
`Cbey (F)`	Early effect on b-e diffusion charge.
`Cbez (F)`	Early effect on b-e diffusion charge.
`Cbcx (F)`	Early effect on b-c diffusion charge.
`Cbcy (F)`	Capacitance floor b-c junction.
`Cbcz (F)`	Capacitance floor b-c junction.

© 2023 Cadence Design Systems, Inc.

Cbcex (F)	Capacitance extrinsic b-c junction.
XCbcex (F)	Capacitance extrinsic b-c junction.
Cb1b2 (F)	Capacitance AC current crowding.
Cb1b2x (F)	Cross-capacitance of the AC current crowding.
Cb1b2y (F)	Cross-capacitance of the AC current crowding.
Cb1b2z (F)	Cross-capacitance of the AC current crowding.
gm (1/Ω)	Transconductance.
beta	Current amplification.
gout (1/Ω)	Output conductance.
gmu (1/Ω)	Feedback transconductance.
RB (Ω)	Base resistance.
Cbe (F)	Base-emitter capacitance.
Cbc (F)	Base-collector capacitance.
fT (Hz)	Good approximation for cut-off frequency.
Iqs (A)	Current at onset of quasi-saturation.
XiWepi (M)	Thickness of injection layer.
Vb2c2star (V)	Physical value of internal base-collector bias.
Pdiss (W)	Dissipation.
pwr (W)	Power dissipation.
TK (K)	Actual temperature.
Isub (A)	Substrate current.
XIsub (A)	Substrate current.
Isf (A)	Substrate failure current.
Qts (C)	Collector-substrate depletion charge.
gS (1/Ω)	Conductance parasitic PNP transistor.
XgS (1/Ω)	Conductance parasitic PNP transistor.
gSf (1/Ω)	Conductance of s-c junction.
Cts (F)	Capacitance s-c junction.
jtype	Type: +1=npn and -1=pnp.

© 2023 Cadence Design Systems, Inc.

w_estimate (M)
l_estimate (M)

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504t)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd504t)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

Compact Bipolar-Transistor Model (bjtd3500t)

Compact Bipolar-Transistor Model (bjt504t)

This is SimKit 5.2.

Compact Bipolar-Transistor Model

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Instance Syntax

```
Name  c  b  e  s  dt ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjt504t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=504`	Bipolar Level.
`paramchk=0`	Level of clip warning info.
`mexlev=2`	flag for ELDO model.
`tref=25 deg. C`	Reference temperature.
`dta=0 K`	Difference between the local ambient and global ambient temperature.
`exmod=1`	Flag for extended modelling of reverse current gain.
`exphi=1`	Flag for the distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modelling of avalanche currents.
`exsub=0`	Flag for extended modelling of substrate currents.
`is=2.2e-17 A`	Collector-emitter saturation current.
`ik=0.1 A`	Collector-emitter high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`bf=215`	Ideal forward current gain.
`ibf=2.7e-15 A`	Saturation current of the non-ideal forward base current.
`mlf=2`	Non ideality factor of the non-ideal forward base current.
`xibi=0`	Part of ideal base current that belongs to the sidewall.
`izeb=0 A`	Pre-factor of emitter-base Zener tunneling current.
`nzeb=22`	Coefficient of emitter-base Zener tunneling current.
`bri=7`	Ideal reverse current gain.
`ibr=1e-15 A`	Saturation current of the non-ideal reverse base current.
`vlr=0.2 V`	Cross-over voltage of the non-ideal reverse base current.
`xext=0.63`	Part of Iex, Qtex, Qex and Isub that depends on Vbc3(Vbc3) instead of Vb1c4(Vb1c4).

© 2023 Cadence Design Systems, Inc.

`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.
`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model (when EXAVL=1).
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of the base resistance.
`rbv=18 Ω`	Zero-bias value of the variable part of the base resistance.
`rcc=12 Ω`	Collector contact resistance.
`rcblx=0`	Resistance of collector buried layer under the extrinsic transistor.
`rcbli=0`	Resistance of collector buried layer under the Intrinsic transistor.
`rcv=150 Ω`	Resistance of the un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of the epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in the epilayer.
`axi=0.3`	Smoothness parameter for the onset of quasi-saturation.
`cje=7.3e-14 F`	Zero-bias emitter-base depletion capacitance.
`vde=0.95 V`	Emitter-base diffusion voltage.
`pe=0.4`	Emitter-base grading coefficient.
`xcje=0.4`	Fraction of the emitter-base depletion capacitance that belongs to the sidewall.
`cbeo=0`	Emitter-base overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias collector-base depletion capacitance.
`vdc=0.68 V`	Collector-base diffusion voltage.
`pc=0.5`	Collector-base grading coefficient.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for the current modulation of the collector-base depletion capacitance.

© 2023 Cadence Design Systems, Inc.

xcjc=0.032	Fraction of the collector-base depletion capacitance under the emitter.
cbco=0	Collector-base overlap capacitance.
mtau=1	Non-ideality factor of the emitter stored charge.
taue=2e-12 s	Minimum transit time of stored emitter charge.
taub=4.2e-12 s	Transit time of stored base charge.
tepi=4.1e-11 s	Transit time of stored epilayer charge.
taur=5.2e-10 s	Transit time of reverse extrinsic base charge.
deg=0 eV	Bandgap difference over the base.
xrec=0	Pre-factor of the recombination part of Ib1.
xqb=0.333	Fraction of the total base charge supplied by the collector instead of the base (Base charge partitioning).
aqbo=0.3	Temperature coefficient of the zero-bias base charge.
ae=0	Temperature coefficient of the resistivity of the emitter.
ab=1	Temperature coefficient of the resistivity of the base.
dais=0	Parameter for fine tuning of temperature dependence of collector-emitter saturation current.
aepi=2.5	Temperature coefficient of the resistivity of the epilayer.
aex=0.62	Temperature coefficient of the resistivity of the extrinsic base.
ac=2	Temperature coefficient of the resistivity of the collector contact.
acbl=2	Temperature coefficient of the resistivity of the collector buried layer.
dvgbf=0.05 V	Bandgap voltage difference of forward current gain.
dvgbr=0.045 V	Bandgap voltage difference of reverse current gain.
vgb=1.17 V	Bandgap voltage of the base.
vgc=1.18 V	Bandgap voltage of the collector.
vgj=1.15 V	Bandgap voltage recombination emitter-base junction.

© 2023 Cadence Design Systems, Inc.

vgzeb=1.15 V	Band-gap at reference temperature relevant to the Zener effect in the emitter-base junction.
avgeb=0.000473 V/K	Temperature scaling coefficient of emitter-base Zener tunneling current.
tvgeb=636 K	Temperature scaling coefficient of emitter-base Zener tunneling current.
dvgte=0.05 V	Bandgap voltage difference of emitter stored charge.
af=2	Exponent of the Flicker-noise.
kf=2e-11	Flicker-noise coefficient of the ideal base current.
kfn=2e-11	Flicker-noise coefficient of the non-ideal base current.
kavl=0	Switch for white noise contribution due to avalanche.
kavlver=504	Switch for avalanche noise of 504.11 and 504.12.
kc=0	Switch for RF correlation noise model selection.
ke=0	Fraction of QE in excess phase shift.
ftaun=0	Fraction of noise transit time to total transit time.
iss=4.8e-17 A	Base-substrate saturation current.
icss=-1 A	Collector-substrate ideal saturation current.
iks=0.00025 A	Base-substrate high injection knee current.
cjs=3.15e-13 F	Zero-bias collector-substrate depletion capacitance.
vds=0.62 V	Collector-substrate diffusion voltage.
ps=0.34	Collector-substrate grading coefficient.
vgs=1.2 V	Band-gap voltage of the substrate.
as=1.58	For a closed buried layer: As=Ac: for an open buried layer: As=Aepi.
asub=2	Temperature coefficient for mobility of minorities in the substrate.
rth=300 K/W	Thermal resistance.
cth=3e-09 J/K	Thermal capacitance.
ath=0	Temperature coefficient of the thermal resistance.

© 2023 Cadence Design Systems, Inc.

`vexlim=400`	Upper limit of exp() function argument for convergence.
`subs=1`	Flag of supporting substrate or not.
`type=npn`	Transistor gender. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`imax=1000 A`	Explosion current.
`mvt0=0.0`	Threshold mismatch intercept.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`Ic (A)`	External DC collector current.
`Ib (A)`	External DC base current.
`Ie (A)`	External DC emitter current.
`Is (A)`	External DC substrate current.
`BetaDC`	External DC current gain Ic/Ib.
`Vbe (V)`	External base-emitter bias.
`Vbc (V)`	External base-collector bias.
`Vce (V)`	External collector-emitter bias.
`Vse (V)`	External substrate-emitter bias.
`Vbs (V)`	External base-substrate bias.
`Vsc (V)`	External substrate-collector bias.
`Vb2e1 (V)`	Internal base-emitter bias.
`Vb2c2 (V)`	Internal base-collector bias.
`Vb2c1 (V)`	Internal base-collector bias including epilayer.
`Vb1c1 (V)`	External base-collector bias without contact resistances.
`Vb1c4 (V)`	External base-collector bias with contact resistance RCBLI.
`Vc3c4 (V)`	External collector-collector bias over contact resistance RCBLX.
`Vc4c1 (V)`	Bias over intrinsic buried layer.
`Ve1e (V)`	Bias over emitter resistance.
`In (A)`	Main current.
`Ic1c2 (A)`	Epilayer current.

© 2023 Cadence Design Systems, Inc.

`Ib1b2 (A)`	Pinched-base current.
`Ib1 (A)`	Ideal forward base current.
`SIb1 (A)`	Ideal side-wall base current.
`Izteb (A)`	Zener tunneling current in the emitter base junction.
`Ib2 (A)`	Non-ideal forward base current.
`Ib3 (A)`	Non-ideal reverse base current.
`Iex (A)`	Extrinsic reverse base current.
`XIex (A)`	Extrinsic reverse base current.
`Iavl (A)`	Avalanche current.
`IRE (A)`	Current through emitter resistance.
`IRBC (A)`	Current through constant base resistance.
`IRCC (A)`	Current through collector contact resistance.
`IRCBLX (A)`	Current through extrinsic collector resistance.
`IRCBLI (A)`	Current through intrinsic collector resistance.
`Qe (C)`	Emitter charge or emitter neutral charge.
`Qte (C)`	Base-emitter depletion charge.
`SQte (C)`	Sidewall base-emitter depletion charge.
`Qbe (C)`	Base-emitter diffusion charge.
`Qbc (C)`	Base-collector diffusion charge.
`Qtc (C)`	Base-collector depletion charge.
`Qepi (C)`	Epilayer diffusion charge.
`Qb1b2 (C)`	AC current crowding charge.
`Qtex (C)`	Extrinsic base-collector depletion charge.
`XQtex (C)`	Extrinsic base-collector depletion charge.
`Qex (C)`	Extrinsic base-collector diffusion charge.
`XQex (C)`	Extrinsic base-collector diffusion charge.
`gx (1/Ω)`	Forward transconductance.
`gy (1/Ω)`	Reverse transconductance.
`gz (1/Ω)`	Reverse transconductance.

© 2023 Cadence Design Systems, Inc.

Sgpi (1/Ω)	Conductance sidewall b-e junction.
gpix (1/Ω)	Conductance floor b-e junction.
gpiy (1/Ω)	Early effect on recombination base current.
gpiz (1/Ω)	Early effect on recombination base current.
gmux (1/Ω)	Early effect on avalanche current limiting.
gmuy (1/Ω)	Conductance of avalanche current.
gmuz (1/Ω)	Conductance of avalanche current.
gmuex (1/Ω)	Conductance extrinsic b-c junction.
Xgmuex (1/Ω)	Conductance extrinsic b-c junction.
grcvy (1/Ω)	Conductance of the epilayer current.
grcvz (1/Ω)	Conductance of the epilayer current.
Rbv (Ω)	Base resistance.
grbvx (1/Ω)	Early-effect on base resistance.
grbvy (1/Ω)	Early-effect on base resistance.
grbvz (1/Ω)	Early-effect on base resistance:.
RE (Ω)	Emitter resistance.
RBC (Ω)	Constant part of the base resistance.
RCC (Ω)	Collector contact resistance.
RCBLX (Ω)	Resistance of collector buried layer under the extrinsic transistor.
RCBLI (Ω)	Resistance of collector buried layer under the Intrinsic transistor.
SCbe (F)	Capacitance sidewall b-e junction.
Cbex (F)	Capacitance floor b-e junction.
Cbey (F)	Early effect on b-e diffusion charge.
Cbez (F)	Early effect on b-e diffusion charge.
Cbcx (F)	Early effect on b-c diffusion charge.
Cbcy (F)	Capacitance floor b-c junction.
Cbcz (F)	Capacitance floor b-c junction.

© 2023 Cadence Design Systems, Inc.

Cbcex (F)	Capacitance extrinsic b-c junction.
XCbcex (F)	Capacitance extrinsic b-c junction.
Cb1b2 (F)	Capacitance AC current crowding.
Cb1b2x (F)	Cross-capacitance of the AC current crowding.
Cb1b2y (F)	Cross-capacitance of the AC current crowding.
Cb1b2z (F)	Cross-capacitance of the AC current crowding.
gm (1/Ω)	Transconductance.
beta	Current amplification.
gout (1/Ω)	Output conductance.
gmu (1/Ω)	Feedback transconductance.
RB (Ω)	Base resistance.
Cbe (F)	Base-emitter capacitance.
Cbc (F)	Base-collector capacitance.
fT (Hz)	Good approximation for cut-off frequency.
Iqs (A)	Current at onset of quasi-saturation.
XiWepi (M)	Thickness of injection layer.
Vb2c2star (V)	Physical value of internal base-collector bias.
Pdiss (W)	Dissipation.
pwr (W)	Power dissipation.
TK (K)	Actual temperature.
Isub (A)	Substrate current.
XIsub (A)	Substrate current.
Isf (A)	Substrate failure current.
Qts (C)	Collector-substrate depletion charge.
gS (1/Ω)	Conductance parasitic PNP transistor.
XgS (1/Ω)	Conductance parasitic PNP transistor.
gSf (1/Ω)	Conductance of s-c junction.
Cts (F)	Capacitance s-c junction.
jtype	Type: +1=npn and -1=pnp.

© 2023 Cadence Design Systems, Inc.

`w_estimate (M)`
`l_estimate (M)`

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd504t)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

Compact Bipolar-Transistor Model (bjtd3500t)

Compact Bipolar-Transistor Model (bjt505)

This is SimKit 5.2.

BJT505 Model

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Instance Syntax

```
Name  c  b  e ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`dta=0 degC`	Difference between the local and global ambient temperatures.
`mult=1`	Multiplication factor.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid.Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjt505 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=505`	Model level.
`paramchk=0`	Level of clip warning info.
`version=505`	Model version.
`type=npn`	Flag for NPN (1) or PNP (-1) transistor type.Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`tref=25 degC`	Reference temperature.
`exmod=1`	Flag for extended modeling of the reverse current gain.
`exphi=1`	Flag for distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modeling of avalanche currents.
`exsub=1`	Flag for extended modeling of substrate currents.
`is=2.2e-17 A`	Saturation current of main current.
`nff=1`	Non-ideality factor of forward main current.
`nfr=1`	Non-ideality factor of reverse main current.
`ik=0.1 A`	CE high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`ibi=1e-19 A`	Saturation current of ideal base current.
`nbi=1`	Non-ideality factor of ideal base current.
`ibis=0 A`	Saturation current of ideal side wall base current.
`nbis=1`	Non-ideality factor of ideal side wall base current.
`ibf=2.7e-15 A`	Saturation current of non-ideal forward base current.
`mlf=2`	Non-ideality factor of non-ideal forward base current.
`ibfs=0 A`	Saturation current of non-ideal side wall forward base current.
`mlfs=2`	Non-ideality factor of non-ideal side wall forward base current.
`ibx=3.14e-18 A`	Saturation current of extrinsic reverse base current.

© 2023 Cadence Design Systems, Inc.

`ikbx=0.0143 A`	Extrinsic CB high injection knee current.
`ibr=1e-15 A`	Saturation current of non-ideal reverse base current.
`mlr=2`	Non-ideality factor of non-ideal reverse base current.
`xext=0.63`	Part of currents and charges that belong to extrinsic region.
`izeb=0 A`	Pre-factor of EB Zener tunneling current.
`nzeb=22`	Coefficient of EB Zener tunneling current.
`izcb=0 A`	Pre-factor of CB Zener tunneling current.
`nzcb=22`	Coefficient of CB Zener tunneling current.
`swavl=1`	Switch of avalanche factor Gem model.
`aavl=400`	aavl of swavl=1 Gem model.
`cavl=-0.37`	cavl of swavl=1 Gem model.
`itoavl=0.5 A`	Current dependence parameter of swavl=1 Gem model.
`bavl=25`	bavl of swavl=1 Gem model.
`vdcavl=0.1 V`	CB diffusion voltage dedicated for swavl=1 Gem model.
`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.
`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model when exavl=1.
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of base resistance.
`rbv=18 Ω`	Zero-bias value of variable part of the base resistance.
`rcc=12 Ω`	Constant part of collector resistance.
`rcblx=0 Ω`	Resistance Collector Buried Layer extrinsic.
`rcbli=0 Ω`	Resistance Collector Buried Layer Intrinsic.
`rcv=150 Ω`	Resistance of un-modulated epilayer.
`scrcv=1.25e+03 Ω`	

© 2023 Cadence Design Systems, Inc.

	Space charge resistance of epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in epilayer.
`axi=0.3`	Smoothness parameter for onset of quasi-saturation.
`vdc=0.68 V`	CB diffusion voltage.
`cje=7.3e-14 F`	Zero-bias EB depletion capacitance.
`vde=0.95 V`	EB diffusion voltage.
`pe=0.4`	EB grading coefficient.
`xcje=0.4`	Sidewall fraction of EB depletion capacitance.
`cbeo=0 F`	EB overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias CB depletion capacitance.
`vdcctc=0.68 V`	CB diffusion voltage of depletion capacitance.
`pc=0.5`	CB grading coefficient.
`swvchc=0`	Switch of Vch for CB depletion capacitance.
`swvjunc=0`	Switch of Vjunc for collector junction capacitance.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for current modulation of CB depletion capacitance.
`xcjc=0.032`	Fraction of CB depletion capacitance under the emitter.
`cbco=0 F`	CB overlap capacitance.
`vbrcb=100 V`	Breakdown voltage for CB junction leakage.
`pbrcb=4 V`	Breakdown onset tuning parameter for CB junction leakage.
`frevcb=1e+03`	Coefficient for limiting CB junction breakdown leakage current.
`swjbrcb=0`	Switch for breakdown in CB junction leakage.
`mtau=1`	Non-ideality factor of emitter stored charge.
`taue=2e-12 s`	Minimum transit time of stored emitter charge.
`taub=4.2e-12 s`	Transit time of stored base charge.
`tepi=4.1e-11 s`	Transit time of stored epilayer charge.

© 2023 Cadence Design Systems, Inc.

`taur=5.2e-10 s`	Transit time of reverse extrinsic stored base charge.
`deg=0 eV`	Bandgap difference over the base.
`xrec=0`	Pre-factor of the recombination part of Ib1.
`xqb=0.333`	Emitter-fraction of base diffusion charge.
`ke=0`	Fraction of QE in excess phase shift.
`aqbo=0.3`	Temperature coefficient of zero-bias base charge.
`ab=1`	Temperature coefficient of resistivity of the base.
`ae=0`	Temperature coefficient of resistivity of the emitter.
`aepi=2.5`	Temperature coefficient of resistivity of the epilayer.
`aex=0.62`	Temperature coefficient of resistivity of the extrinsic base.
`ac=2`	Temperature coefficient of resistivity of the collector contact.
`acx=1.3`	Temperature coefficient of extrinsic reverse base current.
`acbl=2`	Temperature coefficient of resistivity of the collector buried layer.
`vgb=1.17 V`	Band-gap voltage of base.
`vgc=1.18 V`	Band-gap voltage of collector.
`vge=1.12 V`	Band-gap voltage of emitter.
`vgcx=1.12 V`	Band-gap voltage of extrinsic collector.
`vgj=1.15 V`	Band-gap voltage recombination EB junction.
`vgzeb=1.15 V`	Band-gap voltage at Tref for EB tunneling.
`avgeb=0.000473 V/K`	Temperature coefficient of band-gap voltage for EB tunneling.
`tvgeb=636 K`	Temperature coefficient of band-gap voltage for EB tunneling.
`vgzcb=1.15 V`	Band-gap voltage at Tref for CB tunneling.
`avgcb=0.000473 V/K`	Temperature coefficient of band-gap voltage for CB tunneling.

© 2023 Cadence Design Systems, Inc.

tvgcb=636 K	Temperature coefficient of band-gap voltage for CB tunneling.
dvgte=0.05 V	Band-gap voltage difference of emitter stored charge.
dais=0	Fine tuning of temperature dependence of CE saturation current.
tnff=0 /K	Temperature coefficient of nff.
tnfr=0 /K	Temperature coefficient of nfr.
tbavl=0.0005	Temperature scaling parameter of bavl when swavl=1.
af=2	Exponent of Flicker-noise of ideal base current.
afn=2	Exponent of Flicker-noise of non-ideal base current.
kf=2e-11	Flicker-noise coefficient of ideal base current.
kfn=2e-11	Flicker-noise coefficient of non-ideal base current.
kavl=0	Switch for white noise contribution due to avalanche.
kc=0	Switch for RF correlation noise model selection.
ftaun=0	Fraction of noise transit time to total transit time.
iss=4.8e-17 A	Saturation current of parasitic BCS transistor main current.
icss=0 A	CS ideal saturation current.
iks=0.000545 A	Knee current for BCS transistor main current.
ikcs=5e-05 A	Knee current for CS junction diode current.
cjs=3.15e-13 F	Zero-bias CS depletion capacitance.
vds=0.62 V	CS diffusion voltage.
ps=0.34	CS grading coefficient.
vgs=1.2 V	Band-gap voltage of the substrate.
as=1.58	Substrate temperature coefficient.
asub=2	Temperature coefficient for mobility of minorities in the substrate.
xisubi=0	Part of substrate current that belongs to intrinsic region.

© 2023 Cadence Design Systems, Inc.

`swvsch=0`	Switch for Vsc induced high injection in main currents of BCS transistors and CS diode current.
`isibrel=0 A`	Saturation current of base current for reliability simulation.
`nfibrel=2`	Non-ideality factor of base current for reliability simulation.
`gmin=1e-13`	Minimum conductance.
`vexlim=400`	Upper limit of exp() function argument for convergence.
`imax=1000 A`	Explosion current.
`tnom (degC)`	Parameters measurement temperature.
`tr (degC)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator.Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`jtype`	type: +1=npn and -1=pnp.
`r_e (Ω)`	Emitter resistance.
`rb_c (Ω)`	Constant base resistance.
`rc_c (Ω)`	Collector contact resistance.
`rc_blx (Ω)`	Extrinsic buried layer resistance.
`rc_bli (Ω)`	Intrinsic buried layer resistance.
`rc (Ω)`	Collector resistance.
`tk (K)`	Actual temperature.
`ic (A)`	External DC collector current.
`ib (A)`	External DC base current.
`betadc`	External DC current gain Ic/Ib.
`ie (A)`	External DC emitter current.
`vbe (V)`	External base-emitter bias.
`vce (V)`	External collector-emitter bias.
`vbc (V)`	External base-collector bias.
`isx (A)`	External DC substrate current.
`vse (V)`	External substrate-emitter bias.
`vbs (V)`	External base-substrate bias.
`vsc (V)`	External substrate-collector bias.
`vb2e1 (V)`	Internal base-emitter bias.
`vb2c2 (V)`	Internal base-collector bias.
`vb2c1 (V)`	Internal base-collector bias including epilayer.
`vb1c1 (V)`	External base-collector bias without contact resistances.

© 2023 Cadence Design Systems, Inc.

`vc4c1 (V)`	Bias over intrinsic buried layer.
`vc3c4 (V)`	Bias over extrinsic buried layer.
`ve1e (V)`	Bias over emitter resistance.
`in (A)`	Main current.
`ic1c2 (A)`	Epilayer current.
`ib1b2 (A)`	Pinched-base current.
`ib1 (A)`	Ideal forward base current.
`ib1s (A)`	Ideal side-wall base current.
`ib2s (A)`	Non-ideal side-wall base current.
`ibrel (A)`	Additional non-ideal base current for reliability simulation.
`izteb (A)`	Zener tunneling current in the emitter base junction.
`iztcb (A)`	Zener tunneling current in the collector base junction.
`ib2 (A)`	Non-ideal forward base current.
`ib3 (A)`	Non-ideal reverse base current.
`iavl (A)`	Avalanche current.
`iex (A)`	Extrinsic reverse base current.
`xiex (A)`	Extrinsic reverse base current.
`isub (A)`	Substrate current.
`xisub (A)`	Substrate current.
`isf (A)`	Substrate failure current.
`ire (A)`	Current through emitter resistance.
`irbc (A)`	Current through constant base resistance.
`ircblx (A)`	Current through extrinsic buried layer resistance.
`ircbli (A)`	Current through intrinsic buried layer resistance.
`ircc (A)`	Current through collector contact resistance.
`qe (coul)`	Emitter charge or emitter neutral charge.
`qte (coul)`	Base-emitter depletion charge.
`sqte (coul)`	Sidewall base-emitter depletion charge.

© 2023 Cadence Design Systems, Inc.

`qbe (coul)`	Base-emitter diffusion charge.
`qbc (coul)`	Base_collector diffusion charge.
`qtc (coul)`	Base-collector depletion charge.
`qepi (coul)`	Epilayer diffusion charge.
`qb1b2 (coul)`	ac current crowding charge.
`qtex (coul)`	Extrinsic base-collector depletion charge.
`xqtex (coul)`	Extrinsic base-collector depletion charge.
`qex (coul)`	Extrinsic base-collector diffusion charge.
`xqex (coul)`	Extrinsic base-collector diffusion charge.
`qts (coul)`	Collector-substrate depletion charge.
`gx (S)`	Forward transconductance.
`gy (S)`	Reverse transconductance.
`gz (S)`	Reverse transconductance.
`sgpi (S)`	Conductance sidewall b-e junction.
`gpix (S)`	Conductance floor b-e junction.
`gpiy (S)`	Early effect on recombination base current.
`gpiz (S)`	Early effect on recombination base current.
`gmux (S)`	Early effect on avalanche current limiting.
`gmuy (S)`	Conductance of avalanche current.
`gmuz (S)`	Conductance of avalanche current.
`gmuex (S)`	Conductance of extrinsic b-c junction.
`xgmuex (S)`	Conductance of extrinsic b-c junction.
`grcvy (S)`	Conductance of epilayer current.
`grcvz (S)`	Conductance of epilayer current.
`rb_v (Ω)`	Variable base resistance.
`grbvx (S)`	Early effect on variable base resistance.
`grbvy (S)`	Early effect on variable base resistance.
`grbvz (S)`	Early effect on variable base resistance.
`gs (S)`	Conductance parasitic PNP transistor.

© 2023 Cadence Design Systems, Inc.

`xgs (S)`	Conductance parasitic PNP transistor.
`gsf (S)`	Conductance substrate failure current.
`scbe (F)`	Capacitance sidewall b-e junction.
`cbex (F)`	Capacitance floor b-e junction.
`cbey (F)`	Early effect on b-e diffusion charge.
`cbez (F)`	Early effect on b-e diffusion charge.
`cbcx (F)`	Early effect on b-c diffusion charge.
`cbcy (F)`	Capacitance floor b-c junction.
`cbcz (F)`	Capacitance floor b-c junction.
`cbcex (F)`	Capacitance extrinsic b-c junction.
`xcbcex (F)`	Capacitance extrinsic b-c junction.
`cb1b2 (F)`	Capacitance AC current crowding.
`cb1b2x (F)`	Cross-capacitance AC current crowding.
`cb1b2y (F)`	Cross-capacitance AC current crowding.
`cb1b2z (F)`	Cross-capacitance AC current crowding.
`cts (F)`	Capacitance s-c junction.
`gm (S)`	transconductance.
`beta`	Current amplification.
`gout (S)`	Output conductance.
`gmu (S)`	Feedback transconductance.
`rb (Ω)`	Base resistance.
`cbe (F)`	Base-emitter capacitance.
`cbc (F)`	Base-collector capacitance.
`ft (Hz)`	Good approximation for cut-off frequency.
`iqs (A)`	Current at onset of quasi-saturation.
`xiwepi`	Thickness of injection layer normalized to epi layer width.
`vb2c2star (V)`	Physical value of internal base-collector bias

© 2023 Cadence Design Systems, Inc.

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt504t)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd504t)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

Compact Bipolar-Transistor Model (bjtd3500t)

Compact Bipolar-Transistor Model (bjt505t)

Description

This is SiMKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

Instance Syntax

```
Name  c  b  e  s  dt ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`dta=0 degC`	Difference between the local and global ambient temperatures.
`mult=1`	Multiplication factor.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjt505t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=505`	Model level.
`paramchk=0`	Level of clip warning info.
`version=505`	Model version.
`type=npn`	Flag for NPN (1) or PNP (-1) transistor type.Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`tref=25 degC`	Reference temperature.
`exmod=1`	Flag for extended modeling of the reverse current gain.
`exphi=1`	Flag for distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modeling of avalanche currents.
`exsub=1`	Flag for extended modeling of substrate currents.
`is=2.2e-17 A`	Saturation current of main current.
`nff=1`	Non-ideality factor of forward main current.
`nfr=1`	Non-ideality factor of reverse main current.
`ik=0.1 A`	CE high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`ibi=1e-19 A`	Saturation current of ideal base current.
`nbi=1`	Non-ideality factor of ideal base current.
`ibis=0 A`	Saturation current of ideal side wall base current.
`nbis=1`	Non-ideality factor of ideal side wall base current.
`ibf=2.7e-15 A`	Saturation current of non-ideal forward base current.
`mlf=2`	Non-ideality factor of non-ideal forward base current.
`ibfs=0 A`	Saturation current of non-ideal side wall forward base current.
`mlfs=2`	Non-ideality factor of non-ideal side wall forward base current.
`ibx=3.14e-18 A`	Saturation current of extrinsic reverse base current.
`ikbx=0.0143 A`	Extrinsic CB high injection knee current.
`ibr=1e-15 A`	Saturation current of non-ideal reverse base current.

© 2023 Cadence Design Systems, Inc.

`mlr=2`	Non-ideality factor of non-ideal reverse base current.
`xext=0.63`	Part of currents and charges that belong to extrinsic region.
`izeb=0 A`	Pre-factor of EB Zener tunneling current.
`nzeb=22`	Coefficient of EB Zener tunneling current.
`izcb=0 A`	Pre-factor of CB Zener tunneling current.
`nzcb=22`	Coefficient of CB Zener tunneling current.
`swavl=1`	Switch of avalanche factor Gem model.
`aavl=400`	aavl of swavl=1 Gem model.
`cavl=-0.37`	cavl of swavl=1 Gem model.
`itoavl=0.5 A`	Current dependence parameter of swavl=1 Gem model.
`bavl=25`	bavl of swavl=1 Gem model.
`vdcavl=0.1 V`	CB diffusion voltage dedicated for swavl=1 Gem model.
`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.
`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model when exavl=1.
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of base resistance.
`rbv=18 Ω`	Zero-bias value of variable part of the base resistance.
`rcc=12 Ω`	Constant part of collector resistance.
`rcblx=0 Ω`	Resistance Collector Buried Layer extrinsic.
`rcbli=0 Ω`	Resistance Collector Buried Layer Intrinsic.
`rcv=150 Ω`	Resistance of un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in epilayer.
`axi=0.3`	Smoothness parameter for onset of quasi-saturation.
`vdc=0.68 V`	CB diffusion voltage.

© 2023 Cadence Design Systems, Inc.

`cje=7.3e-14 F`	Zero-bias EB depletion capacitance.
`vde=0.95 V`	EB diffusion voltage.
`pe=0.4`	EB grading coefficient.
`xcje=0.4`	Sidewall fraction of EB depletion capacitance.
`cbeo=0 F`	EB overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias CB depletion capacitance.
`vdcctc=0.68 V`	CB diffusion voltage of depletion capacitance.
`pc=0.5`	CB grading coefficient.
`swvchc=0`	Switch of Vch for CB depletion capacitance.
`swvjunc=0`	Switch of Vjunc for collector junction capacitance.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for current modulation of CB depletion capacitance.
`xcjc=0.032`	Fraction of CB depletion capacitance under the emitter.
`cbco=0 F`	CB overlap capacitance.
`vbrcb=100 V`	Breakdown voltage for CB junction leakage.
`pbrcb=4 V`	Breakdown onset tuning parameter for CB junction leakage.
`frevcb=1e+03`	Coefficient for limiting CB junction breakdown leakage current.
`swjbrcb=0`	Switch for breakdown in CB junction leakage.
`mtau=1`	Non-ideality factor of emitter stored charge.
`taue=2e-12 s`	Minimum transit time of stored emitter charge.
`taub=4.2e-12 s`	Transit time of stored base charge.
`tepi=4.1e-11 s`	Transit time of stored epilayer charge.
`taur=5.2e-10 s`	Transit time of reverse extrinsic stored base charge.
`deg=0 eV`	Bandgap difference over the base.
`xrec=0`	Pre-factor of the recombination part of Ib1.
`xqb=0.333`	Emitter-fraction of base diffusion charge.
`ke=0`	Fraction of QE in excess phase shift.

© 2023 Cadence Design Systems, Inc.

`aqbo=0.3`	Temperature coefficient of zero-bias base charge.
`ae=0`	Temperature coefficient of resistivity of the emitter.
`ab=1`	Temperature coefficient of resistivity of the base.
`aepi=2.5`	Temperature coefficient of resistivity of the epilayer.
`aex=0.62`	Temperature coefficient of resistivity of the extrinsic base.
`ac=2`	Temperature coefficient of resistivity of the collector contact.
`acx=1.3`	Temperature coefficient of extrinsic reverse base current.
`acbl=2`	Temperature coefficient of resistivity of the collector buried layer.
`vgb=1.17 V`	Band-gap voltage of base.
`vgc=1.18 V`	Band-gap voltage of collector.
`vge=1.12 V`	Band-gap voltage of emitter.
`vgcx=1.12 V`	Band-gap voltage of extrinsic collector.
`vgj=1.15 V`	Band-gap voltage recombination EB junction.
`vgzeb=1.15 V`	Band-gap voltage at Tref for EB tunneling.
`avgeb=0.000473 V/K`	Temperature coefficient of band-gap voltage for EB tunneling.
`tvgeb=636 K`	Temperature coefficient of band-gap voltage for EB tunneling.
`vgzcb=1.15 V`	Band-gap voltage at Tref for CB tunneling.
`avgcb=0.000473 V/K`	Temperature coefficient of band-gap voltage for CB tunneling.
`tvgcb=636 K`	Temperature coefficient of band-gap voltage for CB tunneling.
`dvgte=0.05 V`	Band-gap voltage difference of emitter stored charge.
`dais=0`	Fine tuning of temperature dependence of CE saturation current.

© 2023 Cadence Design Systems, Inc.

`tnff=0 /K`	Temperature coefficient of nff.
`tnfr=0 /K`	Temperature coefficient of nfr.
`tbavl=0.0005`	Temperature scaling parameter of bavl when swavl=1.
`af=2`	Exponent of Flicker-noise of ideal base current.
`afn=2`	Exponent of Flicker-noise of non-ideal base current.
`kf=2e-11`	Flicker-noise coefficient of ideal base current.
`kfn=2e-11`	Flicker-noise coefficient of non-ideal base current.
`kavl=0`	Switch for white noise contribution due to avalanche.
`kc=0`	Switch for RF correlation noise model selection.
`ftaun=0`	Fraction of noise transit time to total transit time.
`iss=4.8e-17 A`	Saturation current of parasitic BCS transistor main current.
`icss=0 A`	CS ideal saturation current.
`iks=0.000545 A`	Knee current for BCS transistor main current.
`ikcs=5e-05 A`	Knee current for CS junction diode current.
`cjs=3.15e-13 F`	Zero-bias CS depletion capacitance.
`vds=0.62 V`	CS diffusion voltage.
`ps=0.34`	CS grading coefficient.
`vgs=1.2 V`	Band-gap voltage of the substrate.
`as=1.58`	Substrate temperature coefficient.
`asub=2`	Temperature coefficient for mobility of minorities in the substrate.
`xisubi=0`	Part of substrate current that belongs to intrinsic region.
`swvsch=0`	Switch for Vsc induced high injection in main currents of BCS transistors and CS diode current
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of thermal resistance.
`isibrel=0 A`	Saturation current of base current for reliability simulation.

© 2023 Cadence Design Systems, Inc.

`nfibrel=2`	Non-ideality factor of base current for reliability simulation.
`gmin=1e-13`	Minimum conductance.
`vexlim=400`	Upper limit of exp() function argument for convergence.
`imax=1000 A`	Explosion current.
`tnom (degC)`	Parameters measurement temperature.
`tr (degC)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`jtype`	type: +1=npn and -1=pnp.
`ic (A)`	External DC collector current.
`ib (A)`	External DC base current.
`betadc`	External DC current gain Ic/Ib.
`ie (A)`	External DC emitter current.
`vbe (V)`	External base-emitter bias.
`vce (V)`	External collector-emitter bias.
`vbc (V)`	External base-collector bias.
`isx (A)`	External DC substrate current.
`vse (V)`	External substrate-emitter bias.
`vbs (V)`	External base-substrate bias.
`vsc (V)`	External substrate-collector bias.
`vb2e1 (V)`	Internal base-emitter bias.
`vb2c2 (V)`	Internal base-collector bias.
`vb2c1 (V)`	Internal base-collector bias including epilayer.
`vb1c1 (V)`	External base-collector bias without contact resistances.
`vc4c1 (V)`	Bias over intrinsic buried layer.
`vc3c4 (V)`	Bias over extrinsic buried layer.
`ve1e (V)`	Bias over emitter resistance.
`in (A)`	Main current.
`ic1c2 (A)`	Epilayer current.
`ib1b2 (A)`	Pinched-base current.
`ib1 (A)`	Ideal forward base current.

© 2023 Cadence Design Systems, Inc.

`ib1s (A)`	Ideal side-wall base current.
`ib2s (A)`	Non-ideal side-wall base current.
`ibrel (A)`	Additional non-ideal base current for reliability simulation.
`izteb (A)`	Zener tunneling current in the emitter base junction.
`iztcb (A)`	Zener tunneling current in the collector base junction.
`ib2 (A)`	Non-ideal forward base current.
`ib3 (A)`	Non-ideal reverse base current.
`iavl (A)`	Avalanche current.
`iex (A)`	Extrinsic reverse base current.
`xiex (A)`	Extrinsic reverse base current.
`isub (A)`	Substrate current.
`xisub (A)`	Substrate current.
`isf (A)`	Substrate failure current.
`ire (A)`	Current through emitter resistance.
`irbc (A)`	Current through constant base resistance.
`ircblx (A)`	Current through extrinsic buried layer resistance.
`ircbli (A)`	Current through intrinsic buried layer resistance.
`ircc (A)`	Current through collector contact resistance.
`qe (coul)`	Emitter charge or emitter neutral charge.
`qte (coul)`	Base-emitter depletion charge.
`sqte (coul)`	Sidewall base-emitter depletion charge.
`qbe (coul)`	Base-emitter diffusion charge.
`qbc (coul)`	Base_collector diffusion charge.
7 `qtc (coul)`	Base-collector depletion charge.
`qepi (coul)`	Epilayer diffusion charge.
`qb1b2 (coul)`	ac current crowding charge.
`qtex (coul)`	Extrinsic base-collector depletion charge.
`xqtex (coul)`	Extrinsic base-collector depletion charge.

© 2023 Cadence Design Systems, Inc.

`qex (coul)`	Extrinsic base-collector diffusion charge.
`xqex (coul)`	Extrinsic base-collector diffusion charge.
`qts (coul)`	Collector-substrate depletion charge.
`gx (S)`	Forward transconductance.
`gy (S)`	Reverse transconductance.
`gz (S)`	Reverse transconductance.
`sgpi (S)`	Conductance sidewall b-e junction.
`gpix (S)`	Conductance floor b-e junction.
`gpiy (S)`	Early effect on recombination base current.
`gpiz (S)`	Early effect on recombination base current.
`gmux (S)`	Early effect on avalanche current limiting.
`gmuy (S)`	Conductance of avalanche current.
`gmuz (S)`	Conductance of avalanche current.
`gmuex (S)`	Conductance of extrinsic b-c junction.
`xgmuex (S)`	Conductance of extrinsic b-c junction.
`grcvy (S)`	Conductance of epilayer current.
`grcvz (S)`	Conductance of epilayer current.
`rb_v (Ω)`	Variable base resistance.
`grbvx (S)`	Early effect on variable base resistance.
`grbvy (S)`	Early effect on variable base resistance.
`grbvz (S)`	Early effect on variable base resistance.
`r_e (Ω)`	Emitter resistance.
`rb_c (Ω)`	Constant base resistance.
`rc_c (Ω)`	Collector contact resistance.
`rc_blx (Ω)`	Extrinsic buried layer resistance.
`rc_bli (Ω)`	Intrinsic buried layer resistance.
`gs (S)`	Conductance parasitic PNP transistor.
`xgs (S)`	Conductance parasitic PNP transistor.
`gsf (S)`	Conductance substrate failure current.

© 2023 Cadence Design Systems, Inc.

`scbe (F)`	Capacitance sidewall b-e junction.
`cbex (F)`	Capacitance floor b-e junction.
`cbey (F)`	Early effect on b-e diffusion charge.
`cbez (F)`	Early effect on b-e diffusion charge.
`cbcx (F)`	Early effect on b-c diffusion charge.
`cbcy (F)`	Capacitance floor b-c junction.
`cbcz (F)`	Capacitance floor b-c junction.
`cbcex (F)`	Capacitance extrinsic b-c junction.
`xcbcex (F)`	Capacitance extrinsic b-c junction.
`cb1b2 (F)`	Capacitance AC current crowding.
`cb1b2x (F)`	Cross-capacitance AC current crowding.
`cb1b2y (F)`	Cross-capacitance AC current crowding.
`cb1b2z (F)`	Cross-capacitance AC current crowding.
`cts (F)`	Capacitance s-c junction.
`gm (S)`	transconductance.
`beta`	Current amplification.
`gout (S)`	Output conductance.
`gmu (S)`	Feedback transconductance.
`rb (Ω)`	Base resistance.
`rc (Ω)`	Collector resistance.
`cbe (F)`	Base-emitter capacitance.
`cbc (F)`	Base-collector capacitance.
`ft (Hz)`	Good approximation for cut-off frequency.
`iqs (A)`	Current at onset of quasi-saturation.
`xiwepi`	Thickness of injection layer normalized to epi layer width.
`vb2c2star (V)`	Physical value of internal base-collector bias.
`pdiss (W)`	Dissipation.
`tk (K)`	Actual temperature.

© 2023 Cadence Design Systems, Inc.

`pwr (W)` Power.

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt504t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd504t)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

Compact Bipolar-Transistor Model (bjtd3500t)

Compact Bipolar-Transistor Model (bjtd504)

This is SimKit 5.2.

Compact Bipolar-Transistor Model

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

Instance Syntax

```
Name  c  b  e ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of multiplication factor.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjtd504 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=504`	Bipolar Level.
`paramchk=0`	Level of clip warning info.
`mexlev=2`	Flag for ELDO model.
`tref=25 deg. C`	Reference temperature.
`dta=0 K`	Difference between the local ambient and global ambient temperature.
`exmod=1`	Flag for extended modelling of reverse current gain.
`exphi=1`	Flag for the distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modelling of avalanche currents.
`is=2.2e-17 A`	Collector-emitter saturation current.
`ik=0.1 A`	Collector-emitter high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`bf=215`	Ideal forward current gain.
`ibf=2.7e-15 A`	Saturation current of the non-ideal forward base current.
`mlf=2`	Non ideality factor of the non-ideal forward base current.
`xibi=0`	Part of ideal base current that belongs to the sidewall.
`izeb=0 A`	Pre-factor of emitter-base Zener tunneling current.
`nzeb=22`	Coefficient of emitter-base Zener tunneling current.
`bri=7`	Ideal reverse current gain.
`ibr=1e-15 A`	Saturation current of the non-ideal reverse base current.
`vlr=0.2 V`	Cross-over voltage of the non-ideal reverse base current.
`xext=0.63`	Part of Iex, Qtex, Qex and Isub that depends on Vbc3(Vbc3) instead of Vb1c4(Vb1c4).
`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.

© 2023 Cadence Design Systems, Inc.

`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model (when EXAVL=1).
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of the base resistance.
`rbv=18 Ω`	Zero-bias value of the variable part of the base resistance.
`rcc=12 Ω`	Collector contact resistance.
`rcblx=0`	Resistance of collector buried layer under the extrinsic transistor.
`rcbli=0`	Resistance of collector buried layer under the Intrinsic transistor.
`rcv=150 Ω`	Resistance of the un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of the epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in the epilayer.
`axi=0.3`	Smoothness parameter for the onset of quasi-saturation.
`cje=7.3e-14 F`	Zero-bias emitter-base depletion capacitance.
`vde=0.95 V`	Emitter-base diffusion voltage.
`pe=0.4`	Emitter-base grading coefficient.
`xcje=0.4`	Fraction of the emitter-base depletion capacitance that belongs to the sidewall.
`cbeo=0`	Emitter-base overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias collector-base depletion capacitance.
`vdc=0.68 V`	Collector-base diffusion voltage.
`pc=0.5`	Collector-base grading coefficient.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for the current modulation of the collector-base depletion capacitance.

© 2023 Cadence Design Systems, Inc.

xcjc=0.032	Fraction of the collector-base depletion capacitance under the emitter.
cbco=0	Collector-base overlap capacitance.
mtau=1	Non-ideality factor of the emitter stored charge.
taue=2e-12 s	Minimum transit time of stored emitter charge.
taub=4.2e-12 s	Transit time of stored base charge.
tepi=4.1e-11 s	Transit time of stored epilayer charge.
taur=5.2e-10 s	Transit time of reverse extrinsic base charge.
deg=0 eV	Bandgap difference over the base.
xrec=0	Pre-factor of the recombination part of Ib1.
xqb=0.333	Fraction of the total base charge supplied by the collector instead of the base (Base charge partitioning).
aqbo=0.3	Temperature coefficient of the zero-bias base charge.
ae=0	Temperature coefficient of the resistivity of the emitter.
ab=1	Temperature coefficient of the resistivity of the base.
dais=0	Parameter for fine tuning of temperature dependence of collector-emitter saturation current.
aepi=2.5	Temperature coefficient of the resistivity of the epilayer.
aex=0.62	Temperature coefficient of the resistivity of the extrinsic base.
ac=2	Temperature coefficient of the resistivity of the collector contact.
acbl=2	Temperature coefficient of the resistivity of the collector buried layer.
dvgbf=0.05 V	Bandgap voltage difference of forward current gain.
dvgbr=0.045 V	Bandgap voltage difference of reverse current gain.
vgb=1.17 V	Bandgap voltage of the base.
vgc=1.18 V	Bandgap voltage of the collector.
vgj=1.15 V	Bandgap voltage recombination emitter-base junction.

© 2023 Cadence Design Systems, Inc.

`vgzeb=1.15 V`	Band-gap at reference temperature relevant to the Zener effect in the emitter-base junction.
`avgeb=0.000473 V/K`	Temperature scaling coefficient of emitter-base Zener tunneling current.
`tvgeb=636 K`	Temperature scaling coefficient of emitter-base Zener tunneling current.
`dvgte=0.05 V`	Bandgap voltage difference of emitter stored charge.
`af=2`	Exponent of the Flicker-noise.
`kf=2e-11`	Flicker-noise coefficient of the ideal base current.
`kfn=2e-11`	Flicker-noise coefficient of the non-ideal base current.
`kavl=0`	Switch for white noise contribution due to avalanche.
`kavlver=504`	Switch for avalanche noise of 504.11 and 504.12.
`kc=0`	Switch for RF correlation noise model selection.
`ke=0`	Fraction of QE in excess phase shift.
`ftaun=0`	Fraction of noise transit time to total transit time.
`vexlim=400`	Upper limit of exp() function argument for convergence.
`subs=1`	Flag of supporting substrate or not.
`type=npn`	Transistor gender. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`imax=1000 A`	Explosion current.
`mvt0=0.0`	Threshold mismatch intercept.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`Ic (A)`	External DC collector current.
`Ib (A)`	External DC base current.
`Ie (A)`	External DC emitter current.
`BetaDC`	External DC current gain Ic/Ib.
`Vbe (V)`	External base-emitter bias.
`Vbc (V)`	External base-collector bias.
`Vce (V)`	External collector-emitter bias.
`Vb2e1 (V)`	Internal base-emitter bias.
`Vb2c2 (V)`	Internal base-collector bias.
`Vb2c1 (V)`	Internal base-collector bias including epilayer.
`Vb1c1 (V)`	External base-collector bias without contact resistances.
`Vb1c4 (V)`	External base-collector bias with contact resistance RCBLI.
`Vc3c4 (V)`	External collector-collector bias over contact resistance RCBLX.
`Vc4c1 (V)`	Bias over intrinsic buried layer.
`Ve1e (V)`	Bias over emitter resistance.
`In (A)`	Main current.
`Ic1c2 (A)`	Epilayer current.
`Ib1b2 (A)`	Pinched-base current.
`Ib1 (A)`	Ideal forward base current.
`SIb1 (A)`	Ideal side-wall base current.
`Izteb (A)`	Zener tunneling current in the emitter base junction.

© 2023 Cadence Design Systems, Inc.

`Ib2 (A)`	Non-ideal forward base current.
`Ib3 (A)`	Non-ideal reverse base current.
`Iex (A)`	Extrinsic reverse base current.
`XIex (A)`	Extrinsic reverse base current.
`Iavl (A)`	Avalanche current.
`IRE (A)`	Current through emitter resistance.
`IRBC (A)`	Current through constant base resistance.
`IRCC (A)`	Current through collector contact resistance.
`IRCBLX (A)`	Current through extrinsic collector resistance.
`IRCBLI (A)`	Current through intrinsic collector resistance.
`Qe (C)`	Emitter charge or emitter neutral charge.
`Qte (C)`	Base-emitter depletion charge.
`SQte (C)`	Sidewall base-emitter depletion charge.
`Qbe (C)`	Base-emitter diffusion charge.
`Qbc (C)`	Base-collector diffusion charge.
`Qtc (C)`	Base-collector depletion charge.
`Qepi (C)`	Epilayer diffusion charge.
`Qb1b2 (C)`	AC current crowding charge.
`Qtex (C)`	Extrinsic base-collector depletion charge.
`XQtex (C)`	Extrinsic base-collector depletion charge.
`Qex (C)`	Extrinsic base-collector diffusion charge.
`XQex (C)`	Extrinsic base-collector diffusion charge.
`gx (1/Ω)`	Forward transconductance.
`gy (1/Ω)`	Reverse transconductance.
`gz (1/Ω)`	Reverse transconductance.
`Sgpi (1/Ω)`	Conductance sidewall b-e junction.
`gpix (1/Ω)`	Conductance floor b-e junction.
`gpiy (1/Ω)`	Early effect on recombination base current.
`gpiz (1/Ω)`	Early effect on recombination base current.

© 2023 Cadence Design Systems, Inc.

gmux (1/Ω)	Early effect on avalanche current limiting.
gmuy (1/Ω)	Conductance of avalanche current.
gmuz (1/Ω)	Conductance of avalanche current.
gmuex (1/Ω)	Conductance extrinsic b-c junction.
Xgmuex (1/Ω)	Conductance extrinsic b-c junction.
grcvy (1/Ω)	Conductance of the epilayer current.
grcvz (1/Ω)	Conductance of the epilayer current.
Rbv (Ω)	Base resistance.
grbvx (1/Ω)	Early-effect on base resistance.
grbvy (1/Ω)	Early-effect on base resistance.
grbvz (1/Ω)	Early-effect on base resistance:.
RE (Ω)	Emitter resistance.
RBC (Ω)	Constant part of the base resistance.
RCC (Ω)	Collector contact resistance.
RCBLX (Ω)	Resistance of collector buried layer under the extrinsic transistor.
RCBLI (Ω)	Resistance of collector buried layer under the Intrinsic transistor.
SCbe (F)	Capacitance sidewall b-e junction.
Cbex (F)	Capacitance floor b-e junction.
Cbey (F)	Early effect on b-e diffusion charge.
Cbez (F)	Early effect on b-e diffusion charge.
Cbcx (F)	Early effect on b-c diffusion charge.
Cbcy (F)	Capacitance floor b-c junction.
Cbcz (F)	Capacitance floor b-c junction.
Cbcex (F)	Capacitance extrinsic b-c junction.
XCbcex (F)	Capacitance extrinsic b-c junction.
Cb1b2 (F)	Capacitance AC current crowding.
Cb1b2x (F)	Cross-capacitance AC current crowding.

© 2023 Cadence Design Systems, Inc.

Cb1b2y (F)	Cross-capacitance AC current crowding.
Cb1b2z (F)	Cross-capacitance AC current crowding.
gm (1/Ω)	Transconductance.
beta	Current amplification.
gout (1/Ω)	Output conductance.
gmu (1/Ω)	Feedback transconductance.
RB (Ω)	Base resistance.
Cbe (F)	Base-emitter capacitance.
Cbc (F)	Base-collector capacitance.
fT (Hz)	Good approximation for cut-off frequency.
Iqs (A)	Current at onset of quasi-saturation.
XiWepi (M)	Thickness of injection layer.
Vb2c2star (V)	Physical value of internal base-collector bias.
Pdiss (W)	Dissipation.
pwr (W)	Dissipation.
TK (K)	Actual temperature.
jtype	Type: +1=npn and -1=pnp.
w_estimate (M)	
l_estimate (M	

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjt504t)

Compact Bipolar-Transistor Model (bjtd504t)

© 2023 Cadence Design Systems, Inc.

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

Compact Bipolar-Transistor Model (bjtd3500t)

Compact Bipolar-Transistor Model (bjtd504t)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

Instance Syntax

```
Name  c  b  e  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjtd504t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=504`	Bipolar Level.
`paramchk=0`	Level of clip warning info.
`mexlev=2`	Flag for ELDO model.
`tref=25 deg. C`	Reference temperature.
`dta=0 K`	Difference between the local ambient and global ambient temperature.
`exmod=1`	Flag for extended modelling of reverse current gain.
`exphi=1`	Flag for the distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modelling of avalanche currents.
`is=2.2e-17 A`	Collector-emitter saturation current.
`ik=0.1 A`	Collector-emitter high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`bf=215`	Ideal forward current gain.
`ibf=2.7e-15 A`	Saturation current of the non-ideal forward base current.
`mlf=2`	Non ideality factor of the non-ideal forward base current.
`xibi=0`	Part of ideal base current that belongs to the sidewall.
`izeb=0 A`	Pre-factor of emitter-base Zener tunneling current.
`nzeb=22`	Coefficient of emitter-base Zener tunneling current.
`bri=7`	Ideal reverse current gain.
`ibr=1e-15 A`	Saturation current of the non-ideal reverse base current.
`vlr=0.2 V`	Cross-over voltage of the non-ideal reverse base current.
`xext=0.63`	Part of Iex, Qtex, Qex and Isub that depends on Vbc3(Vbc3) instead of Vb1c4(Vb1c4).
`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.

© 2023 Cadence Design Systems, Inc.

`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model (when EXAVL=1).
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of the base resistance.
`rbv=18 Ω`	Zero-bias value of the variable part of the base resistance.
`rcc=12 Ω`	Collector contact resistance.
`rcblx=0`	Resistance of collector buried layer under the extrinsic transistor.
`rcbli=0`	Resistance of collector buried layer under the Intrinsic transistor.
`rcv=150 Ω`	Resistance of the un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of the epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in the epilayer.
`axi=0.3`	Smoothness parameter for the onset of quasi-saturation.
`cje=7.3e-14 F`	Zero-bias emitter-base depletion capacitance.
`vde=0.95 V`	Emitter-base diffusion voltage.
`pe=0.4`	Emitter-base grading coefficient.
`xcje=0.4`	Fraction of the emitter-base depletion capacitance that belongs to the sidewall.
`cbeo=0`	Emitter-base overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias collector-base depletion capacitance.
`vdc=0.68 V`	Collector-base diffusion voltage.
`pc=0.5`	Collector-base grading coefficient.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for the current modulation of the collector-base depletion capacitance.

© 2023 Cadence Design Systems, Inc.

xcjc=0.032	Fraction of the collector-base depletion capacitance under the emitter.
cbco=0	Collector-base overlap capacitance.
mtau=1	Non-ideality factor of the emitter stored charge.
taue=2e-12 s	Minimum transit time of stored emitter charge.
taub=4.2e-12 s	Transit time of stored base charge.
tepi=4.1e-11 s	Transit time of stored epilayer charge.
taur=5.2e-10 s	Transit time of reverse extrinsic base charge.
deg=0 eV	Bandgap difference over the base.
xrec=0	Pre-factor of the recombination part of Ib1.
xqb=0.333	Fraction of the total base charge supplied by the collector instead of the base (Base charge partitioning).
aqbo=0.3	Temperature coefficient of the zero-bias base charge.
ae=0	Temperature coefficient of the resistivity of the emitter.
ab=1	Temperature coefficient of the resistivity of the base.
dais=0	Parameter for fine tuning of temperature dependence of collector-emitter saturation current.
aepi=2.5	Temperature coefficient of the resistivity of the epilayer.
aex=0.62	Temperature coefficient of the resistivity of the extrinsic base.
ac=2	Temperature coefficient of the resistivity of the collector contact.
acbl=2	Temperature coefficient of the resistivity of the collector buried layer.
dvgbf=0.05 V	Bandgap voltage difference of forward current gain.
dvgbr=0.045 V	Bandgap voltage difference of reverse current gain.
vgb=1.17 V	Bandgap voltage of the base.
vgc=1.18 V	Bandgap voltage of the collector.
vgj=1.15 V	Bandgap voltage recombination emitter-base junction.

© 2023 Cadence Design Systems, Inc.

`vgzeb=1.15 V`	Band-gap at reference temperature relevant to the Zener effect in the emitter-base junction.
`avgeb=0.000473 V/K`	Temperature scaling coefficient of emitter-base Zener tunneling current.
`tvgeb=636 K`	Temperature scaling coefficient of emitter-base Zener tunneling current.
`dvgte=0.05 V`	Bandgap voltage difference of emitter stored charge.
`af=2`	Exponent of the Flicker-noise.
`kf=2e-11`	Flicker-noise coefficient of the ideal base current.
`kfn=2e-11`	Flicker-noise coefficient of the non-ideal base current.
`kavl=0`	Switch for white noise contribution due to avalanche.
`kavlver=504`	Switch for avalanche noise of 504.11 and 504.12.
`kc=0`	Switch for RF correlation noise model selection.
`ke=0`	Fraction of QE in excess phase shift.
`ftaun=0`	Fraction of noise transit time to total transit time.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`vexlim=400`	Upper limit of exp() function argument for convergence.
`subs=1`	Flag of supporting substrate or not.
`type=npn`	Transistor gender. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`imax=1000 A`	Explosion current.
`mvt0=0.0`	Threshold mismatch intercept.
`tnom (deg. C)`	Parameters measurement temperature.
`tr (deg. C)`	Alias of tnom.
`compatible=spectre`	

© 2023 Cadence Design Systems, Inc.

	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`Ic (A)`	External DC collector current.
`Ib (A)`	External DC base current.
`Ie (A)`	External DC emitter current.
`BetaDC`	External DC current gain Ic/Ib.
`Vbe (V)`	External base-emitter bias.
`Vbc (V)`	External base-collector bias.
`Vce (V)`	External collector-emitter bias.
`Vb2e1 (V)`	Internal base-emitter bias.
`Vb2c2 (V)`	Internal base-collector bias.
`Vb2c1 (V)`	Internal base-collector bias including epilayer.
`Vb1c1 (V)`	External base-collector bias without contact resistances.
`Vb1c4 (V)`	External base-collector bias with contact resistance RCBLI.
`Vc3c4 (V)`	External collector-collector bias over contact resistance RCBLX.
`Vc4c1 (V)`	Bias over intrinsic buried layer.
`Ve1e (V)`	Bias over emitter resistance.
`In (A)`	Main current.
`Ic1c2 (A)`	Epilayer current.
`Ib1b2 (A)`	Pinched-base current.
`Ib1 (A)`	Ideal forward base current.
`SIb1 (A)`	Ideal side-wall base current.
`Izteb (A)`	Zener tunneling current in the emitter base junction.
`Ib2 (A)`	Non-ideal forward base current.
`Ib3 (A)`	Non-ideal reverse base current.
`Iex (A)`	Extrinsic reverse base current.
`XIex (A)`	Extrinsic reverse base current.
`Iavl (A)`	Avalanche current.

© 2023 Cadence Design Systems, Inc.

IRE (A)	Current through emitter resistance.
IRBC (A)	Current through constant base resistance.
IRCC (A)	Current through collector contact resistance.
IRCBLX (A)	Current through extrinsic collector resistance.
IRCBLI (A)	Current through intrinsic collector resistance.
Qe (C)	Emitter charge or emitter neutral charge.
Qte (C)	Base-emitter depletion charge.
SQte (C)	Sidewall base-emitter depletion charge.
Qbe (C)	Base-emitter diffusion charge.
Qbc (C)	Base-collector diffusion charge.
Qtc (C)	Base-collector depletion charge.
Qepi (C)	Epilayer diffusion charge.
Qb1b2 (C)	AC current crowding charge.
Qtex (C)	Extrinsic base-collector depletion charge.
XQtex (C)	Extrinsic base-collector depletion charge.
Qex (C)	Extrinsic base-collector diffusion charge.
XQex (C)	Extrinsic base-collector diffusion charge.
gx (1/Ω)	Forward transconductance.
gy (1/Ω)	Reverse transconductance.
gz (1/Ω)	Reverse transconductance.
Sgpi (1/Ω)	Conductance sidewall b-e junction.
gpix (1/Ω)	Conductance floor b-e junction.
gpiy (1/Ω)	Early effect on recombination base current.
gpiz (1/Ω)	Early effect on recombination base current.
gmux (1/Ω)	Early effect on avalanche current limiting.
gmuy (1/Ω)	Conductance of avalanche current.
gmuz (1/Ω)	Conductance of avalanche current.
gmuex (1/Ω)	Conductance extrinsic b-c junction.
Xgmuex (1/Ω)	Conductance extrinsic b-c junction.

© 2023 Cadence Design Systems, Inc.

grcvy (1/Ω)	Conductance of the epilayer current.
grcvz (1/Ω)	Conductance of the epilayer current.
Rbv (Ω)	Base resistance.
grbvx (1/Ω)	Early-effect on base resistance.
grbvy (1/Ω)	Early-effect on base resistance.
grbvz (1/Ω)	Early-effect on base resistance:.
RE (Ω)	Emitter resistance.
RBC (Ω)	Constant part of the base resistance.
RCC (Ω)	Collector contact resistance.
RCBLX (Ω)	Resistance of collector buried layer under the extrinsic transistor.
RCBLI (Ω)	Resistance of collector buried layer under the Intrinsic transistor.
SCbe (F)	Capacitance sidewall b-e junction.
Cbex (F)	Capacitance floor b-e junction.
Cbey (F)	Early effect on b-e diffusion charge.
Cbez (F)	Early effect on b-e diffusion charge.
Cbcx (F)	Early effect on b-c diffusion charge.
Cbcy (F)	Capacitance floor b-c junction.
Cbcz (F)	Capacitance floor b-c junction.
Cbcex (F)	Capacitance extrinsic b-c junction.
XCbcex (F)	Capacitance extrinsic b-c junction.
Cb1b2 (F)	Capacitance AC current crowding.
Cb1b2x (F)	Cross-capacitance AC current crowding.
Cb1b2y (F)	Cross-capacitance AC current crowding.
Cb1b2z (F)	Cross-capacitance AC current crowding.
gm (1/Ω)	Transconductance.
beta	Current amplification.
gout (1/Ω)	Output conductance.

© 2023 Cadence Design Systems, Inc.

gmu (1/Ω)	Feedback transconductance.
RB (Ω)	Base resistance.
Cbe (F)	Base-emitter capacitance.
Cbc (F)	Base-collector capacitance.
fT (Hz)	Good approximation for cut-off frequency.
Iqs (A)	Current at onset of quasi-saturation.
XiWepi (M)	Thickness of injection layer.
Vb2c2star (V)	Physical value of internal base-collector bias.
Pdiss (W)	Dissipation.
pwr (W)	Dissipation.
TK (K)	Actual temperature.
jtype	Type: +1=npn and -1=pnp.
w_estimate (M)	
l_estimate (M)	

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd504t)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

Compact Bipolar-Transistor Model (bjtd3500t)

© 2023 Cadence Design Systems, Inc.

Compact Bipolar-Transistor Model (bjtd505)

Description

This is SiMKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

Instance Syntax

```
Name  c  b  e ModelName parameter=value ...
```

Instance Parameters

`dta=0 degC`	Difference between the local and global ambient temperatures.
`mult=1`	Multiplication factor.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjtd505 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=505`	Model level.
`paramchk=0`	Level of clip warning info.
`version=505`	Model version.
`type=npn`	Flag for NPN (1) or PNP (-1) transistor type. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`tref=25 degC`	Reference temperature.
`exmod=1`	Flag for extended modeling of the reverse current gain.
`exphi=1`	Flag for distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modeling of avalanche currents.
`is=2.2e-17 A`	Saturation current of main current.
`nff=1`	Non-ideality factor of forward main current.
`nfr=1`	Non-ideality factor of reverse main current.
`ik=0.1 A`	CE high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`ibi=1e-19 A`	Saturation current of ideal base current.
`nbi=1`	Non-ideality factor of ideal base current.
`ibis=0 A`	Saturation current of ideal side wall base current.
`nbis=1`	Non-ideality factor of ideal side wall base current.
`ibf=2.7e-15 A`	Saturation current of non-ideal forward base current.
`mlf=2`	Non-ideality factor of non-ideal forward base current.
`ibfs=0 A`	Saturation current of non-ideal side wall forward base current.
`mlfs=2`	Non-ideality factor of non-ideal side wall forward base current.
`ibx=3.14e-18 A`	Saturation current of extrinsic reverse base current.
`ikbx=0.0143 A`	Extrinsic CB high injection knee current.
`ibr=1e-15 A`	Saturation current of non-ideal reverse base current.

© 2023 Cadence Design Systems, Inc.

`mlr=2`	Non-ideality factor of non-ideal reverse base current.
`xext=0.63`	Part of currents and charges that belong to extrinsic region.
`izeb=0 A`	Pre-factor of EB Zener tunneling current.
`nzeb=22`	Coefficient of EB Zener tunneling current.
`izcb=0 A`	Pre-factor of CB Zener tunneling current.
`nzcb=22`	Coefficient of CB Zener tunneling current.
`swavl=1`	Switch of avalanche factor Gem model.
`aavl=400`	aavl of swavl=1 Gem model.
`cavl=-0.37`	cavl of swavl=1 Gem model.
`itoavl=0.5 A`	Current dependence parameter of swavl=1 Gem model.
`bavl=25`	bavl of swavl=1 Gem model.
`vdcavl=0.1 V`	CB diffusion voltage dedicated for swavl=1 Gem model.
`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.
`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model when exavl=1.
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of base resistance.
`rbv=18 Ω`	Zero-bias value of variable part of the base resistance.
`rcc=12 Ω`	Constant part of collector resistance.
`rcblx=0 Ω`	Resistance Collector Buried Layer extrinsic.
`rcbli=0 Ω`	Resistance Collector Buried Layer Intrinsic.
`rcv=150 Ω`	Resistance of un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in epilayer.
`axi=0.3`	Smoothness parameter for onset of quasi-saturation.
`vdc=0.68 V`	CB diffusion voltage.

© 2023 Cadence Design Systems, Inc.

`cje=7.3e-14 F`	Zero-bias EB depletion capacitance.
`vde=0.95 V`	EB diffusion voltage.
`pe=0.4`	EB grading coefficient.
`xcje=0.4`	Sidewall fraction of EB depletion capacitance.
`cbeo=0 F`	EB overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias CB depletion capacitance.
`vdcctc=0.68 V`	CB diffusion voltage of depletion capacitance.
`pc=0.5`	CB grading coefficient.
`swvchc=0`	Switch of Vch for CB depletion capacitance.
`swvjunc=0`	Switch of Vjunc for collector junction capacitance.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for current modulation of CB depletion capacitance.
`xcjc=0.032`	Fraction of CB depletion capacitance under the emitter.
`cbco=0 F`	CB overlap capacitance.
`vbrcb=100 V`	Breakdown voltage for CB junction leakage.
`pbrcb=4 V`	Breakdown onset tuning parameter for CB junction leakage.
`frevcb=1e+03`	Coefficient for limiting CB junction breakdown leakage current.
`swjbrcb=0`	Switch for breakdown in CB junction leakage.
`mtau=1`	Non-ideality factor of emitter stored charge.
`taue=2e-12 s`	Minimum transit time of stored emitter charge.
`taub=4.2e-12 s`	Transit time of stored base charge.
`tepi=4.1e-11 s`	Transit time of stored epilayer charge.
`taur=5.2e-10 s`	Transit time of reverse extrinsic stored base charge.
`deg=0 eV`	Bandgap difference over the base.
`xrec=0`	Pre-factor of the recombination part of Ib1.
`xqb=0.333`	Emitter-fraction of base diffusion charge.
`ke=0`	Fraction of QE in excess phase shift.

© 2023 Cadence Design Systems, Inc.

`aqbo=0.3`	Temperature coefficient of zero-bias base charge.
`ae=0`	Temperature coefficient of resistivity of the emitter.
`ab=1`	Temperature coefficient of resistivity of the base.
`aepi=2.5`	Temperature coefficient of resistivity of the epilayer.
`aex=0.62`	Temperature coefficient of resistivity of the extrinsic base.
`ac=2`	Temperature coefficient of resistivity of the collector contact.
`acx=1.3`	Temperature coefficient of extrinsic reverse base current.
`acbl=2`	Temperature coefficient of resistivity of the collector buried layer.
`vgb=1.17 V`	Band-gap voltage of base.
`vgc=1.18 V`	Band-gap voltage of collector.
`vge=1.12 V`	Band-gap voltage of emitter.
`vgcx=1.12 V`	Band-gap voltage of extrinsic collector.
`vgj=1.15 V`	Band-gap voltage recombination EB junction.
`vgzeb=1.15 V`	Band-gap voltage at Tref for EB tunneling.
`avgeb=0.000473 V/K`	Temperature coefficient of band-gap voltage for EB tunneling.
`tvgeb=636 K`	Temperature coefficient of band-gap voltage for EB tunneling.
`vgzcb=1.15 V`	Band-gap voltage at Tref for CB tunneling.
`avgcb=0.000473 V/K`	Temperature coefficient of band-gap voltage for CB tunneling.
`tvgcb=636 K`	Temperature coefficient of band-gap voltage for CB tunneling.
`dvgte=0.05 V`	Band-gap voltage difference of emitter stored charge.
`dais=0`	Fine tuning of temperature dependence of CE saturation current.
`tnff=0 /K`	Temperature coefficient of nff.
`tnfr=0 /K`	Temperature coefficient of nfr.

© 2023 Cadence Design Systems, Inc.

`tbavl=0.0005`	Temperature scaling parameter of bavl when swavl=1.
`af=2`	Exponent of Flicker-noise of ideal base current.
`afn=2`	Exponent of Flicker-noise of non-ideal base current.
`kf=2e-11`	Flicker-noise coefficient of ideal base current.
`kfn=2e-11`	Flicker-noise coefficient of non-ideal base current.
`kavl=0`	Switch for white noise contribution due to avalanche.
`kc=0`	Switch for RF correlation noise model selection.
`ftaun=0`	Fraction of noise transit time to total transit time.
`isibrel=0 A`	Saturation current of base current for reliability simulation.
`nfibrel=2`	Non-ideality factor of base current for reliability simulation.
`gmin=1e-13`	Minimum conductance.
`vexlim=400`	Upper limit of exp() function argument for convergence.
`imax=1000 A`	Explosion current.
`tnom (degC)`	Parameters measurement temperature.
`tr (degC)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`jtype`	type: +1=npn and -1=pnp.
`r_e (Ω)`	Emitter resistance.
`rb_c (Ω)`	Constant base resistance.
`rc_c (Ω)`	Collector contact resistance.
`rc_blx (Ω)`	Extrinsic buried layer resistance.
`rc_bli (Ω)`	Intrinsic buried layer resistance.
`rc (Ω)`	Collector resistance.
`tk (K)`	Actual temperature.
`ic (A)`	External DC collector current.
`ib (A)`	External DC base current.
`betadc`	External DC current gain Ic/Ib.
`ie (A)`	External DC emitter current.
`vbe (V)`	External base-emitter bias.
`vce (V)`	External collector-emitter bias.
`vbc (V)`	External base-collector bias.
`vb2e1 (V)`	Internal base-emitter bias.
`vb2c2 (V)`	Internal base-collector bias.
`vb2c1 (V)`	Internal base-collector bias including epilayer.
`vb1c1 (V)`	External base-collector bias without contact resistances.
`vc4c1 (V)`	Bias over intrinsic buried layer.
`vc3c4 (V)`	Bias over extrinsic buried layer.
`ve1e (V)`	Bias over emitter resistance.
`in (A)`	Main current.

© 2023 Cadence Design Systems, Inc.

`ic1c2 (A)`	Epilayer current.
`ib1b2 (A)`	Pinched-base current.
`ib1 (A)`	Ideal forward base current.
`ib1s (A)`	Ideal side-wall base current.
`ib2s (A)`	Non-ideal side-wall base current.
`ibrel (A)`	Additional non-ideal base current for reliability simulation.
`izteb (A)`	Zener tunneling current in the emitter base junction.
`iztcb (A)`	Zener tunneling current in the collector base junction.
`ib2 (A)`	Non-ideal forward base current.
`ib3 (A)`	Non-ideal reverse base current.
`iavl (A)`	Avalanche current.
`iex (A)`	Extrinsic reverse base current.
`xiex (A)`	Extrinsic reverse base current.
`ire (A)`	Current through emitter resistance.
`irbc (A)`	Current through constant base resistance.
`ircblx (A)`	Current through extrinsic buried layer resistance.
`ircbli (A)`	Current through intrinsic buried layer resistance.
`ircc (A)`	Current through collector contact resistance.
`qe (coul)`	Emitter charge or emitter neutral charge.
`qte (coul)`	Base-emitter depletion charge.
`sqte (coul)`	Sidewall base-emitter depletion charge.
`qbe (coul)`	Base-emitter diffusion charge.
`qbc (coul)`	Base_collector diffusion charge.
`qtc (coul)`	Base-collector depletion charge.
`qepi (coul)`	Epilayer diffusion charge.
`qb1b2 (coul)`	ac current crowding charge.
`qtex (coul)`	Extrinsic base-collector depletion charge.
`xqtex (coul)`	Extrinsic base-collector depletion charge.

© 2023 Cadence Design Systems, Inc.

`qex (coul)`	Extrinsic base-collector diffusion charge.
`xqex (coul)`	Extrinsic base-collector diffusion charge.
`gx (S)`	Forward transconductance.
`gy (S)`	Reverse transconductance.
`gz (S)`	Reverse transconductance.
`sgpi (S)`	Conductance sidewall b-e junction.
`gpix (S)`	Conductance floor b-e junction.
`gpiy (S)`	Early effect on recombination base current.
`gpiz (S)`	Early effect on recombination base current.
`gmux (S)`	Early effect on avalanche current limiting.
`gmuy (S)`	Conductance of avalanche current.
`gmuz (S)`	Conductance of avalanche current.
`gmuex (S)`	Conductance of extrinsic b-c junction.
`xgmuex (S)`	Conductance of extrinsic b-c junction.
`grcvy (S)`	Conductance of epilayer current.
`grcvz (S)`	Conductance of epilayer current.
`rb_v (Ω)`	Variable base resistance.
`grbvx (S)`	Early effect on variable base resistance.
`grbvy (S)`	Early effect on variable base resistance.
`grbvz (S)`	Early effect on variable base resistance.
`scbe (F)`	Capacitance sidewall b-e junction.
`cbex (F)`	Capacitance floor b-e junction.
`cbey (F)`	Early effect on b-e diffusion charge.
`cbez (F)`	Early effect on b-e diffusion charge.
`cbcx (F)`	Early effect on b-c diffusion charge.
`cbcy (F)`	Capacitance floor b-c junction.
`cbcz (F)`	Capacitance floor b-c junction.
`cbcex (F)`	Capacitance extrinsic b-c junction.
`xcbcex (F)`	Capacitance extrinsic b-c junction.

© 2023 Cadence Design Systems, Inc.

`cb1b2 (F)`	Capacitance AC current crowding.
`cb1b2x (F)`	Cross-capacitance AC current crowding.
`cb1b2y (F)`	Cross-capacitance AC current crowding.
`cb1b2z (F)`	Cross-capacitance AC current crowding.
`gm (S)`	transconductance.
`beta`	Current amplification.
`gout (S)`	Output conductance.
`gmu (S)`	Feedback transconductance.
`rb (Ω)`	Base resistance.
`cbe (F)`	Base-emitter capacitance.
`cbc (F)`	Base-collector capacitance.
`ft (Hz)`	Good approximation for cut-off frequency.
`iqs (A)`	Current at onset of quasi-saturation.
`xiwepi`	Thickness of injection layer normalized to epi layer width.
`vb2c2star (V)`	Physical value of internal base-collector bias.

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

Compact Bipolar-Transistor Model (bjtd3500t)

© 2023 Cadence Design Systems, Inc.

Compact Bipolar-Transistor Model (bjtd505t)

Description

This is SiMKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so.

Instance Syntax

```
Name  c  b  e  dt ModelName parameter=value ...
```

Instance Parameters

`dta=0 degC`	Difference between the local and global ambient temperatures.
`mult=1`	Multiplication factor.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjtd505t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=505`	Model level.
`paramchk=0`	Level of clip warning info.
`version=505`	Model version.
`type=npn`	Flag for NPN (1) or PNP (-1) transistor type. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`tref=25 degC`	Reference temperature.
`exmod=1`	Flag for extended modeling of the reverse current gain.
`exphi=1`	Flag for distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modeling of avalanche currents.
`is=2.2e-17 A`	Saturation current of main current.
`nff=1`	Non-ideality factor of forward main current.
`nfr=1`	Non-ideality factor of reverse main current.
`ik=0.1 A`	CE high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`ibi=1e-19 A`	Saturation current of ideal base current.
`nbi=1`	Non-ideality factor of ideal base current.
`ibis=0 A`	Saturation current of ideal side wall base current.
`nbis=1`	Non-ideality factor of ideal side wall base current.
`ibf=2.7e-15 A`	Saturation current of non-ideal forward base current.
`mlf=2`	Non-ideality factor of non-ideal forward base current.
`ibfs=0 A`	Saturation current of non-ideal side wall forward base current.
`mlfs=2`	Non-ideality factor of non-ideal side wall forward base current.
`ibx=3.14e-18 A`	Saturation current of extrinsic reverse base current.
`ikbx=0.0143 A`	Extrinsic CB high injection knee current.

© 2023 Cadence Design Systems, Inc.

`ibr=1e-15 A`	Saturation current of non-ideal reverse base current.
`mlr=2`	Non-ideality factor of non-ideal reverse base current.
`xext=0.63`	Part of currents and charges that belong to extrinsic region.
`izeb=0 A`	Pre-factor of EB Zener tunneling current.
`nzeb=22`	Coefficient of EB Zener tunneling current.
`izcb=0 A`	Pre-factor of CB Zener tunneling current.
`nzcb=22`	Coefficient of CB Zener tunneling current.
`swavl=1`	Switch of avalanche factor Gem model.
`aavl=400`	aavl of swavl=1 Gem model.
`cavl=-0.37`	cavl of swavl=1 Gem model.
`itoavl=0.5 A`	Current dependence parameter of swavl=1 Gem model.
`bavl=25`	bavl of swavl=1 Gem model.
`vdcavl=0.1 V`	CB diffusion voltage dedicated for swavl=1 Gem model.
`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.
`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model when exavl=1.
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of base resistance.
`rbv=18 Ω`	Zero-bias value of variable part of the base resistance.
`rcc=12 Ω`	Constant part of collector resistance.
`rcblx=0 Ω`	Resistance Collector Buried Layer extrinsic.
`rcbli=0 Ω`	Resistance Collector Buried Layer Intrinsic.
`rcv=150 Ω`	Resistance of un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of epilayer.

© 2023 Cadence Design Systems, Inc.

`ihc=0.004 A`	Critical current for velocity saturation in epilayer.
`axi=0.3`	Smoothness parameter for onset of quasi-saturation.
`vdc=0.68 V`	CB diffusion voltage.
`cje=7.3e-14 F`	Zero-bias EB depletion capacitance.
`vde=0.95 V`	EB diffusion voltage.
`pe=0.4`	EB grading coefficient.
`xcje=0.4`	Sidewall fraction of EB depletion capacitance.
`cbeo=0 F`	EB overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias CB depletion capacitance.
`vdcctc=0.68 V`	CB diffusion voltage of depletion capacitance.
`pc=0.5`	CB grading coefficient.
`swvchc=0`	Switch of Vch for CB depletion capacitance.
`swvjunc=0`	Switch of Vjunc for collector junction capacitance.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for current modulation of CB depletion capacitance.
`xcjc=0.032`	Fraction of CB depletion capacitance under the emitter.
`cbco=0 F`	CB overlap capacitance.
`vbrcb=100 V`	Breakdown voltage for CB junction leakage.
`pbrcb=4 V`	Breakdown onset tuning parameter for CB junction leakage.
`frevcb=1e+03`	Coefficient for limiting CB junction breakdown leakage current.
`swjbrcb=0`	Switch for breakdown in CB junction leakage.
`mtau=1`	Non-ideality factor of emitter stored charge.
`taue=2e-12 s`	Minimum transit time of stored emitter charge.
`taub=4.2e-12 s`	Transit time of stored base charge.
`tepi=4.1e-11 s`	Transit time of stored epilayer charge.
`taur=5.2e-10 s`	Transit time of reverse extrinsic stored base charge.

© 2023 Cadence Design Systems, Inc.

`deg=0 eV`	Bandgap difference over the base.
`xrec=0`	Pre-factor of the recombination part of Ib1.
`xqb=0.333`	Emitter-fraction of base diffusion charge.
`ke=0`	Fraction of QE in excess phase shift.
`aqbo=0.3`	Temperature coefficient of zero-bias base charge.
`ae=0`	Temperature coefficient of resistivity of the emitter.
`ab=1`	Temperature coefficient of resistivity of the base.
`aepi=2.5`	Temperature coefficient of resistivity of the epilayer.
`aex=0.62`	Temperature coefficient of resistivity of the extrinsic base.
`ac=2`	Temperature coefficient of resistivity of the collector contact.
`acx=1.3`	Temperature coefficient of extrinsic reverse base current.
`acbl=2`	Temperature coefficient of resistivity of the collector buried layer.
`vgb=1.17 V`	Band-gap voltage of base.
`vgc=1.18 V`	Band-gap voltage of collector.
`vge=1.12 V`	Band-gap voltage of emitter.
`vgcx=1.12 V`	Band-gap voltage of extrinsic collector.
`vgj=1.15 V`	Band-gap voltage recombination EB junction.
`vgzeb=1.15 V`	Band-gap voltage at Tref for EB tunneling.
`avgeb=0.000473 V/K`	Temperature coefficient of band-gap voltage for EB tunneling.
`tvgeb=636 K`	Temperature coefficient of band-gap voltage for EB tunneling.
`vgzcb=1.15 V`	Band-gap voltage at Tref for CB tunneling.
`avgcb=0.000473 V/K`	Temperature coefficient of band-gap voltage for CB tunneling.
`tvgcb=636 K`	Temperature coefficient of band-gap voltage for CB tunneling.

© 2023 Cadence Design Systems, Inc.

`dvgte=0.05 V`	Band-gap voltage difference of emitter stored charge.
`dais=0`	Fine tuning of temperature dependence of CE saturation current.
`tnff=0 /K`	Temperature coefficient of nff.
`tnfr=0 /K`	Temperature coefficient of nfr.
`tbavl=0.0005`	Temperature scaling parameter of bavl when swavl=1.
`af=2`	Exponent of Flicker-noise of ideal base current.
`afn=2`	Exponent of Flicker-noise of non-ideal base current.
`kf=2e-11`	Flicker-noise coefficient of ideal base current.
`kfn=2e-11`	Flicker-noise coefficient of non-ideal base current.
`kavl=0`	Switch for white noise contribution due to avalanche.
`kc=0`	Switch for RF correlation noise model selection.
`ftaun=0`	Fraction of noise transit time to total transit time.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of thermal resistance.
`isibrel=0 A`	Saturation current of base current for reliability simulation.
`nfibrel=2`	Non-ideality factor of base current for reliability simulation.
`gmin=1e-13`	Minimum conductance.
`imax=1000 A`	Explosion current.
`vexlim=400`	Upper limit of exp() function argument for convergence.
`tnom (degC)`	Parameters measurement temperature.
`tr (degC)`	Alias of tnom.
`compatible=spectre`	

© 2023 Cadence Design Systems, Inc.

Encourage device equations to be compatible with a foreign simulator.
Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`jtype`	type: +1=npn and -1=pnp.
`ic (A)`	External DC collector current.
`ib (A)`	External DC base current.
`betadc`	External DC current gain Ic/Ib.
`ie (A)`	External DC emitter current.
`vbe (V)`	External base-emitter bias.
`vce (V)`	External collector-emitter bias.
`vbc (V)`	External base-collector bias.
`vb2e1 (V)`	Internal base-emitter bias.
`vb2c2 (V)`	Internal base-collector bias.
`vb2c1 (V)`	Internal base-collector bias including epilayer.
`vb1c1 (V)`	External base-collector bias without contact resistances.
`vc4c1 (V)`	Bias over intrinsic buried layer.
`vc3c4 (V)`	Bias over extrinsic buried layer.
`ve1e (V)`	Bias over emitter resistance.
`in (A)`	Main current.
`ic1c2 (A)`	Epilayer current.
`ib1b2 (A)`	Pinched-base current.
`ib1 (A)`	Ideal forward base current.
`ib1s (A)`	Ideal side-wall base current.
`ib2s (A)`	Non-ideal side-wall base current.
`ibrel (A)`	Additional non-ideal base current for reliability simulation.

© 2023 Cadence Design Systems, Inc.

`izteb (A)`	Zener tunneling current in the emitter base junction.
`iztcb (A)`	Zener tunneling current in the collector base junction.
`ib2 (A)`	Non-ideal forward base current.
`ib3 (A)`	Non-ideal reverse base current.
`iavl (A)`	Avalanche current.
`iex (A)`	Extrinsic reverse base current.
`xiex (A)`	Extrinsic reverse base current.
`ire (A)`	Current through emitter resistance.
`irbc (A)`	Current through constant base resistance.
`ircblx (A)`	Current through extrinsic buried layer resistance.
`ircbli (A)`	Current through intrinsic buried layer resistance.
`ircc (A)`	Current through collector contact resistance.
`qe (coul)`	Emitter charge or emitter neutral charge.
`qte (coul)`	Base-emitter depletion charge.
`sqte (coul)`	Sidewall base-emitter depletion charge.
`qbe (coul)`	Base-emitter diffusion charge.
`qbc (coul)`	Base_collector diffusion charge.
`qtc (coul)`	Base-collector depletion charge.
`qepi (coul)`	Epilayer diffusion charge.
`qb1b2 (coul)`	ac current crowding charge.
`qtex (coul)`	Extrinsic base-collector depletion charge.
`xqtex (coul)`	Extrinsic base-collector depletion charge.
`qex (coul)`	Extrinsic base-collector diffusion charge.
`xqex (coul)`	Extrinsic base-collector diffusion charge.
`gx (S)`	Forward transconductance.
`gy (S)`	Reverse transconductance.
`gz (S)`	Reverse transconductance.
`sgpi (S)`	Conductance sidewall b-e junction.
`gpix (S)`	Conductance floor b-e junction.

© 2023 Cadence Design Systems, Inc.

gpiy (S)	Early effect on recombination base current.
gpiz (S)	Early effect on recombination base current.
gmux (S)	Early effect on avalanche current limiting.
gmuy (S)	Conductance of avalanche current.
gmuz (S)	Conductance of avalanche current.
gmuex (S)	Conductance of extrinsic b-c junction.
xgmuex (S)	Conductance of extrinsic b-c junction.
grcvy (S)	Conductance of epilayer current.
grcvz (S)	Conductance of epilayer current.
rb_v (Ω)	Variable base resistance.
grbvx (S)	Early effect on variable base resistance.
grbvy (S)	Early effect on variable base resistance.
grbvz (S)	Early effect on variable base resistance.
r_e (Ω)	Emitter resistance.
rb_c (Ω)	Constant base resistance.
rc_c (Ω)	Collector contact resistance.
rc_blx (Ω)	Extrinsic buried layer resistance.
rc_bli (Ω)	Intrinsic buried layer resistance.
scbe (F)	Capacitance sidewall b-e junction.
cbex (F)	Capacitance floor b-e junction.
cbey (F)	Early effect on b-e diffusion charge.
cbez (F)	Early effect on b-e diffusion charge.
cbcx (F)	Early effect on b-c diffusion charge.
cbcy (F)	Capacitance floor b-c junction.
cbcz (F)	Capacitance floor b-c junction.
cbcex (F)	Capacitance extrinsic b-c junction.
xcbcex (F)	Capacitance extrinsic b-c junction.
cb1b2 (F)	Capacitance AC current crowding.
cb1b2x (F)	Cross-capacitance AC current crowding.

© 2023 Cadence Design Systems, Inc.

`cb1b2y (F)`	Cross-capacitance AC current crowding.
`cb1b2z (F)`	Cross-capacitance AC current crowding.
`gm (S)`	transconductance.
`beta`	Current amplification.
`gout (S)`	Output conductance.
`gmu (S)`	Feedback transconductance.
`rb (Ω)`	Base resistance.
`rc (Ω)`	Collector resistance.
`cbe (F)`	Base-emitter capacitance.
`cbc (F)`	Base-collector capacitance.
`ft (Hz)`	Good approximation for cut-off frequency.
`iqs (A)`	Current at onset of quasi-saturation.
`xiwepi`	Thickness of injection layer normalized to epi layer width.
`vb2c2star (V)`	Physical value of internal base-collector bias.
`pdiss (W)`	Dissipation.
`tk (K)`	Actual temperature.
`pwr (W)`	Power.

Compact Bipolar-Transistor Model (bjtd3500)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Instance Syntax

```
Name  c  b  e ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjtd3500 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=3.5e+03`	Bipolar Level.
`paramchk=0`	Level of clip warning info.
`mexlev=2`	flag for ELDO model.
`tref=25 deg. C`	Reference temperature.
`dta=0 K`	Difference between the local ambient and global ambient temperature.
`exmod=1`	Flag for extended modelling of reverse current gain.
`exphi=1`	Flag for the distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modelling of avalanche currents.
`is=2.2e-17 A`	Collector-emitter saturation current.
`ik=0.1 A`	Collector-emitter high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`bf=215`	Ideal forward current gain.
`ibf=2.7e-15 A`	Saturation current of the non-ideal forward base current.
`mlf=2`	Non ideality factor of the non-ideal forward base current.
`mhf=1`	Non ideality factor of the non-ideal forward base current.
`mlr=2`	Non ideality factor of the non-ideal reverse base current.
`mhr=1`	Non ideality factor of the ideal reverse base current.
`mf=1`	Non ideality factor of main current.
`xibi=0`	Part of ideal base current that belongs to the sidewall.
`izeb=0 A`	Pre-factor of emitter-base Zener tunneling current.
`nzeb=22`	Coefficient of emitter-base Zener tunneling current.
`bri=7`	Ideal reverse current gain.

© 2023 Cadence Design Systems, Inc.

`ibr=1e-15 A`	Saturation current of the non-ideal reverse base current.
`vlr=0.2 V`	Cross-over voltage of the non-ideal reverse base current.
`xext=0.63`	Part of Iex, Qtex, Qex and Isub that depends on Vbc3(Vbc3) instead of Vb1c4(Vb1c4).
`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.
`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model (when EXAVL=1).
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of the base resistance.
`rbv=18 Ω`	Zero-bias value of the variable part of the base resistance.
`rcc=12 Ω`	Collector contact resistance.
`rcblx=0`	Resistance of collector buried layer under the extrinsic transistor.
`rcbli=0`	Resistance of collector buried layer under the Intrinsic transistor.
`rcv=150 Ω`	Resistance of the un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of the epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in the epilayer.
`axi=0.3`	Smoothness parameter for the onset of quasi-saturation.
`cje=7.3e-14 F`	Zero-bias emitter-base depletion capacitance.
`vde=0.95 V`	Emitter-base diffusion voltage.
`pe=0.4`	Emitter-base grading coefficient.
`xcje=0.4`	Fraction of the emitter-base depletion capacitance that belongs to the sidewall.
`cbeo=0`	Emitter-base overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias collector-base depletion capacitance.

© 2023 Cadence Design Systems, Inc.

`vdc=0.68 V`	Collector-base diffusion voltage.
`pc=0.5`	Collector-base grading coefficient.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for the current modulation of the collector-base depletion capacitance.
`xcjc=0.032`	Fraction of the collector-base depletion capacitance under the emitter.
`cbco=0`	Collector-base overlap capacitance.
`vos=0.04 V`	Voltage describing overshoot.
`isat=0.067 A`	Saturation current.
`repi=6 Ω`	Ohmic resistance epilayer.
`rdmin=0`	Minimum relative collector doping.
`sbjn=0.1`	Smoothness parameter Qtc model.
`sbeb=0.1`	Smoothness parameter Qtc model.
`etavdr=0.23`	Slope-parameter of Vdrift at high electric field.
`nvdr=4`	Power describing saturation behavior of Qtc.
`alfaw=0`	Smooth switch for reachthrough modelling.
`sw=0.1`	Smoothness parameter for reachthrough modelling.
`mtau=1`	Non-ideality factor of the emitter stored charge.
`taue=2e-12 s`	Minimum transit time of stored emitter charge.
`taub=4.2e-12 s`	Transit time of stored base charge.
`tepi=4.1e-11 s`	Transit time of stored epilayer charge.
`taur=5.2e-10 s`	Transit time of reverse extrinsic base charge.
`deg=0 eV`	Bandgap difference over the base.
`xrec=0`	Pre-factor of the recombination part of Ib1.
`aqbo=0.3`	Temperature coefficient of the zero-bias base charge.
`ae=0`	Temperature coefficient of the resistivity of the emitter.
`ab=1`	Temperature coefficient of the resistivity of the base.
`dais=0`	Parameter for fine tuning of temperature dependence of collector-emitter saturation current.

© 2023 Cadence Design Systems, Inc.

`aepi=2.5`	Temperature coefficient of the resistivity of the epilayer.
`aex=0.62`	Temperature coefficient of the resistivity of the extrinsic base.
`ac=2`	Temperature coefficient of the resistivity of the collector contact.
`acbl=2`	Temperature coefficient of the resistivity of the collector buried layer.
`aisat=-0.37`	Temperature coefficient of the saturation current.
`dvgbf=0.05 V`	Bandgap voltage difference of forward current gain.
`dvgbr=0.045 V`	Bandgap voltage difference of reverse current gain.
`vgb=1.17 V`	Bandgap voltage of the base.
`vgc=1.18 V`	Bandgap voltage of the collector.
`vgj=1.15 V`	Bandgap voltage recombination emitter-base junction.
`vgzeb=1.15 V`	Band-gap at reference temperature relevant to the Zener effect in the emitter-base junction.
`avgeb=0.000473 V/K`	Temperature scaling coefficient of emitter-base Zener tunneling current.
`tvgeb=636 K`	Temperature scaling coefficient of emitter-base Zener tunneling current.
`dvgte=0.05 V`	Bandgap voltage difference of emitter stored charge.
`af=2`	Exponent of the Flicker-noise.
`kf=2e-11`	Flicker-noise coefficient of the ideal base current.
`kfn=2e-11`	Flicker-noise coefficient of the non-ideal base current.
`kavl=0`	Switch for white noise contribution due to avalanche.
`type=npn`	Transistor gender. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`imax=1000 A`	Explosion current.
`tnom (deg. C)`	alias of tnom.
`tr (deg. C)`	alias of tnom.
`compatible=spectre`	

© 2023 Cadence Design Systems, Inc.

	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`Ic (A)`	External DC collector current.
`Ib (A)`	External DC base current.
`Ie (A)`	External DC emitter current.
`BetaDC`	External DC current gain Ic/Ib.
`Vbe (V)`	External base-emitter bias.
`Vbc (V)`	External base-collector bias.
`Vce (V)`	External collector-emitter bias.
`Vb2e1 (V)`	Internal base-emitter bias.
`Vb2c2 (V)`	Internal base-collector bias.
`Vb2c1 (V)`	Internal base-collector bias including epilayer.
`Vb1c1 (V)`	External base-collector bias without contact resistances.
`Vb1c4 (V)`	External base-collector bias with contact resistance RCBLI.
`Vc3c4 (V)`	External collector-collector bias over contact resistance RCBLX.
`Vc4c1 (V)`	Bias over intrinsic buried layer.
`Ve1e (V)`	Bias over emitter resistance.
`In (A)`	Main current.
`Ic1c2 (A)`	Epilayer current.
`Ib1b2 (A)`	Pinched-base current.
`Ib1 (A)`	Ideal forward base current.
`SIb1 (A)`	Ideal side-wall base current.
`Izteb (A)`	Zener tunneling current in the emitter base junction.

© 2023 Cadence Design Systems, Inc.

`Ib2 (A)`	Non-ideal forward base current.
`Ib3 (A)`	Non-ideal reverse base current.
`Iex (A)`	Extrinsic reverse base current.
`XIex (A)`	Extrinsic reverse base current.
`Iavl (A)`	Avalanche current.
`IRE (A)`	Current through emitter resistance.
`IRBC (A)`	Current through constant base resistance.
`IRCC (A)`	Current through collector contact resistance.
`IRCBLX (A)`	Current through extrinsic collector resistance.
`IRCBLI (A)`	Current through intrinsic collector resistance.
`Qe (C)`	Emitter charge or emitter neutral charge.
`Qte (C)`	Base-emitter depletion charge.
`SQte (C)`	Sidewall base-emitter depletion charge.
`Qbe (C)`	Base-emitter diffusion charge.
`Qbc (C)`	Base-collector diffusion charge.
`Qtc (C)`	Base-collector depletion charge.
`Qepi (C)`	Epilayer diffusion charge.
`Qb1b2 (C)`	AC current crowding charge.
`Qtex (C)`	Extrinsic base-collector depletion charge.
`XQtex (C)`	Extrinsic base-collector depletion charge.
`Qex (C)`	Extrinsic base-collector diffusion charge.
`XQex (C)`	Extrinsic base-collector diffusion charge.
`gx (1/Ω)`	Forward transconductance.
`gy (1/Ω)`	Reverse transconductance.
`gz (1/Ω)`	Reverse transconductance.
`Sgpi (1/Ω)`	Conductance sidewall b-e junction.
`gpix (1/Ω)`	Conductance floor b-e junction.
`gpiy (1/Ω)`	Early effect on recombination base current.
`gpiz (1/Ω)`	Early effect on recombination base current.

© 2023 Cadence Design Systems, Inc.

gmux (1/Ω)	Early effect on avalanche current limiting.
gmuy (1/Ω)	Conductance of avalanche current.
gmuz (1/Ω)	Conductance of avalanche current.
gmuex (1/Ω)	Conductance extrinsic b-c junction.
Xgmuex (1/Ω)	Conductance extrinsic b-c junction.
grcvy (1/Ω)	Conductance of the epilayer current.
grcvz (1/Ω)	Conductance of the epilayer current.
Rbv (Ω)	Base resistance.
grbvx (1/Ω)	Early-effect on base resistance.
grbvy (1/Ω)	Early-effect on base resistance.
grbvz (1/Ω)	Early-effect on base resistance:.
RE (Ω)	Emitter resistance.
RBC (Ω)	Constant part of the base resistance.
RCC (Ω)	Collector contact resistance.
RCBLX (Ω)	Resistance of collector buried layer under the extrinsic transistor.
RCBLI (Ω)	Resistance of collector buried layer under the Intrinsic transistor.
SCbe (F)	Capacitance sidewall b-e junction.
Cbex (F)	Capacitance floor b-e junction.
Cbey (F)	Early effect on b-e diffusion charge.
Cbez (F)	Early effect on b-e diffusion charge.
Cbcx (F)	Early effect on b-c diffusion charge.
Cbcy (F)	Capacitance floor b-c junction.
Cbcz (F)	Capacitance floor b-c junction.
Cbcex (F)	Capacitance extrinsic b-c junction.
XCbcex (F)	Capacitance extrinsic b-c junction.
Cb1b2 (F)	Capacitance AC current crowding.
Cb1b2x (F)	Cross-capacitance AC current crowding.

© 2023 Cadence Design Systems, Inc.

Cb1b2y (F)	Cross-capacitance of the AC current crowding.
Cb1b2z (F)	Cross-capacitance of the AC current crowding.
gm (1/Ω)	Transconductance.
beta	Current amplification.
gout (1/Ω)	Output conductance.
gmu (1/Ω)	Feedback transconductance.
RB (Ω)	Base resistance.
Cbe (F)	Base-emitter capacitance.
Cbc (F)	Base-collector capacitance.
fT (Hz)	Good approximation for cut-off frequency.
Iqs (A)	Current at onset of quasi-saturation.
XiWepi (M)	Thickness of injection layer.
Vb2c2star (V)	Physical value of internal base-collector bias.
Pdiss (W)	Dissipation.
TK (K)	Actual temperature.
pwr (W)	Power.

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd504t)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500t)

© 2023 Cadence Design Systems, Inc.

Compact Bipolar-Transistor Model (bjtd3500t)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /vols/mmsimP4_t1b_006/ws/ling/ling_2110_isr3_mif/spectre_dev/tools.lnx86/cmi/lib/64bit/5.0.doc/libphilips_sh.so

Instance Syntax

```
Name  c  b  e  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=fwd`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `sat`, `rev`, and `fwd`.
`m=1`	Alias of mult.
`area=1`	Multiplication factor for bjt devices.

Model Syntax

```
model modelName bjtd3500t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=3.5e+03`	Bipolar Level.
`paramchk=0`	Level of clip warning info.
`mexlev=2`	Flag for ELDO model.
`tref=25 deg. C`	Reference temperature.
`dta=0 K`	Difference between the local ambient and global ambient temperature.
`exmod=1`	Flag for extended modelling of reverse current gain.
`exphi=1`	Flag for the distributed high-frequency effects in transient.
`exavl=0`	Flag for extended modelling of avalanche currents.
`is=2.2e-17 A`	Collector-emitter saturation current.
`ik=0.1 A`	Collector-emitter high injection knee current.
`ver=2.5 V`	Reverse Early voltage.
`vef=44 V`	Forward Early voltage.
`bf=215`	Ideal forward current gain.
`ibf=2.7e-15 A`	Saturation current of the non-ideal forward base current.
`mlf=2`	Non ideality factor of the non-ideal forward base current.
`mhf=1`	Non ideality factor of the non-ideal forward base current.
`mlr=2`	Non ideality factor of the non-ideal reverse base current.
`mhr=1`	Non ideality factor of the ideal reverse base current.
`mf=1`	Non ideality factor of main current.
`xibi=0`	Part of ideal base current that belongs to the sidewall.
`izeb=0 A`	Pre-factor of emitter-base Zener tunneling current.
`nzeb=22`	Coefficient of emitter-base Zener tunneling current.
`bri=7`	Ideal reverse current gain.

© 2023 Cadence Design Systems, Inc.

`ibr=1e-15 A`	Saturation current of the non-ideal reverse base current.
`vlr=0.2 V`	Cross-over voltage of the non-ideal reverse base current.
`xext=0.63`	Part of Iex, Qtex, Qex and Isub that depends on Vbc3(Vbc3) instead of Vb1c4(Vb1c4).
`wavl=1.1e-06 m`	Epilayer thickness used in weak-avalanche model.
`vavl=3 V`	Voltage determining curvature of avalanche current.
`sfh=0.3`	Current spreading factor of avalanche model (when EXAVL=1).
`re=5 Ω`	Emitter resistance.
`rbc=23 Ω`	Constant part of the base resistance.
`rbv=18 Ω`	Zero-bias value of the variable part of the base resistance.
`rcc=12 Ω`	Collector contact resistance.
`rcblx=0`	Resistance of collector buried layer under the extrinsic transistor.
`rcbli=0`	Resistance of collector buried layer under the Intrinsic transistor.
`rcv=150 Ω`	Resistance of the un-modulated epilayer.
`scrcv=1.25e+03 Ω`	Space charge resistance of the epilayer.
`ihc=0.004 A`	Critical current for velocity saturation in the epilayer.
`axi=0.3`	Smoothness parameter for the onset of quasi-saturation.
`cje=7.3e-14 F`	Zero-bias emitter-base depletion capacitance.
`vde=0.95 V`	Emitter-base diffusion voltage.
`pe=0.4`	Emitter-base grading coefficient.
`xcje=0.4`	Fraction of the emitter-base depletion capacitance that belongs to the sidewall.
`cbeo=0`	Emitter-base overlap capacitance.
`cjc=7.8e-14 F`	Zero-bias collector-base depletion capacitance.

© 2023 Cadence Design Systems, Inc.

`vdc=0.68 V`	Collector-base diffusion voltage.
`pc=0.5`	Collector-base grading coefficient.
`xp=0.35`	Constant part of Cjc.
`mc=0.5`	Coefficient for the current modulation of the collector-base depletion capacitance.
`xcjc=0.032`	Fraction of the collector-base depletion capacitance under the emitter.
`cbco=0`	Collector-base overlap capacitance.
`vos=0.04 V`	Voltage describing overshoot.
`isat=0.067 A`	Saturation current.
`repi=6 Ω`	Ohmic resistance epilayer.
`rdmin=0`	Minimum relative collector doping.
`sbjn=0.1`	Smoothness parameter Qtc model.
`sbeb=0.1`	Smoothness parameter Qtc model.
`etavdr=0.23`	Slope-parameter of Vdrift at high electric field.
`nvdr=4`	Power describing saturation behavior of Qtc.
`alfaw=0`	Smooth switch for reachthrough modelling.
`sw=0.1`	Smoothness parameter for reachthrough modelling.
`mtau=1`	Non-ideality factor of the emitter stored charge.
`taue=2e-12 s`	Minimum transit time of stored emitter charge.
`taub=4.2e-12 s`	Transit time of stored base charge.
`tepi=4.1e-11 s`	Transit time of stored epilayer charge.
`taur=5.2e-10 s`	Transit time of reverse extrinsic base charge.
`deg=0 eV`	Bandgap difference over the base.
`xrec=0`	Pre-factor of the recombination part of Ib1.
`aqbo=0.3`	Temperature coefficient of the zero-bias base charge.
`ae=0`	Temperature coefficient of the resistivity of the emitter.
`ab=1`	Temperature coefficient of the resistivity of the base.
`dais=0`	Parameter for fine tuning of temperature dependence of collector-emitter saturation current.

© 2023 Cadence Design Systems, Inc.

`aepi=2.5`	Temperature coefficient of the resistivity of the epilayer.
`aex=0.62`	Temperature coefficient of the resistivity of the extrinsic base.
`ac=2`	Temperature coefficient of the resistivity of the collector contact.
`acbl=2`	Temperature coefficient of the resistivity of the collector buried layer.
`aisat=-0.37`	Temperature coefficient of the saturation current.
`dvgbf=0.05 V`	Bandgap voltage difference of forward current gain.
`dvgbr=0.045 V`	Bandgap voltage difference of reverse current gain.
`vgb=1.17 V`	Bandgap voltage of the base.
`vgc=1.18 V`	Bandgap voltage of the collector.
`vgj=1.15 V`	Bandgap voltage recombination emitter-base junction.
`vgzeb=1.15 V`	Band-gap at reference temperature relevant to the Zener effect in the emitter-base junction.
`avgeb=0.000473 V/K`	Temperature scaling coefficient of emitter-base Zener tunneling current.
`tvgeb=636 K`	Temperature scaling coefficient of emitter-base Zener tunneling current.
`dvgte=0.05 V`	Bandgap voltage difference of emitter stored charge.
`af=2`	Exponent of the Flicker-noise.
`kf=2e-11`	Flicker-noise coefficient of the ideal base current.
`kfn=2e-11`	Flicker-noise coefficient of the non-ideal base current.
`kavl=0`	Switch for white noise contribution due to avalanche.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`dtmax=1e+03 K`	Maximal dynamic temperature increase.
`exrth=0`	Flag for extended modelling of non-linear thermal resistance.

© 2023 Cadence Design Systems, Inc.

`type=npn`	Transistor gender. Possible values are `npn`, `pnp`, `npnv`, `pnpv`, `npnl`, and `pnpl`.
`imax=1000 A`	Explosion current.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.
`compatible=spectre`	
	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`Ic (A)`	External DC collector current.
`Ib (A)`	External DC base current.
`Ie (A)`	External DC emitter current.
`BetaDC`	External DC current gain Ic/Ib.
`Vbe (V)`	External base-emitter bias.
`Vbc (V)`	External base-collector bias.
`Vce (V)`	External collector-emitter bias.
`Vb2e1 (V)`	Internal base-emitter bias.
`Vb2c2 (V)`	Internal base-collector bias.
`Vb2c1 (V)`	Internal base-collector bias including epilayer.
`Vb1c1 (V)`	External base-collector bias without contact resistances.
`Vb1c4 (V)`	External base-collector bias with contact resistance RCBLI.
`Vc3c4 (V)`	External collector-collector bias over contact resistance RCBLX.
`Vc4c1 (V)`	Bias over intrinsic buried layer.
`Ve1e (V)`	Bias over emitter resistance.
`In (A)`	Main current.
`Ic1c2 (A)`	Epilayer current.
`Ib1b2 (A)`	Pinched-base current.
`Ib1 (A)`	Ideal forward base current.
`SIb1 (A)`	Ideal side-wall base current.
`Izteb (A)`	Zener tunneling current in the emitter base junction.

© 2023 Cadence Design Systems, Inc.

`Ib2 (A)`	Non-ideal forward base current.
`Ib3 (A)`	Non-ideal reverse base current.
`Iex (A)`	Extrinsic reverse base current.
`XIex (A)`	Extrinsic reverse base current.
`Iavl (A)`	Avalanche current.
`IRE (A)`	Current through emitter resistance.
`IRBC (A)`	Current through constant base resistance.
`IRCC (A)`	Current through collector contact resistance.
`IRCBLX (A)`	Current through extrinsic collector resistance.
`IRCBLI (A)`	Current through intrinsic collector resistance.
`Qe (C)`	Emitter charge or emitter neutral charge.
`Qte (C)`	Base-emitter depletion charge.
`SQte (C)`	Sidewall base-emitter depletion charge.
`Qbe (C)`	Base-emitter diffusion charge.
`Qbc (C)`	Base-collector diffusion charge.
`Qtc (C)`	Base-collector depletion charge.
`Qepi (C)`	Epilayer diffusion charge.
`Qb1b2 (C)`	AC current crowding charge.
`Qtex (C)`	Extrinsic base-collector depletion charge.
`XQtex (C)`	Extrinsic base-collector depletion charge.
`Qex (C)`	Extrinsic base-collector diffusion charge.
`XQex (C)`	Extrinsic base-collector diffusion charge.
`gx (1/Ω)`	Forward transconductance.
`gy (1/Ω)`	Reverse transconductance.
`gz (1/Ω)`	Reverse transconductance.
`Sgpi (1/Ω)`	Conductance sidewall b-e junction.
`gpix (1/Ω)`	Conductance floor b-e junction.
`gpiy (1/Ω)`	Early effect on recombination base current.
`gpiz (1/Ω)`	Early effect on recombination base current.

© 2023 Cadence Design Systems, Inc.

gmux (1/Ω)	Early effect on avalanche current limiting.
gmuy (1/Ω)	Conductance of avalanche current.
gmuz (1/Ω)	Conductance of avalanche current.
gmuex (1/Ω)	Conductance extrinsic b-c junction.
Xgmuex (1/Ω)	Conductance extrinsic b-c junction.
grcvy (1/Ω)	Conductance of the epilayer current.
grcvz (1/Ω)	Conductance of the epilayer current.
Rbv (Ω)	Base resistance.
grbvx (1/Ω)	Early-effect on base resistance.
grbvy (1/Ω)	Early-effect on base resistance.
grbvz (1/Ω)	Early-effect on base resistance:.
RE (Ω)	Emitter resistance.
RBC (Ω)	Constant part of the base resistance.
RCC (Ω)	Collector contact resistance.
RCBLX (Ω)	Resistance of collector buried layer under the extrinsic transistor.
RCBLI (Ω)	Resistance of collector buried layer under the Intrinsic transistor.
SCbe (F)	Capacitance sidewall b-e junction.
Cbex (F)	Capacitance floor b-e junction.
Cbey (F)	Early effect on b-e diffusion charge.
Cbez (F)	Early effect on b-e diffusion charge.
Cbcx (F)	Early effect on b-c diffusion charge.
Cbcy (F)	Capacitance floor b-c junction.
Cbcz (F)	Capacitance floor b-c junction.
Cbcex (F)	Capacitance extrinsic b-c junction.
XCbcex (F)	Capacitance extrinsic b-c junction.
Cb1b2 (F)	Capacitance of the AC current crowding.
Cb1b2x (F)	Cross-capacitance of the AC current crowding.

© 2023 Cadence Design Systems, Inc.

`Cb1b2y (F)`	Cross-capacitance of the AC current crowding.
`Cb1b2z (F)`	Cross-capacitance of the AC current crowding.
`gm (1/Ω)`	Transconductance.
`beta`	Current amplification.
`gout (1/Ω)`	Output conductance.
`gmu (1/Ω)`	Feedback transconductance.
`RB (Ω)`	Base resistance.
`Cbe (F)`	Base-emitter capacitance.
`Cbc (F)`	Base-collector capacitance.
`fT (Hz)`	Good approximation for cut-off frequency.
`Iqs (A)`	Current at onset of quasi-saturation.
`XiWepi (M)`	Thickness of injection layer.
`Vb2c2star (V)`	Physical value of internal base-collector bias.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual temperature.
`pwr (W)`	Power.

Related Topics

Philips Models

Compact Bipolar-Transistor Model (bjt504)

Compact Bipolar-Transistor Model (bjt505)

Compact Bipolar-Transistor Model (bjt505t)

Compact Bipolar-Transistor Model (bjtd504)

Compact Bipolar-Transistor Model (bjtd504t)

Compact Bipolar-Transistor Model (bjtd505t)

Compact Bipolar-Transistor Model (bjtd3500)

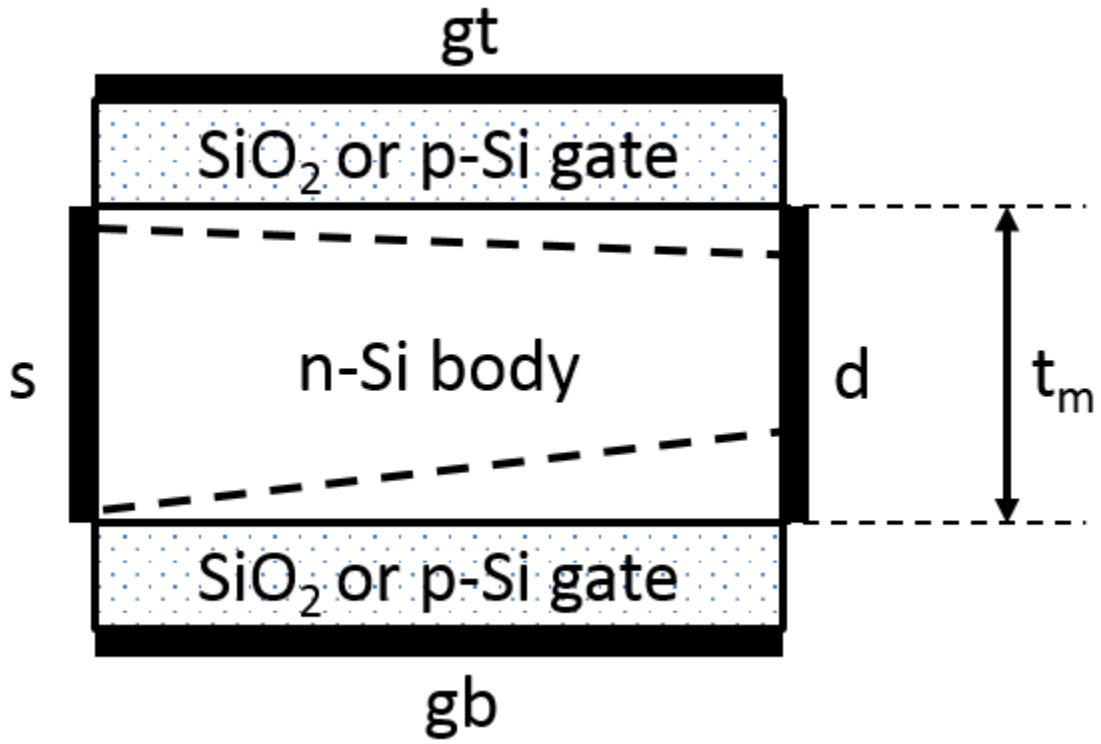
© 2023 Cadence Design Systems, Inc.

JFETIDG Model (jfetidg)

JFETIDG is a compact model for four-terminal (that is, independent dual-gate) JFETs that is applicable to all regions of operation. It can also be applied to:

- resistors (diffused or polysilicon) with a metal shield
- the drift region of LDMOS transistors
- the collector resistance of four-terminal vertical BJTs
- junctionless MOS transistors

A cross-section of an n-channel device that can be modeled by JFETIDG is shown below (the thicker dashed lines represent the edges of the depletion regions in the channel region, from both the bottom and top gates; the metallurgical thickness of the channel is tm).



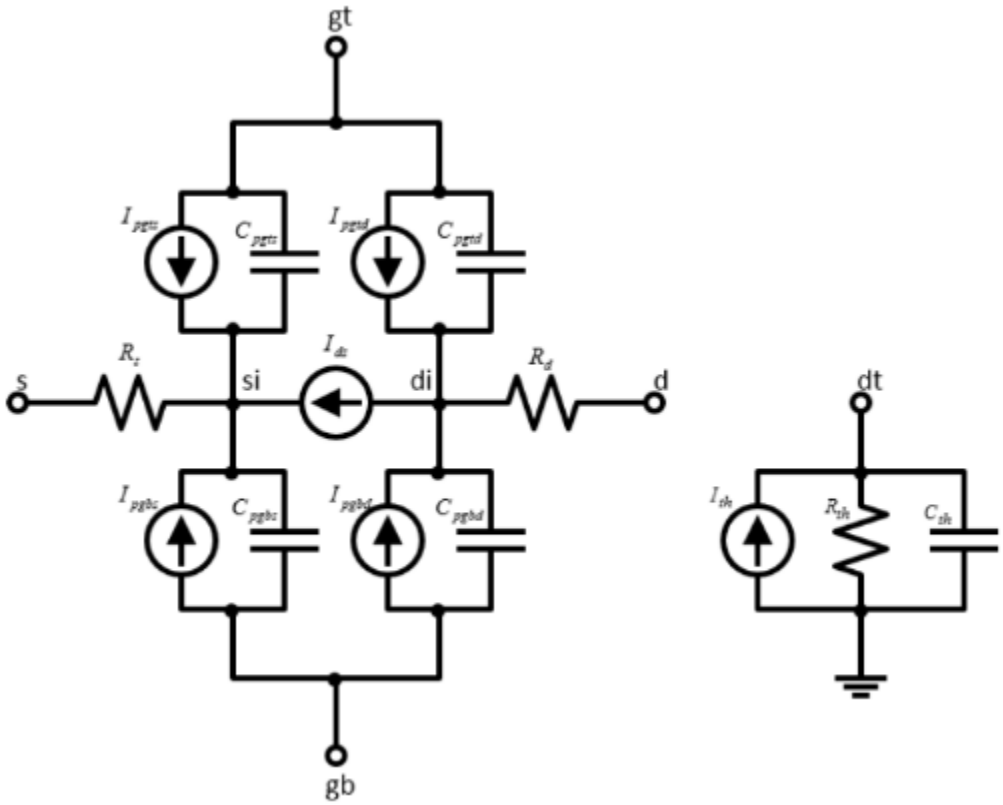
JFETIDG uses a unified, physical formulation for depletion pinching of the conducting channel that is applicable to both pn-junction gates and MOS gates, and independent of gate type (apart from how the JFETIDG model parameters are computed from physical parameters). JFETIDG uses an exact solution for depletion pinching modulation of the channel current Ids, which is more accurate than linearizing with respect to the mid-point-potential. JFETIDG also models:

© 2023 Cadence Design Systems, Inc.

- self-heating
- velocity saturation (inherited from the r3 model)
- channel length modulation (CLM)
- drain-induced barrier lowering (DIBL)
- impact ionization (i.e. weak avalanche)
- mobility modulation, by both bottom and top gate biases
- parasitic pn-junction leakage current
- parasitic pn-junction breakdown current
- depletion and diffusion capacitance for pn-junction gates
- fixed capacitance for MOS gates
- selectable local (single geometry) and global (geometry dependent) models
- channel conductance and depletion modulation parameters can either be specified directly or calculated from physical doping and layer thickness values
- temperature dependence
- noise, including from parasitic pn-junction currents
- statistical variations

© 2023 Cadence Design Systems, Inc.

The large-signal equivalent circuit for JFETIDG is shown below.



The power generated by the electrical part of JFETIDG (the left side of the network above), I_{th}, drives the thermal part of JFETIDG (the right side of the network above), and the behavior of the electrical part depends on the local temperature rise, `Temp(dt)`, generated by the thermal part. The electrical and thermal parts are solved self-consistently. The parasitic capacitances include both linear components (for MOS gates) and non-linear components (for pn-junction gates); The parasitic currents include pn-junction, breakdown, and impact ionization components; these are only applicable to pn-junction gates so are turned off for MOS gates.

Terminology and Notation

non-pinch-off	operation when neither end of a device is pinched off (analogous to MOSFET strong inversion non-saturation)
drain pinch-off	operation when one end of a device is pinched off (analogous to MOSFET strong inversion saturation)

© 2023 Cadence Design Systems, Inc.

source pinch-off	operation when both ends of a device are pinched off (analogous to MOSFET weak inversion)
`Vds`	voltage across the intrinsic body portion of the device `V(di)-V(si)`
`Ids`	current through the intrinsic body portion of the device (see equivalent circuit below)
`Vgbs`	bottom-gate to intrinsic source voltage `V(gb)-V(si)`
`Vgbd`	bottom-gate to intrinsic drain voltage `V(gb)-V(di)`
`Vgts`	top-gate to intrinsic source voltage `V(gt)-V(si)`
`Vgtd`	top-gate to intrinsic drain voltage `V(gt)-V(di)`
`[sd]`	applies for both source and drain
`[bt]`	applies for both bottom and top gate
`[ap]`	applies for both area and perimeter components
`[2]`	also applies to an optional second perimeter component

Parameters and nodes are set in Courier New font. `k` is Boltzmann's constant, `q` is the magnitude of the electronic charge, and `ni` is the intrinsic carrier concentration. The thermal voltage is $\Phi t=kT/q$ where `T` is the device temperature in K. εSi and εox are the permittivities of silicon and silicon dioxide, respectively.

For convenience, and to be able to help debug circuit problems and understand what is the dominant source of nonlinearity, the physical effects can be turned off individually.

- setting `swlin` to 1 turns off all nonlinearities
- setting `swet` to 0 turns off self-heating
- setting the thermal conductance `gth` to 0 when the local termperature rise port `dt` is not connected turns off self-heating
- setting `ecrit` to be >=10^9 V/m turns off modeling of velocity saturation (the breakdown field for silicon is about 3×10^7 V/m)
- setting `dfbfac` to 0 turns off modeling of depletion pinching by the bottom gate
- setting `dftfac` to 0 turns off modeling of depletion pinching by the top gate

Any combination of sources of nonlinearity can be switched off by appropriate specification of these parameters.

© 2023 Cadence Design Systems, Inc.

Model Version

SPECTRE supports `JFETIDG` model version 1.0.0.

Component Statements

This device is supported within altergroups.

Instance Syntax

```
Name ( d gb s gt [dt] ) ModelName <parameter=value> ...
```

Instance Parameters

`w=1e-06 m`	Design width of JFET body.
`l=1e-06 m`	Design length of JFET body.
`wd=0 m`	Dogbone width (total; not per side).
`asb=0 m^2`	Area of source to bottom gate.
`ast=0 m^2`	Area of source to top gate.
`psb=0 m`	Perimeter of source to bottom gate.
`psb2=0 m`	Perimeter of source to bottom gate (2nd component).
`pst=0 m`	Perimeter of source to top gate.
`pst2=0 m`	Perimeter of source to top gate (2nd component).
`cs=0`	Number of contacts at source end.
`adb=0 m^2`	Area of drain to bottom gate.
`adt=0 m^2`	Area of drain to top gate.
`pdb=0 m`	Perimeter of drain to bottom gate.
`pdb2=0 m`	Perimeter of drain to bottom gate (2nd component).
`pdt=0 m`	Perimeter of drain to top gate.
`pdt2=0 m`	Perimeter of drain to top gate (2nd component).
`cd=0`	Number of contacts at drain end.

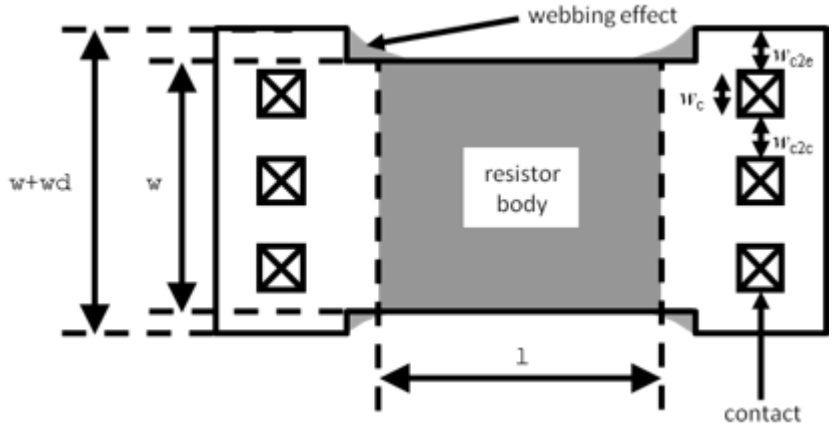
© 2023 Cadence Design Systems, Inc.

`trise=0 degC`	Local temperature delta to ambient (before self-heating).
`dta=0 degC`	Local temperature delta to ambient (before self-heating).
`dtemp=0 degC`	Local temperature delta to ambient (before self-heating).
`nsmm_rsh=0`	Number of standard deviations of local variation for rsh.
`nsmm_w=0`	Number of standard deviations of local variation for w.
`nsmm_l=0`	Number of standard deviations of local variation for l.
`mult=1`	Multiplicity factor.
`swnoise=1`	Switch to include noise: 0=no and 1=yes.
`swet=1`	Switch to include self-heating: 0=no and 1=yes.
`swlin=0`	Switch to force linearity: 0=no and 1=yes.
`swmman`	Switch to enable mismatch analysis: 0=no and 1=yes.
`m=1`	Alias of mult.

The switch parameters can also be specified as model parameters, and a value specified on an instance line overrides a value specified on a model card.

The following figure shows how the instance parameters should be determined for a typical JFET layout.

Note: The end region dogbone may be asymmetric between the two sides.



The total width of the source end region is:

© 2023 Cadence Design Systems, Inc.

$$w + wd = cs \cdot w_c + (cs - 1)w_{c2c} + 2w_{c2e}$$

where the contact width, contact spacing, and contact-to-edge distances, `wc`, `wc2c`, and `wc2e`, respectively, are shown in the layout.

If `cs` is zero (which happens for non-end sections of a multi-section model) then `as[bt]` and `ps[bt]` should be calculated as half of the area and length direction perimeter, respectively, of the body of the JFET (that is, `0.5·w·l` and `l`, respectivey). If `cs` is greater than zero then the area and (non-body adjacent) perimeter of the left end region should be added to these values. Similarly for `ad[bt]` and `pd[bt]`.

Model Syntax

```
model ModelName jfetidg <parameter=value> ...
```

Model Parameters

The naming convention for parameters follows the PSP style. Global model parameters append `o`, `l`, `w`, `lw`, and so on, to the name of the associated local geometry model parameter.

`level=1`	Model level.
`paramchk=0`	Model parameter checking selector.
`version=1`	Model version.
`subversion=0`	Model subversion.
`revision=2`	Model revision.
`tmin=100 degC`	Minimum ambient temperature.
`tmax=500 degC`	Maximum ambient temperature.
`gmin=1e-12 S`	Minimum parasitic conductance.
`imax=1 A`	Current at which to linearize diode currents.
`scale=1`	Scale factor for instance geometries.
`shrink=0 %`	Shrink percentage for instance geometries.
`rthresh=0.001 Ω`	Threshold to switch end resistance to V=I*R form.
`type=n`	JFET type: +1=n-body and -1=p-body. Possible values are `n` and `p`.

© 2023 Cadence Design Systems, Inc.

`swbgmos=0`	Switch to indicate bottom gate type: 0=pn-junction and 1=mos.
`swtgmos=0`	Switch to indicate top gate type: 0=pn-junction and 1=mos.
`swgeo=1`	Switch for geometry modeling: 0=local and 1=global.
`swgdep=1`	Switch for geometry mapping basis: 0=drawn and 1=effective.
`tnom=27 degC`	Nominal (reference) temperature.
`lmin=0.0 m`	Minimum allowed drawn length.
`lmax=9e+09 m`	Maximum allowed drawn length.
`wmin=0.0 m`	Minimum allowed drawn width.
`wmax=9.9e+09 m`	Maximum allowed drawn width.
`jmax=1e+08 A/m`	Maximum current density.
`vmax=9.9e09 V`	Maximum drain or source voltage w.r.t. either gate.
`tminclip=(-100) degC`	Clip minimum temperature.
`tmaxclip=800 degC`	Clip maximum temperature.
`grpo=1e-12`	Minimum body conductance in pinch-off (ratio w.r.t. Vc=0).
`xw=0 m`	Width offset (total).
`nwxw=0 m`	Narrow width offset correction coefficient.
`wexw=0 m`	Webbing effect width offset correction coefficient (for dogboned devices).
`fdrwo=1e-06 m`	Finite doping width offset reference width.
`fdxwo=0 m`	Finite doping width offset width value for wide devices.
`xl=0 m`	Length offset (total).
`xlw=0 m`	Width dependence of length offset.
`dxlsat=0 m`	Additional length offset for velocity saturation calculation.
`tm=5e-07 m`	Channel thickness (metallurgical).
`nc=1e+23 /m^3`	Channel doping concentration.

© 2023 Cadence Design Systems, Inc.

`nb=1e+22 /m^3`	Bottom-gate doping concentration.
`toxb=4e-07 m`	Bottom-gate oxide thickness.
`vfbb=0 V`	Bottom-gate flatband voltage.
`nt=1e+26 /m^3`	Top-gate doping concentration.
`toxt=4e-07 m`	Top-gate xide thickness.
`vfbt=0 V`	Top-gate flatband voltage.
`dfb=0.01 /V^0.5`	Bottom-gate depletion factor (overrides calculation if specified).
`dfbo=0.01 /V^0.5`	`dfb` Geometry-independent part.
`dfbl=0`	`dfb 1/l` coefficient.
`dfble=1`	`dfb 1/l` exponent.
`dfbw=0`	`dfb 1/w` coefficient.
`dfbwe=1`	`dfb 1/w` exponent.
`dfblw=0`	`dfb 1/(l*w)` coefficient.
`dfbfac=1`	`dfb` adjustment coefficient.
`psirb=2 V`	Bottom-gate depletion potential (overrides calculation if specified).
`psirbo=2 V`	`psirb` Geometry-independent part.
`psirbl=0`	`psirb 1/l` coefficient.
`psirble=1`	`psirb 1/l` exponent.
`psirbw=0`	`psirb 1/w` coefficient.
`psirbwe=1`	`psirb 1/w` exponent.
`psirblw=0`	`psirb 1/(l*w)` coefficient.
`psirbfac=1`	`psirb` adjustment coefficient.
`dft=0.01 /V^0.5`	Top-gate depletion factor (overrides calculation if specified).
`dfto=0.01 /V^0.5`	`dft` Geometry-independent part.
`dftl=0.0`	`dft 1/l` coefficient.
`dftle=1.0`	`dft 1/l` exponent.
`dftw=0.0`	`dft 1/w` coefficient.

© 2023 Cadence Design Systems, Inc.

`dftwe=1.0`	`dft 1/w` exponent.
`dftlw=0.0`	`dft 1/(l*w)` coefficient.
`dftfac=1.0`	`dft` adjustment coefficient.
`psirt=2.0 V`	Top-gate depletion potential (overrides calculation if specified).
`psirto=2.0 V`	`psirt` Geometry-independent part.
`psirtl=0.0`	`psirt 1/l` coefficient.
`psirtle=1.0`	`psirt 1/l` exponent.
`psirtw=0.0`	`psirt 1/w` coefficient.
`psirtwe=1.0`	`psirt 1/w` exponent.
`psirtlw=0.0`	`psirt 1/(l*w)` coefficient.
`psirtfac=1.0`	`psirt` adjustment coefficient.
`mu0=0.05 m^2/V/s`	Low-field mobility
`r0=100 Ohm`	Zero-bias resistance.
`rsh0=100 Ohm/sq`	Zero-bias sheet resistance (overrides calculation if specified).
`rzd=100 Ohm`	Zero-depletion resistance.
`rshzd=100 Ohm/sq`	Zero-depletion sheet resistance (overrides calculation if specified).
`rcs=0 Ohm`	Source contact resistance.
`rcd=0 Ohm`	Drain contact resistance.
`rc=0 Ohm`	Resistance per contact.
`rcw=0 Ohm`	Width adjustment for contact resistance.
`diblb=0`	Bottom-gate `dibl`.
`diblbl=0`	`diblb l` dependence coefficient.
`diblt=0`	Top-gate `dibl`.
`dibltl=0`	`diblt l` dependence coefficient.
`diblle=1`	`dibl l` dependence exponent.
`diblv=0.1 V`	`dibl` voltage offset.
`dible=0.5`	`dibl` voltage exponent.

© 2023 Cadence Design Systems, Inc.

`clm1=0`	`clm` linear component.
`clm1l=0`	`clm1 l` dependence coefficient.
`clm1le=1`	`clm1 l` dependence exponent.
`clm1c=0 /V`	`clm1 V(gx)` dependence coefficient.
`clm2=0`	`clm` nonlinear component.
`clm2l=0`	`clm2 l` dependence coefficient.
`clm2le=1`	`clm2 l` dependence exponent.
`clm2v=0.1 V`	`clm2` voltage offset.
`clm2e=0.5`	`clm2` voltage exponent.
`ats=0.0 V`	Saturation smoothing parameter.
`atso=0 V`	`ats` Geometry-independent part.
`atsl=0 V`	`ats 1/l` coefficient.
`axs=0`	Second saturation smoothing parameter.
`axso=0`	`axs` Geometry-independent part.
`axsl=0`	`axs 1/l` coefficient.
`nspo=1`	Slope parameter under source pinch-off.
`nspoo=1`	`nspo` Geometry-independent part.
`nspol=0`	`nspo 1/l` coefficient.
`nspole=1`	`nspo 1/l` exponent.
`nspow=0`	`nspo 1/w` coefficient.
`nspowe=1`	`nspo 1/w` exponent.
`nspolw=0`	`nspo 1/(l*w)` coefficient.
`alphab=0 /V`	Bottom-gate impact ionization current prefactor.
`alphabo=0 /V`	`alphab` Geometry-independent part.
`alphabl=0 /V`	`alphab 1/l` coefficient.
`alphat=0 /V`	Top-gate impact ionization current prefactor.
`alphato=0 /V`	`alphat` Geometry-independent part.
`alphatl=0 /V`	`alphat 1/l` coefficient.
`beta=10 V`	Impact ionization current exponent for both gates.

© 2023 Cadence Design Systems, Inc.

`mumb=0 /V`	Bottom-gate mobility modulation coefficient.
`mumboff=0 V`	Bottom-gate mobility modulation voltage offset.
`mumbs=1`	Bottom-gate mobility modulation smoothing parameter.
`mumbe=1`	Bottom-gate mobility modulation exponent.
`mumbo=0 /V`	`mumb` Geometry-independent part.
`mumbl=0`	`mumb 1/l` coefficient.
`mumbw=0`	`mumb 1/w` coefficient.
`mumblw=0`	`mumb 1/(l*w)` coefficient.
`mumt=0 /V`	Top-gate mobility modulation coefficient.
`mumtoff=0 V`	Top-gate mobility modulation voltage offset.
`mumts=1`	Top-gate mobility modulation smoothing parameter.
`mumte=1`	Top-gate mobility modulation exponent.
`mumto=0 /V`	`mumt` Geometry-independent part.
`mumtl=0`	`mumt 1/l` coefficient.
`mumtw=0`	`mumt 1/w` coefficient.
`mumtlw=0`	`mumt 1/(l*w)` coefficient.
`mumii1=0 /V^2`	Linear impact ionization mobility modulation coefficient.
`mumii2=0 /V^4`	Quadratic impact ionization mobility modulation coefficient.
`vcrit=4 V`	Velocity saturation critical voltage.
`ecrit=4e+06 V/m`	Velocity saturation critical field.
`vcorn=0.4 V`	Velocity saturation corner voltage.
`ecorn=4e+05 V/m`	Velocity saturation corner field.
`du=0.02`	Mobility reduction at ecorn.
`voffspo=0`	Source pinchoff offset (number of `nspo*phi_t`).
`moffspo=1`	Source pinchoff smoothing factor.
`gth=0 W/K`	Thermal conductance.
`gtho=0 W/K`	`gth` Geometry-independent part.
`gthp=0 W/K/m`	`gth` perimeter component.

© 2023 Cadence Design Systems, Inc.

`gtha=0 W/K/m`^{2}	`gth` area component.
`gthc=0 W/K`	`gth` contact component.
`cth=0 s W/K`	Thermal capacitance.
`ctho=0 s W/K`	`cth` Geometry-independent part.
`cthp=0 s W/K/m`	`cth` perimeter component.
`ctha=0 s W/K/m`^{2}	`cth` area component.
`cthc=0 s W/K`	cth contact component.
`fc=0.9`	Ddepletion capacitance linearization factor.
`isab=0 A/m`^{2}	Bottom-gate diode saturation current per unit area.
`nab=1`	Bottom-gate ideality factor for `isa`.
`cab=0 F/m`^{2}	Bottom-gate fixed capacitance per unit area.
`cjab=0 F/m`^{2}	Bottom-gate depletion capacitance per unit area.
`pab=0.75 V`	Bottom-gate built-in potential for cja.
`mab=0.33`	Bottom-gate grading coefficient for cja.
`ajab=-0.5 V`	Bottom-gate smoothing parameter for cja.
`ispb=0 A/m`	Bottom-gate diode saturation current per unit perimeter.
`npb=1`	Bottom-gate ideality factor for isp.
`cpb=0 F/m`	Bottom-gate fixed capacitance per unit perimeter.
`cpb2=0 F/m`	Bottom-gate fixed capacitance per unit perimeter (2nd component).
`cjpb=0 F/m`	Bottom-gate depletion capacitance per unit perimeter.
`ppb=0.75 V`	Bottom-gate built-in potential for cjp.
`mpb=0.33`	Bottom-gate grading coefficient for cjp.
`ajpb=-0.5 V`	Bottom-gate smoothing parameter for cjp.
`ttb=0 s`	Bottom-gate transit time for diffusion charge.
`vbvb=0 V`	Bottom-gate breakdown voltage.
`nbvb=1`	Bottom-gate ideality factor for breakdown current.
`isat=0 A/m`^{2}	Top-gate diode saturation current per unit area.
`nat=1`	Top-gate ideality factor for isa.

© 2023 Cadence Design Systems, Inc.

`cat=0 F/m`^{2}	Top-gate fixed capacitance per unit area.
`cjat=0 F/m`^{2}	Top-gate depletion capacitance per unit area.
`pat=0.75 V`	Top-gate built-in potential for cja.
`mat=0.33`	Top-gate grading coefficient for cja.
`ajat=-0.5 V`	Top-gate smoothing parameter for cja.
`ispt=0 A/m`	Top-gate diode saturation current per unit perimeter.
`npt=1`	Top-gate ideality factor for isp.
`cpt=0 F/m`	Top-gate fixed capacitance per unit perimeter.
`cpt2=0 F/m`	Top-gate fixed capacitance per unit perimeter (2nd component).
`cjpt=0 F/m`	Top-gate depletion capacitance per unit perimeter.
`ppt=0.75 V`	Top-gate built-in potential for cjp.
`mpt=0.33`	Top-gate grading coefficient for cjp.
`ajpt=-0.5 V`	Top-gate smoothing parameter for cjp.
`ttt=0 s`	Top-gate transit time for diffusion charge.
`vbvt=0 V`	Top-gate breakdown voltage.
`nbvt=1`	Top-gate ideality factor for breakdown current.
`ibv=1e-06 A`	Current at breakdown.
`kfn=0 m`^{2}	Flicker noise coefficient.
`afn=2`	Flicker noise current exponent.
`bfn=1`	Flicker noise 1/f exponent.
`swfngeo=0`	Switch for flicker noise geometry calculation: 0=drawn and 1=effective.
`tc1psirb=0 /K`	`psirb` linear TC.
`tc2psirb=0 /K`^{2}	`psirb` quadratic TC.
`tc1psirt=0 /K`	`psirt` linear TC.
`tc2psirt=0 /K`^{2}	`psirt` quadratic TC.
`tc1=0 /K`	Resistance linear TC.
`tc2=0 /K`^{2}	Resistance quadratic TC.

© 2023 Cadence Design Systems, Inc.

`tc1o=0 /K`	`tc1` Geometry-independent part.
`tc2o=0 /K`^{2}	`tc2` Geometry-independent part.
`tc1w=0 m/K`	`tc1 1/w` coefficient.
`tc2w=0 m/K`^{2}	`tc2 1/w` coefficient.
`tc1l=0 m/K`	`tc1 1/l` coefficient.
`tc2l=0 m/K`^{2}	`tc2 1/l` coefficient.
`tc1lw=0 m`^{2}`/K`	`tc1 1/(l*w)` coefficient.
`tc2lw=0 m`^{2}`/K`^{2}	`tc2 1/(l*w)` coefficient.
`tsl=0 /K`	Slope of resistance change compared to temperature at low temperature.
`tsh=0 /K`	Slope of resistance change compared to temperature at high temperature.
`tsct=100 degC`	Critical temperature where resistance change slope goes from tsl to tsh.
`tssm=10 degC`	Resistance change slope smoothing parameter.
`tslo=0 /K`	`tsl` Geometry-independent part.
`tsho=0 /K`	`tsh` Geometry-independent part.
`tscto=100 degC`	`tsct` Geometry-independent part.
`tssmo=10 degC`	`tssm` Geometry-independent part.
`tslw=0 m/K`	`tsl 1/w` coefficient.
`tshw=0 m/K`	`tsh 1/w` coefficient.
`tsctw=0 m degC`	`tsct 1/w` coefficient.
`tssmw=0 m degC`	`tssm 1/w` coefficient.
`tsll=0 m/K`	`tsl 1/l` coefficient.
`tshl=0 m/K`	`tsh 1/l` coefficient.
`tsctl=0 m degC`	`tsct 1/l` coefficient.
`tssml=0 m degC`	`tssm 1/l` coefficient.
`tsllw=0 m`^{2}`/K`	`tsl 1/(l*w)` coefficient.
`tshlw=0 m`^{2}`/K`	`tsh 1/(l*w)` coefficient.
`tsctlw=0 m`^{2} `degC`	`tsct 1/(l*w)` coefficient.

© 2023 Cadence Design Systems, Inc.

`tssmlw=0 m^2 degC`	`tssm 1/(l*w)` coefficient.
`tc1rc=0 /K`	Contact resistance linear TC.
`tc2rc=0 /K^2`	Contact resistance quadratic TC.
`xbeta=0`	Exponent for impact ionization current exponent temperature dependence.
`tegth=0`	Thermal conductance temperature exponent.
`xvsat=0`	Exponent for saturation velocity temperature dependence.
`xvsato=0`	`xvsat` Geometry-independent part.
`xvsatl=0`	`xvsat 1/l` coefficient.
`xvsatle=1`	`xvsat 1/l` exponent.
`ea=1.12 V`	Activation voltage for diode temperature dependence.
`xis=3`	Exponent for diode temperature dependence.
`tc1vbvb=0 /K`	Breakdown voltage linear TC (bottom gate).
`tc2vbvb=0 /K^2`	Breakdown voltage quadratic TC (bottom gate).
`tc1nbvb=0 /K`	Breakdown ideality factor linear TC (bottom gate).
`tc1vbvt=0 /K`	Breakdown voltage linear TC (top gate).
`tc2vbvt=0 /K^2`	Breakdown voltage quadratic TC (top gate).
`tc1nbvt=0 /K`	Breakdown ideality factor linear TC (top gate).
`tc1kfn=0 /K`	Flicker noise coefficient linear TC.
`nsig_rsh=0`	Number of standard deviations of global variation for `rsh`.
`nsig_w=0`	Number of standard deviations of global variation for `w`.
`nsig_l=0`	Number of standard deviations of global variation for `l`.
`sig_rsh=0 %`	Global variation standard deviation for `rsh` (relative).
`sig_w=0 m`	Global variation standard deviation for `w` (absolute).
`sig_l=0 m`	Global variation standard deviation for `l` (absolute).
`smm_rsh=0 %m`	Local variation standard deviation for `rsh` (relative).
`smm_w=0 m^1.5`	Local variation standard deviation for `w` (absolute).
`smm_l=0 m^1.5`	Local variation standard deviation for `l` (absolute).

© 2023 Cadence Design Systems, Inc.

`swmmgdep=0`	Switch for mismatch geometry calculation: 0=drawn and 1=effective.
`swnoise=1`	Switch to include noise: 0=no and 1=yes.
`swet=1`	Switch to include self-heating: 0=no and 1=yes.
`swlin=0`	Switch to force linearity: 0=no and 1=yes.
`swmman=0`	Switch to enable mismatch analysis: 0=no and 1=yes.
`tref (degC)`	Alias of tnom.
`tr (degC)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating Point Parameters

`jtype`	JFET type: +1=n-body and -1=p-body.
`leff_m (m`	Effective electrical length.
`weff_m (m)`	Effective electrical width.
`rth (K/W)`	Thermal resistance at ambient temperature.
`cth_i (s W/K)`	Thermal capacitance.
`v (V)`	Voltage across JFET.
`ids (A)`	Current through JFET body.
`r_dc (Ω)`	DC resistance (including bias and temperature dependence).

© 2023 Cadence Design Systems, Inc.

`r_ac (Ω)`	AC resistance (including bias and temperature dependence).
`cgbs (F)`	Bottom-gate to source capacitance.
`cgbd (F)`	Bottom-gate to drain capacitance.
`cgts (F)`	Top-gate to source capacitance.
`cgtd (F)`	Top-gate to drain capacitance.
`vsp (V)`	Source voltage difference w.r.t. to pinch-off.
`vdsat (V)`	Drain-source saturation voltage.

Related Topics

Philips Models

Long Channel JFET/MOSFET Model (mos30)

Long Channel JFET/MOSFET Model (mos3002)

Long Channel JFET/MOSFET Model (mos30)

This long channel JFET/MOSFET model is specially developed to describe the drift region of LDMOS, EPMOS and VDMOS devices. It is described in the Philips MOST Modelbook (Dec.95) as MOS model, level 30 (Used for DMOS). Information on how to obtain this document can be found on Source Link by searching for Philips.

Note: In noise analysis, mos30 instances will not generate any contribution, since there are no noise sources included in the mos30 model.

Warning: Dont use this model. It is obsolete.

Mos30 will be removed from spectre in the next release.

(c) Philips Electronics N.V. 1993, 1994, 1996

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

```
mn30 (1 2 0 0) nchmod area=2 mult=1
```

Sample Model Statement

```
model nchmod mos30 type=n tox=1.1e-5 ron=150 rsat=500 psat=2 vsat=1 vsub=0.59
cgate=1.65e-12 csub=1.1e-9 tref=25
```

Instance Syntax

```
Name  d  g  s  [b] ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`area=1`	Alias of mult.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, or `subth`.
`m=1`	Multiplicity factor.

Model Syntax

```
model modelName mos30 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`type=n`	Transistor gender. Possible values are `n` or `p`.
`ron=1.0 Ω`	Ohmic resistance at zero bias.
`rsat=1.0 Ω`	Space charge resistance at zero bias.
`vsat=10.0 V`	Critical drain-source voltage for hot carriers.
`psat=1.0`	Velocity saturation coefficient.
`vp=-1.0 V`	Pinch off voltage at zero gate and substrate voltages.
`tox=-1.0 cm`	Gate oxide thickness.
`dch=1.0e15` cm^{-3}	Doping level channel.
`dsub=1.0e15` cm^{-3}	Doping level substrate.
`vsub=0.6 V`	Substrate diffusion voltage.
`vgap=1.2 V`	Bandgap voltage channel.
`cgate=0.0 F`	Gate capacitance at zero bias.
`csub=0.0 F`	Substrate capacitance at zero bias.
`tausc=0.0 s`	Space charge transit time of the channel.
`ach=0.0`	Temperature coefficient resistivity of the channel.
`kf=0.0`	Flickernoise coefficient.
`af=1.0`	Flickernoise exponent.
`tr (C)`	Reference temperature. Default set by option `tnom`.
`tref (C)`	Alias of tr. Default set by option `tnom`.
`tnom (C)`	Alias of tr. Default set by option `tnom`.
`dta=0.0 K`	Temperature offset of the device.
`trise=0.0 K`	Alias of `dta`.

Output Parameters

`ront (Ω)`	Ohmic resistance at zero bias.
`rsat (Ω)`	Space charge resistance at zero bias.
`vsatt (V)`	Critical drain-source voltage for hot carriers.

© 2023 Cadence Design Systems, Inc.

`vsubt (V)`	Substrate diffusion voltage.
`cgate (F)`	Gate capacitance at zero bias.
`csubt (F)`	Substrate capacitance at zero bias.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`pwr (W)`	Power.
`ids (A)`	Total current including velocity saturation.
`qb (Coul)`	Substrate charge.
`qg (Coul)`	Gate charge.
`qds (Coul)`	Space charge in the channel.
`gdsd (S)`	Conductance (d ids / d vd).
`gdsg (S)`	Conductance (d ids / d vg).
`gdss (S)`	Conductance (d ids / d vs).
`gdsb (S)`	Conductance (d ids / d vb).
`cbd (F)`	Capacitance (d qb / d vd).
`cbg (F)`	Capacitance (d qb / d vg).
`cbs (F)`	Capacitance (d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgd (F)`	Capacitance (d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (d qg / d vs).
`cgb (F)`	Capacitance (d qg / d vb).
`cdsd (F)`	Capacitance (d qds / d vd).
`cdsg (F)`	Capacitance (d qds / d vg).
`cdss (F)`	Capacitance (d qds / d vs).
`cdsb (F)`	Capacitance (d qds / d vb).

Related Topics

Philips Models

JFETIDG Model (jfetidg)

Long Channel JFET/MOSFET Model (mos3002)

© 2023 Cadence Design Systems, Inc.

MOS Model 40, Level 40 (mos40t)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.

Model Syntax

```
model modelName mos40t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

level=40	Level of this model.
paramchk=0	Level of clip warning info.
vbox=0 V	Oxide breakdown voltage.
vbds=0 V	Drain-source breakdown voltage.
vbdblow=0 V	Low limit of drain-bulk voltage
vbdbhigh=0 V	High limit of drain-bulk voltage.
vbsblow=0 V	Low limit of source-bulk voltage.
vbsbhigh=0 V	High limit of source-bulk voltage.
vballmsg=1	All ovcheck messages if set to 1.
tmin=0 s	Ovcheck tmin value.
tdelay=0 s	Stop simulation on overvoltage when STOP==1.
stop=0	Ohmic resistance at zero bias.
ron=1 Ω	Ohmic resistance at zero bias.
rsat=1 Ω	Space charge resistance at zero bias.
vsat=10 V	Critical drain-source voltage for hot carriers.
psat=1	Velocity saturation coefficient.
vp=-1 V	Pinch off voltage at zero gate and substrate voltages.
tox=-1 m	Gate oxide thickness.
dch=1e+21 m^{-3}	Doping level channel.
tbox=-1 m^{-3}	Box oxide thickness.
cgate=0 F	Gate capacitance at zero bias.
cbox=0 F	Wafer capacitance.
tausc=0 s	Space charge transit time of the channel.
ach=0	Temperature coefficient resistivity of the channel.
achmod=0	Parameter to switch to extended temperature scaling.
achron=0	Temperature coefficient of ohmic resistance at zero bias.

© 2023 Cadence Design Systems, Inc.

`achvsat=0`	Temperature coefficient of critical drain-source voltage for hot carriers.
`achrsat=0`	Temperature coefficient of space charge resistance at zero bias.
`tref=25 C`	Reference temperature.
`dta=0 K`	Temperature offset of the device.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`tnom (C)`	Alias of tnom.
`tr (C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`ids (A)`	Drain source current.
`vds (V)`	Drain source voltage.
`vgs (V)`	Gate source voltage.
`vbs (V)`	Bulk source voltage.
`vp (V)`	Channel pinch-off voltage.
`gm (A/V)`	Transconductance.
`gmb (A/V)`	Bulk transconductance.
`gds (A/V)`	Output conductance.
`qg (C)`	Gate charge.
`cgd (F)`	Gate charge dependence on drain voltage.
`cgg (F)`	Gate charge dependence on gate voltage.
`cgs (F)`	Gate charge dependence on substrate voltage.
`cgb (F)`	Gate charge dependence on bulk voltage.
`qb (C)`	Bulk charge.
`cbd (F)`	Bulk charge dependence on drain voltage.
`cbg (F)`	Bulk charge dependence on gate voltage.
`cbs (F)`	Bulk charge dependence on substrate voltage.
`cbb (F)`	Bulk charge dependence on bulk voltage.
`qd (C)`	Drain charge.
`cdd (F)`	Drain charge dependence on drain voltage (dQd/dVd).
`cdg (F)`	Drain charge dependence on gate voltage (-dQd/dVg).
`cds (F)`	Drain charge dependence on source voltage (-dQd/dVs).
`cdb (F)`	Drain charge dependence on bulk voltage (-dQd/dVb).

© 2023 Cadence Design Systems, Inc.

`qs (C)`	Source charge.
`csd (F)`	Source charge dependence on drain voltage (-dQs/dVd).
`csg (F)`	Source charge dependence on gate voltage (-dQs/dVg).
`css (F)`	Source charge dependence on source voltage (dQs/dVs).
`csb (F)`	Source charge dependence on bulk voltage (-dQs/dVb).
`u`	Transistor gain.
`rout (Ω)`	Small-signal output resistance.
`vearly (V)`	Equivelant early voltage.
`iohm (A)`	Drain source current excluding velocity saturation.
`ihc (A)`	Critical current for velocity saturation.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual temperature.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`pwr (W)`	Power.
`mos_region`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.

Related Topics

Philips Models

MOS Model 11, Level 1101 (mos11010)

MOS Model 11, Level 1101 (mos11010t)

MOS Model 11, Level 1101 (mos11011)

MOS Model 11, Level 1101 (mos11011t)

© 2023 Cadence Design Systems, Inc.

Long Channel JFET/MOSFET Model (mos3002)

This long channel JFET/MOSFET model is specially developed to describe the drift region of LDMOS, EPMOS and VDMOS devices. It is described in the Philips MOST Modelbook (Dec.98) as MOS model, level 3002 (Used for DMOS). Information on how to obtain this document can be found on Source Link by searching for Philips.

Note: In noise analysis, mos3002 instances will not generate any contribution, since there are no noise sources included in the mos3002 model.

(c) Philips Electronics N.V. 1993, 1994, 1996, 1998

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Sample Instance Statement

```
mn3 (1 2 0 0) nch3002 area=1 m=2
```

Sample Model Statement

```
model nch3002 mos3002 ron=20 rsat=150 vsat=1 tox=1.23e-5 dch=1.1e16 vsub=0.58
csub=5.43e-13 tausc=1.2e-12 kf=1 tref=27 psat=1 dta=0
```

Instance Syntax

```
Name  d  g  s  [b] ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`area=1`	Alias of mult.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, or `subth`.
`m=1`	Multiplicity factor.

Model Syntax

```
model modelName mos3002 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`type=n`	Transistor gender. Possible values are `n` or `p`.
`ron=1.0 Ω`	Ohmic resistance at zero bias.
`rsat=1.0 Ω`	Space charge resistance at zero bias.
`vsat=10.0 V`	Critical drain-source voltage for hot carriers.
`psat=1.0`	Velocity saturation coefficient.
`vp=-1.0 V`	Pinch off voltage at zero gate and substrate voltages.
`tox=-1.0 cm`	Gate oxide thickness.
`dch=1.0e15` cm^{-3}	Doping level channel.
`dsub=1.0e15` cm^{-3}	Doping level substrate.
`vsub=0.6 V`	Substrate diffusion voltage.
`vgap=1.2 V`	Band gap voltage channel.
`cgate=0.0 F`	Gate capacitance at zero bias.
`csub=0.0 F`	Substrate capacitance at zero bias.
`tausc=0.0 s`	Space charge transit time of the channel.
`ach=0.0`	Temperature coefficient resistivity of the channel.
`kf=0.0`	Flickernoise coefficient.
`af=1.0`	Flickernoise exponent.
`tr (C)`	Reference temperature. Default set by option `tnom`.
`tref (C)`	Alias of tr. Default set by option `tnom`.
`tnom (C)`	Alias of tr. Default set by option `tnom`.
`dta=0.0 K`	Temperature offset of the device.
`trise=0.0 K`	Alias of `dta`.

Output Parameters

`ront (Ω)`	Ohmic resistance at zero bias.
`rsat (Ω)`	Space charge resistance at zero bias.
`vsatt (V)`	Critical drain-source voltage for hot carriers.

© 2023 Cadence Design Systems, Inc.

`vsubt (V)`	Substrate diffusion voltage.
`cgate (F)`	Gate capacitance at zero bias.
`csubt (F)`	Substrate capacitance at zero bias.

Operating-Point Parameters

`pwr (W)`	Power.
`ids (A)`	Total current including velocity saturation.
`qb (Coul)`	Substrate charge.
`qg (Coul)`	Gate charge.
`qds (Coul)`	Space charge in the channel.
`gdsd (S)`	Conductance (d ids / d vd).
`gdsg (S)`	Conductance (d ids / d vg).
`gdss (S)`	Conductance (d ids / d vs).
`gdsb (S)`	Conductance (d ids / d vb).
`cbd (F)`	Capacitance (d qb / d vd).
`cbg (F)`	Capacitance (d qb / d vg).
`cbs (F)`	Capacitance (d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgd (F)`	Capacitance (d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (d qg / d vs).
`cgb (F)`	Capacitance (d qg / d vb).
`cdsd (F)`	Capacitance (d qds / d vd).
`cdsg (F)`	Capacitance (d qds / d vg).
`cdss (F)`	Capacitance (d qds / d vs).
`cdsb (F)`	Capacitance (d qds / d vb).

© 2023 Cadence Design Systems, Inc.

Related Topics

Philips Models

Long Channel JFET/MOSFET Model (mos30)

JFETIDG Model (jfetidg)

Compact MOS-Transistor Model (mos705)

The mos705 model is a compact MOS-transistor model, intended for the simulation of circuit behavior with emphasis on analog applications. It is described in the Philips MOST Modelbook (Dec.93) as MOS model, level 705.

(c) Philips Electronics N.V. 1993, 1994

In extension to the model book description a minimum conductance `gmin` is inserted between the drain and source node, to aid convergence. The value of `gmin` is set by an options statement, default = 1e-12 S.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Sample Instance Statement:

```
mn1 (1 2 0 0) mna7 ln=120e-6 wn=12e-6
```

Sample Model Statement:

```
model mna7 mos705 type=n vtn=0.853 betan=77e-6 tox=15e-9 vfb=-850e-3 tref=25
subthn=3 phi=0.645 lap=100e-9 gkn=-350e-9 th1n=0.15 th2n=0.046 th3n=0.1 fnoise=1e-
10
```

Instance Syntax

```
Name  d  g  s  [b] ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`wn=1.0 scale m`	Drawn channel width in the lay-out of the actual transistor. Scale set by option scale.
`ln=1.0 scale m`	Drawn channel length in the lay-out of the actual transistor. Scale set by option scale.
`w=1.0 scale m`	Alias for `wn`.
`l=1.0 scale m`	Alias for `ln`.
`mult=1`	Number of devices in parallel.
`area=1`	Alias of `mult`.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, or `subth`.
`m=1`	Multiplicity factor.
`trise=0 K`	Temperature rise from ambient.

Model Syntax

```
model modelName mos705 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`type=n`	Transistor gender. Possible values are `n` or `p`.
`vtn=0 V`	Threshold voltage of the reference transistor at the reference temperature.
`kon=0 √V`	`Ko` of the reference transistor.
`kn=100m √V`	`K` of the reference transistor.
`vsbxn=0 V`	`Vsbx` of the reference transistor.
`delvx=0 V`	`Dvsbx` of the reference transistor.
`th1n=0 1/V`	`The1` of the reference transistor.
`th2n=0 1/√V`	`The2` of the reference transistor.
`th3n=0 1/V`	`The3` of the reference transistor at the reference temperature.
`gamman=0`	`Gam` of the reference transistor.
`shiftn=0 V^(1-n)`	`Sh` of the reference transistor.
`nn=0`	`N` of the reference transistor.
`pn=0 1/V`	`P` of the reference transistor.
`ava=0`	`A` of the reference transistor.
`avb=1 V`	`B` of the reference transistor.
`avc=0`	`C` of the reference transistor.
`wref=100u m`	Effective width of the reference transistor.
`wtol=0 m`	Difference between drawn and effective gate width.
`dvtn=0 V m`	Narrow-width factor of the threshold voltage at `vsbref`.
`dkon=0 √v m`	Narrow-width factor of `ko`.
`dkn=0 √v m`	Narrow-width factor of `k`.
`dvsbxn=0 V m`	Narrow-width factor of `vsbx`.
`ddelvx=0 Vm`	Narrow-width factor of `dvsbx`.
`betan=20u A/V^2`	Gain factor of a infinite-square transistor at the reference temperature.
`dth1n=0 m/V`	Narrow-width factor of `the1`.

© 2023 Cadence Design Systems, Inc.

dth2n=0 m/√V	Narrow-width factor of the2.
dth3n=0 m/V	Narrow-width factor of the3.
dgamn=0 m	Narrow-width factor of gam.
dava=0 m	Narrow-width factor of a.
davb=0 V m	Narrow-width factor of b.
davc=0 m	Narrow-width factor of c.
lref=100u m	Effective length of the reference transistor.
ltol=0 m	Difference between drawn and actual gate polysilicon length.
gvtn=0 V m	Short-channel factor of the threshold voltage at vsbref.
gkon=0 √V m	Short-channel factor of ko.
gkn=0 √V m	Short-channel factor of k.
gvsbxn=0 V m	Short-channel factor of vsbx.
gdelvx=0 V m	Short-channel factor of dvsbx.
gth1n=0 m/V	Short-channel factor of the1.
gth2n=0 m/√V	Short-channel factor of the2.
gth3n=0 m/V	Short-channel factor of the3.
ggamn=0 m	Short-channel factor of gam.
gshift=0 V^(1-n) m^2	Short-channel factor of sh.
gnn=0 m	Short-channel factor of n.
gpn=0 m/V	Short-channel factor of p.
gava=0 m	Short-channel factor of a.
gavb=0 V m	Short-channel factor of b.
gavc=0 m	Short-channel factor of c.
lap=0 m	Half of the effective channel-length reduction due to lateral diffusion.
vsbref=0 V	Source to bulk reference voltage for parameter determination.

© 2023 Cadence Design Systems, Inc.

`phi=600m V`	Diffusion potential at the reference temperature.
`tcvt=-1m V/K`	Temperature coefficient of `vto`.
`tbetan=1.5`	Power temperature coefficient of `bet`.
`tth3n=0 1/(V K)`	Temperature coefficient of `the3`.
`tgth3n=0 m/(V K)`	Temperature coefficient of the length dependence of `the3`.
`m=1.0`	Subthreshold-slope factor at reference back bias and at the reference temperature.
`subthn=0`	Weak-inversion factor.
`vtr=0 V`	Depletion-MOS-transistor-transition voltage.
`ratio=0`	Depletion-MOS-transistor-gain ratio.
`vfb=0 V`	Flat-band voltage.
`tox=100n m`	Gate-oxide thickness.
`col=0 F/m`	Gate/drain or gate/source overlap capacitance per unit length.
`fnoise=0` m^2 V^2	Flicker-noise factor.
`tnoise=0`	Thermal-noise factor.

© 2023 Cadence Design Systems, Inc.

Temperature parameters

`tr (C)`	Reference temperature. Default set by option `tnom`.
`tref (C)`	Alias of `tr`. Default set by option `tnom`.
`tnom (C)`	Alias of `tr`. Default set by option `tnom`.
`dta=0 K`	Deviation between the temperature of the transistor and the temperature of the circuit.
`trise=0 K`	Alias of `dta`.

Output Parameters

`weff (V)`	Effective channel width of the actual transistor.
`leff (V)`	Effective channel length of the actual transistor.
`twophif (V)`	Diffusion potential.
`bet (A/V`^{2}`)`	Gain factor of the transistor.
`k (`$\sqrt{V}$ `)`	Body-effect factor.
`ko (`$\sqrt{V}$ `)`	Initial body-effect factor for dual `k` approach.
`vsbx (V)`	Transition voltage for dual `k` approach.
`dvsbx (V)`	Transition-voltage range for dual `K` approach.
`vto (V)`	Threshold voltage.
`von (V)`	Onset voltage of the superthreshold region.
`the1 (1/V)`	Gate-bias-controlled transverse-field mobility reduction factor.
`the2 (1/`$\sqrt{V}$ `)`	Back-bias-controlled transverse-field mobility reduction factor.
`the3 (1/V)`	Lateral-field mobility reduction factor (velocity saturation).
`gam`	Static-drain-feedback factor.
`sh (V^(1-n))`	Threshold-voltage-shift factor.
`n`	Threshold-voltage-shift exponent.
`p (1/V)`	Back-bias-shift factor.
`me (`$\sqrt{V}$ `)`	Auxiliary parameter for subthreshold-slope factor.

© 2023 Cadence Design Systems, Inc.

`a`	Weak-avalanche multiplier.
`b (V)`	Weak-avalanche exponent factor.
`c`	Saturation-voltage reduction factor.
`cox (F)`	Gate capacitance.
`cgso (F)`	Gate/source-overlap capacitance.
`cgdo (F)`	Gate/drain-overlap capacitance.
`vtre (V)`	Depletion MOS transistor transition voltage.
`ratio`	Depletion MOS transistor gain ratio.
`vfbe (V)`	Flat band voltage.
`vtemp (V)`	kT/q at actual device temperature.
`gnoise (V`^{2}`)`	Coefficient of the flicker noise for the actual transistor.
`unoise (J)`	Coefficient of the thermal noise for the actual transistor.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`ide (A)`	Drain current.
`ige (A)`	Gate current.
`ise (A)`	Source current.
`ibe (A)`	Bulk current.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`ids (A)`	Drain-source current.
`idb (A)`	Drain-bulk current.
`isb (A)`	Source-bulk current.
`pwr (W)`	Power.
`vts (V)`	Vto including back-bias effects.
`vgt (V)`	Effective gate drive including back-bias and drain effects.
`vdss (V)`	Saturation voltage at actual bias.
`gm (S)`	Transconductance (d ids / d vgs).
`gmb (S)`	Bulk transconductance (d ids / d vbs).
`gds (S)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).

© 2023 Cadence Design Systems, Inc.

`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|Id|/gds).
`keff (√V )`	Describes body effect at actual bias.
`beff (S/V)`	Effective beta at actual bias in the simple MOS model.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cox)).
`sqrtsfw (V/√Hz )`	Input-referred RMS white noise voltage (sqrt(sth)/gm).
`sqrtsff (V/√Hz )`	Input-referred RMS 1/f noise voltage at 1kHz (sqrt(gnoise/1000)).
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.

Related Topics

Philips Models

Compact MOS-Transistor Model (mos902)

Compact MOS-Transistor Model (mos903)

Compact MOS-Transistor Model (mos902)

The mos902 model is a compact MOS-transistor model, intended for the simulation of circuit behavior with emphasis on analog applications. It is described in the Philips MOST

© 2023 Cadence Design Systems, Inc.

Modelbook (Feb.98) as MOS model, level 902. Information on how to obtain this document can be found on Source Link by searching for Philips.

(c) Philips Electronics N.V. 1993, 1998

In extension to the model book description, a minimum conductance `gmin` is inserted between the drain and source node to aid convergence. The value of `gmin` is set by an options statement, default = 1e-12 S.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Sample Instance Statement:

```
mp1 (0 1 2 2) mos9pch w=10u l=2u area=1.5
```

Sample Model Statement:

```
model mos9pch mos902 ler=0.93e-6 wer=20e-6 tref=27 vtor=1.11 kr=0.54 phibr=0.66
vsbxr=100 the1r=0.19 slk=-0.215e-6 swk=98e-9 swthe3=7.8e-9
```

Instance Syntax

```
Name  d  g  s  [b] ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`w=1.0 scale m`	Drawn channel width in the lay-out. Scale set by option scale.
`l=1.0 scale m`	Drawn channel length in the lay-out. Scale set by option scale.
`mult=1`	Number of devices in parallel.
`area=1`	Alias of `mult`.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, or `subth`.
`m=1`	Multiplicity factor.
`trise=0 K`	Temperature rise from ambient.

Model Syntax

```
model modelName mos902 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

`type=n`	Transistor gender. Possible values are `n` or `p`.

Geometry parameters

`ler=2.5e-6 m`	Effective channel length of the reference transistor.
`wer=25e-6 m`	Effective channel width of the reference transistor.
`lvar=0.3e-6 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=0.1e-6 m`	Effective channel length reduction per side.
`wvar=3e-6 m`	Difference between the actual and the programmed field-oxide opening.
`wot=1e-6 m`	Effective channel width reduction per side.
`wdog=0 m`	Characteristic drawn gate width, below which dogboning appears.

Threshold-voltage parameters

`vtor=0.8 V`	Threshold voltage at zero back-bias.
`stvto=0.01 V/K`	Coefficient of the temperature dependence of `vto`.
`slvto=0.5e-6 V m`	Coefficient of the length dependence of `vto`.
`sl2vto=0 V` m^2	Second coefficient of the length dependence of `vto`.
`swvto=5e-6 V m`	Coefficient of the width dependence of `vto`.
`kor=0.5` $\sqrt{V}$	Low-backbias body factor.
`slko=1e-6` $\sqrt{V}$ `m`	Coefficient of the length dependence of `ko`.
`swko=10e-6` $\sqrt{V}$ `m`	Coefficient of the width dependence of `ko`.
`kr=0.1` $\sqrt{V}$	High-backbias body factor.
`slk=0.5e-6` $\sqrt{V}$ `m`	Coefficient of the length dependence of `k`.
`swk=5e-6` $\sqrt{V}$ `m`	Coefficient of the width dependence of `k`.

© 2023 Cadence Design Systems, Inc.

`phibr=0.65 V`	Surface potential at strong inversion.
`vsbxr=0.9 V`	Transition voltage for the dual-`k`-factor model.
`slvsbx=0.5e-6 V m`	Coefficient of the length dependence of `vsbx`.
`swvsbx=5e-6 V m`	Coefficient of the width dependence of `vsbx`.

© 2023 Cadence Design Systems, Inc.

Channel-current parameters

betsq=0.1e-3 A/V^2	Gain factor for an infinite square transistor.
etabet=0.5	Exponent of the temperature dependence of the gain factor.
the1r=0.05 1/V	Coefficient of the mobility reduction due to the gate-induced field.
stthe1r=3e-3 1/(V K)	Coefficient of the temperature dependence of the1.
slthe1r=50e-9 m/V	Coefficient of the length dependence of the1.
stlthe1=5e-9 m/(V K)	Coefficient of the temperature dependence of slthe1.
swthe1=1e-6 m/V	Coefficient of the width dependence of the1.
fthe1=0	Coefficient describing the width dependence of the1 for w < wdog.
the2r=17e-3 1/√V	Coefficient of the mobility reduction due to the back-bias.
stthe2r=0.1e-3 1/(√V K)	Coefficient of the temperature dependence of the2.
slthe2r=5e-9 m/√V	Coefficient of the length dependence of the2.
stlthe2=0.5e-9 m/(√V K)	Coefficient of the temperature dependence of slthe2.
swthe2=0.1e-6 m/√V	Coefficient of the width dependence of the2.
the3r=37e-3 1/V	Coefficient of the mobility reduction due to the lateral field.
stthe3r=0.1e-3 1/(V K)	Coefficient of the temperature dependence of the3.
slthe3r=5e-9 m/V	Coefficient of the length dependence of the3.
stlthe3=0.5e-9 m/(V K)	Coefficient of the temperature dependence of slthe3.
swthe3=0.1e-6 m/V	Coefficient of the width dependence of the3.

Drain-feedback parameters

gam1r=40e-3 V^(1-etads)

© 2023 Cadence Design Systems, Inc.

	Coefficient for the drain induced threshold shift for large gate drive.
`slgam1=0.1e-6 V^(1-etads) m`	
	Coefficient of the length dependence of `gam1`.
`swgam1=1e-6 V^(1-etads) m`	
	Coefficient of the width dependence of `gam1`.
`etadsr=0.6`	Exponent of the vds dependence of `gam1`.
`alpr=4e-3`	Factor of the channel-length modulation.
`etaalp=0.5`	Exponent of the length dependence of `alp`.
`slalp=0.14e-3 m^etaalp`	
	Coefficient of the length dependence of `alp`.
`swalp=0.1e-6 m`	Coefficient of the width dependence of `alp`.
`vpr=0.25 V`	Characteristic voltage of the channel-length modulation.

© 2023 Cadence Design Systems, Inc.

Sub-threshold parameters

`gamoor=1.1e-3`	Coefficient for the drain induced threshold shift at zero gate drive.
`slgamoo=10e-15 m`^{2}	Coefficient of the length dependence of `gamoo`.
`etagamr=2`	Exponent of the back-bias dependence of `gamo`.
`mor=0.3`	Factor for the subthreshold slope.
`stmo=0.01 1/K`	Coefficient of the temperature dependence of `mo`.
`slmo=1.4e-3 √m`	Coefficient of the length dependence of `mo`.
`etamr=2`	Exponent of the back-bias dependence of m.
`zet1r=0.7`	Weak-inversion correction factor.
`etazet=0.5`	Exponent of the length dependence of `zet1`.
`slzet1=0.14e-6 m^etazet`	Coefficient of the length dependence of `zet1`.
`vsbtr=99 V`	Limiting voltage of the vsb dependence of m and `gamo`.
`slvsbt=10e-6 V m`	Coefficient of the length dependence of `vsbt`.

Weak-avalanche parameters

`a1r=22`	Factor of the weak-avalanche current.
`sta1=0.1 1/K`	Coefficient of the temperature dependence of `a1`.
`sla1=10e-6 m`	Coefficient of the length dependence of `a1`.
`swa1=0.1e-3 m`	Coefficient of the width dependence of `a1`.
`a2r=33 V`	Exponent of the weak-avalanche current.
`sla2=10e-6 V m`	Coefficient of the length dependence of `a2`.
`swa2=0.1e-3 V m`	Coefficient of the width dependence of `a2`.
`a3r=0.6`	Factor of the drain-source voltage above which weak-avalanche occurs.
`sla3=1e-6 m`	Coefficient of the length dependence of `a3`.
`swa3=10e-6 m`	Coefficient of the width dependence of `a3`.

© 2023 Cadence Design Systems, Inc.

Charge parameters

`tox=20e-9 m`	Thickness of the oxide layer.
`col=50e-12 F/m`	Gate overlap capacitance per unit channel width.

Noise parameters

`ntr=21e-21 J`	Coefficient of the thermal noise.
`nfr=16e-12` V^2	Coefficient of the flicker noise.

Temperature parameters

`tr (C)`	Reference temperature. Default set by option `tnom`.
`tref (C)`	Alias of `tr`. Default set by option `tnom`.
`tnom (C)`	Alias of `tr`. Default set by option `tnom`.
`dta=0 K`	Temperature offset of the device.
`trise=0 K`	Alias of `dta`.

Output Parameters

`le (m)`	Effective channel length.
`we (m)`	Effective channel width.
`vto (V)`	Threshold voltage at zero back-bias.
`ko (`$\sqrt{V}$`)`	Low-backbias body factor.
`k (`$\sqrt{V}$`)`	High-backbias body factor.
`phib (V)`	Surface potential at strong inversion.
`vsbx (V)`	Transition voltage for the dual-`k`-factor model.
`bet (`A/V^2`)`	Gain factor (* mult).
`the1 (1/V)`	Coefficient of the mobility reduction due to the gate-induced field.
`the2 (1/`$\sqrt{V}$`)`	Coefficient of the mobility reduction due to the back-bias.

© 2023 Cadence Design Systems, Inc.

the3 (1/V)	Coefficient of the mobility reduction due to the lateral field.
gam1 (V^(1-etads))	Coefficient for the drain induced threshold shift for large gate drive.
etads	Exponent of the vds dependence of gam1.
alp	Factor of the channel-length modulation.
vp (V)	Characteristic voltage of the channel-length modulation.
gamoo	Coefficient for the drain induced threshold shift at zero gate drive.
etagam	Exponent of the back-bias dependence of gamo.
mo	Factor for the subthreshold slope.
etam	Exponent of the back-bias dependence of m.
phit (V)	Thermal voltage.
zet1	Weak-inversion correction factor.
vsbt (V)	Limiting voltage of the vsb dependence of m and gamo.
a1	Factor of the weak-avalanche current.
a2 (V)	Exponent of the weak-avalanche current.
a3	Factor of the drain-source voltage above which weak-avalanche occurs.
cox (F)	Gate-to-channel capacitance (* mult).
cgdo (F)	Gate-drain overlap capacitance (* mult).
cgso (F)	Gate-source overlap capacitance (* mult).
nt (J)	Coefficient of the thermal noise.
nf (V^2)	Coefficient of the flicker noise (/ mult).
lv2 (m)	
lv1 (m)	
lv51 (m)	
lv50 (V)	

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`ide (A)`	Resistive drain current.
`ige (A)`	Resistive gate current.
`ise (A)`	Resistive source current.
`ibe (A)`	Resistive bulk current.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`ids (A)`	Resistive drain-source current.
`idb (A)`	Resistive drain-bulk current.
`isb (A)`	Resistive source-bulk current.
`iavl (A)`	Substrate current.
`pwr (W)`	Power.
`vt1 (V)`	`Vto` including backbias effects.
`vgt2 (V)`	Effective gate drive including backbias and drain effects.
`vdss1 (V)`	Saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (S)`	Transconductance (d ids / d vgs).
`gmb (S)`	Bulk transconductance (d ids / d vbs).
`gds (S)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).

© 2023 Cadence Design Systems, Inc.

csd (F)	Capacitance (- d qs / d vd).
csg (F)	Capacitance (- d qs / d vg).
css (F)	Capacitance (d qs / d vs).
csb (F)	Capacitance (- d qs / d vb).
cbd (F)	Capacitance (- d qb / d vd).
cbg (F)	Capacitance (- d qb / d vg).
cbs (F)	Capacitance (- d qb / d vs).
cbb (F)	Capacitance (d qb / d vb).
u	Transistor gain (gm/gds).
rout (Ω)	Small signal output resistance (1/gds).
vearly (V)	Equivalent Early voltage (lidl/gds).
keff (√V)	Describes body effect at actual bias.
beff (S/V)	Effective beta at actual bias in the simple MOS model (2*lidsl/vgt2^2).
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw (V/√Hz)	Input-referred RMS white noise voltage (sqrt(sth)/gm).
sqrtsff (V/√Hz)	Input-referred RMS 1/f noise voltage at 1kHz (sqrt(nf/1000)).
fknee (Hz)	Cross-over frequency above which white noise is dominant.
lv9 (V)	
lv10 (V)	
lv26 (V)	
lx4 (A)	
lx50 (A)	
lx12 (Coul)	
lx14 (Coul)	
lx16 (Coul)	
linearity_factor	
I1 (A)	

© 2023 Cadence Design Systems, Inc.

Related Topics

Philips Models

Compact MOS-Transistor Model (mos705)

Compact MOS-Transistor Model (mos903)

Compact MOS-Transistor Model (mos903)

The mos903 model is a compact MOS-transistor model, intended for the simulation of circuit behavior with emphasis on analog applications. It is described in the Philips MOST Modelbook (Jun.98) as MOS model, level 903. Information on how to obtain this document can be found on Source Link by searching for Philips.

(c) Philips Electronics N.V. 1993, 1998

In extension to the model book description, a minimum conductance `gmin` is inserted between the drain and source node to aid convergence. The value of `gmin` is set by an options statement, default = 1e-12 S.

This is SimKit 5.0.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Sample Instance Statement

```
m_1 (1 2 0 0) mos9nch w=0.35e-6 l=0.35e-6
```

Sample Model Statement

```
model mos9nch mos903 ler=3.5e-7 wer=1e-5 lvar=0 lap=2.2e-8 wvar=0 wot=3e-8
vtor=0.76 the1r=0.67 stthe1r=-1.76e-3 etaalp=0 slalp=0 alpr=0.01
```

Instance Syntax

```
Name  d  g  s  [b] ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=1.5e-06 m`	Drawn channel length in the lay-out. Scale set by option scale.
`w=2e-05 m`	Drawn channel width in the lay-out. Scale set by option scale.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	alias of mult.

Model Syntax

```
model modelName mos903 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=903`	MOS Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage
`vbdblow=0 V`	Low limit of drain-bulk voltage.
`vbdbhigh=0 V`	High limit of drain-bulk voltage
`vbsblow=0 V`	Low limit of source-bulk voltage.
`vbsbhigh=0 V`	High limit of source-bulk voltage.
`vballmsg=1`	All ovcheck messages if set to 1.
`tmin=0 s`	Ovcheck tmin value.
`tdelay=0 s`	Ovcheck tdelay value.
`stop=0`	Stop simulation on overvoltage when STOP==1.
`ler=1.1e-06(n)/1.25e-06(p) m`	Effective channel length of the reference transistor.
`wer=2e-05 m`	Effective channel width of the reference transistor.
`lvar=-2.2e-07(n)/-4.6e-07(p) m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=1e-07(n)/2.5e-08(p) m`	Effective channel length reduction per side.
`wvar=-2.5e-08(n)/-1.3e-07(p) m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 unitCELSIUS`	Reference temperature. Default set by option `tnom`.
`vtor=0.73(n)/1.1(p) V`	Threshold voltage at zero back-bias.
`stvto=-0.0012(n)/-0.0017(p) V/K`	

© 2023 Cadence Design Systems, Inc.

Coefficient of the temperature dependence of `vto`.

`slvto=-1.35e-07(n)/3.5e-08(p) V m`

Coefficient of the length dependence of `vto`.

`sl2vto=0 V m`^{2} Second coefficient of the length dependence of `vto`.

`sl3vto=0 V` Third coefficient of the length dependence of `vto`.

`swvto=1.3e-07(n)/5e-08(p) V m`

Coefficient of the width dependence of `vto`.

`kor=0.65(n)/0.47(p) V`

Low-backbias body factor.

`slko=-1.3e-07(n)/-2e-07(p) V m`

Coefficient of the length dependence of `ko`.

`sl2ko=0 V1/2m2` Second coefficient of the length dependence of `ko`.

`swko=2e-09(n)/1.15e-07(p) V m`

Coefficient of the width dependence of `ko`.

`kr=0.11(n)/0.47(p) V`

High-backbias body factor.

`slk=-2.8e-07(n)/-2e-07(p) V m`

Coefficient of the length dependence of `k`.

`sl2k=0 V1/2m2` Second coefficient of the length dependence of `k`.

`swk=2.75e-07(n)/1.15e-07(p) V m`

Coefficient of the width dependence of `k`.

`phibr=0.65 V` Surface potential at strong inversion.

`vsbxr=0.66(n)/1e-12(p) V`

Transition voltage for the dual-`k`-factor model.

`slvsbx=0 V m` Coefficient of the length dependence of `vsbx`.

`swvsbx=-6.75e-07(n)/0(p) V m`

Coefficient of the width dependence of `vsbx`.

`betsq=8.3e-05(n)/2.61e-05(p) A/V`^{2}

Gain factor for an infinite square transistor.

© 2023 Cadence Design Systems, Inc.

`etabet=1.6`	Exponent of the temperature dependence of the gain factor.
`lp1=1e-06 m`	Characteristic length of first profile.
`fbet1=0`	Relative mobility decrease due to first profile.
`lp2=1e-08 m`	Characteristic length of second profile.
`fbet2=0`	Relative mobility decrease due to second profile.
`the1r=0.19 1/V`	Coefficient of the mobility reduction due to the gate-induced field.
`stthe1r=0 1/(V K)`	Coefficient of the temperature dependence of `the1`.
`slthe1r=1.4e-07(n)/7e-08(p) m/V`	Coefficient of the length dependence of `the1`.
`stlthe1=0 m/(V K)`	Coefficient of the temperature dependence of `slthe1`.
`gthe1=0`	Parameter that selects either the old (gthe1=0) or the new (gthe1=1) scaling rule of the1.
`swthe1=-5.8e-08(n)/-8e-08(p) m/V`	Coefficient of the width dependence of `the1`.
`wdog=0 m`	Characteristic drawn gate width, below which dogboning appears.
`fthe1=0`	Coefficient describing the width dependence of `the1` for `w` < `wdog`.
`the2r=0.012(n)/0.165(p) 1/|V`	Coefficient of the mobility reduction due to the back-bias.
`stthe2r=0 1/(|V  K)`	Coefficient of the temperature dependence of `the2`.
`slthe2r=-3.3e-08(n)/-7.5e-08(p) m/|V`	Coefficient of the length dependence of `the2`.
`stlthe2=0 m/(|V  K)`	Coefficient of the temperature dependence of `slthe2`.
`swthe2=3e-08(n)/2e-08(p) m/|V`	Coefficient of the width dependence of `the2`.

© 2023 Cadence Design Systems, Inc.

`the3r=0.145(n)/0.027(p) 1/V`

Coefficient of the mobility reduction due to the lateral field.

`stthe3r=-0.00066(n)/0(p) 1/(V K)`

Coefficient of the temperature dependence of `the3`.

`slthe3r=1.85e-07(n)/2.7e-08(p) m/V`

Coefficient of the length dependence of `the3`.

`stlthe3=-6.2e-10(n)/0(p) m/(V K)`

Coefficient of the temperature dependence of `slthe3`.

`swthe3=2e-08(n)/1.1e-08(p) m/V`

Coefficient of the width dependence of `the3`.

`gam1r=0.145(n)/0.077(p) V^(1-etads)`

Coefficient for the drain induced threshold shift for large gate drive.

`slgam1=1.6e-07(n)/1.05e-07(p) V^(1-etads) m`

Coefficient of the length dependence of `gam1`.

`swgam1=-1e-08(n)/-1.1e-08(p) V^(1-etads) m`

Coefficient of the width dependence of `gam1`.

`etadsr=0.6` Exponent of the vds dependence of `gam1`.

`alpr=0.003(n)/0.044(p)`

Factor of the channel-length modulation.

`etaalp=0.15(n)/0.17(p)`

Exponent of the length dependence of `alp`.

`slalp=-0.00565(n)/0.009(p) m^etaalp`

Coefficient of the length dependence of `alp`.

`swalp=1.67e-09(n)/1.8e-10(p) m`

Coefficient of the width dependence of `alp`.

`vpr=0.34(n)/0.235(p) V`

Characteristic voltage of the channel-length modulation.

© 2023 Cadence Design Systems, Inc.

`gamoor=0.018(n)/0.007(p)`

Coefficient for the drain induced threshold shift at zero gate drive.

`slgamoo=2e-14(n)/1.1e-14(p)` m^2

Coefficient of the length dependence of `gamoo`.

`sl2gamoo=0` Second coefficient of the length dependence of `gamoo`.

`etagamr=2(n)/1(p)`

Exponent of the back-bias dependence of `gamo`.

`mor=0.5(n)/0.375(p)`

Factor for the subthreshold slope.

`stmo=0 1/K` Coefficient of the temperature dependence of `mo`.

`slmo=0.00028(n)/4.7e-05(p) m`

Coefficient of the length dependence of `mo`.

`etamr=2(n)/1(p)` Exponent of the back-bias dependence of m.

`zet1r=0.42(n)/1.3(p)`

Weak-inversion correction factor.

`etazet=0.17(n)/0.03(p)`

Exponent of the length dependence of `zet1`.

`slzet1=-0.39(n)/-2.8(p) m^etazet`

Coefficient of the length dependence of `zet1`.

`vsbtr=2.1(n)/100(p) V`

Limiting voltage of the vsb dependence of m and `gamo`.

`slvsbt=-4.4e-06(n)/0(p) V m`

Coefficient of the length dependence of `vsbt`.

`a1r=6(n)/10(p)` Factor of the weak-avalanche current.

`sta1=0 1/K` Coefficient of the temperature dependence of `a1`.

`sla1=1.3e-06(n)/-1.5e-05(p) m`

Coefficient of the length dependence of `a1`.

© 2023 Cadence Design Systems, Inc.

`swa1=3e-06(n)/3e-05(p) m`

Coefficient of the width dependence of `a1`.

`a2r=38(n)/59(p) V` Exponent of the weak-avalanche current.

`sla2=1e-06(n)/-8e-06(p) V m`

Coefficient of the length dependence of `a2`.

`swa2=2e-06(n)/1.5e-05(p) V m`

Coefficient of the width dependence of `a2`.

`a3r=0.65(n)/0.52(p)`

Factor of the drain-source voltage above which weak-avalanche occurs.

`sla3=-5.5e-07(n)/-4.5e-07(p) m`

Coefficient of the length dependence of `a3`.

`swa3=0(n)/-1.4e-07(p) m`

Coefficient of the width dependence of `a3`.

`tox=2.5e-08 m` Thickness of the oxide layer.

`col=3.2e-10 F/m` Gate overlap capacitance per unit channel width.

`ntr=2.44e-20(n)/ 2.11e-20(p) J`

Coefficient of the thermal noise.

`nfmod=0` Switch that selects either old or new flicker noise model.

`nfr=7e-11(n)/2.14e-11(p)` V^2

Flicker noise coefficient of the reference transistor (for nfmod=0).

`nfar=7.15e+22(n)/1.53e+22(p) 1/(V m`^{4}`)`

First coefficient of the flicker noise coefficient of the reference transistor (for nfmod=1).

`nfbr=2.16e+07(n)/4.06e+06(p) 1/(V m`^{2}`)`

Second coefficient of the flicker noise coefficient of the reference transistor (for nfmod=1).

`nfcr=0(n)/2.92e-10(p) 1/V`

© 2023 Cadence Design Systems, Inc.

	Third coefficient of the flicker noise coefficient of the reference transistor (for nfmod=1).
`th3mod=1`	Flag for theta3 clipping.
`dta=0 K`	Temperature offset of the device.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`tnom (unitCELSIUS)`	alias of tnom.
`tref (unitCELSIUS)`	alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`ids (A)`	Resistive drain-source current.
`iavl (A)`	Substrate current.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Threshold voltage at zero back-bias.
`vts (V)`	VT0 including backbias effects.
`vgt (V)`	Effective gate drive including backbias and drain effects.
`vdss (V)`	Saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (S)`	Transconductance (d ids / d vgs).
`gmb (S)`	Bulk transconductance (d ids / d vbs).
`gds (S)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).

© 2023 Cadence Design Systems, Inc.

`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgdol (F)`	Drain overlap capacitance of the actual transistor.
`cgsol (F)`	Gate overlap capacitance of the actual transistor.
`weff (m)`	Effective channel width for geometrical models.
`leff (m)`	Effective channel length for geometrical models.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|id|/gds).
`keff ( V )`	Describes body effect at actual bias.
`beff (S/V)`	Effective beta at actual bias in the simple MOS model (2*|ids|/vgt2^2).
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`sqrtsfw (V/ Hz )`	Input-referred RMS white noise voltage (sqrt(sth)/gm).
`sqrtsff (V/ Hz )`	Input-referred RMS 1/f noise voltage at 1kHz (sqrt(nf/1000)).
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`von (V)`	Signed vts (<0 for PMOS, >0 for NMOS).
`table_ids (A)`	Channel current.
`table_isub (A)`	Substrate current.
`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.

© 2023 Cadence Design Systems, Inc.

`table_vdsat (V)`	Saturation voltage at actual bias.
`table_qg (Coul)`	Charge at g node.
`table_qd (Coul)`	Charge at d node.
`table_qb (Coul)`	Charge at b node.
`mos_region=SUBTHRESHOLD`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.
`diode_region=ON`	DIODE region. Possible values are `off` and `on`.

Related Topics

Philips Models

Compact MOS-Transistor Model (mos902)

Compact MOS-Transistor Model (mos705)

Compact MOS-Transistor Distortion Model (mos1000)

The mos10.00 model is an experimental model based on the thesis of Ronald van Langevelde: "A compact MOSFET Model for Distortion Analysis in Analog Circuit Design", Technische Universiteit Eindhoven, 1998.

Note: In noise analysis, mos10.00 instances will not generate any contribution, since there are no noise sources included (yet) in the mos10.00 model.

(c) Philips Electronics N.V. 1999

In extension to the description, a minimum conductance `gmin` is inserted between the drain and source node to aid convergence. The value of `gmin` is set by an options statement, default = 1e-12 S.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  d  g  s  [b] ModelName parameter=value ...
```

Instance Parameters

`w=1.0 scale m`	Drawn channel width in the layout. Scale set by option scale.
`l=1.0 scale m`	Drawn channel length in the layout. Scale set by option scale.
`mult=1`	Number of devices in parallel.
`area=1`	Alias of `mult`.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Multiplicity factor.
`trise=0 K`	Temperature rise from ambient.

Model Syntax

```
model modelName mos1000 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

`type=n`	Transistor gender. Possible values are `n` and `p`.

Geometry parameters

`ler=1.0e-6 m`	Effective channel length of the reference transistor.
`wer=1e-6 m`	Effective channel width of the reference transistor.
`lvar=0.0 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=45.0e-9 m`	Effective channel length reduction per side.
`wvar=-5.0e-9 m`	Difference between the actual and the programmed field-oxide opening.
`wot=50.0e-9 m`	Effective channel width reduction per side.

Threshold-voltage parameters

`vfbr=-518.9e-03 V`	Flat-band voltage for reference transistor.
`stvfb=-1.2e-03 V/K`	Coefficient of temperature dependence of `vfb`.
`slvfb=24.0e-09 V m`	Coefficient of length dependence of `vfb`.
`sl2vfb=-1.1e-15 V m`^{2}	Second coefficient of length dependence of `vfb`.
`swvfb=4.400e-09 V m`	Coefficient of the width dependency of `vfb`.
`kor=368.0e-03 V`	Body effect coefficient for the reference transistor.
`slko=-8.240e-09 V m`	Coefficient of the length dependence of `ko`.
`sl2ko=-2.260e-15 V m`^{2}	Second coefficient of the length dependence of `ko`.
`swko=5.86e-09 V m`	Coefficient of the width dependence of `ko`.
`phibr=0.6 V`	Surface potential at strong inversion.

© 2023 Cadence Design Systems, Inc.

Channel-current parameters

`betsq=370.9e-06 A/V`^{2}	Gain factor for an infinite square transistor.
`etabet=1.6`	Exponent of the temperature dependence of the gain factor.
`thesrr=16.10e-3 1/V`^{2}	Mobility degradation parameter due to surface roughness scattering.
`stthesr=0.0 1/(V`^{2} `K)`	Coefficient of the temperature dependence of `thesr`.
`swthesr=0.0 1/(V`^{2} `m)`	Coefficient of the width dependence of `thesr`.
`thephr=0.055 1/V`	Mobility degradation parameter due to phonon scattering.
`sttheph=0.0 1/(V K)`	Coefficient of the temperature dependence of `theph`.
`swtheph=0.0 1/(V m)`	Coefficient of the width dependence of `theph`.
`etamobr=1.6`	Effective field parameter for dependence on depletion charge.
`swetamob=0.0 1/m`	Coefficient of the width dependence of `etamobr`.
`thersq=0.155 1/V`	Coefficient of gate voltage independent part of series resistance.
`swther=0.0 1/(V m)`	Coefficient of the width dependence of `ther`.
`ther1=0.0 V`	Numerator of gate voltage independent part of series resistance.
`ther2=1.0 V`	Denominator of gate voltage independent part of series resistance.
`thenr=0.480 1/V`	Velocity saturation parameter due to optical phonon scattering.
`stthen=0.0 1/(V K)`	Coefficient of the temperature dependence of `then`.
`swthen=0.0 1/(V m)`	

© 2023 Cadence Design Systems, Inc.

	Coefficient of the width dependence of `then`.
`thepr=0.0 1/V`	Velocity saturation parameter due to acoustic phonon scattering.
`stthep=0.0 1/(V K)`	
	Coefficient of the temperature dependence of `thep`.
`swthep=0.0 1/(V m)`	
	Coefficient of the width dependence of `thep`.
`gthep=1.0`	Velocity saturation factor due to acoustic phonon scattering.
`thethr=3.227e-3 1/V`^{3}	
	Coefficient of self-heating.
`sltheth=2.460e-9 1/(V`^{3} `m)`	
	Coefficient of the length dependence of `theth`.
`swtheth=0.0 1/(V`^{3} `m)`	
	Coefficient of the width dependence of `theth`.

Sub-threshold parameters

`sdiblo=2.030e-03 1/V`	
	Drain-induced barrier lowering parameter.
`sdiblexp=1.340`	Exponent of the length dependence of `sdibl`.
`dphi=0.800 V`	Parameter for short-channel subthreshold behavior.

© 2023 Cadence Design Systems, Inc.

Saturation parameters

`ssfsq=6.250e-03 1/V`	
	Static feedback parameter.
`swssf=0.0 1/(V m)`	
	Coefficient of the width dependence of `ssf`.
`alpsq=0.010 m`	Characteristic length parameter for channel length modulation.
`swalp=0.0 m`	Coefficient of the width dependence of `alp`.
`vp=0.075 V`	Characteristic voltage of channel-length modulation.

Smoothing parameters

`mexpo=0.093`	Smoothing factor.
`mexpl=0.065`	Coefficient of the length dependence of `mexp`.

Weak-avalanche parameters

`a1r=6`	Factor of the weak-avalanche current.
`sta1=0.0 1/K`	Coefficient of the temperature dependence of `a1`.
`sla1=1.30e-6 m`	Coefficient of the length dependence of `a1`.
`swa1=3.0e-06 m`	Coefficient of the width dependence of `a1`.
`a2r=38.0 V`	Exponent of the weak-avalanche current.
`sla2=1.00e-06 V m`	Coefficient of the length dependence of `a2`.
`swa2=2.00e-06 V m`	Coefficient of the width dependence of `a2`.
`a3r=0.650`	Factor of the drain-source voltage above which weak-avalanche occurs.
`sla3=-550.0e-06 m`	Coefficient of the length dependence of `a3`.
`swa3=0.0 m`	Coefficient of the width dependence of `a3`.

© 2023 Cadence Design Systems, Inc.

Charge parameters

`tox=4.5e-09 m`	Thickness of the oxide layer.
`col=320e-12 F/m`	Gate overlap capacitance per unit channel width.

Temperature parameters

`tr (C)`	Reference temperature. Default set by option `tnom`.
`tref (C)`	Alias of `tr`. Default set by option `tnom`.
`tnom (C)`	Alias of `tr`. Default set by option `tnom`.
`dta=0.0 K`	Temperature offset of the device. It served as the default value of instance trise.
`trise=0.0 K`	Alias of `dta`.

Output Parameters

`le (m)`	Effective channel length.
`we (m)`	Effective channel width.
`vfb (V)`	Flat-band voltage.
`ko (V )`	Body effect coefficient.
`phib (V)`	Surface potential at strong inversion.
`bet (A/V`^{2}`)`	Gain factor.
`thesr (1/V`^{2}`)`	Mobility degradation parameter due to surface roughness scattering.
`theph (1/V)`	Mobility degradation parameter due to phonon scattering.
`etamob`	Effective field parameter for dependence on depletion charge.
`ther (1/V)`	Coefficient of gate voltage independent part of series resistance.
`ther1 (V)`	Numerator of gate voltage independent part of series resistance.

© 2023 Cadence Design Systems, Inc.

`ther2 (V)`	Denominator of gate voltage independent part of series resistance.
`then (1/V)`	Velocity saturation parameter due to optical phonon scattering.
`thep (1/V)`	Velocity saturation parameter due to acoustic phonon scattering.
`gthep`	Velocity saturation factor due to acoustic phonon scattering.
`theth (1/V`^{3}`)`	Coefficient of self-heating.
`sdibl (1/`|`V )`	Drain-induced barrier lowering parameter.
`dphi (V)`	Parameter for short-channel subthreshold behavior.
`ssf (1/`|`V )`	Static feedback parameter.
`alp (m)`	Characteristic length parameter for channel length modulation.
`vp (V)`	Characteristic voltage of channel-length modulation.
`mexp`	Smoothing factor.
`phit (V)`	Thermal voltage.
`a1`	Factor of the weak-avalanche current.
`a2 (V)`	Exponent of the weak-avalanche current.
`a3`	Factor of the drain-source voltage above which weak-avalanche occurs.
`cox (F)`	Gate-to-channel capacitance (* mult).
`cgdo (F)`	Gate-drain overlap capacitance (* mult).
`cgso (F)`	Gate-source overlap capacitance (* mult).

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

ide (A)	Resistive drain current.
ige (A)	Resistive gate current.
ise (A)	Resistive source current.
ibe (A)	Resistive bulk current.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vsb (V)	Source-bulk voltage.
ids (A)	Resistive drain current.
idb (A)	Resistive drain-bulk current.
isb (A)	Resistive source-bulk current.
iavl (A)	Substrate current.
pwr (W)	Power.
vto (V)	Threshold voltage at zero back-bias.
vts (V)	Vts.
vgt (V)	Effective gate drive including backbias and drain effects.
vdss (V)	Saturation voltage at actual bias.
vsat (V)	Saturation limit.
gm (S)	Transconductance (d ids / d vgs).
gmb (S)	Bulk transconductance (d ids / d vbs).
gds (S)	Output conductance (d ids / d vds).
cdd (F)	Capacitance (d qd / d vd).
cdg (F)	Capacitance (- d qd / d vg).
cds (F)	Capacitance (- d qd / d vs).
cdb (F)	Capacitance (- d qd / d vb).
cgd (F)	Capacitance (- d qg / d vd).
cgg (F)	Capacitance (d qg / d vg).
cgs (F)	Capacitance (- d qg / d vs).

© 2023 Cadence Design Systems, Inc.

`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|id|/gds).
`keff (V )`	Describes body effect at actual bias.
`beff (S/V)`	Effective beta at actual bias in the simple MOS model (2*|ids|/vgt2^2).
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).

Related Topics

Philips Models

Compact MOS-Transistor Distortion Model (mos1100)

Compact MOS-Transistor Distortion Model (mos1100e)

Compact MOS-Transistor Distortion Model (mos1100)

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	
`trise=0`	Temperature rise from ambient.

Model Syntax

```
model modelName mos1100 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1.1e+03`	MOS Level.
`paramchk=0`	Level of clip warning info.
`ler=1e-06 m`	Effective channel length of the reference transistor.
`wer=1e-05 m`	Effective channel width of the reference transistor.
`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=4e-08 m`	Effective channel length reduction per side.
`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 C`	Reference temperature. Default set by option `tnom`.
`vfbr=-1.05 V`	Flat-band voltage for reference transistor.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of `vfb`.
`kor=0.5` $\sqrt{V}$	Body effect coefficient for the reference transistor.
`slko=0` $\sqrt{V}\ m$	Coefficient of the length dependence of `ko`.
`sl2ko=0` $\sqrt{V}\ m^2$	Second coefficient of the length dependence of `ko`.
`swko=0` $\sqrt{V}\ m$	Coefficient of the width dependence of `ko`.
`kpinv=0` $1/\sqrt{V}$	Inverse of body-effect factor of the poly-silicon gate.
`phibr=0.95 V`	Surface potential at strong inversion.
`slphib=0 Vm`	Coefficient of the length dependence of phib.
`sl2phib=0` Vm^2	Second coefficient of the length dependence of phib.
`swphib=0 Vm`	Coefficient of the width dependence of phib.
`betsq=0.000371(n)/ 0.000115(p)` A/V^2	Gain factor for an infinite square transistor.
`etabet=1.3(n)/0.5(p)`	Exponent of the temperature dependence of the gain factor.

© 2023 Cadence Design Systems, Inc.

`fbet1=0`	Relative mobility decrease due to first lateral profile.
`lp1=8e-07 m`	Characteristic length of first lateral profile.
`fbet2=0`	Relative mobility decrease due to second lateral profile.
`lp2=8e-07 m`	Characteristic length of second lateral profile.
`thesrr=0.4(n)/ 0.73(p) 1/V`	
	Coefficient of the mobility reduction due to surface roughness scattering.
`swthesr=0 m`	Coefficient of the width dependence of thesr.
`thephr=0.0129(n)/ 0.001(p) 1/V`	
	Coefficient of the mobility reduction due to phonon scattering.
`etaph=1.75`	Exponent of the temperature dependence of theph.
`swtheph=0 m`	Coefficient of the width dependence of theph.
`etamobr=1.4(n)/3(p)`	
	Effective field parameter for dependence on depletion/ inversion charge.
`stetamob=0 1/K`	Coefficient of the temperature dependence of etamob.
`swetamob=0 m`	Coefficient of the width dependence of etamob.
`nur=1`	Exponent of the field dependence of the mobility model minus 1.
`nuexp=5.25(n)/3.23(p)`	
	Exponent of the temperature dependence of parameter nu.
`therr=0.155(n)/0.08(p) 1/V`	
	Coefficient of the series resistance.
`etar=0.95(n)/0.4(p)`	
	Exponent of the temperature dependence of ther.
`swther=0 m`	Coefficient of the width dependence of ther.

© 2023 Cadence Design Systems, Inc.

`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`thesatr=0.5(n)/0.2(p) 1/V`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`slthesat=1`	Coefficient of length dependence of thesat.
`thesatexp=1`	Exponent of length dependence of thesat.
`etasat=1.04(n)/0.86(p)`	Exponent of the temperature dependence of thesat.
`swthesat=0 m`	Coefficient of the width dependence of thesat.
`thethr=0.001(n)/0.0005(p) 1/V`^{3}	Coefficient of self-heating.
`thethexp=1`	Exponent of the length dependence of theth.
`swtheth=0 m`	Coefficient of the width dependence of theth.
`sdiblo=0.002(n)/0.001(p) 1/`$\sqrt{}$`V`	Drain-induced barrier lowering parameter.
`sdiblexp=1.35`	Exponent of the length dependence of sdibl.
`mor=0`	Parameter for short-channel subthreshold slope.
`moexp=1.34`	Exponent of the length dependence of mo.
`ssfr=0.00625 1/`$\sqrt{}$`V`	Static feedback parameter.
`slssf=1e-06 m`	Coefficient of the length dependence of ssf.
`swssf=0 m`	Coefficient of the width dependence of ssf.
`alpr=0.01`	Factor of the channel length modulation.
`slalp=1`	Coefficient of the length dependence of alp.
`alpexp=1`	Exponent of the length dependence of alp.
`swalp=0 m`	Coefficient of the width dependence of `alp`.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.

© 2023 Cadence Design Systems, Inc.

`lmin=1.5e-07 m`	Minimum effective channel length in technology, used for calculation of smoothing factor m.
`a1r=6`	Factor of the weak-avalanche current.
`sta1=0 1/K`	Coefficient of the temperature dependence of a1.
`sla1=0 m`	Coefficient of the length dependence of a1.
`swa1=0 m`	Coefficient of the width dependence of a1.
`a2r=38 V`	Exponent of the weak-avalanche current.
`sla2=0 V m`	Coefficient of the length dependence of a2.
`swa2=0 V m`	Coefficient of the width dependence of a2.
`a3r=1`	Factor of the drain-source voltage above which weak-avalanche occurs.
`sla3=0 m`	Coefficient of the length dependence of a3.
`swa3=0 m`	Coefficient of the width dependence of `a3`.
`iginvr=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) A/V`^{2}	Probability factor for intrinsic gate tunneling current in inversion.
`igaccr=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igovr=0 A/V`^{2}	Gain factor for Source/Drain overlap gate tunneling current.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`col=3.2e-10 F/m`	Gate overlap capacitance per unit channel width.
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`ntr=1.66e-20 J`	Coefficient of the thermal noise.

© 2023 Cadence Design Systems, Inc.

`nfar=1.57e+22(n)/3.83e+23(p) 1/(Vm^4)`	
	First coefficient of the flicker noise.
`nfbr=4.75e+08(n)/1.02e+08(p) 1/(Vm^2)`	
	Second coefficient of the flicker noise.
`nfcr=0(n)/7.3e-09(p) 1/V`	
	Third coefficient of the flicker noise.
`dta=0 K`	Temperature offset of the device.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.
`tnom (C)`	alias of tnom.
`tref (C)`	alias of tnom.

Output Parameters

`vfb (V)`	Flat-band voltage for the actual transistor.
`ko (√V )`	Body-effect factor.
`kpinv (1/√V )`	Inverse of body-effect factor of the poly-silicon gate.
`phib (V)`	Surface potential at the onset of strong inversion.
`bet (A/V^2)`	Gain factor.
`thesr (1/V)`	Mobility degradation parameter due to surface roughness scattering.
`theph (1/V)`	Mobility degradation parameter due to phonon scattering.
`etamob`	Effective field parameter for dependence on depletion charge.
`nu`	Exponent of field dependence of mobility model.
`ther (1/V)`	Coefficient of series resistance.

© 2023 Cadence Design Systems, Inc.

`ther1 (V)`	Numerator of gate voltage dependent part of series resistance.
`ther2 (V)`	Denominator of gate voltage dependent part of series resistance.
`thesat (1/V)`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`theth (1/V^3)`	Coefficient of self-heating.
`sdibl (1/|V )`	Drain-induced barrier lowering parameter.
`mo (V)`	Parameter for (short-channel) subthreshold slope.
`ssf (1/|V )`	Static-feedback parameter.
`alp`	Factor of channel length modulation.
`vp (V)`	Characteristic voltage of channel-length modulation.
`mexp`	Smoothing factor.
`phit (V)`	Thermal voltage at the actual temperature.
`a1`	Factor of the weak-avalanche current.
`a2 (V)`	Exponent of the weak-avalanche current.
`a3`	Factor of the drain-source voltage above which weak-avalanche occurs.
`iginv (A/V^2)`	Gain factor for intrinsic gate tunneling current in inversion.
`binv (A/V^2)`	Probability factor for intrinsic gate tunneling current in inversion.
`igacc (A/V^2)`	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc (V)`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov (V)`	Flat-band voltage for the Source/Drain overlap extensions.
`kov ( |V )`	Body-effect factor for the Source/Drain overlap extensions.
`igov (A/V^2)`	Gain factor for Source/Drain overlap tunneling current.
`cox (F)`	Oxide capacitance for the intrinsic channel (* mult).

© 2023 Cadence Design Systems, Inc.

`cgdo (F)`	Oxide capacitance for the gate-drain overlap (* mult).
`cgso (F)`	Oxide capacitance for the gate-source overlap (* mult).
`gatenoise`	Flag for in/exclusion of induced gate thermal noise.
`nt (J)`	Thermal noise coefficient.
`nfa (1/(Vm`^{4}`))`	First coefficient of the flicker noise.
`nfb (1/(Vm`^{2}`))`	Second coefficient of the flicker noise.
`nfc (1/V)`	Third coefficient of the flicker noise.
`tox (m)`	Thickness of gate oxide layer.
`int_s`	
`int_d`	

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).

© 2023 Cadence Design Systems, Inc.

csg (F)	Capacitance (- d qs / d vg).
css (F)	Capacitance (d qs / d vs).
csb (F)	Capacitance (- d qs / d vb).
cbd (F)	Capacitance (- d qb / d vd).
cbg (F)	Capacitance (- d qb / d vg).
cbs (F)	Capacitance (- d qb / d vs).
cbb (F)	Capacitance (d qb / d vb).
cgdol (F)	Gate-drain overlap capacitance of the actual transistor.
cgsol (F)	Gate-source overlap capacitance of the actual transistor.
weff (m)	Effective channel width for geometrical models.
leff (m)	Effective channel length for geometrical models.
u	Transistor gain (gm/gds).
rout (Ω)	Small-signal output resistance (1/gds).
vearly (V)	Equivalent Early voltage (iidl/gds).
keff (V)	Body effect parameter.
beff (A/V^2)	Gain factor.
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw (V/ Hz)	Input-referred RMS white noise voltage density.
sqrtsff (V/ Hz)	Input-referred RMS white noise voltage density at 1 kHz.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
table_ids (A)	Current.
table_vth (V)	Threshold voltage including back-bias and drain-bias effects.
table_qg (Coul)	Charge at g node.
table_qd (Coul)	Charge at d node.

© 2023 Cadence Design Systems, Inc.

table_qb (Coul)	Charge at b node.
mos_region=SUBTHRESHOLD	
diode_region=ON	

Related Topics

Philips Models

Compact MOS-Transistor Distortion Model (mos1000)

Compact MOS-Transistor Distortion Model (mos1100e)

Compact MOS-Transistor Distortion Model (mos1100e)

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	
`trise=0`	Temperature rise from ambient.

Model Syntax

```
model modelName mos1100e parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1.1e+03`	MOS Level.
`paramchk=0`	Level of clip warning info.
`vfb=-1.05 V`	Flat-band voltage for the actual transistor.
`ko=0.5 √V`	Body-effect factor.
`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
`phib=0.95 V`	Surface potential at the onset of strong inversion.
`bet=0.00192(n)/0.000381(p) A/V`^{2}	Gain factor.
`thesr=0.356(n)/0.73(p) 1/V`	Mobility degradation parameter due to surface roughness scattering.
`theph=0.0129(n)/0.001(p) 1/V`	Mobility degradation parameter due to phonon scattering.
`etamob=1.4(n)/3(p)`	Effective field parameter for dependence on depletion charge.
`nu=2`	Exponent of field dependence of mobility model.
`ther=0.0812(n)/0.079(p) 1/V`	Coefficient of series resistance.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`thesat=0.251(n)/0.173(p) 1/V`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`theth=1e-05(n)/0(p) 1/V`^{3}	Coefficient of self-heating.
`sdibl=0.000853(n)/3.55e-05(p) 1/√V`	

© 2023 Cadence Design Systems, Inc.

	Drain-induced barrier lowering parameter.
`mo=0 V`	Parameter for (short-channel) subthreshold slope.
`ssf=0.012(n)/0.01(p) 1/V`	
	Static-feedback parameter.
`alp=0.025`	Factor of channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`mexp=5`	Smoothing factor.
`phit=0.0266 V`	Thermal voltage at the actual temperature.
`a1=6.02(n)/6.86(p)`	
	Factor of the weak-avalanche current.
`a2=38(n)/57.3(p) V`	
	Exponent of the weak-avalanche current.
`a3=0.641(n)/0.425(p)`	
	Factor of the drain-source voltage above which weak-avalanche occurs.
`iginv=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) A/V`^{2}	
	Probability factor for intrinsic gate tunneling current in inversion.
`igacc=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igov=0 A/V`^{2}	Gain factor for Source/Drain overlap tunneling current.
`cox=2.98e-14(n)/2.72e-14(p) F`	
	Oxide capacitance for the intrinsic channel (* mult).

© 2023 Cadence Design Systems, Inc.

`cgdo=6.39e-15(n)/6.36e-15(p) F`	Oxide capacitance for the gate-drain overlap (* mult).
`cgso=6.39e-15(n)/6.36e-15(p) F`	Oxide capacitance for the gate-source overlap (* mult).
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.66e-20 J`	Thermal noise coefficient.
`nfa=8.32e+22(n)/1.9e+22(p) 1/(Vm`^{4}`)`	First coefficient of the flicker noise.
`nfb=2.51e+07(n)/5.04e+06(p) 1/(Vm`^{2}`)`	Second coefficient of the flicker noise.
`nfc=0(n)/3.63e-10(p) 1/V`	Third coefficient of the flicker noise.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.

Output Parameters

`vfb (V)`	Flat-band voltage for the actual transistor.
`ko (`$\sqrt{V}$` )`	Body-effect factor.
`kpinv (1/`$\sqrt{V}$` )`	Inverse of body-effect factor of the poly-silicon gate.
`phib (V)`	Surface potential at the onset of strong inversion.
`bet (A/V`^{2}`)`	Gain factor.
`thesr (1/V)`	Mobility degradation parameter due to surface roughness scattering.
`theph (1/V)`	Mobility degradation parameter due to phonon scattering.

© 2023 Cadence Design Systems, Inc.

`etamob`	Effective field parameter for dependence on depletion charge.
`nu`	Exponent of field dependence of mobility model.
`ther (1/V)`	Coefficient of series resistance.
`ther1 (V)`	Numerator of gate voltage dependent part of series resistance.
`ther2 (V)`	Denominator of gate voltage dependent part of series resistance.
`thesat (1/V)`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`theth` ($1/V^3$)	Coefficient of self-heating.
`sdibl` ($1/\sqrt{V}$)	Drain-induced barrier lowering parameter.
`mo (V)`	Parameter for (short-channel) subthreshold slope.
`ssf` ($1/\sqrt{V}$)	Static-feedback parameter.
`alp`	Factor of channel length modulation.
`vp (V)`	Characteristic voltage of channel-length modulation.
`mexp`	Smoothing factor.
`phit (V)`	Thermal voltage at the actual temperature.
`a1`	Factor of the weak-avalanche current.
`a2 (V)`	Exponent of the weak-avalanche current.
`a3`	Factor of the drain-source voltage above which weak-avalanche occurs.
`iginv` (A/V^2)	Gain factor for intrinsic gate tunneling current in inversion.
`binv` (A/V^2)	Probability factor for intrinsic gate tunneling current in inversion.
`igacc` (A/V^2)	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc (V)`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov (V)`	Flat-band voltage for the Source/Drain overlap extensions.

© 2023 Cadence Design Systems, Inc.

kov (V)	Body-effect factor for the Source/Drain overlap extensions.
igov (A/V^2)	Gain factor for Source/Drain overlap tunneling current.
cox (F)	Oxide capacitance for the intrinsic channel (* mult).
cgdo (F)	Oxide capacitance for the gate-drain overlap (* mult).
cgso (F)	Oxide capacitance for the gate-source overlap (* mult).
gatenoise	Flag for in/exclusion of induced gate thermal noise.
nt (J)	Thermal noise coefficient.
nfa (1/(Vm^4))	First coefficient of the flicker noise.
nfb (1/(Vm^2))	Second coefficient of the flicker noise.
nfc (1/V)	Third coefficient of the flicker noise.
tox (m)	Thickness of gate oxide layer.
int_s	
int_d	

Operating-Point Parameters

ids (A)	Drain current, excluding avalanche and tunnel currents.
iavl (A)	Substrate current due to weak-avalanche.
igs (A)	Gate-to-source current due to direct tunneling.
igd (A)	Gate-to-drain current due to direct tunneling.
igb (A)	Gate-to-bulk current due to direct tunneling.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vsb (V)	Source-bulk voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back-bias effects.
vth (V)	Threshold voltage including back-bias and drain-bias effects.

© 2023 Cadence Design Systems, Inc.

`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgdol (F)`	Gate-drain overlap capacitance of the actual transistor.
`cgsol (F)`	Gate-source overlap capacitance of the actual transistor.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|idl|/gds).

© 2023 Cadence Design Systems, Inc.

keff (V)	Body effect parameter.
beff (A/V^2)	Gain factor.
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw (V/Hz)	Input-referred RMS white noise voltage density.
sqrtsff (V/Hz)	Input-referred RMS white noise voltage density at 1 kHz.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
table_ids (A)	Current.
table_vth (V)	Threshold voltage including back-bias and drain-bias effects.
table_qg (Coul)	Charge at g node.
table_qd (Coul)	Charge at d node.
table_qb (Coul)	Charge at b node.
mos_region=SUBTHRESHOLD	
diode_region=ON	

Related Topics

Philips Models

Compact MOS-Transistor Distortion Model (mos1000)

Compact MOS-Transistor Distortion Model (mos1100)

MOS Model 11, Level 1101 (mos11010)

This is SimKit 5.2.

© 2023 Cadence Design Systems, Inc.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
`nf=1`	Number of fingers.
`ngcon=1`	Number of gate contacts.
`xgw=1e-07 m`	Distance from the gate contact to the channel edge.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos11010 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1.1e+04`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=4e-08 m`	Effective channel length reduction per side.
`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 C`	Reference temperature.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of VFB.
`kor=0.5 V`	Body effect coefficient for the reference transistor.
`slko=0`	Coefficient of the length dependence of KO.
`sl2ko=0`	Second coefficient of the length dependence of KO.
`sl3ko=0`	Third coefficient of the length dependence of KO.
`sl3koexp=1`	Exponent belonging to the third coefficient of the length dependence of KO.
`swko=0`	Coefficient of the width dependence of KO.
`kpinv=0 1/V`	Inverse of body-effect factor of the poly-silicon gate.
`phibr=0.95 V`	Surface potential at strong inversion.
`stphib=-0.00085 V/K`	Coefficient of the temperature dependency of PHIB.
`slphib=0`	Coefficient of the length dependence of PHIB.
`sl2phib=0`	Second coefficient of the length dependence of PHIB.
`swphib=0`	Coefficient of the width dependence of PHIB.

© 2023 Cadence Design Systems, Inc.

`betsq=0.000371(n)/ 0.000115(p) A/V`^{2}	
	Gain factor for an infinite square transistor.
`etabetr=1.3(n)/ 0.5(p)`	
	Exponent of the temperature dependence of the gain factor.
`sletabet=0`	Coefficient of length dependence of ETABETR.
`fbet1=0`	Relative mobility decrease due to first lateral profile.
`lp1=8e-07 m`	Characteristic length of first lateral profile.
`fbet2=0`	Relative mobility decrease due to second lateral profile.
`lp2=8e-07 m`	Characteristic length of second lateral profile.
`thesrr=0.4(n)/ 0.73(p) 1/V`	
	Coefficient of the mobility reduction due to surface roughness scattering.
`etasr=0.65(n)/0.5(p)`	
	Exponent of the temperature dependence of THESR.
`swthesr=0`	Coefficient of the width dependence of THESR.
`thephr=0.0129(n)/ 0.001(p) 1/V`	
	Coefficient of the mobility reduction due to phonon scattering.
`etaph=1.35(n)/ 3.75(p)`	
	Exponent of the temperature dependence of THEPH.
`swtheph=0`	Coefficient of the width dependence of THEPH.
`etamobr=1.4(n)/3(p)`	
	Effective field parameter for dependence on depletion/ inversion charge.

© 2023 Cadence Design Systems, Inc.

stetamob=0 1/K	Coefficient of the temperature dependence of ETAMOB.
swetamob=0	Coefficient of the width dependence of ETAMOB.
nu=2	Exponent of field dependence of mobility model.
nuexp=5.25(n)/ 3.23(p)	Exponent of the temperature dependence of parameter NU.
therr=0.155(n)/ 0.08(p) 1/V	Coefficient of the series resistance.
etar=0.95(n)/0.4(p)	Exponent of the temperature dependence of THER.
swther=0	Coefficient of the width dependence of THER.
ther1=0 V	Numerator of gate voltage dependent part of series resistance.
ther2=1 V	Denominator of gate voltage dependent part of series resistance.
thesatr=0.5(n)/ 0.2(p) 1/V	Velocity saturation parameter due to optical/acoustic phonon scattering.
etasat=1.04(n)/ 0.86(p)	Exponent of the temperature dependence of THESAT.
slthesat=1	Coefficient of length dependence of THESAT.
thesatexp=1	Exponent of length dependence of THESAT.
swthesat=0	Coefficient of the width dependence of THESAT.
thethr=0.001(n)/ 0.0005(p) 1/V^3	Coefficient of self-heating.
thethexp=1	Exponent of the length dependence of THETH.

© 2023 Cadence Design Systems, Inc.

swtheth=0	Coefficient of the width dependence of THETH.
sdiblo=0.0001 1/V	Drain-induced barrier lowering parameter.
sdiblexp=1.35	Exponent of the length dependence of SDIBL.
moo=0	Parameter for short-channel subthreshold slope.
mor=0	Parameter for short-channel subthreshold slope per unit length.
moexp=1.34	Exponent of the length dependence of MO.
ssfr=0.00625 1/V	Static feedback parameter.
slssf=1	Coefficient of the length dependence of SSF.
swssf=0	Coefficient of the width dependence of SSF.
alpr=0.01	Factor of the channel length modulation.
slalp=1	Coefficient of the length dependence of ALP.
alpexp=1	Exponent of the length dependence of ALP.
swalp=0	Coefficient of the width dependence of ALP.
vp=0.05 V	Characteristic voltage of channel-length modulation.
lmin=1.5e-07 m	Minimum effective channel length in technology, used for calculation of smoothing factor m.
a1r=6	Factor of the weak-avalanche current.
sta1=0 1/K	Coefficient of the temperature dependence of A1.
sla1=0	Coefficient of the length dependence of A1.
swa1=0	Coefficient of the width dependence of A1.
a2r=38 V	Exponent of the weak-avalanche current.
sla2=0	Coefficient of the length dependence of A2.
swa2=0	Coefficient of the width dependence of A2.
a3r=1	Factor of the drain-source voltage above which weak-avalanche occurs.
sla3=0	Coefficient of the length dependence of A3.
swa3=0	Coefficient of the width dependence of A3.

© 2023 Cadence Design Systems, Inc.

iginvr=0 A/V^2	Gain factor for intrinsic gate tunneling current in inversion.
binv=48(n)/87.5(p) V	Probability factor for intrinsic gate tunneling current in inversion.
igaccr=0 A/V^2	Gain factor for intrinsic gate tunneling current in accumulation.
bacc=48 V	Probability factor for intrinsic gate tunneling current in accumulation.
vfbov=0 V	Flat-band voltage for the Source/Drain overlap extensions.
kov=2.5 V	Body-effect factor for the Source/Drain overlap extensions.
igovr=0 A/V^2	Gain factor for Source/Drain overlap gate tunneling current.
agidlr=0 A/V^3	Gain factor for gate-induced leakage current.
bgidl=41 V	Probability factor for gate-induced drain leakage current at reference temperature.
stbgidl=-0.000364 V/K	Coefficient of the temperature dependence of BGIDL.
cgidl=0	Factor for the lateral field dependence of the gate-induced leakage current.
tox=3.2e-09 m	Thickness of gate oxide layer.
col=3.2e-16 F	Gate overlap capacitance for a channel width of 1 um.
gatenoise=0	Flag for in/exclusion of induced gate thermal noise.
nt=1.62e-20 J	Thermal noise coefficient.
nfar=1.57e+23(n)/3.83e+24(p) 1/(Vm^4)	First coefficient of the flicker noise for a channel area of 1 um^2.
nfbr=4.75e+09(n)/1.02e+09(p) 1/(Vm^2)	

© 2023 Cadence Design Systems, Inc.

	Second coefficient of the flicker noise for a channel area of 1 um^2.
nfcr=0(n)/7.3e-08(p) 1/V	
	Third coefficient of the flicker noise for a channel area of 1 um^2.
dta=0 K	Temperature offset of the device.
rgo=0 Ω	Gate resistance.
rint=0 Ω m^2	Contact resistance between silicide and poly.
rvpoly=0 Ω m^2	Vertical poly resistance.
rshg=0 Ω/Sqr	Gate electrode diffusion sheet resistance.
dlsil=0 m	Silicide extension over the physical gate length.
binning=0	flag for eldo model.
type=n	Transistor gender. Possible values are n and p.
imax=1000 A	Explosion current.
tnom (C)	alias of tnom.
tref (C)	alias of tnom.
compatible=spectre	
	Encourage device equations to be compatible with a foreign simulator. Possible values are spectre, spice2, spice3, cdsspice, spiceplus, eldo, sspice, mica, and pspice.

Output Parameters

tempeff (C)	Effective temperature for a single device.
meff	Effective multiplicity factor (m-factor).
int_s	
int_d	

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).

© 2023 Cadence Design Systems, Inc.

csd (F)	Capacitance (- d qs / d vd).
csg (F)	Capacitance (- d qs / d vg).
css (F)	Capacitance (d qs / d vs).
csb (F)	Capacitance (- d qs / d vb).
cbd (F)	Capacitance (- d qb / d vd).
cbg (F)	Capacitance (- d qb / d vg).
cbs (F)	Capacitance (- d qb / d vs).
cbb (F)	Capacitance (d qb / d vb).
cgdol (F)	Gate-drain overlap capacitance of the actual transistor.
cgsol (F)	Gate-source overlap capacitance of the actual transistor.
weff (m)	Effective channel width for geometrical models.
leff (m)	Effective channel length for geometrical models.
rg (Ω)	Gate resistance.
u	Transistor gain (gm/gds).
rout (Ω)	Small-signal output resistance (1/gds).
vearly (V)	Equivalent Early voltage (iidl/gds).
keff (V)	Body effect parameter.
beff (A/V^2)	Gain factor.
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw (V/ Hz)	Input-referred RMS white noise voltage density.
sqrtsff (V/ Hz)	Input-referred RMS white noise voltage density at 1 kHz.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
ctype	Channel type (-1 for PMOS, +1 for NMOS).
von (V)	Signed vth (<0 for PMOS, >0 for NMOS).
table_ids (A)	Current.

© 2023 Cadence Design Systems, Inc.

`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`table_qg (Coul)`	Charge at g node.
`table_qd (Coul)`	Charge at d node.
`table_qb (Coul)`	Charge at b node.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Related Topics

Philips Models

MOS Model 11, Level 1101 (mos11010t)

MOS Model 11, Level 1101 (mos11011)

MOS Model 11, Level 1101 (mos11011t)

MOS Model 11, Level 1101 (mos11010t)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
`nf=1`	Number of fingers.
`ngcon=1`	Number of gate contacts.
`xgw=1e-07 m`	Distance from the gate contact to the channel edge.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos11010t parameter=value ...
```

Model Parameters

`level=1.1e+04`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.

© 2023 Cadence Design Systems, Inc.

`tmin=0 s`	Ovcheck tmin value.
`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=4e-08 m`	Effective channel length reduction per side.
`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 C`	Reference temperature.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of VFB.
`kor=0.5 √V`	Body effect coefficient for the reference transistor.
`slko=0`	Coefficient of the length dependence of KO.
`sl2ko=0`	Second coefficient of the length dependence of KO.
`sl3ko=0`	Third coefficient of the length dependence of KO.
`sl3koexp=1`	Exponent belonging to the third coefficient of the length dependence of KO.
`swko=0`	Coefficient of the width dependence of KO.
`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
`phibr=0.95 V`	Surface potential at strong inversion.
`stphib=-0.00085 V/K`	Coefficient of the temperature dependency of PHIB.
`slphib=0`	Coefficient of the length dependence of PHIB.
`sl2phib=0`	Second coefficient of the length dependence of PHIB.
`swphib=0`	Coefficient of the width dependence of PHIB.
`betsq=0.000371(n)/0.000115(p) A/V`^{2}	Gain factor for an infinite square transistor.
`etabetr=1.3(n)/0.5(p)`	Exponent of the temperature dependence of the gain factor.
`sletabet=0`	Coefficient of length dependence of ETABETR.

© 2023 Cadence Design Systems, Inc.

`fbet1=0`	Relative mobility decrease due to first lateral profile.
`lp1=8e-07 m`	Characteristic length of first lateral profile.
`fbet2=0`	Relative mobility decrease due to second lateral profile.
`lp2=8e-07 m`	Characteristic length of second lateral profile.
`thesrr=0.4(n)/0.73(p) 1/V`	Coefficient of the mobility reduction due to surface roughness scattering.
`etasr=0.65(n)/0.5(p)`	Exponent of the temperature dependence of THESR.
`swthesr=0`	Coefficient of the width dependence of THESR.
`thephr=0.0129(n)/0.001(p) 1/V`	Coefficient of the mobility reduction due to phonon scattering.
`etaph=1.35(n)/3.75(p)`	Exponent of the temperature dependence of THEPH.
`swtheph=0`	Coefficient of the width dependence of THEPH.
`etamobr=1.4(n)/3(p)`	Effective field parameter for dependence on depletion/ inversion charge.
`stetamob=0 1/K`	Coefficient of the temperature dependence of ETAMOB.
`swetamob=0`	Coefficient of the width dependence of ETAMOB.
`nu=2`	Exponent of field dependence of mobility model.
`nuexp=5.25(n)/3.23(p)`	Exponent of the temperature dependence of parameter NU.
`therr=0.155(n)/0.08(p) 1/V`	Coefficient of the series resistance.
`etar=0.95(n)/0.4(p)`	Exponent of the temperature dependence of THER.

© 2023 Cadence Design Systems, Inc.

`swther=0`	Coefficient of the width dependence of THER.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`thesatr=0.5(n)/0.2(p) 1/V`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`etasat=1.04(n)/0.86(p)`	Exponent of the temperature dependence of THESAT.
`slthesat=1`	Coefficient of length dependence of THESAT.
`thesatexp=1`	Exponent of length dependence of THESAT.
`swthesat=0`	Coefficient of the width dependence of THESAT.
`thethr=0.001(n)/0.0005(p) 1/V`^{3}	Coefficient of self-heating.
`thethexp=1`	Exponent of the length dependence of THETH.
`swtheth=0`	Coefficient of the width dependence of THETH.
`sdiblo=0.0001 1/V`	Drain-induced barrier lowering parameter.
`sdiblexp=1.35`	Exponent of the length dependence of SDIBL.
`moo=0`	Parameter for short-channel subthreshold slope.
`mor=0`	Parameter for short-channel subthreshold slope per unit length.
`moexp=1.34`	Exponent of the length dependence of MO.
`ssfr=0.00625 1/V`	Static feedback parameter.
`slssf=1`	Coefficient of the length dependence of SSF.
`swssf=0`	Coefficient of the width dependence of SSF.
`alpr=0.01`	Factor of the channel length modulation.
`slalp=1`	Coefficient of the length dependence of ALP.

© 2023 Cadence Design Systems, Inc.

`alpexp=1`	Exponent of the length dependence of ALP.
`swalp=0`	Coefficient of the width dependence of ALP.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`lmin=1.5e-07 m`	Minimum effective channel length in technology, used for calculation of smoothing factor m.
`a1r=6`	Factor of the weak-avalanche current.
`sta1=0 1/K`	Coefficient of the temperature dependence of A1.
`sla1=0`	Coefficient of the length dependence of A1.
`swa1=0`	Coefficient of the width dependence of A1.
`a2r=38 V`	Exponent of the weak-avalanche current.
`sla2=0`	Coefficient of the length dependence of A2.
`swa2=0`	Coefficient of the width dependence of A2.
`a3r=1`	Factor of the drain-source voltage above which weak-avalanche occurs.
`sla3=0`	Coefficient of the length dependence of A3.
`swa3=0`	Coefficient of the width dependence of A3.
`iginvr=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) V`	Probability factor for intrinsic gate tunneling current in inversion.
`igaccr=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igovr=0 A/V`^{2}	Gain factor for Source/Drain overlap gate tunneling current.
`agidlr=0 A/V`^{3}	Gain factor for gate-induced leakage current.

© 2023 Cadence Design Systems, Inc.

`bgidl=41 V`	Probability factor for gate-induced drain leakage current at reference temperature.
`stbgidl=-0.000364 V/K`	Coefficient of the temperature dependence of BGIDL.
`cgidl=0`	Factor for the lateral field dependence of the gate-induced leakage current.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`col=3.2e-16 F`	Gate overlap capacitance for a channel width of 1 um.
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`nfar=1.57e+23(n)/3.83e+24(p) 1/(Vm`^{4}`)`	First coefficient of the flicker noise for a channel area of 1 um^2.
`nfbr=4.75e+09(n)/1.02e+09(p) 1/(Vm`^{2}`)`	Second coefficient of the flicker noise for a channel area of 1 um^2.
`nfcr=0(n)/7.3e-08(p) 1/V`	Third coefficient of the flicker noise for a channel area of 1 um^2.
`dta=0 K`	Temperature offset of the device.
`rgo=0` Ω	Gate resistance.
`rint=0` Ω `m`^{2}	Contact resistance between silicide and poly.
`rvpoly=0` Ω `m`^{2}	Vertical poly resistance.
`rshg=0` Ω`/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0 m`	Silicide extension over the physical gate length.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`binning=0`	flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.

© 2023 Cadence Design Systems, Inc.

`imax=1000 A`	Explosion current.
`tnom (C)`	alias of tnom.
`tref (C)`	alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`int_s`	
`int_d`	

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).

© 2023 Cadence Design Systems, Inc.

cds (F)	Capacitance (- d qd / d vs).
cdb (F)	Capacitance (- d qd / d vb).
cgd (F)	Capacitance (- d qg / d vd).
cgg (F)	Capacitance (d qg / d vg).
cgs (F)	Capacitance (- d qg / d vs).
cgb (F)	Capacitance (- d qg / d vb).
csd (F)	Capacitance (- d qs / d vd).
csg (F)	Capacitance (- d qs / d vg).
css (F)	Capacitance (d qs / d vs).
csb (F)	Capacitance (- d qs / d vb).
cbd (F)	Capacitance (- d qb / d vd).
cbg (F)	Capacitance (- d qb / d vg).
cbs (F)	Capacitance (- d qb / d vs).
cbb (F)	Capacitance (d qb / d vb).
cgdol (F)	Gate-drain overlap capacitance of the actual transistor.
cgsol (F)	Gate-source overlap capacitance of the actual transistor.
weff (m)	Effective channel width for geometrical models.
leff (m)	Effective channel length for geometrical models.
rg (Ω)	Gate resistance.
u	Transistor gain (gm/gds).
rout (Ω)	Small-signal output resistance (1/gds).
vearly (V)	Equivalent Early voltage (iidl/gds).
keff ($\sqrt{V}$)	Body effect parameter.
beff (A/V^2)	Gain factor.
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw ($V/\sqrt{Hz}$)	Input-referred RMS white noise voltage density.
sqrtsff ($V/\sqrt{Hz}$)	

© 2023 Cadence Design Systems, Inc.

	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual device temperature.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`von (V)`	Signed vth (<0 for PMOS, >0 for NMOS).
`table_ids (A)`	Current.
`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`table_qg (Coul)`	Charge at g node.
`table_qd (Coul)`	Charge at d node.
`table_qb (Coul)`	Charge at b node.
`pwr (W)`	Power.
`mos_region`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.
`diode_region=ON`	DIODE region. Possible values are `off` and `on`.

Related Topics

Philips Models

MOS Model 11, Level 1101 (mos11010)

MOS Model 11, Level 1101 (mos11011)

MOS Model 11, Level 1101 (mos11011t)

MOS Model 11, Level 1101 (mos11011)

This is SimKit 5.0.

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
`nf=1`	Number of fingers.
`ngcon=1`	Number of gate contacts.
`xgw=1e-07 m`	Distance from the gate contact to the channel edge.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos11011 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1.1e+04`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=4e-08 m`	Effective channel length reduction per side.
`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 C`	Reference temperature.
`lmin=0 m`	Device length low limit for binning selection.
`lmax=1 m`	Device length high limit for binning selection.
`wmin=0 m`	Device width low limit for binning selection.
`wmax=1 m`	Device width high limit for binning selection.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`poko=0.5 √V`	Coefficient for the geometry-independent part of KO.
`plko=0 √V`	Coefficient for the length dependence of KO.
`pwko=0 √V`	Coefficient for the width dependence of KO.
`plwko=0 √V`	Coefficient for the length times width dependence of KO.
`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
`pophib=0.95 V`	Coefficient for the geometric independent part of PHIB.
`plphib=0 V`	Coefficient for the length dependence of PHIB.
`pwphib=0 V`	Coefficient for the width dependence of PHIB.
`plwphib=0 V`	Coefficient for the length times width dependence of PHIB.
`pobet=0.00192(n)/0.000381(p) A/V`^{2}	

© 2023 Cadence Design Systems, Inc.

	Coefficient for the geometry-independent part of BET.
`plbet=0 A/V`^{2}	Coefficient for the length dependence of BET.
`pwbet=0 A/V`^{2}	Coefficient for the width dependence of BET.
`plwbet=0 A/V`^{2}	Coefficient for the width over length dependence of BET.
`pothesr=0.356(n)/0.73(p) 1/V`	
	Coefficient of the geometry-independent part of THESR.
`plthesr=0 1/V`	Coefficient of the length dependence of THESR.
`pwthesr=0 1/V`	Coefficient of the width dependence of THESR.
`plwthesr=0 1/V`	Coefficient of the length times width dependence of THESR.
`potheph=0.0129(n)/0.001(p) 1/V`	
	Coefficient of the geometry-independent part of THEPH.
`pltheph=0 1/V`	Coefficient of the length dependence of THEPH.
`pwtheph=0 1/V`	Coefficient of the width dependence of THEPH.
`plwtheph=0 1/V`	Coefficient of the length times width dependence of THEPH.
`poetamob=1.4(n)/3(p)`	
	Coefficient of the geometry-independent part of ETAMOB.
`pletamob=0`	Coefficient of the length dependence of ETAMOB.
`pwetamob=0`	Coefficient of the width dependence of ETAMOB.
`plwetamob=0`	Coefficient of the length times width dependence of ETAMOB.
`pother=0.0812(n)/0.079(p) 1/V`	
	Coefficient of the geometry-independent part of THER.
`plther=0 1/V`	Coefficient of the length dependence of THER.
`pwther=0 1/V`	Coefficient of the width dependence of THER.

© 2023 Cadence Design Systems, Inc.

`plwther=0 1/V`	Coefficient of the length times width dependence of THER.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`pothesat=0.251(n)/0.173(p) 1/V`	Coefficient of the geometry-independent part of THESAT.
`plthesat=0 1/V`	Coefficient of the length dependence of THESAT.
`pwthesat=0 1/V`	Coefficient of the width dependence of THESAT.
`plwthesat=0 1/V`	Coefficient of the length times width dependence of THESAT.
`potheth=1e-05(n)/0(p) 1/V`^{3}	Coefficient of the geometry-independent part of THETH.
`pltheth=0 1/V`^{3}	Coefficient of the length dependence of THETH.
`pwtheth=0 1/V`^{3}	Coefficient of the width dependence of THETH.
`plwtheth=0 1/V`^{3}	Coefficient of the length times width dependence of THETH.
`posdibl=0.000853(n)/3.55e-05(p) 1/|V`	Coefficient of the geometry-independent part of SDIBL.
`plsdibl=0 1/|V`	Coefficient of the length dependence of SDIBL.
`pwsdibl=0 1/|V`	Coefficient of the width dependence of SDIBL.
`plwsdibl=0 1/|V`	Coefficient of the length times width dependence of SDIBL.
`pomo=0`	Coefficient of the geometry-independent part of MO.
`plmo=0`	Coefficient of the length dependence of MO.

© 2023 Cadence Design Systems, Inc.

pwmo=0	Coefficient of the width dependence of MO.
plwmo=0	Coefficient of the length times width dependence of MO.
possf=0.012(n)/0.01(p) 1/√V	Coefficient of the geometry-independent part of SSF.
plssf=0 1/√V	Coefficient of the length dependence of SSF.
pwssf=0 1/√V	Coefficient of the width dependence of SSF.
plwssf=0 1/√V	Coefficient of the length times width dependence of SSF.
poalp=0.025	Coefficient of the geometry-independent part of ALP.
plalp=0	Coefficient of the length dependence of ALP.
pwalp=0	Coefficient of the width dependence of ALP.
plwalp=0	Coefficient of the length times width dependence of ALP.
vp=0.05 V	Characteristic voltage of channel-length modulation.
pomexp=0.2	Coefficient of the geometry-independent part of MEXP.
plmexp=0	Coefficient of the length dependence of MEXP.
pwmexp=0	Coefficient of the width dependence of MEXP.
plwmexp=0	Coefficient of the length times width dependence of MEXP.
poa1=6.02(n)/6.86(p)	Coefficient of the geometry-independent part of A1.
pla1=0	Coefficient of the length dependence of A1.
pwa1=0	Coefficient of the width dependence of A1.
plwa1=0	Coefficient of the length times width dependence of A1.
poa2=38(n)/57.3(p) V	Coefficient of the geometry-independent part of A2.
pla2=0 V	Coefficient of the length dependence of A2.

© 2023 Cadence Design Systems, Inc.

`pwa2=0 V`	Coefficient of the width dependence of A2.
`plwa2=0 V`	Coefficient of the length times width dependence of A2.
`poa3=0.641(n)/0.425(p)`	Coefficient of the geometry-independent part of A3.
`pla3=0`	Coefficient of the length dependence of A3.
`pwa3=0`	Coefficient of the width dependence of A3.
`plwa3=0`	Coefficient of the length times width dependence of A3.
`poiginv=0 A/V`^{2}	Coefficient of the geometry-independent part of IGINV.
`pliginv=0 A/V`^{2}	Coefficient of the length dependence of IGINV.
`pwiginv=0 A/V`^{2}	Coefficient of the width dependence of IGINV.
`plwiginv=0 A/V`^{2}	Coefficient of the length times width dependence of IGINV.
`pobinv=48(n)/87.5(p) V`	Coefficient of the geometry-independent part of BINV.
`plbinv=0 V`	Coefficient of the length dependence of BINV.
`pwbinv=0 V`	Coefficient of the width dependence of BINV.
`plwbinv=0 V`	Coefficient of the length times width dependence of BINV.
`poigacc=0 A/V`^{2}	Coefficient of the geometry-independent part of IGACC.
`pligacc=0 A/V`^{2}	Coefficient of the length dependence of IGACC.
`pwigacc=0 A/V`^{2}	Coefficient of the width dependence of IGACC.
`plwigacc=0 A/V`^{2}	Coefficient of the length times width dependence of IGACC.
`pobacc=48 V`	Coefficient of the geometry-independent part of BACC.
`plbacc=0 V`	Coefficient of the length dependence of BACC.
`pwbacc=0 V`	Coefficient of the width dependence of BACC.
`plwbacc=0 V`	Coefficient of the length times width dependence of BACC.

© 2023 Cadence Design Systems, Inc.

`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`poigov=0` A/V^2	Coefficient of the geometry-independent part of IGOV.
`pligov=0` A/V^2	Coefficient of the length dependence of IGOV.
`pwigov=0` A/V^2	Coefficient of the width dependence of IGOV.
`plwigov=0` A/V^2	Coefficient of the length times width dependence of IGOV.
`poagidl=0` A/V^3	Coefficient of the geometry-independent part of AGIDL.
`plagidl=0` A/V^3	Coefficient of the length dependence of AGIDL.
`pwagidl=0` A/V^3	Coefficient of the width dependence of AGIDL.
`plwagidl=0` A/V^3	Coefficient of the length times width dependence of AGIDL.
`pobgidl=41 V`	Coefficient of the geometry-independent part of BGIDL.
`plbgidl=0 V`	Coefficient of the length dependence of BGIDL.
`pwbgidl=0 V`	Coefficient of the width dependence of BGIDL.
`plwbgidl=0 V`	Coefficient of the length times width dependence of BGIDL.
`pocgidl=0`	Coefficient of the geometry-independent part of CGIDL.
`plcgidl=0`	Coefficient of the length dependence of CGIDL.
`pwcgidl=0`	Coefficient of the width dependence of CGIDL.
`plwcgidl=0`	Coefficient of the length times width dependence of CGIDL.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`pocox=2.98e-14(n)/2.72e-14(p) F`	Coefficient of the geometry-independent part of COX.
`plcox=0 F`	Coefficient of the length dependence of COX.
`pwcox=0 F`	Coefficient of the width dependence of COX.

© 2023 Cadence Design Systems, Inc.

`plwcox=0 F`	Coefficient of the length times width dependence of COX.
`pocgdo=6.39e-15(n)/ 6.36e-15(p) F`	Coefficient of the geometry-independent part of CGDO.
`plcgdo=0 F`	Coefficient of the length dependence of CGDO.
`pwcgdo=0 F`	Coefficient of the width dependence of CGDO.
`plwcgdo=0 F`	Coefficient of the length time width dependence of CGDO.
`pocgso=6.39e-15(n)/6.36e-15(p) F`	Coefficient of the geometry-independent part of CGSO.
`plcgso=0 F`	Coefficient of the length dependence of CGSO.
`pwcgso=0 F`	Coefficient of the width dependence of CGSO.
`plwcgso=0 F`	Coefficient of the length times width dependence of CGSO.
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`ponfa=8.32e+22(n)/1.9e+22(p) 1/V m`^{4}	Coefficient of the geometry-independent part of NFA.
`plnfa=0 1/V m`^{4}	Coefficient of the length dependence of NFA.
`pwnfa=0 1/V m`^{4}	Coefficient of the width dependence of NFA.
`plwnfa=0 1/V m`^{4}	Coefficient of the length times width dependence of NFA.
`ponfb=2.51e+07(n)/5.04e+06(p) 1/V m`^{2}	Coefficient of the geometry-independent part of NFB.
`plnfb=0 1/V m`^{2}	Coefficient of the length dependence of NFB.
`pwnfb=0 1/V m`^{2}	Coefficient of the width dependence of NFB.
`plwnfb=0 1/V m`^{2}	Coefficient of the length times width dependence of NFB.

© 2023 Cadence Design Systems, Inc.

`ponfc=0(n)/3.63e-10(p) 1/V`	
	Coefficient of the geometry-independent part of NFC.
`plnfc=0 1/V`	Coefficient of the length dependence of NFC.
`pwnfc=0 1/V`	Coefficient of the width dependence of NFC.
`plwnfc=0 1/V`	Coefficient of the length times width dependence of NFC.
`potvfb=0.0005 V/K`	Coefficient of the geometry-independent part of STVFB.
`pltvfb=0 V/K`	Coefficient of the length dependence of STVFB.
`pwtvfb=0 V/K`	Coefficient of the width dependence of STVFB.
`plwtvfb=0 V/K`	Coefficient of the length times width dependence of STVFB.
`potphib=-0.00085 V/K`	
	Coefficient of the geometry-independent part of STPHIB.
`pltphib=0 V/K`	Coefficient of the length dependence of STPHIB.
`pwtphib=0 V/K`	Coefficient of the width dependence of STPHIB.
`plwtphib=0 V/K`	Coefficient of the length times width dependence of STPHIB.
`potetabet=1.3(n)/0.5(p)`	
	Coefficient of the geometry-independent part of ETABET.
`pltetabet=0`	Coefficient of the length dependence of ETABET.
`pwtetabet=0`	Coefficient of the width dependence of ETABET.
`plwtetabet=0`	Coefficient of the length times width dependence of ETABET.
`potetasr=0.65(n)/0.5(p)`	
	Coefficient of the geometry-independent part of ETASR.
`pltetasr=0`	Coefficient of the length dependence of ETASR.
`pwtetasr=0`	Coefficient of the width dependence of ETASR.

© 2023 Cadence Design Systems, Inc.

plwtetasr=0	Coefficient of the length times width dependence of ETASR.
potetaph=1.35(n)/3.75(p)	Coefficient of the geometry-independent part of ETAPH.
pltetaph=0	Coefficient of the length dependence of ETAPH.
pwtetaph=0	Coefficient of the width dependence of ETAPH.
plwtetaph=0	Coefficient of the length times width dependence of ETAPH.
potetamob=0 1/K	Coefficient of the geometry-independent part of STETAMOB.
pltetamob=0 1/K	Coefficient of the length dependence of STETAMOB.
pwtetamob=0 1/K	Coefficient of the width dependence of STETAMOB.
plwtetamob=0 1/K	Coefficient of the length times width dependence of STETAMOB.
nu=2	Exponent of field dependence of mobility model.
potnuexp=5.25(n)/3.23(p)	Coefficient of the geometry-independent part of NUEXP.
pltnuexp=0	Coefficient of the length dependence of NUEXP.
pwtnuexp=0	Coefficient of the width dependence of NUEXP.
plwtnuexp=0	Coefficient of the length times width dependence of NUEXP.
potetar=0.95(n)/0.4(p)	Coefficient of the geometry-independent part of ETAR.
pltetar=0	Coefficient of the length dependence of ETAR.
pwtetar=0	Coefficient of the width dependence of ETAR.
plwtetar=0	Coefficient of the length times width dependence of ETAR.
potetasat=1.04(n)/ 0.86(p)	

© 2023 Cadence Design Systems, Inc.

	Coefficient of the geometry-independent part of ETASAT.
`pltetasat=0`	Coefficient of the length dependence of ETASAT.
`pwtetasat=0`	Coefficient of the width dependence of ETASAT.
`plwtetasat=0`	Coefficient of the length times width dependence of ETASAT.
`pota1=0 1/K`	Coefficient of the geometry-independent part of STA1.
`plta1=0 1/K`	Coefficient of the length dependence of STA1.
`pwta1=0 1/K`	Coefficient of the width dependence of STA1.
`plwta1=0 1/K`	Coefficient of the length times width dependence of STA1.
`potbgidl=-0.000364 V/K`	
	Coefficient of the geometry-independent part of STBGIDL.
`pltbgidl=0 V/K`	Coefficient of the length dependence of STBGIDL.
`pwtbgidl=0 V/K`	Coefficient of the width dependence of STBGIDL.
`plwtbgidl=0 V/K`	Coefficient of the length times width dependence of STBGIDL.
`dta=0 K`	Temperature offset of the device.
`rgo=0` Ω	Gate resistance.
`rint=0` Ω m^2	Contact resistance between silicide and poly.
`rvpoly=0` Ω m^2	Vertical poly resistance.
`rshg=0` Ω`/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0 m`	Silicide extension over the physical gate length.
`binning=0`	flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`tnom (C)`	alias of tnom.
`tref (C)`	alias of tnom.
`compatible=spectre`	

© 2023 Cadence Design Systems, Inc.

	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`int_s`	
`int_d`	

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).

© 2023 Cadence Design Systems, Inc.

`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgdol (F)`	Gate-drain overlap capacitance of the actual transistor.
`cgsol (F)`	Gate-source overlap capacitance of the actual transistor.
`weff (m)`	Effective channel width for geometrical models.
`leff (m)`	Effective channel length for geometrical models.
`rg (Ω)`	Gate resistance.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|idl/gds).
`keff (√V )`	Body effect parameter.
`beff (A/V^2)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`sqrtsfw (V/√Hz )`	Input-referred RMS white noise voltage density.
`sqrtsff (V/√Hz )`	

© 2023 Cadence Design Systems, Inc.

	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`BET (A/V`^{2}`)`	Gain factor.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`von (V)`	Signed vth (<0 for PMOS, >0 for NMOS).
`table_ids (A)`	Current.
`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`table_qg (Coul)`	Charge at g node.
`table_qd (Coul)`	Charge at d node.
`table_qb (Coul)`	Charge at b node.
`mos_region=SUBTHRESHOLD`	
	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.
`diode_region=ON`	DIODE region. Possible values are `off` and `on`.

Related Topics

Philips Models

MOS Model 11, Level 1101 (mos11010t)

MOS Model 11, Level 1101 (mos11010)

MOS Model 11, Level 1101 (mos11011t)

MOS Model 11, Level 1101 (mos11011t)

This is SimKit 5.2.

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
`nf=1`	Number of fingers.
`ngcon=1`	Number of gate contacts.
`xgw=1e-07 m`	Distance from the gate contact to the channel edge.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
0 `m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos11011t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1.1e+04`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=4e-08 m`	Effective channel length reduction per side.
`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 C`	Reference temperature.
`lmin=0 m`	Device length low limit for binning selection.
`lmax=1 m`	Device length high limit for binning selection.
`wmin=0 m`	Device width low limit for binning selection.
`wmax=1 m`	Device width high limit for binning selection.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`poko=0.5 √V`	Coefficient for the geometry-independent part of KO.
`plko=0 √V`	Coefficient for the length dependence of KO.
`pwko=0 √V`	Coefficient for the width dependence of KO.
`plwko=0 √V`	Coefficient for the length times width dependence of KO.
`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
`pophib=0.95 V`	Coefficient for the geometric independent part of PHIB.
`plphib=0 V`	Coefficient for the length dependence of PHIB.
`pwphib=0 V`	Coefficient for the width dependence of PHIB.
`plwphib=0 V`	Coefficient for the length times width dependence of PHIB.
`pobet=0.00192(n)/0.000381(p) A/V`^{2}	

© 2023 Cadence Design Systems, Inc.

	Coefficient for the geometry-independent part of BET.
`plbet=0 A/V`^{2}	Coefficient for the length dependence of BET.
`pwbet=0 A/V`^{2}	Coefficient for the width dependence of BET.
`plwbet=0 A/V`^{2}	Coefficient for the width over length dependence of BET.
`pothesr=0.356(n)/0.73(p) 1/V`	
	Coefficient of the geometry-independent part of THESR.
`plthesr=0 1/V`	Coefficient of the length dependence of THESR.
`pwthesr=0 1/V`	Coefficient of the width dependence of THESR.
`plwthesr=0 1/V`	Coefficient of the length times width dependence of THESR.
`potheph=0.0129(n)/0.001(p) 1/V`	
	Coefficient of the geometry-independent part of THEPH.
`pltheph=0 1/V`	Coefficient of the length dependence of THEPH.
`pwtheph=0 1/V`	Coefficient of the width dependence of THEPH.
`plwtheph=0 1/V`	Coefficient of the length times width dependence of THEPH.
`poetamob=1.4(n)/3(p)`	
	Coefficient of the geometry-independent part of ETAMOB.
`pletamob=0`	Coefficient of the length dependence of ETAMOB.
`pwetamob=0`	Coefficient of the width dependence of ETAMOB.
`plwetamob=0`	Coefficient of the length times width dependence of ETAMOB.
`pother=0.0812(n)/0.079(p) 1/V`	
	Coefficient of the geometry-independent part of THER.
`plther=0 1/V`	Coefficient of the length dependence of THER.
`pwther=0 1/V`	Coefficient of the width dependence of THER.

© 2023 Cadence Design Systems, Inc.

`plwther=0 1/V`	Coefficient of the length times width dependence of THER.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`pothesat=0.251(n)/0.173(p) 1/V`	Coefficient of the geometry-independent part of THESAT.
`plthesat=0 1/V`	Coefficient of the length dependence of THESAT.
`pwthesat=0 1/V`	Coefficient of the width dependence of THESAT.
`plwthesat=0 1/V`	Coefficient of the length times width dependence of THESAT.
`potheth=1e-05(n)/0(p) 1/V`^{3}	Coefficient of the geometry-independent part of THETH.
`pltheth=0 1/V`^{3}	Coefficient of the length dependence of THETH.
`pwtheth=0 1/V`^{3}	Coefficient of the width dependence of THETH.
`plwtheth=0 1/V`^{3}	Coefficient of the length times width dependence of THETH.
`posdibl=0.000853(n)/3.55e-05(p) 1/|V`	Coefficient of the geometry-independent part of SDIBL.
`plsdibl=0 1/|V`	Coefficient of the length dependence of SDIBL.
`pwsdibl=0 1/|V`	Coefficient of the width dependence of SDIBL.
`plwsdibl=0 1/|V`	Coefficient of the length times width dependence of SDIBL.
`pomo=0`	Coefficient of the geometry-independent part of MO.
`plmo=0`	Coefficient of the length dependence of MO.
`pwmo=0`	Coefficient of the width dependence of MO.

© 2023 Cadence Design Systems, Inc.

`plwmo=0`	Coefficient of the length times width dependence of MO.
`possf=0.012(n)/0.01(p) 1/√V`	Coefficient of the geometry-independent part of SSF.
`plssf=0 1/√V`	Coefficient of the length dependence of SSF.
`pwssf=0 1/√V`	Coefficient of the width dependence of SSF.
`plwssf=0 1/√V`	Coefficient of the length times width dependence of SSF.
`poalp=0.025`	Coefficient of the geometry-independent part of ALP.
`plalp=0`	Coefficient of the length dependence of ALP.
`pwalp=0`	Coefficient of the width dependence of ALP.
`plwalp=0`	Coefficient of the length times width dependence of ALP.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`pomexp=0.2`	Coefficient of the geometry-independent part of MEXP.
`plmexp=0`	Coefficient of the length dependence of MEXP.
`pwmexp=0`	Coefficient of the width dependence of MEXP.
`plwmexp=0`	Coefficient of the length times width dependence of MEXP.
`poa1=6.02(n)/6.86(p)`	Coefficient of the geometry-independent part of A1.
`pla1=0`	Coefficient of the length dependence of A1.
`pwa1=0`	Coefficient of the width dependence of A1.
`plwa1=0`	Coefficient of the length times width dependence of A1.
`poa2=38(n)/57.3(p) V`	Coefficient of the geometry-independent part of A2.
`pla2=0 V`	Coefficient of the length dependence of A2.
`pwa2=0 V`	Coefficient of the width dependence of A2.
`plwa2=0 V`	Coefficient of the length times width dependence of A2.

© 2023 Cadence Design Systems, Inc.

`poa3=0.641(n)/0.425(p)`	
	Coefficient of the geometry-independent part of A3.
`pla3=0`	Coefficient of the length dependence of A3.
`pwa3=0`	Coefficient of the width dependence of A3.
`plwa3=0`	Coefficient of the length times width dependence of A3.
`poiginv=0 A/V`^{2}	Coefficient of the geometry-independent part of IGINV.
`pliginv=0 A/V`^{2}	Coefficient of the length dependence of IGINV.
`pwiginv=0 A/V`^{2}	Coefficient of the width dependence of IGINV.
`plwiginv=0 A/V`^{2}	Coefficient of the length times width dependence of IGINV.
`pobinv=48(n)/87.5(p) V`	
	Coefficient of the geometry-independent part of BINV.
`plbinv=0 V`	Coefficient of the length dependence of BINV.
`pwbinv=0 V`	Coefficient of the width dependence of BINV.
`plwbinv=0 V`	Coefficient of the length times width dependence of BINV.
`poigacc=0 A/V`^{2}	Coefficient of the geometry-independent part of IGACC.
`pligacc=0 A/V`^{2}	Coefficient of the length dependence of IGACC.
`pwigacc=0 A/V`^{2}	Coefficient of the width dependence of IGACC.
`plwigacc=0 A/V`^{2}	Coefficient of the length times width dependence of IGACC.
`pobacc=48 V`	Coefficient of the geometry-independent part of BACC.
`plbacc=0 V`	Coefficient of the length dependence of BACC.
`pwbacc=0 V`	Coefficient of the width dependence of BACC.
`plwbacc=0 V`	Coefficient of the length times width dependence of BACC.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.

© 2023 Cadence Design Systems, Inc.

`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`poigov=0 A/V`^{2}	Coefficient of the geometry-independent part of IGOV.
`pligov=0 A/V`^{2}	Coefficient of the length dependence of IGOV.
`pwigov=0 A/V`^{2}	Coefficient of the width dependence of IGOV.
`plwigov=0 A/V`^{2}	Coefficient of the length times width dependence of IGOV.
`poagidl=0 A/V`^{3}	Coefficient of the geometry-independent part of AGIDL.
`plagidl=0 A/V`^{3}	Coefficient of the length dependence of AGIDL.
`pwagidl=0 A/V`^{3}	Coefficient of the width dependence of AGIDL.
`plwagidl=0 A/V`^{3}	Coefficient of the length times width dependence of AGIDL.
`pobgidl=41 V`	Coefficient of the geometry-independent part of BGIDL.
`plbgidl=0 V`	Coefficient of the length dependence of BGIDL.
`pwbgidl=0 V`	Coefficient of the width dependence of BGIDL.
`plwbgidl=0 V`	Coefficient of the length times width dependence of BGIDL.
`pocgidl=0`	Coefficient of the geometry-independent part of CGIDL.
`plcgidl=0`	Coefficient of the length dependence of CGIDL.
`pwcgidl=0`	Coefficient of the width dependence of CGIDL.
`plwcgidl=0`	Coefficient of the length times width dependence of CGIDL.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`pocox=2.98e-14(n)/2.72e-14(p) F`	Coefficient of the geometry-independent part of COX.
`plcox=0 F`	Coefficient of the length dependence of COX.
`pwcox=0 F`	Coefficient of the width dependence of COX.
`plwcox=0 F`	Coefficient of the length times width dependence of COX.

© 2023 Cadence Design Systems, Inc.

`pocgdo=6.39e-15(n)/6.36e-15(p) F`	Coefficient of the geometry-independent part of CGDO.
`plcgdo=0 F`	Coefficient of the length dependence of CGDO.
`pwcgdo=0 F`	Coefficient of the width dependence of CGDO.
`plwcgdo=0 F`	Coefficient of the length time width dependence of CGDO.
`pocgso=6.39e-15(n)/6.36e-15(p) F`	Coefficient of the geometry-independent part of CGSO.
`plcgso=0 F`	Coefficient of the length dependence of CGSO.
`pwcgso=0 F`	Coefficient of the width dependence of CGSO.
`plwcgso=0 F`	Coefficient of the length times width dependence of CGSO.
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`ponfa=8.32e+22(n)/1.9e+22(p) 1/V m`^{4}	Coefficient of the geometry-independent part of NFA.
`plnfa=0 1/V m`^{4}	Coefficient of the length dependence of NFA.
`pwnfa=0 1/V m`^{4}	Coefficient of the width dependence of NFA.
`plwnfa=0 1/V m`^{4}	Coefficient of the length times width dependence of NFA.
`ponfb=2.51e+07(n)/5.04e+06(p) 1/V m`^{2}	Coefficient of the geometry-independent part of NFB.
`plnfb=0 1/V m`^{2}	Coefficient of the length dependence of NFB.
`pwnfb=0 1/V m`^{2}	Coefficient of the width dependence of NFB.
`plwnfb=0 1/V m`^{2}	Coefficient of the length times width dependence of NFB.
`ponfc=0(n)/3.63e-10(p) 1/V`	Coefficient of the geometry-independent part of NFC.
`plnfc=0 1/V`	Coefficient of the length dependence of NFC.

© 2023 Cadence Design Systems, Inc.

`pwnfc=0 1/V`	Coefficient of the width dependence of NFC.
`plwnfc=0 1/V`	Coefficient of the length times width dependence of NFC.
`potvfb=0.0005 V/K`	Coefficient of the geometry-independent part of STVFB.
`pltvfb=0 V/K`	Coefficient of the length dependence of STVFB.
`pwtvfb=0 V/K`	Coefficient of the width dependence of STVFB.
`plwtvfb=0 V/K`	Coefficient of the length times width dependence of STVFB.
`potphib=-0.00085 V/K`	Coefficient of the geometry-independent part of STPHIB.
`pltphib=0 V/K`	Coefficient of the length dependence of STPHIB.
`pwtphib=0 V/K`	Coefficient of the width dependence of STPHIB.
`plwtphib=0 V/K`	Coefficient of the length times width dependence of STPHIB.
`potetabet=1.3(n)/0.5(p)`	Coefficient of the geometry-independent part of ETABET.
`pltetabet=0`	Coefficient of the length dependence of ETABET.
`pwtetabet=0`	Coefficient of the width dependence of ETABET.
`plwtetabet=0`	Coefficient of the length times width dependence of ETABET.
`potetasr=0.65(n)/0.5(p)`	Coefficient of the geometry-independent part of ETASR.
`pltetasr=0`	Coefficient of the length dependence of ETASR.
`pwtetasr=0`	Coefficient of the width dependence of ETASR.
`plwtetasr=0`	Coefficient of the length times width dependence of ETASR.
`potetaph=1.35(n)/3.75(p)`	

© 2023 Cadence Design Systems, Inc.

	Coefficient of the geometry-independent part of ETAPH.
`pltetaph=0`	Coefficient of the length dependence of ETAPH.
`pwtetaph=0`	Coefficient of the width dependence of ETAPH.
`plwtetaph=0`	Coefficient of the length times width dependence of ETAPH.
`potetamob=0 1/K`	Coefficient of the geometry-independent part of STETAMOB.
`pltetamob=0 1/K`	Coefficient of the length dependence of STETAMOB.
`pwtetamob=0 1/K`	Coefficient of the width dependence of STETAMOB.
`plwtetamob=0 1/K`	Coefficient of the length times width dependence of STETAMOB.
`nu=2`	Exponent of field dependence of mobility model.
`potnuexp=5.25(n)/3.23(p)`	
	Coefficient of the geometry-independent part of NUEXP.
`pltnuexp=0`	Coefficient of the length dependence of NUEXP.
`pwtnuexp=0`	Coefficient of the width dependence of NUEXP.
`plwtnuexp=0`	Coefficient of the length times width dependence of NUEXP.
`potetar=0.95(n)/0.4(p)`	
	Coefficient of the geometry-independent part of ETAR.
`pltetar=0`	Coefficient of the length dependence of ETAR.
`pwtetar=0`	Coefficient of the width dependence of ETAR.
`plwtetar=0`	Coefficient of the length times width dependence of ETAR.
`potetasat=1.04(n)/0.86(p)`	
	Coefficient of the geometry-independent part of ETASAT.
`pltetasat=0`	Coefficient of the length dependence of ETASAT.
`pwtetasat=0`	Coefficient of the width dependence of ETASAT.

© 2023 Cadence Design Systems, Inc.

`plwtetasat=0`	Coefficient of the length times width dependence of ETASAT.
`pota1=0 1/K`	Coefficient of the geometry-independent part of STA1.
`plta1=0 1/K`	Coefficient of the length dependence of STA1.
`pwta1=0 1/K`	Coefficient of the width dependence of STA1.
`plwta1=0 1/K`	Coefficient of the length times width dependence of STA1.
`potbgidl=-0.000364 V/K`	Coefficient of the geometry-independent part of STBGIDL.
`pltbgidl=0 V/K`	Coefficient of the length dependence of STBGIDL.
`pwtbgidl=0 V/K`	Coefficient of the width dependence of STBGIDL.
`plwtbgidl=0 V/K`	Coefficient of the length times width dependence of STBGIDL.
`dta=0 K`	Temperature offset of the device.
`rgo=0 Ω`	Gate resistance.
`rint=0 Ω m`^{2}	Contact resistance between silicide and poly.
`rvpoly=0 Ω m`^{2}	Vertical poly resistance.
`rshg=0 Ω/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0 m`	Silicide extension over the physical gate length.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`binning=0`	flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`tnom (C)`	alias of tnom.
`tref (C)`	alias of tnom.

© 2023 Cadence Design Systems, Inc.

`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).

© 2023 Cadence Design Systems, Inc.

cgd (F)	Capacitance (- d qg / d vd).
cgg (F)	Capacitance (d qg / d vg).
cgs (F)	Capacitance (- d qg / d vs).
cgb (F)	Capacitance (- d qg / d vb).
csd (F)	Capacitance (- d qs / d vd).
csg (F)	Capacitance (- d qs / d vg).
css (F)	Capacitance (d qs / d vs).
csb (F)	Capacitance (- d qs / d vb).
cbd (F)	Capacitance (- d qb / d vd).
cbg (F)	Capacitance (- d qb / d vg).
cbs (F)	Capacitance (- d qb / d vs).
cbb (F)	Capacitance (d qb / d vb).
cgdol (F)	Gate-drain overlap capacitance of the actual transistor.
cgsol (F)	Gate-source overlap capacitance of the actual transistor.
weff (m)	Effective channel width for geometrical models.
leff (m)	Effective channel length for geometrical models.
rg (Ω)	Gate resistance.
u	Transistor gain (gm/gds).
rout (Ω)	Small-signal output resistance (1/gds).
vearly (V)	Equivalent Early voltage (|id|/gds).
keff ($\sqrt{V}$)	Body effect parameter.
beff (A/V^2)	Gain factor.
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw ($V/\sqrt{Hz}$)	Input-referred RMS white noise voltage density.
sqrtsff ($V/\sqrt{Hz}$)	Input-referred RMS white noise voltage density at 1 kHz.
fknee (Hz)	Cross-over frequency above which white noise is dominant.

© 2023 Cadence Design Systems, Inc.

`Pdiss (W)`	Dissipation.
`TK (K)`	Actual device temperature.
`BET (A/V`^{2}`)`	Gain factor.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`von (V)`	Signed vth (<0 for PMOS, >0 for NMOS).
`table_ids (A)`	Current.
`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`table_qg (Coul)`	Charge at g node.
`table_qd (Coul)`	Charge at d node.
`table_qb (Coul)`	Charge at b node.
`pwr (W)`	Power.
`mos_region=SUBTHRESHOLD`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`
`diode_region=ON`	DIODE region. Possible values are `off` and `on`.

Related Topics

Philips Models

MOS Model 11, Level 1101 (mos11010t)

MOS Model 11, Level 1101 (mos11010)

MOS Model 11, Level 1101 (mos11011)

MOS Model 11, Level 1101 (mos1101e)

This is SimKit 5.2.

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos1101e parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1.1e+03`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`tr=21 C`	Reference temperature.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of VFB.
`ko=0.5 |V`	Body-effect factor.
`kpinv=0 1/|V`	Inverse of body-effect factor of the poly-silicon gate.
`phib=0.95 V`	Surface potential at the onset of strong inversion.
`stphib=-0.00085 V/K`	Coefficient of the temperature dependency of PHIB.
`bet=0.00192(n)/0.000381(p) A/V`^{2}	Gain factor.
`etabet=1.3(n)/0.5(p)`	Exponent of the temperature dependence of the gain factor.
`thesr=0.356(n)/0.73(p) 1/V`	Mobility degradation parameter due to surface roughness scattering.
`etasr=0.65(n)/0.5(p)`	Exponent of the temperature dependence of THESR.
`theph=0.0129(n)/0.001(p) 1/V`	Mobility degradation parameter due to phonon scattering.
`etaph=1.35(n)/3.75(p)`	Exponent of the temperature dependence of THEPH.
`etamob=1.4(n)/3(p)`	

© 2023 Cadence Design Systems, Inc.

	Effective field parameter for dependence on depletion charge.
`stetamob=0 1/K`	Coefficient of the temperature dependence of ETAMOB.
`nu=2`	Exponent of field dependence of mobility model.
`nuexp=5.25(n)/3.23(p)`	Exponent of the temperature dependence of parameter NU.
`ther=0.0812(n)/0.079(p) 1/V`	Coefficient of series resistance.
`etar=0.95(n)/0.4(p)`	Exponent of the temperature dependence of THER.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`thesat=0.251(n)/0.173(p) 1/V`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`etasat=1.04(n)/0.86(p)`	Exponent of the temperature dependence of THESAT.
`theth=1e-05(n)/0(p) 1/V`^{3}	Coefficient of self-heating.
`sdibl=0.000853(n)/3.55e-05(p) 1/V`	Drain-induced barrier lowering parameter.
`mo=0`	Parameter for (short-channel) subthreshold slope.
`ssf=0.012(n)/0.01(p) 1/V`	Static-feedback parameter.
`alp=0.025`	Factor of channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`mexp=5`	Smoothing factor.

© 2023 Cadence Design Systems, Inc.

`a1=6.02(n)/6.86(p)`	
	Factor of the weak-avalanche current.
`sta1=0 1/K`	Coefficient of the temperature dependence of A1.
`a2=38(n)/57.3(p) V`	
	Exponent of the weak-avalanche current.
`a3=0.641(n)/0.425(p)`	
	Factor of the drain-source voltage above which weak-avalanche occurs.
`iginv=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) V`	
	Probability factor for intrinsic gate tunneling current in inversion.
`igacc=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igov=0 A/V`^{2}	Gain factor for Source/Drain overlap tunneling current.
`agidl=0 A/V`^{3}	Gain factor for gate-induced leakage current.
`bgidl=41 V`	Probability factor for gate-induced drain leakage current at reference temperature.
`stbgidl=-0.000364 V/K`	
	Coefficient of the temperature dependence of BGIDL.
`cgidl=0`	Factor for the lateral field dependence of the gate-induced leakage current.
`cox=2.98e-14(n)/2.72e-14(p) F`	
	Oxide capacitance for the intrinsic channel (* mult).
`cgdo=6.39e-15(n)/6.36e-15(p) F`	

© 2023 Cadence Design Systems, Inc.

	Oxide capacitance for the gate-drain overlap (* mult).
`cgso=6.39e-15(n)/6.36e-15(p) F`	
	Oxide capacitance for the gate-source overlap (* mult).
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`nfa=8.32e+22(n)/1.9e+22(p) 1/(Vm`^{4}`)`	
	First coefficient of the flicker noise.
`nfb=2.51e+07(n)/ 5.04e+06(p) 1/(Vm`^{2}`)`	
	Second coefficient of the flicker noise.
`nfc=0(n)/3.63e-10(p) 1/V`	
	Third coefficient of the flicker noise.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`dta=0 K`	Temperature offset of the device.
`rg=0` Ω	Gate resistance.
`binning=0`	Flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`tnom (C)`	Alias of tnom.
`tref (C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`int_s`	
`int_d`	

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).

© 2023 Cadence Design Systems, Inc.

`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgdol (F)`	Gate-drain overlap capacitance of the actual transistor.
`cgsol (F)`	Gate-source overlap capacitance of the actual transistor.
`rg (Ω)`	Gate resistance.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|id|/gds).
`keff (√V )`	Body effect parameter.
`beff (A/V^2)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`sqrtsfw (V/√Hz )`	Input-referred RMS white noise voltage density.
`sqrtsff (V/√Hz )`	Input-referred RMS white noise voltage density at 1 kHz.

© 2023 Cadence Design Systems, Inc.

`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`von (V)`	Signed vth (<0 for PMOS, >0 for NMOS).
`table_ids (A)`	Current.
`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`table_qg (Coul)`	Charge at g node.
`table_qd (Coul)`	Charge at d node.
`table_qb (Coul)`	Charge at b node.
`mos_region=SUBTHRESHOLD`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.
`diode_region=ON`	DIODE region. Possible values are `off` and `on`.

Related Topics

Philips Models

MOS Model 11, Level 1101 (mos1101et)

MOS Model 11, Level 1101 (mos1101et)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos1101et parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1.1e+03`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`tr=21 C`	Reference temperature.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of VFB.
`ko=0.5 |V`	Body-effect factor.
`kpinv=0 1/|V`	Inverse of body-effect factor of the poly-silicon gate.
`phib=0.95 V`	Surface potential at the onset of strong inversion.
`stphib=-0.00085 V/K`	Coefficient of the temperature dependency of PHIB.
`bet=0.00192(n)/0.000381(p) A/V`^{2}	Gain factor.
`etabet=1.3(n)/0.5(p)`	Exponent of the temperature dependence of the gain factor.
`thesr=0.356(n)/0.73(p) 1/V`	Mobility degradation parameter due to surface roughness scattering.
`etasr=0.65(n)/0.5(p)`	Exponent of the temperature dependence of THESR.
`theph=0.0129(n)/0.001(p) 1/V`	Mobility degradation parameter due to phonon scattering.
`etaph=1.35(n)/3.75(p)`	Exponent of the temperature dependence of THEPH.
`etamob=1.4(n)/3(p)`	

© 2023 Cadence Design Systems, Inc.

	Effective field parameter for dependence on depletion charge.
`stetamob=0 1/K`	Coefficient of the temperature dependence of ETAMOB.
`nu=2`	Exponent of field dependence of mobility model.
`nuexp=5.25(n)/3.23(p)`	Exponent of the temperature dependence of parameter NU.
`ther=0.0812(n)/0.079(p) 1/V`	Coefficient of series resistance.
`etar=0.95(n)/0.4(p)`	Exponent of the temperature dependence of THER.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`thesat=0.251(n)/0.173(p) 1/V`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`etasat=1.04(n)/0.86(p)`	Exponent of the temperature dependence of THESAT.
`theth=1e-05(n)/0(p) 1/V`^{3}	Coefficient of self-heating.
`sdibl=0.000853(n)/3.55e-05(p) 1/V`	Drain-induced barrier lowering parameter.
`mo=0`	Parameter for (short-channel) subthreshold slope.
`ssf=0.012(n)/0.01(p) 1/V`	Static-feedback parameter.
`alp=0.025`	Factor of channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`mexp=5`	Smoothing factor.

© 2023 Cadence Design Systems, Inc.

`a1=6.02(n)/6.86(p)`	
	Factor of the weak-avalanche current.
`sta1=0 1/K`	Coefficient of the temperature dependence of A1.
`a2=38(n)/57.3(p) V`	
	Exponent of the weak-avalanche current.
`a3=0.641(n)/0.425(p)`	
	Factor of the drain-source voltage above which weak-avalanche occurs.
`iginv=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) V`	
	Probability factor for intrinsic gate tunneling current in inversion.
`igacc=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igov=0 A/V`^{2}	Gain factor for Source/Drain overlap tunneling current.
`agidl=0 A/V`^{3}	Gain factor for gate-induced leakage current.
`bgidl=41 V`	Probability factor for gate-induced drain leakage current at reference temperature.
`stbgidl=-0.000364 V/K`	
	Coefficient of the temperature dependence of BGIDL.
`cgidl=0`	Factor for the lateral field dependence of the gate-induced leakage current.
`cox=2.98e-14(n)/2.72e-14(p) F`	
	Oxide capacitance for the intrinsic channel (* mult).

© 2023 Cadence Design Systems, Inc.

`cgdo=6.39e-15(n)/6.36e-15(p) F`	Oxide capacitance for the gate-drain overlap (* mult).
`cgso=6.39e-15(n)/6.36e-15(p) F`	Oxide capacitance for the gate-source overlap (* mult).
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`nfa=8.32e+22(n)/1.9e+22(p) 1/(Vm`^{4}`)`	First coefficient of the flicker noise.
`nfb=2.51e+07(n)/ 5.04e+06(p) 1/(Vm`^{2}`)`	Second coefficient of the flicker noise.
`nfc=0(n)/3.63e-10(p) 1/V`	Third coefficient of the flicker noise.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`dta=0 K`	Temperature offset of the device.
`rg=0` Ω	Gate resistance.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`binning=0`	Flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`tnom (C)`	Alias of tnom.
`tref (C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`int_s`	
`int_d`	

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).

© 2023 Cadence Design Systems, Inc.

`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgdol (F)`	Gate-drain overlap capacitance of the actual transistor.
`cgsol (F)`	Gate-source overlap capacitance of the actual transistor.
`rg (Ω)`	Gate resistance.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|id|/gds).
`keff (√V )`	Body effect parameter.
`beff (A/V^2)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`sqrtsfw (V/√Hz )`	Input-referred RMS white noise voltage density.
`sqrtsff (V/√Hz )`	Input-referred RMS white noise voltage density at 1 kHz.

© 2023 Cadence Design Systems, Inc.

`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`von (V)`	Signed vth (<0 for PMOS, >0 for NMOS).
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual device temperature.
`table_ids (A)`	Current.
`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`table_qg (Coul)`	Charge at g node.
`table_qd (Coul)`	Charge at d node.
`table_qb (Coul)`	Charge at b node.
`pwr (W)`	Power.
`mos_region`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`
`diode_region`	DIODE region. Possible values are `off` and `on`.

Related Topics

Philips Models

MOS Model 11, Level 1101 (mos1101e)

MOS Model 11, Level 1102 (mos11020)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
`nf=1`	Number of fingers.
`ngcon=1`	Number of gate contacts.
`xgw=1e-07 m`	Distance from the gate contact to the channel edge.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos11020 parameter=value ...
```

Model Parameters

`level=1.1e+04`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.

© 2023 Cadence Design Systems, Inc.

`tmin=0 s`	Ovcheck tmin value.
`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=4e-08 m`	Effective channel length reduction per side.
`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 C`	Reference temperature.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of VFB.
`kor=0.5 √V`	Body effect coefficient for the reference transistor.
`slko=0`	Coefficient of the length dependence of KO.
`sl2ko=0`	Second coefficient of the length dependence of KO.
`sl3ko=0`	Third coefficient of the length dependence of KO.
`sl3koexp=1`	Exponent belonging to the third coefficient of the length dependence of KO.
`swko=0`	Coefficient of the width dependence of KO.
`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
`phibr=0.95 V`	Surface potential at strong inversion.
`stphib=-0.00085 V/K`	Coefficient of the temperature dependency of PHIB.
`slphib=0`	Coefficient of the length dependence of PHIB.
`sl2phib=0`	Second coefficient of the length dependence of PHIB.
`swphib=0`	Coefficient of the width dependence of PHIB.
`betsq=0.000371(n)/0.000115(p) A/V`^{2}	Gain factor for an infinite square transistor.
`etabetr=1.3(n)/0.5(p)`	Exponent of the temperature dependence of the gain factor.
`sletabet=0`	Coefficient of length dependence of ETABETR.

© 2023 Cadence Design Systems, Inc.

`fbet1=0`	Relative mobility decrease due to first lateral profile.
`lp1=8e-07 m`	Characteristic length of first lateral profile.
`fbet2=0`	Relative mobility decrease due to second lateral profile.
`lp2=8e-07 m`	Characteristic length of second lateral profile.
`thesrr=0.4(n)/0.73(p) 1/V`	Coefficient of the mobility reduction due to surface roughness scattering.
`etasr=0.65(n)/0.5(p)`	Exponent of the temperature dependence of THESR.
`swthesr=0`	Coefficient of the width dependence of THESR.
`thephr=0.0129(n)/0.001(p) 1/V`	Coefficient of the mobility reduction due to phonon scattering.
`etaph=1.35(n)/3.75(p)`	Exponent of the temperature dependence of THEPH.
`swtheph=0`	Coefficient of the width dependence of THEPH.
`etamobr=1.4(n)/3(p)`	Effective field parameter for dependence on depletion/ inversion charge.
`stetamob=0 1/K`	Coefficient of the temperature dependence of ETAMOB.
`swetamob=0`	Coefficient of the width dependence of ETAMOB.
`nu=2`	Exponent of field dependence of mobility model.
`nuexp=5.25(n)/3.23(p)`	Exponent of the temperature dependence of parameter NU.
`therr=0.155(n)/0.08(p) 1/V`	Coefficient of the series resistance.
`etar=0.95(n)/0.4(p)`	Exponent of the temperature dependence of THER.

© 2023 Cadence Design Systems, Inc.

`swther=0`	Coefficient of the width dependence of THER.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`thesatr=0.5(n)/0.2(p) 1/V`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`etasat=1.04(n)/0.86(p)`	Exponent of the temperature dependence of THESAT.
`slthesat=1`	Coefficient of length dependence of THESAT.
`thesatexp=1`	Exponent of length dependence of THESAT.
`swthesat=0`	Coefficient of the width dependence of THESAT.
`thethr=0.001(n)/0.0005(p) 1/V`^{3}	Coefficient of self-heating.
`thethexp=1`	Exponent of the length dependence of THETH.
`swtheth=0`	Coefficient of the width dependence of THETH.
`sdiblo=0.0001 1/V`	Drain-induced barrier lowering parameter.
`sdiblexp=1.35`	Exponent of the length dependence of SDIBL.
`moo=0`	Parameter for short-channel subthreshold slope.
`mor=0`	Parameter for short-channel subthreshold slope per unit length.
`moexp=1.34`	Exponent of the length dependence of MO.
`ssfr=0.00625 1/V`	Static feedback parameter.
`slssf=1`	Coefficient of the length dependence of SSF.
`swssf=0`	Coefficient of the width dependence of SSF.
`alpr=0.01`	Factor of the channel length modulation.
`slalp=1`	Coefficient of the length dependence of ALP.

© 2023 Cadence Design Systems, Inc.

`alpexp=1`	Exponent of the length dependence of ALP.
`swalp=0`	Coefficient of the width dependence of ALP.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`lmin=1.5e-07 m`	Minimum effective channel length in technology, used for calculation of smoothing factor m.
`a1r=6`	Factor of the weak-avalanche current.
`sta1=0 1/K`	Coefficient of the temperature dependence of A1.
`sla1=0`	Coefficient of the length dependence of A1.
`swa1=0`	Coefficient of the width dependence of A1.
`a2r=38 V`	Exponent of the weak-avalanche current.
`sla2=0`	Coefficient of the length dependence of A2.
`swa2=0`	Coefficient of the width dependence of A2.
`a3r=1`	Factor of the drain-source voltage above which weak-avalanche occurs.
`sla3=0`	Coefficient of the length dependence of A3.
`swa3=0`	Coefficient of the width dependence of A3.
`iginvr=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) V`	Probability factor for intrinsic gate tunneling current in inversion.
`igaccr=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igovr=0 A/V`^{2}	Gain factor for Source/Drain overlap gate tunneling current.
`agidlr=0 A/V`^{3}	Gain factor for gate-induced leakage current.

© 2023 Cadence Design Systems, Inc.

`bgidl=41 V`	Probability factor for gate-induced drain leakage current at reference temperature.
`stbgidl=-0.000364 V/K`	Coefficient of the temperature dependence of BGIDL.
`cgidl=0`	Factor for the lateral field dependence of the gate-induced leakage current.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`col=3.2e-16 F`	Gate overlap capacitance for a channel width of 1 um.
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`nfar=1.57e+23(n)/3.83e+24(p) 1/(Vm`^{4}`)`	First coefficient of the flicker noise for a channel area of 1 um^2.
`nfbr=4.75e+09(n)/1.02e+09(p) 1/(Vm`^{2}`)`	Second coefficient of the flicker noise for a channel area of 1 um^2.
`nfcr=0(n)/7.3e-08(p) 1/V`	Third coefficient of the flicker noise for a channel area of 1 um^2.
`dta=0 K`	Temperature offset of the device.
`csr=0`	Factor of the Coulomb scattering.
`slcs=0`	Coefficient of the length dependence of CS.
`csexp=1`	Exponent of the length dependence of CS.
`swcs=0`	Coefficient of the width dependence of CS.
`etacs=0`	Exponent of the temperature dependence of CS.
`rgo=0` Ω	Gate resistance.
`rint=0` Ω `m`^{2}	Contact resistance between silicide and poly.
`rvpoly=0` Ω `m`^{2}	Vertical poly resistance.
`rshg=0` Ω`/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0 m`	Silicide extension over the physical gate length.

© 2023 Cadence Design Systems, Inc.

`scalelev=1.1e+04`	flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`mbeo=0.0`	DCmatch parameter.
`mvto=0.0`	Threshold mismatch intercept.
`tnom (C)`	alias of tnom.
`tref (C)`	alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`int_s`	
`int_d`	

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.

© 2023 Cadence Design Systems, Inc.

`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgdol (F)`	Gate-drain overlap capacitance of the actual transistor.
`cgsol (F)`	Gate-source overlap capacitance of the actual transistor.

© 2023 Cadence Design Systems, Inc.

`weff (m)`	Effective channel width for geometrical models.
`leff (m)`	Effective channel length for geometrical models.
`rg (Ω)`	Gate resistance.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (lidl/gds).
`keff (√V )`	Body effect parameter.
`beff (A/V`^{2}`)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`sqrtsfw (V/√Hz )`	Input-referred RMS white noise voltage density.
`sqrtsff (V/√Hz )`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`table_ids (A)`	Current.
`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`table_qg (Coul)`	Charge at g node.
`table_qd (Coul)`	Charge at d node.
`table_qb (Coul)`	Charge at b node.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`von (V)`	Signed vth (<0 for PMOS, >0 for NMOS).
`mos_region=SUBTHRESHOLD`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.
`diode_region=ON`	DIODE region. Possible values are `off` and `on`.

© 2023 Cadence Design Systems, Inc.

Related Topics

Philips Models

MOS Model 11, Level 1102 (mos11020t)

MOS Model 11, Level 1102 (mos11021)

MOS Model 11, Level 1102 (mos11021t)

MOS Model 11, Level 1102 (mos11020t)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
`nf=1`	Number of fingers.
`ngcon=1`	Number of gate contacts.
`xgw=1e-07 m`	Distance from the gate contact to the channel edge.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos11020t parameter=value ...
```

Model Parameters

`level=1.1e+04`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.

© 2023 Cadence Design Systems, Inc.

`lap=4e-08 m`	Effective channel length reduction per side.
`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 C`	Reference temperature.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of VFB.
`kor=0.5 √V`	Body effect coefficient for the reference transistor.
`slko=0`	Coefficient of the length dependence of KO.
`sl2ko=0`	Second coefficient of the length dependence of KO.
`sl3ko=0`	Third coefficient of the length dependence of KO.
`sl3koexp=1`	Exponent belonging to the third coefficient of the length dependence of KO.
`swko=0`	Coefficient of the width dependence of KO.
`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
`phibr=0.95 V`	Surface potential at strong inversion.
`stphib=-0.00085 V/K`	Coefficient of the temperature dependency of PHIB.
`slphib=0`	Coefficient of the length dependence of PHIB.
`sl2phib=0`	Second coefficient of the length dependence of PHIB.
`swphib=0`	Coefficient of the width dependence of PHIB.
`betsq=0.000371(n)/0.000115(p) A/V`^{2}	Gain factor for an infinite square transistor.
`etabetr=1.3(n)/0.5(p)`	Exponent of the temperature dependence of the gain factor.
`sletabet=0`	Coefficient of length dependence of ETABETR.
`fbet1=0`	Relative mobility decrease due to first lateral profile.
`lp1=8e-07 m`	Characteristic length of first lateral profile.

© 2023 Cadence Design Systems, Inc.

`fbet2=0`	Relative mobility decrease due to second lateral profile.
`lp2=8e-07 m`	Characteristic length of second lateral profile.
`thesrr=0.4(n)/0.73(p) 1/V`	Coefficient of the mobility reduction due to surface roughness scattering.
`etasr=0.65(n)/0.5(p)`	Exponent of the temperature dependence of THESR.
`swthesr=0`	Coefficient of the width dependence of THESR.
`thephr=0.0129(n)/0.001(p) 1/V`	Coefficient of the mobility reduction due to phonon scattering.
`etaph=1.35(n)/3.75(p)`	Exponent of the temperature dependence of THEPH.
`swtheph=0`	Coefficient of the width dependence of THEPH.
`etamobr=1.4(n)/3(p)`	Effective field parameter for dependence on depletion/ inversion charge.
`stetamob=0 1/K`	Coefficient of the temperature dependence of ETAMOB.
`swetamob=0`	Coefficient of the width dependence of ETAMOB.
`nu=2`	Exponent of field dependence of mobility model.
`nuexp=5.25(n)/3.23(p)`	Exponent of the temperature dependence of parameter NU.
`therr=0.155(n)/0.08(p) 1/V`	Coefficient of the series resistance.
`etar=0.95(n)/0.4(p)`	Exponent of the temperature dependence of THER.
`swther=0`	Coefficient of the width dependence of THER.

© 2023 Cadence Design Systems, Inc.

`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`thesatr=0.5(n)/0.2(p) 1/V`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`etasat=1.04(n)/0.86(p)`	Exponent of the temperature dependence of THESAT.
`slthesat=1`	Coefficient of length dependence of THESAT.
`thesatexp=1`	Exponent of length dependence of THESAT.
`swthesat=0`	Coefficient of the width dependence of THESAT.
`thethr=0.001(n)/0.0005(p) 1/V`^{3}	Coefficient of self-heating.
`thethexp=1`	Exponent of the length dependence of THETH.
`swtheth=0`	Coefficient of the width dependence of THETH.
`sdiblo=0.0001 1/V`	Drain-induced barrier lowering parameter.
`sdiblexp=1.35`	Exponent of the length dependence of SDIBL.
`moo=0`	Parameter for short-channel subthreshold slope.
`mor=0`	Parameter for short-channel subthreshold slope per unit length.
`moexp=1.34`	Exponent of the length dependence of MO.
`ssfr=0.00625 1/V`	Static feedback parameter.
`slssf=1`	Coefficient of the length dependence of SSF.
`swssf=0`	Coefficient of the width dependence of SSF.
`alpr=0.01`	Factor of the channel length modulation.
`slalp=1`	Coefficient of the length dependence of ALP.
`alpexp=1`	Exponent of the length dependence of ALP.

© 2023 Cadence Design Systems, Inc.

`swalp=0`	Coefficient of the width dependence of ALP.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`lmin=1.5e-07 m`	Minimum effective channel length in technology, used for calculation of smoothing factor m.
`a1r=6`	Factor of the weak-avalanche current.
`sta1=0 1/K`	Coefficient of the temperature dependence of A1.
`sla1=0`	Coefficient of the length dependence of A1.
`swa1=0`	Coefficient of the width dependence of A1.
`a2r=38 V`	Exponent of the weak-avalanche current.
`sla2=0`	Coefficient of the length dependence of A2.
`swa2=0`	Coefficient of the width dependence of A2.
`a3r=1`	Factor of the drain-source voltage above which weak-avalanche occurs.
`sla3=0`	Coefficient of the length dependence of A3.
`swa3=0`	Coefficient of the width dependence of A3.
`iginvr=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) V`	Probability factor for intrinsic gate tunneling current in inversion.
`igaccr=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igovr=0 A/V`^{2}	Gain factor for Source/Drain overlap gate tunneling current.
`agidlr=0 A/V`^{3}	Gain factor for gate-induced leakage current.

© 2023 Cadence Design Systems, Inc.

`bgidl=41 V`	Probability factor for gate-induced drain leakage current at reference temperature.
`stbgidl=-0.000364 V/K`	Coefficient of the temperature dependence of BGIDL.
`cgidl=0`	Factor for the lateral field dependence of the gate-induced leakage current.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`col=3.2e-16 F`	Gate overlap capacitance for a channel width of 1 um.
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`nfar=1.57e+23(n)/3.83e+24(p) 1/(Vm`^{4}`)`	First coefficient of the flicker noise for a channel area of 1 um^2.
`nfbr=4.75e+09(n)/1.02e+09(p) 1/(Vm`^{2}`)`	Second coefficient of the flicker noise for a channel area of 1 um^2.
`nfcr=0(n)/7.3e-08(p) 1/V`	Third coefficient of the flicker noise for a channel area of 1 um^2.
`dta=0 K`	Temperature offset of the device.
`csr=0`	Factor of the Coulomb scattering.
`slcs=0`	Coefficient of the length dependence of CS.
`csexp=1`	Exponent of the length dependence of CS.
`swcs=0`	Coefficient of the width dependence of CS.
`etacs=0`	Exponent of the temperature dependence of CS.
`rgo=0 Ω`	Gate resistance.
`rint=0 Ω m`^{2}	Contact resistance between silicide and poly.
`rvpoly=0 Ω m`^{2}	Vertical poly resistance.
`rshg=0 Ω/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0 m`	Silicide extension over the physical gate length.

© 2023 Cadence Design Systems, Inc.

`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`scalelev=1.1e+04`	flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`mbeo=0.0`	DCmatch parameter.
`mvto=0.0`	Threshold mismatch intercept.
`tnom (C)`	Alias of tnom.
`tref (C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`int_s`	
`int_d`	

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.

© 2023 Cadence Design Systems, Inc.

`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).

© 2023 Cadence Design Systems, Inc.

cbb (F)	Capacitance (d qb / d vb).
cgdol (F)	Gate-drain overlap capacitance of the actual transistor.
cgsol (F)	Gate-source overlap capacitance of the actual transistor.
weff (m)	Effective channel width for geometrical models.
leff (m)	Effective channel length for geometrical models.
rg (Ω)	Gate resistance.
u	Transistor gain (gm/gds).
rout (Ω)	Small-signal output resistance (1/gds).
vearly (V)	Equivalent Early voltage (iidl/gds).
keff (V)	Body effect parameter.
beff (A/V^2)	Gain factor.
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw (V/ Hz)	Input-referred RMS white noise voltage density.
sqrtsff (V/ Hz)	Input-referred RMS white noise voltage density at 1 kHz.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
Pdiss (W)	Dissipation.
TK (K)	Actual device temperature.
table_ids (A)	Current.
table_vth (V)	Threshold voltage including back-bias and drain-bias effects.
table_qg (Coul)	Charge at g node.
table_qd (Coul)	Charge at d node.
table_qb (Coul)	Charge at b node.
ctype	Channel type (-1 for PMOS, +1 for NMOS).
von (V)	Signed vth (<0 for PMOS, >0 for NMOS).

© 2023 Cadence Design Systems, Inc.

`pwr (W)`	Power.
`mos_region`	
	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`
`diode_region`	DIODE region. Possible values are `off` and `on`.

Parameter Index

In the following index, `I` refers to instance parameters, `M` refers to the model parameters section, `O` refers to the output parameters section, and `OP` refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of `M-35` means the 35th model parameter.

Pdiss OP-48.
TK OP-49.
a1r M-77.
a2r M-81.
a3r M-84.
agidlr M-94.
alpexp M-73.
alpr M-71.
ath M-118.
bacc M-90.
beff OP-43.
betsq M-32.
bgidl M-95.
fbet1 M-35.
fbet2 M-37.
fknee OP-47.
fug OP-44.
gatenoise M-100.
gds OP-17.
gm OP-15.
gmb OP-16.
iavl OP-2.
ids OP-1.
igaccr M-89.
igb OP-5.
igd OP-4.
region I-9.
rg OP-38.
rgo M-111.
rint M-112.
rout OP-40.
rshg M-114.
rth M-116.
rvpoly M-113.
scalelev M-119.
sdiblexp M-64.
sdiblo M-63.
sl2ko M-22.
sl2phib M-30.
table_qb OP-54.
table_qd OP-53.
table_qg OP-52.
table_vth OP-51.
tdelay M-11.
tempeff O-1.
thephr M-42.
ther1 M-53.
ther2 M-54.
therr M-50.
thesatexp M-58.
thesatr M-55.
thesrr M-39.

© 2023 Cadence Design Systems, Inc.

binv M-88.
cbb OP-33.
cbd OP-30.
cbg OP-31.
cbs OP-32.
cdb OP-21.
cdd OP-18.
cdg OP-19.
cds OP-20.
cgb OP-25.
cgd OP-22.
cgdol OP-34.
cgg OP-23.
cgidl M-97.
cgs OP-24.
cgsol OP-35.
col M-99.
compatible M-125.
csb OP-29.
csd OP-26.
csexp M-108.
csg OP-27.
iginvr M-87.
igovr M-93.
igs OP-3.
keff OP-42.
kor M-20.
kov M-92.
kpinv M-26.
l I-2.
lap M-14.
leff OP-37.
level M-1.
lmin M-76.
lp1 M-36.
lp2 M-38.
lvar M-13.
m I-10.
mbeo M-121.
meff O-2.
moexp M-67.
moo M-65.
mor M-66.
mos_region OP-58.
sl3ko M-23.
sl3koexp M-24.
sla1 M-79.
sla2 M-82.
sla3 M-85.
slalp M-72.
slcs M-107.
sletabet M-34.
slko M-21.
slphib M-29.
slssf M-69.
slthesat M-57.
sqrtsff OP-46.
sqrtsfw OP-45.
ssfr M-68.
sta1 M-78.
stbgidl M-96.
stetamob M-46.
stop M-12.
stphib M-28.
stvfb M-19.
swa1 M-80.
thethexp M-61.
thethr M-60.
tmin M-10.
tnom M-123.
tox M-98.
tr M-17.
tref M-124.
trise I-8.
type M-120.
u OP-39.
vballmsg M-9.
vbdbhigh M-6.
vbdblow M-5.
vbds M-4.
vbox M-3.
vbsbhigh M-8.
vbsblow M-7.
vds OP-6.
vdss OP-13.
vearly OP-41.
vfb M-18.
vfbov M-91.

© 2023 Cadence Design Systems, Inc.

csr M-106. **mult I-1.** **swa2 M-83.** **vgs OP-7.**

css OP-28. **mvto M-122.** **swa3 M-86.** **vgt OP-12.**

cth M-117. **nf I-4.** **swalp M-74.** **von OP-56.**

ctype OP-55. **nfar M-102.** **swcs M-109.** **vp M-75.**

diode_region OP-59. **nfbr M-103.** **swetamob M-47.** **vsat OP-14.**

dlsil M-115. **nfcr M-104.** **swko M-25.** **vsb OP-8.**

dta M-105. **ngcon I-5.** **swphib M-31.** **vth OP-11.**

etabetr M-33. **nt M-101.** **swssf M-70.** **vto OP-9.**

etacs M-110. **nu M-48.** **swtheph M-44.** **vts OP-10.**

etamobr M-45. **nuexp M-49.** **swther M-52.** **w I-3.**

etaph M-43. **paramchk M-2.** **swthesat M-59.** **weff OP-36.**

etar M-51. **phibr M-27.** **swthesr M-41.** **wot M-16.**

etasat M-56. **printscaled I-7.** **swtheth M-62.** **wvar M-15.**

etasr M-40. **pwr OP-57.** **table_ids OP-50.** **xgw I-6.**

MOS Model 11, Level 1102 (mos11021)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

1	`mult=1`	Number of devices in parallel.
2	`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
3	`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
4	`nf=1`	Number of fingers.
5	`ngcon=1`	Number of gate contacts.
6	`xgw=1e-07 m`	Distance from the gate contact to the channel edge.
7	`printscaled=0`	Print scaled parameter info if value not equal to zero.
8	`trise=0 K`	Difference between the local ambient and global ambient temperature.
9	`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
10	`m=1`	alias of mult.
11	`mos_region=SUBTHRESHOLD`	
12	`diode_region=ON`	

Model Definition

```
model modelName mos11021 parameter=value ...
```

Model Parameters

1	`level=1.1e+04`	Transistor Level.
2	`paramchk=0`	Level of clip warning info.
3	`vbox=0 V`	Oxide breakdown voltage.
4	`vbds=0 V`	Drain-source breakdown voltage.
5	`tmin=0 s`	Ovcheck tmin value.
6	`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.

© 2023 Cadence Design Systems, Inc.

7	`lap=4e-08 m`	Effective channel length reduction per side.
8	`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
9	`wot=0 m`	Effective channel width reduction per side.
10	`tr=21 C`	Reference temperature.
11	`lmin=0 m`	Device length low limit for binning selection.
12	`lmax=1 m`	Device length high limit for binning selection.
13	`wmin=0 m`	Device width low limit for binning selection.
14	`wmax=1 m`	Device width high limit for binning selection.
15	`vfb=-1.05 V`	Flat-band voltage at reference temperature.
16	`poko=0.5 √V`	Coefficient for the geometry-independent part of KO.
17	`plko=0 √V`	Coefficient for the length dependence of KO.
18	`pwko=0 √V`	Coefficient for the width dependence of KO.
19	`plwko=0 √V`	Coefficient for the length times width dependence of KO.
20	`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
21	`pophib=0.95 V`	Coefficient for the geometric independent part of PHIB.
22	`plphib=0 V`	Coefficient for the length dependence of PHIB.
23	`pwphib=0 V`	Coefficient for the width dependence of PHIB.
24	`plwphib=0 V`	Coefficient for the length times width dependence of PHIB.
25	`pobet=0.00192(n)/0.000381(p) A/V^2`	Coefficient for the geometry-independent part of BET.
26	`plbet=0 A/V^2`	Coefficient for the length dependence of BET.
27	`pwbet=0 A/V^2`	Coefficient for the width dependence of BET.
28	`plwbet=0 A/V^2`	Coefficient for the width over length dependence of BET.
29	`pothesr=0.356(n)/0.73(p) 1/V`	Coefficient of the geometry-independent part of THESR.

© 2023 Cadence Design Systems, Inc.

30	`plthesr=0 1/V`	Coefficient of the length dependence of THESR.
31	`pwthesr=0 1/V`	Coefficient of the width dependence of THESR.
32	`plwthesr=0 1/V`	Coefficient of the length times width dependence of THESR.
33	`potheph=0.0129(n)/0.001(p) 1/V`	Coefficient of the geometry-independent part of THEPH.
34	`pltheph=0 1/V`	Coefficient of the length dependence of THEPH.
35	`pwtheph=0 1/V`	Coefficient of the width dependence of THEPH.
36	`plwtheph=0 1/V`	Coefficient of the length times width dependence of THEPH.
37	`poetamob=1.4(n)/3(p)`	Coefficient of the geometry-independent part of ETAMOB.
38	`pletamob=0`	Coefficient of the length dependence of ETAMOB.
39	`pwetamob=0`	Coefficient of the width dependence of ETAMOB.
40	`plwetamob=0`	Coefficient of the length times width dependence of ETAMOB.
41	`pother=0.0812(n)/0.079(p) 1/V`	Coefficient of the geometry-independent part of THER.
42	`plther=0 1/V`	Coefficient of the length dependence of THER.
43	`pwther=0 1/V`	Coefficient of the width dependence of THER.
44	`plwther=0 1/V`	Coefficient of the length times width dependence of THER.
45	`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
46	`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
47	`pothesat=0.251(n)/0.173(p) 1/V`	Coefficient of the geometry-independent part of THESAT.
48	`plthesat=0 1/V`	Coefficient of the length dependence of THESAT.

© 2023 Cadence Design Systems, Inc.

49	`pwthesat=0 1/V`	Coefficient of the width dependence of THESAT.
50	`plwthesat=0 1/V`	Coefficient of the length times width dependence of THESAT.
51	`potheth=1e-05(n)/0(p) 1/V`^{3}	Coefficient of the geometry-independent part of THETH.
52	`pltheth=0 1/V`^{3}	Coefficient of the length dependence of THETH.
53	`pwtheth=0 1/V`^{3}	Coefficient of the width dependence of THETH.
54	`plwtheth=0 1/V`^{3}	Coefficient of the length times width dependence of THETH.
55	`posdibl=0.000853(n)/3.55e-05(p) 1/`$\sqrt{\text{V}}$	Coefficient of the geometry-independent part of SDIBL.
56	`plsdibl=0 1/`$\sqrt{\text{V}}$	Coefficient of the length dependence of SDIBL.
57	`pwsdibl=0 1/`$\sqrt{\text{V}}$	Coefficient of the width dependence of SDIBL.
58	`plwsdibl=0 1/`$\sqrt{\text{V}}$	Coefficient of the length times width dependence of SDIBL.
59	`pomo=0`	Coefficient of the geometry-independent part of MO.
60	`plmo=0`	Coefficient of the length dependence of MO.
61	`pwmo=0`	Coefficient of the width dependence of MO.
62	`plwmo=0`	Coefficient of the length times width dependence of MO.
63	`possf=0.012(n)/0.01(p) 1/`$\sqrt{\text{V}}$	Coefficient of the geometry-independent part of SSF.
64	`plssf=0 1/`$\sqrt{\text{V}}$	Coefficient of the length dependence of SSF.
65	`pwssf=0 1/`$\sqrt{\text{V}}$	Coefficient of the width dependence of SSF.
66	`plwssf=0 1/`$\sqrt{\text{V}}$	

© 2023 Cadence Design Systems, Inc.

		Coefficient of the length times width dependence of SSF.
67	`poalp=0.025`	Coefficient of the geometry-independent part of ALP.
68	`plalp=0`	Coefficient of the length dependence of ALP.
69	`pwalp=0`	Coefficient of the width dependence of ALP.
70	`plwalp=0`	Coefficient of the length times width dependence of ALP.
71	`vp=0.05 V`	Characteristic voltage of channel-length modulation.
72	`pomexp=0.2`	Coefficient of the geometry-independent part of MEXP.
73	`plmexp=0`	Coefficient of the length dependence of MEXP.
74	`pwmexp=0`	Coefficient of the width dependence of MEXP.
75	`plwmexp=0`	Coefficient of the length times width dependence of MEXP.
76	`poa1=6.02(n)/6.86(p)`	
		Coefficient of the geometry-independent part of A1.
77	`pla1=0`	Coefficient of the length dependence of A1.
78	`pwa1=0`	Coefficient of the width dependence of A1.
79	`plwa1=0`	Coefficient of the length times width dependence of A1.
80	`poa2=38(n)/57.3(p) V`	
		Coefficient of the geometry-independent part of A2.
81	`pla2=0 V`	Coefficient of the length dependence of A2.
82	`pwa2=0 V`	Coefficient of the width dependence of A2.
83	`plwa2=0 V`	Coefficient of the length times width dependence of A2.
84	`poa3=0.641(n)/0.425(p)`	
		Coefficient of the geometry-independent part of A3.
85	`pla3=0`	Coefficient of the length dependence of A3.
86	`pwa3=0`	Coefficient of the width dependence of A3.
87	`plwa3=0`	Coefficient of the length times width dependence of A3.

© 2023 Cadence Design Systems, Inc.

88	`poiginv=0 A/V`^{2}	Coefficient of the geometry-independent part of IGINV.
89	`pliginv=0 A/V`^{2}	Coefficient of the length dependence of IGINV.
90	`pwiginv=0 A/V`^{2}	Coefficient of the width dependence of IGINV.
91	`plwiginv=0 A/V`^{2}	Coefficient of the length times width dependence of IGINV.
92	`pobinv=48(n)/87.5(p) V`	Coefficient of the geometry-independent part of BINV.
93	`plbinv=0 V`	Coefficient of the length dependence of BINV.
94	`pwbinv=0 V`	Coefficient of the width dependence of BINV.
95	`plwbinv=0 V`	Coefficient of the length times width dependence of BINV.
96	`poigacc=0 A/V`^{2}	Coefficient of the geometry-independent part of IGACC.
97	`pligacc=0 A/V`^{2}	Coefficient of the length dependence of IGACC.
98	`pwigacc=0 A/V`^{2}	Coefficient of the width dependence of IGACC.
99	`plwigacc=0 A/V`^{2}	Coefficient of the length times width dependence of IGACC.
100	`pobacc=48 V`	Coefficient of the geometry-independent part of BACC.
101	`plbacc=0 V`	Coefficient of the length dependence of BACC.
102	`pwbacc=0 V`	Coefficient of the width dependence of BACC.
103	`plwbacc=0 V`	Coefficient of the length times width dependence of BACC.
104	`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
105	`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
106	`poigov=0 A/V`^{2}	Coefficient of the geometry-independent part of IGOV.
107	`pligov=0 A/V`^{2}	Coefficient of the length dependence of IGOV.
108	`pwigov=0 A/V`^{2}	Coefficient of the width dependence of IGOV.
109	`plwigov=0 A/V`^{2}	Coefficient of the length times width dependence of IGOV.

© 2023 Cadence Design Systems, Inc.

110	`poagidl=0 A/V`^{3}	Coefficient of the geometry-independent part of AGIDL.
111	`plagidl=0 A/V`^{3}	Coefficient of the length dependence of AGIDL.
112	`pwagidl=0 A/V`^{3}	Coefficient of the width dependence of AGIDL.
113	`plwagidl=0 A/V`^{3}	Coefficient of the length times width dependence of AGIDL.
114	`pobgidl=41 V`	Coefficient of the geometry-independent part of BGIDL.
115	`plbgidl=0 V`	Coefficient of the length dependence of BGIDL.
116	`pwbgidl=0 V`	Coefficient of the width dependence of BGIDL.
117	`plwbgidl=0 V`	Coefficient of the length times width dependence of BGIDL.
118	`pocgidl=0`	Coefficient of the geometry-independent part of CGIDL.
119	`plcgidl=0`	Coefficient of the length dependence of CGIDL.
120	`pwcgidl=0`	Coefficient of the width dependence of CGIDL.
121	`plwcgidl=0`	Coefficient of the length times width dependence of CGIDL.
122	`tox=3.2e-09 m`	Thickness of gate oxide layer.
123	`pocox=2.98e-14(n)/2.72e-14(p) F`	Coefficient of the geometry-independent part of COX.
124	`plcox=0 F`	Coefficient of the length dependence of COX.
125	`pwcox=0 F`	Coefficient of the width dependence of COX.
126	`plwcox=0 F`	Coefficient of the length times width dependence of COX.
127	`pocgdo=6.39e-15(n)/6.36e-15(p) F`	Coefficient of the geometry-independent part of CGDO.
128	`plcgdo=0 F`	Coefficient of the length dependence of CGDO.
129	`pwcgdo=0 F`	Coefficient of the width dependence of CGDO.
130	`plwcgdo=0 F`	Coefficient of the length time width dependence of CGDO.

© 2023 Cadence Design Systems, Inc.

131	`pocgso=6.39e-15(n)/6.36e-15(p) F`	Coefficient of the geometry-independent part of CGSO.
132	`plcgso=0 F`	Coefficient of the length dependence of CGSO.
133	`pwcgso=0 F`	Coefficient of the width dependence of CGSO.
134	`plwcgso=0 F`	Coefficient of the length times width dependence of CGSO.
135	`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
136	`nt=1.62e-20 J`	Thermal noise coefficient.
137	`ponfa=8.32e+22(n)/1.9e+22(p) 1/V m`^{4}	Coefficient of the geometry-independent part of NFA.
138	`plnfa=0 1/V m`^{4}	Coefficient of the length dependence of NFA.
139	`pwnfa=0 1/V m`^{4}	Coefficient of the width dependence of NFA.
140	`plwnfa=0 1/V m`^{4}	Coefficient of the length times width dependence of NFA.
141	`ponfb=2.51e+07(n)/5.04e+06(p) 1/V m`^{2}	Coefficient of the geometry-independent part of NFB.
142	`plnfb=0 1/V m`^{2}	Coefficient of the length dependence of NFB.
143	`pwnfb=0 1/V m`^{2}	Coefficient of the width dependence of NFB.
144	`plwnfb=0 1/V m`^{2}	Coefficient of the length times width dependence of NFB.
145	`ponfc=0(n)/3.63e-10(p) 1/V`	Coefficient of the geometry-independent part of NFC.
146	`plnfc=0 1/V`	Coefficient of the length dependence of NFC.
147	`pwnfc=0 1/V`	Coefficient of the width dependence of NFC.
148	`plwnfc=0 1/V`	Coefficient of the length times width dependence of NFC.
149	`potvfb=0.0005 V/K`	Coefficient of the geometry-independent part of STVFB.
150	`pltvfb=0 V/K`	Coefficient of the length dependence of STVFB.
151	`pwtvfb=0 V/K`	Coefficient of the width dependence of STVFB.

© 2023 Cadence Design Systems, Inc.

152	`plwtvfb=0 V/K`	Coefficient of the length times width dependence of STVFB.
153	`potphib=-0.00085 V/K`	Coefficient of the geometry-independent part of STPHIB.
154	`pltphib=0 V/K`	Coefficient of the length dependence of STPHIB.
155	`pwtphib=0 V/K`	Coefficient of the width dependence of STPHIB.
156	`plwtphib=0 V/K`	Coefficient of the length times width dependence of STPHIB.
157	`potetabet=1.3(n)/0.5(p)`	Coefficient of the geometry-independent part of ETABET.
158	`pltetabet=0`	Coefficient of the length dependence of ETABET.
159	`pwtetabet=0`	Coefficient of the width dependence of ETABET.
160	`plwtetabet=0`	Coefficient of the length times width dependence of ETABET.
161	`potetasr=0.65(n)/0.5(p)`	Coefficient of the geometry-independent part of ETASR.
162	`pltetasr=0`	Coefficient of the length dependence of ETASR.
163	`pwtetasr=0`	Coefficient of the width dependence of ETASR.
164	`plwtetasr=0`	Coefficient of the length times width dependence of ETASR.
165	`potetaph=1.35(n)/3.75(p)`	Coefficient of the geometry-independent part of ETAPH.
166	`pltetaph=0`	Coefficient of the length dependence of ETAPH.
167	`pwtetaph=0`	Coefficient of the width dependence of ETAPH.
168	`plwtetaph=0`	Coefficient of the length times width dependence of ETAPH.
169	`potetamob=0 1/K`	Coefficient of the geometry-independent part of STETAMOB.

© 2023 Cadence Design Systems, Inc.

170	`pltetamob=0 1/K`	Coefficient of the length dependence of STETAMOB.
171	`pwtetamob=0 1/K`	Coefficient of the width dependence of STETAMOB.
172	`plwtetamob=0 1/K`	Coefficient of the length times width dependence of STETAMOB.
173	`nu=2`	Exponent of field dependence of mobility model.
174	`potnuexp=5.25(n)/3.23(p)`	Coefficient of the geometry-independent part of NUEXP.
175	`pltnuexp=0`	Coefficient of the length dependence of NUEXP.
176	`pwtnuexp=0`	Coefficient of the width dependence of NUEXP.
177	`plwtnuexp=0`	Coefficient of the length times width dependence of NUEXP.
178	`potetar=0.95(n)/0.4(p)`	Coefficient of the geometry-independent part of ETAR.
179	`pltetar=0`	Coefficient of the length dependence of ETAR.
180	`pwtetar=0`	Coefficient of the width dependence of ETAR.
181	`plwtetar=0`	Coefficient of the length times width dependence of ETAR.
182	`potetasat=1.04(n)/0.86(p)`	Coefficient of the geometry-independent part of ETASAT.
183	`pltetasat=0`	Coefficient of the length dependence of ETASAT.
184	`pwtetasat=0`	Coefficient of the width dependence of ETASAT.
185	`plwtetasat=0`	Coefficient of the length times width dependence of ETASAT.
186	`pota1=0 1/K`	Coefficient of the geometry-independent part of STA1.
187	`plta1=0 1/K`	Coefficient of the length dependence of STA1.
188	`pwta1=0 1/K`	Coefficient of the width dependence of STA1.
189	`plwta1=0 1/K`	Coefficient of the length times width dependence of STA1.
190	`potbgidl=-0.000364 V/K`	

© 2023 Cadence Design Systems, Inc.

		Coefficient of the geometry-independent part of STBGIDL.
191	`pltbgidl=0 V/K`	Coefficient of the length dependence of STBGIDL.
192	`pwtbgidl=0 V/K`	Coefficient of the width dependence of STBGIDL.
193	`plwtbgidl=0 V/K`	Coefficient of the length times width dependence of STBGIDL.
194	`dta=0 K`	Temperature offset of the device.
195	`pocs=0`	Coefficient of the geometry-independent part of CS.
196	`plcs=0`	Coefficient of the length dependence of CS.
197	`pwcs=0`	Coefficient of the width dependence of CS.
198	`plwcs=0`	Coefficient of the length times width dependence of CS.
199	`potetacs=0`	Coefficient of the geometry-independent part of ETACS.
200	`pltetacs=0`	Coefficient of the length dependence of ETACS.
201	`pwtetacs=0`	Coefficient of the width dependence of ETACS.
202	`plwtetacs=0`	Coefficient of the length times width dependence of ETACS.
203	`rgo=0` Ω	Gate resistance.
204	`rint=0` Ω m^2	Contact resistance between silicide and poly.
205	`rvpoly=0` Ω m^2	Vertical poly resistance.
206	`rshg=0` Ω/Sqr	Gate electrode diffusion sheet resistance.
207	`dlsil=0 m`	Silicide extension over the physical gate length.
208	`scalelev=1.1e+04`	flag for eldo model.
209	`type=n`	Transistor gender. Possible values are `n` and `p`.
210	`imax=1000 A`	Explosion current.
211	`mbeo=0.0`	DCmatch parameter.
212	`mvto=0.0`	Threshold mismatch intercept.
213	`tnom (C)`	Alias of tnom.
214	`tref (C)`	Alias of tnom.

© 2023 Cadence Design Systems, Inc.

216	`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

Output Parameters

1	`tempeff (C)`	Effective temperature for a single device.
2	`meff`	Effective multiplicity factor (m-factor).
3	`int_s`	
4	`int_d`	

Operating-Point Parameters

1	`ids (A)`	Drain current, excluding avalanche and tunnel currents.
2	`iavl (A)`	Substrate current due to weak-avalanche.
3	`igs (A)`	Gate-to-source current due to direct tunneling.
4	`igd (A)`	Gate-to-drain current due to direct tunneling.
5	`igb (A)`	Gate-to-bulk current due to direct tunneling.
6	`vds (V)`	Drain-source voltage.
7	`vgs (V)`	Gate-source voltage.
8	`vsb (V)`	Source-bulk voltage.
9	`vto (V)`	Zero-bias threshold voltage.
10	`vts (V)`	Threshold voltage including back-bias effects.
11	`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
12	`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
13	`vdss (V)`	Drain saturation voltage at actual bias.
14	`vsat (V)`	Saturation limit.

© 2023 Cadence Design Systems, Inc.

15	`gm (A/V)`	Transconductance (d ids / d vgs).
16	`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
17	`gds (A/V)`	Output conductance (d ids / d vds).
18	`cdd (F)`	Capacitance (d qd / d vd).
19	`cdg (F)`	Capacitance (- d qd / d vg).
20	`cds (F)`	Capacitance (- d qd / d vs).
21	`cdb (F)`	Capacitance (- d qd / d vb).
22	`cgd (F)`	Capacitance (- d qg / d vd).
23	`cgg (F)`	Capacitance (d qg / d vg).
24	`cgs (F)`	Capacitance (- d qg / d vs).
25	`cgb (F)`	Capacitance (- d qg / d vb).
26	`csd (F)`	Capacitance (- d qs / d vd).
27	`csg (F)`	Capacitance (- d qs / d vg).
28	`css (F)`	Capacitance (d qs / d vs).
29	`csb (F)`	Capacitance (- d qs / d vb).
30	`cbd (F)`	Capacitance (- d qb / d vd).
31	`cbg (F)`	Capacitance (- d qb / d vg).
32	`cbs (F)`	Capacitance (- d qb / d vs).
33	`cbb (F)`	Capacitance (d qb / d vb).
34	`cgdol (F)`	Gate-drain overlap capacitance of the actual transistor.
35	`cgsol (F)`	Gate-source overlap capacitance of the actual transistor.
36	`weff (m)`	Effective channel width for geometrical models.
37	`leff (m)`	Effective channel length for geometrical models.
38	`rg (Ω)`	Gate resistance.
39	`u`	Transistor gain (gm/gds).
40	`rout (Ω)`	Small-signal output resistance (1/gds).
41	`vearly (V)`	Equivalent Early voltage (|idl/gds).
42	`keff (V )`	Body effect parameter.

© 2023 Cadence Design Systems, Inc.

43	`beff (A/V`^{2}`)`	Gain factor.
44	`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
45	`sqrtsfw (V/√Hz )`	Input-referred RMS white noise voltage density.
46	`sqrtsff (V/√Hz )`	Input-referred RMS white noise voltage density at 1 kHz.
47	`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
48	`table_ids (A)`	Current.
49	`table_vth (V)`	Threshold voltage including back-bias and drain-bias effects.
50	`table_qg (Coul)`	Charge at g node.
51	`table_qd (Coul)`	Charge at d node.
52	`table_qb (Coul)`	Charge at b node.
53	`BET (A/V`^{2}`)`	Gain factor.
54	`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
55	`von (V)`	Signed vth (<0 for PMOS, >0 for NMOS).
56	`mos_region=SUBTHRESHOLD`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.
57	`diode_region=ON`	DIODE region. Possible values are `off` and `on`.

Related Topics

Philips Models

MOS Model 11, Level 1102 (mos11020)

MOS Model 11, Level 1102 (mos11021t)

MOS Model 11, Level 1102 (mos11020)

© 2023 Cadence Design Systems, Inc.

MOS Model 11, Level 1102 (mos11021t)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`l=2e-06 m`	Drawn channel length in the layout. Scale set by option scale.
`w=1e-05 m`	Drawn channel width in the layout. Scale set by option scale.
`nf=1`	Number of fingers.
`ngcon=1`	Number of gate contacts.
`xgw=1e-07 m`	Distance from the gate contact to the channel edge.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos11021t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=1.1e+04`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`lvar=0 m`	Difference between the actual and the programmed poly-silicon gate length.
`lap=4e-08 m`	Effective channel length reduction per side.
`wvar=0 m`	Difference between the actual and the programmed field-oxide opening.
`wot=0 m`	Effective channel width reduction per side.
`tr=21 C`	Reference temperature.
`lmin=0 m`	Device length low limit for binning selection.
`lmax=1 m`	Device length high limit for binning selection.
`wmin=0 m`	Device width low limit for binning selection.
`wmax=1 m`	Device width high limit for binning selection.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`poko=0.5 √V`	Coefficient for the geometry-independent part of KO.
`plko=0 √V`	Coefficient for the length dependence of KO.
`pwko=0 √V`	Coefficient for the width dependence of KO.
`plwko=0 √V`	Coefficient for the length times width dependence of KO.
`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
`pophib=0.95 V`	Coefficient for the geometric independent part of PHIB.
`plphib=0 V`	Coefficient for the length dependence of PHIB.
`pwphib=0 V`	Coefficient for the width dependence of PHIB.
`plwphib=0 V`	Coefficient for the length times width dependence of PHIB.

© 2023 Cadence Design Systems, Inc.

`pobet=0.00192(n)/0.000381(p) A/V^2`
: Coefficient for the geometry-independent part of BET.

`plbet=0 A/V^2`
: Coefficient for the length dependence of BET.

`pwbet=0 A/V^2`
: Coefficient for the width dependence of BET.

`plwbet=0 A/V^2`
: Coefficient for the width over length dependence of BET.

`pothesr=0.356(n)/0.73(p) 1/V`
: Coefficient of the geometry-independent part of THESR.

`plthesr=0 1/V`
: Coefficient of the length dependence of THESR.

`pwthesr=0 1/V`
: Coefficient of the width dependence of THESR.

`plwthesr=0 1/V`
: Coefficient of the length times width dependence of THESR.

`potheph=0.0129(n)/0.001(p) 1/V`
: Coefficient of the geometry-independent part of THEPH.

`pltheph=0 1/V`
: Coefficient of the length dependence of THEPH.

`pwtheph=0 1/V`
: Coefficient of the width dependence of THEPH.

`plwtheph=0 1/V`
: Coefficient of the length times width dependence of THEPH.

`poetamob=1.4(n)/3(p)`
: Coefficient of the geometry-independent part of ETAMOB.

`pletamob=0`
: Coefficient of the length dependence of ETAMOB.

`pwetamob=0`
: Coefficient of the width dependence of ETAMOB.

`plwetamob=0`
: Coefficient of the length times width dependence of ETAMOB.

`pother=0.0812(n)/0.079(p) 1/V`
: Coefficient of the geometry-independent part of THER.

`plther=0 1/V`
: Coefficient of the length dependence of THER.

`pwther=0 1/V`
: Coefficient of the width dependence of THER.

© 2023 Cadence Design Systems, Inc.

`plwther=0 1/V`	Coefficient of the length times width dependence of THER.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`pothesat=0.251(n)/0.173(p) 1/V`	Coefficient of the geometry-independent part of THESAT.
`plthesat=0 1/V`	Coefficient of the length dependence of THESAT.
`pwthesat=0 1/V`	Coefficient of the width dependence of THESAT.
`plwthesat=0 1/V`	Coefficient of the length times width dependence of THESAT.
`potheth=1e-05(n)/0(p) 1/V`^{3}	Coefficient of the geometry-independent part of THETH.
`pltheth=0 1/V`^{3}	Coefficient of the length dependence of THETH.
`pwtheth=0 1/V`^{3}	Coefficient of the width dependence of THETH.
`plwtheth=0 1/V`^{3}	Coefficient of the length times width dependence of THETH.
`posdibl=0.000853(n)/3.55e-05(p) 1/|V`	Coefficient of the geometry-independent part of SDIBL.
`plsdibl=0 1/|V`	Coefficient of the length dependence of SDIBL.
`pwsdibl=0 1/|V`	Coefficient of the width dependence of SDIBL.
`plwsdibl=0 1/|V`	Coefficient of the length times width dependence of SDIBL.
`pomo=0`	Coefficient of the geometry-independent part of MO.
`plmo=0`	Coefficient of the length dependence of MO.

© 2023 Cadence Design Systems, Inc.

`pwmo=0`	Coefficient of the width dependence of MO.
`plwmo=0`	Coefficient of the length times width dependence of MO.
`possf=0.012(n)/0.01(p) 1/√V`	Coefficient of the geometry-independent part of SSF.
`plssf=0 1/√V`	Coefficient of the length dependence of SSF.
`pwssf=0 1/√V`	Coefficient of the width dependence of SSF.
`plwssf=0 1/√V`	Coefficient of the length times width dependence of SSF.
`poalp=0.025`	Coefficient of the geometry-independent part of ALP.
`plalp=0`	Coefficient of the length dependence of ALP.
`pwalp=0`	Coefficient of the width dependence of ALP.
`plwalp=0`	Coefficient of the length times width dependence of ALP.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`pomexp=0.2`	Coefficient of the geometry-independent part of MEXP.
`plmexp=0`	Coefficient of the length dependence of MEXP.
`pwmexp=0`	Coefficient of the width dependence of MEXP.
`plwmexp=0`	Coefficient of the length times width dependence of MEXP.
`poa1=6.02(n)/6.86(p)`	Coefficient of the geometry-independent part of A1.
`pla1=0`	Coefficient of the length dependence of A1.
`pwa1=0`	Coefficient of the width dependence of A1.
`plwa1=0`	Coefficient of the length times width dependence of A1.
`poa2=38(n)/57.3(p) V`	Coefficient of the geometry-independent part of A2.
`pla2=0 V`	Coefficient of the length dependence of A2.

© 2023 Cadence Design Systems, Inc.

`pwa2=0 V`	Coefficient of the width dependence of A2.
`plwa2=0 V`	Coefficient of the length times width dependence of A2.
`poa3=0.641(n)/0.425(p)`	Coefficient of the geometry-independent part of A3.
`pla3=0`	Coefficient of the length dependence of A3.
`pwa3=0`	Coefficient of the width dependence of A3.
`plwa3=0`	Coefficient of the length times width dependence of A3.
`poiginv=0 A/V`^{2}	Coefficient of the geometry-independent part of IGINV.
`pliginv=0 A/V`^{2}	Coefficient of the length dependence of IGINV.
`pwiginv=0 A/V`^{2}	Coefficient of the width dependence of IGINV.
`plwiginv=0 A/V`^{2}	Coefficient of the length times width dependence of IGINV.
`pobinv=48(n)/87.5(p) V`	Coefficient of the geometry-independent part of BINV.
`plbinv=0 V`	Coefficient of the length dependence of BINV.
`pwbinv=0 V`	Coefficient of the width dependence of BINV.
`plwbinv=0 V`	Coefficient of the length times width dependence of BINV.
`poigacc=0 A/V`^{2}	Coefficient of the geometry-independent part of IGACC.
`pligacc=0 A/V`^{2}	Coefficient of the length dependence of IGACC.
`pwigacc=0 A/V`^{2}	Coefficient of the width dependence of IGACC.
`plwigacc=0 A/V`^{2}	Coefficient of the length times width dependence of IGACC.
`pobacc=48 V`	Coefficient of the geometry-independent part of BACC.
`plbacc=0 V`	Coefficient of the length dependence of BACC.
`pwbacc=0 V`	Coefficient of the width dependence of BACC.
`plwbacc=0 V`	Coefficient of the length times width dependence of BACC.

© 2023 Cadence Design Systems, Inc.

`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`poigov=0` A/V^2	Coefficient of the geometry-independent part of IGOV.
`pligov=0` A/V^2	Coefficient of the length dependence of IGOV.
`pwigov=0` A/V^2	Coefficient of the width dependence of IGOV.
`plwigov=0` A/V^2	Coefficient of the length times width dependence of IGOV.
`poagidl=0` A/V^3	Coefficient of the geometry-independent part of AGIDL.
`plagidl=0` A/V^3	Coefficient of the length dependence of AGIDL.
`pwagidl=0` A/V^3	Coefficient of the width dependence of AGIDL.
`plwagidl=0` A/V^3	Coefficient of the length times width dependence of AGIDL.
`pobgidl=41 V`	Coefficient of the geometry-independent part of BGIDL.
`plbgidl=0 V`	Coefficient of the length dependence of BGIDL.
`pwbgidl=0 V`	Coefficient of the width dependence of BGIDL.
`plwbgidl=0 V`	Coefficient of the length times width dependence of BGIDL.
`pocgidl=0`	Coefficient of the geometry-independent part of CGIDL.
`plcgidl=0`	Coefficient of the length dependence of CGIDL.
`pwcgidl=0`	Coefficient of the width dependence of CGIDL.
`plwcgidl=0`	Coefficient of the length times width dependence of CGIDL.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`pocox=2.98e-14(n)/2.72e-14(p) F`	Coefficient of the geometry-independent part of COX.
`plcox=0 F`	Coefficient of the length dependence of COX.
`pwcox=0 F`	Coefficient of the width dependence of COX.

© 2023 Cadence Design Systems, Inc.

`plwcox=0 F`	Coefficient of the length times width dependence of COX.
`pocgdo=6.39e-15(n)/6.36e-15(p) F`	Coefficient of the geometry-independent part of CGDO.
`plcgdo=0 F`	Coefficient of the length dependence of CGDO.
`pwcgdo=0 F`	Coefficient of the width dependence of CGDO.
`plwcgdo=0 F`	Coefficient of the length time width dependence of CGDO.
`pocgso=6.39e-15(n)/6.36e-15(p) F`	Coefficient of the geometry-independent part of CGSO.
`plcgso=0 F`	Coefficient of the length dependence of CGSO.
`pwcgso=0 F`	Coefficient of the width dependence of CGSO.
`plwcgso=0 F`	Coefficient of the length times width dependence of CGSO.
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`ponfa=8.32e+22(n)/1.9e+22(p) 1/V m`^{4}	Coefficient of the geometry-independent part of NFA.
`plnfa=0 1/V m`^{4}	Coefficient of the length dependence of NFA.
`pwnfa=0 1/V m`^{4}	Coefficient of the width dependence of NFA.
`plwnfa=0 1/V m`^{4}	Coefficient of the length times width dependence of NFA.
`ponfb=2.51e+07(n)/5.04e+06(p) 1/V m`^{2}	Coefficient of the geometry-independent part of NFB.
`plnfb=0 1/V m`^{2}	Coefficient of the length dependence of NFB.
`pwnfb=0 1/V m`^{2}	Coefficient of the width dependence of NFB.
`plwnfb=0 1/V m`^{2}	Coefficient of the length times width dependence of NFB.
`ponfc=0(n)/3.63e-10(p) 1/V`	

© 2023 Cadence Design Systems, Inc.

	Coefficient of the geometry-independent part of NFC.
`plnfc=0 1/V`	Coefficient of the length dependence of NFC.
`pwnfc=0 1/V`	Coefficient of the width dependence of NFC.
`plwnfc=0 1/V`	Coefficient of the length times width dependence of NFC.
`potvfb=0.0005 V/K`	Coefficient of the geometry-independent part of STVFB.
`pltvfb=0 V/K`	Coefficient of the length dependence of STVFB.
`pwtvfb=0 V/K`	Coefficient of the width dependence of STVFB.
`plwtvfb=0 V/K`	Coefficient of the length times width dependence of STVFB.
`potphib=-0.00085 V/K`	
	Coefficient of the geometry-independent part of STPHIB.
`pltphib=0 V/K`	Coefficient of the length dependence of STPHIB.
`pwtphib=0 V/K`	Coefficient of the width dependence of STPHIB.
`plwtphib=0 V/K`	Coefficient of the length times width dependence of STPHIB.
`potetabet=1.3(n)/0.5(p)`	
	Coefficient of the geometry-independent part of ETABET.
`pltetabet=0`	Coefficient of the length dependence of ETABET.
`pwtetabet=0`	Coefficient of the width dependence of ETABET.
`plwtetabet=0`	Coefficient of the length times width dependence of ETABET.
`potetasr=0.65(n)/0.5(p)`	
	Coefficient of the geometry-independent part of ETASR.
`pltetasr=0`	Coefficient of the length dependence of ETASR.
`pwtetasr=0`	Coefficient of the width dependence of ETASR.
`plwtetasr=0`	Coefficient of the length times width dependence of ETASR.

© 2023 Cadence Design Systems, Inc.

`potetaph=1.35(n)/3.75(p)`	Coefficient of the geometry-independent part of ETAPH.
`pltetaph=0`	Coefficient of the length dependence of ETAPH.
`pwtetaph=0`	Coefficient of the width dependence of ETAPH.
`plwtetaph=0`	Coefficient of the length times width dependence of ETAPH.
`potetamob=0 1/K`	Coefficient of the geometry-independent part of STETAMOB.
`pltetamob=0 1/K`	Coefficient of the length dependence of STETAMOB.
`pwtetamob=0 1/K`	Coefficient of the width dependence of STETAMOB.
`plwtetamob=0 1/K`	Coefficient of the length times width dependence of STETAMOB.
`nu=2`	Exponent of field dependence of mobility model.
`potnuexp=5.25(n)/3.23(p)`	Coefficient of the geometry-independent part of NUEXP.
`pltnuexp=0`	Coefficient of the length dependence of NUEXP.
`pwtnuexp=0`	Coefficient of the width dependence of NUEXP.
`plwtnuexp=0`	Coefficient of the length times width dependence of NUEXP.
`potetar=0.95(n)/0.4(p)`	Coefficient of the geometry-independent part of ETAR.
`pltetar=0`	Coefficient of the length dependence of ETAR.
`pwtetar=0`	Coefficient of the width dependence of ETAR.
`plwtetar=0`	Coefficient of the length times width dependence of ETAR.
`potetasat=1.04(n)/0.86(p)`	Coefficient of the geometry-independent part of ETASAT.
`pltetasat=0`	Coefficient of the length dependence of ETASAT.

© 2023 Cadence Design Systems, Inc.

`pwtetasat=0`	Coefficient of the width dependence of ETASAT.
`plwtetasat=0`	Coefficient of the length times width dependence of ETASAT.
`pota1=0 1/K`	Coefficient of the geometry-independent part of STA1.
`plta1=0 1/K`	Coefficient of the length dependence of STA1.
`pwta1=0 1/K`	Coefficient of the width dependence of STA1.
`plwta1=0 1/K`	Coefficient of the length times width dependence of STA1.
`potbgidl=-0.000364 V/K`	Coefficient of the geometry-independent part of STBGIDL.
`pltbgidl=0 V/K`	Coefficient of the length dependence of STBGIDL.
`pwtbgidl=0 V/K`	Coefficient of the width dependence of STBGIDL.
`plwtbgidl=0 V/K`	Coefficient of the length times width dependence of STBGIDL.
`dta=0 K`	Temperature offset of the device.
`pocs=0`	Coefficient of the geometry-independent part of CS.
`plcs=0`	Coefficient of the length dependence of CS.
`pwcs=0`	Coefficient of the width dependence of CS.
`plwcs=0`	Coefficient of the length times width dependence of CS.
`potetacs=0`	Coefficient of the geometry-independent part of ETACS.
`pltetacs=0`	Coefficient of the length dependence of ETACS.
`pwtetacs=0`	Coefficient of the width dependence of ETACS.
`plwtetacs=0`	Coefficient of the length times width dependence of ETACS.
`rgo=0` Ω	Gate resistance.
`rint=0` Ω m^2	Contact resistance between silicide and poly.
`rvpoly=0` Ω m^2	Vertical poly resistance.
`rshg=0` Ω/Sqr	Gate electrode diffusion sheet resistance.

© 2023 Cadence Design Systems, Inc.

`dlsil=0 m`	Silicide extension over the physical gate length.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`scalelev=1.1e+04`	flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`mbeo=0.0`	DCmatch parameter.
`mvto=0.0`	Threshold mismatch intercept.
`tnom (C)`	Alias of tnom.
`tref (C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`int_s`	
`int_d`	

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.

© 2023 Cadence Design Systems, Inc.

`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).

© 2023 Cadence Design Systems, Inc.

cbs (F)	Capacitance (- d qb / d vs).
cbb (F)	Capacitance (d qb / d vb).
cgdol (F)	Gate-drain overlap capacitance of the actual transistor.
cgsol (F)	Gate-source overlap capacitance of the actual transistor.
weff (m)	Effective channel width for geometrical models.
leff (m)	Effective channel length for geometrical models.
rg (Ω)	Gate resistance.
u	Transistor gain (gm/gds).
rout (Ω)	Small-signal output resistance (1/gds).
vearly (V)	Equivalent Early voltage (iidl/gds).
keff (V)	Body effect parameter.
beff (A/V^2)	Gain factor.
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw (V/ Hz)	Input-referred RMS white noise voltage density.
sqrtsff (V/ Hz)	Input-referred RMS white noise voltage density at 1 kHz.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
Pdiss (W)	Dissipation.
TK (K)	Actual device temperature.
table_ids (A)	Current.
table_vth (V)	Threshold voltage including back-bias and drain-bias effects.
table_qg (Coul)	Charge at g node.
table_qd (Coul)	Charge at d node.
table_qb (Coul)	Charge at b node.
BET (A/V^2)	Gain factor.

© 2023 Cadence Design Systems, Inc.

ctype	Channel type (-1 for PMOS, +1 for NMOS).
von (V)	Signed vth (<0 for PMOS, >0 for NMOS).
pwr (W)	Power.
mos_region	MOS region. Possible values are off, sat, triode, and subth
diode_region	DIODE region. Possible values are off and on.

Related Topics

Philips Models

MOS Model 11, Level 1102 (mos11020)

MOS Model 11, Level 1102 (mos11020t)

MOS Model 11, Level 1102 (mos11021)

MOS Model 11, Level 1102 (mos1102e)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

mult=1	Number of devices in parallel.
printscaled=0	Print scaled parameter info if value not equal to zero.
trise=0 K	Difference between the local ambient and global ambient temperature.

© 2023 Cadence Design Systems, Inc.

`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos1102e parameter=value ...
```

Model Parameters

`level=1.1e+03`	Transistor Level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`tr=21 C`	Reference temperature.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of VFB.
`ko=0.5 √V`	Body-effect factor.
`kpinv=0 1/√V`	Inverse of body-effect factor of the poly-silicon gate.
`phib=0.95 V`	Surface potential at the onset of strong inversion.
`stphib=-0.00085 V/K`	Coefficient of the temperature dependency of PHIB.
`bet=0.00192(n)/0.000381(p) A/V^2`	Gain factor.
`etabet=1.3(n)/0.5(p)`	Exponent of the temperature dependence of the gain factor.

© 2023 Cadence Design Systems, Inc.

`thesr=0.356(n)/0.73(p) 1/V`

Mobility degradation parameter due to surface roughness scattering.

`etasr=0.65(n)/0.5(p)`

Exponent of the temperature dependence of THESR.

`theph=0.0129(n)/0.001(p) 1/V`

Mobility degradation parameter due to phonon scattering.

`etaph=1.35(n)/3.75(p)`

Exponent of the temperature dependence of THEPH.

`etamob=1.4(n)/3(p)`

Effective field parameter for dependence on depletion charge.

`stetamob=0 1/K` Coefficient of the temperature dependence of ETAMOB.

`nu=2` Exponent of field dependence of mobility model.

`nuexp=5.25(n)/3.23(p)`

Exponent of the temperature dependence of parameter NU.

`ther=0.0812(n)/0.079(p) 1/V`

Coefficient of series resistance.

`etar=0.95(n)/0.4(p)`

Exponent of the temperature dependence of THER.

`ther1=0 V` Numerator of gate voltage dependent part of series resistance.

`ther2=1 V` Denominator of gate voltage dependent part of series resistance.

`thesat=0.251(n)/0.173(p) 1/V`

Velocity saturation parameter due to optical/acoustic phonon scattering.

`etasat=1.04(n)/0.86(p)`

© 2023 Cadence Design Systems, Inc.

	Exponent of the temperature dependence of THESAT.
`theth=1e-05(n)/0(p) 1/V`^{3}	
	Coefficient of self-heating.
`sdibl=0.000853(n)/3.55e-05(p) 1/V`	
	Drain-induced barrier lowering parameter.
`mo=0`	Parameter for (short-channel) subthreshold slope.
`ssf=0.012(n)/0.01(p) 1/V`	
	Static-feedback parameter.
`alp=0.025`	Factor of channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`mexp=5`	Smoothing factor.
`a1=6.02(n)/6.86(p)`	
	Factor of the weak-avalanche current.
`sta1=0 1/K`	Coefficient of the temperature dependence of A1.
`a2=38(n)/57.3(p) V`	
	Exponent of the weak-avalanche current.
`a3=0.641(n)/0.425(p)`	
	Factor of the drain-source voltage above which weak-avalanche occurs.
`iginv=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) V`	
	Probability factor for intrinsic gate tunneling current in inversion.
`igacc=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.

© 2023 Cadence Design Systems, Inc.

`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igov=0 A/V`^{2}	Gain factor for Source/Drain overlap tunneling current.
`agidl=0 A/V`^{3}	Gain factor for gate-induced leakage current.
`bgidl=41 V`	Probability factor for gate-induced drain leakage current at reference temperature.
`stbgidl=-0.000364 V/K`	Coefficient of the temperature dependence of BGIDL.
`cgidl=0`	Factor for the lateral field dependence of the gate-induced leakage current.
`cox=2.98e-14(n)/2.72e-14(p) F`	Oxide capacitance for the intrinsic channel (* mult).
`cgdo=6.39e-15(n)/6.36e-15(p) F`	Oxide capacitance for the gate-drain overlap (* mult).
`cgso=6.39e-15(n)/6.36e-15(p) F`	Oxide capacitance for the gate-source overlap (* mult).
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`nfa=8.32e+22(n)/1.9e+22(p) 1/(Vm`^{4}`)`	First coefficient of the flicker noise.
`nfb=2.51e+07(n)/5.04e+06(p) 1/(Vm`^{2}`)`	Second coefficient of the flicker noise.
`nfc=0(n)/3.63e-10(p) 1/V`	Third coefficient of the flicker noise.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`dta=0 K`	Temperature offset of the device.
`cs=0`	Coefficient of Coulomb scattering.
`etacs=0`	Exponent of the temperature dependence of CS.
`rg=0 Ω`	Gate resistance.
`scalelev=1.1e+04`	Flag for eldo model.

© 2023 Cadence Design Systems, Inc.

type=n	Transistor gender. Possible values are n and p.
imax=1000 A	Explosion current.
mbe=0.0	DCmatch parameter.
mvt=0.0	Threshold mismatch intercept.
tnom (C)	alias of tnom.
tref (C)	Alias of tnom.
compatible=spectre	Encourage device equations to be compatible with a foreign simulator. Possible values are spectre, spice2, spice3, cdsspice, spiceplus, eldo, sspice, mica, and pspice.

Output Parameters

tempeff (C)	Effective temperature for a single device.
meff	Effective multiplicity factor (m-factor).
int_s	
int_d	

Operating-Point Parameters

ids (A)	Drain current, excluding avalanche and tunnel currents.
iavl (A)	Substrate current due to weak-avalanche.
igs (A)	Gate-to-source current due to direct tunneling.
igd (A)	Gate-to-drain current due to direct tunneling.
igb (A)	Gate-to-bulk current due to direct tunneling.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vsb (V)	Source-bulk voltage.
vto (V)	Zero-bias threshold voltage.

© 2023 Cadence Design Systems, Inc.

`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgdol (F)`	Gate-drain overlap capacitance of the actual transistor.
`cgsol (F)`	Gate-source overlap capacitance of the actual transistor.
`rg (Ω)`	Gate resistance.

© 2023 Cadence Design Systems, Inc.

u	Transistor gain (gm/gds).
rout (Ω)	Small-signal output resistance (1/gds).
vearly (V)	Equivalent Early voltage (|id|/gds).
keff ($\sqrt{V}$)	Body effect parameter.
beff (A/V^2)	Gain factor.
fug (Hz)	Unity gain frequency at actual bias (gm/(2*pi*cin)).
sqrtsfw ($V/\sqrt{Hz}$)	Input-referred RMS white noise voltage density.
sqrtsff ($V/\sqrt{Hz}$)	Input-referred RMS white noise voltage density at 1 kHz.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
table_ids (A)	Current.
table_vth (V)	Threshold voltage including back-bias and drain-bias effects.
table_qg (Coul)	Charge at g node.
table_qd (Coul)	Charge at d node.
table_qb (Coul)	Charge at b node.
ctype	Channel type (-1 for PMOS, +1 for NMOS).
von (V)	Signed vth (<0 for PMOS, >0 for NMOS).
mos_region=SUBTHRESHOLD	MOS region. Possible values are off, sat, triode, and subth.
diode_region=ON	DIODE region. Possible values are off and on.

Related Topics

Philips Models

MOS Model 11, Level 1102 (mos1102et)

© 2023 Cadence Design Systems, Inc.

MOS Model 11, Level 1102 (mos1102et)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos1102et parameter=value ...
```

Model Parameters

`level=1.1e+03`	Transistor Level.
`paramchk=0`	Level of clip warning info.

© 2023 Cadence Design Systems, Inc.

`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`tr=21 C`	Reference temperature.
`vfb=-1.05 V`	Flat-band voltage at reference temperature.
`stvfb=0.0005 V/K`	Coefficient of temperature dependence of VFB.
`ko=0.5 |V`	Body-effect factor.
`kpinv=0 1/|V`	Inverse of body-effect factor of the poly-silicon gate.
`phib=0.95 V`	Surface potential at the onset of strong inversion.
`stphib=-0.00085 V/K`	Coefficient of the temperature dependency of PHIB.
`bet=0.00192(n)/0.000381(p) A/V`^{2}	Gain factor.
`etabet=1.3(n)/0.5(p)`	Exponent of the temperature dependence of the gain factor.
`thesr=0.356(n)/0.73(p) 1/V`	Mobility degradation parameter due to surface roughness scattering.
`etasr=0.65(n)/0.5(p)`	Exponent of the temperature dependence of THESR.
`theph=0.0129(n)/0.001(p) 1/V`	Mobility degradation parameter due to phonon scattering.
`etaph=1.35(n)/3.75(p)`	Exponent of the temperature dependence of THEPH.
`etamob=1.4(n)/3(p)`	Effective field parameter for dependence on depletion charge.

© 2023 Cadence Design Systems, Inc.

`stetamob=0 1/K`	Coefficient of the temperature dependence of ETAMOB.
`nu=2`	Exponent of field dependence of mobility model.
`nuexp=5.25(n)/3.23(p)`	Exponent of the temperature dependence of parameter NU.
`ther=0.0812(n)/0.079(p) 1/V`	Coefficient of series resistance.
`etar=0.95(n)/0.4(p)`	Exponent of the temperature dependence of THER.
`ther1=0 V`	Numerator of gate voltage dependent part of series resistance.
`ther2=1 V`	Denominator of gate voltage dependent part of series resistance.
`thesat=0.251(n)/0.173(p) 1/V`	Velocity saturation parameter due to optical/acoustic phonon scattering.
`etasat=1.04(n)/0.86(p)`	Exponent of the temperature dependence of THESAT.
`theth=1e-05(n)/0(p) 1/V`^{3}	Coefficient of self-heating.
`sdibl=0.000853(n)/3.55e-05(p) 1/|V`	Drain-induced barrier lowering parameter.
`mo=0`	Parameter for (short-channel) subthreshold slope.
`ssf=0.012(n)/0.01(p) 1/|V`	Static-feedback parameter.
`alp=0.025`	Factor of channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel-length modulation.
`mexp=5`	Smoothing factor.
`a1=6.02(n)/6.86(p)`	

© 2023 Cadence Design Systems, Inc.

	Factor of the weak-avalanche current.
`sta1=0 1/K`	Coefficient of the temperature dependence of A1.
`a2=38(n)/57.3(p) V`	
	Exponent of the weak-avalanche current.
`a3=0.641(n)/0.425(p)`	
	Factor of the drain-source voltage above which weak-avalanche occurs.
`iginv=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in inversion.
`binv=48(n)/87.5(p) V`	
	Probability factor for intrinsic gate tunneling current in inversion.
`igacc=0 A/V`^{2}	Gain factor for intrinsic gate tunneling current in accumulation.
`bacc=48 V`	Probability factor for intrinsic gate tunneling current in accumulation.
`vfbov=0 V`	Flat-band voltage for the Source/Drain overlap extensions.
`kov=2.5 V`	Body-effect factor for the Source/Drain overlap extensions.
`igov=0 A/V`^{2}	Gain factor for Source/Drain overlap tunneling current.
`agidl=0 A/V`^{3}	Gain factor for gate-induced leakage current.
`bgidl=41 V`	Probability factor for gate-induced drain leakage current at reference temperature.
`stbgidl=-0.000364 V/K`	
	Coefficient of the temperature dependence of BGIDL.
`cgidl=0`	Factor for the lateral field dependence of the gate-induced leakage current.
`cox=2.98e-14(n)/2.72e-14(p) F`	
	Oxide capacitance for the intrinsic channel (* mult).
`cgdo=6.39e-15(n)/6.36e-15(p) F`	
	Oxide capacitance for the gate-drain overlap (* mult).

© 2023 Cadence Design Systems, Inc.

`cgso=6.39e-15(n)/6.36e-15(p) F`	Oxide capacitance for the gate-source overlap (* mult).
`gatenoise=0`	Flag for in/exclusion of induced gate thermal noise.
`nt=1.62e-20 J`	Thermal noise coefficient.
`nfa=8.32e+22(n)/1.9e+22(p) 1/(Vm`^{4}`)`	First coefficient of the flicker noise.
`nfb=2.51e+07(n)/5.04e+06(p) 1/(Vm`^{2}`)`	Second coefficient of the flicker noise.
`nfc=0(n)/3.63e-10(p) 1/V`	Third coefficient of the flicker noise.
`tox=3.2e-09 m`	Thickness of gate oxide layer.
`dta=0 K`	Temperature offset of the device.
`cs=0`	Coefficient of Coulomb scattering.
`etacs=0`	Exponent of the temperature dependence of CS.
`rg=0` Ω	Gate resistance.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`scalelev=1.1e+04`	Flag for eldo model.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`mbe=0.0`	DCmatch parameter.
`mvt=0.0`	Threshold mismatch intercept.
`tnom (C)`	Alias of tnom.
`tref (C)`	Alias of tnom.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`igs (A)`	Gate-to-source current due to direct tunneling.
`igd (A)`	Gate-to-drain current due to direct tunneling.
`igb (A)`	Gate-to-bulk current due to direct tunneling.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vdss (V)`	Drain saturation voltage at actual bias.
`vsat (V)`	Saturation limit.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).

© 2023 Cadence Design Systems, Inc.

`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`cgdol (F)`	Gate-drain overlap capacitance of the actual transistor.
`cgsol (F)`	Gate-source overlap capacitance of the actual transistor.
`rg (Ω)`	Gate resistance.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (iidl/gds).
`keff (√V )`	Body effect parameter.
`beff (A/V^2)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`sqrtsfw (V/√Hz )`	Input-referred RMS white noise voltage density.
`sqrtsff (V/√Hz )`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`Pdiss (W)`	Dissipation.

© 2023 Cadence Design Systems, Inc.

TK (K)	Actual device temperature.
table_ids (A)	Current.
table_vth (V)	Threshold voltage including back-bias and drain-bias effects.
table_qg (Coul)	Charge at g node.
table_qd (Coul)	Charge at d node.
table_qb (Coul)	Charge at b node.
ctype	Channel type (-1 for PMOS, +1 for NMOS).
von (V)	Signed vth (<0 for PMOS, >0 for NMOS).
pwr (W)	Power.
mos_region	MOS region. Possible values are off, sat, triode, and subth
diode_region	DIODE region. Possible values are off and on.

Related Topics

Philips Models

MOS Model 11, Level 1102 (mos1102e)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)

This is SimKit 3.7.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

w=2e-05 m	Drawn width of the channel region.
wd=2e-05 m	Drawn width of the drift region.
mult=1	Number of devices in parallel.
region=triode	Estimated DC operating region, used as a convergence aid. Possible values are off, triode, sat, and subth.
m=1	alias of mult.
mos_region=SUBTHRESHOLD	
diode_region=ON	
trise=0	Temperature rise from ambient.

Model Syntax

```
model modelName mos2001 parameter=value ...
```

Model Parameters

level=2e+03	Must be 2001.
paramchk=0	Level of clip warning info.
wvar=0 m	Width offset of the channel region.
wdvar=0 m	Width offset of the drift region.
tref=25 deg. C	Reference temperature.
vfb=-1 V	Flatband voltage of the channel region, at reference temperature.
stvfb=0 V/K	Temperature scaling coefficient for VFB.
vfbd=-0.1 V	Flatband voltage of the drift region, at reference temperature.
stvfbd=0 V/K	Temperature scaling coefficient for the flatband voltage of the drift region.
kor=1.6 V^1/2	Body factor of the channel region of an infinitely wide transistor.

© 2023 Cadence Design Systems, Inc.

swko=0	Width scaling coefficient for KO.
kodr=1 V^1/2	Body factor of the drift region of an infinitely wide transistor.
swkod=0	Width scaling coefficient for the body factor of the drift region.
phib=0.86 V	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
stphib=-0.0012 V/K	Temperature scaling coefficient for PHIB.
phibd=0.78 V	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
stphibd=-0.0012 V/K	Temperature scaling coefficient for PHIBD.
betw=7e-05 A/V^2	Gain factor of a channel region of 1 um wide, at reference temperature.
etabet=1.6	Temperature scaling exponent for BET.
betaccw=7e-05 A/V^{-2}	Gain factor of drift region of 1 um wide, at reference temperature.
etabetacc=1.5	Temperature scaling exponent for BETACC.
rdw=4e+03 Ω	On-resistance of a drift region of 1 um wide, at reference temperature.
etard=1.5	Temperature scaling exponent for RD.
lamd=0.2	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
the1r=0.09 V^-1	Mobility reduction coefficient of infinitely wide transistor, due to vertical strong-inversion field in a channel region.
swthe1=0	Width scaling coefficient for THE1.
the1acc=0.02 V^-1	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
the2r=0.03 V^(-1/2)	

© 2023 Cadence Design Systems, Inc.

	Mobility reduction coefficient for VSB > 0 of an infinitely wide transistor, due to vertical depletion field in channel region.
`swthe2=0`	Width scaling coefficient for THE2.
`the3r=0.4 V^-1`	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation.
`etathe3=1`	Temperature scaling exponent for THE3.
`swthe3=0`	Width scaling coefficient for THE3.
`mexp=2`	Smoothing factor for transition from linear to saturation regime.
`alp=0.002`	Factor for channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel length modulation.
`sdibl=0.001 V^(-1/2)`	
	Factor for drain-induced barrier lowering.
`msdibl=3`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo=0 V`	Parameter for the (short-channel) sub-threshold slope.
`ssf=1e-12 V^(-1/2)`	
	Factor for static feedback.
`a1r=15`	Factor of weak avalanche current of an infinitely wide transistor, at reference temperature.
`sta1=0 K^-1`	Temperature scaling coefficient for A1.
`swa1=0`	Width scaling coefficient for A1.
`a2=73 V`	Exponent of weak avalanche current.
`a3=0.8`	Factor of the drain-source voltage above which weak avalanche occurs.
`coxw=7.5e-16 F`	Oxide capacitance for an intrinsic channel region of 1um wide.
`coxdw=7.5e-16 F`	Oxide capacitance for an intrinsic drift region of 1um wide.
`cgdow=0 F`	Gate-to-drain overlap capacitance for a drift region of 1 um wide.

© 2023 Cadence Design Systems, Inc.

`cgsow=0 F`	Gate-to-source overlap capacitance for a channel region of 1 um wide.
`nt=1.65e-20 J`	Coefficient of thermal noise, at reference temperature.
`nfaw=1.4e+25 V^-1 m^-4`	First coefficient of flicker noise for a channel region of 1 um wide.
`nfbw=2e+08 V^-1 m`$^{-2}$	Second coefficient of flicker noise for a channel region of 1 um wide.
`nfcw=0 V^-1`	Third coefficient of flicker noise for a channel region of 1 um wide.
`tox=3.8e-08 m`	Thickness of the oxide above the channel region.
`dta=0 K`	Temperature offset to the ambient temperature.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.

Output Parameters

`vfb (V)`	Flatband voltage of the channel region, at reference temperature.
`vfbd (V)`	Flatband voltage of the drift region.
`ko (V^1/2)`	Body factor of the channel region.
`kod (V^1/2)`	Body factor of the drift region.
`phib (V)`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`phibd (V)`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.

© 2023 Cadence Design Systems, Inc.

`bet (A/V^2)`	Gain factor of the channel region, at reference temperature.
`betacc (A/V^2)`	Gain factor for accumulation in the drift region, at reference temperature.
`rd (Ω)`	On-resistance of the drift region, at reference temperature.
`lamd`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1 (V^-1)`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc (V^-1)`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2 (V^-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3 (V^-1)`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`mexp`	Smoothing factor for transition from linear to saturation regime.
`alp`	Factor for channel length modulation.
`vp (V)`	Characteristic voltage of channel length modulation.
`sdibl (V^-1/2)`	Factor for drain-induced barrier lowering.
`msdibl`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo (V)`	Parameter for the (short-channel) sub-threshold slope.
`ssf (V^-1/2)`	Factor for static feedback.
`a1`	Factor of weak avalanche current, at reference temperature.
`a2 (V)`	Exponent of weak avalanche current.
`a3`	Factor of the drain-source voltage above which weak avalanche occurs.
`cox (F)`	Oxide capacitance for the intrinsic channel region.

© 2023 Cadence Design Systems, Inc.

coxd (F)	Oxide capacitance for the intrinsic drift region.
cgdo (F)	Gate-to-drain overlap capacitance.
cgso (F)	Gate-to-source overlap capacitance.
nt (J)	Coefficient of thermal noise, at reference temperature.
nfa (V^-1 m^-4)	First coefficient of flicker noise.
nfb (V^-1 m^{-2})	Second coefficient of flicker noise.
nfc (V^-1)	Third coefficient of flicker noise.
tox (m)	Thickness of the oxide above the channel region.
int_s	
int_d	

Operating-Point Parameters

ids (A)	Drain current, excluding avalanche and tunnel currents.
iavl (A)	Substrate current due to weak-avalanche.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vsb (V)	Source-bulk voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back-bias effects.
vth (V)	Threshold voltage including back-bias and drain-bias effects.
vgt (V)	Effective gate drive voltage including back-bias and drain voltage effects.
vtod (V)	Threshold voltage of the drift region.
vdiseff (V)	Effective internal drain-to-source voltage at actual bias.
vdissat (V)	Internal drain saturation voltage at actual bias.
vdssat (V)	Drain-source saturation voltage at actual bias.
gm (A/V)	Transconductance (d ids / d vgs).

© 2023 Cadence Design Systems, Inc.

`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`weff (m)`	Effective channel width for geometrical models.
`wdeff (m)`	Effective drift region width for geometrical model.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|idl/gds).
`beff (A/V`^{2}`)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`gmmos (A/V)`	Transconductance of channel region.
`sqrtsfw (V/Hz^1/2)`	Input-referred RMS white noise voltage density.
`sqrtsff (V/Hz^1/2)`	

© 2023 Cadence Design Systems, Inc.

	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Related Topics

Philips Models

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)

This is SimKit 3.7.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	
`trise=0`	Temperature rise from ambient.

Model Syntax

```
model modelName mos2001e parameter=value ...
```

Model Parameters

`level=2e+03`	Must be 2001.
`paramchk=0`	Level of clip warning info.
`tref=25 deg. C`	Reference temperature.
`vfb=-1 V`	Flatband voltage of the channel region, at reference temperature.
`stvfb=0 V/K`	Temperature scaling coefficient for VFB.
`vfbd=-0.1 V`	Flatband voltage of the drift region, at reference temperature.
`stvfbd=0 V/K`	Temperature scaling coefficient for the flatband voltage of the drift region.
`ko=1.6 V^1/2`	Body factor of the channel region.
`kod=1 V^1/2`	Body factor of the drift region.
`phib=0.86 V`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`stphib=-0.0012 V/K`	

© 2023 Cadence Design Systems, Inc.

	Temperature scaling coefficient for PHIB.
`phibd=0.78 V`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`stphibd=-0.0012 V/K`	
	Temperature scaling coefficient for PHIBD.
`bet=0.0014 A/V`^{2}	Gain factor of the channel region, at reference temperature.
`etabet=1.6`	Temperature scaling exponent for BET.
`betacc=0.0014 A/V`$^{-2}$	
	Gain factor for accumulation in the drift region, at reference temperature.
`etabetacc=1.5`	Temperature scaling exponent for BETACC.
`rd=200` Ω	On-resistance of the drift region, at reference temperature.
`etard=1.5`	Temperature scaling exponent for RD.
`lamd=0.2`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1=0.09 V^-1`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc=0.02 V^-1`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2=0.03 V^(-1/2)`	
	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3=0.4 V^-1`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`etathe3=1`	Temperature scaling exponent for THE3.
`mexp=2`	Smoothing factor for transition from linear to saturation regime.
`alp=0.002`	Factor for channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel length modulation.

© 2023 Cadence Design Systems, Inc.

`sdibl=0.001 V^(-1/2)`	
	Factor for drain-induced barrier lowering.
`msdibl=3`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo=0 V`	Parameter for the (short-channel) sub-threshold slope.
`ssf=1e-12 V^(-1/2)`	
	Factor for static feedback.
`a1=15`	Factor of weak avalanche current, at reference temperature.
`sta1=0 K^-1`	Temperature scaling coefficient for A1.
`a2=73 V`	Exponent of weak avalanche current.
`a3=0.8`	Factor of the drain-source voltage above which weak avalanche occurs.
`cox=1.5e-14 F`	Oxide capacitance for the intrinsic channel region.
`coxd=1.5e-14 F`	Oxide capacitance for the intrinsic drift region.
`cgdo=0 F`	Gate-to-drain overlap capacitance.
`cgso=0 F`	Gate-to-source overlap capacitance.
`nt=1.65e-20 J`	Coefficient of thermal noise, at reference temperature.
`nfa=7e+23 V^-1 m^-4`	
	First coefficient of flicker noise.
`nfb=1e+07 V^-1 m`$^{-2}$	
	Second coefficient of flicker noise.
`nfc=0 V^-1`	Third coefficient of flicker noise.
`tox=3.8e-08 m`	Thickness of the oxide above the channel region.
`dta=0 K`	Temperature offset to the ambient temperature.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.
`tnom (deg. C)`	Alias of tnom.

© 2023 Cadence Design Systems, Inc.

`tr (deg. C)`	Alias of tnom.

Output Parameters

`vfb (V)`	Flatband voltage of the channel region, at reference temperature.
`vfbd (V)`	Flatband voltage of the drift region.
`ko (V^1/2)`	Body factor of the channel region.
`kod (V^1/2)`	Body factor of the drift region.
`phib (V)`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`phibd (V)`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`bet (A/V`^{2}`)`	Gain factor of the channel region, at reference temperature.
`betacc (A/V`^{2}`)`	Gain factor for accumulation in the drift region, at reference temperature.
`rd (Ω)`	On-resistance of the drift region, at reference temperature.
`lamd`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1 (V^-1)`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc (V^-1)`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2 (V^-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3 (V^-1)`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`mexp`	Smoothing factor for transition from linear to saturation regime.

© 2023 Cadence Design Systems, Inc.

alp	Factor for channel length modulation.
vp (V)	Characteristic voltage of channel length modulation.
sdibl (V^-1/2)	Factor for drain-induced barrier lowering.
msdibl	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
mo (V)	Parameter for the (short-channel) sub-threshold slope.
ssf (V^-1/2)	Factor for static feedback.
a1	Factor of weak avalanche current, at reference temperature.
a2 (V)	Exponent of weak avalanche current.
a3	Factor of the drain-source voltage above which weak avalanche occurs.
cox (F)	Oxide capacitance for the intrinsic channel region.
coxd (F)	Oxide capacitance for the intrinsic drift region.
cgdo (F)	Gate-to-drain overlap capacitance.
cgso (F)	Gate-to-source overlap capacitance.
nt (J)	Coefficient of thermal noise, at reference temperature.
nfa (V^-1 m^-4)	First coefficient of flicker noise.
nfb (V^-1 m^{-2})	Second coefficient of flicker noise.
nfc (V^-1)	Third coefficient of flicker noise.
tox (m)	Thickness of the oxide above the channel region.
int_s	
int_d	

Operating-Point Parameters

ids (A)	Drain current, excluding avalanche and tunnel currents.
iavl (A)	Substrate current due to weak-avalanche.
vds (V)	Drain-source voltage.

© 2023 Cadence Design Systems, Inc.

`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vtod (V)`	Threshold voltage of the drift region.
`vdiseff (V)`	Effective internal drain-to-source voltage at actual bias.
`vdissat (V)`	Internal drain saturation voltage at actual bias.
`vdssat (V)`	Drain-source saturation voltage at actual bias.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).

© 2023 Cadence Design Systems, Inc.

`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (lidl/gds).
`beff (A/V`^{2}`)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`gmmos (A/V)`	Transconductance of channel region.
`sqrtsfw (V/Hz^1/2)`	Input-referred RMS white noise voltage density.
`sqrtsff (V/Hz^1/2)`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Related Topics

Philips Models

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)

© 2023 Cadence Design Systems, Inc.

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)

This is SimKit 3.7.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`trise=0`	Temperature rise from ambient.

Model Syntax

```
model modelName mos2001et parameter=value ...
```

Model Parameters

`level=2e+03`	Must be 2001.
`paramchk=0`	Level of clip warning info.
`tref=25 deg. C`	Reference temperature.
`vfb=-1 V`	Flatband voltage of the channel region, at reference temperature.
`stvfb=0 V/K`	Temperature scaling coefficient for VFB.

© 2023 Cadence Design Systems, Inc.

`vfbd=-0.1 V`	Flatband voltage of the drift region, at reference temperature.
`stvfbd=0 V/K`	Temperature scaling coefficient for the flatband voltage of the drift region.
`ko=1.6 V^1/2`	Body factor of the channel region.
`kod=1 V^1/2`	Body factor of the drift region.
`phib=0.86 V`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`stphib=-0.0012 V/K`	Temperature scaling coefficient for PHIB.
`phibd=0.78 V`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`stphibd=-0.0012 V/K`	Temperature scaling coefficient for PHIBD.
`bet=0.0014 A/V`^{2}	Gain factor of the channel region, at reference temperature.
`etabet=1.6`	Temperature scaling exponent for BET.
`betacc=0.0014 A/V`$^{-2}$	Gain factor for accumulation in the drift region, at reference temperature.
`etabetacc=1.5`	Temperature scaling exponent for BETACC.
`rd=200` Ω	On-resistance of the drift region, at reference temperature.
`etard=1.5`	Temperature scaling exponent for RD.
`lamd=0.2`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1=0.09 V^-1`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc=0.02 V^-1`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2=0.03 V^(-1/2)`	

© 2023 Cadence Design Systems, Inc.

	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3=0.4 V^-1`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`etathe3=1`	Temperature scaling exponent for THE3.
`mexp=2`	Smoothing factor for transition from linear to saturation regime.
`alp=0.002`	Factor for channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel length modulation.
`sdibl=0.001 V^(-1/2)`	
	Factor for drain-induced barrier lowering.
`msdibl=3`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo=0 V`	Parameter for the (short-channel) sub-threshold slope.
`ssf=1e-12 V^(-1/2)`	
	Factor for static feedback.
`a1=15`	Factor of weak avalanche current, at reference temperature.
`sta1=0 K^-1`	Temperature scaling coefficient for A1.
`a2=73 V`	Exponent of weak avalanche current.
`a3=0.8`	Factor of the drain-source voltage above which weak avalanche occurs.
`cox=1.5e-14 F`	Oxide capacitance for the intrinsic channel region.
`coxd=1.5e-14 F`	Oxide capacitance for the intrinsic drift region.
`cgdo=0 F`	Gate-to-drain overlap capacitance.
`cgso=0 F`	Gate-to-source overlap capacitance.
`nt=1.65e-20 J`	Coefficient of thermal noise, at reference temperature.
`nfa=7e+23 V^-1 m^-4`	
	First coefficient of flicker noise.

© 2023 Cadence Design Systems, Inc.

`nfb=1e+07 V^-1 m^-2`	
	Second coefficient of flicker noise.
`nfc=0 V^-1`	Third coefficient of flicker noise.
`tox=3.8e-08 m`	Thickness of the oxide above the channel region.
`dta=0 K`	Temperature offset to the ambient temperature.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.

Output Parameters

`vfb (V)`	Flatband voltage of the channel region, at reference temperature.
`vfbd (V)`	Flatband voltage of the drift region.
`ko (V^1/2)`	Body factor of the channel region.
`kod (V^1/2)`	Body factor of the drift region.
`phib (V)`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`phibd (V)`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`bet (A/V^2)`	Gain factor of the channel region, at reference temperature.
`betacc (A/V^2)`	Gain factor for accumulation in the drift region, at reference temperature.

© 2023 Cadence Design Systems, Inc.

`rd (Ω)`	On-resistance of the drift region, at reference temperature.
`lamd`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1 (V^-1)`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc (V^-1)`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2 (V^-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3 (V^-1)`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`mexp`	Smoothing factor for transition from linear to saturation regime.
`alp`	Factor for channel length modulation.
`vp (V)`	Characteristic voltage of channel length modulation.
`sdibl (V^-1/2)`	Factor for drain-induced barrier lowering.
`msdibl`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo (V)`	Parameter for the (short-channel) sub-threshold slope.
`ssf (V^-1/2)`	Factor for static feedback.
`a1`	Factor of weak avalanche current, at reference temperature.
`a2 (V)`	Exponent of weak avalanche current.
`a3`	Factor of the drain-source voltage above which weak avalanche occurs.
`cox (F)`	Oxide capacitance for the intrinsic channel region.
`coxd (F)`	Oxide capacitance for the intrinsic drift region.
`cgdo (F)`	Gate-to-drain overlap capacitance.
`cgso (F)`	Gate-to-source overlap capacitance.
`nt (J)`	Coefficient of thermal noise, at reference temperature.

© 2023 Cadence Design Systems, Inc.

`nfa (V^-1 m^-4)`	First coefficient of flicker noise.
`nfb (V^-1 m^-2)`	Second coefficient of flicker noise.
`nfc (V^-1)`	Third coefficient of flicker noise.
`tox (m)`	Thickness of the oxide above the channel region.
`rth (K/W)`	Thermal resistance.
`cth (J/K)`	Thermal capacitance.
`int_s`	
`int_d`	

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vtod (V)`	Threshold voltage of the drift region.
`vdiseff (V)`	Effective internal drain-to-source voltage at actual bias.
`vdissat (V)`	Internal drain saturation voltage at actual bias.
`vdssat (V)`	Drain-source saturation voltage at actual bias.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).

© 2023 Cadence Design Systems, Inc.

`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (lidl/gds).
`beff (A/V^2)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`gmmos (A/V)`	Transconductance of channel region.
`sqrtsfw (V/Hz^1/2)`	Input-referred RMS white noise voltage density.
`sqrtsff (V/Hz^1/2)`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual temperature.
`pwr (W)`	Power.

Related Topics

Philips Models

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)

© 2023 Cadence Design Systems, Inc.

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)

This is SimKit 3.7.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

`w=2e-05 m`	Drawn width of the channel region.
`wd=2e-05 m`	Drawn width of the drift region.
`mult=1`	Number of devices in parallel.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	
`trise=0`	Temperature rise from ambient.

Model Syntax

```
model modelName mos2001t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=2e+03`	Must be 2001.
`paramchk=0`	Level of clip warning info.
`wvar=0 m`	Width offset of the channel region.
`wdvar=0 m`	Width offset of the drift region.
`tref=25 deg. C`	Reference temperature.
`vfb=-1 V`	Flatband voltage of the channel region, at reference temperature.
`stvfb=0 V/K`	Temperature scaling coefficient for VFB.
`vfbd=-0.1 V`	Flatband voltage of the drift region, at reference temperature.
`stvfbd=0 V/K`	Temperature scaling coefficient for the flatband voltage of the drift region.
`kor=1.6 V^1/2`	Body factor of the channel region of an infinitely wide transistor.
`swko=0`	Width scaling coefficient for KO.
`kodr=1 V^1/2`	Body factor of the drift region of an infinitely wide transistor.
`swkod=0`	Width scaling coefficient for the body factor of the drift region.
`phib=0.86 V`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`stphib=-0.0012 V/K`	Temperature scaling coefficient for PHIB.
`phibd=0.78 V`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`stphibd=-0.0012 V/K`	Temperature scaling coefficient for PHIBD.
`betw=7e-05 A/V`^{2}	Gain factor of a channel region of 1 um wide, at reference temperature.
`etabet=1.6`	Temperature scaling exponent for BET.
`betaccw=7e-05 A/V`$^{-2}$	

© 2023 Cadence Design Systems, Inc.

	Gain factor of drift region of 1 um wide, at reference temperature.
`etabetacc=1.5`	Temperature scaling exponent for BETACC.
`rdw=4e+03 Ω`	On-resistance of a drift region of 1 um wide, at reference temperature.
`etard=1.5`	Temperature scaling exponent for RD.
`lamd=0.2`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1r=0.09 V^-1`	Mobility reduction coefficient of infinitely wide transistor, due to vertical strong-inversion field in a channel region.
`swthe1=0`	Width scaling coefficient for THE1.
`the1acc=0.02 V^-1`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2r=0.03 V^(-1/2)`	
	Mobility reduction coefficient for VSB > 0 of an infinitely wide transistor, due to vertical depletion field in channel region.
`swthe2=0`	Width scaling coefficient for THE2.
`the3r=0.4 V^-1`	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation.
`etathe3=1`	Temperature scaling exponent for THE3.
`swthe3=0`	Width scaling coefficient for THE3.
`mexp=2`	Smoothing factor for transition from linear to saturation regime.
`alp=0.002`	Factor for channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel length modulation.
`sdibl=0.001 V^(-1/2)`	
	Factor for drain-induced barrier lowering.
`msdibl=3`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo=0 V`	Parameter for the (short-channel) sub-threshold slope.

© 2023 Cadence Design Systems, Inc.

`ssf=1e-12 V^(-1/2)`	Factor for static feedback.
`a1r=15`	Factor of weak avalanche current of an infinitely wide transistor, at reference temperature.
`sta1=0 K^-1`	Temperature scaling coefficient for A1.
`swa1=0`	Width scaling coefficient for A1.
`a2=73 V`	Exponent of weak avalanche current.
`a3=0.8`	Factor of the drain-source voltage above which weak avalanche occurs.
`coxw=7.5e-16 F`	Oxide capacitance for an intrinsic channel region of 1um wide.
`coxdw=7.5e-16 F`	Oxide capacitance for an intrinsic drift region of 1um wide.
`cgdow=0 F`	Gate-to-drain overlap capacitance for a drift region of 1 um wide.
`cgsow=0 F`	Gate-to-source overlap capacitance for a channel region of 1 um wide.
`nt=1.65e-20 J`	Coefficient of thermal noise, at reference temperature.
`nfaw=1.4e+25 V^-1 m^-4`	First coefficient of flicker noise for a channel region of 1 um wide.
`nfbw=2e+08 V^-1 m`$^{-2}$	Second coefficient of flicker noise for a channel region of 1 um wide.
`nfcw=0 V^-1`	Third coefficient of flicker noise for a channel region of 1 um wide.
`tox=3.8e-08 m`	Thickness of the oxide above the channel region.
`dta=0 K`	Temperature offset to the ambient temperature.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.

© 2023 Cadence Design Systems, Inc.

`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.

Output Parameters

`vfb (V)`	Flatband voltage of the channel region, at reference temperature.
`vfbd (V)`	Flatband voltage of the drift region.
`ko (V^1/2)`	Body factor of the channel region.
`kod (V^1/2)`	Body factor of the drift region.
`phib (V)`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`phibd (V)`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`bet (A/V`^{2}`)`	Gain factor of the channel region, at reference temperature.
`betacc (A/V`^{2}`)`	Gain factor for accumulation in the drift region, at reference temperature.
`rd (`Ω`)`	On-resistance of the drift region, at reference temperature.
`lamd`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1 (V^-1)`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc (V^-1)`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.

© 2023 Cadence Design Systems, Inc.

`the2 (V^-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3 (V^-1)`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`mexp`	Smoothing factor for transition from linear to saturation regime.
`alp`	Factor for channel length modulation.
`vp (V)`	Characteristic voltage of channel length modulation.
`sdibl (V^-1/2)`	Factor for drain-induced barrier lowering.
`msdibl`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo (V)`	Parameter for the (short-channel) sub-threshold slope.
`ssf (V^-1/2)`	Factor for static feedback.
`a1`	Factor of weak avalanche current, at reference temperature.
`a2 (V)`	Exponent of weak avalanche current.
`a3`	Factor of the drain-source voltage above which weak avalanche occurs.
`cox (F)`	Oxide capacitance for the intrinsic channel region.
`coxd (F)`	Oxide capacitance for the intrinsic drift region.
`cgdo (F)`	Gate-to-drain overlap capacitance.
`cgso (F)`	Gate-to-source overlap capacitance.
`nt (J)`	Coefficient of thermal noise, at reference temperature.
`nfa (V^-1 m^-4)`	First coefficient of flicker noise.
`nfb (V^-1 m`$^{-2}$`)`	Second coefficient of flicker noise.
`nfc (V^-1)`	Third coefficient of flicker noise.
`tox (m)`	Thickness of the oxide above the channel region.
`rth (K/W)`	Thermal resistance.
`cth (J/K)`	Thermal capacitance.

© 2023 Cadence Design Systems, Inc.

int_s
int_d

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vtod (V)`	Threshold voltage of the drift region.
`vdiseff (V)`	Effective internal drain-to-source voltage at actual bias.
`vdissat (V)`	Internal drain saturation voltage at actual bias.
`vdssat (V)`	Drain-source saturation voltage at actual bias.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).

© 2023 Cadence Design Systems, Inc.

`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`weff (m)`	Effective channel width for geometrical models.
`wdeff (m)`	Effective drift region width for geometrical model.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (lidl/gds).
`beff (A/V`^{2}`)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`gmmos (A/V)`	Transconductance of channel region.
`sqrtsfw (V/Hz^1/2)`	Input-referred RMS white noise voltage density.
`sqrtsff (V/Hz^1/2)`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual temperature.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Related Topics

Philips Models

© 2023 Cadence Design Systems, Inc.

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)

This is SimKit 3.7.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`mult=1`	Number of devices in parallel.
`w=2e-05 m`	Drawn width of the channel region.
`wd=2e-05 m`	Drawn width of the drift region.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	
`trise=0`	Temperature rise from ambient.

Model Syntax

```
model modelName mos2002 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=2e+03`	Must be 2002.
`paramchk=0`	Level of clip warning info.
`wvar=0 m`	Width offset of the channel region.
`wdvar=0 m`	Width offset of the drift region.
`tref=25 deg. C`	Reference temperature.
`vfb=-1 V`	Flatband voltage of the channel region, at reference temperature.
`stvfb=0 V/K`	Temperature scaling coefficient for VFB.
`vfbd=-0.1 V`	Flatband voltage of the drift region, at reference temperature.
`stvfbd=0 V/K`	Temperature scaling coefficient for the flatband voltage of the drift region.
`kor=1.6 V^1/2`	Body factor of the channel region of an infinitely wide transistor.
`swko=0`	Width scaling coefficient for KO.
`kodr=1 V^1/2`	Body factor of the drift region of an infinitely wide transistor.
`swkod=0`	Width scaling coefficient for the body factor of the drift region.
`phib=0.86 V`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`stphib=-0.0012 V/K`	Temperature scaling coefficient for PHIB.
`phibd=0.78 V`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`stphibd=-0.0012 V/K`	Temperature scaling coefficient for PHIBD.
`betw=7e-05 A/V`^{2}	Gain factor of a channel region of 1 um wide, at reference temperature.
`etabet=1.6`	Temperature scaling exponent for BET.
`betaccw=7e-05 A/V`$^{-2}$	

© 2023 Cadence Design Systems, Inc.

	Gain factor of drift region of 1 um wide, at reference temperature.
`etabetacc=1.5`	Temperature scaling exponent for BETACC.
`rdw=4e+03 Ω`	On-resistance of a drift region of 1 um wide, at reference temperature.
`etard=1.5`	Temperature scaling exponent for RD.
`lamd=0.2`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1r=0.09 V^-1`	Mobility reduction coefficient of infinitely wide transistor, due to vertical strong-inversion field in a channel region.
`swthe1=0`	Width scaling coefficient for THE1.
`the1acc=0.02 V^-1`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2r=0.03 V^(-1/2)`	
	Mobility reduction coefficient for VSB > 0 of an infinitely wide transistor, due to vertical depletion field in channel region.
`swthe2=0`	Width scaling coefficient for THE2.
`the3r=0.4 V^-1`	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation.
`etathe3=1`	Temperature scaling exponent for THE3.
`swthe3=0`	Width scaling coefficient for THE3.
`mexp=2`	Smoothing factor for transition from linear to saturation regime.
`the3dr=0 V^-1`	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation.
`etathe3d=1`	Temperature scaling exponent for THE3D.
`swthe3d=0`	Width scaling coefficient for THE3D.
`mexpd=2`	Smoothing factor for transition from linear to quasi-saturation regime.
`alp=0.002`	Factor for channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel length modulation.

© 2023 Cadence Design Systems, Inc.

`sdibl=0.001 V^(-1/2)`	Factor for drain-induced barrier lowering.
`msdibl=3`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo=0 V`	Parameter for the (short-channel) sub-threshold slope.
`ssf=1e-12 V^(-1/2)`	Factor for static feedback.
`a1chr=15`	Factor of channel weak avalanche current of an infinitely wide transistor, at reference temperature.
`sta1ch=0 K^-1`	Temperature scaling coefficient for A1CH.
`swa1ch=0`	Width scaling coefficient for A1CH.
`a2ch=73 V`	Exponent of channel weak avalanche current.
`a3ch=0.8`	Factor of the drain-source voltage above which channel weak avalanche occurs.
`a1drr=15`	Factor of drift weak avalanche current of an infinitely wide transistor, at reference temperature.
`sta1dr=0 K^-1`	Temperature scaling coefficient for A1DR.
`swa1dr=0`	Width scaling coefficient for A1DR.
`a2dr=73 V`	Exponent of drift weak avalanche current.
`a3dr=0.8`	Factor of the drain-source voltage above which drift weak avalanche occurs.
`coxw=7.5e-16 F`	Oxide capacitance for an intrinsic channel region of 1um wide.
`coxdw=7.5e-16 F`	Oxide capacitance for an intrinsic drift region of 1um wide.
`cgdow=0 F`	Gate-to-drain overlap capacitance for a drift region of 1 um wide.
`cgsow=0 F`	Gate-to-source overlap capacitance for a channel region of 1 um wide.
`nt=1.65e-20 J`	Coefficient of thermal noise, at reference temperature.
`nfaw=1.4e+25 V^-1 m^-4`	

© 2023 Cadence Design Systems, Inc.

	First coefficient of flicker noise for a channel region of 1 um wide.
`nfbw=2e+08 V^-1 m^-2`	
	Second coefficient of flicker noise for a channel region of 1 um wide.
`nfcw=0 V^-1`	Third coefficient of flicker noise for a channel region of 1 um wide.
`tox=3.8e-08 m`	Thickness of the oxide above the channel region.
`dta=0 K`	Temperature offset to the ambient temperature.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.

Output Parameters

`vfb (V)`	Flatband voltage of the channel region, at reference temperature.
`vfbd (V)`	Flatband voltage of the drift region.
`ko (V^1/2)`	Body factor of the channel region.
`kod (V^1/2)`	Body factor of the drift region.
`phib (V)`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`phibd (V)`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`bet (A/V^2)`	Gain factor of the channel region, at reference temperature.
`betacc (A/V^2)`	Gain factor for accumulation in the drift region, at reference temperature.

© 2023 Cadence Design Systems, Inc.

`rd (Ω)`	On-resistance of the drift region, at reference temperature.
`lamd`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1 (V^-1)`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc (V^-1)`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2 (V^-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3 (V^-1)`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`mexp`	Smoothing factor for transition from linear to saturation regime.
`the3d (V^-1)`	Mobility reduction coefficient in the drift region due to the horizontal electrical field caused by velocity saturation.
`mexpd`	Smoothing factor for transition from linear to quasi-saturation regime.
`alp`	Factor for channel length modulation.
`vp (V)`	Characteristic voltage of channel length modulation.
`sdibl (V^-1/2)`	Factor for drain-induced barrier lowering.
`msdibl`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo (V)`	Parameter for the (short-channel) sub-threshold slope.
`ssf (V^-1/2)`	Factor for static feedback.
`a1ch`	Factor of channel weak avalanche current, at reference temperature.
`a2ch (V)`	Exponent of channel weak avalanche current.
`a3ch`	Factor of the drain-source voltage above which channel weak avalanche occurs.

© 2023 Cadence Design Systems, Inc.

a1dr	Factor of drift weak avalanche current, at reference temperature.
a2dr (V)	Exponent of drift weak avalanche current.
a3dr	Factor of the drain-source voltage above which drift weak avalanche occurs.
cox (F)	Oxide capacitance for the intrinsic channel region.
coxd (F)	Oxide capacitance for the intrinsic drift region.
cgdo (F)	Gate-to-drain overlap capacitance.
cgso (F)	Gate-to-source overlap capacitance.
nt (J)	Coefficient of thermal noise.
nfa (V^-1 m^-4)	First coefficient of flicker noise.
nfb (V^-1 m^{-2})	Second coefficient of flicker noise.
nfc (V^-1)	Third coefficient of flicker noise.
tox (m)	Thickness of the oxide above the channel region.

Operating-Point Parameters

ids (A)	Drain current, excluding avalanche and tunnel currents.
iavl (A)	Substrate current due to weak-avalanche.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vsb (V)	Source-bulk voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back-bias effects.
vth (V)	Threshold voltage including back-bias and drain-bias effects.
vgt (V)	Effective gate drive voltage including back-bias and drain voltage effects.
vtod (V)	Threshold voltage of the drift region.

© 2023 Cadence Design Systems, Inc.

`vdiseff (V)`	Effective internal drain-to-source voltage at actual bias.
`vdissat (V)`	Saturation voltage of channel region at actual bias.
`vddisat (V)`	Saturation voltage of drift region at actual bias.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`weff (m)`	Effective channel width for geometrical models.
`wdeff (m)`	Effective drift region width for geometrical model.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (lidl/gds).
`beff (A/V`^{2}`)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).

© 2023 Cadence Design Systems, Inc.

`gmmos (A/V)`	Transconductance of channel region.
`sqrtsfw (V/Hz^1/2)`	Input-referred RMS white noise voltage density.
`sqrtsff (V/Hz^1/2)`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Related Topics

Philips Models

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)

This is SimKit 3.7.

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	
`trise=0`	Temperature rise from ambient.

Model Syntax

```
model modelName mos2002e parameter=value ...
```

Model Parameters

`level=2e+03`	Must be 2002.
`paramchk=0`	Level of clip warning info.
`tref=25 deg. C`	Reference temperature.
`vfb=-1 V`	Flatband voltage of the channel region, at reference temperature.
`stvfb=0 V/K`	Temperature scaling coefficient for VFB.
`vfbd=-0.1 V`	Flatband voltage of the drift region, at reference temperature.
`stvfbd=0 V/K`	Temperature scaling coefficient for the flatband voltage of the drift region.
`ko=1.6 V^1/2`	Body factor of the channel region.

© 2023 Cadence Design Systems, Inc.

`kod=1 V^1/2`	Body factor of the drift region.
`phib=0.86 V`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`stphib=-0.0012 V/K`	Temperature scaling coefficient for PHIB.
`phibd=0.78 V`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`stphibd=-0.0012 V/K`	Temperature scaling coefficient for PHIBD.
`bet=0.0014 A/V`^{2}	Gain factor of the channel region, at reference temperature.
`etabet=1.6`	Temperature scaling exponent for BET.
`betacc=0.0014 A/V`$^{-2}$	Gain factor for accumulation in the drift region, at reference temperature.
`etabetacc=1.5`	Temperature scaling exponent for BETACC.
`rd=200` Ω	On-resistance of the drift region, at reference temperature.
`etard=1.5`	Temperature scaling exponent for RD.
`lamd=0.2`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1=0.09 V^-1`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc=0.02 V^-1`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2=0.03 V^(-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3=0.4 V^-1`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`etathe3=1`	Temperature scaling exponent for THE3.

© 2023 Cadence Design Systems, Inc.

`mexp=2`	Smoothing factor for transition from linear to saturation regime.
`the3d=0 V^-1`	Mobility reduction coefficient in the drift region due to the horizontal electrical field caused by velocity saturation.
`etathe3d=1`	Temperature scaling exponent for THE3D.
`mexpd=2`	Smoothing factor for transition from linear to quasi-saturation regime.
`alp=0.002`	Factor for channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel length modulation.
`sdibl=0.001 V^(-1/2)`	Factor for drain-induced barrier lowering.
`msdibl=3`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo=0 V`	Parameter for the (short-channel) sub-threshold slope.
`ssf=1e-12 V^(-1/2)`	Factor for static feedback.
`a1ch=15`	Factor of channel weak avalanche current, at reference temperature.
`sta1ch=0 K^-1`	Temperature scaling coefficient for A1CH.
`a2ch=73 V`	Exponent of channel weak avalanche current.
`a3ch=0.8`	Factor of the drain-source voltage above which channel weak avalanche occurs.
`a1dr=15`	Factor of drift weak avalanche current, at reference temperature.
`sta1dr=0 K^-1`	Temperature scaling coefficient for A1DR.
`a2dr=73 V`	Exponent of drift weak avalanche current.
`a3dr=0.8`	Factor of the drain-source voltage above which drift weak avalanche occurs.
`cox=1.5e-14 F`	Oxide capacitance for the intrinsic channel region.
`coxd=1.5e-14 F`	Oxide capacitance for the intrinsic drift region.
`cgdo=0 F`	Gate-to-drain overlap capacitance.

© 2023 Cadence Design Systems, Inc.

`cgso=0 F`	Gate-to-source overlap capacitance.
`nt=1.65e-20 J`	Coefficient of thermal noise, at reference temperature.
`nfa=7e+23 V^-1 m^-4`	First coefficient of flicker noise.
`nfb=1e+07 V^-1 m`$^{-2}$	Second coefficient of flicker noise.
`nfc=0 V^-1`	Third coefficient of flicker noise.
`tox=3.8e-08 m`	Thickness of the oxide above the channel region.
`dta=0 K`	Temperature offset to the ambient temperature.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.

Output Parameters

`vfb (V)`	Flatband voltage of the channel region, at reference temperature.
`vfbd (V)`	Flatband voltage of the drift region.
`ko (V^1/2)`	Body factor of the channel region.
`kod (V^1/2)`	Body factor of the drift region.
`phib (V)`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`phibd (V)`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`bet (A/V`^{2}`)`	Gain factor of the channel region, at reference temperature.

© 2023 Cadence Design Systems, Inc.

`betacc (A/V^2)`	Gain factor for accumulation in the drift region, at reference temperature.
`rd (Ω)`	On-resistance of the drift region, at reference temperature.
`lamd`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1 (V^-1)`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc (V^-1)`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2 (V^-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3 (V^-1)`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`mexp`	Smoothing factor for transition from linear to saturation regime.
`the3d (V^-1)`	Mobility reduction coefficient in the drift region due to the horizontal electrical field caused by velocity saturation.
`mexpd`	Smoothing factor for transition from linear to quasi-saturation regime.
`alp`	Factor for channel length modulation.
`vp (V)`	Characteristic voltage of channel length modulation.
`sdibl (V^-1/2)`	Factor for drain-induced barrier lowering.
`msdibl`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo (V)`	Parameter for the (short-channel) sub-threshold slope.
`ssf (V^-1/2)`	Factor for static feedback.
`a1ch`	Factor of channel weak avalanche current, at reference temperature.
`a2ch (V)`	Exponent of channel weak avalanche current.

© 2023 Cadence Design Systems, Inc.

a3ch	Factor of the drain-source voltage above which channel weak avalanche occurs.
a1dr	Factor of drift weak avalanche current, at reference temperature.
a2dr (V)	Exponent of drift weak avalanche current.
a3dr	Factor of the drain-source voltage above which drift weak avalanche occurs.
cox (F)	Oxide capacitance for the intrinsic channel region.
coxd (F)	Oxide capacitance for the intrinsic drift region.
cgdo (F)	Gate-to-drain overlap capacitance.
cgso (F)	Gate-to-source overlap capacitance.
nt (J)	Coefficient of thermal noise.
nfa (V^-1 m^-4)	First coefficient of flicker noise.
nfb (V^-1 m^{-2})	Second coefficient of flicker noise.
nfc (V^-1)	Third coefficient of flicker noise.
tox (m)	Thickness of the oxide above the channel region.

Operating-Point Parameters

ids (A)	Drain current, excluding avalanche and tunnel currents.
iavl (A)	Substrate current due to weak-avalanche.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vsb (V)	Source-bulk voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back-bias effects.
vth (V)	Threshold voltage including back-bias and drain-bias effects.
vgt (V)	Effective gate drive voltage including back-bias and drain voltage effects.

© 2023 Cadence Design Systems, Inc.

`vtod (V)`	Threshold voltage of the drift region.
`vdiseff (V)`	Effective internal drain-to-source voltage at actual bias.
`vdissat (V)`	Saturation voltage of channel region at actual bias.
`vddisat (V)`	Saturation voltage of drift region at actual bias.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (lidl/gds).
`beff (A/V`^{2}`)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`gmmos (A/V)`	Transconductance of channel region.

© 2023 Cadence Design Systems, Inc.

`sqrtsfw (V/Hz^1/2)`	Input-referred RMS white noise voltage density.
`sqrtsff (V/Hz^1/2)`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Related Topics

Philips Models

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)

This is SimKit 3.7.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

mult=1	Number of devices in parallel.
region=triode	Estimated DC operating region, used as a convergence aid. Possible values are off, triode, sat, and subth.
m=1	Alias of mult.
trise=0	Temperature rise from ambient.

Model Syntax

```
model modelName mos2002et parameter=value ...
```

Model Parameters

evel=2e+03	Must be 2002.
paramchk=0	Level of clip warning info.
tref=25 deg. C	Reference temperature.
vfb=-1 V	Flatband voltage of the channel region, at reference temperature.
stvfb=0 V/K	Temperature scaling coefficient for VFB.
vfbd=-0.1 V	Flatband voltage of the drift region, at reference temperature.
stvfbd=0 V/K	Temperature scaling coefficient for the flatband voltage of the drift region.
ko=1.6 V^1/2	Body factor of the channel region.
kod=1 V^1/2	Body factor of the drift region.
phib=0.86 V	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
stphib=-0.0012 V/K	

© 2023 Cadence Design Systems, Inc.

	Temperature scaling coefficient for PHIB.
`phibd=0.78 V`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`stphibd=-0.0012 V/K`	
	Temperature scaling coefficient for PHIBD.
`bet=0.0014 A/V`^{2}	Gain factor of the channel region, at reference temperature.
`etabet=1.6`	Temperature scaling exponent for BET.
`betacc=0.0014 A/V`$^{-2}$	
	Gain factor for accumulation in the drift region, at reference temperature.
`etabetacc=1.5`	Temperature scaling exponent for BETACC.
`rd=200` Ω	On-resistance of the drift region, at reference temperature.
`etard=1.5`	Temperature scaling exponent for RD.
`lamd=0.2`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1=0.09 V^-1`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc=0.02 V^-1`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2=0.03 V^(-1/2)`	
	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3=0.4 V^-1`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`etathe3=1`	Temperature scaling exponent for THE3.
`mexp=2`	Smoothing factor for transition from linear to saturation regime.

© 2023 Cadence Design Systems, Inc.

`the3d=0 V^-1`	Mobility reduction coefficient in the drift region due to the horizontal electrical field caused by velocity saturation.
`etathe3d=1`	Temperature scaling exponent for THE3D.
`mexpd=2`	Smoothing factor for transition from linear to quasi-saturation regime.
`alp=0.002`	Factor for channel length modulation.
`vp=0.05 V`	Characteristic voltage of channel length modulation.
`sdibl=0.001 V^(-1/2)`	Factor for drain-induced barrier lowering.
`msdibl=3`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo=0 V`	Parameter for the (short-channel) sub-threshold slope.
`ssf=1e-12 V^(-1/2)`	Factor for static feedback.
`a1ch=15`	Factor of channel weak avalanche current, at reference temperature.
`sta1ch=0 K^-1`	Temperature scaling coefficient for A1CH.
`a2ch=73 V`	Exponent of channel weak avalanche current.
`a3ch=0.8`	Factor of the drain-source voltage above which channel weak avalanche occurs.
`a1dr=15`	Factor of drift weak avalanche current, at reference temperature.
`sta1dr=0 K^-1`	Temperature scaling coefficient for A1DR.
`a2dr=73 V`	Exponent of drift weak avalanche current.
`a3dr=0.8`	Factor of the drain-source voltage above which drift weak avalanche occurs.
`cox=1.5e-14 F`	Oxide capacitance for the intrinsic channel region.
`coxd=1.5e-14 F`	Oxide capacitance for the intrinsic drift region.
`cgdo=0 F`	Gate-to-drain overlap capacitance.
`cgso=0 F`	Gate-to-source overlap capacitance.

© 2023 Cadence Design Systems, Inc.

`nt=1.65e-20 J`	Coefficient of thermal noise, at reference temperature.
`nfa=7e+23 V^-1 m^-4`	First coefficient of flicker noise.
`nfb=1e+07 V^-1 m`$^{-2}$	Second coefficient of flicker noise.
`nfc=0 V^-1`	Third coefficient of flicker noise.
`tox=3.8e-08 m`	Thickness of the oxide above the channel region.
`dta=0 K`	Temperature offset to the ambient temperature.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`vbox=0.0 V`	Oxide breakdown voltage.
`vbds=0.0 V`	Drain-source breakdown voltage.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.

Output Parameters

`vfb (V)`	Flatband voltage of the channel region, at reference temperature.
`vfbd (V)`	Flatband voltage of the drift region.
`ko (V^1/2)`	Body factor of the channel region.
`kod (V^1/2)`	Body factor of the drift region.
`phib (V)`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`phibd (V)`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.

© 2023 Cadence Design Systems, Inc.

`bet (A/V^2)`	Gain factor of the channel region, at reference temperature.
`betacc (A/V^2)`	Gain factor for accumulation in the drift region, at reference temperature.
`rd (Ω)`	On-resistance of the drift region, at reference temperature.
`lamd`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1 (V^-1)`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc (V^-1)`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2 (V^-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3 (V^-1)`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`mexp`	Smoothing factor for transition from linear to saturation regime.
`the3d (V^-1)`	Mobility reduction coefficient in the drift region due to the horizontal electrical field caused by velocity saturation.
`mexpd`	Smoothing factor for transition from linear to quasi-saturation regime.
`alp`	Factor for channel length modulation.
`vp (V)`	Characteristic voltage of channel length modulation.
`sdibl (V^-1/2)`	Factor for drain-induced barrier lowering.
`msdibl`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo (V)`	Parameter for the (short-channel) sub-threshold slope.
`ssf (V^-1/2)`	Factor for static feedback.
`a1ch`	Factor of channel weak avalanche current, at reference temperature.

© 2023 Cadence Design Systems, Inc.

a2ch (V)	Exponent of channel weak avalanche current.
a3ch	Factor of the drain-source voltage above which channel weak avalanche occurs.
a1dr	Factor of drift weak avalanche current, at reference temperature.
a2dr (V)	Exponent of drift weak avalanche current.
a3dr	Factor of the drain-source voltage above which drift weak avalanche occurs.
cox (F)	Oxide capacitance for the intrinsic channel region.
coxd (F)	Oxide capacitance for the intrinsic drift region.
cgdo (F)	Gate-to-drain overlap capacitance.
cgso (F)	Gate-to-source overlap capacitance.
nt (J)	Coefficient of thermal noise.
nfa (V^-1 m^-4)	First coefficient of flicker noise.
nfb (V^-1 m^{-2})	Second coefficient of flicker noise.
nfc (V^-1)	Third coefficient of flicker noise.
tox (m)	Thickness of the oxide above the channel region.
rth (K/W)	Thermal resistance.
cth (J/K)	Thermal capacitance.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`ids (A)`	Drain current, excluding avalanche and tunnel currents.
`iavl (A)`	Substrate current due to weak-avalanche.
`vds (V)`	Drain-source voltage.
`vgs (V)`	Gate-source voltage.
`vsb (V)`	Source-bulk voltage.
`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vtod (V)`	Threshold voltage of the drift region.
`vdiseff (V)`	Effective internal drain-to-source voltage at actual bias.
`vdissat (V)`	Saturation voltage of channel region at actual bias.
`vddisat (V)`	Saturation voltage of drift region at actual bias.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).

© 2023 Cadence Design Systems, Inc.

`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (lidl/gds).
`beff (A/V`^{2}`)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`gmmos (A/V)`	Transconductance of channel region.
`sqrtsfw (V/Hz^1/2)`	Input-referred RMS white noise voltage density.
`sqrtsff (V/Hz^1/2)`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual temperature.
`pwr (W)`	Power.

Related Topics

Philips Models

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)

© 2023 Cadence Design Systems, Inc.

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002t)

This is SimKit 3.7.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`w=2e-05 m`	Drawn width of the channel region.
`wd=2e-05 m`	Drawn width of the drift region.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	
`trise=0`	Temperature rise from ambient.

Model Syntax

```
model modelName mos2002t parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=2e+03`	Must be 2002.
`paramchk=0`	Level of clip warning info.
`wvar=0 m`	Width offset of the channel region.
`wdvar=0 m`	Width offset of the drift region.
`tref=25 deg. C`	Reference temperature.
`vfb=-1 V`	Flatband voltage of the channel region, at reference temperature.
`stvfb=0 V/K`	Temperature scaling coefficient for VFB.
`vfbd=-0.1 V`	Flatband voltage of the drift region, at reference temperature.
`stvfbd=0 V/K`	Temperature scaling coefficient for the flatband voltage of the drift region.
`kor=1.6 V^1/2`	Body factor of the channel region of an infinitely wide transistor.
`swko=0`	Width scaling coefficient for KO.
`kodr=1 V^1/2`	Body factor of the drift region of an infinitely wide transistor.
`swkod=0`	Width scaling coefficient for the body factor of the drift region.
`phib=0.86 V`	Surface potential at the onset of strong inversion in the channel region, at reference temperature.
`stphib=-0.0012 V/K`	Temperature scaling coefficient for PHIB.
`phibd=0.78 V`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`stphibd=-0.0012 V/K`	Temperature scaling coefficient for PHIBD.
`betw=7e-05 A/V`^{2}	Gain factor of a channel region of 1 um wide, at reference temperature.
`etabet=1.6`	Temperature scaling exponent for BET.

© 2023 Cadence Design Systems, Inc.

betaccw=7e-05 A/V^{-2}	
	Gain factor of drift region of 1 um wide, at reference temperature.
etabetacc=1.5	Temperature scaling exponent for BETACC.
rdw=4e+03 Ω	On-resistance of a drift region of 1 um wide, at reference temperature.
etard=1.5	Temperature scaling exponent for RD.
lamd=0.2	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
the1r=0.09 V^-1	Mobility reduction coefficient of infinitely wide transistor, due to vertical strong-inversion field in a channel region.
swthe1=0	Width scaling coefficient for THE1.
the1acc=0.02 V^-1	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
the2r=0.03 V^(-1/2)	
	Mobility reduction coefficient for VSB > 0 of an infinitely wide transistor, due to vertical depletion field in channel region.
swthe2=0	Width scaling coefficient for THE2.
the3r=0.4 V^-1	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation.
etathe3=1	Temperature scaling exponent for THE3.
swthe3=0	Width scaling coefficient for THE3.
mexp=2	Smoothing factor for transition from linear to saturation regime.
the3dr=0 V^-1	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation.
etathe3d=1	Temperature scaling exponent for THE3D.
swthe3d=0	Width scaling coefficient for THE3D.
mexpd=2	Smoothing factor for transition from linear to quasi-saturation regime.
alp=0.002	Factor for channel length modulation.

© 2023 Cadence Design Systems, Inc.

`vp=0.05 V`	Characteristic voltage of channel length modulation.
`sdibl=0.001 V^(-1/2)`	Factor for drain-induced barrier lowering.
`msdibl=3`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo=0 V`	Parameter for the (short-channel) sub-threshold slope.
`ssf=1e-12 V^(-1/2)`	Factor for static feedback.
`a1chr=15`	Factor of channel weak avalanche current of an infinitely wide transistor, at reference temperature.
`sta1ch=0 K^-1`	Temperature scaling coefficient for A1CH.
`swa1ch=0`	Width scaling coefficient for A1CH.
`a2ch=73 V`	Exponent of channel weak avalanche current.
`a3ch=0.8`	Factor of the drain-source voltage above which channel weak avalanche occurs.
`a1drr=15`	Factor of drift weak avalanche current of an infinitely wide transistor, at reference temperature.
`sta1dr=0 K^-1`	Temperature scaling coefficient for A1DR.
`swa1dr=0`	Width scaling coefficient for A1DR.
`a2dr=73 V`	Exponent of drift weak avalanche current.
`a3dr=0.8`	Factor of the drain-source voltage above which drift weak avalanche occurs.
`coxw=7.5e-16 F`	Oxide capacitance for an intrinsic channel region of 1um wide.
`coxdw=7.5e-16 F`	Oxide capacitance for an intrinsic drift region of 1um wide.
`cgdow=0 F`	Gate-to-drain overlap capacitance for a drift region of 1 um wide.
`cgsow=0 F`	Gate-to-source overlap capacitance for a channel region of 1 um wide.
`nt=1.65e-20 J`	Coefficient of thermal noise, at reference temperature.

© 2023 Cadence Design Systems, Inc.

nfaw=1.4e+25 V^-1 m^-4	First coefficient of flicker noise for a channel region of 1 um wide.
nfbw=2e+08 V^-1 m^{-2}	Second coefficient of flicker noise for a channel region of 1 um wide.
nfcw=0 V^-1	Third coefficient of flicker noise for a channel region of 1 um wide.
tox=3.8e-08 m	Thickness of the oxide above the channel region.
dta=0 K	Temperature offset to the ambient temperature.
rth=300 K/W	Thermal resistance.
cth=3e-09 J/K	Thermal capacitance.
ath=0	Temperature coefficient of the thermal resistance.
type=n	Transistor gender. Possible values are n and p.
imax=1000 A	Explosion current.
vbox=0.0 V	Oxide breakdown voltage.
vbds=0.0 V	Drain-source breakdown voltage.
tnom (deg. C)	Alias of tnom.
tr (deg. C)	Alias of tnom.

Output Parameters

vfb (V)	Flatband voltage of the channel region, at reference temperature.
vfbd (V)	Flatband voltage of the drift region.
ko (V^1/2)	Body factor of the channel region.
kod (V^1/2)	Body factor of the drift region.
phib (V)	Surface potential at the onset of strong inversion in the channel region, at reference temperature.

© 2023 Cadence Design Systems, Inc.

`phibd (V)`	Surface potential at the onset of strong inversion in the drift region, at reference temperature.
`bet (A/V`^{2}`)`	Gain factor of the channel region, at reference temperature.
`betacc (A/V`^{2}`)`	Gain factor for accumulation in the drift region, at reference temperature.
`rd (Ω)`	On-resistance of the drift region, at reference temperature.
`lamd`	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V.
`the1 (V^-1)`	Mobility reduction coefficient in the channel region due to vertical electrical field caused by strong inversion.
`the1acc (V^-1)`	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation.
`the2 (V^-1/2)`	Mobility reduction coefficient for VSB > 0 in the channel region due to the vertical electrical field caused by depletion.
`the3 (V^-1)`	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation.
`mexp`	Smoothing factor for transition from linear to saturation regime.
`the3d (V^-1)`	Mobility reduction coefficient in the drift region due to the horizontal electrical field caused by velocity saturation.
`mexpd`	Smoothing factor for transition from linear to quasi-saturation regime.
`alp`	Factor for channel length modulation.
`vp (V)`	Characteristic voltage of channel length modulation.
`sdibl (V^-1/2)`	Factor for drain-induced barrier lowering.
`msdibl`	Exponent for the drain-induced barrier lowering dependence on the backgate bias.
`mo (V)`	Parameter for the (short-channel) sub-threshold slope.
`ssf (V^-1/2)`	Factor for static feedback.

© 2023 Cadence Design Systems, Inc.

a1ch	Factor of channel weak avalanche current, at reference temperature.
a2ch (V)	Exponent of channel weak avalanche current.
a3ch	Factor of the drain-source voltage above which channel weak avalanche occurs.
a1dr	Factor of drift weak avalanche current, at reference temperature.
a2dr (V)	Exponent of drift weak avalanche current.
a3dr	Factor of the drain-source voltage above which drift weak avalanche occurs.
cox (F)	Oxide capacitance for the intrinsic channel region.
coxd (F)	Oxide capacitance for the intrinsic drift region.
cgdo (F)	Gate-to-drain overlap capacitance.
cgso (F)	Gate-to-source overlap capacitance.
nt (J)	Coefficient of thermal noise.
nfa (V^-1 m^-4)	First coefficient of flicker noise.
nfb (V^-1 m^{-2})	Second coefficient of flicker noise.
nfc (V^-1)	Third coefficient of flicker noise.
tox (m)	Thickness of the oxide above the channel region.
rth (K/W)	Thermal resistance.
cth (J/K)	Thermal capacitance.

Operating-Point Parameters

ids (A)	Drain current, excluding avalanche and tunnel currents.
iavl (A)	Substrate current due to weak-avalanche.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vsb (V)	Source-bulk voltage.

© 2023 Cadence Design Systems, Inc.

`vto (V)`	Zero-bias threshold voltage.
`vts (V)`	Threshold voltage including back-bias effects.
`vth (V)`	Threshold voltage including back-bias and drain-bias effects.
`vgt (V)`	Effective gate drive voltage including back-bias and drain voltage effects.
`vtod (V)`	Threshold voltage of the drift region.
`vdiseff (V)`	Effective internal drain-to-source voltage at actual bias.
`vdissat (V)`	Saturation voltage of channel region at actual bias.
`vddisat (V)`	Saturation voltage of drift region at actual bias.
`gm (A/V)`	Transconductance (d ids / d vgs).
`gmb (A/V)`	Substrate-transconductance (d ids / d vbs).
`gds (A/V)`	Output conductance (d ids / d vds).
`cdd (F)`	Capacitance (d qd / d vd).
`cdg (F)`	Capacitance (- d qd / d vg).
`cds (F)`	Capacitance (- d qd / d vs).
`cdb (F)`	Capacitance (- d qd / d vb).
`cgd (F)`	Capacitance (- d qg / d vd).
`cgg (F)`	Capacitance (d qg / d vg).
`cgs (F)`	Capacitance (- d qg / d vs).
`cgb (F)`	Capacitance (- d qg / d vb).
`csd (F)`	Capacitance (- d qs / d vd).
`csg (F)`	Capacitance (- d qs / d vg).
`css (F)`	Capacitance (d qs / d vs).
`csb (F)`	Capacitance (- d qs / d vb).
`cbd (F)`	Capacitance (- d qb / d vd).
`cbg (F)`	Capacitance (- d qb / d vg).
`cbs (F)`	Capacitance (- d qb / d vs).
`cbb (F)`	Capacitance (d qb / d vb).

© 2023 Cadence Design Systems, Inc.

`weff (m)`	Effective channel width for geometrical models.
`wdeff (m)`	Effective drift region width for geometrical model.
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small-signal output resistance (1/gds).
`vearly (V)`	Equivalent Early voltage (|id|/gds).
`beff (A/V^2)`	Gain factor.
`fug (Hz)`	Unity gain frequency at actual bias (gm/(2*pi*cin)).
`gmmos (A/V)`	Transconductance of channel region.
`sqrtsfw (V/Hz^1/2)`	Input-referred RMS white noise voltage density.
`sqrtsff (V/Hz^1/2)`	Input-referred RMS white noise voltage density at 1 kHz.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual temperature.
`pwr (W)`	Power.

Related Topics

Philips Models

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001e)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001t)

Lateral Double-diffused MOS Model (MOS Model Level 2001) (mos2001et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002e)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002et)

Lateral Double-diffused MOS Model (MOS Model Level 2002) (mos2002)

© 2023 Cadence Design Systems, Inc.

MOS Model 31, Level 3100 (mos3100)

This is SimKit 5.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos3100 parameter=value ...
```

Model Parameters

`level=3.1e+03`	Transistor level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.

© 2023 Cadence Design Systems, Inc.

`tmin=0 s`	Ovcheck tmin value.
`ron=1 Ω`	Ohmic resistance at zero bias.
`rsat=1 Ω`	Space charge resistance at zero bias.
`vsat=10 V`	Critical drain-source voltage for hot carriers.
`psat=1`	Velocity saturation coefficient.
`vp=-1 V`	Pinch off voltage at zero gate and substrate voltages.
`tox=-1 m`	Gate oxide thickness.
`dch=1e+21` m^{-3}	Doping level channel.
`dsub=1e+21` m^{-3}	Doping level substrate.
`vsub=0.6 V`	Substrate diffusion voltage.
`vgap=1.2 V`	Bandgap voltage channel.
`cgate=0 F`	Gate capacitance at zero bias.
`csub=0 F`	Substrate capacitance at zero bias.
`tausc=0 s`	Space charge transit time of the channel.
`ach=0`	Temperature coefficient resistivity of the channel.
`achmod=0`	Parameter to switch to extended temperature scaling.
`achron=0`	Temperature coefficient of ohmic resistance at zero bias.
`achvsat=0`	Temperature coefficient of critical drain-source voltage for hot carriers.
`achrsat=0`	Temperature coefficient of space charge resistance at zero bias.
`tref=25 deg. C`	Reference temperature.
`dta=0 deg. C`	Temperature offset of the device.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.

© 2023 Cadence Design Systems, Inc.

`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

tempeff (C)	Effective temperature for a single device.
meff	Effective multiplicity factor (m-factor).
int_s	
int_d	

Operating-Point Parameters

ids (A)	Drain source current (including velocity saturation).
vds (V)	Drain source voltage.
vgs (V)	Gate source voltage.
vbs (V)	Bulk source voltage.
vp (V)	Channel pinch off voltage.
gm (A/V)	Transconductance (dIds/dVg).
gmb (A/V)	Bulk transconductance (dIds/dVb).
gds (A/V)	Output conductance (dIds/dVd).
qg (C)	Gate charge.
cgd (F)	Gate charge dependence on drain voltage (- dQg/dVd).
cgg (F)	Gate charge dependence on gate voltage (dQg/dVg).
cgs (F)	Gate charge dependence on source voltage (-dQg/dVs).
cgb (F)	Gate charge dependence on bulk voltage (-dQg/dVb).
qb (C)	Bulk charge.
cbd (F)	Bulk charge dependence on drain voltage (-dQb/dVd).
cbg (F)	Bulk charge dependence on gate voltage (-dQb/dVg).
cbs (F)	Bulk charge dependence on source voltage (-dQb/dVs).
cbb (F)	Bulk charge dependence on bulk voltage (dQb/dVb).
qd (C)	Drain charge.

© 2023 Cadence Design Systems, Inc.

`cdd (F)`	Drain charge dependence on drain voltage (dQd/dVd).
`cdg (F)`	Drain charge dependence on gate voltage (-dQd/dVg).
`cds (F)`	Drain charge dependence on source voltage (-dQd/dVs).
`cdb (F)`	Drain charge dependence on bulk voltage (-dQd/dVb).
`qs (C)`	Source charge.
`csd (F)`	Source charge dependence on drain voltage (-dQs/dVd).
`csg (F)`	Source charge dependence on gate voltage (-dQs/dVg).
`css (F)`	Source charge dependence on source voltage (dQs/dVs).
`csb (F)`	Source charge dependence on bulk voltage (-dQs/dVb).
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small signal output resistance (1/gds).
`vearly (V)`	Equivalent early voltage (|Ids|/gds).
`iohm (A)`	Drain source current excluding velocity saturation.
`ihc (A)`	Critical current for velocity saturation.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`mos_region=SUBTHRESHOLD`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.

Related Topics

Philips Models

MOS Model 31, Level 3100 (mos3100t)

MOS Model 31, Level 3100 (mos3100t)

This is SimKit 5.2.

© 2023 Cadence Design Systems, Inc.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b  dt ModelName parameter=value ...
```

Instance Parameters

`mult=1`	Number of devices in parallel.
`printscaled=0`	Print scaled parameter info if value not equal to zero.
`trise=0 K`	Difference between the local ambient and global ambient temperature.
`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, and `subth`.
`m=1`	Alias of mult.
`mos_region=SUBTHRESHOLD`	
`diode_region=ON`	

Model Syntax

```
model modelName mos3100t parameter=value ...
```

Model Parameters

`level=3.1e+03`	Transistor level.
`paramchk=0`	Level of clip warning info.
`vbox=0 V`	Oxide breakdown voltage.
`vbds=0 V`	Drain-source breakdown voltage.
`tmin=0 s`	Ovcheck tmin value.
`ron=1 Ω`	Ohmic resistance at zero bias.
`rsat=1 Ω`	Space charge resistance at zero bias.

© 2023 Cadence Design Systems, Inc.

`vsat=10 V`	Critical drain-source voltage for hot carriers.
`psat=1`	Velocity saturation coefficient.
`vp=-1 V`	Pinch off voltage at zero gate and substrate voltages.
`tox=-1 m`	Gate oxide thickness.
`dch=1e+21` m^{-3}	Doping level channel.
`dsub=1e+21` m^{-3}	Doping level substrate.
`vsub=0.6 V`	Substrate diffusion voltage.
`vgap=1.2 V`	Bandgap voltage channel.
`cgate=0 F`	Gate capacitance at zero bias.
`csub=0 F`	Substrate capacitance at zero bias.
`tausc=0 s`	Space charge transit time of the channel.
`ach=0`	Temperature coefficient resistivity of the channel.
`achmod=0`	Parameter to switch to extended temperature scaling.
`achron=0`	Temperature coefficient of ohmic resistance at zero bias.
`achvsat=0`	Temperature coefficient of critical drain-source voltage for hot carriers.
`achrsat=0`	Temperature coefficient of space charge resistance at zero bias.
`tref=25 deg. C`	Reference temperature.
`dta=0 deg. C`	Temperature offset of the device.
`rth=300 K/W`	Thermal resistance.
`cth=3e-09 J/K`	Thermal capacitance.
`ath=0`	Temperature coefficient of the thermal resistance.
`type=n`	Transistor gender. Possible values are `n` and `p`.
`imax=1000 A`	Explosion current.
`tnom (deg. C)`	Alias of tnom.
`tr (deg. C)`	Alias of tnom.

© 2023 Cadence Design Systems, Inc.

`compatible=spectre`	Make device equations to be compatible with a foreign simulator. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, and `pspice`.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`int_s`	
`int_d`	

Operating-Point Parameters

`ids (A)`	Drain source current (including velocity saturation).
`vds (V)`	Drain source voltage.
`vgs (V)`	Gate source voltage.
`vbs (V)`	Bulk source voltage.
`vp (V)`	Channel pinch off voltage.
`gm (A/V)`	Transconductance (dIds/dVg).
`gmb (A/V)`	Bulk transconductance (dIds/dVb).
`gds (A/V)`	Output conductance (dIds/dVd).
`qg (C)`	Gate charge.
`cgd (F)`	Gate charge dependence on drain voltage (- dQg/dVd).
`cgg (F)`	Gate charge dependence on gate voltage (dQg/dVg).
`cgs (F)`	Gate charge dependence on source voltage (-dQg/dVs).
`cgb (F)`	Gate charge dependence on bulk voltage (-dQg/dVb).
`qb (C)`	Bulk charge.

© 2023 Cadence Design Systems, Inc.

`cbd (F)`	Bulk charge dependence on drain voltage (-dQb/dVd).
`cbg (F)`	Bulk charge dependence on gate voltage (-dQb/dVg).
`cbs (F)`	Bulk charge dependence on source voltage (-dQb/dVs).
`cbb (F)`	Bulk charge dependence on bulk voltage (dQb/dVb).
`qd (C)`	Drain charge.
`cdd (F)`	Drain charge dependence on drain voltage (dQd/dVd).
`cdg (F)`	Drain charge dependence on gate voltage (-dQd/dVg).
`cds (F)`	Drain charge dependence on source voltage (-dQd/dVs).
`cdb (F)`	Drain charge dependence on bulk voltage (-dQd/dVb).
`qs (C)`	Source charge.
`csd (F)`	Source charge dependence on drain voltage (-dQs/dVd).
`csg (F)`	Source charge dependence on gate voltage (-dQs/dVg).
`css (F)`	Source charge dependence on source voltage (dQs/dVs).
`csb (F)`	Source charge dependence on bulk voltage (-dQs/dVb).
`u`	Transistor gain (gm/gds).
`rout (Ω)`	Small signal output resistance (1/gds).
`vearly (V)`	Equivalent early voltage (|Ids|/gds).
`iohm (A)`	Drain source current excluding velocity saturation.
`ihc (A)`	Critical current for velocity saturation.
`Pdiss (W)`	Dissipation.
`TK (K)`	Actual temperature.
`ctype`	Channel type (-1 for PMOS, +1 for NMOS).
`pwr (W)`	Power.
`mos_region`	MOS region. Possible values are `off`, `sat`, `triode`, and `subth`.

© 2023 Cadence Design Systems, Inc.

Related Topics

Philips Models

MOS Model 31, Level 3100 (mos3100)

© 2023 Cadence Design Systems, Inc.

13

Common MOSFET Equations

Spectre® circuit simulator has the following public-domain MOSFET models: Level-1, Level-2, Level-3, EKV, BSIM1 (Level-4), BSIM2 (Level-5), BSIM3v2, and 7BSIM3v3.

When the Spectre option `approx` is set to `yes`, `pow()` in the junction depletion capacitance calculation and `sqrt()` in the BJT and MOSFET level 1-5 models are replaced by a spline-function approximation. For more information, see `spectre -h options`.

Click to view the following sub-topics:

- Parameters Common to BSIM1 and BSIM2 Models
- Parameters Common to Levels 1-3 Only
- Source/Drain Bulk Junction Models
- Temperature Effect on Model Parameters
- Noise Model

© 2023 Cadence Design Systems, Inc.

Parameters Common to BSIM1 and BSIM2 Models

Electrical parameters that you specify override electrical parameters calculated with process parameters. The Spectre circuit simulator selects the default parameter value if you do not specify an electrical or a process parameter.

Channel Width and Length

(13-1)

$$W_{scaled} = w \times scale + xw \times scalem$$

(13-2)

$$W_{eff} = \begin{cases} w \times scale + xw \times scalem - 2wd \times scalem & \text{Level 1-3} \\ w \times scale + xw \times scalem - dw \times scalem & \text{BSIM 1-2} \end{cases}$$

(13-3)

$$L_{eff} = \begin{cases} l \times scale + xl \times scalem - 2ld \times scalem & \text{Level 1-3} \\ l \times scale + xl \times scalem - ld \times scalem & \text{BSIM 1-2} \end{cases}$$

Parameters Common to Levels 1-3 Only

This topic discusses parameters that are common to levels 1-3 only.

- If you do not give vto and $nsub$ is specified, vto is calculated from

(13-4)

$$vto = V_{FB} + phi + gamma\sqrt{phi}$$

where

(13-5)

$$V_{FB} = \phi_{MS} - \frac{q(nss)}{C_{ox}}$$

© 2023 Cadence Design Systems, Inc.

is the flat-band voltage and ϕ_{MS} is the work function difference between the gate material and the silicon substrate. With the following equations, the tpg (tps) parameter determines the value of ϕ_{MS}.

(13-6)

$$\phi_{MS} = \begin{cases} -0.5(E_g + phi) & \text{if } tpg = 1 \\ 0.5(E_g - phi) & \text{if } tpg = -1 \\ -0.05 - 0.5(E_g + phi) & \text{if } tpg = 0 \end{cases}$$

E_g is the energy gap whose equation is given later.

- If vto is specified, V_{FB} is calculated from

(13-7)

$$V_{FB} = vto - phi - gamma\sqrt{phi}$$

- If you do not give phi and $nsub$ is specified, phi is calculated from

(13-8)

$$phi = 2V_t \ln\left[\frac{nsub}{n_i}\right]$$

where n_i is the intrinsic carrier concentration of silicon and V_t is the thermal voltage given by kT/q.

- If you do not give $gamma$ and $nsub$ is specified, $gamma$ is calculated from

(13-9)

$$gamma = \frac{\sqrt{2q\varepsilon_{si}nsub}}{C_{ox}}$$

- The consistency between kp, uo, and C_{ox}($kp = uoC_{ox}$) is checked according to the following rules:
  - If tox is not given, C_{ox} is calculated from the default value of tox.
  - If kp is given, uo is calculated from $uo = kp/C_{ox}$, whether uo is given or not. If this uo value is different from that specified in the model, a warning message tells you that the specified kp and uo values are inconsistent.

© 2023 Cadence Design Systems, Inc.

- If you do not give kp and uo is specified, kp is calculated from $kp = uo * C_{ox}$.
- If neither kp nor uo is given, their default values are used.

In SPICE, if you give kp but not uo, uo is not calculated from kp. The default value of uo (600) is used. If you specify both kp and uo, SPICE does not check the consistency between them. In the Spectre circuit simulator, kp and uo are always consistent. This can cause the simulation results of the Spectre and SPICE simulators to be different. SPICE uses kp to evaluate the drain current (through the b term) while it uses uo to evaluate the drain saturation voltage V_{DSAT} (if $vmax$ is also specified).

Often only kp is specified in the model. SPICE then assigns a default value (600) to uo, but Spectre calculates uo from kp. This usually causes drain currents to be smaller in the Spectre simulator than in SPICE. If you need SPICE compatibility, you can set `compatible` to any option other than `spectre` (for example, `spice2`, `spice3`, `cdsspice`, or `spiceplus`) in the `.options` card, and the Spectre simulator does not force uo to be consistent with kp. In SPICE, V_{DSAT} is a function of (uo/$vmax$) rather than uo alone. Therefore, you can still make uo consistent with kp by proportionally adjusting the $vmax$ value without changing the results. However, you should check the parameter extraction program to find out how uo and $vmax$ are extracted before comparing SPICE and Spectre results or changing any of the model parameters.

- If tox is not indicated in the Level-1 model, the intrinsic MOSFET gate capacitances are not calculated.

Related Topics

Common MOSFET Equations

Source/Drain Bulk Junction Models

Temperature Effect on Model Parameters

Noise Model

Source/Drain Bulk Junction Models

Junction Leakage Current

(13-10)

© 2023 Cadence Design Systems, Inc.

$$I_{BS(BD)} = \begin{cases} is\left(e^{\frac{V_{BS(BD)}}{V_t}} - 1\right) & \text{if } V_{BS(BD)} \le V_{Expl} \\ I_{offset} + G_{Expl} V_{BS(BD)} & \text{otherwise} \end{cases}$$

where

© 2023 Cadence Design Systems, Inc.

(13-11)

$$V_{Expl} = V_t \ln\left[1 + \frac{imax}{is}\right]$$

is the forward explosion voltage,

(13-12)

$$G_{Expl} = V_t(imax + is)$$

is the conductance at V_{Expl}, and

(13-13)

$$I_{offset} = imax - V_{Expl}G_{Expl}$$

is the linear extrapolated current at $V_{BS(BD)}$ = 0 from V_{Expl}.

Bulk-Junction Bottom (Sidewall) Capacitance

(13-14)

$$C_{BS(BD)} = \begin{cases} \dfrac{cbs(cbd)}{\left(1 - \dfrac{V_{BS(BD)}}{pb}\right)^{mj}} & \text{if } V_{BS(BD)} \le fc \times pb \\ \dfrac{cbs(cbd)}{(1-fc)^{mj}}\left[1 + \dfrac{mj(V_{BS(BD)} - pb*fc)}{pb(1-fc)}\right] & \text{otherwise} \end{cases}$$

These equations also apply to the sidewall capacitances with pb and fc replaced by $fcsw$ and $pbsw$. If $fcsw$ is not given, fc is used. If $pbsw$ is not given, pb is used.

Drain and Source Area

The drain and source areas are calculated in the order shown in the following equations:

© 2023 Cadence Design Systems, Inc.

(13-15)

$$\text{Drain area} = \begin{cases} ad & \text{if } ad \text{ is given} \\ 2hdif * scalem * W_{scaled} & \text{if } hdif \text{ is given} \\ W_{eff} * ld & \text{if } ld \text{ is given} \\ W_{eff} * ldd & \text{if } ldd \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

(13-16)

$$\text{Source area} = \begin{cases} as & \text{if } as \text{ is given} \\ 2hdif * scalem * W_{scaled} & \text{if } hdif \text{ is given} \\ W_{eff} * ls & \text{if } ls \text{ is given} \\ W_{eff} * lds & \text{if } lds \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

Note: The ld (length of drain) parameter is an instance parameter that is different from the model parameter ld (lateral diffusion) used in calculating L_{eff}.

Drain and Source Perimeters

The drain and source perimeters are calculated in the order shown in the following equations:

(13-17)

$$\text{Drain perimeter} = \begin{cases} pd & \text{if } pd \text{ is given} \\ 4hdif * scalem + 2W_{scaled} & \text{if } hdif \text{ is given} \\ W_{eff} + 2ld & \text{if } ld \text{ is given} \\ W_{eff} + 2ldd & \text{if } ldd \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

(13-18)

$$\text{Source perimeter} = \begin{cases} ps & \text{if } ps \text{ is given} \\ 4hdif * scalem + 2W_{scaled} & \text{if } hdif \text{ is given} \\ W_{eff} + 2ls & \text{if } ls \text{ is given} \\ W_{eff} + 2lds & \text{if } lds \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

Note: The ld (length of drain) parameter is an instance parameter that is different from the model parameter ld (lateral diffusion) used in calculating L_{eff}.

Drain and Source Squares

The number of drain and source squares is calculated in the order shown in the following equations:

(13-19)

$$\text{Number of drain squares} = \begin{cases} nrd & \text{if } nrd \text{ is given} \\ hdif / W_{scaled} & \text{if } hdif \text{ is given} \\ lgcd / W_{eff} & \text{if } lgcd \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

(13-20)

$$\text{Number of source squares} = \begin{cases} nrs & \text{if } nrs \text{ is given} \\ hdif / W_{scaled} & \text{if } hdif \text{ is given} \\ lgcs / W_{eff} & \text{if } lgcs \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Junction Saturation Current

is always overrides js. If you give js but not is, the saturation currents are calculated from js and the source and drain areas.

(13-21)

$$\text{Drain saturation current} = \begin{cases} is & \text{if } is \text{ is given} \\ js * ad & \text{otherwise} \end{cases}$$

(13-22)

$$\text{Source saturation current} = \begin{cases} is & \text{if } is \text{ is given} \\ js * as & \text{otherwise} \end{cases}$$

Junction Capacitance

cbs (cbd) always overrides cj. If you do not give cbs (cbd) and cj is specified, cbs (cbd) is calculated from cj and the source (drain) area.

(13-23)

$$\text{Drain capacitance} = \begin{cases} cbd & \text{if } cbd \text{ is specified} \\ cj * ad & \text{otherwise} \end{cases}$$

(13-24)

$$\text{Source capacitance} = \begin{cases} cbs & \text{if } cbs \text{ is specified} \\ cj * as & \text{otherwise} \end{cases}$$

Drain and Source Parasitic Resistance

For MSOFET models except EKV,

© 2023 Cadence Design Systems, Inc.

(13-25)

$$\text{Drain Resistance } (R_{Deff}) = \begin{cases} nrd*rsh + \frac{rdc}{N_{SC}} + \frac{rd(ld+ldif)scalem}{W_{scaled}} & \text{if } ldif \text{ is given} \\ nrd*rsh + \frac{rdc}{N_{SC}} + rd + \frac{rdd}{W_{eff}} & \text{otherwise} \end{cases}$$

(13-26)

$$\text{Source Resistance } (R_{Seff}) = \begin{cases} nrs*rsh + \frac{rsc}{N_{SC}} + \frac{rs(ld+ldif)scalem}{W_{scaled}} & \text{if } ldif \text{ is given} \\ nrs*rsh + \frac{rsc}{N_{SC}} + rs + \frac{rss}{W_{eff}} & \text{otherwise} \end{cases}$$

z

(13-27)

$$N_{SC} = \begin{cases} 1 & \text{if } sc \text{ is infinity or negative (default)} \\ W_{eff} & \text{if } sc = 0 \\ MAX\left[INT\left(\frac{W_{eff}}{sc}\right), 1\right] & \text{otherwise} \end{cases}$$

For EKV,

(13-28)

$$\text{Drain Resistance (rdeff)} = \begin{cases} nrd*rsh + \frac{rdc}{W_{eff}} + \frac{rd(ld+ldif)scalem}{W_{scaled}} & \text{if } ldif \text{ is given} \\ nrd*rsh + \frac{rdc}{W_{eff}} + rd + \frac{rdd}{Width} & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

(13-29)

$$\text{Source Resistance (rseff)} = \begin{cases} nrs*rsh + \dfrac{rsc}{W_{eff}} + \dfrac{rs(ld+ldif)scalem}{W_{scaled}} & \text{if } ldif \text{ is given} \\ nrs*rsh + \dfrac{rsc}{W_{eff}} + rs + \dfrac{rdd}{Width} & \text{otherwise} \end{cases}$$

The diffusion resistance depends on the value you specify for the `maxrsd` parameter.

- If the parasitic resistance is more than the maxrsd value, the diffusion resistance is calculated as described above.
- If the parasitic resistance is less than the maxrsd value, the resistor is removed and the correction is added to the current as compensation. The correction is calculated as follows:

(13-30)

$$I'_{ds} = \frac{I_{ds}}{(1 + r_{ddiff} \cdot g_{ds} + r_{sdiff} \cdot (g_{ds} + g_m + g_{mbs}))}$$

where

(13-31)

$$g_{ds} = \frac{dI_{ds}}{dV_{ds}}$$

(13-32)

$$g_m = \frac{dI_{ds}}{dV_{gs}}$$

(13-33)

$$g_{mbs} = \frac{dI_{ds}}{dV_{bs}}$$

© 2023 Cadence Design Systems, Inc.

For more information on the `maxrsd` parameter, refer to `spectre -h bsim4`.

Overlap Capacitance

(13-34)

$$C_{gd} = \begin{cases} \text{cgdo/scalem} * W_{eff} & \text{if } cgdo \text{ is given} \\ W_{scaled}(ld + meto)\text{scalem} * C_{ox} & \text{if } meto \text{ is given} \end{cases}$$

(13-35)

$$C_{gs} = \begin{cases} \text{cgso/scalem} * W_{eff} & \text{if } cgso \text{ is given} \\ W_{scaled}(ld + meto)\text{scalem} * C_{ox} & \text{if } meto \text{ is given} \end{cases}$$

(13-36)

$$C_{gb} = \begin{cases} cgbo/scalem * L_{eff} & \text{if } cgbo \text{ is given} \\ 2L_{eff}(ld + meto)\text{scalem} * C_{ox} & \text{if } meto \text{ is given} \end{cases}$$

where

(13-37)

$$C_{ox} = \frac{\varepsilon_{ox}}{tox * scalem}$$

Related Topics

Common MOSFET Equations

Source/Drain Bulk Junction Models

Temperature Effect on Model Parameters

Noise Model

© 2023 Cadence Design Systems, Inc.

Temperature Effect on Model Parameters

You can set both the model and the instance temperatures with the $trise$ parameter. If the instance $trise$ is specified, it overrides the model $trise$. The device temperature T is calculated by

(13-38)

$$T = trise + T_{ambient}$$

where $T_{ambient}$ is the global temperature set by the simulator.

© 2023 Cadence Design Systems, Inc.

Mobility and Transconductance Parameters

(13-39)

$$uo = uo_{nom}\left(\frac{T}{Tnom}\right)^{ute}$$

(13-40)

$$kp = kp_{nom}\left(\frac{T}{Tnom}\right)^{ute}$$

where ute is the exponent parameter. Default value of ute is `-1.5`.

Energy Band Gap

(13-41)

$$E_g(T) = \begin{cases} eg - \dfrac{gap1 * T^2}{T + gap2} & \text{if } tlev = 2 \\ \left(1.17 - \dfrac{4.73 \times 10^{-4} T^2}{T + 636}\right) & \text{if } tlev = 0 \text{ or } 1 \text{ and } compatible{=}spectre \\ \left(1.16 - \dfrac{7.02 \times 10^{-4} T^2}{T + 1108}\right) & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Surface Potential

(13-42)

$$phi(T) = \begin{cases} phi_{nom}\left(\frac{T}{Tnom}\right) - \Delta\phi & \text{if } tlevc = 0 \\ phi_{nom} - ptc\Delta T & \text{if } tlevc = 1 \text{ or } 2 \\ phi_{nom} - \frac{d\phi}{dT}\Delta T & \text{if } tlevc = 3 \end{cases}$$

where

(13-43)

$$\Delta\phi = V_t(T)\left\{3 \ln\left[\frac{T}{Tnom}\right] + \frac{E_{g,nom}}{V_{t,nom}} - \frac{E_g(T)}{V_t(T)}\right\}$$

(13-44)

$$E_{g,nom} = E_g(Tnom)$$

(13-45)

$$V_{t,nom} = \frac{k(Tnom)}{q}$$

(13-46)

$$\Delta T = T - Tnom$$

(13-47)

$$n_i = 1.45 \times 10^{10}\left(\frac{T}{300}\right)^{1.5} \exp\left[\frac{1.12}{0.0516} - \frac{E_g(T)}{2V_t(T)}\right]$$

© 2023 Cadence Design Systems, Inc.

(13-48)

$$\frac{d\phi}{dT} = \begin{cases} \dfrac{-\left[\Delta E_{phi} + (1.16 - E_{g,nom}) * \left(2 - \dfrac{Tnom}{Tnom + 1108}\right)\right]}{Tnom} & \text{if } tlev = 0, 1 \\ \dfrac{-\left[\Delta E_{phi} + (eg - E_{g,nom}) * \left(2 - \dfrac{Tnom}{Tnom + gap2}\right)\right]}{Tnom} & \text{if } tlev = 2 \end{cases}$$

where

(13-49) $$\Delta E_{phi} = E_{g,nom} + 3V_{t,nom} - phi_{nom}$$

Built-in Voltage of Source/Drain Junctions

If $tlevc = 0$,

(13-50)

$$pb(T) = pb_{nom}\left(\frac{T}{Tnom}\right) - \Delta\phi$$

(13-51)

$$pbsw(T) = pbsw_{nom}\left(\frac{T}{Tnom}\right) - \Delta\phi$$

If $tlevc = 1,2$,

(13-52)

$$pb(T) = pb_{nom} - pta\Delta T$$

(13-53)

$$pbsw(T) = pbsw_{nom} - ptp\Delta T$$

© 2023 Cadence Design Systems, Inc.

If $tlevc = 3$,

(13-54)

$$pb(T) = pb_{nom} + \left(\frac{d\phi_B}{dT}\right)\Delta T$$

(13-55)

$$pbsw(T) = pbsw_{nom} + \left(\frac{d\phi_{sw}}{dT}\right)\Delta T$$

where

(13-56)

$$\frac{d\phi_B}{dT} = \begin{cases} \dfrac{-\left[\Delta E_{PB} + (1.16 - E_{g,nom}) * \left(2 - \dfrac{Tnom}{Tnom + 1108}\right)\right]}{Tnom} & \text{if } tlev = 0, 1 \\ \dfrac{-\left[\Delta E_{PB} + (eg - E_{g,nom}) * \left(2 - \dfrac{Tnom}{Tnom + gap2}\right)\right]}{Tnom} & \text{if } tlev = 2 \end{cases}$$

(13-57)

$$\frac{d\phi_{BSW}}{dT} = \begin{cases} \dfrac{-\left[\Delta E_{PBSW} + (1.16 - E_{g,nom}) * \left(2 - \dfrac{Tnom}{Tnom + 1108}\right)\right]}{Tnom} & \text{if } tlev = 0, 1 \\ \dfrac{-\left[\Delta E_{PBSW} + (eg - E_{g,nom}) * \left(2 - \dfrac{Tnom}{Tnom + gap2}\right)\right]}{Tnom} & \text{if } tlev = 2 \end{cases}$$

where

(13-58)

$$\Delta E_{PB} = E_{g,nom} + 3V_{t,nom} - pb_{nom}$$

© 2023 Cadence Design Systems, Inc.

(13-59)

$$\Delta E_{PBSW} = E_{g,\,nom} + 3V_{t,\,nom} - pbsw_{nom}$$

Junction Leakage Currents

(13-60)

$$is(T) = is_{nom} e^{Fact/n}$$

(13-61)

$$js(T) = js_{nom} e^{Fact/n}$$

where

(13-62)

$$Fact = \frac{E_{g,\,nom}}{V_{t,\,nom}} - \frac{E_g(T)}{V_t} + xti \ln\left[\frac{T}{Tnom}\right]$$

Junction Capacitances

If $tlevc = 0$

(13-63)

$$cbd(T) = cbd_{nom}\left[1 + mj\left(0.0004\Delta T - \frac{pb(T)}{pb_{nom}} + 1\right)\right]$$

(13-64)

$$cbs(T) = cbs_{nom}\left[1 + mj\left(0.0004\Delta T - \frac{pb(T)}{pb_{nom}} + 1\right)\right]$$

© 2023 Cadence Design Systems, Inc.

(13-65)

$$cj(T) = cj_{nom}\left[1 + mj\left(0.0004\Delta T - \frac{pb(T)}{pb_{nom}} + 1\right)\right]$$

(13-66)

$$cjsw(T) = cjsw_{nom}\left[1 + mjsw\left(0.0004\Delta T - \frac{pbsw(T)}{pbsw_{nom}} + 1\right)\right]$$

If $tlevc = 1$

(13-67)

$$cbd(T) = cbd_{nom}(1 + cta\Delta T)$$

(13-68)

$$cbs(T) = cbs_{nom}(1 + cta\Delta T)$$

(13-69)

$$cj(T) = cj_{nom}(1 + cta\Delta T)$$

(13-70)

$$cjsw(T) = cjsw_{nom}(1 + ctp\Delta T)$$

If $tlevc = 2$,

(13-71)

$$cbd(T) = cbd_{nom}\left(\frac{pb_{nom}}{pb(T)}\right)^{mj}$$

(13-72)

$$cbs(T) = cbs_{nom}\left(\frac{pb_{nom}}{pb(T)}\right)^{mj}$$

© 2023 Cadence Design Systems, Inc.

(13-73)

$$cj(T) = cj_{nom}\left(\frac{pb_{nom}}{pb(T)}\right)^{mj}$$

(13-74)

$$cjsw(T) = cjsw_{nom}\left(\frac{pbsw_{nom}}{pbsw(T)}\right)^{mjsw}$$

If $tlevc = 3$,

(13-75)

$$cbd(T) = cbd_{nom}\left[1 - 0.5\left(\frac{d\phi_B}{dT}\right)\left(\frac{\Delta T}{pb_{nom}}\right)\right]$$

(13-76)

$$cbs(T) = cbs_{nom}\left[1 - 0.5\left(\frac{d\phi_B}{dT}\right)\left(\frac{\Delta T}{pb_{nom}}\right)\right]$$

(13-77)

$$cj(T) = cj_{nom}\left[1 - 0.5\left(\frac{d\phi_B}{dT}\right)\left(\frac{\Delta T}{pb_{nom}}\right)\right]$$

(13-78)

$$cjsw(T) = cjsw_{nom}\left[1 - 0.5\left(\frac{d\phi_{SW}}{dT}\right)\left(\frac{\Delta T}{pbsw_{nom}}\right)\right]$$

© 2023 Cadence Design Systems, Inc.

Channel Length Modulation

(13-79)

$$lambda(T) = lambda_{nom}(1 + lamex\Delta T)$$

(13-80)

$$kappa(T) = kappa_{nom}(1 + lamex\Delta T)$$

Threshold Voltage

If $tlev$ = 0,

(13-81)

$$V_{bi}(T) = vto_{nom} - gamma\sqrt{phi_{nom}} + \frac{phi(T) - phi_{nom}}{2} + \frac{E_{g,nom} - E_g(T)}{2}$$

(13-82)

$$vto(T) = V_{bi}(T) + gamma\sqrt{phi(T)}$$

If $tlev$ = 1,

(13-83)

$$vto(T) = vto_{nom} - tcv\Delta T$$

Note: tcv is negative.

(13-84)

$$V_{bi}(T) = vto(T) - gamma\sqrt{phi(T)}$$

© 2023 Cadence Design Systems, Inc.

If $tlev = 2$,

(13-85)

$$vto(T) = vto_{nom} + \left(1 + \frac{gamma}{2\sqrt{phi_{nom}}}\right)\frac{d\phi}{dT}\Delta T$$

(13-86)

$$V_{bi}(T) = vto(T) - gamma\sqrt{phi(T)}$$

Drain and Source Parasitic Resistance

(13-87)

$$rd(T) = rd_{nom}(1 + trd\Delta T)$$

(13-88)

$$rs(T) = rs_{nom}(1 + trs\Delta T)$$

Critical Field

(13-89)

$$ucrit(T) = ucrit_{nom}\left(\frac{T}{Tnom}\right)^{flex}$$

Related Topics

Common MOSFET Equations

Source/Drain Bulk Junction Models

Noise Model

© 2023 Cadence Design Systems, Inc.

Parameters Common to BSIM1 and BSIM2 Models

© 2023 Cadence Design Systems, Inc.

Noise Model

This topic contains model equations for the noise model.

Drain Resistance Thermal Noise

(13-90)

$$\overline{i_{Rd}^2} = \frac{4kT}{R_d}\Delta f$$

Source Resistance Thermal Noise

(13-91)

$$\overline{i_{Rs}^2} = \frac{4kT}{R_s}\Delta f$$

Channel Thermal and Flicker Noise

(13-92)

$$\overline{i_{DS}^2} = \overline{i_{n,\,thermal}^2} + \frac{kfI_{DS}^{af}\Delta f}{C_{ox}W_{eff}L_{eff}f^{ef}}$$

where

(13-93)

$$\overline{i_{n,\,thermal}^2} = \frac{8kT(g_m + g_{mb} + g_{ds})\Delta f}{3}\left[\frac{3}{2} - \frac{V'_{DS}}{2V_{DSAT}}\right]$$

© 2023 Cadence Design Systems, Inc.

(13-94)

$$V'_{DS} = MIN(V_{DS}, V_{DSAT})$$

g_m is the transconductance, g_{ds} is the channel conductance, and g_{mb} is the body transconductance. The Spectre® circuit simulator default values for kf, af, and ef are 0.0, 1.0, and 1.0, respectively.

Related Topics

Common MOSFET Equations

Source/Drain Bulk Junction Models

Temperature Effect on Model Parameters

Parameters Common to BSIM1 and BSIM2 Models

© 2023 Cadence Design Systems, Inc.

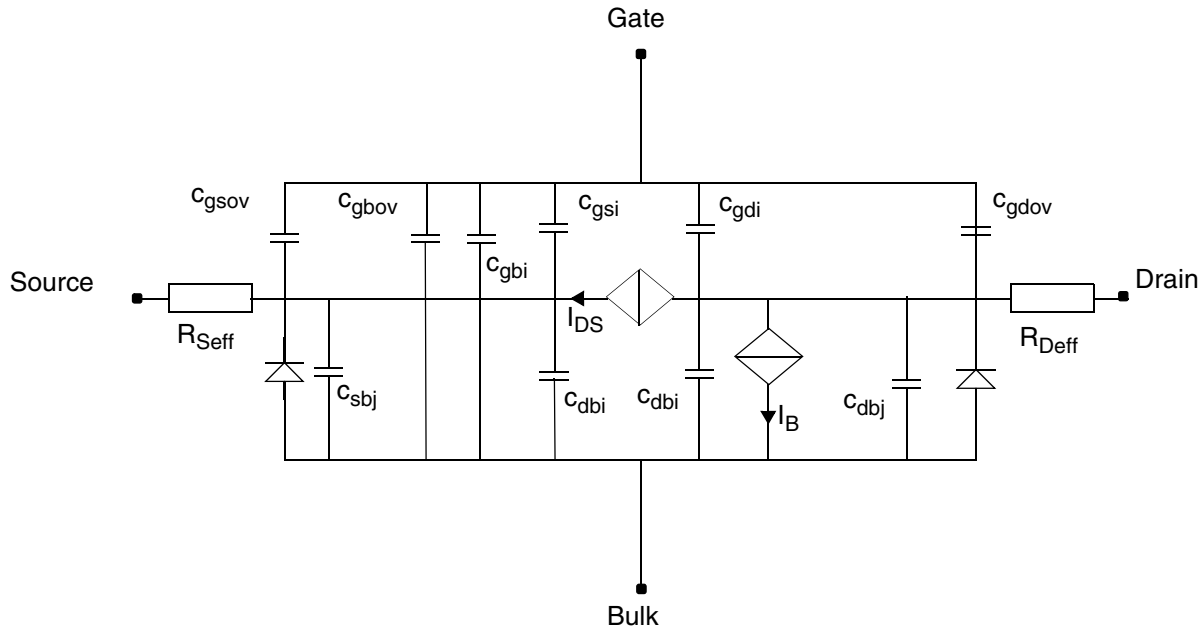
© 2023 Cadence Design Systems, Inc.

14

MOS Capacitance Model

Click the following links to view model equations for the MOS capacitance model:

- Modified Meyer Model
- Yang-Chatterjee Model
- BSIM Charge Model with 0/100 Partitioning (xpart=1)
- BSIM Charge Model with 40/60 Partitioning (xpart=0)
- BSIM Charge Model with 50/50 Partitioning (xpart=0.5)
- Scaling Effects



The Spectre® circuit simulator has three charge-based MOS capacitance models that you can select with the model parameter `capmod`:

© 2023 Cadence Design Systems, Inc.

- The modified Meyer model

  The modified Meyer model is a first-order model with 40/60 channel charge partitioning in the saturation region. This model does not include any short-channel effects.

- The Yang-Chatterjee model

  The Yang-Chatterjee model uses a 0/100 channel charge partitioning method and includes some short-channel effects.

- The BSIM charge model

  The BSIM charge model provides three methods for partitioning. You choose the method you want with the `xpart` parameter:

  - 40/60 for `xpart = 0` (or `xpart < 0.5`)

    For `xpart = 0`, the BSIM charge model is similar to the modified Meyer model, but it includes short-channel effects.

  - 50/50 for `xpart = 0.5`

  - 0/100 for `xpart = 1.0` (or `xpart > 0.5`)

    For `xpart = 1`, the BSIM charge model is identical to the Yang-Chatterjee model.

Modified Meyer Model

(14-1)

$$V_{TH} = V_{FB} + phi + gamma\sqrt{phi - V_{BS}}$$

(14-2)

$$V_{DSAT} = V_{GS} - V_{TH}$$

(14-3)

$$V_{GST} = V_{GS} - V_{TH}$$

(14-4)

$$V_{GDT} = V_{GS} - V_{TH} - V_{DS}$$

© 2023 Cadence Design Systems, Inc.

(14-5)

$$C_o = C_{ox} W_{eff} L_{eff}$$

(14-6)

$$C_{ij} \equiv \frac{dQ_i}{dV_j} \qquad i, j = g, d, s, b$$

Accumulation Region

Note: These equations apply when $V_{GS} - V_{BS} \leq V_{FB}$.

(14-7)

$$C_{gg} = C_{bb} = C_o$$

(14-8)

$$C_{gb} = C_{bg} = -C_o$$

All other capacitances are zero.

Subthreshold Region

Note: These equations apply when $V_{GS} \leq V_{TH}$.

(14-9)

$$C_{gg} = C_{bb} = \frac{C_o gamma}{2\sqrt{\left(\frac{gamma}{2}\right)^2 + V_{GS} - V_{BS} - V_{FB}}}$$

(14-10)

$$C_{gb} = C_{bg} = -C_{gg}$$

All other capacitances are zero.

© 2023 Cadence Design Systems, Inc.

Saturation Region

These equations apply when $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{DSAT}$.

(14-11)

$$C_{gg} = \frac{2}{3}C_o$$

(14-12)

$$C_{gb} = \frac{1}{3}C_o\frac{dV_{TH}}{dV_{BS}}$$

(14-13)

$$C_{gs} = -(C_{gg} + C_{gb})$$

(14-14)

$$C_{bb} = -C_o\frac{dV_{TH}}{dV_{BS}}$$

(14-15)

$$C_{bs} = -C_{bb}$$

(14-16)

$$C_{dg} = -\frac{4}{15}C_o$$

(14-17)

$$C_{db} = \frac{4}{15}C_o\frac{dV_{TH}}{dV_{BS}}$$

(14-18)

© 2023 Cadence Design Systems, Inc.

$$C_{ds} = -(C_{dg} + C_{db})$$

(14-19)

$$C_{sg} = -\frac{6}{15}C_o$$

(14-20)

$$C_{sb} = \frac{6}{15}C_o\frac{dV_{TH}}{dV_{BS}}$$

(14-21)

$$C_{ss} = -(C_{sg} + C_{sb})$$

All other capacitances are zero.

Triode Region

Note: These equations apply when $V_{GS} \geq V_{TH}$ and $V_{DS} \leq V_{DSAT}$.

(14-22)

$$C_{gg} = \frac{2}{3}C_o\left[1 + \frac{2V_{GST}V_{GDT}}{(V_{GST} + V_{GDT})^2}\right]$$

(14-23)

$$C_{gd} = -\frac{2}{3}C_o\left[1 - \frac{V_{GST}^2}{(V_{GST} + V_{GDT})^2}\right]$$

(14-24)

$$C_{gb} = \frac{1}{3}C_o\left[1 - \frac{4V_{GST}V_{GDT}}{(V_{gst} + V_{GDT})^2}\right]$$

© 2023 Cadence Design Systems, Inc.

(14-25)

$$C_{gs} = -(C_{gg} + C_{gd} + C_{gb})$$

(14-26)

$$C_{bb} = -C_o \frac{dV_{TH}}{dV_{BS}}$$

(14-27)

$$C_{bs} = -C_{bb}$$

(14-28)

$$C_{dg} = -\frac{1}{3} C_o \left[1 + \frac{2V_{GST}V_{GDT}}{(V_{GST} + V_{GDT})^2} + \frac{1}{5} \frac{(V_{GDT} - V_{GST})^3}{(V_{GST} + V_{GDT})^3} \right]$$

(14-29)

$$C_{dd} = \frac{2}{15} C_o \left[3 - \left(\frac{V_{GST}^2}{(V_{GST} + V_{GDT})^2} - \frac{2V_{GST}^3}{(V_{GST} + V_{GDT})^3} \right) \right]$$

(14-30)

$$C_{db} = \frac{1}{3} C_o \frac{dV_{TH}}{dV_{BS}} \left[1 + 2V_{GST}V_{GDT}(V_{GST} + V_{GDT})^2 + \frac{1}{5} \frac{(V_{GDT} - V_{GST})^3}{(V_{GST} + V_{GDT})^3} \right]$$

(14-31)

$$C_{ds} = -(C_{dg} + C_{dd} + C_{ds})$$

(14-32)

$$C_{sg} = -(C_{gg} + C_{dg}) = -\frac{1}{3} C_o \left[1 + \frac{2V_{GST}V_{GDT}}{(V_{GST} + V_{GDT})^2} + \frac{1}{5} \frac{(V_{GST} - V_{GDT})^3}{(V_{GST} + V_{GDT})^3} \right]$$

© 2023 Cadence Design Systems, Inc.

(14-33)

$$C_{sg} = -(C_{gg} + C_{dg}) = \frac{4}{15} C_o \left(\frac{V_{GDT}}{(V_{GST} + V_{GDT})} \left[1 + \frac{V_{GST} V_{GDT}}{(V_{GST} + V_{GDT})^2} \right] \right)$$

(14-34)

$$C_{sb} = -(C_{gs} + C_{db} + C_{bb}) = \frac{1}{3} C_o \frac{dV_{TH}}{dV_{BS}} \left[1 + \frac{2 V_{GST} V_{GDT}}{(V_{GST} + V_{GDT})^2} + \frac{1}{5} \frac{(V_{GST} - V_{GDT})^3}{(V_{GST} + V_{GDT})^3} \right]$$

(14-35)

$$C_{ss} = -(C_{gs} + C_{ds} + C_{bs}) = -(C_{sg} + C_{sd} + C_{sb})$$

Related Topics

MOS Capacitance Model

Yang-Chatterjee Model

Yang-Chatterjee Model

(14-36)

$$V_{TH} = V_{FB} + phi + gamma \sqrt{phi - V_{BS}}$$

(14-37)

$$V_{GST} = V_{GS} - V_{TH}$$

(14-38)

$$V_{GDT} = V_{GS} - V_{TH} - V_{DS}$$

(14-39)

$$C_o = C_{ox} W_{eff} L_{eff}$$

© 2023 Cadence Design Systems, Inc.

(14-40)

$$\alpha_x = \frac{V_{GST}}{V_{DSAT}}$$

(14-41)

$$C_{ij} \equiv \frac{dQ_i}{dV_j} \qquad i, j = g, d, s, b$$

Accumulation Region

Note: These equations apply when $V_{GS} - V_{BS} \leq V_{FB}$.

(14-42)

$$C_{gg} = C_{bb} = C_o$$

(14-43)

$$C_{gb} = C_{bg} = -C_o$$

All other capacitances are zero.

Subthreshold Region

Note: These equations apply when $V_{GS} \leq V_{TH}$.

(14-44)

$$C_{gg} = C_{bb} = \frac{C_o gamma}{2\sqrt{\left(\frac{gamma}{2}\right)^2 + V_{GS} - V_{BS} - V_{FB}}}$$

(14-45)

$$C_{gb} = C_{bg} = -C_{gg}$$

© 2023 Cadence Design Systems, Inc.

All other capacitances are zero.

Saturation Region

Note: These equations apply when $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{DSAT}$.

(14-46)

$$C_{gg} = C_o\left[1 - \frac{1}{3\alpha_x} + \frac{V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{GS}}\right]$$

(14-47)

$$C_{gb} = C_o\left[\frac{1}{3\alpha_x}\frac{dV_{TH}}{dV_{BS}} + \frac{V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{BS}}\right]$$

(14-48)

$$C_{gs} = -(C_{gg} + C_{gb})$$

(14-49)

$$C_{bg} = C_o\left[\frac{V_{GST}}{3\alpha_x}\frac{d\alpha_x}{dV_{GS}} - \frac{(1-\alpha_x)}{3\alpha_x} + \frac{(1-\alpha_x)V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{GS}}\right]$$

(14-50)

$$C_{bb} = C_o\left[-\frac{dV_{TH}}{dV_{BS}} + \frac{V_{GST}}{3\alpha_x}\frac{d\alpha_x}{dV_{BS}} + \frac{(1-\alpha_x)}{3\alpha_x}\frac{d\alpha_x}{dV_{BS}} + \frac{(1-\alpha_x)V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{BS}}\right]$$

(14-51)

$$C_{bs} = -(C_{bg} + C_{bb})$$

(14-52)

© 2023 Cadence Design Systems, Inc.

$$C_{sg} = -\frac{2}{3}C_o$$

(14-53)

$$C_{sb} = \frac{2}{3}C_o\frac{dV_{TH}}{dV_{BS}}$$

(14-54)

$$C_{ss} = -(C_{sg} + C_{sb})$$

All other capacitances are zero.

Triode Region

Note: These equations apply when $V_{GS} \geq V_{TH}$ and $V_{DS} \leq V_{DSAT}$.

(14-55)

$$Fac \equiv \left(V_{GST} - \frac{1}{2}\alpha_x V_{DS}\right)$$

(14-56)

$$C_{gg} = C_o\left[1 + \frac{V_{DS}^2}{12Fac}\frac{d\alpha_x}{dV_{GS}} - \frac{\alpha_x V_{DS}^2}{12Fac^2}\left(1 - \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}}\right)\right]$$

(14-57)

$$C_{gd} = C_o\left[-\frac{1}{2} + \frac{V_{DS}^2}{12Fac}\frac{d\alpha_x}{dV_{DS}} + \frac{\alpha_x V_{DS}}{6Fac} + \frac{\alpha_x^2 V_{DS}^2}{24Fac^2}\right]$$

(14-58)

$$C_{gb} = Co\left[\frac{V_{DS}^2}{12Fac}\frac{d\alpha_x}{dV_{BS}} + \frac{\alpha_x V_{DS}^2}{12Fac^2}\left(\frac{dV_{TH}}{dV_{BS}} + \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{BS}}\right)\right]$$

© 2023 Cadence Design Systems, Inc.

(14-59)

$$C_{gs} = -(C_{gg} + C_{gd} + C_{gb})$$

(14-60)

$$C_{bg} = C_o\left[-\frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}} - \frac{(1-2\alpha_x)V_{DS}^2}{12Fac}\frac{d\alpha_x}{dV_{GS}} + \frac{(1-\alpha_x)\alpha_x V_{DS}^2}{12Fac^2}\left(1 - \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}}\right)\right]$$

(14-61)

$$C_{bb} = C_o\left[-\frac{dV_{TH}}{dV_{BS}} - \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{BS}} - \frac{(1-2\alpha_x)V_{DS}^2}{12Fac}\frac{d\alpha_x}{dV_{BS}} - \frac{(1-\alpha_x)\alpha_x V_{DS}^2}{12Fac^2}\left(\frac{dV_{TH}}{dV_{BS}} + \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{BS}}\right)\right]$$

(14-62)

$$C_{bd} = C_o\left[\frac{(1-\alpha_x)}{2} - \frac{(1-\alpha_x)\alpha_x V_{DS}}{6Fac} - \frac{(1-\alpha_x)\alpha_x^2 V_{DS}^2}{24Fac^2}\right]$$

(14-63)

$$C_{bs} = -(C_{bg} + C_{bd} + C_{bb})$$

(14-64)

$$C_{dg} = -C_o\left[\frac{1}{2} - \frac{V_{DS}}{4}\left(3 - \frac{\alpha_x V_{DS}}{Fac}\right)\frac{d\alpha_x}{dV_{GS}} - \frac{\alpha_x^2 V_{DS}^2}{8Fac}\left(1 - \frac{V_{DS}}{2}\right)d\alpha_x dV_{GS}\right]$$

(14-65)

$$C_{db} = -C_o\left[-\frac{1}{2}\frac{dV_{TH}}{dV_{BS}} - \frac{V_{DS}}{4}\left(3 - \frac{\alpha_x V_{DS}}{Fac}\right)\frac{d\alpha_x}{dV_{BS}} - \frac{\alpha_x^2 V_{DS}^2}{8Fac}\left(1 - \frac{V_{DS}}{2}\right)\frac{d\alpha_x}{dV_{BS}}\right]$$

(14-66)

© 2023 Cadence Design Systems, Inc.

$$C_{dd} = -C_o\left[-\frac{3}{4}\alpha_x + \frac{\alpha_x^2 V_{DS}}{4Fac} + \frac{\alpha_x^3 V_{DS}^2}{16Fac^2}\right]$$

(14-67)

$$C_{ds} = -(C_{dg} + C_{dd} + C_{ds})$$

(14-68)

$$C_{sg} = -(C_{gg} + C_{dg} + C_{bg})$$

(14-69)

$$C_{sd} = -(C_{gd} + C_{dd} + C_{bd})$$

(14-70)

$$C_{sb} = -(C_{gb} + C_{db} + C_{bb})$$

(14-71)

$$C_{ss} = -(C_{gs} + C_{ds} + C_{bs})$$

BSIM Charge Model with 0/100 Partitioning (xpart=1)

This model is the same as the Yang-Chatterjee model.

BSIM Charge Model with 40/60 Partitioning (xpart=0)

(14-72)

$$V_{TH} = V_{FB} + phi + gamma\sqrt{phi - V_{BS}}$$

(14-73)

$$V_{GST} = V_{GS} - V_{TH}$$

© 2023 Cadence Design Systems, Inc.

(14-74)

$$V_{GDT} = V_{GS} - V_{TH} - V_{DS}$$

(14-75)

$$C_o = C_{ox} W_{eff} L_{eff}$$

(14-76)

$$\alpha_x = \frac{V_{GST}}{V_{DSAT}}$$

(14-77)

$$C_{ij} \equiv \frac{dQ_i}{dV_j} \qquad i, j = g, d, s, b$$

Accumulation Region

Note: These equations apply when $V_{GS} - V_{BS} \leq V_{FB}$.

(14-78)

$$C_{gg} = C_{bb} = C_o$$

(14-79)

$$C_{gb} = C_{bg} = -C_o$$

All other capacitances are zero.

Subthreshold Region

Note: These equations apply when $V_{GS} \leq V_{TH}$.

(14-80)

© 2023 Cadence Design Systems, Inc.

$$C_{gg} = C_{bb} = \frac{C_o gamma}{2\sqrt{\left(\frac{gamma}{2}\right)^2 + V_{GS} - V_{BS} - V_{FB}}}$$

(14-81)

$$C_{gb} = C_{bg} = -C_{gg}$$

All other capacitances are zero.

Saturation Region

Note: These equations apply when $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{DSAT}$.

(14-82)

$$C_{gg} = C_o\left[1 - \frac{1}{3\alpha_x} + \frac{V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{GS}}\right]$$

(14-83)

$$C_{gb} = C_o\left[\frac{1}{3\alpha_x}\frac{dV_{TH}}{dV_{BS}} + \frac{V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{BS}}\right]$$

(14-84)

$$C_{gs} = -(C_{gg} + C_{gb})$$

(14-85)

$$C_{bg} = C_o\left[\frac{V_{GST}}{3\alpha_x}\frac{d\alpha_x}{dV_{gs}} - \frac{(1-\alpha_x)}{3\alpha_x} + \frac{(1-\alpha_x)V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{GS}}\right]$$

(14-86)

© 2023 Cadence Design Systems, Inc.

$$C_{bb} = C_o\left[-\frac{dV_{TH}}{dV_{BS}} + \frac{V_{GST}}{3\alpha_x}\frac{d\alpha_x}{dV_{BS}} + \frac{(1-\alpha_x)}{3\alpha_x}\frac{d\alpha_x}{dV_{BS}} + \frac{(1-\alpha_x)V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{BS}}\right]$$

(14-87)

$$C_{bs} = -(C_{bg} + C_{bb})$$

(14-88)

$$C_{sg} = -\frac{6}{15}C_o$$

(14-89)

$$C_{sb} = \frac{6}{15}C_o\frac{dV_{TH}}{dV_{BS}}$$

(14-90)

$$C_{ss} = -(C_{sg} + C_{sb})$$

(14-91)

$$C_{dg} = -\frac{4}{15}C_o$$

(14-92)

$$C_{db} = \frac{4}{15}C_o\frac{dV_{TH}}{dV_{BS}}$$

(14-93)

$$C_{ds} = -(C_{dg} + C_{db})$$

All other capacitances are zero.

© 2023 Cadence Design Systems, Inc.

Triode Region

Note: These equations apply when $V_{GS} \geq V_{TH}$ and $V_{DS} \leq V_{DSAT}$.

(14-94)

$$Fac \equiv (2V_{DSAT} - V_{DS})$$

(14-95)

$$C_{gg} = C_o\left[1 + \frac{V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{GS}} - \frac{V_{DS}^2}{3\alpha_x Fac^2}\left(1 - \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}}\right)\right]$$

(14-96)

$$C_{gd} = C_o\left[-\frac{1}{2} + \frac{V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{DS}} + \frac{V_{DS}}{3Fac} + \frac{V_{DS}^2}{6Fac^2}\right]$$

(14-97)

$$C_{gb} = Co\left[\frac{V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{BS}} + \frac{V_{DS}^2}{3\alpha_x Fac^2}\left(\frac{dV_{TH}}{dV_{BS}} + \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{BS}}\right)\right]$$

(14-98)

$$C_{gs} = -(C_{gg} + C_{gd} + C_{gb})$$

(14-99)

$$C_{bg} = C_o\left[-\frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}} - \frac{(1-2\alpha_x)V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{GS}} + \frac{(1-\alpha_x)V_{DS}^2}{3\alpha_x Fac^2}\left(1 - \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}}\right)\right]$$

(14-100)

$$C_{bd} = C_o\left[\frac{(1-\alpha_x)}{2} - \frac{(1-\alpha_x)V_{DS}}{3Fac} - \frac{(1-\alpha_x)V_{DS}^2}{12Fac^2}\right]$$

© 2023 Cadence Design Systems, Inc.

(14-101)

$$C_{bs} = -(C_{bg} + C_{bd} + C_{bb})$$

(14-102)

$$C_{dg} = -\frac{C_o}{4}\left[2V_{DSAT} - 2V_{DS} + \frac{V_{DS}}{3Fac^2}\left(8V_{DSAT}^2 - 6V_{DSAT}V_{DS} + \frac{6}{5}V_{DS}^2\right)\right]\frac{d\alpha_x}{dV_{GS}}$$
$$-\frac{\alpha_x}{4}C_o\left[2 - \frac{4V_{DS}}{3Fac^3}\left(8V_{DSAT}^2 - 6V_{DSAT}V_{DS} + \frac{6}{5}V_{DS}^2\right) + \frac{V_{DS}(16V_{DSAT} - 6V_{DS})}{3Fac^2}\right]\frac{dV_{DSAT}}{dV_{GS}}$$

(14-103)

$$C_{db} = -\frac{C_o}{4}\left[2V_{DSAT} - 2V_{DS} + \frac{V_{DS}}{3Fac^2}\left(8V_{DSAT}^2 - 6V_{DSAT}V_{DS} + \frac{6}{5}V_{DS}^2\right)\right]\frac{d\alpha_x}{dV_{BS}}$$
$$-\frac{\alpha_x}{4}C_o\left[2 - \frac{4V_{DS}}{3Fac^3}\left(8V_{DSAT}^2 - 6V_{DSAT}V_{DS} + \frac{6}{5}V_{DS}^2\right) + \frac{V_{DS}(16V_{DSAT} - 6V_{DS})}{3Fac^2}\right]\frac{dV_{DSAT}}{dV_{BS}}$$

(14-104)

$$C_{dd} = \frac{\alpha_x}{4}C_o\left[\left(2 + \left(\frac{1}{3Fac^2} + \frac{2V_{DS}}{3Fac^3}\right)\left(8V_{DSAT}^2 - 6V_{DSAT}V_{DS} + \frac{6}{5}V_{DS}^2\right)\right)\right.$$
$$\left. + \frac{V_{DS}\left(\frac{12}{5}V_{DS} - 6V_{DSAT}\right)}{3Fac^2}\right]$$

(14-105)

$$C_{ds} = -(C_{dg} + C_{dd} + C_{ds})$$

(14-106)

$$C_{sg} = -(C_{gg} + C_{dg} + C_{bg})$$

(14-107)

© 2023 Cadence Design Systems, Inc.

$$C_{sd} = -(C_{gd} + C_{dd} + C_{bd})$$

(14-108)

$$C_{sb} = -(C_{gb} + C_{db} + C_{bb})$$

(14-109)

$$C_{ss} = -(C_{gs} + C_{ds} + C_{bs})$$

BSIM Charge Model with 50/50 Partitioning (xpart=0.5)

(14-110)

$$V_{TH} = V_{FB} + phi + gamma\sqrt{phi - V_{BS}}$$

(14-111)

$$V_{GST} = V_{GS} - V_{TH}$$

(14-112)

$$V_{GDT} = V_{GS} - V_{TH} - V_{DS}$$

(14-113)

$$C_o = C_{ox} W_{eff} L_{eff}$$

(14-114)

$$\alpha_x = \frac{V_{GST}}{V_{DSAT}}$$

(14-115)

$$C_{ij} \equiv \frac{dQ_i}{dV_j} \qquad i, j = g, d, s, b$$

© 2023 Cadence Design Systems, Inc.

Accumulation Region

Note: These equations apply when $V_{GS} - V_{BS} \le V_{FB}$.

(14-116)

$$C_{gg} = C_{bb} = C_o$$

(14-117)

$$C_{gb} = C_{bg} = -C_o$$

All other capacitances are zero.

Subthreshold Region

Note: These equations apply when $V_{GS} \le V_{TH}$.

(14-118)

$$C_{gg} = C_{bb} = \frac{C_o gamma}{2\sqrt{\left(\frac{gamma}{2}\right)^2 + V_{GS} - V_{BS} - V_{FB}}}$$

(14-119)

$$C_{gb} = C_{bg} = -C_{gg}$$

All other capacitances are zero.

Saturation Region

Note: These equations apply when $V_{GS} \ge V_{TH}$ and $V_{DS} \ge V_{DSAT}$.

(14-120)

$$C_{gg} = C_o\left[1 - \frac{1}{3\alpha_x} + \frac{V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{GS}}\right]$$

© 2023 Cadence Design Systems, Inc.

(14-121)

$$C_{gb} = C_o\left[\frac{1}{3\alpha_x}\frac{dV_{TH}}{dV_{BS}} + \frac{V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{BS}}\right]$$

(14-122)

$$C_{gs} = -(C_{gg} + C_{gb})$$

(14-123)

$$C_{bg} = C_o\left[\frac{V_{GST}}{3\alpha_x}\frac{d\alpha_x}{dV_{gs}} - \frac{(1-\alpha_x)}{3\alpha_x} + \frac{(1-\alpha_x)V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{GS}}\right]$$

(14-124)

$$C_{bb} = C_o\left[-\frac{dV_{TH}}{dV_{BS}} + \frac{V_{GST}}{3\alpha_x}\frac{d\alpha_x}{dV_{BS}} + \frac{(1-\alpha_x)}{3\alpha_x}\frac{d\alpha_x}{dV_{BS}} + \frac{(1-\alpha_x)V_{GST}}{3\alpha_x^2}\frac{d\alpha_x}{dV_{BS}}\right]$$

(14-125)

$$C_{bs} = -(C_{bg} + C_{bb})$$

(14-126)

$$C_{sg} = C_{dg} = -\frac{1}{3}C_o$$

(14-127)

$$C_{sb} = C_{db} = \frac{1}{3}C_o\frac{dV_{TH}}{dV_{BS}}$$

(14-128)

$$C_{ss} = C_{ds} = -(C_{sg} + C_{sb})$$

All other capacitances are zero.

© 2023 Cadence Design Systems, Inc.

Triode Region

Note: These equations apply when $V_{GS} \geq V_{TH}$ and $V_{DS} \leq V_{DSAT}$.

(14-129)

$$Fac \equiv (2V_{DSAT} - V_{DS})$$

(14-130)

$$C_{gg} = C_o\left[1 + \frac{V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{GS}} - \frac{V_{DS}^2}{3\alpha_x Fac^2}\left(1 - \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}}\right)\right]$$

(14-131)

$$C_{gd} = C_o\left[-\frac{1}{2} + \frac{V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{DS}} + \frac{V_{DS}}{3Fac} + \frac{V_{DS}^2}{6Fac^2}\right]$$

(14-132)

$$C_{gb} = C_o\left[\frac{V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{BS}} + \frac{V_{DS}^2}{3\alpha_x Fac^2}\left(\frac{dV_{TH}}{dV_{BS}} + \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{BS}}\right)\right]$$

(14-133)

$$C_{gs} = -(C_{gg} + C_{gd} + C_{gb})$$

(14-134)

$$C_{bg} = C_o\left[-\frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}} - \frac{(1-2\alpha_x)V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{GS}} + \frac{(1-\alpha_x)V_{DS}^2}{3\alpha_x Fac^2}\left(1 - \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{GS}}\right)\right]$$

(14-135)

$$C_{bb} = C_o\left[-\frac{dV_{TH}}{dV_{BS}} - \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{BS}} - \frac{(1-2\alpha_x)V_{DS}^2}{6\alpha_x Fac}\frac{d\alpha_x}{dV_{BS}} - \frac{(1-\alpha_x)V_{DS}^2}{3\alpha_x Fac^2}\left(\frac{dV_{TH}}{dV_{BS}} + \frac{V_{DS}}{2}\frac{d\alpha_x}{dV_{BS}}\right)\right]$$

© 2023 Cadence Design Systems, Inc.

(14-136)

$$C_{bd} = C_o\left[\frac{(1-\alpha_x)}{2} - \frac{(1-\alpha_x)V_{DS}}{3Fac} - \frac{(1-\alpha_x)V_{DS}^2}{12Fac^2}\right]$$

(14-137)

$$C_{bs} = -(C_{bg} + C_{bd} + C_{bb})$$

(14-138)

$$C_{sg} = C_{dg} = -\frac{1}{4}C_o\left(2V_{DSAT} - V_{DS} + \frac{V_{DS}}{3Fac}\right)\frac{d\alpha_x}{dV_{GS}} - \frac{\alpha_x}{4}C_o\left(2 - \frac{2V_{DS}^2}{3Fac^2}\right)\frac{dV_{DSAT}}{dV_{GS}}$$

(14-139)

$$C_{sb} = C_{db} = -\frac{1}{4}C_o\left(2V_{DSAT} - V_{DS} + \frac{V_{DS}}{3Fac}\right)\frac{d\alpha_x}{dV_{BS}} - \frac{\alpha_x}{4}C_o\left(2 - \frac{2V_{DS}^2}{3Fac^2}\right)\frac{dV_{DSAT}}{dV_{BS}}$$

(14-140)

$$C_{sd} = C_{dd} = \frac{\alpha_x}{4}C_o\left(1 - \frac{2V_{DS}}{3Fac} - \frac{V_{DS}^2}{3Fac^2}\right)$$

(14-141)

$$C_{ss} = C_{ds} = -(C_{sg} + C_{sd} + C_{sb})$$

Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem).

Related Topics

MOS Capacitance Model

© 2023 Cadence Design Systems, Inc.

Modified Meyer Model

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

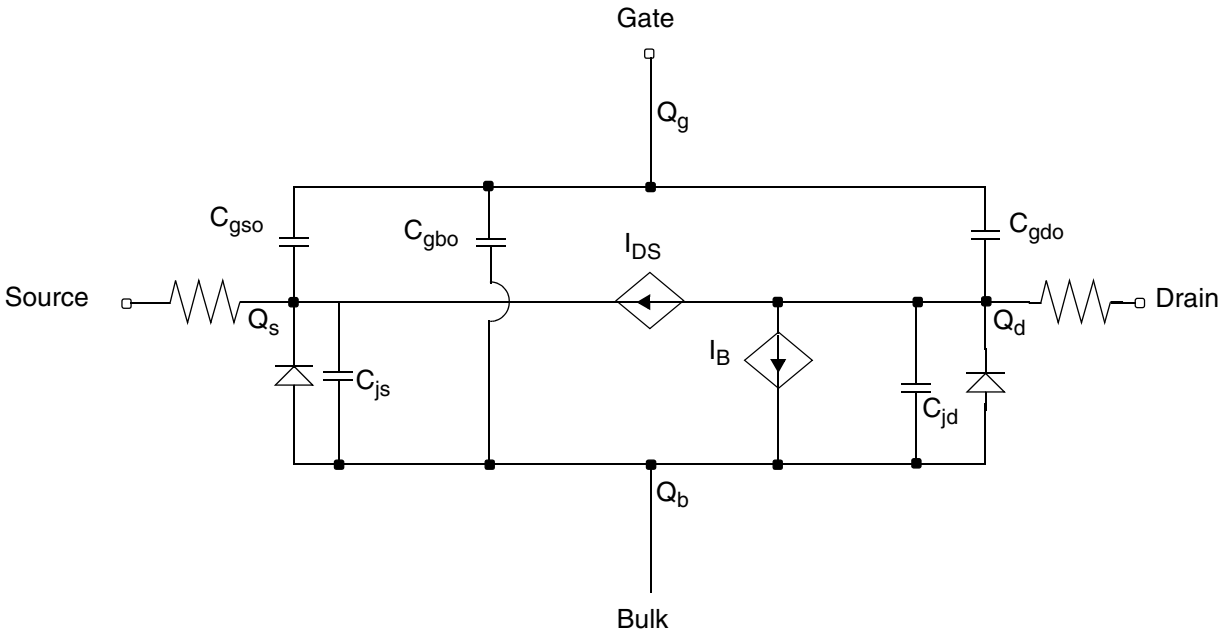
15

MOS Level-1 Model (mos1)

The MOS1 model is derived from the FET model of Shichman and Hodges. Velocity saturation and the mobility variation effects can also be incorporated into this model. Click the following links to view the information about the MOS1 model:

- Channel Width and Length
- Threshold Voltage
- Drain Saturation Voltage
- Drain Current for the Subthreshold Region
- Drain Current for the Triode Region
- Drain Current for the Saturation Region
- Drain Saturation Voltage (Modified Level-1 Model)
- Drain Current for the Triode Region (Modified Level-1 Model)
- Drain Current for the Saturation Region (Modified Level-1 Model)
- Substrate Current
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.



Channel Width and Length

(15-1)

$$W_{scaled} = w*scale + xw*scalem$$

(15-2)

$$W_{eff} = \begin{cases} w*scale + xw*scalem - 2wd*scalem & \text{(Level 1-3)} \\ w*scale + xw*scalem - dw*scalem & \text{(BSIM 1-2)} \end{cases}$$

(15-3)

$$L_{eff} = \begin{cases} l*scale + xl*scalem - 2ld*scalem & \text{(Level 1-3)} \\ l*scale + xl*scalem - dl*scalem & \text{(BSIM 1-2)} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Threshold Voltage

(15-4)

$$V_{TH} = vto + gamma(\sqrt{phi - V_{BS}} - \sqrt{phi})$$

Drain Saturation Voltage

(15-5)

$$V_{DSAT} = V_{GS} - V_{TH} \equiv V_{GST}$$

Drain Current for the Subthreshold Region

Note: These equations apply when $V_{GS} - V_{ON} \leq 0$.

You cannot use the subthreshold current equations without nfs.

(15-6)

$$V_{ON} = \begin{cases} V_{TH} + nV_t & \text{if } nfs \text{ is specified} \\ V_{TH} & \text{otherwise} \end{cases}$$

where

(15-7)

$$n = 1 + \frac{C_{FS} + C_D}{C_{ox}}$$

(15-8)

$$C_{FS} = q \times (nfs)$$

(15-9)

© 2023 Cadence Design Systems, Inc.

$$C_D = \frac{gamma\ C_{ox}}{2\sqrt{phi - V_{BS}}}$$

(15-10)

$$I_{DS} = I_{DS,ON} e^{(V_{GS} - V_{ON})/nV_t}$$

where $I_{DS,ON}$ is the drain current evaluated at $V_{GS} = V_{ON}$.

Drain Current for the Triode Region

Note: These equations apply when $V_{GS} \geq V_{ON}$ and $V_{DS} \leq V_{DSAT}$.

(15-11)

$$I_{DS} = \beta\left(V_{GST} - \frac{1}{2}V_{DS}\right)V_{DS}(1 + lambda * V_{DS})$$

where

(15-12)

$$\beta = \frac{kp * W_{eff}}{L_{eff}}$$

The mobility temperature offset parameter uto affects both u_{eff} and kp_{eff}, as shown below.

(15-13)

$$u_{eff} = uo * \mathrm{pow}(T/(Tnom + uto), ute)$$

(15-14)

$$kp_{eff} = kp * \mathrm{pow}(T/(Tnom + uto), ute)$$

© 2023 Cadence Design Systems, Inc.

Drain Current for the Saturation Region

Note: This equation applies when V_{GS}ŠV_{ON} and V_{DS}ŠV_{DSAT}.

(15-15)

$$I_{DS} = \frac{\beta V_{GST}^2}{2}(1 + lambda * V_{DS})$$

Because the standard SPICE Level-1 model does not include any of the short-channel phenomena, such as mobility modulation and velocity-saturation effects, the uses for this model are limited. To retain high computational efficiency and improve accuracy, the Spectre® circuit simulator incorporates two parameters, $theta$ and $vmax$, into the Level-1 model. The meanings of $theta$ and $vmax$ are the same as those in the Level-3 model. The modified Level-1 model is like a simplified Level-3 model. Spectre uses the modified Level-1 model if $theta$ or $vmax$ (or both) is specified. The drain current equations for the modified Level-1 model are shown in the following section.

Drain Saturation Voltage (Modified Level-1 Model)

(15-16)

$$V_{DSAT} = \frac{V_{GST}}{\sqrt{K}}$$

where

(15-17)

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2}$$

(15-18)

$$V_c = \frac{V_{GST} uo}{vmax * L_{eff}}$$

© 2023 Cadence Design Systems, Inc.

Drain Current for the Triode Region (Modified Level-1 Model)

(15-19)

$$I_{DS} = \frac{\beta\left(V_{GST} - \frac{1}{2}V_{DS}\right)V_{DS}[1 + lambda * V_{DS}]}{(1 + theta * V_{GST})(1 + V_{DS}/(E_c L_{eff}))}$$

where

(15-20)

$$E_c = \frac{vmax}{uo}$$

The mobility temperature offset parameter `uto` affects both u_{eff} and kp_{eff}, as shown below.

(15-21)

$$u_{eff} = u0*\mathrm{pow}(T/(Tnom + uto), ute)$$

(15-22)

$$kp_{eff} = kp*\mathrm{pow}(T/(Tnom + uto), ute)$$

Drain Current for the Saturation Region (Modified Level-1 Model)

(15-23)

$$I_{DS} = \frac{\beta\left(V_{GST} - \frac{1}{2}V_{DSAT}\right)V_{DSAT}[1 + lambda * V_{DS}]}{(1 + theta * V_{GST})(1 + V_{DSAT}/E_c L_{eff})}$$

© 2023 Cadence Design Systems, Inc.

Substrate Current

The substrate current is the result of impact ionization in the velocity saturation region near the drain. This impact-ionization induced current (I_{DB}) flows between the drain and the substrate. You need both aio and bio to use the impact-ionization model.

(15-24)

$$I_{DB} = \begin{cases} I_{DS} A_i (V_{DS} - V_{DSAT}) e^{-B_i/(V_{DS} - V_{DSAT})} & \text{if } V_{DS} < V_{DSAT} \\ 0 & \text{otherwise} \end{cases}$$

where

(15-25)

$$A_i = aio + \frac{laio \times 10^{-6}}{L_{eff}} + \frac{waio \times 10^{-6}}{W_{eff}}$$

(15-26)

$$B_i = bio + \frac{lbio \times 10^{-6}}{L_{eff}} + \frac{wbio \times 10^{-6}}{W_{eff}}$$

Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem).

Component Statements

This device is supported within altergroups.

Sample Instance Statement

```
nch1 (1 2 0 0) nchmod1 l=2u w=15u ad=60p as=37.5p pd=23u ps=6u
```


© 2023 Cadence Design Systems, Inc.

Sample Model Statement

```
model nchmod1 mos1 vto=0.78 gamma=0.56 kp=0.8675e-4 tox=0.21e-7 nsub=0.21e17
ld=0.55e-6 capmod=yang vmax=4e5 theta=0.19 cbs=11e-15 cbd=10e-15 lambda=0.1
```

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

w (m)	Channel width.
l (m)	Channel length.
as (m^2)	Area of source diffusion.
ad (m^2)	Area of drain diffusion.
ps (m)	Perimeter of source diffusion.
pd (m)	Perimeter of drain diffusion.
nrd (m/m)	Number of squares of drain diffusion.
nrs (m/m)	Number of squares of source diffusion.
ld (m)	Length of drain diffusion region.
ls (m)	Length of source diffusion region.
m=1	Multiplicity factor (number of MOSFETs in parallel).
region=triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, or `breakdown`.
trise	Temperature rise from ambient.
isnoisy=yes	Should resistor generate noise. Possible values are `no` or `yes`.
degradation=no	Hot-electron degradation flag. Possible values are `no` or `yes`.

Model Syntax

```
model modelName mos1 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

Drain current model parameters

`vto=0 V`	Threshold voltage at zero body bias.
`kp=2.0718e-5 A/V`^{2}	Transconductance parameter.
`lambda=0 1/V`	Channel length modulation parameter.
`phi=0.7 V`	Surface potential at strong inversion.
`gamma=0` $\sqrt{V}$	Body-effect parameter.
`uo=600 cm`^{2}`/V s`	Carrier surface mobility.
`vmax= 0.0 m/s`	Carrier saturation velocity.
`theta=0 1/V`	Mobility modulation coefficient.

Process parameters

`nsub=1.13e16 cm`$^{-3}$	Channel doping concentration.
`nss=0 cm`$^{-2}$	Surface state density.
`nfs=0 cm`$^{-2}$	Fast surface state density.
`tpg=+1`	Type of gate (+1 = opposite of substrate, -1 = same as substrate, 0 = aluminum).
`ld=0 m`	Lateral diffusion.
`wd=0 m`	Field-oxide encroachment.
`xw=0 m`	Width variation due to masking and etching.
`xl=0 m`	Length variation due to masking and etching.
`tox=1e-7 m`	Gate oxide thickness.

© 2023 Cadence Design Systems, Inc.

Impact ionization parameters

`ai0=0 1/V`	Impact ionization current coefficient.
`lai0=0 µm/V`	Length sensitivity of `ai0`.
`wai0=0 µm/V`	Width sensitivity of `ai0`.
`bi0=0 V`	Impact ionization current exponent.
`lbi0=0 µm V`	Length sensitivity of `bi0`.
`wbi0=0 µm V`	Width sensitivity of `bi0`.

Overlap capacitance parameters

`cgso=0 F/m`	Gate-source overlap capacitance.
`cgdo=0 F/m`	Gate-drain overlap capacitance.
`cgbo=0 F/m`	Gate-bulk overlap capacitance.
`meto=0 m`	Metal overlap in fringing field.

Charge model selection parameters

`capmod=bsim`	Intrinsic charge model. Possible values are `none`, `meyer`, `yang`, or `bsim`.
`xpart=1`	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
`xqc=0`	Drain/source channel charge partition in saturation for charge models, e.g. use 0.4 for 40/60, 0.5 for 50/50, 0 for 0/100.

Parasitic resistance parameters

`rs=0 Ω`	Source resistance.
`rd=0 Ω`	Drain resistance.
`rss=0 Ω m`	Scalable source resistance.
`rdd=0 Ω m`	Scalable drain resistance.

© 2023 Cadence Design Systems, Inc.

`rsh=0 Ω/sqr`	Source/drain diffusion sheet resistance.
`rsc=0 Ω`	Source contact resistance.
`rdc=0 Ω`	Drain contact resistance.
`minr=0.1 Ω`	Minimum source/drain resistance.
`ldif=0 m`	Lateral diffusion beyond the gate.
`hdif=0 m`	Length of heavily doped diffusion.
`lgcs=0 m`	Gate-to-contact length of source side.
`lgcd=0 m`	Gate-to-contact length of drain side.
`sc=∞ m`	Spacing between contacts.

© 2023 Cadence Design Systems, Inc.

Junction diode model parameters

`js (A/m^2)`	Bulk junction reverse saturation current density.
`is=1e-14 A`	Bulk junction reverse saturation current.
`n=1`	Junction emission coefficient.
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`. Possible values are `no` or `yes`.
`imelt=`imax' A`	Explosion current, diode is linearized beyond this current to aid convergence.
`jmelt=`jmax' A/m'^2`	Explosion current density, diode is linearized beyond this current to aid convergence.

Junction capacitance model parameters

`cbs=0 F`	Bulk-source zero-bias junction capacitance.
`cbd=0 F`	Bulk-drain zero-bias junction capacitance.
`cj=0 F/m^2`	Zero-bias junction bottom capacitance density.
`mj=1/2`	Bulk junction bottom grading coefficient.
`pb=0.8 V`	Bulk junction built-in potential.
`fc=0.5`	Forward-bias depletion capacitance threshold.
`cjsw=0 F/m`	Zero-bias junction sidewall capacitance density.
`mjsw=1/3`	Bulk junction sidewall grading coefficient.
`pbsw=0.8 V`	Side-wall junction built-in potential.
`fcsw=0.5`	Side-wall forward-bias depletion capacitance threshold.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, or `rev`.
`imax=1 A`	Maximum current, currents above this limit generate a warning.

© 2023 Cadence Design Systems, Inc.

`jmax=1e8 A/m`^{2}	Maximum current density, currents above this limit generate a warning.
`bvj=∞ V`	Junction reverse breakdown voltage.
`vbox=1e9 tox V`	Oxide breakdown voltage.

Temperature effects parameters

`tnom (C)`	Parameters measurement temperature. Default set by `options`.
`trise=0 C`	Temperature rise from ambient.
`uto=0 C`	Mobility temperature offset.
`ute=-1.5`	Mobility temperature exponent.
`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eg=1.12452 V`	Energy band gap.
`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.
`f1ex=0`	Temperature exponent for `ucrit`.
`lamex=0 1/C`	Temperature parameter for `lambda` and `kappa`.
`trs=0 1/C`	Temperature parameter for source resistance.
`trd=0 1/C`	Temperature parameter for drain resistance.
`xti=3`	Saturation current temperature exponent.
`ptc=0 V/C`	Surface potential temperature coefficient.
`tcv=0 V/C`	Threshold voltage temperature coefficient.
`pta=0 V/C`	Junction potential temperature coefficient.
`ptp=0 V/C`	Sidewall junction potential temperature coefficient.
`cta=0 1/C`	Junction capacitance temperature coefficient.
`ctp=0 1/C`	Sidewall junction capacitance temperature coefficient.

© 2023 Cadence Design Systems, Inc.

Default instance parameters

`w=3e-6 m`	Default channel width.
`l=3e-6 m`	Default channel length.
`as=0 m`^{2}	Default area of source diffusion.
`ad=0 m`^{2}	Default area of drain diffusion.
`ps=0 m`	Default perimeter of source diffusion.
`pd=0 m`	Default perimeter of drain diffusion.
`nrd=0 m/m`	Default number of squares of drain diffusion.
`nrs=0 m/m`	Default number of squares of source diffusion.
`ldd=0 m`	Default length of drain diffusion region.
`lds=0 m`	Default length of source diffusion region.

Noise model parameters

`noisemod=1`	Noise model selector.
`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`ef=1`	Flicker (1/f) noise frequency exponent.
`wnoi=1e-5 m`	Channel width at which noise parameters were extracted.

Auto Model Selector parameters

`wmax=1.0 m`	Maximum channel width for which the model is valid.
`wmin=0.0 m`	Minimum channel width for which the model is valid.
`lmax=1.0 m`	Maximum channel length for which the model is valid.
`lmin=0.0 m`	Minimum channel length for which the model is valid.

Degradation parameters

© 2023 Cadence Design Systems, Inc.

degramod=spectre	Degradation model selector. Possible values are spectre or bert.
degradation=no	Hot-electron degradation flag. Possible values are no or yes.
dvthc=1 V	Degradation coefficient for threshold voltage.
dvthe=1	Degradation exponent for threshold voltage.
duoc=1 S	Degradation coefficient for transconductance.
duoe=1	Degradation exponent for transconductance.
crivth=0.1 V	Maximum allowable threshold voltage shift.
criuo=10%	Maximum allowable normalized mobility change.
crigm=10%	Maximum allowable normalized transconductance change.
criids=10%	Maximum allowable normalized drain current change.
wnom=5e-6 m	Nominal device width in degradation calculation.
lnom=1e-6 m	Nominal device length in degradation calculation.
vbsn=0 V	Substrate voltage in degradation calculation.
vdsni=0.1 V	Drain voltage in Ids degradation calculation.
vgsni=5 V	Gate voltage in Ids degradation calculation.
vdsng=0.1 V	Drain voltage in Gm degradation calculation.
vgsng=5 V	Gate voltage in Gm degradation calculation.

Spectre stress parameters

esat=1.1e7 V/m	Critical field in Vdsat calculation.
esatg=2.5e6 1/m	Gate voltage dependence of esat.
vpg=-0.25	Gate voltage modifier.
vpb=-0.13	Gate voltage modifier.
subc1=2.24e-5	Substrate current coefficient.
subc2=-0.1e-5 1/V	Substrate current coefficient.

© 2023 Cadence Design Systems, Inc.

`sube=6.4`	Substrate current exponent.
`strc=1`	Stress coefficient.
`stre=1`	Stress exponent.

BERT stress parameters

`h0=1`	Aging coefficient.
`hgd=0 1/V`	Bias dependence of `h0`.
`m0=1`	Aging exponent.
`mgd=0 1/V`	Bias dependence of `m0`.
`ecrit0=1.1e5 V/cm`	Critical electric field.
`lecrit0=0 µm V/cm`	Length dependence of `ecrit0`.
`wecrit0=0 µm V/cm`	Width dependence of `ecrit0`.
`ecritg=0 1/cm`	Gate voltage dependence of `ecrit0`.
`lecritg=0 µm/cm`	Length dependence of `ecritg`.
`wecritg=0 µm/cm`	Width dependence of `ecritg`.
`ecritb=0 1/cm`	Substrate voltage dependence of `ecrit0`.
`lecritb=0 µm/cm`	Length dependence of `ecritb`.
`wecritb=0 µm/cm`	Width dependence of `ecritb`.
`lc0=1`	Substrate current coefficient.
`llc0=0 µm`	Length dependence of `lc0`.
`wlc0=0 µm`	Width dependence of `lc0`.
`lc1=1`	Substrate current coefficient.
`llc1=0 µm`	Length dependence of `lc1`.
`wlc1=0 µm`	Width dependence of `lc1`.
`lc2=1`	Substrate current coefficient.
`llc2=0 µm`	Length dependence of `lc2`.
`wlc2=0 µm`	Width dependence of `lc2`.
`lc3=1`	Substrate current coefficient.

© 2023 Cadence Design Systems, Inc.

`llc3=0 µm`	Length dependence of `lc3`.
`wlc3=0 µm`	Width dependence of `lc3`.
`lc4=1`	Substrate current coefficient.
`llc4=0 µm`	Length dependence of `lc4`.
`wlc4=0 µm`	Width dependence of `lc4`.
`lc5=1`	Substrate current coefficient.
`llc5=0 µm`	Length dependence of `lc5`.
`wlc5=0 µm`	Width dependence of `lc5`.
`lc6=1`	Substrate current coefficient.
`llc6=0 µm`	Length dependence of `lc6`.
`wlc6=0 µm`	Width dependence of `lc6`.
`lc7=1`	Substrate current coefficient.
`llc7=0 µm`	Length dependence of `lc7`.
`wlc7=0 µm`	Width dependence of `lc7`.

Shrink Parameters

Imax and Imelt:

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and Spectre prints a warning.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, the base and collector currents are composed of many exponential terms, Spectre issues a warning and the results become inaccurate. The junction current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

Both of these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

© 2023 Cadence Design Systems, Inc.

Auto Model Selection

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin` should be given. The selection criteria to choose a model is as follows:

lmin <= inst_length < lmax and wmin <= inst_width < wmax

Example:

model ModelName ModelType {

1: <model parameters> lmin=2 lmax=4 wmin=1 wmax=2

2: <model parameters> lmin=1 lmax=2 wmin=2 wmax=4

3: <model parameters> lmin=2 lmax=4 wmin=4 wmax=6

}

Then for a given instance

M1 1 2 3 4 ModelName w=3 l=1.5

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.

© 2023 Cadence Design Systems, Inc.

`weff (m)`	Effective channel width.
`meff`	Effective multiplicity factor (m-factor).
`leff (m)`	Effective channel length.
`rseff (Ω)`	Effective source resistance.
`rdeff (Ω)`	Effective drain resistance.
`aseff (m^2)`	Effective area of source diffusion.
`adeff (m^2)`	Effective area of drain diffusion.
`pseff (m)`	Effective perimeter of source diffusion.
`pdeff (m)`	Effective perimeter of source diffusion.
`isseff (A)`	Effective source-bulk junction reverse saturation current.
`isdeff (A)`	Effective drain-bulk junction reverse saturation current.
`cbseff (F)`	Effective zero-bias source-bulk junction capacitance.
`cbdeff (F)`	Effective zero-bias drain-bulk junction capacitance.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.
`region=triode`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, or `breakdown`.
`trise (C)`	Temperature rise from ambient.
`degradation=no`	Hot-electron degradation flag. Possible values are `no` or `yes`.
`reversed`	Reverse mode indicator. Possible values are `no` or `yes`.
`ids (A)`	Resistive drain-to-source current.
`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.

© 2023 Cadence Design Systems, Inc.

`vbs (V)`	Bulk-source voltage.
`vth (V)`	Threshold voltage.
`vdsat (V)`	Drain-source saturation voltage.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`gmbs (S)`	Body-transconductance.
`gameff` ($\sqrt{V}$)	Effective body effect coefficient.
`betaeff` (A/V^2)	Effective `beta`.
`cbd (F)`	Drain-bulk junction capacitance.
`cbs (F)`	Source-bulk junction capacitance.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`cgb (F)`	Gate-bulk capacitance.
`ron` (Ω)	On-resistance.
`id (A)`	Resistive drain current.
`ibulk (A)`	Resistive bulk current.
`pwr (W)`	Power at op point.
`gmoverid (1/V)`	`Gm/Ids`.
`isub (A)`	Substrate current.
`stress`	Hot-electron stress.
`age (s)`	Device age.
`he_vdsat (V)`	Hot Electron `Vdsat`.

Related Topics

MOS Level-1 Model (mos1)

MOS Capacitance Model

© 2023 Cadence Design Systems, Inc.

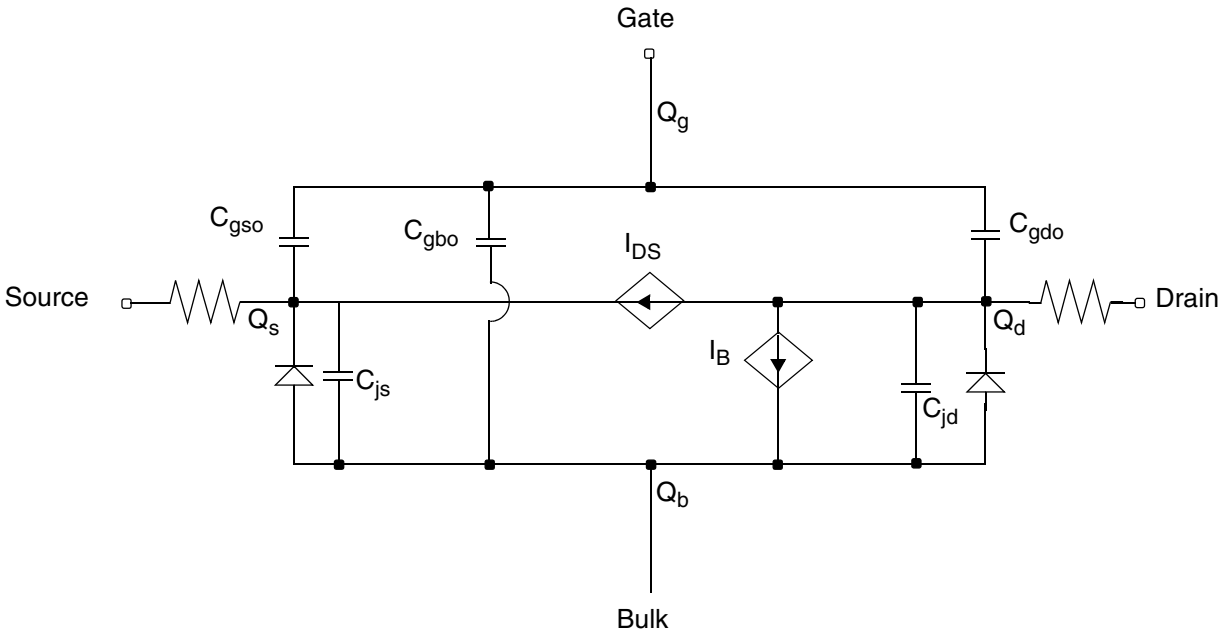
16

MOS Level-2 Model (mos2)

The MOS2 model is the level-2 model from Berkeley SPICE. The MOS2 model is an analytical, one-dimensional model that incorporates most of the second-order small-size effects. A smoother version of the level-2 model (with continuous `Gds` at `Vdsat`) as well as three charge models are also available. Click to view the following links for information about the MOS2 model:

- Channel Width and Length
- Threshold Voltage
- Drain Saturation Voltage
- Drain Current for the Subthreshold Region
- Drain Current for the Triode Region
- Drain Current for the Saturation Region
- Substrate Current
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.



Channel Width and Length

(16-1)

$$W_{scaled} = w*scale + xw*scalem$$

(16-2)

$$W_{eff} = \begin{cases} w*scale + xw*scalem - 2wd*scalem & \text{(Level 1-3)} \\ w*scale + xw*scalem - dw*scalem & \text{(BSIM 1-2)} \end{cases}$$

(16-3)

$$L_{eff} = \begin{cases} l*scale + xl*scalem - 2ld*scalem & \text{(Level 1-3)} \\ l*scale + xl*scalem - dl*scalem & \text{(BSIM 1-2)} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Threshold Voltage

(16-4)

$$V_{TH} = V_{BI} + \gamma_s \sqrt{phi - V_{BS}} + (\eta - 1)(phi - V_{BS})$$

where

(16-5)

$$V_{BI} = vto - gamma\sqrt{phi}$$

(16-6)

$$\gamma_s = gamma(1 - \alpha_S - \alpha_D)$$

(16-7)

$$\alpha_S = \frac{xj}{2L_{eff}}\left[\sqrt{1 + \frac{2W_S}{xj}} - 1\right]$$

(16-8)

$$\alpha_D = \frac{xj}{2L_{eff}}\left[\sqrt{1 + \frac{2W_D}{xj}} - 1\right]$$

(16-9)

$$W_S = X_D\sqrt{phi - V_{BS}}$$

(16-10)

$$W_D = X_D\sqrt{phi - V_{BS} + V_{DS}}$$

(16-11)

© 2023 Cadence Design Systems, Inc.

$$X_D = \begin{cases} \sqrt{\dfrac{2\varepsilon_{si}}{q*(nsub)}} & \text{if } vmax \text{ is not specified} \\ \sqrt{\dfrac{2\varepsilon_{si}}{q*neff*nsub}} & \text{otherwise} \end{cases}$$

(16-12)

$$\eta = 1 + \frac{delta\pi\varepsilon_{si}}{4C_{ox}W_{eff}}$$

If xj or $nsub$ is zero, the short-channel effects on threshold voltage are not evaluated (that is, $\gamma_s = gamma$).

Drain Saturation Voltage

If $vmax$ is not specified, V_{DSAT} is determined by the pinchoff condition and is given by

(16-13)

$$V_{DSAT} = \frac{V_{GS} - V_{BIN}}{\eta} + \frac{1}{2}\left(\frac{\gamma_s}{\eta}\right)^2 (1 - Fac)$$

where

(16-14)

$$V_{BIN} = V_{BI} + \frac{delta\pi\varepsilon_{si}}{4C_{ox}W_{eff}}(phi - V_{BS})$$

(16-15)

$$Fac = \sqrt{1 + 4\left(\frac{\eta}{\gamma_s}\right)^2\left(\frac{V_{GS} - V_{BIN}}{\eta} + phi - V_{BS}\right)}$$

If $vmax$ is specified, V_{DSAT} is determined by the velocity saturation effect.

© 2023 Cadence Design Systems, Inc.

(16-16)

$$vmax = \frac{I_{DSAT}}{W_{eff} Q_{chan}}$$

where

(16-17)

$$Q_{chan} = W_{eff} C_{ox}[V_{GS} - V_{BIN} - \eta V_{DSAT} - \gamma_s \sqrt{phi - V_{BS} + V_{DSAT}}]$$

μ_{eff} is the effective mobility, defined later. V_{DSAT} can be calculated by solving the preceding equations.

Drain Current for the Subthreshold Region

Note: These equations apply when $V_{GS} \leq V_{ON}$.

You cannot use the subthreshold current equations without *nfs*.

(16-18)

$$V_{ON} = \begin{cases} V_{TH} + nV_t & \text{if } nfs \text{ is specified} \\ V_{TH} & \text{otherwise} \end{cases}$$

where

(16-19)

$$n = 1 + \frac{C_{FS} + C_D}{C_{ox}}$$

(16-20)

$$C_{FS} = q \times (nfs)$$

(16-21)

© 2023 Cadence Design Systems, Inc.

$$C_D = \left[\frac{\gamma_s}{2\sqrt{phi - V_{BS}}} - \frac{d\gamma_s}{dV_{BS}}\sqrt{phi - V_{BS}} + (\eta - 1)\right]C_{ox}$$

(16-22)

$$I_{DS} = I_{DS,\,ON}e^{(V_{GS} - V_{ON})/nV_t}$$

where $I_{DS,ON}$ is the drain current evaluated at $V_{GS} = V_{ON}$.

Drain Current for the Triode Region

Note: These equations apply when $V_{GS} \geq V_{ON}$ and $V_{DS} \leq V_{DSAT}$.

(16-23)

$$I_{DS} = \beta\left\{\left(V_{GS} - V_{BIN} - \frac{\eta V_{DS}}{2}\right)V_{DS} - \frac{2}{3}\gamma_s[(phi - V_{BS} + V_{DS})^{3/2} - (phi - V_{BS})^{3/2}]\right\}$$

where

(16-24)

$$\beta = \frac{\mu_{eff}\, C_{ox} W_{eff}}{L_{eff} - \Delta L}$$

(16-25)

$$\mu_{eff} = uo\left[\frac{ucrit\ \varepsilon_{si}}{C_{ox}(V_{GS} - V_{TH} - utra * V_{DS})}\right]^{uexp}$$

SPICE does not implement the $utra$ effect. Also, if $(V_{GS} - V_{TH}) \leq (ucrit\varepsilon_{si}/C_{ox})$, μ_{eff} is clipped to uo. This creates a discontinuity in the first derivatives of the drain current. The Spectre® circuit simulator does not have this clipping effect.

(16-26)

© 2023 Cadence Design Systems, Inc.

$$\Delta L = \begin{cases} 0 & \text{if } lambda \text{ is given} \\ lambda\, L_{eff} V_{DS} & \text{if } nsub \text{ is not given} \\ X_D\sqrt{\left(\frac{V_{DS}-V_{DSAT}}{4}\right)+\sqrt{1+\left(\frac{V_{DS}-V_{DSAT}}{4}\right)^2}} & \text{if } vmax \text{ is not given} \\ X_D\left\{\sqrt{\left(\frac{X_D vmax}{2\mu_{eff}}\right)^2+V_{DS}-V_{DSAT}}-\frac{X_D vmax}{2\mu_{eff}}\right\} & \text{if } V_{DS}\geq V_{DSAT} \end{cases}$$

If $\Delta L \geq (L_{eff} - W_B)$, β is calculated from the following equation to avoid device punch-through:

(16-27)

$$\beta = \frac{\mu_{eff} C_{ox} W_{eff}}{L_{eff}}\left(\frac{L_{eff}}{W_B}\right)^2\left(\frac{2W_B}{L_{eff}}+\frac{\Delta L}{L_{eff}}-1\right)$$

where

(16-28)

$$W_B = X_D\sqrt{\mathrm{pb}}$$

Drain Current for the Saturation Region

Note: This equation applies when $V_{GS} \geq V_{ON}$ and $V_{DS} \geq V_{DSAT}$.

(16-29)

$$I_{DS} = \beta\left\{\left(V_{GS}-V_{BIN}-\frac{\eta V_{DSAT}}{2}\right)V_{DSAT}-\frac{2}{3}\gamma_s[(phi-V_{BS}+V_{DSAT})^{3/2}-(phi-V_{BS})^{3/2}]\right\}$$

© 2023 Cadence Design Systems, Inc.

Substrate Current

The substrate current results from impact ionization in the velocity saturation region near the drain. This impact-ionization induced current (I_{DB}) flows between the drain and the substrate. You need both aio and bio to use the impact-ionization model.

(16-30)

$$I_{DB} = \begin{cases} I_{DS} A_i (V_{DS} - V_{DSAT}) e^{-B_i/(V_{DS}-V_{DSAT})} & \text{if} \quad V_{DS} \le V_{DSAT} \\ 0 & \text{otherwise} \end{cases}$$

where

(16-31)

$$A_i = aio + \frac{laio \times 10^{-6}}{L_{eff}} + \frac{waio \times 10^{-6}}{W_{eff}}$$

(16-32)

$$B_i = bio + \frac{lbio \times 10^{-6}}{L_{eff}} + \frac{wbio \times 10^{-6}}{W_{eff}}$$

Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem).

Component Statements

This device is supported within altergroups.

Sample Instance Statement

```
mn2 (1 2 0 0) nch2 w=10u ad=20p as=20p ps=24u pd=24u
```

Sample Model Statement

```
model nch2 mos2 type=n vto=0.66 lambda=0.018 gamma=0.6 nsub=0.213e16 kp=0.978e-4
tpg=-1 vmax=6e4 ucrit=1e7 utra=0.1 uexp=0.2 is=0
```


© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

w (m)	Channel width.
l (m)	Channel length.
as (m^2)	Area of source diffusion.
ad (m^2)	Area of drain diffusion.
ps (m)	Perimeter of source diffusion.
pd (m)	Perimeter of drain diffusion.
nrd (m/m)	Number of squares of drain diffusion.
nrs (m/m)	Number of squares of source diffusion.
ld (m)	Length of drain diffusion region.
ls (m)	Length of source diffusion region.
m=1	Multiplicity factor (number of MOSFETs in parallel).
region=triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are off, triode, sat, subth, or breakdown.
trise	Temperature rise from ambient.
isnoisy=yes	Should resistor generate noise. Possible values are no or yes.
degradation=no	Hot-electron degradation flag. Possible values are no or yes.

Model Definition

```
model modelName mos2 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

Drain current model parameters

`vto=0 V`	Threshold voltage at zero body bias.
`kp=2.0718e-5 A/V`^{2}	Transconductance parameter.
`lambda=0 1/V`	Channel length modulation parameter.
`phi=0.7 V`	Surface potential at strong inversion.
`gamma=0` $\sqrt{V}$	Body-effect parameter.
`uo=600 cm`^{2}`/V s`	Carrier surface mobility.
`vmax=0.0 m/s`	Carrier saturation velocity.
`ucrit=0 V/cm`	Critical field for mobility degradation.
`uexp=0`	Critical field exponent for mobility degradation.
`utra=0 1/V`	Transverse field for mobility.
`neff=1`	Total channel charge coefficient.
`delta=0`	Width effect on threshold voltage.
`smooth=yes`	Drain current smoothing flag. Possible values are `no` or `yes`.

Process parameters

`nsub=1.13e16 cm`$^{-3}$	Channel doping concentration.
`nss=0 cm`$^{-2}$	Surface state density.
`nfs=0 cm`$^{-2}$	Fast surface state density.
`tpg=+1`	Type of gate (+1 = opposite of substrate, -1 = same as substrate, 0 = aluminum).

© 2023 Cadence Design Systems, Inc.

`tox=1e-7 m`	Gate oxide thickness.
`ld=0 m`	Lateral diffusion.
`wd=0 m`	Field-oxide encroachment.
`xw=0 m`	Width variation due to masking and etching.
`xl=0 m`	Length variation due to masking and etching.
`xj=0 m`	Source/drain junction depth.

© 2023 Cadence Design Systems, Inc.

Impact ionization parameters

`ai0=0 1/V`	Impact ionization current coefficient.
`lai0=0 µm/V`	Length sensitivity of `ai0`.
`wai0=0 µm/V`	Width sensitivity of `ai0`.
`bi0=0 V`	Impact ionization current exponent.
`lbi0=0 µm V`	Length sensitivity of `bi0`.
`wbi0=0 µm V`	Width sensitivity of `bi0`.

Overlap capacitance parameters

`cgso=0 F/m`	Gate-source overlap capacitance.
`cgdo=0 F/m`	Gate-drain overlap capacitance.
`cgbo=0 F/m`	Gate-bulk overlap capacitance.
`meto=0 m`	Metal overlap in fringing field.

Charge model selection parameters

`capmod=bsim`	Intrinsic charge model. Possible values are `none`, `meyer`, `yang`, or `bsim`.
`xpart=1`	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
`xqc=0`	Drain/source channel charge partition in saturation for charge models, e.g. use 0.4 for 40/60, 0.5 for 50/50, 0 for 0/100.

Parasitic resistance parameters

`rs=0 Ω`	Source resistance.
`rd=0 Ω`	Drain resistance.
`rsh=0 Ω/sqr`	Source/drain diffusion sheet resistance.
`rss=0 Ω m`	Scalable source resistance.

© 2023 Cadence Design Systems, Inc.

`rdd=0 Ω m`	Scalable drain resistance.
`rsc=0 Ω`	Source contact resistance.
`rdc=0 Ω`	Drain contact resistance.
`minr=0.1 Ω`	Minimum source/drain resistance.
`ldif=0 m`	Lateral diffusion beyond the gate.
`hdif=0 m`	Length of heavily doped diffusion.
`lgcs=0 m`	Gate-to-contact length of source side.
`lgcd=0 m`	Gate-to-contact length of drain side.
`sc=∞ m`	Spacing between contacts.

© 2023 Cadence Design Systems, Inc.

Junction diode model parameters

`js (A/m^2)`	Bulk junction reverse saturation current density.
`is=1e-14 A`	Bulk junction reverse saturation current.
`n=1`	Junction emission coefficient.
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`. Possible values are `no` or `yes`.
`imelt=`imax' A`	Explosion current, diode is linearized beyond this current to aid convergence.
`jmelt=`jmax' A/m'^2`	Explosion current density, diode is linearized beyond this current to aid convergence.

Junction capacitance model parameters

`cbs=0 F`	Bulk-source zero-bias junction capacitance.
`cbd=0 F`	Bulk-drain zero-bias junction capacitance.
`cj=0 F/m^2`	Zero-bias junction bottom capacitance density.
`mj=1/2`	Bulk junction bottom grading coefficient.
`pb=0.8 V`	Bulk junction built-in potential.
`fc=0.5`	Forward-bias depletion capacitance threshold.
`cjsw=0 F/m`	Zero-bias junction sidewall capacitance density.
`mjsw=1/3`	Bulk junction sidewall grading coefficient.
`pbsw=0.8 V`	Side-wall junction built-in potential.
`fcsw=0.5`	Side-wall forward-bias depletion capacitance threshold.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, or `rev`.
`imax=1 A`	Maximum current, currents above this limit generate a warning.

© 2023 Cadence Design Systems, Inc.

`jmax=1e8 A/m`^{2}	Maximum current density, currents above this limit generate a warning.
`bvj=∞ V`	Junction reverse breakdown voltage.
`vbox=1e9 tox V`	Oxide breakdown voltage.

Temperature effects parameters

`tnom (C)`	Parameters measurement temperature. Default set by `options`.
`trise=0 C`	Temperature rise from ambient.
`uto=0 C`	Mobility temperature offset.
`ute=-1.5`	Mobility temperature exponent.
`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eg=1.12452 V`	Energy band gap.
`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.
`f1ex=0`	Temperature exponent for `ucrit`.
`lamex=0 1/C`	Temperature parameter for `lambda` and `kappa`.
`trs=0 1/C`	Temperature parameter for source resistance.
`trd=0 1/C`	Temperature parameter for drain resistance.
`xti=3`	Saturation current temperature exponent.
`ptc=0 V/C`	Surface potential temperature coefficient.
`tcv=0 V/C`	Threshold voltage temperature coefficient.
`pta=0 V/C`	Junction potential temperature coefficient.
`ptp=0 V/C`	Sidewall junction potential temperature coefficient.
`cta=0 1/C`	Junction capacitance temperature coefficient.
`ctp=0 1/C`	Sidewall junction capacitance temperature coefficient.

© 2023 Cadence Design Systems, Inc.

Default instance parameters

`w=3e-6 m`	Default channel width.
`l=3e-6 m`	Default channel length.
`as=0 m`^{2}	Default area of source diffusion.
`ad=0 m`^{2}	Default area of drain diffusion.
`ps=0 m`	Default perimeter of source diffusion.
`pd=0 m`	Default perimeter of drain diffusion.
`nrd=0 m/m`	Default number of squares of drain diffusion.
`nrs=0 m/m`	Default number of squares of source diffusion.
`ldd=0 m`	Default length of drain diffusion region.
`lds=0 m`	Default length of source diffusion region.

Noise model parameters

`noisemod=1`	Noise model selector.
`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`ef=1`	Flicker (1/f) noise frequency exponent.
`wnoi=1e-5 m`	Channel width at which noise parameters were extracted.

Auto Model Selector parameters

`wmax=1.0 m`	Maximum channel width for which the model is valid.
`wmin=0.0 m`	Minimum channel width for which the model is valid.
`lmax=1.0 m`	Maximum channel length for which the model is valid.
`lmin=0.0 m`	Minimum channel length for which the model is valid.

© 2023 Cadence Design Systems, Inc.

Degradation parameters

`degramod=spectre`	Degradation model selector. Possible values are `spectre` or `bert`.
`degradation=no`	Hot-electron degradation flag. Possible values are `no` or `yes`.
`dvthc=1 V`	Degradation coefficient for threshold voltage.
`dvthe=1`	Degradation exponent for threshold voltage.
`duoc=1 S`	Degradation coefficient for transconductance.
`duoe=1`	Degradation exponent for transconductance.
`crivth=0.1 V`	Maximum allowable threshold voltage shift.
`criuo=10%`	Maximum allowable normalized mobility change.
`crigm=10%`	Maximum allowable normalized transconductance change.
`criids=10%`	Maximum allowable normalized drain current change.
`wnom=5e-6 m`	Nominal device width in degradation calculation.
`lnom=1e-6 m`	Nominal device length in degradation calculation.
`vbsn=0 V`	Substrate voltage in degradation calculation.
`vdsni=0.1 V`	Drain voltage in `Ids` degradation calculation.
`vgsni=5 V`	Gate voltage in `Ids` degradation calculation.
`vdsng=0.1 V`	Drain voltage in `Gm` degradation calculation.
`vgsng=5 V`	Gate voltage in `Gm` degradation calculation.

Spectre stress parameters

`esat=1.1e7 V/m`	Critical field in Vdsat calculation.
`esatg=2.5e6 1/m`	Gate voltage dependence of `esat`.
`vpg=-0.25`	Gate voltage modifier.
`vpb=-0.13`	Gate voltage modifier.
`subc1=2.24e-5`	Substrate current coefficient.
`subc2=-0.1e-5 1/V`	Substrate current coefficient.

© 2023 Cadence Design Systems, Inc.

sube=6.4	Substrate current exponent.
strc=1	Stress coefficient.
stre=1	Stress exponent.

BERT stress parameters

h0=1	Aging coefficient.
hgd=0 1/V	Bias dependence of h0.
m0=1	Aging exponent.
mgd=0 1/V	Bias dependence of m0.
ecrit0=1.1e5 V/cm	Critical electric field.
lecrit0=0 µm V/cm	Length dependence of ecrit0.
wecrit0=0 µm V/cm	Width dependence of ecrit0.
ecritg=0 1/cm	Gate voltage dependence of ecrit0.
lecritg=0 µm/cm	Length dependence of ecritg.
wecritg=0 µm/cm	Width dependence of ecritg.
ecritb=0 1/cm	Substrate voltage dependence of ecrit0.
lecritb=0 µm/cm	Length dependence of ecritb.
wecritb=0 µm/cm	Width dependence of ecritb.
lc0=1	Substrate current coefficient.
llc0=0 µm	Length dependence of lc0.
wlc0=0 µm	Width dependence of lc0.
lc1=1	Substrate current coefficient.
llc1=0 µm	Length dependence of lc1.
wlc1=0 µm	Width dependence of lc1.
lc2=1	Substrate current coefficient.
llc2=0 µm	Length dependence of lc2.
wlc2=0 µm	Width dependence of lc2.
lc3=1	Substrate current coefficient.

© 2023 Cadence Design Systems, Inc.

`llc3=0 µm`	Length dependence of `lc3`.
`wlc3=0 µm`	Width dependence of `lc3`.
`lc4=1`	Substrate current coefficient.
`llc4=0 µm`	Length dependence of `lc4`.
`wlc4=0 µm`	Width dependence of `lc4`.
`lc5=1`	Substrate current coefficient.
`llc5=0 µm`	Length dependence of `lc5`.
`wlc5=0 µm`	Width dependence of `lc5`.
`lc6=1`	Substrate current coefficient.
`llc6=0 µm`	Length dependence of `lc6`.
`wlc6=0 µm`	Width dependence of `lc6`.
`lc7=1`	Substrate current coefficient.
`llc7=0 µm`	Length dependence of `lc7`.
`wlc7=0 µm`	Width dependence of `lc7`.

Shrink Parameters

Imax and Imelt

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and Spectre prints a warning.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, the base and collector currents are composed of many exponential terms, Spectre issues a warning and the results become inaccurate. The junction current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

Both of these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

© 2023 Cadence Design Systems, Inc.

Auto Model Selection

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin` should be given. The selection criteria to choose a model is as follows:

```
  lmin <= inst_length < lmax  and   wmin <= inst_width  < wmax
```

Example:

```
model ModelName ModelType {
   1:     <model parameters> lmin=2 lmax=4 wmin=1 wmax=2
   2:     <model parameters> lmin=1 lmax=2 wmin=2 wmax=4
   3:     <model parameters> lmin=2 lmax=4 wmin=4 wmax=6
}
```

Then for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`weff (m)`	Effective channel width.
`leff (m)`	Effective channel length.
`rseff (Ω)`	Effective source resistance.

© 2023 Cadence Design Systems, Inc.

rdeff (Ω)	Effective drain resistance.
aseff (m^2)	Effective area of source diffusion.
adeff (m^2)	Effective area of drain diffusion.
pseff (m)	Effective perimeter of source diffusion.
pdeff (m)	Effective perimeter of source diffusion.
isseff (A)	Effective source-bulk junction reverse saturation current.
isdeff (A)	Effective drain-bulk junction reverse saturation current.
cbseff (F)	Effective zero-bias source-bulk junction capacitance.
cbdeff (F)	Effective zero-bias drain-bulk junction capacitance.

Operating-Point Parameters

type=n	Transistor type. Possible values are n or p.
region=triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are off, triode, sat, subth, or breakdown.
trise (C)	Temperature rise from ambient.
degradation=no	Hot-electron degradation flag. Possible values are no or yes.
reversed	Reverse mode indicator. Possible values are no or yes.
ids (A)	Resistive drain-to-source current.
vgs (V)	Gate-source voltage.
vds (V)	Drain-source voltage.
vbs (V)	Bulk-source voltage.
vth (V)	Threshold voltage.
vdsat (V)	Drain-source saturation voltage.
gm (S)	Common-source transconductance.
gds (S)	Common-source output conductance.

© 2023 Cadence Design Systems, Inc.

`gmbs (S)`	Body-transconductance.
`gameff (√V )`	Effective body effect coefficient.
`betaeff (A/V`^{2}`)`	Effective `beta`.
`cbd (F)`	Drain-bulk junction capacitance.
`cbs (F)`	Source-bulk junction capacitance.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`cgb (F)`	Gate-bulk capacitance.
`ron (Ω)`	On-resistance.
`id (A)`	Resistive drain current.
`ibulk (A)`	Resistive bulk current.
`pwr (W)`	Power at op point.
`gmoverid (1/V)`	`Gm/Ids`.
`isub (A)`	Substrate current.
`stress`	Hot-electron stress.
`age (s)`	Device age.
`he_vdsat (V)`	Hot Electron `Vdsat`.

Related Topics

MOS Level-3 Model (mos3)

BSIM1 Level-4 Model (bsim1)

BSIM2 Level-5 Model (bsim2)

BSIM3v2 Level-10 Model (bsim3)

© 2023 Cadence Design Systems, Inc.

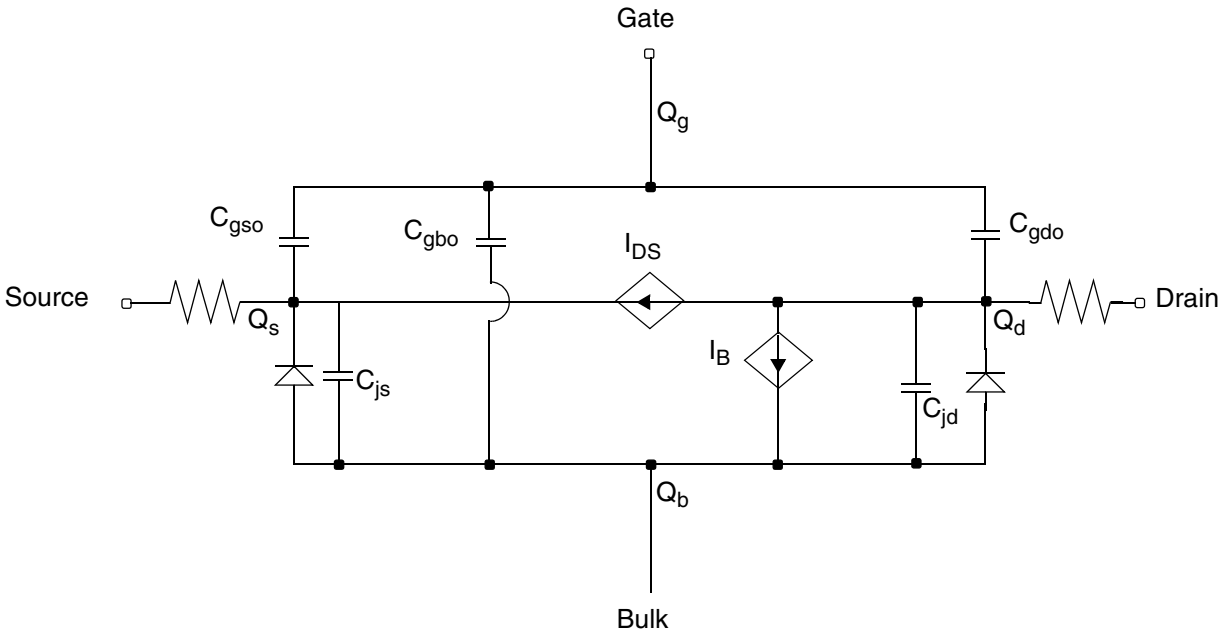
17

MOS Level-3 Model (mos3)

The MOS3 model is the level-3 model from Berkeley SPICE, and is a semi-empirical model. Three charge models are available. Click to view the following links for information about the MOS3 model:

- Channel Width and Length
- Threshold Voltage
- Drain Saturation Voltage
- Drain Current for the Subthreshold Region
- Drain Current for the Triode Region
- Drain Current for the Saturation Region
- Substrate Current
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.



Channel Width and Length

(17-1)

$$W_{scaled} = w*scale + xw*scalem$$

(17-2)

$$W_{eff} = \begin{cases} w*scale + xw*scalem - 2wd*scalem & \text{(Level 1-3)} \\ w*scale + xw*scalem - dw*scalem & \text{(BSIM 1-2)} \end{cases}$$

(17-3)

$$L_{eff} = \begin{cases} l*scale + xl*scalem - 2ld*scalem & \text{(Level 1-3)} \\ l*scale + xl*scalem - dl*scalem & \text{(BSIM 1-2)} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Threshold Voltage

(17-4)

$$V_{TH} = V_{BI} + gamma\ F_S\sqrt{phi - V_{BS}} - \sigma V_{DS} + F_N(phi - V_{BS})$$

where

(17-5)

$$V_{BI} = vto - gamma\sqrt{phi}$$

(17-6)

$$\sigma = \frac{8.15 \times 10^{-22} eta}{C_{ox} L^3_{eff}}$$

(17-7)

$$F_S = 1 - \frac{xj}{L_{eff}}\left\{\left(\frac{ld}{xj} + \frac{W_C}{xj}\right)\sqrt{1 - \left(\frac{W_p}{1 + W_p}\right)^2} - \frac{ld}{xj}\right\}$$

(17-8)

$$W_p = \frac{X_D}{xj}\sqrt{phi - V_{BS}}$$

(17-9)

$$X_D = \sqrt{\frac{2\varepsilon_{si}}{q * nsub}}$$

(17-10)

$$\frac{W_c}{xj} = 0.0631353 + 0.8013292 W_p - 0.01110777 W_p^2$$

© 2023 Cadence Design Systems, Inc.

(17-11)

$$F_N = \frac{delta * \pi * \varepsilon_{si}}{2 C_{ox} W_{eff}}$$

If either xj or $nsub$ is zero, the short-channel effects on threshold voltage are not evaluated; that is, F_S = 1.

Drain Saturation Voltage

If $vmax$ is not input, V_{DSAT} is determined by the pinchoff condition and is given by

(17-12)

$$V_{DSAT} = \frac{V_{GST}}{1 + F_B}$$

where

(17-13)

$$V_{GST} = V_{GS} - V_{TH}$$

(17-14)

$$F_B = \frac{gamma\ F_S}{4\sqrt{phi - V_{BS}}} + F_N$$

If $vmax$ is specified, V_{DSAT} is determined by the velocity saturation effect.

(17-15)

$$V_{DSAT} = \frac{V_{GST}}{1 + F_B} + E_c L_{eff} - \sqrt{\left(\frac{V_{GST}}{1 + F_B}\right)^2 + (E_c L_{eff})^2}$$

where

(17-16)

© 2023 Cadence Design Systems, Inc.

$$E_c = \frac{vmax}{\mu_{eff}}$$

μ_{eff} is the effective mobility that is defined later.

Drain Current for the Subthreshold Region

Note: These equations apply when $V_{GS} \le V_{ON}$.

You cannot use the subthreshold current equations without nfs.

(17-17)

$$V_{ON} = \begin{cases} V_{TH} + nV_t & \text{if } nfs \text{ is specified} \\ V_{TH} & \text{otherwise} \end{cases}$$

where

(17-18)

$$n = 1 + \frac{C_{FS} + C_D}{C_{ox}}$$

(17-19)

$$C_{FS} = q(nfs)$$

(17-20)

$$C_D = \left[\frac{\gamma_s}{2\sqrt{phi - V_{BS}}} - \frac{d\gamma_s}{dV_{BS}} \sqrt{phi - V_{BS}} + F_N \right] C_{ox}$$

(17-21)

$$I_{DS} = I_{DS,ON} e^{(V_{GS} - V_{ON})/nV_t}$$

where $I_{DS,ON}$ is the drain current evaluated at $V_{GS} = V_{ON}$.

© 2023 Cadence Design Systems, Inc.

Drain Current for the Triode Region

Note: These equations apply when $V_{GS} \geq V_{ON}$ and $V_{DS} \leq V_{DSAT}$.

(17-22)

$$I_{DS} = \frac{\beta\left[V_{GS} - V_{TH} - \frac{(1+F_B)}{2}V_{DS}\right]V_{DS}}{1 + \frac{\mu_{eff}V_{DS}}{vmax\ L_{eff}}} \quad \backslash$$

where

(17-23)

$$\beta = \frac{\mu_{eff}C_{ox}W_{eff}}{L_{eff}} \quad \backslash$$

(17-24)

$$\mu_{eff} = \frac{uo}{1 + theta(V_{GS} - V_{TH})}$$

Drain Current for the Saturation Region

Note: These equations apply when $V_{GS} \geq V_{ON}$ and $V_{DS} \geq V_{DSAT}$.

(17-25)

$$I_{DS} = \frac{\beta\left[V_{GS} - V_{TH} - \frac{(1+F_B)}{2}V_{DSAT}\right]V_{DSAT}}{1 + \frac{\mu_{eff}V_{DSAT}}{vmax\ L_{eff}}}$$

where

(17-26)

© 2023 Cadence Design Systems, Inc.

$$\beta = \frac{\mu_{eff} C_{ox} W_{eff}}{L_{eff} - \Delta L}$$

(17-27)

$$\Delta L = \begin{cases} \sqrt{kappa\ X_D^2 (V_{DS} - V_{DSAT})} & \text{if } vmax \text{ is not specified} \\ \sqrt{E_x^2 + kappa\ X_D^2 (V_{DS} - V_{DSAT})} - E_x & \text{otherwise} \end{cases}$$

If ΔL Š L_{eff}/2, a new value of ΔL(ΔL_{new}) is calculated to avoid device punchthrough.

(17-28)

$$\Delta L_{new} = L_{eff} - \frac{L_{eff}^2}{4\Delta L}$$

Substrate Current

The substrate current results from impact ionization in the velocity saturation region near the drain. This impact-ionization induced current (I_{DB}) flows between the drain and the substrate. You need both aio and bio to use the impact-ionization model.

(17-29)

$$I_{DB} = \begin{cases} I_{DS} A_i (V_{DS} - V_{DSAT}) e^{-B_i/(V_{DS} - V_{DSAT})} & \text{if } V_{DS} \le V_{DSAT} \\ 0 & \text{otherwise} \end{cases}$$

where

(17-30)

$$A_i = aio + \frac{laio \times 10^{-6}}{L_{eff}} + \frac{waio \times 10^{-6}}{W_{eff}}$$

(17-31)

© 2023 Cadence Design Systems, Inc.

$$B_i = bio + \frac{lbio \times 10^{-6}}{L_{eff}} + \frac{wbio \times 10^{-6}}{W_{eff}}$$

Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem).

Component Statements

This device is supported within altergroups.

Sample Instance Statement:

```
mp3 (0 1 2 2) pchmos3 l=2u w=30u ad=120p as=75p pd=36u ps=6u
```

Sample Model Statement:

```
model pchmos3 mos3 type=p vto=-0.83 gamma=0.4511 kappa=5 ld=0.45e-6 kp=0.334e-4
tox=0.3e-7 nsub=0.2e17 capmod=yang vmax=4.5e5 theta=0.25 cbs=10e-15 cbd=10e-15
```

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

w (m)	Channel width.
l (m)	Channel length.
as (m^2)	Area of source diffusion.
ad (m^2)	Area of drain diffusion.
ps (m)	Perimeter of source diffusion.
pd (m)	Perimeter of drain diffusion.
nrd (m/m)	Number of squares of drain diffusion.
nrs (m/m)	Number of squares of source diffusion.
ld (m)	Length of drain diffusion region.
ls (m)	Length of source diffusion region.
m=1	Multiplicity factor (number of MOSFETs in parallel).
region=triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are off, triode, sat, subth, or breakdown.
trise	Temperature rise from ambient.
isnoisy=yes	Should resistor generate noise. Possible values are no or yes.
degradation=no	Hot-electron degradation flag. Possible values are no or yes.

Model Syntax

```
model modelName mos3 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

Drain current model parameters

`vto=0 V`	Threshold voltage at zero body bias.
`kp=2.0718e-5 A/V`^{2}	Transconductance parameter.
`theta=0 1/V`	Mobility modulation coefficient.
`phi=0.7 V`	Surface potential at strong inversion.
`gamma=0` $\sqrt{V}$	Body-effect parameter.
`uo=600 cm`^{2}`/V s`	Carrier surface mobility.
`vmax=`∞ `m/s`	Carrier saturation velocity.
`eta=0 1/V`	Static feedback coefficient.
`kappa=0.2`	Saturation field factor.
`delta=0`	Width effect on threshold voltage.

Process parameters

`nsub=1.13e16 cm`$^{-3}$	Channel doping concentration.
`nss=0 cm`$^{-2}$	Surface state density.
`nfs=0 cm`$^{-2}$	Fast surface state density.
`tpg=+1`	Type of gate (+1 = opposite of substrate, -1 = same as substrate, 0 = aluminum).
`tox=1e-7 m`	Gate oxide thickness.
`ld=0 m`	Lateral diffusion.
`wd=0 m`	Field-oxide encroachment.

© 2023 Cadence Design Systems, Inc.

`xw=0 m`	Width variation due to masking and etching.
`xl=0 m`	Length variation due to masking and etching.
`xj=0 m`	Source/drain junction depth.

© 2023 Cadence Design Systems, Inc.

Impact ionization parameters

`ai0=0 1/V`	Impact ionization current coefficient.
`lai0=0 µm/V`	Length sensitivity of `ai0`.
`wai0=0 µm/V`	Width sensitivity of `ai0`.
`bi0=0 V`	Impact ionization current exponent.
`lbi0=0 µm V`	Length sensitivity of `bi0`.
`wbi0=0 µm V`	Width sensitivity of `bi0`.

Overlap capacitance parameters

`cgso=0 F/m`	Gate-source overlap capacitance.
`cgdo=0 F/m`	Gate-drain overlap capacitance.
`cgbo=0 F/m`	Gate-bulk overlap capacitance.
`meto=0 m`	Metal overlap in fringing field.

Charge model selection parameters

`capmod=bsim`	Intrinsic charge model. Possible values are `none`, `meyer`, `yang`, or `bsim`.
`xpart=1`	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
`xqc=0`	Drain/source channel charge partition in saturation for charge models, for example, use 0.4 for 40/60, 0.5 for 50/50, 0 for 0/100.

Parasitic resistance parameters

`rs=0 Ω`	Source resistance.
`rd=0 Ω`	Drain resistance.
`rsh=0 Ω/sqr`	Source/drain diffusion sheet resistance.
`rss=0 Ω m`	Scalable source resistance.

© 2023 Cadence Design Systems, Inc.

`rdd=0 Ω m`	Scalable drain resistance.
`rsc=0 Ω`	Source contact resistance.
`rdc=0 Ω`	Drain contact resistance.
`minr=0.1 Ω`	Minimum source/drain resistance.
`ldif=0 m`	Lateral diffusion beyond the gate.
`hdif=0 m`	Length of heavily doped diffusion.
`lgcs=0 m`	Gate-to-contact length of source side.
`lgcd=0 m`	Gate-to-contact length of drain side.
`sc=∞ m`	Spacing between contacts.

© 2023 Cadence Design Systems, Inc.

Junction diode model parameters

`js (A/m^2)`	Bulk junction reverse saturation current density.
`is=1e-14 A`	Bulk junction reverse saturation current.
`n=1`	Junction emission coefficient.
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`. Possible values are `no` or `yes`.
`imelt=`imax' A`	Explosion current, diode is linearized beyond this current to aid convergence.
`jmelt=`jmax' A/m'^2`	Explosion current density, diode is linearized beyond this current to aid convergence.

Junction capacitance model parameters

`cbs=0 F`	Bulk-source zero-bias junction capacitance.
`cbd=0 F`	Bulk-drain zero-bias junction capacitance.
`cj=0 F/m^2`	Zero-bias junction bottom capacitance density.
`mj=1/2`	Bulk junction bottom grading coefficient.
`pb=0.8 V`	Bulk junction built-in potential.
`fc=0.5`	Forward-bias depletion capacitance threshold.
`cjsw=0 F/m`	Zero-bias junction sidewall capacitance density.
`mjsw=1/3`	Bulk junction sidewall grading coefficient.
`pbsw=0.8 V`	Side-wall junction built-in potential.
`fcsw=0.5`	Side-wall forward-bias depletion capacitance threshold.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, or `rev`.

© 2023 Cadence Design Systems, Inc.

`imax=1 A`	Maximum current, currents above this limit generate a warning.
`jmax=1e8 A/m`^{2}	Maximum current density, currents above this limit generate a warning.
`bvj=∞ V`	Junction reverse breakdown voltage.
`vbox=1e9 tox V`	Oxide breakdown voltage.

© 2023 Cadence Design Systems, Inc.

Temperature effects parameters

`tnom (C)`	Parameters measurement temperature. Default set by `options`.
`trise=0 C`	Temperature rise from ambient.
`uto=0 C`	Mobility temperature offset.
`ute=-1.5`	Mobility temperature exponent.
`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eg=1.12452 V`	Energy band gap.
`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.
`f1ex=0`	Temperature exponent for `ucrit`.
`lamex=0 1/C`	Temperature parameter for `lambda` and `kappa`.
`trs=0 1/C`	Temperature parameter for source resistance.
`trd=0 1/C`	Temperature parameter for drain resistance.
`xti=3`	Saturation current temperature exponent.
`ptc=0 V/C`	Surface potential temperature coefficient.
`tcv=0 V/C`	Threshold voltage temperature coefficient.
`pta=0 V/C`	Junction potential temperature coefficient.
`ptp=0 V/C`	Sidewall junction potential temperature coefficient.
`cta=0 1/C`	Junction capacitance temperature coefficient.
`ctp=0 1/C`	Sidewall junction capacitance temperature coefficient.

Default instance parameters

`w=3e-6 m`	Default channel width.
`l=3e-6 m`	Default channel length.
`as=0` m^2	Default area of source diffusion.
`ad=0` m^2	Default area of drain diffusion.

© 2023 Cadence Design Systems, Inc.

`ps=0 m`	Default perimeter of source diffusion.
`pd=0 m`	Default perimeter of drain diffusion.
`nrd=0 m/m`	Default number of squares of drain diffusion.
`nrs=0 m/m`	Default number of squares of source diffusion.
`ldd=0 m`	Default length of drain diffusion region.
`lds=0 m`	Default length of source diffusion region.

© 2023 Cadence Design Systems, Inc.

Noise model parameters

`noisemod=1`	Noise model selector.
`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`ef=1`	Flicker (1/f) noise frequency exponent.
`wnoi=1e-5 m`	Channel width at which noise parameters were extracted.

Auto Model Selector parameters

`wmax=1.0 m`	Maximum channel width for which the model is valid.
`wmin=0.0 m`	Minimum channel width for which the model is valid.
`lmax=1.0 m`	Maximum channel length for which the model is valid.
`lmin=0.0 m`	Minimum channel length for which the model is valid.

Degradation parameters

`degramod=spectre`	Degradation model selector. Possible values are `spectre` or `bert`.
`degradation=no`	Hot-electron degradation flag. Possible values are `no` or `yes`.
`dvthc=1 V`	Degradation coefficient for threshold voltage.
`dvthe=1`	Degradation exponent for threshold voltage.
`duoc=1 S`	Degradation coefficient for transconductance.
`duoe=1`	Degradation exponent for transconductance.
`crivth=0.1 V`	Maximum allowable threshold voltage shift.
`criuo=10%`	Maximum allowable normalized mobility change.
`crigm=10%`	Maximum allowable normalized transconductance change.

© 2023 Cadence Design Systems, Inc.

`criids=10%`	Maximum allowable normalized drain current change.
`wnom=5e-6 m`	Nominal device width in degradation calculation.
`lnom=1e-6 m`	Nominal device length in degradation calculation.
`vbsn=0 V`	Substrate voltage in degradation calculation.
`vdsni=0.1 V`	Drain voltage in `Ids` degradation calculation.
`vgsni=5 V`	Gate voltage in `Ids` degradation calculation.
`vdsng=0.1 V`	Drain voltage in `Gm` degradation calculation.
`vgsng=5 V`	Gate voltage in `Gm` degradation calculation.

© 2023 Cadence Design Systems, Inc.

Spectre stress parameters

`esat=1.1e7 V/m`	Critical field in Vdsat calculation.
`esatg=2.5e6 1/m`	Gate voltage dependence of `esat`.
`vpg=-0.25`	Gate voltage modifier.
`vpb=-0.13`	Gate voltage modifier.
`subc1=2.24e-5`	Substrate current coefficient.
`subc2=-0.1e-5 1/V`	Substrate current coefficient.
`sube=6.4`	Substrate current exponent.
`strc=1`	Stress coefficient.
`stre=1`	Stress exponent.

BERT stress parameters

`h0=1`	Aging coefficient.
`hgd=0 1/V`	Bias dependence of `h0`.
`m0=1`	Aging exponent.
`mgd=0 1/V`	Bias dependence of `m0`.
`ecrit0=1.1e5 V/cm`	Critical electric field.
`lecrit0=0 µm V/cm`	Length dependence of `ecrit0`.
`wecrit0=0 µm V/cm`	Width dependence of `ecrit0`.
`ecritg=0 1/cm`	Gate voltage dependence of `ecrit0`.
`lecritg=0 µm/cm`	Length dependence of `ecritg`.
`wecritg=0 µm/cm`	Width dependence of `ecritg`.
`ecritb=0 1/cm`	Substrate voltage dependence of `ecrit0`.
`lecritb=0 µm/cm`	Length dependence of `ecritb`.
`wecritb=0 µm/cm`	Width dependence of `ecritb`.
`lc0=1`	Substrate current coefficient.
`llc0=0 µm`	Length dependence of `lc0`.
`wlc0=0 µm`	Width dependence of `lc0`.

© 2023 Cadence Design Systems, Inc.

`lc1=1`	Substrate current coefficient.
`llc1=0 µm`	Length dependence of `lc1`.
`wlc1=0 µm`	Width dependence of `lc1`.
`lc2=1`	Substrate current coefficient.
`llc2=0 µm`	Length dependence of `lc2`.
`wlc2=0 µm`	Width dependence of `lc2`.
`lc3=1`	Substrate current coefficient.
`llc3=0 µm`	Length dependence of `lc3`.
`wlc3=0 µm`	Width dependence of `lc3`.
`lc4=1`	Substrate current coefficient.
`llc4=0 µm`	Length dependence of `lc4`.
`wlc4=0 µm`	Width dependence of `lc4`.
`lc5=1`	Substrate current coefficient.
`llc5=0 µm`	Length dependence of `lc5`.
`wlc5=0 µm`	Width dependence of `lc5`.
`lc6=1`	Substrate current coefficient.
`llc6=0 µm`	Length dependence of `lc6`.
`wlc6=0 µm`	Width dependence of `lc6`.
`lc7=1`	Substrate current coefficient.
`llc7=0 µm`	Length dependence of `lc7`.
`wlc7=0 µm`	Width dependence of `lc7`.

Shrink Parameters

Imax and Imelt

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and Spectre prints a warning.

© 2023 Cadence Design Systems, Inc.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, the base and collector currents are composed of many exponential terms, Spectre issues a warning and the results become inaccurate. The junction current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

Both of these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

Auto Model Selection

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin` should be given. The selection criteria to choose a model is as follows:

```
  lmin <= inst_length < lmax  and   wmin <= inst_width  < wmax
```

Example:

```
model ModelName ModelType {
   1:     <model parameters> lmin=2 lmax=4 wmin=1 wmax=2
   2:     <model parameters> lmin=1 lmax=2 wmin=2 wmax=4
   3:     <model parameters> lmin=2 lmax=4 wmin=4 wmax=6
}
```

Then for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`weff (m)`	Effective channel width.
`leff (m)`	Effective channel length.
`rseff (Ω)`	Effective source resistance.
`rdeff (Ω)`	Effective drain resistance.
`aseff ($m^2$)`	Effective area of source diffusion.
`adeff ($m^2$)`	Effective area of drain diffusion.
`pseff (m)`	Effective perimeter of source diffusion.
`pdeff (m)`	Effective perimeter of source diffusion.
`isseff (A)`	Effective source-bulk junction reverse saturation current.
`isdeff (A)`	Effective drain-bulk junction reverse saturation current.
`cbseff (F)`	Effective zero-bias source-bulk junction capacitance.
`cbdeff (F)`	Effective zero-bias drain-bulk junction capacitance.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.
`region=triode`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, or `breakdown`.
`trise (C)`	Temperature rise from ambient.
`degradation=no`	Hot-electron degradation flag. Possible values are `no` or `yes`.
`reversed`	Reverse mode indicator. Possible values are `no` or `yes`.
`ids (A)`	Resistive drain-to-source current.
`vgs (V)`	Gate-source voltage.

© 2023 Cadence Design Systems, Inc.

`vds (V)`	Drain-source voltage.
`vbs (V)`	Bulk-source voltage.
`vth (V)`	Threshold voltage.
`vdsat (V)`	Drain-source saturation voltage.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`gmbs (S)`	Body-transconductance.
`gameff` ($\sqrt{V}$)	Effective body effect coefficient.
`betaeff` (A/V^2)	Effective `beta`.
`cbd (F)`	Drain-bulk junction capacitance.
`cbs (F)`	Source-bulk junction capacitance.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`cgb (F)`	Gate-bulk capacitance.
`ron` (Ω)	On-resistance.
`id (A)`	Resistive drain current.
`ibulk (A)`	Resistive bulk current.
`pwr (W)`	Power at op point.
`gmoverid (1/V)`	`Gm/Ids`.
`isub (A)`	Substrate current.
`stress`	Hot-electron stress.
`age (s)`	Device age.
`he_vdsat (V)`	Hot Electron `Vdsat`.

Related Topics

MOS Level-2 Model (mos2)

BSIM1 Level-4 Model (bsim1)

BSIM2 Level-5 Model (bsim2)

© 2023 Cadence Design Systems, Inc.

BSIM3v2 Level-10 Model (bsim3)

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

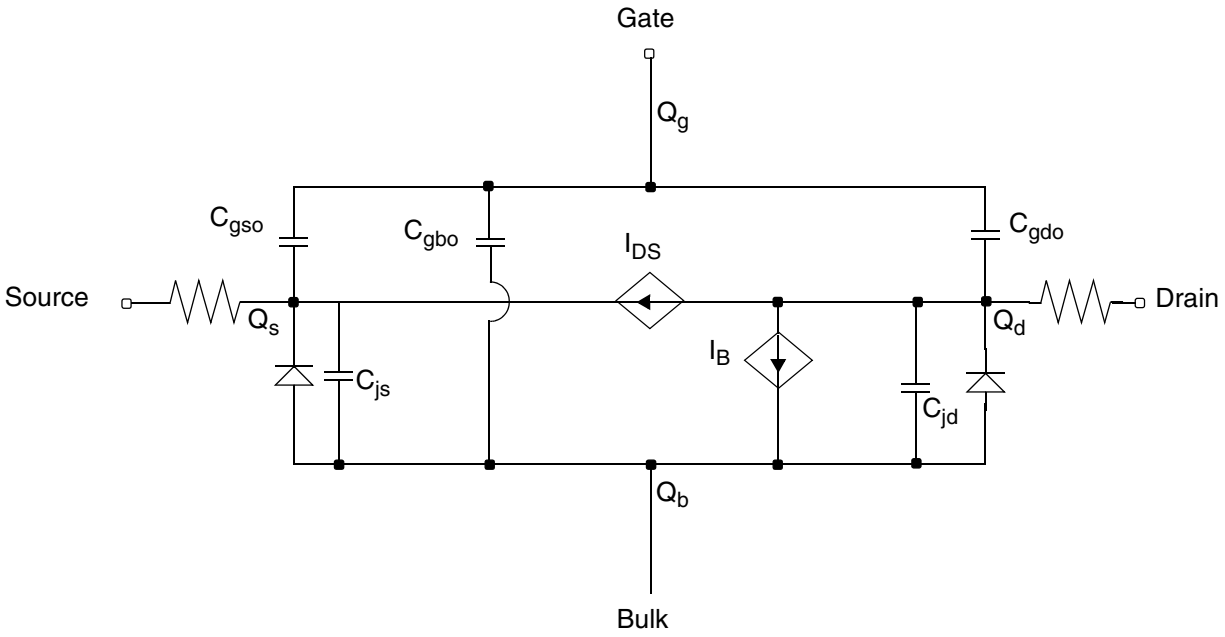
18

BSIM1 Level-4 Model (bsim1)

The BSIM1 model is based on the industry standard efforts of the Compact Modeling Counsel (CMC) and the BSIM modeling group at the University of California, Berkeley. Click to view the following links for information about the BSIM1 model:

- Parameter Calculation
- Drain Current Model
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.



BSIM1 stands for Berkeley Short-Channel IGFET Model version-1. The BSIM1 model is a semiempirical model suitable for devices with channel length from long channel to about 0.8 µm. This model extracts all model parameters directly from physical devices. You can obtain an automated parameter extraction program, based on the HP9836 and HP4145 systems, from the ILP office, Department of EECS, University of California, Berkeley. The following table shows the correspondence between the input parameter names and the equation symbols for the BSIM1 model.

Parameter	Symbol	Parameter	Symbol	Parameter	Symbol
vfb	$V_{FB,0}$	lvfb	$V_{FB,L}$	wvfb	$V_{FB,W}$
phi	ϕ_0	lphi	ϕ_L	wphi	ϕ_W
k1	K_1	lk1	$K_{1,L}$	wk1	$K_{1,W}$
k2	K_2	lk2	$K_{2,L}$	wk2	$K_{2,W}$
eta	η_0	leta	η_L	weta	η_W
muz	μ_0	dl	dl	dw	dw
u0	$U_{0,0}$	lu0	$U_{0,L}$	wu0	$U_{0,W}$
u1	$U_{1,0}$	lu1	$U_{1,L}$	wu1	$U_{1,W}$

© 2023 Cadence Design Systems, Inc.

Parameter	Symbol	Parameter	Symbol	Parameter	Symbol
x2mz	$\mu_{0B,0}$	lx2mz	$\mu_{0B,L}$	wx2mz	$\mu_{0B,W}$
x2e	$\eta_{B,0}$	lx2e	$\eta_{B,L}$	wx2e	$\eta_{B,W}$
x3e	$\eta_{D,0}$	lx3e	$\eta_{D,L}$	wx3e	$\eta_{D,W}$
x2u0	$U_{0B,0}$	lx2u0	$U_{0B,L}$	wx2u0	$U_{0B,W}$
x2u1	$U_{1B,0}$	lx2u1	$U_{1B,L}$	wx2u1	$U_{1,B,W}$
mus	μ_s	lmus	$\mu_{s,L}$	wmus	$\mu_{s,W}$
x2ms	$\mu_{sB,0}$	lx2ms	$\mu_{sB,L}$	wx2ms	$\mu_{sB,W}$
x3ms	$\mu_{sD,0}$	lx3ms	$\mu_{sD,L}$	wx3ms	$\mu_{sD,W}$
x3u1	$U_{1D,0}$	lx3u1	$U_{1D,L}$	wx3u1	$U_{1D,W}$
n0	$N_{0,0}$	ln0	$N_{0,L}$	wn0	$N_{0,W}$
nb	$N_{B,0}$	lnb	$N_{B,L}$	wnb	$N_{B,W}$
nd	$N_{D,0}$	lnd	$N_{D,L}$	wnd	$N_{D,W}$
aio	Ai_0	laio	$Ai_{0,L}$	waio	$Ai_{0,W}$
bio	Bi_0	lbio	$Bi_{0,L}$	wbio	$Bi_{0,W}$
vdd	V_{DD}				

Parameter Calculation

Except for muz, dl, and dw, all device parameters are calculated from the following equation:

(18-1)

$$P_i = P_{i,0} + \frac{P_{i,L}}{L_{eff}} + \frac{P_{i,W}}{W_{eff}}$$

where P_i is any device parameter, $P_{i,0}$ is the parameter value for long channel length and width, and $P_{i,L}$ and $P_{i,W}$ are the channel length and width dependencies of the parameter, respectively. The following example shows how the flat-band voltage for a device with $l = 2$ µm and $w = 5$ µm is calculated from the model parameters:

(18-2)

© 2023 Cadence Design Systems, Inc.

$$V_{FB} = V_{FB,0} + \frac{V_{FB,L}}{2 - dl} + \frac{V_{FB,W}}{5 - dw}$$

Drain Current Model

Channel Width and Length

(18-3)

$$W_{scaled} = w*scale + xw*scalem$$

(18-4)

$$W_{eff} = \begin{cases} w*scale + xw*scalem - 2wd*scalem & \text{(Level 1-3)} \\ w*scale + xw*scalem - dw*scalem & \text{(BSIM 1-2)} \end{cases}$$

(18-5)

$$L_{eff} = \begin{cases} l*scale + xl*scalem - 2ld*scalem & \text{(Level 1-3)} \\ l*scale + xl*scalem - dl*scalem & \text{(BSIM 1-2)} \end{cases}$$

Threshold Voltage

(18-6)

$$V_{TH} = V_{FB} + \phi + K_1\sqrt{\phi - V_{BS}} - K_2(\phi - V_{BS}) - \eta V_{DS}$$

where

(18-7)

$$\eta = \eta_0 + \eta_B V_{BS} + \eta_D(V_{DS} - V_{DD})$$

Drain Saturation Voltage

(18-8)

© 2023 Cadence Design Systems, Inc.

$$V_{DSAT} = \frac{V_{GS} - V_{TH}}{a\sqrt{K}}$$

where

(18-9)

$$a = 1 + \frac{gK_1}{2\sqrt{\phi - V_{BS}}}$$

(18-10)

$$g = 1 - \frac{1}{1.744 + 0.8364(\phi - V_{BS})}$$

(18-11)

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2}$$

(18-12)

$$V_c = \frac{U_{1S}(V_{GS} - V_{TH})}{a}$$

Drain Current for the Subthreshold Region

Note: These equations apply when $V_{GS} \leq V_{TH}$.

If you specify that N_0 is less than 10, the subthreshold current is calculated and added to the drain current.

(18-13)

$$I_{subth} = \frac{I_{EXP}\, I_{LIMIT}}{I_{EXP} + I_{LIMIT}}$$

where

© 2023 Cadence Design Systems, Inc.

(18-14)

$$I_{EXP} = \beta_0 V_t^2 \, e^{1.8 + (V_{GS} - V_{TH})/nV_t}(1 - e^{-V_{DS}/V_t})$$

(18-15)

$$I_{LIMIT} = 4.5\beta_0 V_t^2$$

(18-16)

$$n = N_0 + N_B V_{BS} + N_D V_{DS}$$

The subthreshold current is added to the drain current.

(18-17)

$$I_{DS,\,tot} = I_{DS} + I_{subth}$$

Drain Current for the Triode Region

Note: These equations apply when $V_{GS} \geq V_{ON}$ and $V_{DS} \leq V_{DSAT}$.

(18-18)

$$I_{DS} = \frac{\beta_0\left(V_{GS} - V_{TH} - \frac{a}{2}V_{DS}\right)V_{DS}}{(1 + U_{1S}V_{DS})[1 + \theta(V_{GS} - V_{TH})]}$$

where

(18-19)

$$\theta = U_0 + U_{0B}V_{BS}$$

(18-20)

$$U_{1S} = \frac{U_1 + U_{1B}V_{BS} + U_{1D}(V_{DS} - V_{DD})}{L_{eff}}$$

© 2023 Cadence Design Systems, Inc.

(18-21)

$$\beta_0 = \beta_1\left(\frac{V_{DS}}{V_{DD}} - 1\right)^2 + \beta_2\left(2 - \frac{V_{DS}}{V_{DD}}\right)\frac{V_{DS}}{V_{DD}} + \beta_{sD}V_{DS}\left(\frac{V_{DS}}{V_{DD}} - 1\right)$$

(18-22)

$$\beta_1 = \frac{C_{ox}W_{eff}}{L_{eff}}(\mu_0 + \mu_{0B}V_{BS})$$

(18-23)

$$\beta_2 = \frac{C_{ox}W_{eff}}{L_{eff}}(\mu_s + \mu_{sB}V_{BS})$$

(18-24)

$$\beta_{sD} = \frac{C_{ox}W_{eff}}{L_{eff}}\mu_{sD}$$

Drain Current for the Saturation Region

Note: This equation applies when $V_{GS} \geq V_{ON}$ and $V_{DS} \geq V_{DSAT}$.

(18-25)

$$I_{DS} = \frac{\beta(V_{GS} - V_{TH})^2}{2aK}$$

Substrate Current

The substrate current results from impact ionization in the velocity saturation region near the drain. This impact-ionization induced current (I_{DB}) flows between the drain and the substrate. You need both A_i and B_i to use the impact-ionization model.

(18-26)

© 2023 Cadence Design Systems, Inc.

$$I_{DB} = \begin{cases} I_{DS} A_i (V_{DS} - V_{DSAT}) e^{-B_i/(V_{DS} - V_{DSAT})} & \text{if} \quad V_{DS} \le V_{DSAT} \\ 0 & \text{otherwise} \end{cases}$$

where

(18-27)

$$A_i = A_{io} + \frac{A_{io,L} \times 10^{-6}}{L_{eff}} + \frac{A_{io,W} \times 10^{-6}}{W_{eff}}$$

(18-28)

$$B_i = B_{io} + \frac{B_{io,L} \times 10^{-6}}{L_{eff}} + \frac{B_{io,W} \times 10^{-6}}{W_{eff}}$$

Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem).

Component Statements

This device is supported within altergroups.

Sample Instance Statement

```
m1 (1 2 0 0) nchmod l=5u w=10u as=40u ad=40u pd=28u ps=28u m=1
```

Sample Model Statement

```
model nchmod bsim1 vfb0=-0.5 lvfb=0.5 wvfb=0.3 phi0=0.8 eta0=0.056 k1=0.5 muz=454
eg=0.99 gap1=5.5e-04 trs=1e-3 trd=1e-3 xpart=0.5 rs=10 rd=10
```

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

w	(m)	Channel width.
l	(m)	Channel length.
as	(m^2)	Area of source diffusion.
ad	(m^2)	Area of drain diffusion.
ps	(m)	Perimeter of source diffusion.
pd	(m)	Perimeter of drain diffusion.
nrd	(m/m)	Number of squares of drain diffusion.
nrs	(m/m)	Number of squares of source diffusion.
ld	(m)	Drain diffusion length.
ls	(m)	Source diffusion length.
m	1	Multiplicity factor (number of MOSFETs in parallel).
region	triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile.Possible values are off, triode, sat, subth and breakdown.
trise	(C)	Temperature rise from ambient.
degradation	no	Hot-electron degradation flag.Possible values are no and yes.
isnoisy	yes	Should device generate noise.Possible values are no and yes.

Model Syntax

```
model modelName bsim1 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

type	n	Transistor type.Possible values are n and p.

Threshold voltage parameters

vfb0	-0.8 V	Flat-band voltage.
lvfb	0 V µm	Length dependence of vfb.
wvfb	0 V µm	Width dependence of vfb.
pvfb	0 V µm	Width-length dependence of vfb.
phi0	0.75 V	Surface potential.
lphi	0 V µm	Length dependence of phi.
wphi	0 V µm	Width dependence of phi.
pphi	0 V µm	Width-length dependence of phi.
k1	0.7 √V	Body-effect coefficient.
lk1	0 √V µm	Length dependence of k1.
wk1	0 √V µm	Width dependence of k1.
pk1	0 √V µm	Width-length dependence of k1.
k2	0	Charge-sharing parameter.
lk2	0 µm	Length dependence of k2.

© 2023 Cadence Design Systems, Inc.

wk2	0 µm	Width dependence of k2.
pk2	0 µm	Width-length dependence of k2.
eta0	0	Drain-induced barrier-lowering coefficient.
leta	0 µm	Length dependence of eta.
weta	0 µm	Width dependence of eta.
peta	0 µm	Width-length dependence of eta.
x2e	0 1/V	Body-bias dependence of eta.
lx2e	0 µm/V	Length dependence of x2e.
wx2e	0 µm/V	Width dependence of x2e.
px2e	0 µm/V	Width-length dependence of x2e.
x3e	0 1/V	Drain-bias dependence of eta.
lx3e	0 µm/V	Length dependence of x3e.
wx3e	0 µm/V	Width dependence of x3e.
px3e	0 µm/V	Width-length dependence of x3e.

© 2023 Cadence Design Systems, Inc.

Mobility parameters

muz	400 $cm^2/V\ s$	Low-field mobility.
lmuz	0 $cm^2/V\ s$	Length dependence of 'muz'.
wmuz	0 $cm^2/V\ s$	Width dependence of 'muz'.
pmuz	0 $cm^2/V\ s$	Width-length dependence of 'muz'.
x2mz	0 $cm^2/V^2\ s$	Body-bias dependence of muz.
lx2mz	0 $cm^2\ \mu m/V^2\ s$	Length dependence of x2mz.
wx2mz	0 $cm^2\ \mu m/V^2\ s$	Width dependence of x2mz.
px2mz	0 $cm^2\ \mu m/V^2\ s$	Width-length dependence of x2mz.
mus	450 $cm^2/V\ s$	Mobility in the saturation region.
lmus	0 $cm^2\ \mu m/V\ s$	Length dependence of mus.
wmus	0 $cm^2\ \mu m/V\ s$	Width dependence of mus.
pmus	0 $cm^2\ \mu m/V\ s$	Width-length dependence of mus.
x2ms	0 $cm^2/V^2\ s$	Body-bias dependence of mus.

© 2023 Cadence Design Systems, Inc.

lx2ms	0 cm^2 $\mu m/V^2$ s	Length dependence of x2ms.
wx2ms	0 cm^2 $\mu m/V^2$ s	Width dependence of x2ms.
px2ms	0 cm^2 $\mu m/V^2$ s	Width-length dependence of x2ms.
x3ms	0 cm^2/V^2 s	Drain-bias dependence of mus.
lx3ms	0 cm^2 $\mu m/V^2$ s	Length dependence of x3ms.
wx3ms	0 cm^2 $\mu m/V^2$ s	Width dependence of x3ms.
px3ms	0 cm^2 $\mu m/V^2$ s	Width-length dependence of x3ms.

© 2023 Cadence Design Systems, Inc.

Mobility modulation parameters

u00	0 1/V	Gate voltage dependence of mobility.
lu0	0 µm/V	Length dependence of u0.
wu0	0 µm/V	Width dependence of u0.
pu0	0 µm/V	Width-length dependence of u0.
x2u0	0 $1/V^2$	Body-bias dependence of u0.
lx2u0	0 $\mu m/V^2$	Length dependence of x2u0.
wx2u0	0 $\mu m/V^2$	Width dependence of x2u0.
px2u0	0 $\mu m/V^2$	Width-length dependence of x2u0.

Velocity saturation parameters

u10	0 1/V	Velocity saturation coefficient.
lu1	0 µm/V	Length dependence of u1.
wu1	0 µm/V	Width dependence of u1.
pu1	0 µm/V	Width-length dependence of u1.
x2u1	0 $1/V^2$	Body-bias dependence of u1.
lx2u1	0 $\mu m/V^2$	Length dependence of x2u1.
wx2u1	0 $\mu m/V^2$	Width dependence of x2u1.
px2u1	0 $\mu m/V^2$	Width-length dependence of x2u1.
x3u1	0 $1/V^2$	Drain-bias dependence of u1.

© 2023 Cadence Design Systems, Inc.

`lx3u1`	0 $\mu m/V^2$	Length dependence of `x3u1`.
`wx3u1`	0 $\mu m/V^2$	Width dependence of `x3u1`.
`px3u1`	0 $\mu m/V^2$	Width-length dependence of `x3u1`.

© 2023 Cadence Design Systems, Inc.

Subthreshold parameters

n0	0	Subthreshold swing parameter.
ln0	0 µm	Length dependence of subthreshold swing parameter.
wn0	0 µm	Width dependence of subthreshold swing parameter.
pn0	0 µm	Width-length dependence of subthreshold swing parameter.
nb	0 V	Body-bias dependence of n0.
lnb	0 V µm	Length dependence of nb.
wnb	0 V µm	Width dependence of nb.
pnb	0 V µm	Width-length dependence of nb.
nd	0 1/V	Drain-bias dependence of n0.
lnd	0 µm/V	Length dependence of nd.
wnd	0 µm/V	Width dependence of nd.
pnd	0 µm/V	Width-length dependence of nd.
subthmod	2	Subthreshold model selector.

Impact ionization parameters

ai0	0 1/V	Hot-electron effect on Rout parameter.
lai0	0 µm/V	Length dependence of ai0.

© 2023 Cadence Design Systems, Inc.

wai0	0 µm/V	Width dependence of ai0.
pai0	0 µm/V	Width-length dependence of ai0.
bi0	0 V	Hot-electron effect on Rout exponent.
lbi0	0 V µm	Length dependence of bi0.
wbi0	0 V µm	Width dependence of bi0.
pbi0	0 V µm	Width-length dependence of bi0.

© 2023 Cadence Design Systems, Inc.

Length and width modulation parameters

dl0	0 µm	Lateral diffusion.
dw0	0 µm	Field oxide encroachment.
lref	infinity m	Reference channel length.
wref	infinity m	Reference channel width.
xw	0 m	Width variation due to masking and etching.
xl	0 m	Length variation due to masking and etching.

Temperature effects parameters

temp	(C)	Parameters measurement temperature. Default set by options.
trise	0 C	Temperature rise from ambient.
compatible	spectre	Encourage device equations to be compatible with a foreign simulator.This option does not affect the input synax.Possible values are spectre, spice2, spice3, cdsspice, hspice, spiceplus, eldo, sspice, mica, tispice and pspice.
tempmod	432	Temperature model selector.
version	432	Version selector.
uto	0 C	Mobility temperature offset.
ute	-1.5	Mobility temperature exponent.

© 2023 Cadence Design Systems, Inc.

tlev	0	DC temperature selector.
tlevc	0	AC temperature selector.
eg	1.12452 V	Energy band gap.
gap1	7.02e-4 V/C^2	Band gap temperature coefficient.
gap2	1108 K	Band gap temperature offset.
trs	0 1/C	Temperature coefficient for source resistance.
trd	0 1/C	Temperature coefficient for drain resistance.
xti	3	Saturation current temperature exponent.

© 2023 Cadence Design Systems, Inc.

Overlap capacitance parameters

cgso	0 F/m	Gate-source overlap capacitance.
cgdo	0 F/m	Gate-drain overlap capacitance.
cgbo	0 F/m	Gate-bulk overlap capacitance.
meto	0 m	Metal overlap in fringing field.

Charge model selection parameters

capmod	bsim	Intrinsic charge model.Possible values are none, meyer, yang and bsim.
xpart	1	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
xqc	0	Drain/source channel charge partition in saturation for charge models, e.g. use 0.4 for 40/60, 0.5 for 50/50, or 0 for 0/100.

Parasitic resistance parameters

rs	0 Ω	Source resistance.
rd	0 Ω	Drain resistance.
rsh	0 Ω/sqr	Source/drain diffusion sheet resistance.
rsc	0 Ω	Source contact resistance.
rdc	0 Ω	Drain contact resistance.

© 2023 Cadence Design Systems, Inc.

rss	0 Ω m	Scalable source resistance.
rdd	0 Ω m	Scalable drain resistance.
minr	0.1 Ω	Minimum source/drain resistance.
hdif	0 m	Length of heavily doped diffusion.
ldif	0 m	Lateral diffusion beyond the gate.
lgcs	0 m	Gate-to-contact length of source side.
lgcd	0 m	Gate-to-contact length of drain side.
sc	infinity m	Spacing between contacts.

© 2023 Cadence Design Systems, Inc.

Junction diode parameters

`js`	`(A/m`^{2}`)`	Bulk junction reverse saturation current density.
`is`	`1e-14 A`	Bulk junction reverse saturation current.
`n`	`1`	Junction emission coefficient.
`imelt`	`` `imaxA' ``	Explosion current, diode is linearized beyond this current to aid convergence.
`jmelt`	`` `jmaxA/m'`^{2}	Explosion current density, diode is linearized beyond this current to aid convergence.
`dskip`	`yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`.Possible values are no and yes.

Junction capacitance model parameters

`cbs`	`0 F`	Bulk-source zero-bias junction capacitance.
`cbd`	`0 F`	Bulk-drain zero-bias junction capacitance.
`cj`	`0 F/m`^{2}	Zero-bias junction bottom capacitance density.
`mj`	`1/2`	Bulk junction bottom grading coefficient.
`pb`	`0.8 V`	Bulk junction potential.
`fc`	`0.5`	Forward-bias depletion capacitance threshold.
`cjsw`	`0 F/m`	Zero-bias junction sidewall capacitance density.
`mjsw`	`1/3`	Bulk junction sidewall grading coefficient.
`pbsw`	`0.8 V`	Side-wall junction potential.

© 2023 Cadence Design Systems, Inc.

`fcsw`	`0.5`	Side-wall forward-bias depletion capacitance threshold.

© 2023 Cadence Design Systems, Inc.

Operating region warning control parameters

alarm	none	Forbidden operating region.Possible values are none, off, triode, sat, subth and rev.
imax	1 A	Maximum current, currents above this limit generate a warning.
jmax	1e8 A/m^2	Maximum current density, currents above this limit generate a warning.
bvj	infinity V	Junction reverse breakdown voltage.
vbox	1e9*tox V	Oxide breakdown voltage.

Process and power supply parameters

tox	4e-8 m	Gate oxide thickness.
vdd	5 V	Drain voltage at which parameters are extracted.

Default device parameters

w	3e-6 m	Channel width.
l	3e-6 m	Channel length.
as	0 m^2	Area of source diffusion.
ad	0 m^2	Area of drain diffusion.
ps	0 m	Perimeter of source diffusion.

© 2023 Cadence Design Systems, Inc.

`pd`	`0 m`	Perimeter of drain diffusion.
`nrd`	`0 m/m`	Number of squares of drain diffusion.
`nrs`	`0 m/m`	Number of squares of source diffusion.
`ldd`	`0 m`	Drain diffusion length.
`lds`	`0 m`	Source diffusion length.

© 2023 Cadence Design Systems, Inc.

Noise model parameters

noisemod	1	Noise model selector.
kf	0	Flicker (1/f) noise coefficient.
af	1	Flicker (1/f) noise exponent.
ef	1	Flicker (1/f) noise frequency exponent.
wnoi	1e-5 m	Channel width at which noise parameters were extracted.

Auto Model Selector parameters

wmax	1.0 m	Maximum channel width for which the model is valid.
wmin	0.0 m	Minimum channel width for which the model is valid.
lmax	1.0 m	Maximum channel length for which the model is valid.
lmin	0.0 m	Minimum channel length for which the model is valid.

Degradation parameters

degramod	spectre	Degradation model selector.Possible values are spectre and bert.
degradation	no	Hot-electron degradation flag.Possible values are no and yes.
dvthc	1 V	Degradation coefficient for threshold voltage.

© 2023 Cadence Design Systems, Inc.

dvthe	1	Degradation exponent for threshold voltage.
duoc	1 S	Degradation coefficient for transconductance.
duoe	1	Degradation exponent for transconductance.
crivth	0.1 V	Maximum allowable threshold voltage shift.
criuo	10%	Maximum allowable normalized mobility change.
crigm	10%	Maximum allowable normalized transconductance change.
criids	10%	Maximum allowable normalized drain current change.
wnom	5e-6 m	Nominal device width in degradation calculation.
lnom	1e-6 m	Nominal device length in degradation calculation.
vbsn	0 V	Substrate voltage in degradation calculation.
vdsni	0.1 V	Drain voltage in Ids degradation calculation.
vgsni	5 V	Gate voltage in Ids degradation calculation.
vdsng	0.1 V	Drain voltage in Gm degradation calculation.
vgsng	5 V	Gate voltage in Gm degradation calculation.

© 2023 Cadence Design Systems, Inc.

Spectre stress parameters

esat	1.1e7 V/m	Critical field in Vdsat calculation.
esatg	2.5e6 1/m	Gate voltage dependence of esat.
vpg	-0.25	Gate voltage modifier.
vpb	-0.13	Gate voltage modifier.
subc1	2.24e-5	Substrate current coefficient.
subc2	-0.1e-5 1/V	Substrate current coefficient.
sube	6.4	Substrate current exponent.
strc	1	Stress coefficient.
stre	1	Stress exponent.

BERT stress parameters

h0	1	Aging coefficient.
hgd	0 1/V	Bias dependence of h0.
m0	1	Aging exponent.
mgd	0 1/V	Bias dependence of m0.
ecrit0	1.1e5 V/cm	Critical electric field.

© 2023 Cadence Design Systems, Inc.

lecrit0	0 µm V/cm	Length dependence of ecrit0.
wecrit0	0 µm V/cm	Width dependence of ecrit0.
ecritg	0 1/cm	Gate voltage dependence of ecrit0.
lecritg	0 µm/cm	Length dependence of ecritg.
wecritg	0 µm/cm	Width dependence of ecritg.
ecritb	0 1/cm	Substrate voltage dependence of ecrit0.
lecritb	0 µm/cm	Length dependence of ecritb.
wecritb	0 µm/cm	Width dependence of ecritb.
lc0	1	Substrate current coefficient.
llc0	0 µm	Length dependence of lc0.
wlc0	0 µm	Width dependence of lc0.
lc1	1	Substrate current coefficient.
llc1	0 µm	Length dependence of lc1.
wlc1	0 µm	Width dependence of lc1.
lc2	1	Substrate current coefficient.
llc2	0 µm	Length dependence of lc2.
wlc2	0 µm	Width dependence of lc2.
lc3	1	Substrate current coefficient.

© 2023 Cadence Design Systems, Inc.

`llc3`	0 µm	Length dependence of `lc3`.
`wlc3`	0 µm	Width dependence of `lc3`.
`lc4`	1	Substrate current coefficient.
`llc4`	0 µm	Length dependence of `lc4`.
`wlc4`	0 µm	Width dependence of `lc4`.
`lc5`	1	Substrate current coefficient.
`llc5`	0 µm	Length dependence of `lc5`.
`wlc5`	0 µm	Width dependence of `lc5`.
`lc6`	1	Substrate current coefficient.
`llc6`	0 µm	Length dependence of `lc6`.
`wlc6`	0 µm	Width dependence of `lc6`.
`lc7`	1	Substrate current coefficient.
`llc7`	0 µm	Length dependence of `lc7`.
`wlc7`	0 µm	Width dependence of `lc7`.

Imax and Imelt:

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and Spectre prints a warning.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, the base and collector currents are composed of many exponential terms, Spectre issues a warning and the results become inaccurate. The junction

© 2023 Cadence Design Systems, Inc.

current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

Both of these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

Auto Model Selection:

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin` should be given. The selection criteria to choose a model is as follows:

```
  lmin <= inst_length < lmax  and   wmin <= inst_width  < wmax
```

Example:

```
model ModelName ModelType {
   1:     <model parameters> lmin=2 lmax=4 wmin=1 wmax=2
   2:     <model parameters> lmin=1 lmax=2 wmin=2 wmax=4
   3:     <model parameters> lmin=2 lmax=4 wmin=4 wmax=6
}
```

Then for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

© 2023 Cadence Design Systems, Inc.

Output Parameters

tempeff	(C)	Effective temperature for a single device.
weff	(m)	Effective channel width.
leff	(m)	Effective channel length.
rseff	(Ω)	Effective source resistance.
rdeff	(Ω)	Effective drain resistance.
aseff	(m^2)	Effective area of source diffusion.
adeff	(m^2)	Effective area of drain diffusion.
pseff	(m)	Effective perimeter of source diffusion.
pdeff	(m)	Effective perimeter of source diffusion.
isseff	(A)	Effective source-bulk junction reverse saturation current.
isdeff	(A)	Effective drain-bulk junction reverse saturation current.
cbseff	(F)	Effective zero-bias source-bulk junction capacitance.
cbdeff	(F)	Effective zero-bias drain-bulk junction capacitance.
vto	(V)	Effective zero-bias threshold voltage.
vfb	(V)	Effective flat-band voltage.
phi	(V)	Effective surface potential.
k1	($\sqrt{V}$)	Effective body-effect coefficient.

© 2023 Cadence Design Systems, Inc.

`k2`	Effective charge-sharing parameter.
`eta`	Effective DIBL coefficient.

Related Topics

MOS Level-2 Model (mos2)

MOS Level-3 Model (mos3)

BSIM2 Level-5 Model (bsim2)

BSIM3v2 Level-10 Model (bsim3)

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

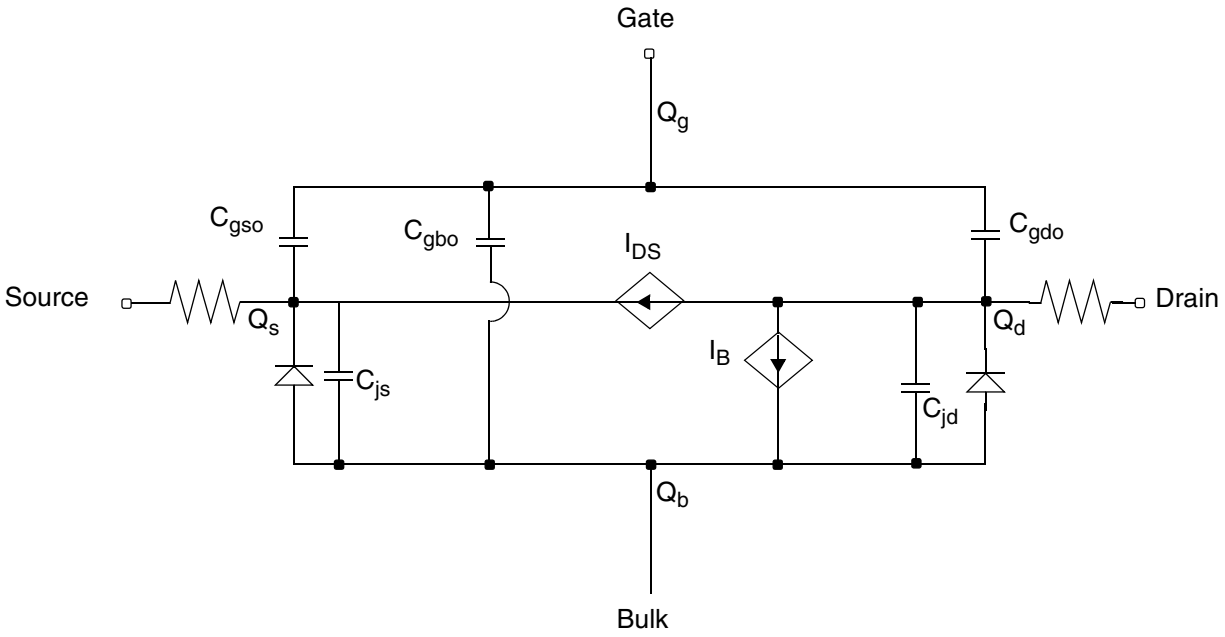
19

BSIM2 Level-5 Model (bsim2)

The BSIM2 model is based on the industry standard efforts of the Compact Modeling Counsel (CMC) and the BSIM modeling group at the University of California, Berkeley. Click the following links for information about the BSIM2 model:

- Parameter Calculation
- Drain Current Model
- Scaling Effects
- Component Statements

© 2023 Cadence Design Systems, Inc.



BSIM2 stands for Berkeley Short-Channel IGFET Model version-2. The BSIM2 is a semi empirical model suitable for devices with channel length from long channel to about 0.2 µm. Because it also models the output resistance, BSIM2 is suitable for both digital and analog applications. BSIM2 extracts all model parameters directly from physical devices. You can obtain an automated parameter extraction program, based on the IBM PC and HP4145 system, from the ILP office, Department of EECS, University of California, Berkeley. The following table shows the correspondence between the input parameter names and the equation symbols for the BSIM2 model.

Parameter	Symbol	Parameter	Symbol	Parameter	Symbol
vfb	$V_{FB,0}$	lvfb	$V_{FB,L}$	wvfb	$V_{FB,W}$
phi	ϕ_0	lphi	ϕ_L	wphi	ϕ_W
k1	K_1	lk1	$K_{1,L}$	wk1	$K_{1,W}$
k2	K_2	lk2	$K_{2,L}$	wk2	$K_{2,W}$
eta0	$\eta_{0,0}$	leta0	$\eta_{0,L}$	weta0	$\eta_{0,W}$
mu0	$\mu_{0,0}$	dl	dl	dw	dw
ua0	$U_{a0,0}$	lua0	$U_{a0,L}$	wua0	$U_{a0,W}$

© 2023 Cadence Design Systems, Inc.

Parameter	Symbol	Parameter	Symbol	Parameter	Symbol
uab	$U_{aB,0}$	luab	$U_{aB,L}$	wuab	$U_{aB,W}$
ub0	$U_{b0,0}$	lub0	$U_{b0,L}$	wub0	$U_{b0,W}$
ubb	$U_{bB,0}$	lubb	$U_{bB,L}$	wubb	$U_{bB,W}$
u10	$U_{10,0}$	lu10	$U_{10,L}$	wu10	$U_{10,W}$
u1b	$U_{1B,0}$	lu1b	$U_{1B,L}$	wu1b	$U_{1B,W}$
u1d	$U_{1D,0}$	lu1d	$U_{1D,L}$	wu1d	$U_{1D,W}$
mu0b	$\mu_{0B,0}$	lmu0b	$\mu_{0B,L}$	mu0b	$\mu_{0B,W}$
mus0	$\mu_{s0,0}$	lmus0	$\mu_{s0,L}$	wmus0	$\mu_{s0,W}$
musb	$\mu_{sB,0}$	lmusb	$\mu_{sB,L}$	wmusb	$\mu_{sB,W}$
mu20	$\mu_{20,0}$	lmu20	$\mu_{20,L}$	wmu20	$\mu_{20,W}$
mu2b	$\mu_{2B,0}$	lmu2b	$\mu_{2B,L}$	wmu2b	$\mu_{2B,W}$
mu2g	$\mu_{2G,0}$	lmu2g	$\mu_{2G,L}$	wmu2g	$\mu_{2G,W}$
mu30	$\mu_{30,0}$	lmu30	$\mu_{30,L}$	wmu30	$\mu_{30,W}$
mu3b	$\mu_{3B,0}$	lmu3b	$\mu_{3B,L}$	wmu3b	$\mu_{3B,W}$
mu3g	$\mu_{3G,0}$	lmu3g	$\mu_{3G,L}$	wmu3g	$\mu_{3G,W}$
mu40	$\mu_{40,0}$	lmu40	$\mu_{40,L}$	wmu40	$\mu_{40,W}$
mu4b	$\mu_{4B,0}$	lmu4b	$\mu_{4B,L}$	wmu4b	$\mu_{4B,W}$
mu4g	$\mu_{4G,0}$	lmu4g	$\mu_{4G,L}$	wmu4g	$\mu_{4G,W}$
etab	$\eta_{B,0}$	letab	$\eta_{B,L}$	wetab	$\eta_{B,W}$
n0	$N_{0,0}$	ln0	$N_{0,L}$	wn0	$N_{0,W}$
nb	$N_{B,0}$	lnb	$N_{B,L}$	wnb	$N_{B,W}$
nd	$N_{D,0}$	lnd	$N_{D,L}$	wnd	$N_{D,W}$
vof0	$V_{offset0,0}$	lvof0	$V_{offset0,L}$	wvof0	$V_{offset0,W}$
vofb	$V_{offsetB,0}$	lvofb	$V_{offsetB,L}$	wvofb	$V_{offsetB,W}$
vofd	$V_{offsetD,0}$	lvofd	$V_{offsetD,L}$	wvofd	$V_{offsetD,W}$
ai0	$A_{i0,0}$	lai0	$A_{i0,L}$	wai0	$A_{i0,W}$
aib	$A_{iB,0}$	laib	$A_{iB,L}$	waib	$A_{iB,W}$

© 2023 Cadence Design Systems, Inc.

Parameter	Symbol	Parameter	Symbol	Parameter	Symbol
bi0	$B_{i0,0}$	lbi0	$B_{i0,L}$	wbi0	$B_{i0,W}$
bib	$B_{iB,0}$	lbib	$B_{iB,L}$	wbib	$B_{iB,W}$
vdd	V_{DD}	vgg	V_{GG}	vbb	V_{BB}
vghigh	$V_{G,high}$	vglow	$V_{G,low}$		

Parameter Calculation

Except for mu0, dl, and dw, all device parameters are calculated from the following equation:

(19-1)

$$P_i = P_{i,0} + \frac{P_{i,L}}{L_{eff}} + \frac{P_{i,W}}{W_{eff}}$$

where P_i is any device parameter, $P_{i,0}$ is the parameter value for long channel length and width, and $P_{i,L}$ and $P_{i,W}$ are the channel length and width dependencies of the parameter, respectively. The following is an example showing how the flat-band voltage for a device with l = 2µm and w = 5µm is calculated from the model parameters.

(19-2)

$$V_{FB} = V_{FB,0} + \frac{V_{FB,L}}{2.0 - dl} + \frac{V_{FB,W}}{5.0 - dw}$$

Drain Current Model

Channel Width and Length

(19-3)

$$W_{scaled} = w * scale + xw * scalem$$

(19-4)

© 2023 Cadence Design Systems, Inc.

$$W_{eff} = \begin{cases} w*scale + xw*scalem - 2wd*scalem & \text{(Level 1-3)} \\ w*scale + xw*scalem - dw*scalem & \text{(BSIM 1-2)} \end{cases}$$

(19-5)

$$L_{eff} = \begin{cases} l*scale + xl*scalem - 2ld*scalem & \text{(Level 1-3)} \\ l*scale + xl*scalem - dl*scalem & \text{(BSIM 1-2)} \end{cases}$$

Threshold Voltage

(19-6)

$$V_{TH} = V_{FB} + \phi + K_1\sqrt{\phi - V_{BS}}K_2(\phi - V_{BS}) - \eta V_{DS}$$

where

(19-7)

$$\eta = \eta_0 + \eta_B V_{BS}$$

Drain Saturation Voltage

(19-8)

$$V_{DSAT} = \frac{V_{GST}}{a\sqrt{K}}$$

where

(19-9)

$$V_{GST} = V_{GS} - V_{TH}$$

(19-10)

$$a = 1 + \frac{gK_1}{2\sqrt{\phi - V_{BS}}}$$

© 2023 Cadence Design Systems, Inc.

(19-11)

$$g = 1 - \frac{1}{1.744 + 0.8364(\phi - V_{BS})}$$

(19-12)

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2}$$

(19-13)

$$V_c = \frac{U_{1S} V_{GST}}{a[1 + U_a V_{GST} + U_b V_{GST}^2]}$$

(19-14)

$$U_{1S} = \begin{cases} U_1\left[1 - \frac{U_{1D}(V_{DS} - V_{DSAT})^2}{V_{DSAT}^2}\right] & \text{if } V_{DS} \le V_{DSAT} \\ U_1 & \text{otherwise} \end{cases}$$

(19-15)

$$U_1 = U_{10} + U_{1B} V_{BS}$$

Drain Current for the Subthreshold Region

Note: These equations apply when $V_{GST} \le V_{glow}$.

(19-16)

$$I_{subth} = \beta V_t^2 e^{V_{offset} + V_{GST}/nV_t}\left[1 - e^{-V_{DS}/V_t}\right]$$

where

(19-17)

© 2023 Cadence Design Systems, Inc.

$$n = N_0 + \frac{N_B}{\sqrt{\phi - V_{BS}}} + N_D V_{DS}$$

(19-18)

$$V_{offset} = V_{offset0} + V_{offsetB} V_{BS} + V_{offsetD} V_{DS}$$

Drain Current for the Triode Region

Note: These equations apply when $V_{GST} \geq 0$ and $V_{DS} \leq V_{SAT}$.

(19-19)

$$I_{DS} = \frac{\beta_0 \left(V_{GST} - \frac{a}{2} V_{DS} \right) V_{DS}}{[1 + U_a V_{GST} + U_b V_{GST}^2 + U_{1S} V_{DS}]}$$

where

(19-20)

$$U_a = U_{a0} + U_{a0B} V_{BS}$$

(19-21)

$$U_b = U_{b0} + U_{b0B} V_{BS}$$

(19-22)

$$\beta_0 = \beta_{0lin} + \beta_1 \tanh \left[\frac{\beta_2 V_{DS}}{V_{DSAT}} \right] + \beta_3 V_{DS} - \beta_4 V_{DS}^2$$

(19-23)

$$\beta_{0lin} = \frac{C_{ox} W_{eff}}{L_{eff}} (\mu_0 + \mu_{0B} V_{BS})$$

© 2023 Cadence Design Systems, Inc.

(19-24)

$$\beta_1 = \beta_s - (\beta_{0lin} + \beta_3 V_{DD} - \beta_4 V_{DD}^2)$$

(19-25)

$$\beta_s = \frac{C_{ox} W_{eff}}{L_{eff}} (\mu_{s0} + \mu_{sB} V_{BS})$$

(19-26)

$$\beta_2 = \mu_{20} + \mu_{2B} V_{BS} + \mu_{2G} V_{GS}$$

(19-27)

$$\beta_3 = \frac{C_{ox} W_{eff}}{L_{eff}} (\mu_{30} + \mu_{3B} V_{BS} + \mu_{3G} V_{GS})$$

(19-28)

$$\beta_4 = \frac{C_{ox} W_{eff}}{L_{eff}} (\mu_{40} + \mu_{4b} V_{BS} + \mu_{4G} V_{GS})$$

Drain Current for the Saturation Region

Note: These equations apply when $V_{GST} \geq V_{ghigh}$ and $V_{DS} \geq V_{DSAT}$.

(19-29)

$$I_{DS} = \frac{\beta V_{GST}^2}{2aK} \left(1 + A_i e^{\frac{-B_i}{V_{DS} - V_{DSAT}}} \right)$$

where

(19-30)

© 2023 Cadence Design Systems, Inc.

$$\beta = \frac{\beta_0}{1 + U_a V_{GST} + U_b V_{GST}^2}$$

(19-31)

$$A_i = A_{i0} + A_{iB} V_{BS}$$

(19-32)

$$B_i = B_{i0} + B_{iB} V_{BS}$$

Drain Current for the Transition Region

Note: These equations apply when $V_{glow} \le V_{GST} \le V_{ghigh}$.

Drain current equations are the same as those for the strong-inversion region, except that V'_{GST} replaces all V_{GST} terms. V'_{GST} is calculated from a cubic spline function to match the drain current and its first derivative at the upper and lower bounds (V_{ghigh} and V_{glow}).

(19-33)

$$V'_{GST} = C_0 + C_1 V_{GST} + C_2 V_{GST}^2 + C_3 V_{GST}^3$$

All the coefficients, C_is, are automatically calculated during

(19-34)

$$V_{glow} = V_{TH} + V_{offset} + nV_t \ln\left(\frac{C_{ox}}{10C_d}\right)$$

(19-35)

$$V_{ghigh} = V_{TH} + nV_t \ln\left(\frac{10C_{ox}}{C_d}\right)$$

(19-36)

© 2023 Cadence Design Systems, Inc.

$$C_d = \sqrt{\frac{q\varepsilon_{si}N_{sub}}{2\phi}}$$

Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem).

Component Statements

This device is supported within altergroups.

Sample Instance Statement:

```
m2 (0 2 1 1) pchmod l=5u w=10u as=40u ad=40u pd=28u ps=28u m=1
```

Sample Model Statement:

```
model pchmod bsim2 type=p vfb0=-0.5 lvfb=0.5 wvfb=0.3 phi0=0.8 eta0=0.056 k1=0.5
eg=0.99 gap1=5.5e-04 trs=1e-3 trd=1e-3 xpart=0.5 rs=10 rd=10
```

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

w	(m)	Channel width.
l	(m)	Channel length.
as	(m^2)	Area of source diffusion.
ad	(m^2)	Area of drain diffusion.
ps	(m)	Perimeter of source diffusion.
pd	(m)	Perimeter of drain diffusion.
nrd	(m/m)	Number of squares of drain diffusion.
nrs	(m/m)	Number of squares of source diffusion.
ld	(m)	Drain diffusion length.
ls	(m)	Source diffusion length.
m	1	Multiplicity factor (number of MOSFETs in parallel).
region	triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile.Possible values are off, triode, sat, subth and breakdown.
trise	(C)	Temperature rise from ambient.
degradation	no	Hot-electron degradation flag.Possible values are no and yes.
isnoisy	yes	Should device generate noise.Possible values are no and yes.

Model Syntax

```
model modelName bsim2 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

type	n	Transistor type.Possible values are n and p.

Threshold voltage parameters

vfb0	-0.8 V	Flat-band voltage.
lvfb	0 V µm	Length dependence of vfb.
wvfb	0 V µm	Width dependence of vfb.
pvfb	0 V µm	Width-length dependence of vfb.
phi0	0.75 V	Surface potential.
lphi	0 V µm	Length dependence of phi.
wphi	0 V µm	Width dependence of phi.
pphi	0 V µm	Width-length dependence of phi.
k1	0.7 √V	Body-effect coefficient.
lk1	0 √V µm	Length dependence of k1.
wk1	0 √V µm	Width dependence of k1.
pk1	0 √V µm	Width-length dependence of k1.
k2	0	Charge-sharing parameter.
lk2	0 µm	Length dependence of k2.

© 2023 Cadence Design Systems, Inc.

wk2	0 µm	Width dependence of k2.
pk2	0 µm	Width-length dependence of k2.
eta0	0	Drain-induced barrier-lowering coefficient.
leta0	0 µm	Length dependence of eta0.
weta0	0 µm	Width dependence of eta0.
peta0	0 µm	Width-length dependence of eta0.
etab	0 1/V	Body-bias dependence of eta0.
letab	0 µm/V	Length dependence of etab.
wetab	0 µm/V	Width dependence of etab.
petab	0 µm/V	Width-length dependence of etab.

© 2023 Cadence Design Systems, Inc.

Mobility parameters

mu0	400 $cm^2/V\ s$	Low-field mobility.
lmu0	0 $cm^2/V\ s$	Length dependence of mu0.
wmu0	0 $cm^2/V\ s$	Width dependence of mu0.
pmu0	0 $cm^2/V\ s$	Width-length dependence of mu0.
mu0b	0 $cm^2/V^2\ s$	Body-bias dependence of muz.
lmu0b	0 $cm^2\ \mu m/V^2\ s$	Length dependence of x2mz.
wmu0b	0 $cm^2\ \mu m/V^2\ s$	Width dependence of x2mz.
pmu0b	0 $cm^2\ \mu m/V^2\ s$	Width-length dependence of x2mz.
mus0	450 $cm^2/V\ s$	Mobility in the saturation region.
lmus0	0 $cm^2\ \mu m/V\ s$	Length dependence of mus0.
wmus0	0 $cm^2\ \mu m/V\ s$	Width dependence of mus0.
pmus0	0 $cm^2\ \mu m/V\ s$	Width-length dependence of mus0.
musb	0 $cm^2/V^2\ s$	Body-bias dependence of mus0.

© 2023 Cadence Design Systems, Inc.

lmusb	0 cm^2 $\mu m/V^2$ s	Length dependence of mus0.
wmusb	0 cm^2 $\mu m/V^2$ s	Length dependence of mus0.
pmusb	0 cm^2 $\mu m/V^2$ s	Length dependence of mus0.
mu20	1	Empirical channel length modulation parameter.
lmu20	0 µm	Length dependence of mu20.
wmu20	0 µm	Width dependence of mu20.
pmu20	0 µm	Width-length dependence of mu20.
mu2b	0 1/V	Body-bias dependence of mu20.
lmu2b	0 µm/V	Length dependence of mu2b.
wmu2b	0 µm/V	Width dependence of mu2b.
pmu2b	0 µm/V	Width-length dependence of mu2b.
mu2g	0 1/V	Gate-bias dependence of mu20.
lmu2g	0 µm/V	Length dependence of mu2g.
wmu2g	0 µm/V	Width dependence of mu2g.
pmu2g	0 µm/V	Width-length dependence of mu2g.
mu30	5 cm^2/V^2 s	Empirical output resistance parameter.
lmu30	0 cm^2 $\mu m/V^2$ s	Length dependence of mu30.

© 2023 Cadence Design Systems, Inc.

wmu30	0 cm^2 $\mu m/V^2$ s	Width dependence of mu30.
pmu30	0 cm^2 $\mu m/V^2$ s	Width-length dependence of mu30.
mu3b	0 cm^2/V^3 s	Body-bias dependence of mu30.
lmu3b	0 cm^2 $\mu m/V^3$ s	Length dependence of mu3b.
wmu3b	0 cm^2 $\mu m/V^3$ s	Width dependence of mu3b.
pmu3b	0 cm^2 $\mu m/V^3$ s	Width-length dependence of mu3b.
mu3g	0 cm^2/V^3 s	Gate-bias dependence of mu30.
lmu3g	0 cm^2 $\mu m/V^3$ s	Length dependence of mu3g.
wmu3g	0 cm^2 $\mu m/V^3$ s	Width dependence of mu3g.
pmu3g	0 cm^2 $\mu m/V^3$ s	Width-length dependence of mu3g.
mu40	0 cm^2/V^3 s	Empirical output resistance parameter.
lmu40	0 cm^2 $\mu m/V^3$ s	Length dependence of mu40.
wmu40	0 cm^2 $\mu m/V^3$ s	Width dependence of mu40.

© 2023 Cadence Design Systems, Inc.

pmu40	0 $cm^2/\mu m/V^3$ s	Width-length dependence of mu40.
mu4b	0 cm^2/V^3 s	Empirical output resistance parameter.
lmu4b	0 $cm^2/\mu m/V^3$ s	Length dependence of mu4b.
wmu4b	0 $cm^2/\mu m/V^3$ s	Width dependence of mu4b.
pmu4b	0 $cm^2/\mu m/V^3$ s	Width-length dependence of mu4b.
mu4g	0 cm^2/V^3 s	Gate-bias dependence of mu4g.
lmu4g	0 $cm^2/\mu m/V^3$ s	Length dependence of mu4g.
wmu4g	0 $cm^2/\mu m/V^3$ s	Width dependence of mu4g.
pmu4g	0 $cm^2/\mu m/V^3$ s	Width-length dependence of mu4g.

© 2023 Cadence Design Systems, Inc.

Mobility modulation parameters

ua0	0 1/V	Gate voltage dependence of mobility.
lua0	0 µm/V	Length dependence of ua0.
wua0	0 µm/V	Width dependence of ua0.
pua0	0 µm/V	Width-length dependence of ua0.
uab	0 $1/V^2$	Body-bias dependence of ua.
luab	0 $\mu m/V^2$	Length dependence of uab.
wuab	0 $\mu m/V^2$	Width dependence of uab.
puab	0 $\mu m/V^2$	Width-length dependence of uab.
ub0	0 $1/V^2$	Second-order effect of gate voltage dependence of mobility.
lub0	0 $\mu m/V^2$	Length dependence of ub0.
wub0	0 $\mu m/V^2$	Width dependence of ub0.
pub0	0 $\mu m/V^2$	Width-length dependence of ub0.
ubb	0 $1/V^3$	Body-bias dependence of ub.
lubb	0 $\mu m/V^3$	Length dependence of ubb.
wubb	0 $\mu m/V^3$	Width dependence of ubb.
pubb	0 $\mu m/V^3$	Width-length dependence of ubb.

© 2023 Cadence Design Systems, Inc.

Velocity saturation parameters

u10	0 1/V	Velocity saturation coefficient.
lu10	0 μm/V	Length dependence of u1.
wu10	0 μm/V	Width dependence of u1.
pu10	0 μm/V	Width-length dependence of u1.
u1b	0 $1/V^2$	Body-bias dependence of u1.
lu1b	0 $\mu m/V^2$	Length dependence of u1b.
wu1b	0 $\mu m/V^2$	Width dependence of u1b.
pu1b	0 $\mu m/V^2$	Width-length dependence of u1b.
u1d	0 $1/V^2$	Drain-bias dependence of u1.
lu1d	0 $\mu m/V^2$	Length dependence of u1d.
wu1d	0 $\mu m/V^2$	Width dependence of u1d.
pu1d	0 $\mu m/V^2$	Width-length dependence of u1d.

Subthreshold parameters

n0	0	Subthreshold swing parameter.
ln0	0 μm	Length dependence of subthreshold swing parameter.
wn0	0 μm	Width dependence of subthreshold swing parameter.

© 2023 Cadence Design Systems, Inc.

pn0	0	µm	Width-length dependence of subthreshold swing parameter.
nb	0	1/V	Body-bias dependence of n0.
lnb	0	1/V µm	Length dependence of nb.
wnb	0	1/V µm	Width dependence of nb.
pnb	0	1/V µm	Width-length dependence of nb.
nd	0	1/V	Drain-bias dependence of n0.
lnd	0	µm/V	Length dependence of nd.
wnd	0	µm/V	Width dependence of nd.
pnd	0	µm/V	Width-length dependence of nd.
vof0	1	V	Threshold voltage offset in the subthreshold region.
lvof0	0	V µm	Length dependence of vof.
wvof0	0	V µm	Width dependence of vof.
pvof0	0	V µm	Width-length dependence of vof.
vofb	0		Body-bias dependence of vof0.
lvofb	0	µm	Length dependence of vofb.
wvofb	0	µm	Width dependence of vofb.
pvofb	0	µm	Width-length dependence of vofb.
vofd	0		Drain-bias dependence of vof0.
lvofd	0	µm	Length dependence of vofd.

© 2023 Cadence Design Systems, Inc.

wvofd	0 μm	Width dependence of vofd.
pvofd	0 μm	Width-length dependence of vofd.
subthmod	2	Subthreshold model selector.

© 2023 Cadence Design Systems, Inc.

Impact ionization parameters

ai0	0 1/V	Hot-electron effect on Rout parameter.
lai0	0 μm/V	Length dependence of ai0.
wai0	0 μm/V	Width dependence of ai0.
pai0	0 μm/V	Width-length dependence of ai0.
aib	0 $1/V^2$	Body-bias dependence of ai0.
laib	0 $\mu m/V^2$	Length dependence of aib.
waib	0 $\mu m/V^2$	Width dependence of aib.
paib	0 $\mu m/V^2$	Width-length dependence of aib.
bi0	0 V	Hot-electron effect on Rout exponent.
lbi0	0 V μm	Length dependence of bi0.
wbi0	0 V μm	Width dependence of bi0.
pbi0	0 V μm	Width-length dependence of bi0.
bib	0	Body-bias dependence of bi0.
lbib	0 μm	Length dependence of bib.
wbib	0 μm	Width dependence of bib.
pbib	0 μm	Width-length dependence of bib.

Transition region bound parameters

vghigh	0.2 V	Upper bound of the transition region.

© 2023 Cadence Design Systems, Inc.

`lvghigh`	`0 V µm`	Length dependence of `Vghigh`.
`wvghigh`	`0 V µm`	Width dependence of `Vghigh`.
`pvghigh`	`0 V µm`	Width-length dependence of `Vghigh`.
`vglow`	`-0.15 V`	Lower bound of the transition region.
`lvglow`	`0 V µm`	Length dependence of `Vglow`.
`wvglow`	`0 V µm`	Width dependence of `Vglow`.
`pvglow`	`0 V µm`	Width-length dependence of `Vglow`.

© 2023 Cadence Design Systems, Inc.

Length and width modulation parameters

dl0	0 µm	Lateral diffusion.
dw0	0 µm	Field oxide encroachment.
lref	infinity m	Reference channel length.
wref	infinity m	Reference channel width.
xw	0 m	Width variation due to masking and etching.
xl	0 m	Length variation due to masking and etching.

Temperature effects parameters

temp	(C)	Parameters measurement temperature. Default set by options.
trise	0 C	Temperature rise from ambient.
compatible	spectre	Encourage device equations to be compatible with a foreign simulator.This option does not affect the input synax.Possible values are spectre, spice2, spice3, cdsspice, hspice, spiceplus, eldo, sspice, mica, tispice and pspice.
tempmod	432	Temperature model selector.
version	432	Version selector.
uto	0 C	Mobility temperature offset.
ute	-1.5	Mobility temperature exponent.

© 2023 Cadence Design Systems, Inc.

tlev	0	DC temperature selector.
tlevc	0	AC temperature selector.
ptc	0 V/C	Surface potential temperature coefficient.
eg	1.12452 V	Energy band gap.
gap1	7.02e-4 V/C^2	Band gap temperature coefficient.
gap2	1108 K	Band gap temperature offset.
trs	0 1/C	Temperature coefficient for source resistance.
trd	0 1/C	Temperature coefficient for drain resistance.
xti	3	Saturation current temperature exponent.

© 2023 Cadence Design Systems, Inc.

Overlap capacitance parameters

cgso	0 F/m	Gate-source overlap capacitance.
cgdo	0 F/m	Gate-drain overlap capacitance.
cgbo	0 F/m	Gate-bulk overlap capacitance.
meto	0 m	Metal overlap in fringing field.

Charge model selection parameters

capmod	bsim	Intrinsic charge model.Possible values are none, meyer, yang and bsim.
xpart	1	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
xqc	0	Drain/source channel charge partition in saturation for charge models, e.g. use 0.4 for 40/60, 0.5 for 50/50, or 0 for 0/100.

Parasitic resistance parameters

rs	0 Ω	Source resistance.
rd	0 Ω	Drain resistance.
rsh	0 Ω/sqr	Source/drain diffusion sheet resistance.
rsc	0 Ω	Source contact resistance.
rdc	0 Ω	Drain contact resistance.

© 2023 Cadence Design Systems, Inc.

rss	0 Ω m	Scalable source resistance.
rdd	0 Ω m	Scalable drain resistance.
minr	0.1 Ω	Minimum source/drain resistance.
hdif	0 m	Length of heavily doped diffusion.
ldif	0 m	Lateral diffusion beyond the gate.
lgcs	0 m	Gate-to-contact length of source side.
lgcd	0 m	Gate-to-contact length of drain side.
sc	infinity m	Spacing between contacts.

© 2023 Cadence Design Systems, Inc.

Junction diode parameters

`js`	`(A/m`^{2}`)`	Bulk junction reverse saturation current density.
`is`	`1e-14 A`	Bulk junction reverse saturation current.
`n`	`1`	Junction emission coefficient.
`dskip`	`yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`.Possible values are no and yes.
`imelt`	`` `imaxA' ``	Explosion current, diode is linearized beyond this current to aid convergence.
`jmelt`	`` `jmaxA/m'`^{2}	Explosion current density, diode is linearized beyond this current to aid convergence.

Operating region warning control parameters

`alarm`	`none`	Forbidden operating region.Possible values are none, off, triode, sat, subth and rev.
`imax`	`1 A`	Maximum current, currents above this limit generate a warning.
`jmax`	`1e8 A/m`^{2}	Maximum current density, currents above this limit generate a warning.
`bvj`	`infinity V`	Junction reverse breakdown voltage.
`vbox`	`1e9*tox V`	Oxide breakdown voltage.

© 2023 Cadence Design Systems, Inc.

Junction capacitance model parameters

cbs	0 F	Bulk-source zero-bias junction capacitance.
cbd	0 F	Bulk-drain zero-bias junction capacitance.
cj	0 F/m^2	Zero-bias junction bottom capacitance density.
mj	1/2	Bulk junction bottom grading coefficient.
pb	0.8 V	Bulk junction potential.
fc	0.5	Forward-bias depletion capacitance threshold.
cjsw	0 F/m	Zero-bias junction sidewall capacitance density.
mjsw	1/3	Bulk junction sidewall grading coefficient.
pbsw	0.8 V	Side-wall junction potential.
fcsw	0.5	Side-wall forward-bias depletion capacitance threshold.

Process and power supply parameters

tox	4e-8 m	Gate oxide thickness.
vdd	5 V	Drain voltage at which parameters are extracted.
vgg	5 V	Gate voltage at which parameters are extracted.
vbb	-5 V	Body voltage at which parameters are extracted.

© 2023 Cadence Design Systems, Inc.

Default device parameters

w	3e-6 m	Channel width.
l	3e-6 m	Channel length.
as	0 m^2	Area of source diffusion.
ad	0 m^2	Area of drain diffusion.
ps	0 m	Perimeter of source diffusion.
pd	0 m	Perimeter of drain diffusion.
nrd	0 m/m	Number of squares of drain diffusion.
nrs	0 m/m	Number of squares of source diffusion.
ldd	0 m	Drain diffusion length.
lds	0 m	Source diffusion length.

Noise model parameters

noisemod	1	Noise model selector.
kf	0	Flicker (1/f) noise coefficient.
af	1	Flicker (1/f) noise exponent.
ef	1	Flicker (1/f) noise frequency exponent.
wnoi	1e-5 m	Channel width at which noise parameters were extracted.

© 2023 Cadence Design Systems, Inc.

Auto Model Selector parameters

wmax	1.0 m	Maximum channel width for which the model is valid.
wmin	0.0 m	Minimum channel width for which the model is valid.
lmax	1.0 m	Maximum channel length for which the model is valid.
lmin	0.0 m	Minimum channel length for which the model is valid.

Degradation parameters

degramod	spectre	Degradation model selector.Possible values are spectre and bert.
degradation	no	Hot-electron degradation flag.Possible values are no and yes.
dvthc	1 V	Degradation coefficient for threshold voltage.
dvthe	1	Degradation exponent for threshold voltage.
duoc	1 S	Degradation coefficient for transconductance.
duoe	1	Degradation exponent for transconductance.
crivth	0.1 V	Maximum allowable threshold voltage shift.
criuo	10%	Maximum allowable normalized mobility change.
crigm	10%	Maximum allowable normalized transconductance change.
criids	10%	Maximum allowable normalized drain current change.

© 2023 Cadence Design Systems, Inc.

`wnom`	`5e-6 m`	Nominal device width in degradation calculation.
`lnom`	`1e-6 m`	Nominal device length in degradation calculation.
`vbsn`	`0 V`	Substrate voltage in degradation calculation.
`vdsni`	`0.1 V`	Drain voltage in `Ids` degradation calculation.
`vgsni`	`5 V`	Gate voltage in `Ids` degradation calculation.
`vdsng`	`0.1 V`	Drain voltage in `Gm` degradation calculation.
`vgsng`	`5 V`	Gate voltage in `Gm` degradation calculation.

© 2023 Cadence Design Systems, Inc.

Spectre stress parameters

esat	1.1e7 V/m	Critical field in Vdsat calculation.
esatg	2.5e6 1/m	Gate voltage dependence of esat.
vpg	-0.25	Gate voltage modifier.
vpb	-0.13	Gate voltage modifier.
subc1	2.24e-5	Substrate current coefficient.
subc2	-0.1e-5 1/V	Substrate current coefficient.
sube	6.4	Substrate current exponent.
strc	1	Stress coefficient.
stre	1	Stress exponent.

BERT stress parameters

h0	1	Aging coefficient.
hgd	0 1/V	Bias dependence of h0.
m0	1	Aging exponent.
mgd	0 1/V	Bias dependence of m0.
ecrit0	1.1e5 V/cm	Critical electric field.

© 2023 Cadence Design Systems, Inc.

lecrit0	0 µm V/cm	Length dependence of ecrit0.
wecrit0	0 µm V/cm	Width dependence of ecrit0.
ecritg	0 1/cm	Gate voltage dependence of ecrit0.
lecritg	0 µm/cm	Length dependence of ecritg.
wecritg	0 µm/cm	Width dependence of ecritg.
ecritb	0 1/cm	Substrate voltage dependence of ecrit0.
lecritb	0 µm/cm	Length dependence of ecritb.
wecritb	0 µm/cm	Width dependence of ecritb.
lc0	1	Substrate current coefficient.
llc0	0 µm	Length dependence of lc0.
wlc0	0 µm	Width dependence of lc0.
lc1	1	Substrate current coefficient.
llc1	0 µm	Length dependence of lc1.
wlc1	0 µm	Width dependence of lc1.
lc2	1	Substrate current coefficient.
llc2	0 µm	Length dependence of lc2.
wlc2	0 µm	Width dependence of lc2.
lc3	1	Substrate current coefficient.

© 2023 Cadence Design Systems, Inc.

`llc3`	0 µm	Length dependence of `lc3`.
`wlc3`	0 µm	Width dependence of `lc3`.
`lc4`	1	Substrate current coefficient.
`llc4`	0 µm	Length dependence of `lc4`.
`wlc4`	0 µm	Width dependence of `lc4`.
`lc5`	1	Substrate current coefficient.
`llc5`	0 µm	Length dependence of `lc5`.
`wlc5`	0 µm	Width dependence of `lc5`.
`lc6`	1	Substrate current coefficient.
`llc6`	0 µm	Length dependence of `lc6`.
`wlc6`	0 µm	Width dependence of `lc6`.
`lc7`	1	Substrate current coefficient.
`llc7`	0 µm	Length dependence of `lc7`.
`wlc7`	0 µm	Width dependence of `lc7`.

Imax and Imelt:

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and Spectre prints a warning.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, the base and collector currents are composed of many exponential terms, Spectre issues a warning and the results become inaccurate. The junction

© 2023 Cadence Design Systems, Inc.

current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

Both of these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

Auto Model Selection:

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin` should be given. The selection criteria to choose a model is as follows:

```
  lmin <= inst_length < lmax  and   wmin <= inst_width  < wmax
```

Example:

```
model ModelName ModelType {
   1:     <model parameters> lmin=2 lmax=4 wmin=1 wmax=2
   2:     <model parameters> lmin=1 lmax=2 wmin=2 wmax=4
   3:     <model parameters> lmin=2 lmax=4 wmin=4 wmax=6
}
```

Then for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

© 2023 Cadence Design Systems, Inc.

Output Parameters

tempeff	(C)	Effective temperature for a single device.
weff	(m)	Effective channel width.
leff	(m)	Effective channel length.
rseff	(Ω)	Effective source resistance.
rdeff	(Ω)	Effective drain resistance.
aseff	(m^2)	Effective area of source diffusion.
adeff	(m^2)	Effective area of drain diffusion.
pseff	(m)	Effective perimeter of source diffusion.
pdeff	(m)	Effective perimeter of source diffusion.
isseff	(A)	Effective source-bulk junction reverse saturation current.
isdeff	(A)	Effective drain-bulk junction reverse saturation current.
cbseff	(F)	Effective zero-bias source-bulk junction capacitance.
cbdeff	(F)	Effective zero-bias drain-bulk junction capacitance.
vto	(V)	Effective zero-bias threshold voltage.
vfb	(V)	Effective flat-band voltage.
phi	(V)	Effective surface potential.
k1	($\sqrt{V}$)	Effective body-effect coefficient.

© 2023 Cadence Design Systems, Inc.

`k2`	Effective charge-sharing parameter.
`eta`	Effective DIBL coefficient.

Related Topics

MOS Level-2 Model (mos2)

MOS Level-3 Model (mos3)

BSIM1 Level-4 Model (bsim1)

BSIM3v2 Level-10 Model (bsim3)

© 2023 Cadence Design Systems, Inc.

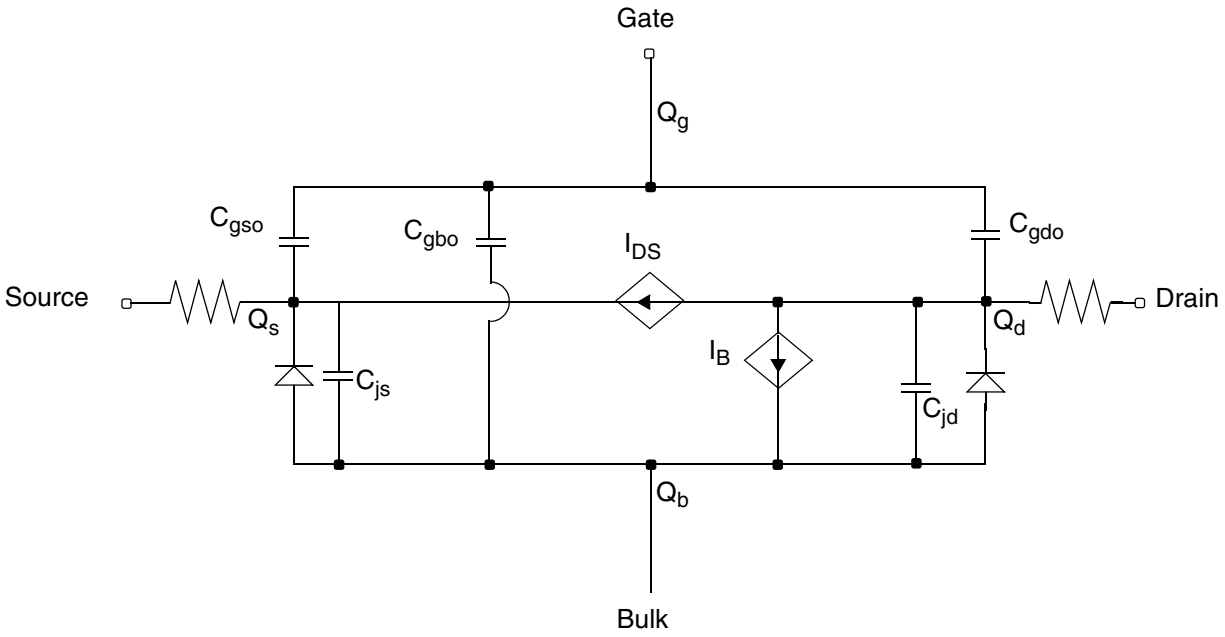
20

BSIM3v2 Level-10 Model (bsim3)

The BSIM3 model is based on the industry standard efforts of the Compact Modeling Counsel (CMC) and the BSIM modeling group at the University of California, Berkeley. It is suitable for both digital and analog applications. Click to view the following links for information about the BSIM3v2 model:

- Threshold Voltage
- Subthreshold Current
- Drain Saturation Voltage
- Drain Current for the Triode Region
- Drain Current for the Saturation Region
- Default Model Parameter Value Calculation
- Scaling Effects
- New Features in BSIM3 Version 3.2.4
- Component Statements

© 2023 Cadence Design Systems, Inc.



Threshold Voltage

(20-1)

$$V_{TH} = vtho + k1(\sqrt{phi - V_{BS}} - \sqrt{phi}) - k2 * V_{BS} - \Delta V_{TH} +$$

$$k1\left[\sqrt{1 + \frac{nlx}{L_{eff}}\sqrt{\frac{phi}{phi - V_{BS}}}} - 1\right]\sqrt{phi} + \frac{k3 * tox * phi}{W_{eff} + w0} + (kt1 + kt2V_{BS})\left(\frac{T}{tnom} - 1\right)$$

where

(20-2)

$$\Delta V_{TH} = \theta(vbi - phi)$$

(20-3)

$$\theta = dvt0 * \theta_0$$

© 2023 Cadence Design Systems, Inc.

(20-4)

$$\theta_0 = e^{-dvt1 * L_{eff}/2l_0} + 2e^{-dvt1 * L_{eff}/l_0}$$

L_{eff} is the effective channel length, and I_0 is given by

(20-5)

$$l_0 = \sqrt{\frac{\varepsilon_{si} toxX_{dep}}{\varepsilon_{ox}}}(1 + dvt2 * V_{BS})$$

and

(20-6)

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}(phi - V_{BS})}{q * npeak}}$$

Subthreshold Current

There are two subthreshold current models that you can select with the `subthmod` parameter. If you set `subthmod` to 0, none of the subthreshold current models are used. For example, the drain current is zero when the gate voltage is less than the threshold voltage. If you set `subthmod` to 1, the summation approach is used. For example, the subthreshold current is always calculated and added to the drain current for the strong-inversion region, regardless of the operating region.

If you set `subthmod` to 2, a transition region between the subthreshold regions and the strong-inversion regions is created. This transition region provides smooth switching between the subthreshold and the strong-inversion regions. The following equations are model equations for the subthreshold and transition regions.

subthmod = 1

(20-7)

$$I_{subth} = \frac{I_{exp} I_{limit}}{I_{exp} + I_{limit}}(1 - e^{-V_{DS}/V_{tm}})$$

© 2023 Cadence Design Systems, Inc.

where

(20-8)

$$I_{limit} = 4.5\beta_0 V_{tm}^2$$

(20-9)

$$I_{exp} = \beta_{subth} V_{tm}^2 e^{(V'_{GST}/nV_{tm})}$$

(20-10)

$$V'_{GST} = V_{GST} - voff + V_{dibl}$$

(20-11)

$$V_{dibl} = (eta0 + etab * V_{BS}) * \theta_d * V_{DS}$$

(20-12)

$$\theta_d = pdibl1[e^{-drout * L_{eff}/2l_{00}} + 2e^{-drout * L_{eff}/l_{00}}]$$

(20-13)

$$l_{00} = \sqrt{\frac{\varepsilon_{si} toxX_{dep0}}{\varepsilon_{ox}}}$$

(20-14)

$$X_{dep0} = \sqrt{\frac{2\varepsilon_{si} phi}{q * npeak}}$$

(20-15)

$$V_{GST} = V_{GS} - V_{TH}$$

(20-16)

© 2023 Cadence Design Systems, Inc.

$$\beta_{subth} = \frac{uoC_{d0}W_{eff}}{L_{eff}}$$

(20-17)

$$n = 1 + \frac{C_d}{C_{ox}}nfactor + \frac{(cdsc + cdsc1 * V_{BS})}{C_{ox}}\theta_0 + \frac{C_{it}}{C_{ox}}$$

subthmod = 2

If $V_{GST} \le V_{glow} - V_{dibl}$, the drain current is given by current.

(20-18)

$$I_{DS} = I_{subth} = \beta_0 V_{tm}^2 e^{(V'_{GST}/nV_{tm})}(1 - e^{-V_{DS}/V_{tm}})$$

If $V_{glow} - V_{dibl} \le V_{GST} \le V_{ghigh} + V_{dibl}$, the device is operated in the transition region and the drain current is given by

(20-19)

$$I_{DS} = (1-t)^2 I_{dlow} + 2t(1-t)I_p + t^2 I_{dhigh}$$

where I_{dlow} is the subthreshold current evaluated at $V_{GST} = V_{glow} - V_{dibl}$, and I_{dhigh} is the strong-inversion drain current evaluated at $V_{GST} = V_{ghigh} + V_{dibl}$.

(20-20)

$$t = \left(\frac{V_p - V_{glow}}{Y}\right)\left[\sqrt{1 + \frac{Y(V_{GST} - V_{glow})}{(V_p - V_{glow})^2}} - 1\right]$$

(20-21)

$$Y = V_{glow} - 2V_p + V_{ghigh}$$

(20-22)

$$I_p = I_{dlow} + g_{mlow}(V_p - V_{glow})$$

© 2023 Cadence Design Systems, Inc.

(20-23)

$$V_p = \frac{(g_{mhigh}V_{ghigh} - g_{mlow}V_{glow}) - (I_{dhigh} - I_{dlow})}{g_{mhigh} - g_{mlow}}$$

g_{mhigh} and g_{mlow} are the transconductances evaluated at $V_{GST} = V_{ghigh} + V_{dibl}$.

Drain Saturation Voltage

If $R_{ds} = 0$,

(20-24)

$$V_{DSAT} = \frac{V_{GST}E_{SAT}L_{eff}}{V_{GST} + A_{bulk}E_{SAT}L_{eff}}$$

otherwise

(20-25)

$$V_{DSAT} = \frac{C_B - \sqrt{C_B^2 - 4C_AC_C}}{2C_A}$$

where

(20-26)

$$R_{ds} = rds0 + \frac{rdsw * 10^{-6}}{W_{eff}}$$

(20-27)

$$E_{SAT} = \frac{2vsat}{\mu_{eff}}$$

(20-28)

© 2023 Cadence Design Systems, Inc.

$$\mu_{eff} = \frac{uo}{U_{vert}}$$

(20-29)

$$U_{vert} = 1 + ua\left(\frac{V_{GS} + V_{TH}}{tox}\right) + ub\left(\frac{V_{GS} + V_{TH}}{tox}\right)^2 + uc * V_{BS}$$

If $keta = 0$,

(20-30)

$$A_{bulk} = 1 + \frac{k1 * a0 * L_{eff}}{2(L_{eff} + 2\sqrt{xjX_{dep}})\sqrt{phi - V_{BS}}}$$

otherwise,

(20-31)

$$A_{bulk} = \left(1 + \frac{k1 * a0 * L_{eff}}{2(L_{eff} + 2\sqrt{xjX_{dep}})\sqrt{phi}}\right)\frac{1}{1 + keta * V_{BS}/L_{eff}}$$

(20-32)

$$C_A = A_{bulk}^2 R_{vcw}$$

(20-33)

$$C_B = V_{GST} + A_{bulk} E_{SAT} L_{eff} + 3A_{bulk} R_{vcw} V_{GST}$$

(20-34)

$$C_C = E_{SAT} L_{eff} V_{GST} + 2R_{vcw} V_{GST}^2$$

(20-35)

$$R_{vcw} = V_{SAT} * R_{ds} C_{ox} W_{eff}$$

© 2023 Cadence Design Systems, Inc.

Drain Current for the Triode Region

Note: These equations apply to $V_{GST} \geq 0$ and $V_{DS} \leq V_{DSAT}$.

(20-36)

$$I_{DS} = \frac{I_{dslin0}}{1 + R_{ds} * I_{dslin0} / V_{DS}} \qquad \backslash$$

where I_{dslin0} is the drain current in the triode region without the presence of source and drain parasitic resistance.

(20-37)

$$I_{dslin0} = \frac{\beta_{effs}\left(V_{GST} - \frac{1}{2}A_{bulk}V_{DS}\right)V_{DS}}{1 + V_{DS} / E_{SAT}L_{eff}}$$

(20-38)

$$\beta_{eff} = \frac{\mu_{eff}C_{ox}W_{eff}}{L_{eff}}$$

Drain Current for the Saturation Region

Note: These equations apply to $V_{GST} > 0$ and $V_{DS} \geq V_{DSAT}$.

(20-39)

$$I_{DSAT} = I_{DSAT0}\left(1 + \frac{V'_{DS}}{V_a}\right) * \left[1 + \frac{pscbe2}{L_{eff}}V'_{DS}e^{(-pscbe1 * litl / V'_{DS})}\right]$$

where

(20-40)

$$I_{DSAT0} = W_{eff}C_{ox}vsat(V_{GST} - A_{bulk}V_{DSAT})$$

(20-41)

© 2023 Cadence Design Systems, Inc.

$$V'_{DS} = V_{DS} - V_{DSAT}$$

satmod = 1

(20-42)

$$V_a = V_{aa} + \left(1 + \frac{eta * ldd}{litl}\right) * \left[\frac{(E_{SAT}L_{eff} + V_{GST})V'_{DS}}{alpha * litl * E_{SAT}}\right]\left(1 - \frac{V'_{DS}}{2litl * em}\right)$$

(20-43)

$$V_{aa} = \frac{E_{SAT}L_{eff} + V_{DSAT} + 2R_{vcw}(V_{GST} - 0.5A_{bulk}V_{DSAT})}{1 + A_{bulk}R_{vcw}}$$

satmod = 2

(20-44)

$$V_a = V_{aa} + \left(1 + \frac{eta * ldd}{litl}\right)\left(\frac{V_{aclm} * V_{dibl}}{V_{aclm} + V_{adibl}}\right) * pvag$$

(20-45)

$$V_{aclm} = \frac{(E_{SAT}L_{eff}A_{bulk} + V_{GST})V'_{DS}}{litl * pclm * E_{SAT}A_{bulk}}$$

(20-46)

$$V_{adibl} = \left(\frac{V_{GST} - \frac{V_{GST}A_{bulk}V_{DSAT}}{V_{GST} + A_{bulk}V_{DSAT}}}{\theta_{rout}}\right)$$

where

(20-47)

© 2023 Cadence Design Systems, Inc.

$$\theta_{rout} = pdibli[e^{-drout*L_{eff}/2l_0} + 2e^{-drout*L_{eff}/l_0}] + pdibl2$$

Default Model Parameter Value Calculation

The following are the calculation methods for default model parameter values under various conditions:

- If $vtho$ is not given, it is calculated from

(20-48)

$$vtho = vfb + phi + k1\sqrt{phi}$$

- If phi is not given, it is calculated from

(20-49)

$$phi = 2V_{tm}\ln\left(\frac{npeak}{n_i}\right)$$

where V_{tm} is the thermal voltage given by

(20-50)

$$V_{tm} = \frac{kT}{q}$$

(20-51)

$$n_i = 1.45 \times 10^{10}\left(\frac{T}{300}\right)^{1.5}\exp\left(\frac{1.12}{0.0516} - \frac{E_g(T)}{2V_{tm}}\right)$$

where $E_g(T)$ is the energy band gap at temperature T. The equation for E_g is shown in BSIM3v2 Level-10 Model (bsim3)

- If $k1$ is not given, it is calculated from

(20-52)

$$k1 = gamma2 + 2k2\sqrt{phi - vbm}$$

- If $k2$ is not given, it is calculated from

© 2023 Cadence Design Systems, Inc.

(20-53)

$$k2 = \frac{(gamma2 - gamma1)(\sqrt{phi - vbx} - \sqrt{phi})}{2\sqrt{phi}(\sqrt{phi - vbm} - \sqrt{phi}) + vbm}$$

- If $gamma1$ is not given, it is calculated from

(20-54)

$$gamma1 = \frac{\sqrt{2q\varepsilon_{si}npeak}}{C_{ox}}$$

- If $gamma2$ is not given, it is calculated from

(20-55)

$$gamma2 = \frac{\sqrt{2q\varepsilon_{si}nsub}}{C_{ox}}$$

- If $litl$ is not given, it is calculated from

(20-56)

$$litl = \sqrt{\frac{\varepsilon_{si}xj}{C_{ox}}}$$

- If $vtho$ is not given, vfb is always calculated from

(20-57)

$$vfb = vtho - phi - k1\sqrt{phi} + k2*phi$$

regardless of any value you specify.

- If V_{bi} is not given, it is calculated from

(20-58)

$$V_{bi} = V_{tm}\ln\left(\frac{10^{22}npeak}{n_i^2}\right)$$

- If V_{bx} is not given, it is calculated from

© 2023 Cadence Design Systems, Inc.

(20-59)

$$V_{bx} = phi - \frac{q*npeak*xt^2}{2\varepsilon_{si}}$$

- If $gamma1$ is given, $npeak$ is calculated from

(20-60)

$$npeak = \frac{gamma1^2 C_{ox}^2}{2q\varepsilon_{si}}$$

  regardless of any value you specify.

  If neither $gamma1$ nor $npeak$ is specified, $npeak$ defaults to 1.7e1.7, and $gamma1$ is calculated from $npeak$.

- The default value for uo is 670 cm^2/V sec for NMOS and 250 cm^2/V sec for PMOS.
- The temperature-dependent mobility is calculated as

(20-61)

$$U_o(T) = U_o\left(\frac{T}{Tnom}\right)^{ute}$$

- The temperature-dependent saturation velocity is calculated as

(20-62)

$$V_{sat}(T) = V_{sat} - at(T - Tnom)$$

- The temperature-dependent mobility degradation parameters are calculated as

(20-63)

$$U_a(T) = U_a - U_{a1}\left(\frac{T}{Tnom} - 1\right)$$

(20-64)

$$U_b(T) = U_b - U_{b1}\left(\frac{T}{Tnom} - 1\right)$$

© 2023 Cadence Design Systems, Inc.

(20-65)

$$U_c(T) = U_c - U_{c1}\left(\frac{T}{Tnom} - 1\right)$$

- If V_{ghigh} is not given, it is calculated from

(20-66)

$$V_{ghigh} = n0V_{tm}\left[ln\left(\frac{10C_{ox}}{C_d}\right) + 3\right]$$

where

(20-67)

$$C_d = \sqrt{\frac{q\varepsilon_{si}npeak}{2phi}}$$

- If V_{glow} is not given, it is calculated from

(20-68)

$$V_{glow} = voff + n0V_{tm}ln\left(\frac{C_{ox}}{10C_d}\right) - theta*vdd$$

- If $cgdo(cgso)$ is not given, it is calculated from

(20-69)

$$cgdo(cgso) = \begin{cases} (dl + meto)*C_{ox} & \text{if } dl \text{ is given} \\ 0.5xj*C_{ox} & \text{otherwise} \end{cases}$$

Also, if $cgdo(cgso)$ is zero, 10^{-7} x C_{ox} is used.

If $cgbo$ is not given, it is calculated from

(20-70)

$$cgbo = 2dw*C_{ox}$$

© 2023 Cadence Design Systems, Inc.

Scaling Effects

For more information about scaling effects, seeScaling Factors (scale and scalem).

New Features in BSIM3 Version 3.2.4

The following features have been added to BSIM3v3.2.4:

1. A Spectre circuit simulator thermal noise model with the noise coefficient varying smoothly between 4 to 8/3 when the device moves from linear region to saturation region.
2. A BSIM4 ACNQS model that enables the NQS effect in AC simulations.
3. A new parameter *lintnoi* introducing an offset to the length reduction parameter (*lint*) to improve the accuracy of the flicker noise model

With the capacitance bug fix in this version, the transcapacitance CGG for capmod=3 is now smooth from the subthreshold region to strong inversion with no negative value.

BSIM3v3.2.4 is backward compatible with the previous versions of the model.

Component Statements

This device is supported within altergroups.

Sample Instance Statement:

```
m3 (1 2 0 0) nchmod l=1.5u w=100u as=450p ad=450p pd=209u ps=209u nrd=207m nrs=207m
m=1
```

Sample Model Statement:

```
model nchmod bsim3 vtho=5.94e-01 phi=0.69 k1=0.72 k2=0 w0=1.3e-07 tox=5.9e-09
rdsw=80 uo=499 xj=2e-07 vsat=600e+04 at=3.4e+04 a0=0.8 cdsc=1.4e-03 nfactor=1.03
```

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

w	(m)	Channel width.
l	(m)	Channel length.
as	(m^2)	Area of source diffusion.
ad	(m^2)	Area of drain diffusion.
ps	(m)	Perimeter of source diffusion.
pd	(m)	Perimeter of drain diffusion.
nrd	(m/m)	Number of squares of drain diffusion.
nrs	(m/m)	Number of squares of source diffusion.
isnoisy	yes	Should device generate noise.Possible values are no and yes.
m	1	Multiplicity factor (number of MOSFETs in parallel).
region	triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile.Possible values are off, triode, sat, subth and breakdown.
trise		Temperature rise from ambient.
geo	0	Geometry selector.

Model Syntax

```
model modelName bsim3 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type *parameters*

type	n	Transistor type.Possible values are n and p.

Threshold voltage *parameters*

vtho	0 V	Threshold voltage at zero body bias.
phi	0.7 V	Surface potential at strong inversion.
k1	0.53 √V	Body-effect coefficient.
k2	-0.0186	Charge-sharing parameter.
k3	80	Narrow width coefficient.
k3b	0 1/V	Narrow width coefficient.
w0	2.5e-6 m	Narrow width coefficient.
nlx	1.74e-7 m	Lateral nonuniform doping coefficient.
gamma1	0 √V	Body-effect coefficient near the surface.
gamma2	0 √V	Body-effect coefficient in the bulk.
theta	0.02 1/V	Drain-induced barrier lowering coefficient.
eta	0.3 1/V	Effective drain voltage coefficient.
litl	(m)	Depth of current path.
vfb	-1.0 V	Flat-band voltage.

© 2023 Cadence Design Systems, Inc.

vbx	(V)	Threshold voltage transition body voltage.
vbi	(V)	Substrate junction built-in potential.
vbm	-5 V	Maximum applied body voltage.
dvt0	2.2	First coefficient of short-channel effects.
dvt1	0.53	Second coefficient of short-channel effects.
dvt2	-0.032 1/V	Body-bias coefficient of short-channel effects.
a0	1 for nmos and 4.4 for pmos	Nonuniform depletion width effect coefficient.
a1	0 for nmos, 0.23 for pmos	No-saturation coefficient.
a2	1 for nmos, 0.08 for pmos	No-saturation coefficient.
keta	-0.047 1/V	Body-bias coefficient for non-uniform depletion width effect.

© 2023 Cadence Design Systems, Inc.

Process *parameters*

nsub	2e15 cm^{-3}	Substrate doping concentration.
npeak	1.7e17 cm^{-3}	Peak channel doping concentration.
ngate	(cm^{-3})	Poly-gate doping concentration.
xj	0.15e-6 m	Source/drain junction depth.
dl	0 m	Lateral diffusion for one side.
dw	0 m	Width reduction for one side.
tox	1.5e-8 m	Gate oxide thickness.
vdd	5 V	Maximum drain voltage.
xt	1.55e-7 m	Doping depth.
ldd	0 m	Total length of lightly doped drain region.
rds0	0 Ω	Total drain-source resistance.
rdsw	0 Ω μm	Width dependence of drain-source resistance.

Mobility *parameters*

uo	670 cm^2/V s	Low-field surface mobility at tnom. Default is 250 for PMOS.
vsat	9.58e4 m/s	Carrier saturation velocity at tnom.

© 2023 Cadence Design Systems, Inc.

ua	2.25e-9 m/v	First-order mobility reduction coefficient.
ub	5.87e-19 m^2/v^2	Second-order mobility reduction coefficient.
uc	0.0465 1/V	Body-bias dependence of mobility.
uc0	0	Mobility coefficient.

© 2023 Cadence Design Systems, Inc.

Output resistance *parameters*

satmod	2	Saturation model selector.
bulkmod	1	Bulk-charge effect model selector.
drout	0.56	DIBL effect on output resistance coefficient.
alpha	1.9	Reference voltage multiplication factor.
em	4.1e7 V/m	Maximum electric field.
pclm	1.3	Channel length modulation coefficient.
pdibl1	0.39	First coefficient of drain-induced barrier lowering.
pdibl2	8.6e-3	Second coefficient of drain-induced barrier lowering.
pscbe1	4.24e8 V/m	First coefficient of substrate current body effect.
pscbe2	1e-5 m/v	Second coefficient of substrate current body effect.
pvag	0	Gate dependence of Early voltage.

Subthreshold *parameters*

subthmod	2	Subthreshold model selector.
vghigh	0.12 V	Upper bound of transition region.
vglow	-0.12 V	Lower bound of transition region.
cdsc	2.4e-4 F/m^2	Source/drain and channel coupling capacitance.
cdscb	0 F/m^2 V	Body-bias dependence of cdsc.

© 2023 Cadence Design Systems, Inc.

`nfactor`	`1`	Subthreshold swing coefficient.
`cit`	`0 F`	Interface trap parameter for subthreshold swing.
`voff`	`-0.11 V`	Threshold voltage offset.
`dsub`	`drout`	DIBL effect in subthreshold region.
`eta0`	`0.08`	DIBL coefficient subthreshold region.
`etab`	`-0.07 1/V`	Body-bias dependence of `et0`.

© 2023 Cadence Design Systems, Inc.

Parasitic resistance *parameters*

rsh	0 Ω/sqr	Source/drain diffusion sheet resistance.
rs	0 Ω	Source resistance.
rd	0 Ω	Drain resistance.
lgcs	0 m	Gate-to-contact length of source side.
lgcd	0 m	Gate-to-contact length of drain side.
rsc	0 Ω	Source contact resistance.
rdc	0 Ω	Drain contact resistance.
rss	0 Ω m	Scalable source resistance.
rdd	0 Ω m	Scalable drain resistance.
sc	infinity m	Spacing between contacts.
ldif	0 m	Lateral diffusion beyond the gate.
hdif	0 m	Length of heavily doped diffusion.
minr	0.1 Ω	Minimum source/drain resistance.

Junction diode model *parameters*

js	(A/m^2)	Bulk junction reverse saturation current density.
is	1e-14 A	Bulk junction reverse saturation current.
n	1	Junction emission coefficient.

© 2023 Cadence Design Systems, Inc.

`dskip`	`yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`.Possible values are no and yes.
`imelt`	`` `imaxA' ``	Explosion current.
`jmelt`	`` `jmaxA/m'^2 ``	Explosion current density.

© 2023 Cadence Design Systems, Inc.

Overlap capacitance *parameters*

cgso	(F/m)	Gate-source overlap capacitance.
cgdo	(F/m)	Gate-drain overlap capacitance.
cgbo	(F/m)	Gate-bulk overlap capacitance.
meto	0 m	Metal overlap in fringing field.

Junction capacitance model *parameters*

cbs	0 F	Bulk-source zero-bias junction capacitance.
cbd	0 F	Bulk-drain zero-bias junction capacitance.
cj	5e-4 F/ m^2	Zero-bias junction bottom capacitance density.
mj	1/2	Bulk junction bottom grading coefficient.
pb	0.8 V	Bulk junction built-in potential.
fc	0.5	Forward-bias depletion capacitance threshold.
cjsw	5e-10 F/ m	Zero-bias junction sidewall capacitance density.
mjsw	1/3	Bulk junction sidewall grading coefficient.
pbsw	0.8 V	Side-wall junction built-in potential.
fcsw	0.5	Side-wall forward-bias depletion capacitance threshold.

© 2023 Cadence Design Systems, Inc.

Charge model selection *parameters*

`capmod`	`yang`	Intrinsic charge model.Possible values are none, meyer, yang and bsim.
`xpart`	`1`	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
`xqc`	`0`	Drain/source channel charge partition in saturation for charge models, e.g. use 0.4 for 40/60, 0.5 for 50/50, 0 for 0/100.

Default instance *parameters*

`w`	`5e-6 m`	Default channel width.
`l`	`5e-6 m`	Default channel length.
`as`	`0 m`^{2}	Default area of source diffusion.
`ad`	`0 m`^{2}	Default area of drain diffusion.
`ps`	`0 m`	Default perimeter of source diffusion.
`pd`	`0 m`	Default perimeter of drain diffusion.
`nrd`	`0 m/m`	Default number of squares of drain diffusion.
`nrs`	`0 m/m`	Default number of squares of source diffusion.

Temperature effects *parameters*

`tnom`	`(C)`	Parameters measurement temperature. Default set by `options`.

© 2023 Cadence Design Systems, Inc.

trise	0 C	Temperature rise from ambient.
tlev	0	DC temperature selector.
tlevc	0	AC temperature selector.
eg	1.12452 V	Energy band gap.
gap1	7.02e-4 V/C	Band gap temperature coefficient.
gap2	1108 C	Band gap temperature offset.
kt1	-0.11 V	Temperature coefficient for threshold voltage.
kt1l	-1.86e-7 v m	Temperature coefficient for threshold voltage.
kt2	0.022	Temperature coefficient for threshold voltage.
at	3.3e4 m/s	Temperature coefficient for vsat.
ua1	4.31e-9 m/v	Temperature coefficient for ua.
ub1	-7.61e-18 m^2/v^2	Temperature coefficient for ub.
uc1	-0.056 1/V	Temperature coefficient for uc.
trs	0 1/C	Temperature parameter for source resistance.
trd	0 1/C	Temperature parameter for drain resistance.
ute	-1.5	Mobility temperature exponent.

© 2023 Cadence Design Systems, Inc.

`xti`	`3`	Saturation current temperature exponent.
`ptc`	`0 V/C`	Surface potential temperature coefficient.
`tcv`	`0 V/C`	Threshold voltage temperature coefficient.
`pta`	`0 V/C`	Junction potential temperature coefficient.
`ptp`	`0 V/C`	Sidewall junction potential temperature coefficient.
`cta`	`0 1/C`	Junction capacitance temperature coefficient.
`ctp`	`0 1/C`	Sidewall junction capacitance temperature coefficient.

© 2023 Cadence Design Systems, Inc.

Noise model *parameters*

noisemod	1	Noise model selector.
kf	0	Flicker (1/f) noise coefficient.
af	1	Flicker (1/f) noise exponent.
ef	1	Flicker (1/f) noise frequency exponent.
wnoi	1e-5 m	Channel width at which noise parameters were extracted.
a	1e16 for nmos and 9.9e14 for pmos	Oxide trap density coefficient.
b	5e4 for nmos and 2.4e3 for pmos	Oxide trap density coefficient.
c	-1.4e-8 for nmos and 1.4e-8 for pmos	Oxide trap density coefficient.

Operating region warning control *parameters*

alarm	none	Forbidden operating region.Possible values are none, off, triode, sat, subth and rev.
imax	1 A	Maximum allowable current.
jmax	1e8 A/m^2	Maximum allowable current density.

© 2023 Cadence Design Systems, Inc.

`bvj`	`infinity V`	Junction reverse breakdown voltage.
`vbox`	`1e9*tox V`	Oxide breakdown voltage.
`maxvp`	`1.12 V`	Maximum allowable voltage across the gate poly layer.

© 2023 Cadence Design Systems, Inc.

Compatibility model *parameters*

compatible	spectre	Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax.Possible values are spectre, spice2, spice3, cdsspice, hspice, spiceplus, eldo, sspice, mica, tispice and pspice.

Auto Model Selector *parameters*

wmax	1.0 m	Maximum channel width for which the model is valid.
wmin	0.0 m	Minimum channel width for which the model is valid.
lmax	1.0 m	Maximum channel length for which the model is valid.
lmin	0.0 m	Minimum channel length for which the model is valid.

Junction *model*

acm	12	Junction area calculation method selector.
jsw	0.0 A/m	Sidewall bulk junction saturation current density.
nds	1.0	Reverse bias slope coefficient.
vnds	-1.0 V	Reverse diode current transition point.
cjgate	`cjswF/m'	Zero bias gate-edge sidewall bulk junction capacitance density.
php	pb V	Bulk junction sidewall contact potential.

© 2023 Cadence Design Systems, Inc.

tt	0.0 s	Transit time.
ld	(m)	Lateral diffusion into the channel from the source and drain diffusion.
wmlt	1.0	Width diffusion layer shrink reduction factor.
ijth	1.0 A	Explosion current.

Imax and Imelt:

The imax parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to imax. If imax is exceeded during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding imax, the results are inaccurate, and Spectre prints a warning.

A separate model parameter, imelt, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds imelt, the base and collector currents are composed of many exponential terms, Spectre issues a warning and the results become inaccurate. The junction current is linearized above the value of imelt to prevent arithmetic exception, with the exponential term replaced by a linear equation at imelt.

Both of these parameters have current density counterparts, jmax and jmelt, that you can specify if you want the absolute current values to depend on the device area.

Auto Model Selection:

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters lmax, lmin, wmax, and wmin should be given. The selection criteria to choose a model is as follows:

```
lmin <= inst_length < lmax  and   wmin <= inst_width  < wmax
```


© 2023 Cadence Design Systems, Inc.

Example:

```
model ModelName ModelType {
   1:     <model parameters> lmin=2 lmax=4 wmin=1 wmax=2
   2:     <model parameters> lmin=1 lmax=2 wmin=2 wmax=4
   3:     <model parameters> lmin=2 lmax=4 wmin=4 wmax=6
}
```

Then for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

Output Parameters

`weff`	(m)	Effective channel width.
`leff`	(m)	Effective channel length.
`rseff`	(Ω)	Effective source resistance.
`rdeff`	(Ω)	Effective drain resistance.

Related Topics

MOS Level-2 Model (mos2)

MOS Level-3 Model (mos3)

BSIM1 Level-4 Model (bsim1)

BSIM2 Level-5 Model (bsim2)

© 2023 Cadence Design Systems, Inc.

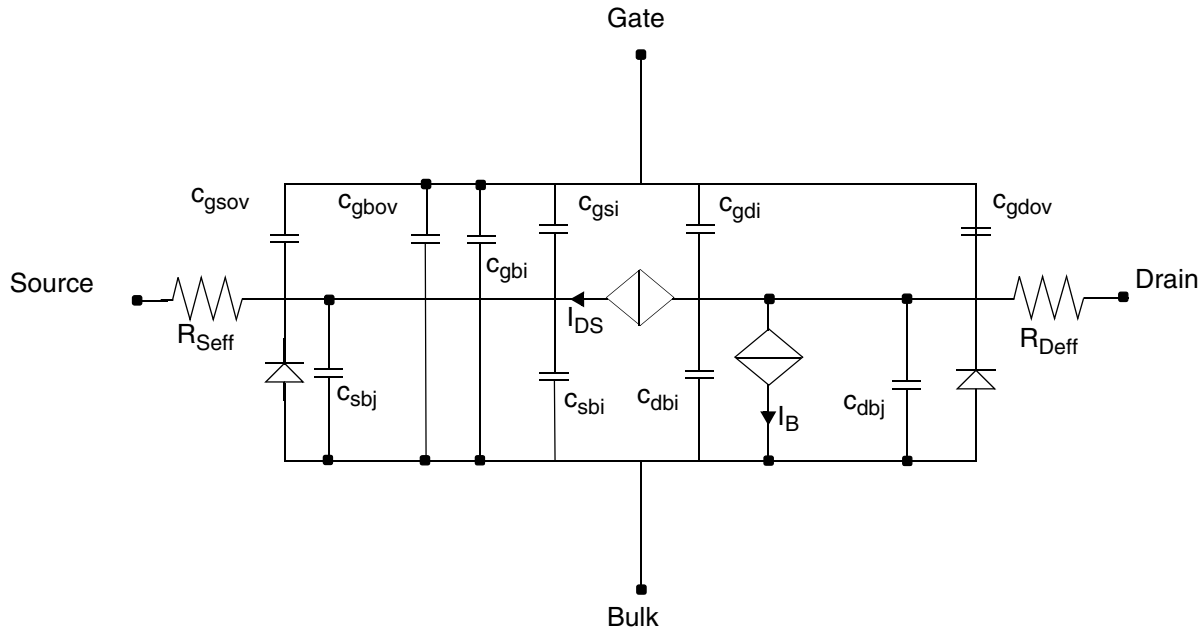
21

BSIM3v3 Level-11 Model (bsim3v3)

The BSIM3v3 model is based on the industry standard efforts of the Compact Modeling Counsel (CMC) and the BSIM modeling group at the University of California, Berkeley. The available versions for BSIM3v3 model are 3.1, 3.2, 3.21, 3.22, 3.23, 3.24, and 3.3. Click the following links to view information about the BSIM3v3 model:

- Spectre-Specific Parameters
- I-V Model
- Capacitance Model
- Nonquasi-static (NQS) Model
- SPICE3 Junction Diode Model
- Flicker Noise
- Channel Thermal Noise
- Default Model Parameter Value Calculation
- Gate Leak Currents
- LOD Model
- Differences between BSIM3v3 Subversions
- Parameter Differences between BSIM3v3 Levels
- Scaling Effects (BSIM3v3)
- Component Statements
- Binning Parameters

© 2023 Cadence Design Systems, Inc.



Spectre-Specific Parameters

Some of the following parameters are left in the model for backward compatibility to other Spectre® circuit simulator models.

Instance Parameters

The instance parameters mentioned in the table below help you in performing mismatch analyses. They represent the statistical variation of the threshold voltage (vth0), the mobility (u0), the body bias coefficient (k1) and the subthreshold swing factor (Nfactor). These parameters are implemented in the following manner:

Parameter	Unit	Description
`Delvto`	`v`	shift in zero-bias threshold voltage vth0. Default value is `0.0`.
`Nulmu0`		Mobility multiplier. Default value is `1.0`.
`Delk1`	$v^{1/2}$	shift in body bias coefficient k1. Default value is `0.0`.
`Delnfct`		Shift in subthreshold swing factor. Default value is `0.0`.

© 2023 Cadence Design Systems, Inc.

The checking of these parameters is as follows:

- If Mulu0 < 0.0 and Paramchk returns a warning message, reset Nulmu0 to 1.0.
- If Delk1 < -K1 (after binning) and Paramchk returns a warning message, reset Delk1 to 0.0.

The parameters are added whether Vto and K1 are given (specified by you or computed internally when not specified). Mulmu0 is multiplied after binning.

Model Parameters

Parameter	Description
`ad`	Area of drain diffusion. This is an instance parameter in Spice, but may be specified as a model parameter in Spectre.
`alarm`	Forbidden operating region. Can be set to `none`, `off`, `triode`, `sat`, `subth`, or `rev`. Spectre will issue a warning if your device's operating point enters this region.
`as`	Area of source diffusion. This is an instance parameter in Spice, but may be specified as a model parameter in Spectre.
`bvj`	The junction reverse breakdown voltage. Spectre checks this at the DC operating point, and also on each step of the transient simulation. Spectre issues a warning if the bulk-drain voltage exceeds this voltage.
`cbd`	Bulk-drain zero bias junction capacitance.
`cbs`	Bulk-drain zero bias junction capacitance.
`cta`	Junction capacitance temperature coefficient.
`ctp`	Sidewall junction capacitance temperature coefficient.
`diomod`	Controls the junction models. If `diomod=1` (default value), the Spectre junction model is used. The equations are described in *Chapter 12: Common MOSFET Equations*. If `diomod=0`, the Berkeley BSIM3v3 junction model is used.
`drout`	DIBL effect on rout coefficient.
`dskip`	Allows the substitution of a simple `pwl` model for the diode current if it falls below 0.1*iabstol.
`eg`	Energy band gap.

© 2023 Cadence Design Systems, Inc.

`fc`	Forward bias depletion capacitance threshold.
`fcsw`	Sidewall forward bias depletion capacitance threshold.
`gap1`	Band gap temperature coefficient.
`gap2`	Bandgap temp offset.
`hdif`	Length of heavily doped diffusion.
`imax`	Maximum current.
`imelt`	Explosion current. The junction current is linearized after this current is exceeded.
`jmax`	Maximum current density.
`jmelt`	Explosion current density.
`is`	Bulk-junction reverse saturation current.
`l`	Default channel length, if not specified on the instance.
`ldif`	Lateral diffusion beyond the gate.
`lgcs`	Gate to contact length of source.
`lgcd`	Gate to contact length of drain.
`meto`	Metal overlap in fringing field.
`minr`	Minimum resistance.
`nrd`	Default number of drain squares. This is an instance parameter also.
`nrs`	Default number of source squares. This is an instance parameter also.
`pd`	Drain perimeter. This is an instance parameter also.
`ps`	Source perimeter. This is an instance parameter also.
`pta`	Junction potential temperature coefficient.
`ptp`	Sidewall junction potential temperature coefficient.
`rd`	Drain resistance.
`rdc`	Drain contact resistance.
`rdd`	Scalable drain resistance.
`rs`	Source resistance.
`rsc`	Source contact resistance.

© 2023 Cadence Design Systems, Inc.

`rss`	Scalable source resistance.
`sc`	Contact spacing.
`tlev`	DC temperature selector.
`tlevc`	AC temperature selector.
`trd`	Temperature param for drain resistance.
`trise`	Temperature rise from ambient.
`trs`	Temperature param for source resistance.
`type`	Specifies `nmos` or `pmos`, since the primitive name is bsim3v3.
`xl`	Length variation from masking and etching.
`xw`	Width variation from masking and etching.
`w`	Default channel width, if not specified on the instance.
`warn`	Parameter to turn warnings off and on.
`wnoi`	Channel width at which noise parameters extracted.
`vbox`	Oxide breakdown voltage.

Note: `n` in the Spectre® circuit simulator is `nj` in Berkeley. `nqsmod` is an instance parameter for Berkeley, but both an instance and model parameter for the Spectre circuit simulator. `level=11` in the Spectre simulator, but `level=8` in Berkeley. The `ijth` parameter (diode-limiting current) is aliased to the Spectre simulator's `imelt` parameter. Some of the Spectre-specific parameters can affect the behavior of the model in such a way to make the model incompatible with other simulators. Cadence recommends that care be taken when using these parameters.

See `spectre -h bsim3v3` for more details about these parameters.

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

Drain and Source Area

I-V Model

Nonquasi-static (NQS) Model

SPICE3 Junction Diode Model

© 2023 Cadence Design Systems, Inc.

Drain and Source Area

The drain and source areas are calculated in the order shown in the following equations.

Drain and Source Perimeters

The drain and source perimeters are calculated in the order shown in the following equations:

(21-1)

$$\text{Drain perimeter} = \begin{cases} pd & \text{if } pd \text{ is given} \\ 4hidif*scalem + 2W_{scaled} & \text{if } hidif \text{ is given} \\ 2\cdot(W_{eff}+ld) & \text{if } ld \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

(21-2)

$$\text{Source perimeter} = \begin{cases} ps & \text{if } ps \text{ is given} \\ 4hidif*scalem + 2W_{scaled} & \text{if } hidif \text{ is given} \\ 2\cdot(W_{eff}+ls) & \text{if } ls \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

Note: The ld (length of drain) parameter is an instance parameter that is different from the model parameter ld (lateral diffusion) used in calculating L_{eff}.

Drain and Source Parasitic Resistance

(21-3)

© 2023 Cadence Design Systems, Inc.

$$\text{Drain area} = \begin{cases} ad & \text{if } ad \text{ is given} \\ 2hidif * scalem * W_{scaled} & \text{if } hidif \text{ is given} \\ W_{eff} * ld & \text{if } ld \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

(21-4)

$$\text{Source area} = \begin{cases} as & \text{if } as \text{ is given} \\ 2hidif * scalem * W_{scaled} & \text{if } hidif \text{ is given} \\ W_{eff} * ls & \text{if } ls \text{ is given} \\ 0 & \text{otherwise} \end{cases}$$

Note: The ld (length of drain) parameter is an instance parameter that is different from the model parameter ld (lateral diffusion) used in calculating L_{eff}.

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

LOD Model

I-V Model

Nonquasi-static (NQS) Model

SPICE3 Junction Diode Model

© 2023 Cadence Design Systems, Inc.

I-V Model

Threshold Voltage

(21-5)

$$V_{TH} = V_{tho} + K_1(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) - K_2 V_{bseff}$$
$$+ K_1\left(\sqrt{1 + \frac{N_{lx}}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + (K_3 + K_{3b}V_{bseff}) \times \frac{T_{ox}}{W'_{eff} + W_0}\Phi_s -$$
$$D_{vtow}\left(\exp\left(-D_{vt1w}\frac{W_{eff}L_{eff}}{2l_{tw}}\right) + 2\exp\left(-D_{vt1w}\frac{W_{eff}L_{eff}}{l_{tw}}\right)\right)(V_{bi} - \Phi_s)$$
$$- D_{vto}\left(\exp\left(-D_{vt1}\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-D_{vt1}\frac{L_{eff}}{l_t}\right)\right)(V_{bi} - \Phi_s)$$
$$-\left(\exp\left(-D_{sub}\frac{L_{eff}}{2l_{to}}\right) + 2\exp\left(-D_{sub}\frac{L_{eff}}{l_{to}}\right)\right)(E_{tao} + E_{tab}V_{bseff})V_{ds}$$

where

(21-6)

$$l_t = \sqrt{\varepsilon_{si}X_{dep}/C_{ox}}(1 + D_{vt2}V_{bseff})$$

(21-7)

$$l_{tw} = \sqrt{\varepsilon_{si}X_{dep}/C_{ox}}(1 + D_{vt2w}V_{bseff})$$

(21-8)

$$l_{to} = \sqrt{\varepsilon_{si}X_{dep0}/C_{ox}}$$

(21-9)

© 2023 Cadence Design Systems, Inc.

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}(\Phi_s - V_{bseff})}{qN_{ch}}}$$

(21-10)

$$X_{dep0} = \sqrt{\frac{2\varepsilon_{si}\Phi_s}{qN_{ch}}}$$

(21-11)

$$V_{bseff} = V_{bc} + 0.5\left[V_{bs} - V_{bc} - \delta_1 + \sqrt{(V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 V_{bc}}\right] \quad (\delta 1 = 0.001)$$

(21-12)

$$V_{bc} = 0.9\left(\Phi_s - \frac{K_1^2}{4K_2^2}\right)$$

(21-13)

$$V_{bi} = V_t \times \ln\left[\frac{N_{ch}N_{DS}}{n_i^2}\right]$$

(21-14)

$N_{DS} = 10^{20}$, $V_t = \frac{kT}{q}$, the thermal voltage

Effective Vgs-Vthc

(21-15)

© 2023 Cadence Design Systems, Inc.

$$V_{gsteff} = \frac{2nv_t \ln\left[1 + \exp\left(\frac{V_{gs} - V_{th}}{2nv_t}\right)\right]}{1 + 2nC_{ox}\sqrt{\frac{2\Phi_s}{q\varepsilon_{si}N_{ch}}}\exp\left(-\frac{V_{gs} - V_{th} - 2V_{off}}{2nv_t}\right)}$$

(21-16)

$$n = 1 + N_{factor}\frac{C_d}{C_{ox}} + \frac{(C_{dsc} + C_{dscd}V_{ds} + C_{dscb}V_{bseff})\left(\exp\left(-D_{vt1}\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-D_{vt1}\frac{L_{eff}}{l_t}\right)\right)}{C_{ox}} + \frac{C_{it}}{C_{ox}}$$

(21-17)

$$C_d = \frac{\varepsilon_{si}}{X_{dep}}$$

Mobility

For `Mobmod`=1,

(21-18)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})\left(\frac{V_{gsteff} + 2V_{th}}{T_{ox}}\right) + U_b\left(\frac{V_{gsteff} + 2V_{th}}{T_{ox}}\right)^2}$$

For `Mobmod`=2,

(21-19)

© 2023 Cadence Design Systems, Inc.

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})\left(\frac{V_{gsteff}}{T_{ox}}\right) + U_b\left(\frac{V_{gsteff}}{T_{ox}}\right)^2}$$

For `Mobmod`=3,

(21-20)

$$\mu_{eff} = \frac{\mu_o}{1 + \left[U_a\left(\frac{V_{gsteff} + 2V_{th}}{T_{ox}}\right) + U_b\left(\frac{V_{gsteff} + 2V_{th}}{T_{ox}}\right)^2\right](1 + U_c V_{bseff})}$$

Drain Saturation Voltage

For $R_{ds} > 0$ or $\lambda \neq 1$,

(21-21)

$$V_{DSAT} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

(21-22)

$$a = A_{bulk}^2 W_{eff} v_{sat} C_{ox} R_{ds} + \left(\frac{1}{\lambda} - 1\right) A_{bulk}$$

(21-23)

$$b = -\left((V_{gsteff} + 2v_t)\left(\frac{2}{\lambda} - 1\right) + A_{bulk} E_{sat} L_{eff} + 3A_{bulk}(V_{gsteff} + 2v_t) W_{eff} v_{sat} C_{ox} R_{ds}\right)$$

(21-24)

$$c = (V_{gsteff} + 2v_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff} v_{sat} C_{ox} R_{ds}$$

(21-25)

© 2023 Cadence Design Systems, Inc.

$$\lambda = A_1 V_{gsteff} + A_2$$

For R_{ds} = 0 and $\lambda = 1$,

(21-26)

$$V_{DSAT} = \frac{E_{sat} L_{eff} (V_{gsteff} + 2v_t)}{A_{bulk} E_{sat} L_{eff} + (V_{gsteff} + 2v_t)}$$

(21-27)

$$A_{bulk} = \left(1 + \frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\left\{\frac{A_o L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}}\left[1 - A_{gs} V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}}\right)^2\right] + \frac{B_o}{Weff + B_1}\right\}\right)\frac{1}{1 + K_{eta} V_{bseff}}$$

(21-28)

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}}$$

Effective Vds

(21-29)

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right)$$

Drain Current Expression

(21-30)

$$I_{DS} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds} I_{dso(Vdseff)}}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_a}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ascbe}}\right)$$

© 2023 Cadence Design Systems, Inc.

(21-31)

$$I_{dso} = I_{dso} = \frac{W_{eff}\mu_{eff}C_{ox}V_{gsteff}\left(1 - A_{bulk}\frac{V_{dseff}}{2(V_{gsteff} + 2v_t)}\right)V_{dseff}}{L_{eff}[1 + V_{dseff}/(E_{sat}L_{eff})]}$$

(21-32)

$$V_a = V_{asat} + \left(1 + \frac{P_{vag}V_{gsteff}}{E_{sat}L_{eff}}\right)\left(\frac{1}{V_{aclm}} + \frac{1}{V_{adiblc}}\right)^{-1}$$

(21-33)

$$V_{aclm} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{P_{clm}A_{bulk}E_{sat}L_{itl}}(V_{ds} - V_{dseff})$$

(21-34)

$$V_{adiblc} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + P_{diblcb}V_{bseff})}\left(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat} + V_{gsteff} + 2v_t}\right)$$

(21-35)

$$\theta_{rout} = P_{diblc1}\left[\exp\left(-D_{rout}\frac{L_{eff}}{2l_{t0}}\right) + 2\exp\left(-D_{rout}\frac{L_{eff}}{l_{t0}}\right)\right] + P_{diblc2}$$

(21-36)

$$\frac{1}{V_{ascbe}} = \frac{p_{scbe2}}{L_{eff}}\exp\left(\frac{-P_{scbe1}L_{itl}}{V_{ds} - V_{dseff}}\right)$$

(21-37)

© 2023 Cadence Design Systems, Inc.

$$V_{asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{ds}v_{sat}C_{ox}W_{eff}V_{gsteff}\left[1 - \frac{A_{bulk}V_{dsat}}{2(V_{gsteff} + 2v_t)}\right]}{2/\lambda - 1 + R_{ds}v_{sat}C_{ox}W_{eff}A_{bulk}}$$

(21-38)

$$L_{itl} = \sqrt{\frac{\varepsilon_{si}T_{ox}X_j}{\varepsilon_{ox}}}$$

Substrate Current

(21-39)

$$I_{sub} = \frac{\alpha}{L_{eff}}(V_{ds} - V_{dseff})\exp\left(-\frac{\beta_o}{V_{ds} - V_{dseff}}\right)\frac{I_{dso}}{1 + \frac{R_{ds}I_{dso}}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_a}\right)$$

(21-40)

$$\alpha = \alpha_0 + \alpha_1 L_{eff}$$

Junction Saturation Current

is always overrides *js*. If you give *js* but not *is*, the saturation currents are calculated from *js* and the source and drain areas.

$$\text{Drain saturation current} = \begin{cases} is & \text{if } is \text{ is given} \\ js * ad + jsw \times pd & \text{otherwise} \end{cases}$$

$$\text{Source saturation current} = \begin{cases} is & \text{if } is \text{ is given} \\ js * as + jsw \times ps & \text{otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Polysilicon Depletion Effect

(21-41)

$$V_{poly} = \frac{1}{2}X_{poly}E_{poly} = \frac{qN_{gate}X_{poly}^2}{2\varepsilon_{si}}$$

(21-42)

$$\varepsilon_{ox}E_{ox} = \varepsilon_{si}E_{poly} = \sqrt{2q\varepsilon_{si}N_{gate}V_{poly}}$$

(21-43)

$$V_{gs} - V_{fb} - \Phi_s = V_{poly} + V_{ox}$$

(21-44)

$$a(V_{gs} - V_{fb} - \Phi_s - V_{poly})^2 - V_{poly} = 0$$

(21-45)

$$a = \frac{\varepsilon_{ox}^2}{2q\varepsilon_{si}N_{gate}T_{ox}^2}$$

(21-46)

$$V_{gs_eff} = V_{fb} + \Phi_s + \frac{q\varepsilon_{si}N_{gate}T_{ox}^2}{\varepsilon_{ox}^2}\left(\sqrt{1 + \frac{2\varepsilon_{ox}^2(V_{gs} - V_{FB} - \Phi_s)}{q\varepsilon_{si}N_{gate}T_{ox}^2}} - 1\right)$$

Effective Channel Length and Width

(21-47)

$$L_{eff} = L_{drawn} - 2dL$$

© 2023 Cadence Design Systems, Inc.

where

(21-48)

$$L_{drawn} = L(given) \times scale + xl \times scalem$$

(21-49)

$$W_{eff} = W_{drawn} - 2dW$$

(21-50)

$$W_{eff}' = W_{drawn} - 2dW'$$

(21-51)

$$dW = dW' + dW_g V_{gsteff} + dW_b(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s})$$

(21-52)

$$dW' = W_{\text{int}} + \frac{W_l}{L^{W_{\ln}}} + \frac{W_w}{W^{W_{wn}}} + \frac{W_{wl}}{L^{W_{\ln}} W^{W_{wn}}}$$

(21-53)

$$dL = L_{\text{int}} + \frac{L_l}{L^{L_{\ln}}} + \frac{L_w}{W^{L_{wn}}} + \frac{L_{wl}}{L^{L_{\ln}} W^{L_{wn}}}$$

(21-54)

$$W_{effc} = W_{drawn} - dWC$$

Drain/Source Resistance

(21-55)

© 2023 Cadence Design Systems, Inc.

$$R_{ds} = \frac{R_{dsw}[1 + P_{rwg}V_{gsteff} + P_{rwb}(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s})]}{(10^6 W_{eff}')^{Wr}}$$

Temperature Effects

(21-56)

$$V_{th(T)} = V_{th}(T_{nom}) + (K_{t1} + K_{t1l}/L_{eff} + K_{t2}V_{bseff})\left(\frac{T}{T_{nom}} - 1\right)$$

(21-57)

$$\mu_{o(T)} = \mu_o(T_{nom})\left(\frac{T}{T_{nom}}\right)^{U_{te}}$$

(21-58)

$$v_{sat(T)} = v_{sat}(T_{nom}) - A_t\left(\frac{T}{T_{nom}} - 1\right)$$

(21-59)

$$R_{dsw(T)} = R_{dsw}(T_{nom}) + P_{rt}\left(\frac{T}{T_{nom}} - 1\right)$$

(21-60)

$$U_{a(T)} = U_a(T_{nom}) + U_{a1}\left(\frac{T}{T_{nom}} - 1\right)$$

(21-61)

$$U_{b(T)} = U_b(T_{nom}) + U_{b1}\left(\frac{T}{T_{nom}} - 1\right)$$

(21-62)

© 2023 Cadence Design Systems, Inc.

$$U_{c(T)} = U_c(T_{nom}) + U_{c1}\left(\frac{T}{T_{nom}} - 1\right)$$

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

LOD Model

Capacitance Model

Nonquasi-static (NQS) Model

SPICE3 Junction Diode Model

Capacitance Model

Dimension Dependence

(21-63)

$$L_{active} = L_{drawn} - 2\delta L_{eff}$$

(21-64)

$$\delta L_{eff} = D_{lc} + \frac{L_{lc}}{L^{L_{ln}}} + \frac{L_{wc}}{W^{L_{wn}}} + \frac{L_{wlc}}{L^{L_{ln}} W^{L_{wn}}}$$

(21-65)

$$W_{active} = W_{drawn} - 2\delta W_{eff}$$

(21-66)

$$\delta W_{eff} = D_{wc} + \frac{W_{lc}}{L^{W_{ln}}} + \frac{W_{wc}}{W^{W_{wn}}} + \frac{W_{wlc}}{L^{W_{ln}} W^{W_{wn}}}$$

© 2023 Cadence Design Systems, Inc.

Junction Capacitance

If pd > W_{eff},

(21-67)

$$cd = ad \times cjbs + pd \times cjbssw - W_{eff} \times cjbssw + W_{eff} \times cjbsswg$$

otherwise

(21-68)

$$cd = ad \times cjbs + pd \times cjbssw$$

where

cjbs is a function of cj, mj, and pb

cjbssw is a function of cjsw, mjsw, and pbsw

cjbsswg is a function of cjswg, mjswg, and pbswg

Overlap Capacitance (for NMOS)

(21-69)

$$OverlapCgs = \begin{cases} C_{gso} & \text{if } cgso \text{ is given} \\ (dlc + meto) \times C_{ox} - C_{gsl} & \text{if } dlc \text{ is given and dlc>0} \\ 0.6 \dot{\times} X_j \times C_{ox} & \text{otherwise} \end{cases}$$

(21-70)

© 2023 Cadence Design Systems, Inc.

$$OverlapCgd = \begin{cases} C_{gdo} & \text{if } cgdo \text{ is given} \\ (dlc + meto) \times C_{ox} - C_{gdl} & \text{if } dlc \text{ is given and dlc>0} \\ 0.6 \times X_j \times C_{ox} & \text{otherwise} \end{cases}$$

(21-71)

$$OverlapCgb = \begin{cases} C_{gbo} & \text{if } cgso \text{ is given} \\ 2.0 \times dwc \times C_{ox} & \text{otherwise} \end{cases}$$

If OverlapCgs/OverlapCgd < 0, OverlapCgs/OverlapCgd=1.0e-7*Tox

OverlapCgb<0, OverlapCgb=0

Source Overlap Capacitance

For `capmod`=0,

(21-72)

$$Q_{overlap,s} = C_{gso} V_{gs} W_{active}$$

For `capmod`=1,

if (V_{gs} < 0),

(21-73)

$$Q_{overlap,s} = \left[C_{gso} V_{gs} + \frac{C_{kappa} C_{gsl}}{2} \left(-1 + \sqrt{1 - \frac{4 V_{gs}}{C_{kappa}}} \right) \right] W_{active}$$

else

© 2023 Cadence Design Systems, Inc.

(21-74)

$$Q_{overlap,\,s} = [(C_{gso} + C_{kappa}C_{gsl})V_{gs}]W_{active}$$

For `capmod`=2,

$$Q_{overlap,\,s} = \left[C_{gso}V_{gs} + C_{gsl}\left\{V_{gs} - V_{gs,\,overlap} + \frac{C_{kappa}}{2}\left(-1 + \sqrt{1 + \frac{4V_{gs,\,overlap}}{C_{kappa}}}\right)\right\}\right] W_{active}$$

(21-75)

$$V_{gs,\,overlap} = \frac{1}{2}\left\{(V_{gs} + \delta_1) - \sqrt{(V_{gs} + \delta_1)^2 + 4\delta_1}\right\} \qquad where \quad \delta_1 = 0.02$$

Drain Overlap Capacitance

For `capmod`=0,

(21-76)

$$Q_{overlap,\,d} = C_{gdo}V_{gd}W_{active}$$

For `capmod`=1,

if ($V_{gd} < 0$),

(21-77)

$$Q_{overlap,\,d} = \left[C_{gdo}V_{gd} + \frac{C_{kappa}C_{gdl}}{2}\left(-1 + \sqrt{1 - \frac{4V_{gd}}{C_{kappa}}}\right)\right] W_{active}$$

else

(21-78)

© 2023 Cadence Design Systems, Inc.

$$\frac{Q_{overlap,\,d}}{W_{active}} = (C_{gdo} + C_{kappa}C_{gdl})V_{gd}$$

For `capmod`=2 or 3,

(21-79)

$$QQ_{overlap,\,d} = \left[C_{gdo}V_{gd} + C_{gdl}\left\{ V_{gd} - V_{gd,\,overlap} + \frac{C_{kappa}}{2}\left(-1 + \sqrt{1 + \frac{4V_{gd,\,overlap}}{C_{kappa}}} \right) \right\} W_{active} \right]$$

(21-80)

$$V_{gd,\,overlap} = \frac{1}{2}\left\{ (V_{gd} + \delta_1) - \sqrt{(V_{gd} + \delta_1)^2 + 4\delta_1} \right\} \qquad where \quad \delta_1 = 0.02$$

Gate Overlap Charge

(21-81)

$$Q_{overlap,\,g} = -(Q_{overlap,\,s} + Q_{overlap,\,d})$$

© 2023 Cadence Design Systems, Inc.

Intrinsic Charges

For capmod=0

Accumulation region ($V_{gs} < V_{fb} + V_{bs}$)

(21-82)

$$Q_g = W_{active} L_{active} C_{ox} (V_{gs} - V_{bs} - V_{fbcv})$$

(21-83)

$$Q_{sub} = -Q_g$$

(21-84)

$$Q_{inv} = 0$$

Subthreshold region ($V_{gs} < V_{th}$)

(21-85)

$$Q_b = -W_{active} L_{active} C_{ox} \frac{K_1^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{fbcv} - V_{bs})}{K_1^2}} \right)$$

(21-86)

$$Q_g = -Q_b$$

(21-87)

$$Q_{inv} = 0$$

Strong inversion ($V_{gs} > V_{th}$)

(21-88)

© 2023 Cadence Design Systems, Inc.

$$V_{dsat,cv} = \frac{V_{gs} - V_{th}}{A_{bulk}'}$$

(21-89)

$$A_{bulk}' = \begin{cases} A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{eff}}\right)^{C_{le}}\right) & \text{if version <= 3.1} \\ A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{active}}\right)^{C_{le}}\right) & \text{if version > 3.1} \end{cases}$$

(21-90)

$$A_{bulk0} = \left(1 + \frac{K_1}{2\sqrt{\Phi_s - V_{bs}}}\left\{\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}} + \frac{B_o}{W_{eff}' + B_1}\right\}\right)\frac{1}{1 + K_{eta} V_{bs}}$$

(21-91)

$$V_{TH} = V_{fbcv} + \Phi_s + K_1\sqrt{\Phi_s - V_{bs}}$$

50/50 Charge Partition

(21-92)

If $V_{ds} < V_{dsat'}$

(21-93)

$$Q_g = C_{ox} W_{active} L_{active}\left[V_{gs} - V_{fbcv} - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' \times V_{ds}^2}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2}\right)}\right]$$

(21-94)

© 2023 Cadence Design Systems, Inc.

$$Q_{inv} = -W_{active}L_{active}C_{ox}\left(V_{gs} - V_{th} - \frac{A_{bulk}' \times V_{ds}}{2} + \frac{A_{bulk}^2{}'V_{ds}^2}{12\left(V_{gs} - V_{th} + -\frac{A_{bulk}'}{2}V_{ds}\right)}\right)$$

(21-95)

$$Q_b = W_{active}L_{active}C_{ox}\left[V_{fbcv} - V_{th} + \Phi_s + \frac{(1 - A_{bulk}')V_{ds}}{2} - \frac{(1-A_{bulk}')A_{bulk}'V_{ds}^2}{12\left(V_{gs}-V_{th}-\frac{A_{bulk}'}{2}V_{ds}\right)}\right]$$

(21-96)

$$Q_s = Q_d = 0.5Q_{inv}$$

(21-97)

$$0.5Q_{inv} = -W_{active}L_{active}C_{ox}\left[V_{gs} - V_{th} - \frac{A_{bulk}'}{2}V_{ds} + \frac{A_{bulk}^2{}'V_{ds}^2}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2}V_{ds}\right)}\right]$$

otherwise,

(21-98)

$$Q_g = W_{active}L_{active}C_{ox}\left(V_{gs} - V_{fbcv} - \Phi_s - \frac{V_{dsat}}{3}\right)$$

(21-99)

$$Q_s = Q_d = -\frac{1}{3}W_{active}L_{active}C_{ox}(V_{gs} - V_{th})$$

(21-100)

$$Q_b = -W_{active}L_{active}C_{ox}\left(V_{fbcv} + \Phi_s - V_{th} + \frac{(1 - A_{bulk}')V_{dsat}}{3}\right)$$

© 2023 Cadence Design Systems, Inc.

40/60 Channel-Charge Partition

If $V_{ds} < V_{dsat}$,

(21-101)

$$Q_g = C_{ox} W_{active} L_{active} \left[V_{gs} - V_{fbcv} - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^2}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds} \right)} \right]$$

(21-102)

$$Q_{inv} = -W_{active} L_{active} C_{ox} \left[V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds} \right)} \right]$$

(21-103)

$$Q_b = W_{active} L_{active} C_{ox} \left[V_{fbcv} - V_{th} + \Phi_s + \frac{(1 - A_{bulk}') V_{ds}}{2} - \frac{(1 - A_{bulk}') A_{bulk}' V_{ds}^2}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds} \right)} \right]$$

(21-104)

$$Q_d = -W_{active} L_{active} C_{ox} \times$$

$$\left[\frac{V_{gs} - V_{th}}{2} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}' V_{ds} \times \left[\frac{(V_{gs} - V_{th})^2}{6} - \frac{A_{bulk}' V_{ds} (V_{gs} - V_{th})}{8} + \frac{A_{bulk}' V_{ds}^2}{40} \right]}{\left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds} \right)^2} \right]$$

© 2023 Cadence Design Systems, Inc.

(21-105)

$$Q_s = -(Q_g + Q_b + Q_d)$$

otherwise,

(21-106)

$$Q_g = W_{active} L_{active} C_{ox} \left(V_{gs} - V_{fbcv} - \Phi_s - \frac{V_{dsat}}{3} \right)$$

(21-107)

$$Q_d = -\frac{4}{15} W_{active} L_{active} C_{ox} (V_{gs} - V_{th})$$

(21-108)

$$Q_s = -(Q_g + Q_b + Q_d)$$

(21-109)

$$Q_b = -W_{active} L_{active} C_{ox} \left(V_{fbcv} + \Phi_s - V_{th} + \frac{(1 - A_{bulk}') V_{dsat}}{3} \right)$$

0/100 Channel-Charge Partition

If $V_{ds} < V_{dsat}$,

(21-110)

$$Q_g = C_{ox} W_{active} L_{active} \left[V_{gs} - V_{fbcv} - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^2}{12\Delta \left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds} \right)} \right]$$

(21-111)

© 2023 Cadence Design Systems, Inc.

$$Q_{inv} = -W_{active}L_{active}C_{ox}\left[V_{gs} - V_{th} - \frac{A_{bulk}'V_{ds}}{2} + \frac{A_{bulk}'^2V_{ds}^2}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2}V_{ds}\right)}\right]$$

(21-112)

$$Q_b = W_{active}L_{active}C_{ox}\left[V_{fbcv} - V_{th} + \Phi_s + \frac{(1 - A_{bulk}')V_{ds}}{2} - \frac{(1 - A_{bulk}')A_{bulk}'V_{ds}^2}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2}V_{ds}\right)}\right]$$

(21-113)

$$Q_d = -W_{active}L_{active}C_{ox}\left[\frac{V_{gs} - V_{th}}{2} + \frac{A_{bulk}'V_{ds}}{4} - \frac{(A_{bulk}'V_{ds})^2}{24\left(V_{gs} - V_{th} - \frac{A_{bulk}'}{2}V_{ds}\right)}\right]$$

(21-114)

$$Q_s = -(Q_g + Q_b + Q_d)$$

otherwise,

(21-115)

$$Q_g = W_{active}L_{active}C_{ox}\left(V_{gs} - V_{fbcv} - \Phi_s - \frac{V_{dsat}}{3}\right)$$

(21-116)

$$Q_b = -W_{active}L_{active}C_{ox}\left(V_{fbcv} + \Phi_s - V_{th} + \frac{(1 - A_{bulk}')V_{dsat}}{3}\right)$$

(21-117)

$$Q_d = 0$$

(21-118)

© 2023 Cadence Design Systems, Inc.

$$Q_s = -(Q_g + Q_b)$$

For capmod=1

if $V_{gs} < V_{fb} + V_{bs} + V_{gsteffcv}$,

(21-119)

$$Q_{g1} = -W_{active} L_{active} C_{ox} (V_{gs} - V_{fb} - V_{bs} - V_{gsteffcv})$$

else

(21-120)

$$Q_{g1} = W_{active} L_{active} C_{ox} \frac{K_1^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FB} - V_{gsteffcv} - V_{bs})}{K_1^2}} \right)$$

(21-121)

$$Q_{b1} = -Q_{g1}$$

(21-122)

$$V_{fb} = \begin{cases} V_{th} - \Phi_s - K_1 \sqrt{\Phi_s} & \text{if version} \leq 3.1 \text{ and version} = 3.2.1 \\ V_{th}(V_{bs} = 0) - \Phi_s - K_1 \sqrt{\Phi_s} & \text{if version} = 3.2 \text{ and version} = 3.2.2 \end{cases}$$

(21-123)

$$V_{dsat,cv} = \frac{V_{gsteffcv}}{A_{bulk}'}$$

(21-124)

© 2023 Cadence Design Systems, Inc.

$$A_{bulk}' = \begin{cases} A_{bulk0}\left(1+\left(\frac{C_{lc}}{L_{eff}}\right)^{C_{le}}\right) & \text{if version <= 3.1} \\ A_{bulk0}\left(1+\left(\frac{C_{lc}}{L_{active}}\right)^{C_{le}}\right) & \text{if version > 3.1} \end{cases}$$

(21-125)

$$A_{bulk0} = \left(1+\frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\left\{\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{X_j X_{dep}}}+\frac{B_o}{W_{eff}'+B_1}\right\}\right)\frac{1}{1+K_{eta}V_{bseff}}$$

(21-126)

$$V_{gsteffcv} = n\times N_{off}\times V_t \ln\left[1+\exp\left(\frac{V_{gs}-V_{th}-V_{offcv}}{n\times N_{off}\times V_t}\right)\right]$$

If $V_{ds} \le V_{dsat}$,

(21-127)

$$Q_g = Q_{g1} + W_{active}L_{active}C_{ox}\left(V_{gsteffcv}-\frac{V_{ds}}{2}+\frac{A_{bulk}'V_{ds}^2}{12\left(V_{gsteffcv}-\frac{A_{bulk}'}{2}V_{ds}\right)}\right)$$

(21-128)

$$Q_b = Q_{b1} + W_{active}L_{active}C_{ox}\left[\frac{(1-A_{bulk}')V_{ds}}{2}-\frac{(1-A_{bulk}')A_{bulk}'V_{ds}^2}{12\left(V_{gsteffcv}-\frac{A_{bulk}'}{2}V_{ds}\right)}\right]$$

50/50 Charge-Channel Partition

(21-129)

© 2023 Cadence Design Systems, Inc.

$$Q_s = Q_d = -\frac{W_{active}L_{active}C_{ox}}{2}\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{ds} + \frac{A_{bulk}'^2 V_{ds}^2}{12\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{ds}\right)}\right)$$

40/60 Channel-Charge Partition

(21-130)

$$Q_s = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteff^{cv}} - \frac{A_{bulk}'}{2}\times V_{ds}\right)^2} \times \left(V_{gsteffcv}^3 - \frac{4}{3}V_{gstefcvf}^2(A_{bulk}'V_{ds}) + \frac{2}{3}V_{gsteffcv}(A_{bulk}'V_{ds})^2 - \frac{2}{15}(A_{bulk}'V_{ds})^3\right)$$

(21-131)

$$Q_d = -(Q_g + Q_b + Q_s)$$

0/100 Channel-Charge Partition

(21-132)

$$Q_s = -W_{active}L_{active}C_{ox}\left(\frac{V_{gstefcv}}{2} + \frac{A_{bulk}'V_{ds}}{4} - \frac{(A_{bulk}'V_{ds})^2}{24\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{ds}\right)}\right)$$

(21-133)

$$Q_d = -(Q_g + Q_b + Q_s)$$

If $V_{ds} > V_{dsat}$,

(21-134)

© 2023 Cadence Design Systems, Inc.

$$Q_g = Q_{g1} + W_{active} L_{active} C_{ox} \left(V_{gsteffcv} - \frac{V_{dsat}}{3} \right)$$

(21-135)

$$Q_b = Q_{b1} - W_{active} L_{active} C_{ox} \left[\frac{V_{gsteffcv} - V_{dsat}}{3} \right]$$

50/50 Channel-Charge Partition

(21-136)

$$Q_s = Q_d = -\frac{W_{active} L_{active} C_{ox}}{3} (V_{gsteffcv})$$

40/60 Channel-Charge Partition

(21-137)

$$Q_s = -\frac{2 W_{active} L_{active} C_{ox}}{5} (V_{gsteffcv})$$

(21-138)

$$Q_d = -(Q_g + Q_b + Q_s)$$

0/100 Channel-Charge Partition

(21-139)

$$Q_s = -W_{active} L_{active} C_{ox} \left(\frac{2 V_{gstefcv}}{3} \right)$$

(21-140)

$$Q_d = -(Q_g + Q_b + Q_s)$$

© 2023 Cadence Design Systems, Inc.

For capmod=2

(21-141)

$$Q_g = -(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub})$$

(21-142)

$$Q_b = Q_{acc} + Q_{sub0} + \delta Q_{sub}$$

(21-143)

$$Q_{inv} = Q_s + Q_d$$

(21-144)

$$V_{FBeff} = V_{fb} - 0.5\left\{V_3 + \sqrt{V_3^2 + 4\delta_3 V_{fb}}\right\} \quad where \quad V_3 = V_{fb} - V_{gb} - \delta_3 \; ; \; \delta_3 = 0.02$$

(21-145)

$$V_{fb} = \begin{cases} V_{th} - \Phi_s - K_1\sqrt{\Phi_s} & \text{if version } \leq 3.1 \text{ or version = 3v3.2.1} \\ V_{th}(V_{bs} = 0) - \Phi_s - K_1\sqrt{\Phi_s} & \text{otherwise} \end{cases}$$

(21-146)

$$Q_{acc} = -W_{active} L_{active} C_{ox} (V_{fbeff} - V_{fb})$$

(21-147)

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \frac{K_1^2}{2}\left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{fbeff} - V_{gsteffcv} - V_{bseff})}{K_1^2}}\right)$$

(21-148)

© 2023 Cadence Design Systems, Inc.

$$V_{dsat,\,cv} = \frac{V_{gsteffcv}}{A_{bulk}'}$$

(21-149)

$$A_{bulk}' = \begin{cases} A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{eff}}\right)^{C_{le}}\right) & \text{if version <= 3.1} \\ A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{active}}\right)^{C_{le}}\right) & \text{if version > 3.1} \end{cases}$$

(21-150)

$$A_{bulk0} = \left(1 + \frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\left\{\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}} + \frac{B_o}{W_{eff}' + B_1}\right\}\right)\frac{1}{1 + K_{eta} V_{bseff}}$$

(21-151)

$$V_{gsteffcv} = n \times N_{off} \times V_t \ln\left[1 + \exp\left(\frac{V_{gs} - V_{th} - V_{offcv}}{n \times N_{off} \times V_t}\right)\right]$$

(21-152)

$$V_{cveff} = V_{dsat,\,cv} - 0.5\left\{V_4 + \sqrt{V_4^2 + 4\delta_4 V_{dsat,\,cv}}\right\}$$

$$where V_4 = V_{dsat,\,cv} - V_{ds} - \delta_4; \quad \delta_4 = 0.02$$

(21-153)

$$Q_{inv} = -W_{active} L_{active} C_{ox}\left(\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff}\right) + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff}\right)}\right)$$

© 2023 Cadence Design Systems, Inc.

(21-154)

$$\delta Q_{sub} = W_{active} L_{active} C_{ox} \left(\frac{1 - A_{bulk}'}{2} V_{cveff} - \frac{(1 - A_{bulk}') A_{bulk}' V_{cveff}^2}{12 \left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

50/50 Charge Partition

(21-155)

$$Q_s = Q_d = 0.5 Q_{inv} =$$

$$(-1) \frac{W_{active} L_{active} C_{ox}}{2} \left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} + \frac{A_{bulk}^2 ' V_{cveff}^2}{12 \left(V_{gsteffcv} - \frac{A_{bulk}}{2} V_{cveff} \right)} \right)$$

40/60 Channel-Charge Partition

(21-156)

$$Q_s = \left(- \frac{W_{active} L_{active} C_{ox}}{2 \left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} \right)^2} \right) \left(V_{gsteffcv}^3 - \frac{4}{3} V_{gsteffcv}^2 (A_{bulk}' V_{cveff}) \right.$$

$$\left. + \frac{2}{3} V_{gsteffcv} (A_{bulk}' V_{cveff})^2 - \frac{2}{15} (A_{bulk}' V_{cveff})^3 \right)$$

(21-157)

© 2023 Cadence Design Systems, Inc.

$$Q_d = \left(-\frac{W_{active} L_{active} C_{ox}}{2\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} \right)^2} \right) \left(V_{gsteffcv}^3 - \frac{5}{3} V_{gsteffcv}^2 (A_{bulk}' V_{cveff}) + \right.$$

$$\left. V_{gsteffcv} (A_{bulk}' V_{cveff})^2 - \frac{1}{5} (A_{bulk}' V_{cveff})^3 \right)$$

0/100 Charge Partition

(21-158)

$$Q_s = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteffcv}}{2} + \frac{A_{bulk}' V_{cveff}}{4} - \frac{(A_{bulk}' V_{cveff})^2}{24\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

(21-159)

$$Q_d = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteffcv}}{2} - \frac{3A_{bulk}' V_{cveff}}{4} + \frac{(A_{bulk}' V_{cveff})^2}{8\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

For capmod = 3

`capmod` = 3 supports only zero-bias V_{fp}; that is, V_{fb} is calculated from bias-independent V_{th}, regardless of the version number. This is different from `capmod` = 1 and 2.

(21-160)

$$Q_g = -(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub})$$

(21-161)

$$Q_b = Q_{acc} + Q_{sub0} + \delta Q_{sub}$$

(21-162)

© 2023 Cadence Design Systems, Inc.

$$Q_{inv} = Q_d + Q_s$$

(21-163)

$$V_{FBeff} = V_{fb} - 0.5\left(V_3 + \sqrt{V_3^2 + 4\delta_3 V_{fb}}\right)$$

where

(21-164)

$$V_3 = V_{fb} - V_{gb} - \delta_3$$

(21-165)

$$\delta_3 = 0.02$$

(21-166)

$$V_{fb} = V_{th}(V_{bs} = 0) - \phi_s - K_1\sqrt{\phi_s}$$

(21-167)

$$Q_{acc} = -W_{active}L_{active}C_{oxeff}(V_{fbeff} - V_{fb})$$

(21-168)

$$C_{oxeff} = \frac{C_{ox}C_{cen}}{C_{ox} + C_{cen}}$$

(21-169)

$$C_{ox} = \frac{E_{ox}}{t_{ox} - dtoxcv}$$

(21-170)

© 2023 Cadence Design Systems, Inc.

$$C_{cen} = \frac{\varepsilon_{si}}{T_{cen}}$$

(21-171)

$$T_{cen} = L_{deb} - 0.5 \times \left(T_3 + \sqrt{T_3^2 + 4 \times 10^{-3} L_{deb} T_{ox}} \right)$$

(21-172)

$$T_3 = L_{deb} \left\{ 1 - \exp\left[\frac{A_{cde} \times (V_{gs} - V_{bseff} - V_{fb})}{10^8 T_{ox}} \right] \right\} - 10^{-3} T_{ox}$$

(21-173)

$$Q_{sub} = -W_{active} L_{active} C_{oxeff} K_1 \left[\sqrt{\frac{K_1^2}{4} + V_{gs} - V_{fbeff} - V_{bseff} - V_{gsteffcv}} - \frac{K_1}{2} \right]$$

(21-174)

$$V_{gsteffcv} = nN_{off} V_t \ln\left[1 + \exp\left(\frac{V_{gs} - V_{th} - V_{offcv}}{nN_{off} V_t} \right) \right]$$

(21-175)

$$Q_{inv} = -W_{active} L_{active} C'_{oxeff} \left[V_{gsteffcv} - \delta\phi_s - \frac{A'_{bulk}}{2} V_{cveff} + \frac{A'^2_{bulk} V_{cveff}^2}{12\left(V_{gsteffcv} - \delta\phi_s - \frac{A'_{bulk}}{2} V_{cveff} \right)} \right]$$

(21-176)

© 2023 Cadence Design Systems, Inc.

$$\delta Q_{sub} = W_{active} L_{active} C'_{oxeff} \left[\frac{1 - A'_{bulk}}{2} V_{cveff} - \frac{(1 - A'_{bulk}) A'_{bulk} V_{cveff}^2}{12\left(V_{gsteffcv} - \delta\phi_s - \frac{A'_{bulk}}{2} V_{cveff} \right)} \right]$$

(21-177)

$$C'_{oxeff} = \frac{C_{ox} C'_{cen}}{C_{ox} + C'_{cen}}$$

(21-178)

$$C'_{cen} = \frac{\varepsilon_{si}}{T'_{cen}}$$

(21-179)

$$T'_{cen} = \frac{1.9 \times 10^{-9}}{1 + \left[\frac{4(V_{th} - V_{fb} - \phi_s) + V_{gsteffcv}}{2 \times 10^8 T_{ox}} \right]^{0.7}}$$

(21-180)

$$\delta\phi_s = V_t \log\left(1 + \frac{2K_1 \sqrt{\phi_s} V_{gsteffcv}}{M_{oin} V_t K_1^2} \right)$$

(21-181)

$$V_{dsat,cv} = \frac{V_{gsteffcv} - \delta\phi_s}{A'_{bulk}}$$

(21-182)

© 2023 Cadence Design Systems, Inc.

$$A_{bulk}' = \begin{cases} A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{eff}}\right)^{C_{le}}\right) & \text{if version <= 3.1} \\ A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{active}}\right)^{C_{le}}\right) & \text{if version > 3.1} \end{cases}$$

(21-183)

$$A_{bulk0} = \left[1 + \frac{K_1}{2\sqrt{\phi_s - V_{bseff}}}\left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}} + \frac{B_0}{W'_{eff} + B_1}\right)\right] \times \frac{1}{1 + K_{eta} V_{bseff}}$$

(21-184)

$$V_{cveff} = V_{dsat,\,cv} - 0.5\left(V_4 + \sqrt{V_4^2 + 4\delta_4 V_{dsat,\,cv}}\right)$$

(21-185)

$$V_4 = V_{dsat,\,cv} - V_{ds} - \delta_4$$

(21-186)

$$\delta_4 = 0.02$$

50/50 Charge Partition

(21-187)

$$Q_s = Q_d = 0.5 Q_{inv}$$

40/60 Charge Partition

(21-188)

© 2023 Cadence Design Systems, Inc.

$$Q_s = -\frac{W_{active}L_{active}C'_{oxeff}}{2\left(V_{gsteffcv} - \delta\phi_s - \frac{A'_{bulk}}{2}V_{cveff}\right)^2}[(V_{gsteffcv} - \delta\phi_s)^3$$
$$-\frac{4}{3}(V_{gsteffcv} - \delta\phi_s)^2 A'_{bulk}V_{cveff} + \frac{2}{3}(V_{gsteffcv} - \delta\phi_s)(A'_{bulk}\,V_{cveff})^2 - \frac{2}{15}(A'_{bulk}\,V_{cveff})^3]$$

(21-189)

$$Q_d = Q_{inv} - Q_s$$

0/100 Charge Partition

(21-190)

$$Q_s = -W_{active}L_{active}C'_{oxeff}\left[\frac{V_{gsteffcv} - \delta\phi_s}{2} + \frac{A'_{bulk}}{4}V_{cveff}\left(-\frac{(A'_{bulk}V_{cveff})^2}{24\left(V_{gsteffcv} - \delta\phi_s - \frac{A'_{bulk}}{2}V_{cveff}\right)}\right)\right]$$

(21-191)

$$Q_d = Q_{inv} - Q_s$$

Intrinsic Capacitances (with Body Bias and DIBL)

(21-192)

$$C_{(s,\,d,\,g,\,b),\,g} = \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{gsteffcv}}\frac{\partial V_{gsteffcv}}{\partial V_{gt}}$$

(21-193)

© 2023 Cadence Design Systems, Inc.

$$C_{(s,\,d,\,g,\,b),\,s} = -\frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{ds}} + \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \left(\frac{\partial V_{th}}{\partial V_{ds}} + \frac{\partial V_{th}}{\partial V_{bs}} \right)$$

(21-194)

$$C_{(s,\,d,\,g,\,b),\,d} = \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{ds}} - \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial (V_{gsteffcv})} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{ds}}$$

(21-195)

$$C_{(s,\,d,\,g,\,b),\,b} = \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{bs}} - \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{bs}}$$

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

LOD Model

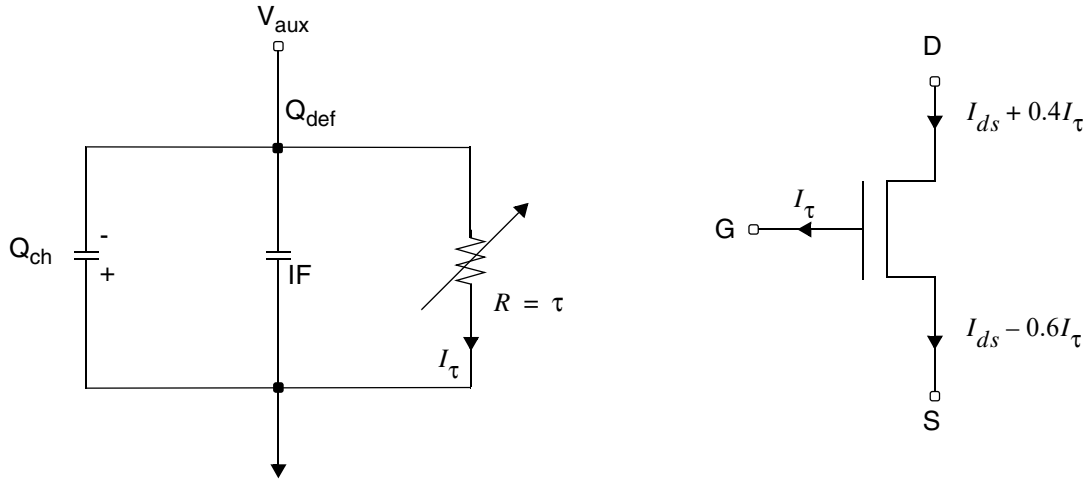
Nonquasi-static (NQS) Model

SPICE3 Junction Diode Model

© 2023 Cadence Design Systems, Inc.

Nonquasi-static (NQS) Model

The following equivalent circuit is used if `nqsmod` = 1. (Only the intrinsic transistor is affected by NQS. The extrinsic components remain the same).



Quasi-static equilibrium channel charge:

(21-196)

$$Q_{eq} = -(Q_g + Q_b)$$

Actual channel charge and `Qdef` obtained from subcircuit:

(21-197)

$$Q_{ch} = Q_{eq} - Q_{def}$$

(21-198)

$$g_\tau = \frac{1}{\tau} = \frac{1}{\tau_{drift}} + \frac{1}{\tau_{diff}}$$

(21-199)

© 2023 Cadence Design Systems, Inc.

$$\tau_{drift} = \frac{C_{ox} W_{eff} L_{eff}^3}{\mu_{eff} \varepsilon |Q_{eq} - \alpha Q_{def}|} \approx \frac{\zeta}{|Q_{eq}|}$$

where

$\varepsilon \equiv$ Elmore Constant (default = 5)

$0.0 \le \alpha \le 1.0$ (default = 0.5)

and

(21-200)

$$\zeta = \frac{C_{ox} W_{eff} L_{eff}^3}{\mu_{eff} \varepsilon}$$

(21-201)

$$\tau_{diff} = \frac{L_{eff}^2}{16 \mu_{eff} V_{tm}}$$

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

LOD Model

Nonquasi-static (NQS) Model

SPICE3 Junction Diode Model

SPICE3 Junction Diode Model

There are two junction models in the BSIM3v3 device model. The `diomod` parameter determines the model to be used in a given simulation:

- If `diomod=1` (default value), the model uses the equations described in the chapter *Common MOSFET Equations*.

© 2023 Cadence Design Systems, Inc.

- If `diomod=0`, the model uses the equations described in *Chapter 9* of the BSIM3v3.2.2 MOSFET Model-Users' Manual available at:

  http://www-device.EECS.Berkeley.EDU/~bsim3/get.html

  The BSIM3v3 device model uses the same equations when `tlev=1`.

Starting with MMSIM1211ISR17, bsim3v3 supports the trap-assisted tunneling current, if `diomod!=100`. For more information, refer to the equations described in the *Total Junction Source/Drain Diode Including Tunneling* section in chapter *BSIM4 Level-14 Model (bsim4)*.

Flicker Noise

Two models exist for flicker noise. Each of these can be toggled by the `noimod` flag.

For noimod = 1 and 4

If `wnoi` is given

(21-202)

$$FlickerNoise = \frac{K_f I_{ds}^{A_f}}{C_{ox} L_{eff}^2 f^{E_f}} \times (wnoi)/(weff)$$

otherwise

(21-203)

$$FlickerNo = \frac{K_f I_{ds}^{A_f}}{C_{ox} L_{eff}^2 f^{E_f}}$$

For noimod = 2 and 3

$V_{gs} > V_{th} + 0.1$:

© 2023 Cadence Design Systems, Inc.

where V_{tm} is the thermal voltage, μ_{eff} is the effective mobility at the given bias condition, L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source given by

(21-204)

$$N_0 = \frac{C_{ox}(V_{gs} - V_{th})}{q}$$

(21-205)

$$FlickerNoise = \frac{V_{tm} q^2 I_{ds} \mu_{eff}}{f^{E_f} L_{eff}^2 C_{ox} \times 10^8} \left[N_{oia} \log\left(\frac{N_0 + 2 \times 10^{14}}{N_l + 2 \times 10^{14}}\right) + N_{oib} \times (N_0 - N_l) + 0.5 \times N_{oic}(N_0^2 - N_l^2) \right] + \frac{V_{tm} I_{ds}^2 \Delta L_{clm}}{f^{E_f} L_{eff}^2 W_{eff} 10^8} \times \frac{N_{oia} + N_{oib} N_l + N_{oic} N_l^2}{(N_l + N_{oid})^2}$$

The parameter N_l is the charge density at the drain given by

(21-206)

$$N_l = \begin{cases} C_{ox}\left(\frac{V_{gs} - V_{th} - V_{ds}}{q}\right) & \text{if version < 3.2.4} \\ \left(C_{OX} \cdot V_{gsteff} \cdot \left(1 - \frac{A_{bulk} V_{dseff}}{V_{gsteff} + 2V_t}\right)\right) / q & \text{if version >= 3.2.4} \end{cases}$$

(21-207)

$$V_{ds} = MIN(V_{ds}, V_{dsat})$$

ΔL_{CLM} refers to channel length reduction due to CLM and is given by

(21-208)

© 2023 Cadence Design Systems, Inc.

$$\Delta L_{clm} = \begin{cases} L_{itl} \times \log\left(\dfrac{\dfrac{V_{ds} - V_{dsat}}{L_{itl}} + E_m}{E_{sat}} \right) & \text{if } V_{DS} > V_{DSAT} \\ 0 & \text{otherwise} \end{cases}$$

(21-209)

$$E_{sat} = \frac{2 \times V_{sat}}{U_{eff}}$$

Otherwise,

(21-210)

$$\text{FlickerNoise} = \frac{S_{limit} \times S_{wi}}{S_{limit} + S_{wi}}$$

where S_{limit} is the flicker noise calculated at $V_{gs} = V_{th} + 0.1$ and S_{wi} is given by

(21-211)

$$S_{wi} = \frac{N_{oia} V_{tm} \times I_{ds}^2}{W_{eff} \times L_{eff} \times f^{E_f} \times 10^8 \times N_{oid}^2}$$

Channel Thermal Noise

Two models exist for channel thermal noise. Each of these can be toggled by the `noimod` flag.

For `noimod`=1 and 3,

(21-212)

$$\overline{i_D^2} = \frac{4kT}{3} \times gamma \times (g_m + g_{ds} + g_{mb})$$

© 2023 Cadence Design Systems, Inc.

where gamma is a new model parameter introduced to model short channel device thermal noise. The default value for gamma is 2/3.

The standard Berkeley BSIM3v3 equation is

(21-213)

$$\overline{i_D^2} = \frac{8kT}{3}(g_m + g_{ds} + g_{mb})$$

For `noimod`=2 and 4,

(21-214)

$$\overline{i_d^2} = \frac{4kTu_{eff}}{L^2_{eff} + u_{eff}|Q_{inv}| \cdot R_{ds}}|Q_{inv}| \quad \text{if version = 3.2.4}$$

$$\overline{i_d^2} = \left(\frac{4kTu_{eff}}{L^2_{eff}} \cdot |Q_{inv}|\right) \quad \text{if version > or < 3.2.4}$$

where Qinv is the channel inversion charge, and is calculated as follows:

- For version 3.1:

(21-215)

$$Q_{inv} = -W_{eff}L_{eff}C_{ox}V_{gsteff}\left(1 - \frac{A_{bulk}}{2(V_{gsteff} + 2V_{tm})}V_{dseff}\right)$$

- For version 3.2, the Qinv equations are described in Intrinsic Charges.

Default Model Parameter Value Calculation

- If $vtho$ is not given, it is calculated from

(21-216)

$$vtho = vfb + phi + k1\sqrt{phi}$$

- If phi is not given, it is calculated from

© 2023 Cadence Design Systems, Inc.

(21-217)

$$phi = 2V_{tm}\ln\left(\frac{nch}{n_i}\right)$$

where V_{tm} is the thermal voltage given by

(21-218)

$$V_{tm} = \frac{kT}{q}$$

(21-219)

$$n_i = 1.45 \times 10^{10}\left(\frac{T}{300}\right)^{1.5}\exp\left(21.5565981 - \frac{E_g(T)}{2V_{tm}}\right)$$

where $E_g(T)$ is the energy band gap at temperature T. The equation for E_g is shown in *Chapter 12 Common MOSFET Equations*.

- If $k1$ is not given, it is calculated from

(21-220)

$$k1 = gamma2 - 2k2\sqrt{phi - vbm}$$

- If $k2$ is not given, it is calculated from

(21-221)

$$k2 = \frac{(gamma1 - gamma2)(\sqrt{phi - vbx} - \sqrt{phi})}{2\sqrt{phi}(\sqrt{phi - vbm} - \sqrt{phi}) + vbm}$$

- If $gamma1$ is not given, it is calculated from

(21-222)

$$gamma1 = \frac{\sqrt{2q\varepsilon_{si}nch}}{C_{ox}}$$

- If $gamma2$ is not given, it is calculated from

(21-223)

© 2023 Cadence Design Systems, Inc.

$$gamma2 = \frac{\sqrt{2q\varepsilon_{si}nsub}}{C_{ox}}$$

- If Version <= 3.1 or version = 3.21, and capmod < 3

(21-224)

$$vfb = vth - phi - k1 \times \sqrt{phi - vbs}$$

otherwise

(21-225)

$$vfb = vth0z - phi - k1\sqrt{phi}$$

- If V_{bi} is not given, it is calculated from

(21-226)

$$V_{bi} = V_{tm}\ln\left(\frac{1.0e20 \times nch}{n_i^2}\right)$$

- If V_{bx} is not given, it is calculated from

(21-227)

$$V_{bx} = phi - \frac{q*nch*xt^2}{2\varepsilon_{si}}$$

- If *cgso* is not given, *dlc* is given, and *dlc* > 0

(21-228)

$$cgso = (dlc + meto) \times cox - cgsl$$

otherwise

(21-229)

$$cgso = 0.6 \times xj \times cox$$

- If *cgdo* not given, *dlc* given, and *dlc* > 0

(21-230)

© 2023 Cadence Design Systems, Inc.

$$cgdo = (dlc + meto) \times cox - cgdl$$

otherwise

(21-231)

$$cgdo = 0.6 \times xj \times cox$$

Gate Leak Currents

This section describes the parameters and equations for gate leak currents.

Instance Parameters

Parameter	Description
`Aforward`	Forward gate leakage current coefficient. Default value is `0.0`.
`Areverse`	Reverse gate leakage current coefficient. Default value is `0.0`.

If Aforward and Areverse are both 0.0, gate leak current is also 0.0.

Model Parameters

Parameter	Description
`Bforward`	Forward gate leakage current coefficient in `pow()`. Default value is `0.0`.
`Breverse`	Reverse gate leakage current coefficient in `pow()`. Default value is `0.0`.
`Cforward`	Forward gate leakage current coefficient in `exp()`. Default value is `0.0`.
`Creverse`	Reverse gate leakage current coefficient in `exp()`. Default value is `0.0`.
`Tcc`	Gate leakage current temperature coefficient. Default value is `0.0`.

Leak current between Gate and Drain

If Vgd>0

© 2023 Cadence Design Systems, Inc.

(21-232)

$$I_{gd} = Aforward \times (1.0 + Tcc \times (Temp - Tnom)) \times pow(Vgd, Bforward) \times \exp(Cforward \times Vgd)$$

If Vgd<0

(21-233)

$$I_{gd} = -Areverse \times (1.0 + Tcc \times (Temp - Tnom)) \times pow(-Vgd, Breverse) \times \exp(Creverse \times Vgd)$$

If Vgd=0

Igd=0.0

Leak current between Gate and Source

- If IgcModel=0 and Igbmodel=0,

  If Vgs>0

(21-234)

$$I_{gs} = Aforward \times (1.0 + Tcc \times (Temp - Tnom)) \times pow(Vgs, Bforward) \times \exp(Cforward \times Vgs)$$

  If Vgs<0

(21-235)

$$I_{gs} = -Areverse \times (1.0 + Tcc \times (Temp - Tnom)) \times pow(-Vgs, Breverse) \times \exp(Creverse \times Vgs)$$

  If Vgs=0

  Igs=0.0

- Otherwise,

  Igc

  If IgcModel=0 and Igbmodel=0, the above equations apply.

© 2023 Cadence Design Systems, Inc.

Otherwise, the following equations apply.

Igc=Igcs+Igcd

(21-236)

$$Igc0 = W_{eff}L_{eff}A \cdot T_{oxratio}V_{gse}V_{aux} \cdot \exp(-B \cdot Toxe(Aigc - Bigc \cdot V_{oxdepinv})(1 + Cigc \cdot V_{oxdepinv}))$$

For Igcmod=1

(21-237)

$$V_{aux} = Nigc \cdot vt \cdot \log\left(1 + \exp\left(\frac{V_{gse} - Vth0}{Nigc \cdot vt}\right)\right)$$

For Igcmod=2

(21-238)

$$V_{aux} = Nigc \cdot vt \cdot \log\left(1 + \exp\left(\frac{V_{gse} - Vth}{Nigc \cdot vt}\right)\right)$$

(21-239)

$$T_{oxratio} = \left(\frac{Toxref}{Toxe}\right)^{Ntox}\frac{1}{Toxe^2}$$

(21-240)

$$V_{oxdepinv} = K1_{ox}\sqrt{\phi_s} + V_{gsteff}$$

Then

(21-241)

$$Igcs = Igc0\frac{Pigcd \cdot V_{dseff} + \exp(-Pigcd \cdot V_{dseff}) - 1 + 1.0e-4}{Pigcd^2V_{dseff}^2 + 2.0e-4}$$

(21-242)

© 2023 Cadence Design Systems, Inc.

$$Igcd = Igc0\frac{1-(Pigcd\cdot V_{dseff}+1)\exp(-Pigcd\cdot V_{dseff})+1.0e-4}{Pigcd^2V_{dseff}^{\ 2}+2.0e-4}$$

Igs and Igd

Igs represents the gate tunneling current between the gate and source diffusion region, while Igd represents the gate tunneling current between the gate and the drain diffusion region.

(21-243)

$$Igs = W_{eff}Dlcig\cdot Aechvb\cdot T_{oxratioedge}V_{gs}V_{gs}'\exp(-Bechvb\cdot Toxe\cdot Poxedge\cdot (Aigsd-Bigsd\cdot V_{gs}'))$$

(21-244)

$$Igd = W_{eff}Dlcig\cdot Aechvb\cdot T_{oxratioedge}V_{gd}V_{gd}'\exp(-Bechvb\cdot Toxe\cdot Poxedge\cdot (Aigsd-Bigsd\cdot V_{gd}'))$$

where

(21-245)

$$T_{oxratioedge} = \left(\frac{T_{oxref}}{T_{oxe}P_{oxedge}}\right)\frac{1}{(T_{oxe}P_{oxedge})^2}$$

Igb

Igb=Igbacc+Igbinv

Igbacc is determined by ECB (Electronic tunneling from Conduction band) and is significant in accumulation and given by:

(21-246)

$$I_{gbacc} = W_{eff}L_{eff}Aechve\cdot T_{oxratio}V_{gb}V_{aux}\cdot \exp(-Bechvb\cdot Toxe(Aigbacc-Bigbacc\cdot V_{oxacc})(1+Cigbac\cdot V_{oxacc}))$$

© 2023 Cadence Design Systems, Inc.

Where

(21-247)

$$V_{oxacc} = V_{fbsb} - V_{fbeff}$$

(21-248)

$$V_{fbsb} = V_{th}\Big|_{Vbs = Vds = 0q} - \phi_s - K1\sqrt{\phi_s}$$

(21-249)

$$V_{aux} = Nigbacc \cdot vt \cdot \log\left(1 + \exp\left(\frac{V_{gb} - V_{fbsb}}{Nigbacc \cdot vt}\right)\right)$$

Igbinv is determined by EVB (Electron tunneling from valence band) and is significant in inversion and given by:

(21-250)

$$I_{gbinv} = W_{eff} L_{eff} Aechve \cdot T_{oxratio} V_{gb} V_{aux} \cdot \exp(-Bechvb \cdot Toxe(Aigbinv - Bigbinv \cdot V_{oxdepinv})(1 + Cigbinv \cdot V_{oxdepinv}))$$

Where

(21-251)

$$V_{aux} = Nigbinv \cdot vt \cdot \log\left(1 + \exp\left(\frac{V_{oxdepinv} - Eigbinv}{Nigbinv \cdot vt}\right)\right)$$

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

LOD Model

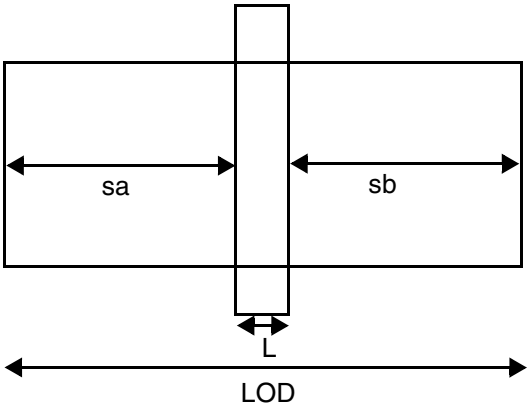
Nonquasi-static (NQS) Model

Differences between BSIM3v3 Subversions

© 2023 Cadence Design Systems, Inc.

LOD Model

The following diagram displays the LOD instance geometry parameters `sa` and `sb`.



(21-252)

$$\rho_{\mu eff} = \frac{ku0}{Kstress_u0} \cdot (Inv_sa + Inv_sb)$$

(21-253)

$$Inv_sa = \frac{1}{SA + 0.5 \cdot L_{drawn}}$$

(21-254)

$$Inv_sb = \frac{1}{SB + 0.5 \cdot L_{drawn}}$$

(21-255)

© 2023 Cadence Design Systems, Inc.

$$Kstress_u0 = \left(1 + \frac{LKU0}{(L_{drawn} + XL)^{LLODKU0}} + \frac{WKU0}{(W_{drawn} + XW + WLOD)^{WLODKU0}} + \frac{PKU0}{(L_{drawn} + XL)^{LLODKU0} \cdot (W_{drawn} + XW + WLOD)^{WLODKU0}}\right) \times \left(1 + TKU0 \cdot \left(\frac{Temperature}{TNOM} - 1\right)\right)$$

For irregular LOD device,

(21-256)

$$\frac{1}{SA_{eff} + 0.5 \cdot L_{drawn}} = \sum_{i=1}^{n} \frac{SW_i}{W_{drawn}} \cdot \frac{1}{sa_i + 0.5 \cdot L_{drawn}}$$

(21-257)

$$\frac{1}{SB_{eff} + 0.5 \cdot L_{drawn}} = \sum_{i=1}^{n} \frac{SW_i}{W_{drawn}} \cdot \frac{1}{sb_i + 0.5 \cdot L_{drawn}}$$

Stress Effect

(21-258)

$$\mu_{eff} = \frac{1 + \rho_{\mu eff}(SA, SB)}{1 + \rho_{\mu eff}(SA_{ref}, SB_{ref})} \mu_{effo}$$

(21-259)

$$\upsilon_{sat} = \frac{1 + K \cdot \rho_{\mu eff}(SA, SB)}{1 + K \cdot \rho_{\mu eff}(SA_{ref}, SB_{ref})} \upsilon_{sato}$$

where μ_{effo}, υ_{sato} are low field mobility, saturation velocity at SA_{ref}, SB_{ref}.

© 2023 Cadence Design Systems, Inc.

(21-260)

$$Kstress_\text{vth0} = 1 + \frac{LKVTH0}{(L_{drawn} + XL)^{LLODKVTH}} + \frac{WKVTH0}{(W_{drawn} + XW + WLOD)^{WLODKVTH}} + \frac{PKVTH0}{(L_{drawn} + XL)^{LLODKVTH} \cdot (W_{drawn} + XW + WLOD)^{WLODKVTH}}$$

(21-261)

$$VTH0 = VTH0_{original} + \frac{KVTH0}{Kstress_\text{vth0}} \cdot (Inv_\text{sa} + Inv_\text{sb} - Inv_\text{sa}_{ref} - Inv_\text{sb}_{ref})$$

(21-262)

$$K2 = K2_{original} + \frac{STK2}{Kstress_\text{vth0}^{LODK2}} \cdot (Inv_\text{sa} + Inv_\text{sb} - Inv_\text{sa}_{ref} - Inv_\text{sb}_{ref})$$

(21-263)

$$ETA0 = ETA0_{original} + \frac{STETAO}{Kstress_\text{vth0}^{LODETO}} \cdot (Inv_\text{sa} + Inv_\text{sb} - Inv_\text{sa}_{ref} - Inv_\text{sb}_{ref})$$

Well Proximity Effect

(21-264)

$$Vth0 = Vth0_{org} + KVth0we \cdot (Sca + Web \cdot Scb + Wec \cdot Scc)$$

(21-265)

$$K2 = K2_{org} + K2we \cdot (Sca + Web \cdot Scb + Wec \cdot Scc)$$

(21-266)

$$\mu_{eff} = \mu_{eff,\,org} \cdot (1 + Ku0we \cdot (Sca + Web \cdot Scb + Wec \cdot Scc))$$

SC is defined as the distance to a single well edge used in calculations of SCA, SCB, and SCC when layout information is not available. If SCA, SCB, and SCC are not given, their estimation is as follows:

© 2023 Cadence Design Systems, Inc.

(21-267)

$$Sca = \frac{Scref^2}{W_{drawn}}\left(\frac{1}{Sc} - \frac{1}{Sc + W_{drawn}}\right)$$

(21-268)

$$Scb = \frac{1}{W_{drawn}Scref}\left(\begin{array}{l} \frac{Scref}{20}Sc \cdot \exp\left(-10\frac{Sc}{Scref}\right) + \frac{Scref^2}{400}\exp\left(-10\frac{Sc}{Scref}\right) \\ -\frac{Scref}{10}(Sc + W_{drawn})\exp\left(-10\frac{Sc + W_{drawn}}{Scref}\right) \\ -\frac{Scref^2}{400}\exp\left(-10\frac{Sc + W_{drawn}}{Scref}\right) \end{array}\right)$$

(21-269)

$$Scc = \frac{1}{W_{drawn}Scref}\left(\begin{array}{l} \frac{Scref}{20}Sc \cdot \exp\left(-20\frac{Sc}{Scref}\right) + \frac{Scref^2}{400}\exp\left(-20\frac{Sc}{Scref}\right) \\ -\frac{Scref}{20}(Sc + W_{drawn})\exp\left(-20\frac{Sc + W_{drawn}}{Scref}\right) \\ -\frac{Scref^2}{400}\exp\left(-20\frac{Sc + W_{drawn}}{Scref}\right) \end{array}\right)$$

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

I-V Model

SPICE3 Junction Diode Model

Nonquasi-static (NQS) Model

Differences between BSIM3v3 Subversions

© 2023 Cadence Design Systems, Inc.

Differences between BSIM3v3 Subversions

1. Intrinsic Charges

When	The equations are
capmod=0	**(21-270)**

$$A_{bulk}' = \begin{cases} A_{bulk0}\left(1+\left(\frac{C_{lc}}{L_{eff}}\right)^{C_{le}}\right) & \text{if version} \le 3.1 \\ A_{bulk0}\left(1+\left(\frac{C_{lc}}{L_{active}}\right)^{C_{le}}\right) & \text{if version} > 3.1 \end{cases}$$

capmod=1 **(21-271)**

$$V_{fb} = \begin{cases} V_{th} - \Phi_s - K_1\sqrt{\Phi_s} & \text{if version} \le 3.1 \text{ and version} = 3.2.1 \\ V_{th}(V_{bs}=0) - \Phi_s - K_1\sqrt{\Phi_s} & \text{if version} = 3.2 \text{ and version} = 3.2.2 \end{cases}$$

(21-272)

$$A_{bulk}' = \begin{cases} A_{bulk0}\left(1+\left(\frac{C_{lc}}{L_{eff}}\right)^{C_{le}}\right) & \text{if version} \le 3.1 \\ A_{bulk0}\left(1+\left(\frac{C_{lc}}{L_{active}}\right)^{C_{le}}\right) & \text{if version} > 3.1 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

When	The equations are
capmod=2	**(21-273)**

$$V_{fb} = \begin{cases} V_{th} - \Phi_s - K_1\sqrt{\Phi_s} & \text{if version} \le 3.1 \text{ or version} = 3.2.1 \\ V_{th}(V_{bs}=0) - \Phi_s - K_1\sqrt{\Phi_s} & \text{otherwise} \end{cases}$$

(21-274)

$$A_{bulk}{}' = \begin{cases} A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{eff}}\right)^{C_{le}}\right) & \text{if version} \le 3.1 \\ A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{active}}\right)^{C_{le}}\right) & \text{if version} > 3.1 \end{cases}$$

capmod=3 **(21-275)**

$$A_{bulk}{}' = \begin{cases} A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{eff}}\right)^{C_{le}}\right) & \text{if version} \le 3.1 \\ A_{bulk0}\left(1 + \left(\frac{C_{lc}}{L_{active}}\right)^{C_{le}}\right) & \text{if version} > 3.1 \end{cases}$$

2. Flicker noise

For noimod=2 and 3

(21-276)

$$N_l = \begin{cases} C_{ox}\left(\frac{V_{gs} - V_{th} - V_{ds}}{q}\right) & \text{if version} < 3.2.4 \\ \left(C_{OX} \cdot V_{gsteff} \cdot \left(1 - \frac{A_{bulk} V_{dseff}}{V_{gsteff} + 2V_t}\right)\right) / q0 & \text{if version Š } 3.2.4 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

3. Channel Thermal Noise

(21-277)

$$\overline{i_d^2} = \frac{4kTu_{eff}}{L^2{}_{eff} + u_{eff}\left|Q_{inv}\right| \cdot R_{ds}}\left|Q_{inv}\right| \quad \text{if version = 3.2.4}$$

$$\overline{i_d^2} = \left(\frac{4kTu_{eff}}{L^2{}_{eff}} \cdot \left|Q_{inv}\right|\right) \quad \text{if version < or > 3.2.4}$$

4. If vto is not given

(21-278)

$$vto = \begin{cases} -1.0 + Phi + K1 \times SqrtPhi + Delvto & \text{if version} \leq 3.1 \\ Vfb + Phi + K1 \times SqrtPhi + Delvto & \text{if version} > 3.1 \end{cases}$$

5. Overlap Capacitance

- If OverlapCgs < 0

  For BSIM3v3 version < 3.1

(21-279)

$$OverlapCgs = 1.0e-7 \times T_{ox}$$

For BSIM3v3 version ≥ 3.1

(21-280)

$$OverlapCgs = 0$$

- If OverlapCgd < 0

  For BSIM3v3 version < 3.1

(21-281)

$$OverlapCgd = 1.0e-7 \times T_{ox}$$

For BSIM3v3 version ≥ 3.1

(21-282)

© 2023 Cadence Design Systems, Inc.

$$OverlapCgs = 0$$

- If OverlapCgb is not given

  For BSIM3v3 version < 3.1

(21-283)

$$OverlapCgb = 0$$

For BSIM3v3 version ≥ 3.1

(21-284)

$$OverlapCgb = 2.0 \times dwc \times C_{ox}$$

Parameter Differences between BSIM3v3 Levels

The following table lists the parameters whose default value depends on the level of the BSIM3v3 model.

Parameter Name	Default Value for each Level	Description
k1	0.53V^1/2 (LEVEL=49/53) 1.90923V^1/2 (LEVEL=11)	Body-effect coefficient
k2	0.0186 (LEVEL=49/53) -0.33 (LEVEL=11)	Charge-sharing parameter
vfbflag	0 (LEVEL=49/53)	Vfb selector
binflag	0 (LEVEL=49/53)	Binning factor
lref	1.0e20 (LEVEL=49/53)	Binning length factor
minr	0.1 Ohm (LEVEL=11) 1e-5 Ohm (LEVEL=49/53)	Minimum source/drain resistance
js	0A/m2 (LEVEL=49) 1e-4A/m2 (LEVEL=53)	Bulk junction reverse saturation current density
f	1.0e20 (LEVEL=49/53)	Binning width factor
is	1e-14 (LEVEL=11)	Bulk junction reverse saturation current

© 2023 Cadence Design Systems, Inc.

Parameter Name	Default Value for each Level	Description
pb	1V (LEVEL=11/53) 0.8V (LEVEL=49)	Bulk junction built-in potential
cjsw	5e-10F/m (LEVEL=11/53) 0F/m (LEVEL=49)	Zero-bias junction sidewall capacitance density
capmod	2 (LEVEL=11) 3 (LEVEL=49/53)	Intrinsic charge model
xpart	0 (LEVEL=11/53) 1 (LEVEL=49)	Drain/source channel charge partition in saturation for BSIM charge model. Use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
version	3.1(LEVEL=11) 3.2(LEVEL=49/53)	Model version selector. The available versions are 3.1, 3.2, 3.21,3.22, 3.23, 3.24 and 3.3.
paramchk	1 (LEVEL=11) 0 (LEVEL=49/53)	Model parameter checking selector
acm	0 (LEVEL=11/49) 10 (LEVEL=53)	BSIM3v3 area calculation method selector
calcacm	0 (LEVEL=49/53)	geometry factor
eg	1.12452V (LEVEL=11) 1.16V (LEVEL=49/53)	Energy band gap
diomod	1 (LEVEL=11/49) 0 (LEVEL=53)	Flag to select junction model: When diomod=1, the junction model described in Common MOSFET Equations section is used. When diomod=0, the Berkeley junction model is used. When diomod=100, the TSMC special diode model is used.
xti	3 (LEVEL=11/53) 0 (LEVEL=49)	Saturation current temperature exponent
nlev	2.0 (LEVEL=49/53)	Noise selector

© 2023 Cadence Design Systems, Inc.

Parameter Name	Default Value for each Level	Description
gdsnoi	1.0 (LEVEL=49/53)	Channel thermal noise coefficient for 49 noise

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

LOD Model

Nonquasi-static (NQS) Model

I-V Model

Scaling Effects (BSIM3v3)

`scale` and `scalem` are options that set the scaling factors for instance and model parameters, respectively. You can specify the scaling factors in the `.options` statement.

The following sections describe the parameters that are scaled.

Instance Parameters

Channel Width

(21-285)

$$w = w \times scale$$

Channel length

(21-286)

$$l = l \times scale$$

Source area

(21-287)

$$as = as \times scale \times scale$$

© 2023 Cadence Design Systems, Inc.

Drain area

(21-288)

$$ad = ad \times scale \times scale$$

Source perimeter

(21-289)

$$ps = ps \times scale \times scale$$

Drain perimeter

(21-290)

$$pd = pd \times scale$$

Component Statements

This device is supported within altergroups.

Sample Instance Statement

```
m4 (0 2 1 1) pchmod w=2u l=0.8u as=250p ad=250p pd=168p ps=168p m=1
```

Sample Model Statement

```
model pchmod bsim3v3 type=p mobmod=1 capmod=2 version=3.1 tox=9e-5 cdsc=1e-3
cdscb=-4.36889e-4 cdscd=0 cit=0 nfactor=1.79 xj=1.5e-7 vsat=1.5737e5 at=1e5
a0=1.2522809 ags=0.2912413 a1=1.01222e-4 a2=0.996841 keta=0 nch=4.06263e17
ngate=7.6e19 k1=0.823562
```

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

w (m)	Channel width.
l (m)	Channel length.
as (m^2)	Area of source diffusion.
ad (m^2)	Area of drain diffusion.
ps (m)	Perimeter of source diffusion.
pd (m)	Perimeter of drain diffusion.
nrd (m/m)	Number of squares of drain diffusion.
nrs (m/m)	Number of squares of source diffusion.
m=1	Multiplicity factor (number of MOSFETs in parallel).
region=triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are off, triode, sat, subth, and breakdown.
nqsmod	NQS flag.
acnqsmod	AC NQS flag.
isnoisy=yes	Should device generate noise. Possible values are yes and no.
trise (C)	Temperature rise from ambient.
aforward=0	Forward gate leakage current coefficient.
areverse=0	Reverse gate leakage current coefficient.
delvto=0 V	Shift in zer0-bias threshold voltage vth0.
mulmu0=1	Mobility multiplier.
mulu0=1	Mobility multiplier.
delk1=0 V	Shift in body bias coefficient k1.
delnfct=0	Shift in subthreshold swing factor nfactor.
geo=0	Geometry selector.
rdc=0	Drain contact resistance.
rsc=0	Source contact resistance.
sa=0 m	Distance between OD edge to poly of one side.
sb=0 m	Distance between OD edge to poly of the other side.

© 2023 Cadence Design Systems, Inc.

sa1=0 m	Distance between OD edge to poly of one side 1.
sa2=0 m	Distance between OD edge to poly of one side 2.
sa3=0 m	Distance between OD edge to poly of one side 3.
sa4=0 m	Distance between OD edge to poly of one side 4.
sa5=0 m	Distance between OD edge to poly of one side 5.
sa6=0 m	Distance between OD edge to poly of one side 6.
sa7=0 m	Distance between OD edge to poly of one side 7.
sa8=0 m	Distance between OD edge to poly of one side 8.
sa9=0 m	Distance between OD edge to poly of one side 9.
sa10=0 m	Distance between OD edge to poly of one side 10.
sb1=0 m	Distance between OD edge to poly of the other side 1.
sb2=0 m	Distance between OD edge to poly of the other side 2.
sb3=0 m	Distance between OD edge to poly of the other side 3.
sb4=0 m	Distance between OD edge to poly of the other side 4.
sb5=0 m	Distance between OD edge to poly of the other side 5.
sb6=0 m	Distance between OD edge to poly of the other side 6.
sb7=0 m	Distance between OD edge to poly of the other side 7.
sb8=0 m	Distance between OD edge to poly of the other side 8.
sb9=0 m	Distance between OD edge to poly of the other side 9.
sb10=0 m	Distance between OD edge to poly of the other side 10.
sw1=0 m	Width of SA1/SB1.
sw2=0 m	Width of SA2/SB2.
sw3=0 m	Width of SA3/SB3.
sw4=0 m	Width of SA4/SB4.
sw5=0 m	Width of SA5/SB5.
sw6=0 m	Width of SA6/SB6.
sw7=0 m	Width of SA7/SB7.
sw8=0 m	Width of SA8/SB8.
sw9=0 m	Width of SA9/SB9.

© 2023 Cadence Design Systems, Inc.

sw10=0 m	Width of SA10/SB10.
stimod	LOD stress effect model selector.
sca=0.0	Integral of the first distribution function for scattered well dopant.
scb=0.0	Integral of the second distribution function for scattered well dopant.
scc=0.0 V	Integral of the third distribution function for scattered well dopant.
sc=0.0 m	Distance to a single well edge .
mulid0=1.0	Ids multiplier.

Model Syntax

```
model modelName bsim3v3 parameter=value ...
```

Model Parameters

Device type parameters

type=n	Transistor type. Possible values are n and p.

Threshold voltage parameters

vtho (V)	Threshold voltage at zero body bias for long-channel devices. For enhancement-mode devices, vtho > 0 for n-channel and vth < 0 for p-channel. Default value is calculated from other model parameters.
vfb=-1 V	Flat-band voltage.
k1=0.5 V	Body-effect coefficient.
k2=-0.0186	Charge-sharing parameter.
k3=80	Narrow width coefficient.
k3b=0 1/V	Narrow width coefficient.

© 2023 Cadence Design Systems, Inc.

`w0=2.5e-6 m`	Narrow width coefficient.
`nlx=1.74e-7 m`	Lateral nonuniform doping coefficient.
`gamma1 ( V )`	Body-effect coefficient near the surface.
`gamma2 ( V )`	Body-effect coefficient in the bulk.
`vbx (V)`	Threshold voltage transition body voltage.
`vbm=-3 V`	Maximum applied body voltage.
`dvt0=2.2`	First coefficient of short-channel effects.
`dvt1=0.53`	Second coefficient of short-channel effects.
`dvt2=-0.032 1/V`	Body-bias coefficient of short-channel effects.
`dvt0w=0 1/m`	First coefficient of narrow-width effects.
`dvt1w=5.3e6 1/m`	Second coefficient of narrow-width effects.
`dvt2w=-0.032 1/V`	Body-bias coefficient of narrow-width effects.
`a0=1`	Nonuniform depletion width effect coefficient.
`b0=0 m`	Bulk charge coefficient due to narrow width effect.
`b1=0 m`	Bulk charge coefficient due to narrow width effect.
`a1=0 1/V`	No-saturation coefficient.
`a2=1`	No-saturation coefficient.
`ags=0 1/v`	Gate-bias dependence of Abulk.
`keta=-0.047 1/V`	Body-bias coefficient for non-uniform depletion width effect.
`vfbflag=0`	49 Vfb selector.
`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.

© 2023 Cadence Design Systems, Inc.

`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.

Process parameters

`nsub=6e16 cm`$^{-3}$	Substrate doping concentration.
`nch=1.7e17 cm`$^{-3}$	Peak channel doping concentration.
`ngate=0 cm`$^{-3}$	Poly-gate doping concentration.
`xj=0.15e-6 m`	Source/drain junction depth.
`lint=0 m`	Lateral diffusion for one side.
`wint=0 m`	Width reduction for one side.
`ll=0 m^lln`	Length dependence of delta L.
`lln=1`	Length exponent of delta L.
`lw=0 m^lwn`	Width dependence of delta L.
`lwn=1`	Width exponent of delta L.
`lwl=0 m^lwn+lln`	Area dependence of delta L.
`wl=0 m^wln`	Length dependence of delta W.
`wln=1`	Length exponent of delta W.
`ww=0 m^wwn`	Width dependence of delta W.
`wwn=1`	Width exponent of delta W.
`wwl=0 m^wwn+wln`	Area dependence of delta W.
`dwg=0 m/v`	Gate-bias dependence of channel width.
`dwb=0 m/v`	Body-bias dependence of channel width.
`tox=1.5e-8 m`	Gate oxide thickness.
`dtoxcv=0.0 m`	Delta oxide thickness.
`toxm=tox m`	Tox at which parameters were extracted.
`toxe=tox m`	Electrical gate equivalent oxide thickness.

© 2023 Cadence Design Systems, Inc.

`xt=1.55e-7 m`	Doping depth.
`rdsw=0 ohm µm^wr`	Width dependence of drain-source resistance.
`prwb=0 1/|v`	Body-effect coefficient for Rds.
`prwg=0 1/V`	Gate-effect coefficient for Rds.
`wr=1`	Width offset for parasitic resistance.
`binunit=1`	Bin parameter unit selector. 1 for microns and 2 for meters.
`binflag=0`	49 binning factor.
`lref=1.0e20`	49 binning length factor.
`wref=1.0e20`	49 binning width factor.

Mobility parameters

`mobmod=1`	Mobility model selector.
`u0=670`	Low-field surface mobility at `tnom`. Default is 250 for PMOS Mobility can also be specified in M2/Vs.
`vsat=8e4 m/s`	Carrier saturation velocity at `tnom`.
`ua=2.25e-9 m/v`	First-order mobility reduction coefficient.
`ub=5.87e-19 m`^{2}`/v`^{2}	Second-order mobility reduction coefficient.
`uc=-4.65e-11 m/v`^{2}	Body-bias dependence of mobility. Default is -0.046 and unit is 1/V for mobmod=3.

Output resistance parameters

`drout=0.56`	DIBL effect on output resistance coefficient.
`pclm=1.3`	Channel length modulation coefficient.
`pdiblc1=0.39`	First coefficient of drain-induced barrier lowering.
`pdiblc2=8.6e-3`	Second coefficient of drain-induced barrier lowering.

© 2023 Cadence Design Systems, Inc.

`pdiblcb=0 1/V`	Body-effect coefficient for DIBL.
`pscbe1=4.24e8 V/m`	First coefficient of substrate current body effect.
`pscbe2=1e-5 m/v`	Second coefficient of substrate current body effect.
`pvag=0`	Gate dependence of Early voltage.
`delta=0.01 V`	Effective drain voltage smoothing parameter.

Subthreshold parameters

`cdsc=2.4e-4 F/m`^{2}	Source/drain and channel coupling capacitance.
`cdscb=0 F/m`^{2} `V`	Body-bias dependence of `cdsc`.
`cdscd=0 F/m`^{2} `V`	Drain-bias dependence of `cdsc`.
`nfactor=1`	Subthreshold swing coefficient.
`cit=0 F/m`^{2}	Interface trap parameter for subthreshold swing.
`voff=-0.08 V`	Threshold voltage offset.
`dsub=drout`	DIBL effect in subthreshold region.
`eta0=0.08`	DIBL coefficient subthreshold region.
`etab=-0.07 1/V`	Body-bias dependence of `et0`.

Substrate current parameters

`alpha0=0 m/v`	Substrate current impact ionization coefficient.
`alpha1=0 1/V`	Substrate current impact ionization coefficient.
`beta0=30 V`	Substrate current impact ionization exponent.

Parasitic resistance parameters

`rsh=0 Ω/sqr`	Source/drain diffusion sheet resistance.
`rs=0 Ω`	Source resistance.
`rd=0 Ω`	Drain resistance.

© 2023 Cadence Design Systems, Inc.

`lgcs=0 m`	Gate-to-contact length of source side.
`lgcd=0 m`	Gate-to-contact length of drain side.
`rsc=0 Ω`	Source contact resistance.
`rdc=0 Ω`	Drain contact resistance.
`rss=0 Ω m`	Scalable source resistance.
`rdd=0 Ω m`	Scalable drain resistance.
`sc=infinity m`	Spacing between contacts.
`ldif=0 m`	Lateral diffusion beyond the gate.
`hdif=0 m`	Length of heavily doped diffusion.
`minr=0.001 Ω`	Minimum source/drain resistance.

Junction diode model parameters

`js (A/m`^{2}`)`	Bulk junction reverse saturation current density.
`jsw=0 A/m`	Sidewall junction reverse saturation current density.
`jssw=0 A/m`	Alias of jsw.
`is=1e-14 A`	Bulk junction reverse saturation current.
`n=1`	Junction emission coefficient.
`nj=1`	Junction emission coefficient.
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`. Possible values are `yes` and `no`.
`imelt=`imaxA'`	Explosion current.
`ijth (A)`	Alias to `imelt`.
`jmelt=`jmaxA/m'`^{2}	Explosion current density.
`vnds=-1`	Reverse diode current transition point.
`nds=1`	Reverse bias slope coefficient.
`tt=0.0 s`	Transit time, spice compatible parameter.

© 2023 Cadence Design Systems, Inc.

Overlap capacitance parameters

`cgso (F/m)`	Gate-source overlap capacitance.
`cgdo (F/m)`	Gate-drain overlap capacitance.
`cgbo=2 Dwc Cox F/m`	Gate-bulk overlap capacitance. The default value is 0 if version=3.0.
`meto=0 m`	Metal overlap in fringing field.
`cgsl=0 F/m`	Gate-source overlap capacitance in LDD region.
`cgdl=0 F/m`	Gate-drain overlap capacitance in LDD region.
`ckappa=0.6 V`	Overlap capacitance fitting parameter.

Junction capacitance model parameters

`cbs=0 F`	Bulk-source zero-bias junction capacitance.
`cbd=0 F`	Bulk-drain zero-bias junction capacitance.
`cj=5e-4 F/m`^{2}	Zero-bias junction bottom capacitance density.
`mj=1/2`	Bulk junction bottom grading coefficient.
`pb=1 V`	Bulk junction built-in potential.
`fc=0.5`	Forward-bias depletion capacitance threshold.
`cjsw=5e-10 F/m`	Zero-bias junction sidewall capacitance density.
`mjsw=0.33`	Bulk junction sidewall grading coefficient.
`pbsw=1 V`	Side-wall junction built-in potential.
`cjswg=cjsw F/m`	Zero-bias gate-side junction capacitance density.
`mjswg=mjsw`	Gate-side junction grading coefficient.
`pbswg=pbsw V`	Gate-side junction built-in potential.
`fcsw=0.5`	Side-wall forward-bias depletion capacitance threshold.

© 2023 Cadence Design Systems, Inc.

Charge model selection parameters

capmod=2	Intrinsic charge model.
nqsmod=0	Non-quasi static model selector. Set to 1 to turn on nqs.
acnqsmod=0	AC Non-quasi static model selector. Set to 1 to turn on nqs.
dwc=wint m	Delta W for capacitance model.
dlc=lint m	Delta L for capacitance model.
clc=1e-7 m	Intrinsic capacitance fitting parameter.
cle=0.6	Intrinsic capacitance fitting parameter.
cf (F/m)	Fringe capacitance parameter.
elm=5	Elmore constant of the channel.
vfbcv=-1	Flat-band voltage for capmod=0.
acde=1 m/v	CV parameter.
moin=15	CV parameter.
noff=1	Transition parameter.
voffcv=0	Transition parameter.
xpart=0	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
llc=ll m^lln	Length dependence of delta L for CV.
lwc=lw m^lwn	Width dependence of delta L for CV.
lwlc=lwl m^lwn+lln	Area dependence of delta L for CV.
wlc=wl m^wln	Length dependence of delta W for CV.
wwc=ww m^wwn	Width dependence of delta W for CV.
wwlc=wwl m^wln+wwn	Area dependence of delta W for CV.
wmlt=1.0	Width shrink reduction factor.
lmlt=1.0	Length shrink reduction factor.

© 2023 Cadence Design Systems, Inc.

Default for instance parameters

`w=5e-6 m`	Default channel width.
`l=5e-6 m`	Default channel length.
`as=0 m`^{2}	Default area of source diffusion.
`ad=0 m`^{2}	Default area of drain diffusion.
`ps=0 m`	Default perimeter of source diffusion.
`pd=0 m`	Default perimeter of drain diffusion.
`nrd=0 m/m`	Default number of squares of drain diffusion.
`nrs=0 m/m`	Default number of squares of source diffusion.
`version=3.1`	Model parameter "version" only accepts real number value, like 3.21 for version=3.2.1. The available versions are 3.1(3.1.0), 3.2(3.2.0), 3.21(3.2.1), 3.22(3.2.2), 3.23(3.2.3), 3.24(3.2.4) and 3.3(3.3.0).
`paramchk=1`	Model parameter checking selector.
`fullreinit=0`	Model parameter full reinit selector.
`level=11`	BSIM3v3 model selector. The available level are 11, 49 and 53.
`acm=0`	BSIM3v3 area calculation method selector.
`geo=0`	geometry selector.
`calcacm=0`	49 geometry factor.

Temperature effects parameters

`tnom (C)`	Parameters measurement temperature. Default set by `options`.
`trise=0 C`	Temperature rise from ambient.
`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eg=1.12452 V`	Energy band gap. Defaulted as 1.16 when spice compatible and 1.11 when tlev is 0 or 1 for spice.

© 2023 Cadence Design Systems, Inc.

`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.
`eglev=0`	DC temperature selector.
`diomod=1`	a flag to select junction model.diomod=1 junction model described in Common MOSFET Equations section will be used. diomod=0 Berkeley junction model is used.diomod=100 TSMC special diode model .
`kt1=-0.11 V`	Temperature coefficient for threshold voltage.
`kt1l=0 v m`	Temperature coefficient for threshold voltage.
`kt2=0.022`	Temperature coefficient for threshold voltage.
`at=3.3e4 m/s`	Temperature coefficient for `vsat`.
`ua1=4.31e-9 m/v`	Temperature coefficient for `ua`.
`ub1=-7.61e-18` m^2/v^2	Temperature coefficient for `ub`.
`uc1=-5.5e-11` m/v^2	Temperature coefficient for `uc`. Default is -0.056 for mobmod=3.
`prt=0` Ω	Temperature coefficient for Rds.
`trs=0 1/C`	Temperature parameter for source resistance.
`trd=0 1/C`	Temperature parameter for drain resistance.
`ute=-1.5`	Mobility temperature exponent.
`xti=3`	Saturation current temperature exponent.
`pta=0 V/C`	Junction potential temperature coefficient.
`tpb=0 V/C`	Temperature coefficient for `pb`.
`ptp=0 V/C`	Sidewall junction potential temperature coefficient.
`tpbsw=0 V/C`	Temperature coefficient for `pbsw`.
`tpbswg=0 V/C`	Temperature coefficient for `pbswg`.
`cta=0 1/C`	Junction capacitance temperature coefficient.
`tcj=0 1/C`	Temperature coefficient for `cj`.
`ctp=0 1/C`	Sidewall junction capacitance temperature coefficient.

© 2023 Cadence Design Systems, Inc.

`tcjsw=0 1/C`	Temperature coefficient for `cjsw`.
`tcjswg=0 1/C`	Temperature coefficient for `cjswg`.

Noise model parameters

`noimod=1`	Noise model selector.
`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`ef=1`	Flicker (1/f) noise frequency exponent.
`noia=1e20`	Oxide trap density coefficient. Default is 9.9e18 for pmos.
`noib=5e4`	Oxide trap density coefficient. Default is 2.4e3 for pmos.
`noic=-1.4e-12`	Oxide trap density coefficient. Default is 1.4e-12 for pmos.
`noid=2e14`	flicker noise subthreshold-above threshold transition coefficient.
`wnoi=1e-5 m`	Channel width at which noise parameters were extracted.
`em=4.1e7 V/m`	Maximum electric field.
`flkmod=0`	Flicker noise model (0 for Ids based model, 1 for gm based model).
`gamma=2.0/3.0`	Thermal noise coefficient.
`nlev=2.0`	49 noise selector.
`gdsnoi=1.0`	Channel thermal noise coefficient for 49 noise.
`lintnoi=0 m`	Lint offset for noise calculation.

Gate-Induced drain leakage parameters

`agidl=0.0 1/Ω`	Pre-exponential coefficient for GIDL.
`bgidl=2.3e9 V/m`	Exponential coefficient for GIDL.

© 2023 Cadence Design Systems, Inc.

`cgidl=0.5 V`^{3}	Parameter for body-bias effect on GIDL.
`egidl=0.8 V`	Fitting parameter for band bending for GIDL.
`agisl=agidl 1/Ω`	Pre-exponential coefficient for GISL.
`bgisl=bgidl V/m`	Exponential coefficient for GISL.
`cgisl=cgidl V`^{3}	Parameter for body-bias effect on GISL.
`egisl=egidl V`	Fitting parameter for band bending for GISL.

Gate leak current parameters

`bforward=0`	Forward gate leakage current coefficient in pow().
`breverse=0`	Reverse gate leakage current coefficient in pow().
`cforward=0`	Forward gate leakage current coefficient in exp().
`creverse=0`	Reverse gate leakage current coefficient in exp().
`tcc=0`	Gate leakage current temperature coefficient.
`aigbinv=1.11e-2 F/g s/m`	Parameter for Igb in inversion.
`bigbinv=9.49e-4 F/g s/(m V)`	Parameter for Igb in inversion.
`cigbinv=0.006 1/V`	Parameter for Igb in inversion.
`eigbinv=1.1 V`	Parameter for Igb in inversion.
`nigbinv=3.0`	Parameter for Igb in inversion.
`aigbacc=1.36e-2 F/g s/m`	Parameter for Igb in accumulation.
`bigbacc=1.71e-3 F/g s/(m V)`	Parameter for Igb in accumulation.
`cigbacc=0.075 1/V`	Parameter for Igb in accumulation.
`nigbacc=1.0`	Parameter for Igb in accumulation.

© 2023 Cadence Design Systems, Inc.

`aigsd=1.36e-2(nmos) / 9.80e-3(pmos)`	`F/g  s/m` Parameter for Igs and Igd.
`bigsd=1.71e-3(nmos) / 7.59e-4(pmos)`	`F/g  s/(m V)` Parameter for Igs and Igd.
`cigsd=0.075(nmos) / 0.03(pmos)`	`1/V` Parameter for Igs and Igd.
`aigc=1.36e-2(nmos) / 9.80e-3(pmos)`	`F/g  s/m` Parameter for Igcs and Igcd.
`bigc=1.71e-3(nmos) / 7.59e-4(pmos)`	`F/g  s/(m V)` Parameter for Igcs and Igcd.
`cigc=0.075(nmos) / 0.03(pmos)`	`1/V` Parameter for Igcs and Igcd.
`nigc=1.0`	Parameter for Igcs, Igcd ,Igs and Igd.
`pigcd=1.0`	Vds dependence of Igcs and Igcd.
`dlcig=`Lintm'`	Source/drain overlap length for Igs and Igd.
`ntox=1.0`	Exponent for the gate oxide ratio.
`toxref=3.0e-9 m`	Nominal gate oxide thickness for gate dielectric tunneling current model only.
`poxedge=1.0`	Factor for the gate oxide thickness in source/drain overlap regions.
`igcmod=0`	Gate-to-channel and gate-to-source, gate-to-drain tunneling model selector.
`igbmod=0`	Gate-to-substrate tunneling model selector.

Auto Model Selector parameters

`wmax=1 m`	Maximum channel width for which the model is valid.
`wmin=0 m`	Minimum channel width for which the model is valid.
`lmax=1 m`	Maximum channel length for which the model is valid.
`lmin=0 m`	Minimum channel length for which the model is valid.

© 2023 Cadence Design Systems, Inc.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, and `rev`.
`imax=1 A`	Maximum allowable current.
`jmax=1e8 A/m`^{2}	Maximum allowable current density.
`bvj=infinity V`	Junction reverse breakdown voltage.
`vbox=3e9 tox V`	Oxide breakdown voltage.
`warn=on`	Parameter to turn warnings on and off. Possible values are `off` and `on`.
`apwarn=0`	Warning message flag.

Safe Operating Areas Parameters

`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.
`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.

© 2023 Cadence Design Systems, Inc.

`vgbr_max=vgb_max V`	
	Maximum allowed reverse voltage cross gate and bulk.
`vbsr_max=vbs_max V`	
	Maximum allowed reverse voltage cross bulk and source.
`vbdr_max=vbd_max V`	
	Maximum allowed reverse voltage cross bulk and drain.

Length dependent parameters

`lvtho=0`	Length dependence of Vth0.
`lvth0`	Alias of lvtho.
`lk1=0`	Length dependence of k1.
`lk2=0`	Length dependence of k2.
`lk3=0`	Length dependence of k3.
`lk3b=0`	Length dependence of k3b.
`lw0=0`	Length dependence of w0.
`lnlx=0`	Length dependence of nlx.
`lgamma1=0`	Length dependence of gamma1.
`lgamma2=0`	Length dependence of gamma2.
`lvbx=0`	Length dependence of vbx.
`lvbm=0`	Length dependence of vbm.
`ldvt0=0`	Length dependence of dvt0.
`ldvt1=0`	Length dependence of dvt1.
`ldvt2=0`	Length dependence of dvt2.
`ldvt0w=0`	Length dependence of dvt0w.
`ldvt1w=0`	Length dependence of dvt1w.
`ldvt2w=0`	Length dependence of dvt2w.
`la0=0`	Length dependence of a0.

© 2023 Cadence Design Systems, Inc.

`lb0=0`	Length dependence of b0.
`lb1=0`	Length dependence of b1.
`la1=0`	Length dependence of a1.
`la2=0`	Length dependence of a2.
`lags=0`	Length dependence of ags.
`lketa=0`	Length dependence of keta.
`lnsub=0`	Length dependence of nsub.
`lnch=0`	Length dependence of nch.
`lngate=0`	Length dependence of ngate.
`lxj=0`	Length dependence of xj.
`ldwg=0`	Length dependence of dwg.
`ldwb=0`	Length dependence of dwb.
`lxt=0`	Length dependence of xt.
`lrdsw=0`	Length dependence of rdsw.
`lprwb=0`	Length dependence of prwb.
`lprwg=0`	Length dependence of prwg.
`lwr=0`	Length dependence of wr.
`lu0=0`	Length dependence of u0.
`lvsat=0`	Length dependence of vsat.
`lua=0`	Length dependence of ua.
`lub=0`	Length dependence of ub.
`luc=0`	Length dependence of uc.
`ldrout=0`	Length dependence of drout.
`lpclm=0`	Length dependence of pclm.
`lpdiblc1=0`	Length dependence of pdiblc1.
`lpdiblc2=0`	Length dependence of pdiblc2.
`lpdiblcb=0`	Length dependence of pdiblcb.
`lpscbe1=0`	Length dependence of pscbe1.
`lpscbe2=0`	Length dependence of pscbe2.

© 2023 Cadence Design Systems, Inc.

`lpvag=0`	Length dependence of pvag.
`ldelta=0`	Length dependence of delta.
`lcdsc=0`	Length dependence of cdsc.
`lcdscb=0`	Length dependence of cdscb.
`lcdscd=0`	Length dependence of cdscd.
`lnfactor=0`	Length dependence of nfactor.
`lcit=0`	Length dependence of cit.
`lvoff=0`	Length dependence of voff.
`ldsub=0`	Length dependence of dsub.
`leta0=0`	Length dependence of eta0.
`letab=0`	Length dependence of etab.
`lalpha0=0`	Length dependence of alpha0.
`lalpha1=0`	Length dependence of alpha1.
`lbeta0=0`	Length dependence of beta0.
`lcgsl=0`	Length dependence of cgsl.
`lcgdl=0`	Length dependence of cgdl.
`lckappa=0`	Length dependence of ckappa.
`lclc=0`	Length dependence of clc.
`lcle=0`	Length dependence of cle.
`lcf=0`	Length dependence of cf.
`lelm=0`	Length dependence of elm.
`lvfbcv=0`	Length-dependence of vfbc.
`lvfb=0`	Length dependence of lvfb.
`lacde=0`	Length dependence of acde.
`lmoin=0`	Length dependence of moin.
`lnoff=0`	Length dependence of noff.
`lvoffcv=0`	Length dependence of voffcv.
`lkt1=0`	Length dependence of kt1.
`lkt1l=0`	Length dependence of kt1l.

© 2023 Cadence Design Systems, Inc.

`lkt2=0`	Length dependence of kt2.
`lat=0`	Length dependence of at.
`lua1=0`	Length dependence of ua1.
`lub1=0`	Length dependence of ub1.
`luc1=0`	Length dependence of uc1.
`lprt=0`	Length dependence of prt.
`lute=0`	Length dependence of ute.
`xl=0 m`	Length variation due to masking and etching.
`xlref=0 m`	Length variation due to masking and etching.
`lagidl=0.0`	Length dependence of agidl.
`lbgidl=0.0`	Length dependence of bgidl.
`lcgidl=0.0`	Length dependence of cgidl.
`legidl=0.0`	Length dependence of egidl.

Width dependent parameters

`wvtho=0`	Width dependence of Vth0.
`wvth0`	Alias of wvtho.
`wk1=0`	Width dependence of k1.
`wk2=0`	Width dependence of k2.
`wk3=0`	Width dependence of k3.
`wk3b=0`	Width dependence of k3b.
`ww0=0`	Width dependence of w0.
`wnlx=0`	Width dependence of nlx.
`wgamma1=0`	Width dependence of gamma1.
`wgamma2=0`	Width dependence of gamma2.
`wvbx=0`	Width dependence of vbx.
`wvbm=0`	Width dependence of vbm.
`wdvt0=0`	Width dependence of dvt0.

© 2023 Cadence Design Systems, Inc.

wdvt1=0	Width dependence of dvt1.
wdvt2=0	Width dependence of dvt2.
wdvt0w=0	Width dependence of dvt0.
wdvt1w=0	Width dependence of dvt1w.
wdvt2w=0	Width dependence of dvt2w.
wa0=0	Width dependence of a0.
wb0=0	Width dependence of b0.
wb1=0	Width dependence of b1.
wa1=0	Width dependence of a1.
wa2=0	Width dependence of a2.
wags=0	Width dependence of ags.
wketa=0	Width dependence of keta.
wnsub=0	Width dependence of nsub.
wnch=0	Width dependence of nch.
wngate=0	Width dependence of ngate.
wxj=0	Width dependence of xj.
wdwg=0	Width dependence of dwg.
wdwb=0	Width dependence of dwb.
wxt=0	Width dependence of xt.
wrdsw=0	Width dependence of rdsw.
wprwb=0	Width dependence of prwb.
wprwg=0	Width dependence of prwg.
wwr=0	Width dependence of wr.
wu0=0	Width dependence of u0.
wvsat=0	Width dependence of vsat.
wua=0	Width dependence of ua.
wub=0	Width dependence of ub.
wuc=0	Width dependence of uc.
wdrout=0	Width dependence of drout.

© 2023 Cadence Design Systems, Inc.

wpclm=0	Width dependence of pclm.
wpdiblc1=0	Width dependence of pdiblc1.
wpdiblc2=0	Width dependence of pdiblc2.
wpdiblcb=0	Width dependence of pdiblcb.
wpscbe1=0	Width dependence of pscbe1.
wpscbe2=0	Width dependence of pscbe2.
wpvag=0	Width dependence of pvag.
wdelta=0	Width dependence of delta.
wcdsc=0	Width dependence of cdsc.
wcdscb=0	Width dependence of cdscb.
wcdscd=0	Width dependence of cdscd.
wnfactor=0	Width dependence of nfactor.
wcit=0	Width dependence of cit.
wvoff=0	Width dependence of voff.
wdsub=0	Width dependence of dsub.
weta0=0	Width dependence of eta0.
wetab=0	Width dependence of etab.
walpha0=0	Width dependence of alpha0.
walpha1=0	Width dependence of alpha1.
wbeta0=0	Width dependence of beta0.
wcgsl=0	Width dependence of cgsl.
wcgdl=0	Width dependence of cgdl.
wckappa=0	Width dependence of ckappa.
wclc=0	Width dependence of clc.
wcle=0	Width dependence of cle.
wcf=0	Width dependence of cf.
welm=0	Width dependence of el.
wvfbcv=0	Width-dependence of vfbcv.
wvfb=0	Width dependence of lvfb.

© 2023 Cadence Design Systems, Inc.

wacde=0	Width dependence of acde.
wmoin=0	Width dependence of moin.
wnoff=0	Width dependence of noff.
wvoffcv=0	Width dependence of voffcv.
wkt1=0	Width dependence of kt1.
wkt1l=0	Width dependence of kt1l.
wkt2=0	Width dependence of kt2.
wat=0	Width dependence of at.
wua1=0	Width dependence of ua1.
wub1=0	Width dependence of ub1.
wuc1=0	Width dependence of uc1.
wprt=0	Width dependence of prt.
wute=0	Width dependence of ute.
xw=0 m	Width variation due to masking and etching.
xwref=0 m	Width variation due to masking and etching.
wagidl=0.0	Width dependence of agidl.
wbgidl=0.0	Width dependence of bgidl.
wcgidl=0.0	Width dependence of cgidl.
wegidl=0.0	Width dependence of egidl.

Cross-term dependent parameters (Not listed)

pvtho=0	Product dependence of Vth0.
pvth0	Alias of pvtho.
pk1=0	Product dependence of k1.
pk2=0	Product dependence of k2.
pk3=0	Product dependence of k3.
pk3b=0	Product dependence of k3b.
pw0=0	Product dependence of w0.

© 2023 Cadence Design Systems, Inc.

pnlx=0	Product dependence of nlx.
pgamma1=0	Product dependence of gamma1.
pgamma2=0	Product dependence of gamma2.
pvbx=0	Product dependence of vbx.
pvbm=0	Product dependence of vbm.
pdvt0=0	Product dependence of dvt0.
pdvt1=0	Product dependence of dvt1.
pdvt2=0	Product dependence of dvt2.
pdvt0w=0	Product dependence of dvt0w.
pdvt1w=0	Product dependence of dvt1w.
pdvt2w=0	Product dependence of dvt2w.
pa0=0	Product dependence of a0.
pb0=0	Product dependence of b0.
pb1=0	Product dependence of b1.
pa1=0	Product dependence of a1.
pa2=0	Product dependence of a2.
pags=0	Product dependence of ags.
pketa=0	Product dependence of keta.
pnsub=0	Product dependence of nsub.
pnch=0	Product dependence of nch.
pngate=0	Product dependence of ngate.
pxj=0	Product dependence of xj.
pdwg=0	Product dependence of dwg.
pdwb=0	Product dependence of dwb.
pxt=0	Product dependence of xt.
prdsw=0	Product dependence of rdsw.
pprwb=0	Product dependence of prwb.
pprwg=0	Product dependence of prwg.
pwr=0	Product dependence of wr.

© 2023 Cadence Design Systems, Inc.

`pu0=0`	Product dependence of u0.
`pvsat=0`	Product dependence of vsat.
`pua=0`	Product dependence of ua.
`pub=0`	Product dependence of ub.
`puc=0`	Product dependence of uc.
`pdrout=0`	Product dependence of drout.
`ppclm=0`	Product dependence of pclm.
`ppdiblc1=0`	Product dependence of pdiblc1.
`ppdiblc2=0`	Product dependence of pdiblc2.
`ppdiblcb=0`	Product dependence of pdiblcb.
`ppscbe1=0`	Product dependence of pscbe1.
`ppscbe2=0`	Product dependence of pscbe2.
`ppvag=0`	Product dependence of pvag.
`pdelta=0`	Product dependence of delta.
`pcdsc=0`	Product dependence of cdsc.
`pcdscb=0`	Product dependence of cdscb.
`pcdscd=0`	Product dependence of cdscd.
`pnfactor=0`	Product dependence of nfactor.
`pcit=0`	Product dependence of cit.
`pvoff=0`	Product dependence of voff.
`pdsub=0`	Product dependence of dsub.
`peta0=0`	Product dependence of eta0.
`petab=0`	Product dependence of etab.
`palpha0=0`	Product dependence of alpha0.
`palpha1=0`	Product dependence of alpha1.
`pbeta0=0`	Product dependence of beta0.
`pcgsl=0`	Product dependence of cgsl.
`pcgdl=0`	Product dependence of cgdl.
`pckappa=0`	Product dependence of ckappa.

© 2023 Cadence Design Systems, Inc.

`pclc=0`	Product dependence of clc.
`pcle=0`	Product dependence of cle.
`pcf=0`	Product dependence of cf.
`pelm=0`	Product dependence of elm.
`pvfbcv=0`	Product dependence of vfbcv.
`pvfb=0`	Product dependence of lvfb.
`pacde=0`	Product dependence of acde.
`pmoin=0`	Product dependence of moin.
`pnoff=0`	Product dependence of noff.
`pvoffcv=0`	Product dependence of voffcv.
`pkt1=0`	Product dependence of kt1.
`pkt1l=0`	Product dependence of kt1l.
`pkt2=0`	Product dependence of kt2.
`pat=0`	Product dependence of at.
`pua1=0`	Product dependence of ua1.
`pub1=0`	Product dependence of ub1.
`puc1=0`	Product dependence of uc1.
`pprt=0`	Product dependence of prt.
`pute=0`	Product dependence of ute.
`pagidl=0.0`	Cross-term dependence of agidl.
`pbgidl=0.0`	Cross-term dependence of bgidl.
`pcgidl=0.0`	Cross-term dependence of cgidl.
`pegidl=0.0`	Cross-term dependence of egidl.

DC-mismatch dependent parameters

`mvtwl=0.0 v m`	Threshold mismatch area dependence.
`mvtwl2=0.0 v m^1.5`	Threshold mismatch area square dependence.

© 2023 Cadence Design Systems, Inc.

`mvt0=0.0 V`	Threshold mismatch intercept.
`mbewl=0.0 m`	Beta mismatch area dependence.
`mbe0=0.0`	Beta mismatch intercept.
`mismatchmod=0`	select Mismatch mode. The available modes are 0, 1, 2 and 3.
`mismatchdist=0 m`	Mismatch Distance.

LOD model parameters

`stimod=1`	LOD stress effect model selector. 0 for no LOD, 1 for UCB LOD, 2 for TSMC LOD.
`sa0=1e-6 m`	reference distance between od edge to poly of one side.
`saref (m)`	Alias to Sa0.
`sb0=1e-6 m`	reference distance between od edge to poly of the other side.
`sbref (m)`	Alias to sb0.
`wlod=0 m`	length parameter for stress effect.
`ku0=0 m`	mobility degradation/enhancement coefficient for stress effect.
`kvsat=0`	saturation velocity degradation/enhancement parameter for stress effect.
`kvth0=0 v m`	threshold shift parameter for stress effect.
`tku0=0`	temperature coefficient of ku0.
`llodku0=0`	length parameter for u0 stress effect.
`wlodku0=0`	width parameter for u0 stress effect.
`llodvth=0`	length parameter for vth stress effect.
`wlodvth=0`	width parameter for vth stress effect.
`lku0=0 m^llodku0`	length dependence of ku0.
`wku0=0 m^wlodku0`	width dependence of ku0.
`pku0=0 m^(llodku0+wlodku0)`	

© 2023 Cadence Design Systems, Inc.

	cross-term dependence of ku0.
`lkvth0=0 v m^llodku0`	
	length dependence of kvth0.
`wkvth0=0 v m^wlodku0`	
	width dependence of kvth0.
`pkvth0=0 v m^(llodku0+wlodku0)`	
	cross-term dependence of kvth0.
`stk2=0 m`	k2 shift factor related to vth0 change.
`lodk2=0`	k2 shift modification factor for stress effect.
`steta0=0 m`	eta0 shift factor related to vth0 change.
`lodeta0=0`	eta0 shift modification factor for stress effect.
`wpemod=0`	Flag for WPE model (WPEMOD=1 to activate this model) .
`web=0.0`	Coefficient for SCB.
`wec=0.0`	Coefficient for SCC.
`kvth0we=0.0 V`	Threshold shift factor for well proximity effect .
`k2we=0.0`	K2 shift factor for well proximity effect.
`lkvth0we=0.0 V`	Length dependence of kvth0we.
`wkvth0we=0.0 V`	Width dependence of kvth0we .
`pkvth0we=0.0 V`	Cross-term dependence of kvth0we .
`lk2we=0.0`	Length dependence of k2we.
`wk2we=0.0`	Width dependence of k2we.
`pk2we=0.0`	Cross-term dependence of k2we.
`ku0we=0.0`	Mobility degradation factor for well proximity effect .
`lku0we=0.0`	Length dependence of ku0we.
`wku0we=0.0`	Width dependence of ku0we.
`pku0we=0.0`	Cross-term dependence of ku0we.
`scref=1.0e-6 m`	Reference distance to calculate SCA, SCB and SCC .

© 2023 Cadence Design Systems, Inc.

TSMC junction diode model parameters

`jtss=0 A/m`^{2}	Source bottom trap-assisted saturation current density.
`jtsd=0 A/m`^{2}	Drain bottom trap-assisted saturation current density.
`jtssws=0 A/m`	Source isolation-edge sidewall trap-assisted saturation current density.
`jtsswd=0 A/m`	Drain isolation-edge sidewall trap-assisted saturation current density.
`jtsswgs=0 A/m`	Source Gate-edge isolation-edge sidewall trap-assisted saturation current density.
`jtsswgd=0 A/m`	Drain isolation-edge sidewall trap-assisted saturation current density.
`njts=60`	Non-ideality factor for Jtss and Jtsd.
`njtssw=60`	Non-ideality factor for Jtssws and Jtsswd.
`njtsswg=20`	Non-ideality factor for Jtsswgs and Jtsswgd.
`njtsd=njts`	Non-ideality factor for jtsd.
`njtsswd=njtssw`	Non-ideality factor for jtsswd.
`njtsswgd=njtsswg`	Non-ideality factor for jtsswgd.
`mnr=21`	Fitting parameter for resistance induced non-ideality factor.
`bnr=0`	Fitting parameter for resistance induced non-ideality factor.
`cnr=0 1/v m`	Fitting parameter for resistance induced non-ideality factor.
`dnr=0 1/v`	Fitting parameter for resistance induced non-ideality factor.
`xtss=0.02`	Power dependence of Jtss on temperature.
`xtsd=0.02`	Power dependence of Jtsd on temperature.
`xtssws=0.02`	Power dependence of Jtssws on temperature.
`xtsswd=0.02`	Power dependence of Jtsswd on temperature.
`xtsswgs=0.02`	Power dependence of Jtsswgs on temperature.
`xtsswgd=0.02`	Power dependence of Jtsswgd on temperature.

© 2023 Cadence Design Systems, Inc.

`tnjts=0`	Temperature coefficient for NJTS.
`tnjtssw=0`	Temperature coefficient for njtssw.
`tnjtsswg=0`	Temperature coefficient for njtsswg.
`tnjtsd=tnjts`	Temperature coefficient for njtsd.
`tnjtsswd=tnjtsssw`	Temperature coefficient for njtsswd.
`tnjtsswgd=tnjtsswg`	Temperature coefficient for njtsswgd.
`tmnr=0`	Temperature coefficient for mnr.
`tcnr=0`	Temperature coefficient for cnr.
`tdnr=0`	Temperature coefficient for dnr.
`jsswg=0`	Sidewall-gate junction reverse saturation current density.
`xjbv=1.0`	Fitting parameter for diodes breakdown.
`ijthrev=0.1`	Reverse maximum allowable current.
`nrfwd=1.0`	Nominal value of Nr for forward linearization.
`vtss=10.0 V`	Source bottom trap-assisted voltage dependent parameter.
`vtsd=`vtssV'`	Drain bottom trap-assisted voltage dependent parameter.
`vtssws=10.0 V`	Source STI sidewall trap-assisted voltage dependent parameter.
`vtsswd=`vtsswsV'`	Drain STI sidewall trap-assisted voltage dependent parameter.
`vtsswgs=10.0 V`	Source gate-edge sidewall trap-assisted voltage dependent parameter.
`vtsswgd=`vtsswgsV'`	Drain gate-edge sidewall trap-assisted voltage dependent parameter.

© 2023 Cadence Design Systems, Inc.

Shrink Parameters

`shrink=0`	linear shrink parameter.
`shrink2=0`	area shrink parameter.
`msgskip=off`	Skip some warning message customer requested. Possible values are `off` and `on`.
`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, `tispice`, and `pspice`.

Imax and Imelt

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below 'imax' or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and a warning is printed out.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, the base and collector currents are composed of many exponential terms, a warning will be issued and the results become inaccurate. The junction current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

Both of these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

Auto Model Selection

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening

© 2023 Cadence Design Systems, Inc.

brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin` should be given. The selection criteria to choose a model is as follows:

lmin <= inst_length < lmax and wmin <= inst_width < wmax

Example:

model ModelName ModelType {

1: <model parameters> lmin=2 lmax=4 wmin=1 wmax=2

2: <model parameters> lmin=1 lmax=2 wmin=2 wmax=4

3: <model parameters> lmin=2 lmax=4 wmin=4 wmax=6

}

Then for a given instance

M1 1 2 3 4 ModelName w=3 l=1.5

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`weff (m)`	Effective channel width (alias=lv2).
`leff (m)`	Effective channel length (alias=lv1).
`rseff (Ω)`	Effective source resistance (alias=lv17).
`rdeff (Ω)`	Effective drain resistance (alias=lv16).
`aseff (m^2)`	Effective source area (alias=lv4).

© 2023 Cadence Design Systems, Inc.

adeff (m^2)	Effective drain area (alias=lv3).
pseff (m)	Effective source perimeter (alias=lv12).
pdeff (m)	Effective drain perimeter (alias=lv11).

Operating-Point Parameters

region=triode	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are off, triode, sat, subth, and breakdown.
trise (C)	Temperature rise from ambient.
reversed	Reverse mode indicator. Possible values are yes and no.
ids (A)	Resistive drain-to-source current (alias=lx4).
isub (A)	substrate current (alias=lx50).
vgs (V)	Gate-source voltage.
vds (V)	Drain-source voltage (alias=lx3).
vbs (V)	Bulk-source voltage.
vgb (V)	gate-bulk voltage.
vdb (V)	Drain-bulk voltage.
vgd (V)	Gate-Drain voltage.
vth (V)	Threshold voltage (alias=lv9).
vdsat (V)	Drain-source saturation voltage (alias=lv10).
vfbeff (V)	Vfb effective (alias=lv26).
gm (S)	Common-source transconductance (alias=lx7).
gds (S)	Common-source output conductance (alias=lx8).
gmbs (S)	Body-transconductance (alias=lx9).
betaeff (A/V^2)	Effective beta.
cjd (F)	Drain-bulk junction capacitance (alias=lx29).
cjs (F)	Source-bulk junction capacitance (alias=lx28).
qb (Coul)	total bulk charge (alias=lx12).

© 2023 Cadence Design Systems, Inc.

`qg (Coul)`	Total gate charge (alias=lx14).
`qd (Coul)`	Total drain charge (alias=lx16).
`qbd (Coul)`	Drain-bulk charge (alias=lx24).
`qbs (Coul)`	Source-bulk charge (alias=lx26).
`cgg (F)`	dQg_dVg (alias=lx18).
`cgd (F)`	dQg_dVd (alias=lx19).
`cgs (F)`	dQg_dVs (alias=lx20).
`cgb (F)`	dQg_dVbk.
`cdg (F)`	dQd_dVg (alias=lx32).
`cdd (F)`	Total drain capacitance (including intrinsic, overlap and fringing components, and junction capacitance) (alias=lx33).
`cds (F)`	dQd_dVs (alias=lx34).
`cdb (F)`	dQd_dVb.
`csg (F)`	dQs_dVg.
`csd (F)`	dQs_dVd.
`css (F)`	dQs_dVs.
`csb (F)`	dQs_dVb.
`cbg (F)`	dQb_dVg (alias=lx21).
`cbd (F)`	dQb_dVd (alias=lx22).
`cbs (F)`	dQb_dVs (alias=lx23).
`cbb (F)`	dQb_dVb.
`ron (Ω)`	On-resistance.
`id (A)`	Resistive drain current (alias=i1).
`is (A)`	Resistive source current (alias=i3).
`ibulk (A)`	Resistive bulk current (alias=i4).
`ibs (A)`	Source-bulk diode current (alias=lx5).
`ibd (A)`	Drain-bulk diode current (alias=lx6).
`pwr (W)`	Power at op point.

© 2023 Cadence Design Systems, Inc.

`gmoverid (1/V)`	Gm/Ids.
`ueff`	ueff.
`cgsovl (F)`	Gate-source overlap and fringing capacitance (alias=lv36).
`cgdovl (F)`	Gate-drain overlap and fringing capacitance (alias=lv37).
`cgbovl (F)`	Gate-bulk overlap capacitance (alias=lv38).
`i1 (A)`	Alias for id.
`i3 (A)`	Alias of Resistive source current.
`i4 (A)`	Alias of Resistive bulk current.
`gbd (S)`	Conductance of the drain diode (alias=lx10).
`gbs (S)`	Conductance of the source diode (alias=lx11).
`vgsteff (V)`	effective vgs.
`qinv (Coul)`	inversion charge.
`igd (A)`	Gate-to-drain leakage current.
`igs (A)`	Gate-to-source leakage current.
`igb (A)`	Gate-to-bulk tunneling current.
`igcs (A)`	Gate-to-channel (source side) tunneling current.
`igcd (A)`	Gate-to-channel (drain side) tunneling current.
`igidl (A)`	Gate-induced drain leakage current.
`igisl (A)`	Gate-induced source leakage current.
`qgi (Coul)`	Intrinsic Gate charge.
`qsi (Coul)`	Intrinsic Source charge.
`qdi (Coul)`	Intrinsic Drain charge.
`qbi (Coul)`	Intrinsic Bulk charge.
`cddbi (F)`	Intrinsic drain capacitance.
`cssbi (F)`	Intrinsic source capacitance.
`cggbi (F)`	Intrinsic gate capacitance.
`cgsbi (F)`	Intrinsic gate-to-source capacitance.

© 2023 Cadence Design Systems, Inc.

`cgdbi (F)`	Intrinsic gate-to-drain capacitance.
`cbdbi (F)`	Intrinsic bulk-to-drain capacitance.
`cbsbi (F)`	Intrinsic bulk-to-source capacitance.
`qsrco (Coul)`	Total Source charge (Charge Conservation: QS=-(QG+QD+QB)).
`ide (A)`	Total DC drain current .
`ige (A)`	Total DC gate current .
`ise (A)`	Total DC source current .
`ibe (A)`	Total DC bulk current .
`idb (A)`	DC drain-bulk current .
`isb (A)`	DC source-bulk current .
`vsb (V)`	Source-Bulk DC voltage .
`gmb (S)`	DC bulk transconductance .
`vgt (V)`	Effective gate drive voltage including back bias drain bias effects .
`vdss (V)`	Drain saturation voltage at actual bias .
`vsat_marg (V)`	Vds margin .
`self_gain`	Transistor self gain .
`rout (Ω)`	AC output resistor .
`beff (A/V`^{2}`)`	Gain factor in saturation .
`fug (Hz)`	Unity current gain frequency at actual bias .
`vearly (V)`	Equivalent early voltage.
`ft (Hz)`	Unity current gain frequency at actual bias.
`vth_drive (V)`	Effective gate drive voltage including back bias drain bias effects.
`vdsat_marg (V)`	Vds margin.
`tk (K)`	Effective temperature for a single device.
`ib (A)`	Total DC bulk current.
`ig (A)`	Total DC gate current.

© 2023 Cadence Design Systems, Inc.

`opdef`	1: Device Physics notation. 2: Circuit Simulator notation.
`ctype`	Flag for channel type of MOSFET. 1: NMOS. -1: PMOS.
`sdop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.
`sdint`	Flag for source-drain interchange. 1: No S-D interchange, -1: S-D interchange.
`dtsh (K)`	Device temperature rise due to self-heating.
`Iavl (A)`	Weak avalanche current.
`vth0 (V)`	Zero-bias threshold voltage, excluding back-bias (body effect) and drain-bias effect (DIBL).
`go (S)`	Output conductance.
`co (F)`	Output Drain-Source capacitance.
`cm (F)`	Capacitance element 1 for QS model.
`cmb (F)`	Capacitance element 2 for QS model.
`cmx (F)`	Capacitance element 3 for QS model.
`tau1 (F)`	Time constant related to NQS first frequency pole.
`fqslim (F)`	QS model frequency limit.
`gmoveri (1/V)`	Transconductance efficiency (Gm over Id or Is ratio).

Binning Parameters

The table below lists geometry sensitivity factors.

The value of a parameter is calculated from the following equation:

If `binunit` =1,

P = p0 + 1e-6 * wp0 / Weff + 1e-6 * lp0 / Leff + 1e-12 * pp0 / (Weff * Leff)

else

P = p0 + wp0 / Weff + lp0 / Leff + pp0 / (Weff * Leff)

where P is the parameter name.

© 2023 Cadence Design Systems, Inc.

Table 21-1 Binning Parameters

Parameter Name	Description
LVTO	VTO length sensitivity
WVTO	VTO width sensitivity
PVTO	VTO length and width sensitivity
LK1	K1 length sensitivity
WK1	K1 width sensitivity
PK1	K1 length and width sensitivity
LK2	K2 length sensitivity
WK2	K2 width sensitivity
PK2	K2 length and width sensitivity
LDVT0	DVT0 length sensitivity
WDVT0	DVT0 width sensitivity
PDVT0	DVT0 length and width sensitivity
LDVT1	DVT1 length sensitivity
WDVT1	DVT1 width sensitivity
PDVT1	DVT1 length and width sensitivity
LDVT2	DVT2 length sensitivity
WDVT2	DVT2 width sensitivity
PDVT2	DVT2 length and width sensitivity
LDVT0W	DVT0W length sensitivity
WDVT0W	DVT0W width sensitivity
PDVT0W	DVT0W length and width sensitivity
LDVT1W	DVT1W length sensitivity
WDVT1W	DVT1W width sensitivity
PDVT1W	DVT1W length and width sensitivity
LDVT2W	DVT2W length sensitivity
WDVT2W	DVT2W width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PDVT2W	VFB length and width sensitivity
LLETA0	LETA0 length sensitivity
WLETA0	LETA0 width sensitivity
PLETA0	LETA0 length and width sensitivity
LETAB	ETAB length sensitivity
WETAB	ETAB width sensitivity
PETAB	ETAB length and width sensitivity
LNSUB	NSUB length sensitivity
WNSUB	NSUB width sensitivity
PNSUB	NSUB length and width sensitivity
LNCH	NCH length sensitivity
WNCH	NCH width sensitivity
PNCH	NCH length and width sensitivity
LNGATE	NGATE length sensitivity
WNGATE	NGATE width sensitivity
PNGATE	NGATE length and width sensitivity
LXJ	XJ length sensitivity
WXJ	XJ width sensitivity
PXJ	XJ length and width sensitivity
LU0	U0 length sensitivity
WU0	U0 width sensitivity
PU0	U0 length and width sensitivity
LVSAT	VSAT length sensitivity
WVSAT	VSAT width sensitivity
PVSAT	VSAT length and width sensitivity
LUA	UA length sensitivity
WUA	UA width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PUA	UA length and width sensitivity
LUB	UB length sensitivity
WUB	UB width sensitivity
PUB	UB length and width sensitivity
LUC	UC length sensitivity
WUC	UC width sensitivity
PUC	UC length and width sensitivity
LPCLM	PCLM length sensitivity
WPCLM	PCLM width sensitivity
PPCLM	PCLM length and width sensitivity
LPDIBLC1	PDIBLC1 length sensitivity
WPDIBLC1	PDIBLC1 width sensitivity
PPDIBLC1	PDIBLC1 length and width sensitivity
LPDIBLC2	PDIBLC2 length sensitivity
WPDIBLC2	PDIBLC2 width sensitivity
PPDIBLC2	PDIBLC2 length and width sensitivity
LPDIBLCB	PDIBLCB length sensitivity
WPDIBLCB	PDIBLCB width sensitivity
PPDIBLCB	PDIBLCB length and width sensitivity
LPSCBE2	PSCBE2 length sensitivity
WPSCBE2	PSCBE2 width sensitivity
PPSCBE2	PSCBE2 length and width sensitivity
LVOFF	VOFF length sensitivity
WVOFF	VOFF width sensitivity
PVOFF	VOFF length and width sensitivity
LRDSW	RDSW length sensitivity
WRDSW	RDSW width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PRDSW	RDSW length and width sensitivity
LPRWB	PRWB length sensitivity
WPRWB	PRWB width sensitivity
PPRWB	PRWB length and width sensitivity
LPRWG	PRWG length sensitivity
WPRWG	PRWG width sensitivity
PPRWG	PRWG length and width sensitivity
LPRT	PRT length sensitivity
WPRT	PRT width sensitivity
PPRT	PRT length and width sensitivity
LAGS	AGS length sensitivity
WAGS	AGS width sensitivity
PAGS	AGS length and width sensitivity
LPVAG	PVAG length sensitivity
WPVAG	PVAG width sensitivity
PPVAG	PVAG length and width sensitivity
LKETA	KETA length sensitivity
WKETA	KETA width sensitivity
PKETA	KETA length and width sensitivity
LELM	ELM length sensitivity
WELM	ELM width sensitivity
PELM	ELM length and width sensitivity
LUTE	UTE length sensitivity
WUTE	UTE width sensitivity
PUTE	UTE length and width sensitivity
LCDSC	CDSC length sensitivity
WCDSC	CDSC width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PCDSC	CDSC length and width sensitivity
LCDSCB	CDSCB length sensitivity
WCDSCB	CDSCB width sensitivity
PCDSCB	CDSCB length and width sensitivity
LCDSCD	CDSCD length sensitivity
WCDSCD	CDSCD width sensitivity
PCDSCD	CDSCD length and width sensitivity
LNFACTOR	NFACTOR length sensitivity
WNFACTOR	NFACTOR width sensitivity
PNFACTOR	NFACTOR length and width sensitivity
LCIT	CIT length sensitivity
WCIT	CIT width sensitivity
PCIT	CIT length and width sensitivity
LAT	AT length sensitivity
WAT	AT width sensitivity
PAT	AT length and width sensitivity
LA0	A0 length sensitivity
WA0	A0 width sensitivity
PA0	A0 length and width sensitivity
LA1	A1 length sensitivity
WA1	A1 width sensitivity
PA1	A1 length and width sensitivity
LA2	A2 length sensitivity
WA2	A2 width sensitivity
PA2	A2 length and width sensitivity
LKT1	KT1 length sensitivity
WKT1	KT1 width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PKT1	KT1 length and width sensitivity
LKT1L	KT1L length sensitivity
WKT1L	KT1L width sensitivity
PKT1L	KT1L length and width sensitivity
LKT2	KT2 length sensitivity
WKT2	KT2 width sensitivity
PKT2	KT2 length and width sensitivity
LK3	K3 length sensitivity
WK3	K3 width sensitivity
PK3	K3 length and width sensitivity
LK3B	K3B length sensitivity
WK3B	K3B width sensitivity
PK3B	K3B length and width sensitivity
LW0	W0 length sensitivity
WW0	W0 width sensitivity
PW0	W0 length and width sensitivity
LNLX	NLX length sensitivity
WNLX	NLX width sensitivity
PNLX	NLX length and width sensitivity
LDROUT	DROUT length sensitivity
WDROUT	DROUT width sensitivity
PDROUT	DROUT length and width sensitivity
LDSUB	DSUB length sensitivity
WDSUB	DSUB width sensitivity
PDSUB	DSUB length and width sensitivity
LUA1	UA1 length sensitivity
WUA1	UA1 width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PUA1	UA1 length and width sensitivity
LUB1	UB1 length sensitivity
WUB1	UB1 width sensitivity
PUB1	UB1 length and width sensitivity
LUC1	UC1 length sensitivity
WUC1	UC1 width sensitivity
PUC1	UC1 length and width sensitivity
LDELTA	DELTA length sensitivity
WDELTA	DELTA width sensitivity
PDELTA	DELTA length and width sensitivity
LB0	B0 length sensitivity
WB0	B0 width sensitivity
PB0	B0 length and width sensitivity
LB1	B1 length sensitivity
WB1	B1 width sensitivity
PB1	B1 length and width sensitivity
LWR	WR length sensitivity
WWR	WR width sensitivity
PWR	WR length and width sensitivity
LDWG	DWG length sensitivity
WDWG	DWG width sensitivity
PDWG	DWG length and width sensitivity
LDWB	DWB length sensitivity
WDWB	DWB width sensitivity
PDWB	DWB length and width sensitivity
LALPHA0	ALPHA0 length sensitivity
WALPHA0	ALPHA0 width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PALPHA0	ALPHA0 length and width sensitivity
LALPHA1	ALPHA1 length sensitivity
WALPHA1	ALPHA1 width sensitivity
PALPHA1	ALPHA1 length and width sensitivity
LBETA0	BETA0 length sensitivity
WBETA0	BETA0 width sensitivity
PBETA0	BETA0 length and width sensitivity
LDWC	DWC length sensitivity
WDWC	DWC width sensitivity
PDWC	DWC length and width sensitivity
LDLC	DLC length sensitivity
WDLC	DLC width sensitivity
PDLC	DLC length and width sensitivity
LCGSL	CGSL length sensitivity
WCGSL	CGSL width sensitivity
PCGSL	CGSL length and width sensitivity
LCGDL	CGDL length sensitivity
WCGDL	CGDL width sensitivity
PCGDL	CGDL length and width sensitivity
LCKAPPA	CKAPPA length sensitivity
WCKAPPA	CKAPPA width sensitivity
PCKAPPA	CKAPPA length and width sensitivity
LCLC	CLC length sensitivity
WCLC	CLC width sensitivity
PCLC	CLC length and width sensitivity
LCLE	CLE length sensitivity
WCLE	CLE width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PCLE	CLE length and width sensitivity
LCF	CF length sensitivity
WCF	CF width sensitivity
PCF	CF length and width sensitivity
LACDE	ACDE length sensitivity
WACDE	ACDE width sensitivity
PACDE	ACDE length and width sensitivity
LMOIN	MOIN length sensitivity
WMOIN	MOIN width sensitivity
PMOIN	MOIN length and width sensitivity
LNOFF	NOFF length sensitivity
WNOFF	NOFF width sensitivity
PNOFF	NOFF length and width sensitivity
LVOFFCV	VOFFCV length sensitivity
WVOFFCV	VOFFCV width sensitivity
PVOFFCV	VOFFCV length and width sensitivity
LGAMMA1	GAMMA1 length sensitivity
WGAMMA1	GAMMA1 width sensitivity
PGAMMA1	GAMMA1 length and width sensitivity
LGAMMA2	GAMMA2 length sensitivity
WGAMMA2	GAMMA2 width sensitivity
PGAMMA2	GAMMA2 length and width sensitivity
LVFB	VFB length sensitivity
WVFB	VFB width sensitivity
PVFB	VFB length and width sensitivity
LVFBCV	VFBCV length sensitivity
WVFBCV	VFBCV width sensitivity

© 2023 Cadence Design Systems, Inc.

Parameter Name	Description
PVFBCV	VFBCV length and width sensitivity
LVBX	VBX length sensitivity
WVBX	VBX width sensitivity
PVBX	VBX length and width sensitivity
LVBM	VBM length sensitivity
WVBM	VBM width sensitivity
PVBM	VBM length and width sensitivity
LXT	XT length sensitivity
WXT	XT width sensitivity
PXT	XT length and width sensitivity

Related Topics

BSIM3v3 Level-11 Model (bsim3v3)

LOD Model

Nonquasi-static (NQS) Model

I-V Model

Differences between BSIM3v3 Subversions

Scaling Effects (BSIM3v3)

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

22

BSIM4 Level-14 Model (bsim4)

BSIM4 model, as the extension of BSIM3v3 model, addresses more physical effects for MOSFET device of 100 nm and beyond. Gate leakage, layout dependent effects, high-K, and so on, are modeled in BSIM4.

Click the following links for information about the BSIM4 model:

- Instance
  - Instance syntax
- Model
  - Model syntax
  - Auto Model Selection
- Equivalent Circuit
- Device Regions
- Global Control Options
- JUNCAP Model
- TMI 1.0 Model
- TMI 2.0 Model
- Model Version Update
  - Version 4.30
  - Version 4.40
  - Version 4.50
  - Version 4.60
  - Version 4.61
  - Version 4.62

© 2023 Cadence Design Systems, Inc.

- Version 4.63
- Version 4.64
- Version 4.65
- Version 4.70
- Version 4.80
- Version 4.81

■ Model Equations

- Effective Oxide Thickness, Channel Length and Channel Width
- Threshold Voltage Model
- Channel Charge and Subthreshold Swing Models
- Gate Direct Tunneling Current Model
- Drain Current Model
- Body Current Model
- Capacitance Model
- Overlap Capacitance Models
- High Speed/RF Models
- Noise Models
- Asymmetric MOS Junction Diode Models
- Layout Dependent Parasitics Models
- Temperature Effects Models
- Stress Effects Models
- Well Proximity Effect Model
- TMIBSIM4 Model (tmibsim4)

■ Models and Equations in Version Updates

■ Component Statements

© 2023 Cadence Design Systems, Inc.

Instance

Instance syntax

BSIM4 instance have 4 terminals. To specify BSIM4 instance element, the ModelName has to be associated with a BSIM4 model card.

```
InstanceName (d g s b) ModelName <parameter=value> ...
```

Sample Instance Statement

```
m4 (0 2 1 1) pchmod w=2u l=0.8u as=250p ad=250p pd=168p ps=168p m=1
```

Model

Model syntax

The following syntax specifies BSIM4 model:

```
model ModelName bsim4 <parameter=value> ...
```

The third parameter, “bsim4”, is the master to indicate this model card is a BSIM4 model card.

Sample Model Statement

```
model pchmod bsim4 type=p mobmod=0 capmod=2 version=4.21 toxe=3e-9 cdsc=2.58e-4
cdscb=0 cdscd=6.1e-8 cit=0 nfactor=1.1 xj=9e-8 vfb=0.76vsat=9.2e4 at=3.3e4 a0=1.1
ags=1.0e-20 a1=0 ngate=9e19 vth0=-0.42 a2=1 delta=0.014 pvag=1e-20 pclm=6.28e-4
pdits=0.2 pditsl=2.3e6pditsd=0.23 fprout=0.2 pdiblcb=3.4e-8 pdiblc1=0.81
drout=0.56pdiblc2=9.84e-6 pscbe1=8.14e8 pscbe2=9.58e-07 lint=5e-9 wint=5e-9
dmcg=5e-6 dmci=5e-6 dmdg=5e-6 dmcgt=6e-7 dwj=4.5e-8 rsh=6cgso=7.43e-10 cgdo=7.43e-
10 cgbo=2.56e-11 cgsl=1e-14 cgdl=1e-14ckappas=0.5 ckappad=0.5 noff=0.9 voffcv=0.02
acde=1 moin=15 xpart=0kt11=0 kt2=2.2e-2 lpe0=5.75e-8 lpeb=2.3e-10 dvt0=2.89
dvt1=0.53dvt2=-3.2e-2 dvt0w=0 dvt1w=0 dvt2w=0 dvtp0=7.32e-7 dvtp1=0.12dsub=0.058
eta0=0.001 u0=4.19e-2 ua=8.7e-16 ub=3.06e-18 k1=0.33uc=4.6e-13 ute=-1.5 ua1=4.31e-
9 ub1=7.61e-18 uc1=-5.6e-11 k2=-1.87e-2 rdsw=369.4 rdw=184.7 rsw=184.7 prwg=3.22e-
8 prwb=6.8e-11 wr=1 rdswmin=0 rdwmin=0 rswmin=0 prt=0 b0=-1e-20 k3=80 k3b=0
w0=2.5e-6b1=0 keta=-0.047 alpha0=7.4e-2 alpha1=0.005 beta0=30
```

Auto Model Selection

BSIM4 supports dependent model parameters; users can tune these parameters to make a single model card to fit all sizes of devices. But with device geometry shrinks, device needs all kinds of optimization, there are complicated physical effects. It is difficult to use a single

© 2023 Cadence Design Systems, Inc.

model card to fit all devices. An alternative approach is binning option that uses interpolation to calculate model parameters covered by inside that bin. The binning equation is given by

```
P = P0 + Pl / Leff + Pw / Weff + Pp / (Leff * Weff)
```

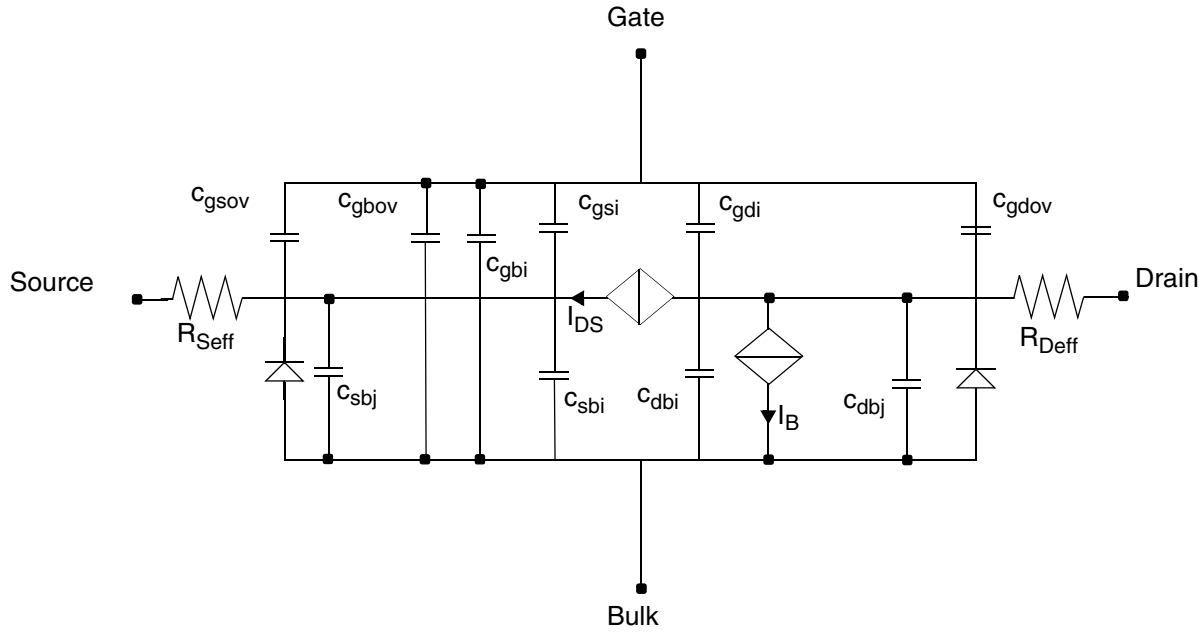
The names of P_l, P_w, and P_p are identical to that of P_0 but with a prefix of l, w, and p, respectively.

Bin selection criteria are as follows:

lmin <= inst_length < lmax and wmin <= inst_width < wmax

Equivalent Circuit

The followings show the equivalent circuits for BSIM4 devices:

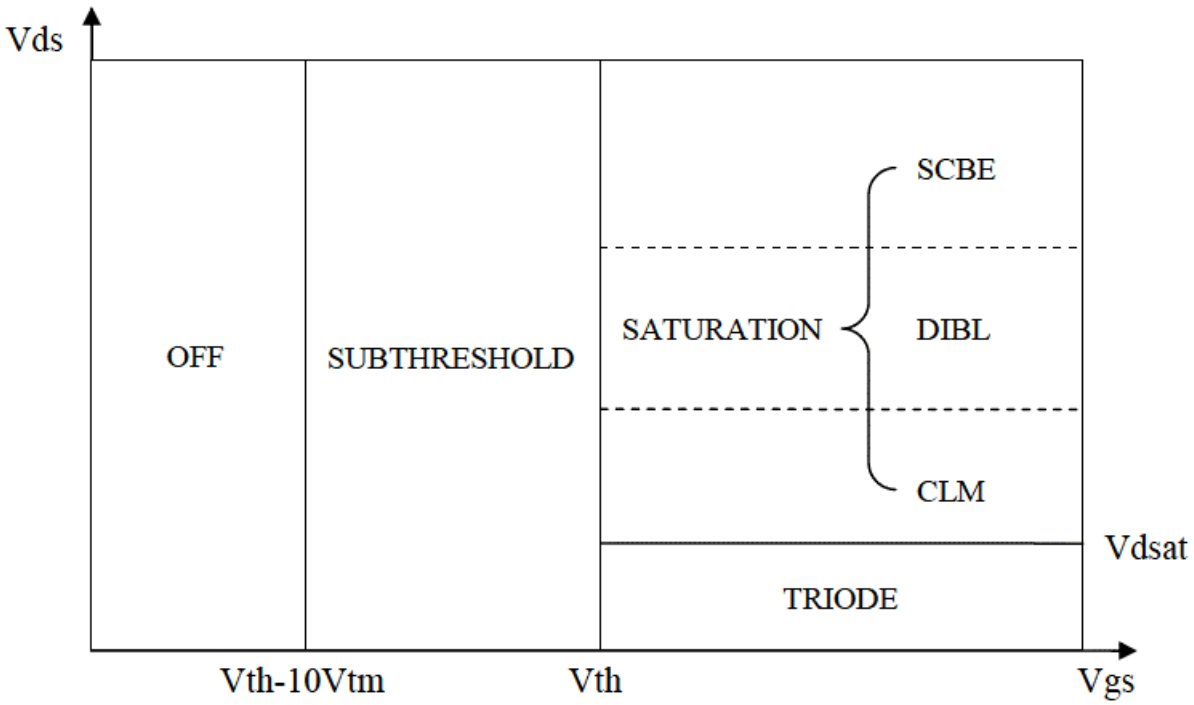


Device Regions

Device region is determined by both Vds and Vgs. The following figure shows the region of N-type BSIM4 device. Saturation region can be splitted to three regions corresponding to different dominant physical mechanism: channel length modulation (CLM) effect, drain-induced barrier lowering (DIBL) effect, and the substrate current induced body effect (SCBE).

© 2023 Cadence Design Systems, Inc.

For P-type device, all the voltage in figure is negative. Vtm is the thermal voltage which is about 0.026V for 300K temperature.



Global Control Options

The following global options affect BSIM4 model.

1. GMIN: GMIN helps solver convergence. It places a conductance in parallel with both the channel and source junction. The default GMIN is 1.0e-12.
2. MINR: Source, drain and gate parasitic resistors inside devices less than minr will be removed. The order of checking inside devices is:
   - Check if resistors are smaller than local minr, if so then remove the parasitic resistors, give warning message.
   - Check global minr, parasitic resistors less than global minr will be removed and warning message will be issued.

Note: Local minr is specified by model parameter minr. The default value is 0.1

3. COMPATIBLE: Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax.

© 2023 Cadence Design Systems, Inc.

Related Topics

BSIM4 Level-14 Model (bsim4)

JUNCAP Model

The JUNCAP model describes the behavior of the diodes that are formed by the source, drain, or well-to-bulk junctions in MOSFET devices. It is integrated into the BSIM4 model to replace the original junction model released by UC Berkeley. The model can be enabled by using the model parameter `juncap`.

- If `juncap=0`, the original junction model in bsim4 is used
- If `juncap=1`, JUNCAP model will be used
- If `juncap=2`, JUNCAP200 model will be used

The equations and parameters of JUNCAP model in bsim4 are the same as JUNCAP/ JUNCAP200 model.

Related Topics

Junction Capacitor (juncap)

JUNCAP2 Model (juncap200) .

TMI 1.0 Model

TMI, TSMC Model Interface, is supported in MMSIM7.1.0.

In order to support customized model equations for advanced technologies, TMI is proposed to provide an alternative approach for this request in addition to adding more macro models.

TMI provides both good flexibility as macro model and good simulation efficiency as build-in standard model at the same time.

TMI 2.0 Model

The TMI 2.0 model feature is released in MMSIM10.1, provides the following new capabilities:

© 2023 Cadence Design Systems, Inc.

Flexible device topology with customized model formulations

With MMSIM 10.1 release, additional component(s) and/or internal node(s) can be added on top of existing standard public domain model topology. This allows the simulator to evaluate (during runtime), the customized model as well as the standard core model formulations, gather/scatter device information and conduct matrix stamping for various type of circuit analysis.

Support for reliability aging modeling and analysis for simulators with and without aging capability

With this feature, the user can add customized aging algorithms for all age integration, extrapolation and mapping. The Safe Operating Areas (SOA) check is also supported.

Related Topics

BSIM4 Level-14 Model (bsim4)

BSIM4 Version 4

BSIM4 Version 5

Model Version Update

Version 4.30

1. Introduced a stress effect model for process induced stress effect;
2. Introduced a temperature model format to predict temperature effects on saturation velocity, mobility, and S/D resistances;
3. Introduced a unified current saturation model that includes all mechanisms of current saturation- velocity saturation, velocity overshoot and source end velocity limit and quasi-ballistic transport;
4. Enhanced holistic thermal noise model;
5. Enhanced forward body bias model;
6. Extended gate direct tunneling model to multiple-layer gate stacks.
7. Fixed minor bugs.

© 2023 Cadence Design Systems, Inc.

Version 4.40

1. Introduced a trap-assisted tunneling and recombination current model, which is applicable to gate-edge side-wall, STI-edge side-wall and bottom junction;
2. Introduced a flatband voltage offset parameter (vfbsdoff) to improve gate overlap tunneling current;
3. Introduced an offset parameter (lintnoi) to length reduction parameter (lint) to improve the accuracy of the flicker noise model;
4. Fixed minor bugs.

Version 4.50

1. Introduced a mobility model which accounts for Coulomb scattering and the channel length dependence of mobility due to heavy halo-doping;
2. Introduced a substrate resistance model (rbodymod = 2), which is scalable with channel length, channel width and number of fingers;
3. Specified gate resistance parameters xgw and ngcon as instance parameters;
4. Improved temperature dependence for model parameters voff and vfbsdoff;
5. Enhanced temperature model (tempmod = 2), where Vth (DITS) and gate tunneling models are functions of nominal temperature and the temperature dependence of flat-band voltage is added;
6. Introduced a new instance parameter delvto to represent threshold voltage variation;
7. Enhanced well-proximity effect model, enable some device parameters to vary with distance from the edge of well-implantation mask due to ion-scattering;
8. Implemented a full BSIM4 Vth model into the Igc equation which enables accurate prediction of the Vbs dependence of Igc.
9. Fixed minor bugs.

Version 4.60

1. Introduced separated model parameters for the GIDL and GISL leakage current modules.
2. Introduced separated parameters for the source and drain side junction diode current due to the trap-assisted tunneling current in space-charge region.

© 2023 Cadence Design Systems, Inc.

3. Introduced separated parameters for the gate tunneling current in the S/D overlap diffusion regions (Igs/Igd).
4. Modified the coulomb scattering term in mobility model to avoid the possibility of non-monoticity in drain current trend with respect to gate voltage.
5. Improved the accuracy for rgatemod = 2 by accounting correctly the contribution from Rgate to overall noise.
6. Set the default value of the parameter vfb to -1.0V.

Version 4.61

1. Introduced new material model (by setting mtrlmod=1) for predictive modeling of non-SiO2 insulator, non-poly Silicon gate and non-silicon channel. Add new parameters including new material model selector (mtrlmod), non-poly silicon gate parameters (phig and epsrgate), non-SiO2 gate dielectric (eot and vddeot), and non-silicon channel parameters (easub, epsrsub, ni0sub, bg0sub, tbgasub, tbgbsub, ados, and bdos).
2. Improved mobility model (mobmod = 0 and 1) through predictive modeling of vertical electric field. The improved mobility model is selected through mtrlmod = 1 for backward compatibility.
3. Improved GIDL/GISL models through an improved definition of flatband voltages at S/D ends. The improved GISL/GIDL model is selected through mtrlmod = 1 for backward compatibility.
4. Modified poly-depletion model to account for new gate and gate-insulator materials.
5. Introduced a new VgsteffCV definition into C-V model (by setting cvchargemod = 1) to improve sub-threshold fitting. Add six new parameters including cvchargemod, minvcv, lminvcv, wminvcv, pminvcv and voffcvl.
6. Fixed an error in the derivative calculation of dVdseffCV_dVb for capmod = 1 and 2.
7. Removed warning messages for the limits of noff and voffcv.

Version 4.62

1. Included the width dependence in trap assisted tunneling (TAT) model. Introduce a new model parameter jtweff and set it to zero to maintain the backward compatibility.
2. Introduced mobility model (mobmod =3) to enhance the modeling of Coulomb scattering in the high-k/metal gate transistors.
3. Fixed minor bugs in:

© 2023 Cadence Design Systems, Inc.

- Output conductance model: vascbe;
- Thermal noise model (tnoimod=0);
- Negative thermal noise (tnoimod=1);
- Source/drain bulk junction capacitance;
- Derivative issue in capacitance model (capmod=0);
- Toxp calculation (mtrlmod=1);
- Source/drain resistance;
- Drain/body breakdown voltage.

Version 4.63

Fixed minor bug in litl calculation.

Version 4.64

1. Fixed bug in thermal noise model when tnoimod=1.
2. Removed duplicate counting of temperature coefficient when mobmod=3.
3. Updated Esat after EsatL calculation.

Version 4.65

1. Set Pseff and Pdeff to zero when they are negative and give a warning message.
2. Turn off source side diode by setting sourceSaturationCurrent=0.0 when Aseff and Pseff are zero. Turn off drain side diode by setting DrainSaturationCurrent=0.0 when Adeff and Pdeff are zero.

Version 4.70

1. Improved GIDL/GISL model from BIMSOI.
   - Add new model with flag gidlmod=1.
   - New binnable parameters `rgidl (lrgidl, wrgidl, prgidl)/rgisl`, `kgidl/kgisl`, and `fgidl/fgisl` have been introduced.

© 2023 Cadence Design Systems, Inc.

- The previous GIDL/GISL model is in gidlmod=0.
- Impacts igidl and igisl.

2. Improved DIBL/Rout model from BIMSOI.
   - Existing DIBL/Rout model in BSIM is proposed to enhance with additional term DVTP5 (with parameters `DVTP2`, `DVTP3`, `DVTP4`, `DVTP5`), to better capture V_{ds} effect in long channel device.
   - Impacts Vth.
3. Improved sub-threshold temperature dependence.
   - Improve formulations to capture temperature dependence of Leakage Current with new parameters `tnfactor`, `teta0`, and `tvoffcv`.
4. Improved thermal noise model (`tnoimod=2`).
   - New noise models have been introduced as `tnoimod=2`. Added new parameters `tnoic` and `rnoic`. Correlated noise is considered.
5. Limiting of diode ideality factor (NJS,NJD).
6. New parameter `mtrlCompatMod` to ensure consistent results of `mtrlMod=0` versus `mtrlMod=1`.
7. BugFix of `Toxm`.
   - Corrected `Toxm` setting in `Initialize()`.
8. BugFix of `igc`.
   - Removed redundant `toxe` term appearing in the Igc formulation

Version 4.80

1. Three new mobility models mobmod=4, mobmod=5, and mobmod=6 have been introduced.
2. The derivative bugs in igcmod=2 have been fixed.
3. Some unused lines have been removed.
4. Parameter check on toxp has been adjusted.
5. The default value of fgidl has been changed to 1.0 for version 4.80.
6. Computational efficiency of rbsbx, rbsby, rbdby, rbpbx, rbpby, rbps0, and rbpd0 has been improved.

© 2023 Cadence Design Systems, Inc.

Version 4.81

- Abnormal Jitter noise temperature dependence with TNOIDMOD =1 is observed.
- Limitation on `TNOIA`, `TNOIB`, `TNOIC` and `RNOIA` being greater than zero is removed and limits have been added in the entire function.
- Warning message has been added for `TNOIMOD=1`.
- When `DLCIG<0` or `DLCIGD<0`, it is clamped to zero and a warning message is generated.
- Model Equations related to Junction Diode IV have been updated.

Related Topics

BSIM4 Level-14 Model (bsim4)

JUNCAP Model

Model Equations

Effective Oxide Thickness, Channel Length and Channel Width

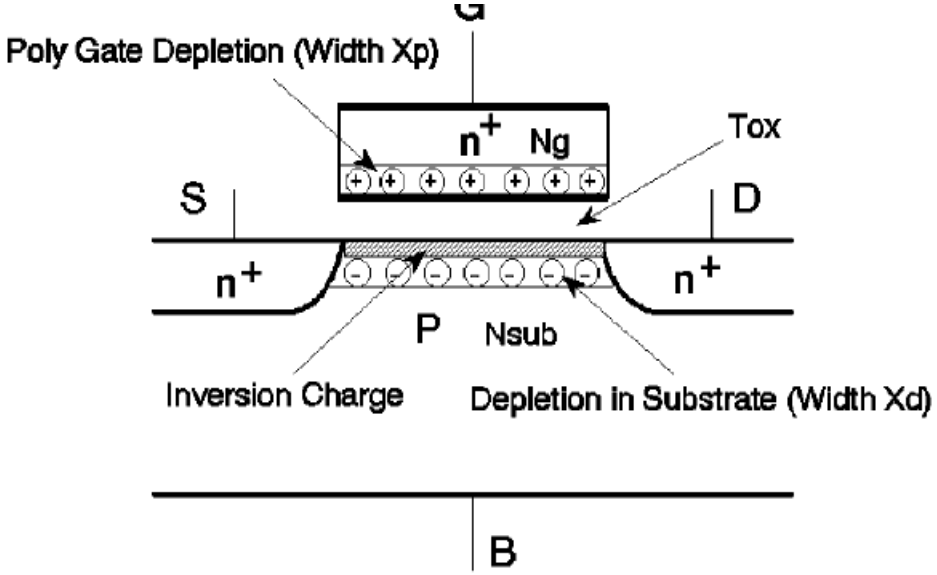
Gate Dielectric Model

The finite chargelayer thickness cannot be ignored when the gate oxide thickness is vigorously scaled down. There are two ways in BSIM4 for modeling this effect in both IV and CV, which can be selected by `mtrlmod`. When `mtrlmod=0` (for SiO2 gate) , the input parameters includes `toxe`, `toxp` and `dtox`. When `mtrlmod=1` (for high-k dielectric gate), the input parameters includes `eot`, `weffeot`, `leffeot`, `tempeot` and `vddeot`. `toxe` is equal to `eot`, and `toxp` could be calculated by the input parameters.

© 2023 Cadence Design Systems, Inc.

Poly-Silicon Gate Depletion

Charge distribution in a MOSFET with the poly gate depletion effect is shown in the following figure. The device is in the strong inversion region.



The effective gate voltage V_{gse} is

For mtrlmod=0

(22-1)

$$V_{gse} = VFB + \Phi_s + \frac{q\varepsilon_{si}NGATE \cdot T^2_{oxe}}{EPSROX^2}\left(\sqrt{1 + \frac{2EPSROX^2(V_{gs} - VFB - \Phi_s)}{q\varepsilon_{si}NGATE \cdot T^2_{oxe}}}\right)$$

For mtrlmod =1(the non-silicon channel or high -k gate insulator

(22-2)

$$V_{gse} = VFB + \Phi_s + \frac{q\varepsilon_{gate}NGATE}{C^2_{oxe}}\left(\sqrt{1 + \frac{2C^2_{oxe}(V_{gs} - VFB - \Phi_s)}{q\varepsilon_{gate}NGATE}} - 1\right)$$

© 2023 Cadence Design Systems, Inc.

Effective Channel Length and Width

(22-3)

$$L_{eff} = L_{drawn} + XL - 2dL$$

(22-4)

$$W_{eff} = \frac{W_{drawn}}{NF} + XW - 2dW$$

(22-5)

$$W_{eff}' = \frac{W_{drawn}}{NF} + XW - 2dW'$$

(22-6)

$$dW = dW' + DWG \cdot V_{gsteff} + DWB(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s})$$

(22-7)

$$dW' = WINT + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WWN}} + \frac{WWL}{L^{WLN}W^{WWN}}$$

(22-8)

$$dL = LINT + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN}W^{LWN}}$$

WINT represents the traditional manner from which "delta *W*" is extracted (from the intercept of straight lines on a $1/R_{ds} \sim W_{drawn}$ plot). The parameters *DWG* and *DWB* are used to account for the contribution of both gate and substrate bias effects. For *dL*, *LINT* represents the traditional manner from which "delta *L*" is extracted from the intercept of lines on a $R_{ds} \sim L_{drawn}$ plot.

The remaining terms in *dW* and *dL* are provided for your convenience. They are meant to allow you to model each parameter as a function of W_{drawn}, L_{drawn}, and their product term. By default, the above geometrical dependencies for *dW* and *dL* are turned off.

© 2023 Cadence Design Systems, Inc.

MOSFET capacitances can be divided into intrinsic and extrinsic components. The intrinsic capacitance is associated with the region between the metallurgical source and drain junction, which is defined by the effective length (L_{active}) and width (W_{active}) when the gate to source/drain regions are under flat-band condition. L_{active} and W_{active} are defined as

(22-9)

$$L_{active} = L_{drawn} + XL - 2dL$$

(22-10)

$$W_{active} = \frac{W_{drawn}}{NF} + XW - 2dW$$

(22-11)

$$dL = DLC + \frac{LLC}{L^{LLN}} + \frac{LWC}{W^{LWN}} + \frac{LWLC}{L^{LLN}W^{LWN}}$$

(22-12)

$$dW = DWC + \frac{WLC}{L^{WLN}} + \frac{WWC}{W^{WWN}} + \frac{WWLC}{L^{WLN}W^{WWN}}$$

The meanings of *DWC* and *DLC* are different from those of *WINT* and *LINT* in the I-V model. Unlike the case of I-V, these dimensions are bias-dependent. The parameter δL_{eff} is equal to the source/drain to gate overlap length plus the difference between drawn and actual POLY CD due to processing (gate patterning, etching, and oxidation) on one side.

The effective channel length L_{eff} for the I-V model does not necessarily carry a physical meaning. It is just a parameter used in the I-V formulation. This L_{eff} is therefore sensitive to the I-V equations and also to the conduction characteristics of the LDD region relative to the channel region. A device with a large L_{eff} and a small parasitic resistance can have a similar current drive as another with a smaller L_{eff} but larger R_{ds}.

The L_{active} parameter extracted from capacitance is a closer representation of the metallurgical junction length (physical length). Due to the graded source/drain junction profile, the source to drain length can have a strong bias dependence. L_{active} is measured at flat-band voltage between gate to source/drain. If *DWC*, *DLC* and the length/width dependence parameters (*LLC*, *LWC*, *LWLC*, *WLC*, *WWC* and *WWLC*) are not specified in technology files, BSIM4 assumes that the DC bias-independent L_{eff} and W_{eff} will be used for the

© 2023 Cadence Design Systems, Inc.

capacitance models, and *DWC*, *DLC*, *LLC*, *LWC*, *LWLC*, *WLC*, *WWC*, and *WWLC* will be set to the values of their DC counterparts.

BSIM4 uses the effective source/drain diffusion width W_{effcj} for modeling parasitics, such as source/drain resistance, gate electrode resistance, and gate induced drain leakage (GIDL) current. W_{effcj} is defined as:

(22-13)

$$W_{effcj} = \frac{W_{drawn}}{NF} - 2 \cdot \left(DWJ + \frac{WLC}{L^{WLN}} + \frac{WWC}{W^{WWN}} + \frac{WWLC}{L^{WLN} W^{WWN}} \right)$$

Threshold Voltage Model

Considering non-uniform doping, short-channel effect, DIBL effect, and narrow-width effect, the complete V_{th} model is:

(22-14)

$$\begin{aligned} V_{th} = {} & VTH0 + (K_{10x} \cdot \sqrt{\Phi_s - V_{bseff}} - K1 \cdot \sqrt{\Phi_s}) \sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox} V_{bseff} \\ & + K_{1ox} \left(\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1 \right) \sqrt{\Phi_s} + (K3 + K3B \cdot V_{bseff}) \frac{TOXE}{W_{eff}' + W0} \Phi_s \\ & - 0.5 \cdot \left[\frac{DVT0W}{\cosh\left(DVT1W \frac{L_{eff} W_{eff}'}{l_{tw}} \right) - 1} + \frac{DVT0}{\cosh\left(DVT1 \frac{L_{eff}}{l_t} \right) - 1} \right] (V_{bi} - \Phi_s) \\ & - \frac{0.5}{\cosh\left(DSUB \frac{L_{eff}}{l_{t0}} \right) - 1} (ETA0 + ETAB \cdot V_{bseff}) \cdot V_{ds} \\ & - nv_t \cdot 1n \left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot \left(1 + e^{-DVTPI \cdot V_{DS}} \right)} \right) - \left(DVTP5 + \frac{DVTP2}{L_{eff}^{DVTP3}} \right) \cdot \tanh(DVTP4.Vds) \end{aligned}$$

© 2023 Cadence Design Systems, Inc.

Channel Charge and Subthreshold Swing Models

A unified expression for channel charge from subthreshold to strong inversion regions is

(22-15)

$$Q_{ch}(y) = C_{oxeff} \cdot V_{gsteff} \cdot \left(1 - \frac{V_F(y)}{V_b}\right)$$

In the above equation, `Vgsteff` (the effective `Vgst(Vgse-Vth)`) used to describe the channel charge densities from subthreshold to strong inversion is modeled by:

$$V_{gsteff} = \frac{n_{vt} \ln\left\{1 + \exp\left[\frac{m^*(V_{gse} - V_{th})}{nv_t}\right]\right\}}{m^* + nC_{oxe} \cdot \sqrt{\frac{2\Phi_s}{qNDEP\varepsilon_{si}}} \exp\left[-\frac{(1-m^*)(V_{gse} - V_{th}) - V'_{off}}{nv_t}\right]}$$

The drain current equation in the subthreshold region can be expressed as:

(22-16)

$$I_{ds} = I_0\left[1 - \exp\left(-\frac{V_{ds}}{v_t}\right)\right] \cdot \exp\left(\frac{V_{gs} - V_{th} - V'_{off}}{nv_t}\right)$$

(22-17)

$$I_0 = \mu\frac{W}{L}\sqrt{\frac{q\varepsilon_{si}NDEP}{2\Phi_s}}v_t^2$$

Gate Direct Tunneling Current Model

In BSIM4, the gate tunneling current components include the tunneling current between gate and substrate (I_{gb}), and the current between gate and channel (I_{gc}), which is partitioned between the source and drain terminals by $I_{gc} = I_{gcs} + I_{gcd}$. The third component happens between gate and source/drain diffusion regions (I_{gs} and I_{gd}). Following figure shows the schematic gate tunneling current flows.

© 2023 Cadence Design Systems, Inc.

I_{gc}, I_{gs}, and I_{gd} are turned on when `igcmod` = 1, 2; I_{gb} is turned on when `igbmod` = 1; no gate tunneling currents are modeled when `igcmod` = 0. V_t (= kT/q) is replaced by V_{tnom}(=kTnom/q) when `tempmod` = 2. The gate tunneling current components are expressed as following:

(22-18)

$$\begin{aligned} I_{gb} &= I_{gbacc} + I_{gbinv} \\ &= W_{eff}L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \\ &\quad \left[\begin{array}{l} \exp(-B \cdot TOXE(AIGBACC - BIGBACC \cdot V_{oxacc}) \cdot (1 + CIGBACC \cdot V_{oxacc})) + \\ \exp(-B \cdot TOXE(AIGBINV - BIGBINV \cdot V_{oxdepinv}) \cdot (1 + CIGBINV \cdot V_{oxdepinv})) \end{array} \right] \end{aligned}$$

(22-19)

$$\begin{aligned} I_{gs} = & W_{eff} \cdot DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gs} \cdot V'_{gs} \\ & \cdot \exp[-B \cdot TOXE \cdot POXEDGE \cdot (AIGS - BIGS \cdot V'_{gs}) \cdot (1 + CIGS \cdot V'_{gs})] \end{aligned}$$

(22-20)

$$\begin{aligned} I_{gd} = & W_{eff} \cdot DLCIGD \cdot A \cdot T_{oxRatioEdge} \cdot V_{gd} \cdot V'_{gd} \\ & \cdot \exp[-B \cdot TOXE \cdot POXEDGE \cdot (AIGD - BIGD \cdot V'_{gd}) \cdot (1 + CIGD \cdot V'_{gd})] \end{aligned}$$

(22-21)

$$I_{gc} = I_{gcs} + I_{gcd}$$

(22-22)

$$Igcs = I_{gc0} \cdot \frac{PIGCD \cdot V_{dseff} + \exp(-PIGCD \cdot V_{dseff}) - 1 + 1.0e-4}{PIGCD^2 \cdot V^2_{dseff} + 2.0e-4}$$

© 2023 Cadence Design Systems, Inc.

(22-23)

$$Igcd = I_{gc0} \cdot \frac{1 + -(PIGCD \cdot V_{dseff} + 1) \cdot \exp(-PIGCD \cdot V_{dseff}) + 1.0e-4}{PIGCD^2 \cdot V^2_{dseff} + 2.0e-4}$$

(22-24)

$$I_{gc0} = \frac{W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gse} \cdot V_{aux}}{\exp[-B \cdot TOXE(AIGC - BIGC \cdot V_{oxdepinv}) \cdot (1 + CIGC \cdot V_{oxdepinv})]}$$

Drain Current Model

Bulk Charge Effect

The bulk charge effect caused by non-zero V_{ds} is modeled as

(22-25)

$$A_{bulk} = \left\{ 1 \pm F\ doping \cdot \left[\frac{A0 L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}} \left(1 - AGSV_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}} \right)^2 \right) + \frac{B0}{W'_{eff} + B1} \right] \right\} \cdot \frac{1}{1 + KETA V_{bseff}}$$

(22-26)

$$F_\text{doping} = \frac{\sqrt{1 + (LPEB)/L_{eff}} K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}} + K_{2ox} - K3B \frac{TOXE}{W'_{eff} + W0} \Phi_s$$

© 2023 Cadence Design Systems, Inc.

Mobility Model

Several mobility models are provided in BSIM4. For `mtrlmod` = 0, `mobmod` = 0 and 1 models are from BSIM3v3.2.2, `mobmod` = 2 is a universal mobility model, which is more accurate and suitable. For `mtrlmod` = 1, a new expression of the vertical field in channel is adopted (introduced by BSIM4.6.1). The mobility model is modified as following:

mobmod=0

(22-27)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UCV_{bseff})E_{eff} + UB \cdot E^2_{eff} + UD\left(\frac{V_{th} \cdot EOT}{V_{gsteff} + 2\sqrt{V^2_{th} + 0.0001}}\right)^2}$$

mobmod=1

(22-28)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UAE_{eff} + UBE^2_{eff})(1 + UCV_{bseff}) + UD\left(\frac{V_{th} \cdot EOT}{V_{gsteff} + 2\sqrt{V^2_{th} + 0.0001}}\right)^2}$$

mobmod=2

(22-29)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UCV_{bseff}) + \left[\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE}\right]^{EU} + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V^2_{th} + 0.0001}}\right)^2}$$

mobmod=3 for high k/metal gate structure (introduced by BSIM4..2):

© 2023 Cadence Design Systems, Inc.

(22-30)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UCV_{bseff}) + \left[\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{6 \cdot TOXE}\right]^{EU} + \frac{UD}{0.5[1 + V_{gsteff}/V_{gsteff} \cdot V_{th}]^{UCS}}}$$

BSIM4.80 introduces three new mobility models, mobmod=4, mobmod=5, and mobmod=6 as modified versions of mobmod=0, mobmod=1, and mobmod=2 respectively.

mobmod=4

(22-31)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UCV_{bseff})\left[\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE}\right] + UB\left(\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE}\right)^2 + UD\left(\frac{C_0 \cdot (VTHO - VFB - \Phi_s) \cdot TOXE}{V_{gseff} + 2\sqrt{C_0^2 \cdot (VTHO - VFB - \Phi_s)^2 + 0.0001}}\right)^2}$$

mobmod=5

(22-32)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + \left[UA\left(\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE}\right) + UB\left(\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE}\right)^2\right](1 + UC \cdot V_{eff}) + UD\left(\frac{C_0 \cdot (VTHO - VFB - \Phi_s) \cdot TOXE}{V_{gseff} + 2\sqrt{C_0^2 \cdot (VTHO - VFB - \Phi_s)^2 + 0.0001}}\right)^2}$$

mobmod=6

© 2023 Cadence Design Systems, Inc.

(22-33)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UC \cdot V_{bseff}) \left[\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE} \right]^{EU} + UD \left(\frac{C_0 \cdot (VTHO - VFB - \Phi_s) \cdot TOXE}{V_{gseff} + 2\sqrt{C_0{}^2 \cdot (VTHO - VFB - \Phi_s)^2 + 0.0001}} \right)^2}$$

Bias-Dependant Source/Drain-Resistance Model

rdsMod=0 (Internal R_{ds} (V))

(22-34)

$$R_{ds}(V) = \left\{ RDSWMIN + RDSW \cdot \left[PRWB \cdot (\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) + \frac{1}{1 + PRWG \cdot V_{gsteff}} \right] \right\} / (1e6 \cdot W_{effcj})^{WR}$$

rdsMod=1 (External R_d(V) and R_s(V)

(22-35)

$$R_d(V) = \left\{ RDWMIN + RDW \cdot \left[-PRWB V_{bd} + \frac{1}{1 + PRWG \cdot (V_{gd} - V_{fbsd})} \right] \right\} / (1e6 \cdot W_{effcj})^{WR} \cdot NF$$

(22-36)

$$R_s(V) = \left\{ RSWMIN + RSW \cdot \left[-PRWB V_{bs} + \frac{1}{1 + PRWG \cdot (V_{gs} - V_{fbsd})} \right] \right\} / (1e6 \cdot W_{effcj})^{WR} \cdot NF$$

Saturation Voltage V_{dsat}

Intrinsic Case

© 2023 Cadence Design Systems, Inc.

(22-37)

$$V_{dsat} = \frac{E_{sat}L(V_{gsteff} + 2v_t)}{A_{bulk}E_{sat}L + V_{gsteff} + 2v_t}$$

© 2023 Cadence Design Systems, Inc.

Extrinsic Case

(22-38)

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

where

(22-39)

$$a = A^2{}_{bulk} W_{eff} VSATC_{oxe} R_{ds} + A_{bulk}\left(\frac{1}{\lambda} - 1\right)$$

(22-40)

$$b = -\begin{bmatrix} (V_{gsteff} + 2v_t)\left(\frac{2}{\lambda} - 1\right) + A_{bulk} E_{sat} L_{eff} \\ +3\mathrm{A}_{bulk}(V_{gsteff} + 2v_t) W_{eff} VSATC_{oxe} R_{ds} \end{bmatrix}$$

(22-41)

$$c = (V_{gsteff} + 2v_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff} VSATC_{oxe} R_{ds}$$

(22-42)

$$\lambda = A1 V_{gsteff} + A2$$

Drain Current

Considering only the channel current, the I-V curve can be divided into two parts: the linear region and the saturation region. In the linear region, carrier velocity is not saturated and the drain current has a strong dependence on the drain voltage. In the saturation region, several physical mechanisms affect the output resistance: channel length modulation (CLM), drain-induced barrier lowering (DIBL), and the substrate current induced body effect (SCBE). These mechanisms all affect the output resistance in the saturation range, but each of them dominates in a specific region. The channel current equation for both linear and saturation regions is:

© 2023 Cadence Design Systems, Inc.

(22-43)

$$I_{ds} = \frac{I_{ds0}NF}{1+\frac{R_{ds}I_{ds0}}{V_{dseff}}}\left[1+\frac{1}{C_{clm}}ln\left(\frac{V_A}{V_{Asat}}\right)\right]\left(1+\frac{V_{ds}-V_{dseff}}{V_{ADIBL}}\right)\left(1+\frac{V_{ds}-V_{dseff}}{V_{ASCBE}}\right)\left(1+\frac{V_{ds}-V_{dseff}}{V_{ADITS}}\right)$$

where NF is the number of device fingers, and Early voltage.

(22-44)

$$V_A = V_{Asat} + V_{ACLM}$$

The Early voltage at $V_{ds} = V_{dsat}$ is

(22-45)

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{ds}vsatC_{oxe}W_{eff}V_{gsteff}}{R_{ds}vsatC_{oxe}W_{eff}A_{bulk} - 1 + \frac{2}{\lambda}}\left[1-\frac{A_{bulk}V_{dsat}}{2(V_{gsteff}+2v_t)}\right]$$

The Early voltage due to CLM effect is

(22-46)

$$V_{ACLIM} = C_{clm}(V_{ds} - V_{dsat})$$

where

(22-47)

The Early voltage due to DIBL effect is

© 2023 Cadence Design Systems, Inc.

$$C_{clm} = \frac{F}{PCLM}\left(1 + PVAG\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)\left(1 + \frac{R_{ds}I_{ds0}}{V_{dseff}}\right)\left(L_{eff} + \frac{V_{sat}}{E_{sat}}\right)\frac{1}{litl}$$

(22-48)

$$V_{ADIBL} = \frac{V_{gsteff} + 2v_t}{\theta_{rout}(1 + PDIBLCB \cdot V_{bseff})}\left(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{sat} + V_{gseff} + 2v_t}\right)\left(1 + PVAG\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)$$

The Early voltage due to SCBE effect is

(22-49)

$$V_{ASCBE} = \frac{L_{eff}}{PSCBE2}\exp\left(\frac{PSCBE1 \cdot litl}{V_{ds} - V_{dsat}}\right)$$

The Early voltage due to Drain-Induced Threshold Shift (DITS) by pocket implant is

(22-50)

$$V_{ADITS} = \frac{F}{PDITS}[1 + (1 + PDITSL \cdot L_{eff})\exp(PDITSD \cdot V_{ds})]$$

Velocity Overshoot and Source End Velocity Limit Model

In the deep-submicron region, the velocity overshoot and source end velocity limit model should be used. The unified current expression with velocity saturation, velocity overshoot and source velocity limit is:

© 2023 Cadence Design Systems, Inc.

(22-51)

$$I_{DS} = \frac{I_{DS,HD}}{[1 + (v_{sHD}/v_{sBT})^{2MM}]^{1/(2MM)}}$$

where the current including the velocity overshoot effect is:

(22-52)

$$I_{DS,HD} = \frac{I_{DS}\left(1 + \frac{V_{dseff}}{L_{eff}E_{sat}}\right)}{1 + \frac{V_{dseff}}{L_{eff}E_{sat}}^{OV}}$$

Body Current Model

I_{sub} Model

When the electrical field near the drain is large (> 0.1MV/cm), some electrons coming from the source (in the case of NMOSFETs) will be energetic (hot) enough to cause impact ionization. This will generate electron-hole pairs when these energetic electrons collide with silicon atoms. The substrate current Isub thus created during impact ionization will increase exponentially with the drain voltage. A well known Isub model is:

(22-53)

$$I_{sub} = \frac{A_i}{B_i} I_{ds}(V_{ds} - V_{dsat}) \exp\left(-\frac{B_i, litl}{V_{ds} - V_{dsat}}\right)$$

© 2023 Cadence Design Systems, Inc.

In addition to the junction diode current and gate-to-body tunneling current, the substrate terminal current consists of the substrate current due to impact ionization (Iii), and gate-induced drain leakage and source leakage currents (I_{GIDL} and I_{GISL}).

I_{ii} Model

(22-54)

$$I_{ii} = \frac{ALPHA0 + ALPHA1 \cdot L_{eff}}{L_{eff}}(V_{ds} - V_{dseff}) \exp\left(\frac{BETA0}{V_{ds} - V_{dseff}}\right) \cdot \frac{I_{ds}}{1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}}$$

I_{GIDL} and I_{GISL} Model

mtrmod=0

(22-55)

$$I_{GIDL} = AGIDL \cdot W_{effCJ} \cdot NF \cdot \frac{V_{ds} - V_{gse} - EGIDL}{3T_{oxe}} \exp\left(-\frac{3T_{oxe} \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL}\right) \frac{V^3_{db}}{CGIDL + V^3_{db}}$$

(22-56)

$$I_{GISL} = AGISL \cdot W_{effCJ} \cdot NF \cdot \frac{-V_{ds} - V_{gde} - EGISL}{3T_{oxe}} \cdot \exp\left(-\frac{3T_{oxe} \cdot BGISL}{-V_{ds} - V_{gde} - EGISL}\right) \cdot \frac{V^3_{sb}}{CGISL + V^3_{sb}}$$

(22-57)

© 2023 Cadence Design Systems, Inc.

mtrmod=1

$$I_{GIDL} = AGIDL \cdot W_{effCJ} \cdot NF \cdot \frac{V_{ds} - V_{gse} - EGIDL + V_{fbsd}}{EOT \cdot \frac{EPSRSUB}{3.9}}$$
$$\cdot \exp(-\frac{EOT \cdot \frac{EPSRSUB}{3.9} \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL + V_{fbsd}}) \cdot \frac{V_{db}^3}{CGIDL + V_{db}^3}$$

(22-58)

$$I_{GISL} = AGISL \cdot W_{effCJ} \cdot NF \cdot \frac{-V_{ds} - V_{gde} - EGISL + V_{fbsd}}{EOT \cdot \frac{EPSRSUB}{3.9}}$$
$$\cdot \exp(-\frac{EOT \cdot \frac{EPSRSUB}{3.9} \cdot BGISL}{-V_{ds} - V_{gde} - EGISL + V_{fbsd}}) \cdot \frac{V_{sb}^3}{CGISL + V_{sb}^3}$$

(22-59)

where

$$V_{fbsd} = PHIG - (EASUB + \frac{Eg0}{2} - BSIM4type \cdot MIN(\frac{Eg0}{2}, v_t \ln(\frac{NSD}{n_i}))$$

Capacitance Model

The following table displays the BSIM4 capacitance model options:

BSIM4 Capacitance Models	Matched capmod in BSIM3v3.2.2
`capMod` = 0 (simple and piecewise model)	Intrinsic `capMod` = 0 + overlap/fringing `capMod`=0
`capMod` = 1 (single equation model)	Intrinsic `capMod` = 2 + overlap/fringing `capMod` = 2
`capMod` = 2 (default; single-equation and charge-thickness model)	Intrinsic `capMod` = 3 + overlap/fringing `capMod` = 2

© 2023 Cadence Design Systems, Inc.

Intrinsic Capacitance Modeling

The relationship of terminal charges (Q_g, Q_b, Q_s, and Q_d) and the channel charge Q_{inv}, accumulation charge Q_{acc} and substrate depletion charge Q_{sub} are:

(22-60)

$$Q_g = -(Q_{sub} + Q_{inv} + Q_{acc})$$

(22-61)

$$Q_b = Q_{acc} + Q_{sub}$$

(22-62)

$$Q_{inv} = Q_s + Q_d$$

All capacitances are derived from the charges to ensure charge conservation. Since there are four terminals, there are a total of 16 components. For each component:

(22-63)

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

where i and j denote the transistor terminals. C_{ij} satisfies

(22-64)

$$\sum_i C_{ij} = \sum_j C_{ij} = 0$$

A new threshold voltage definition is introduced to improve the fitting in subthreshold region. Setting `cvchargemod` = 1 activates the new V_{gsteff}, CV calculation which is similar to the V_{gsteff} formulation in the I-V model. Setting `cvchargemod` = 0 is corresponding to long-channel charge model which assumes a constant mobility with no velocity saturation.

© 2023 Cadence Design Systems, Inc.

Intrinsic capacitance model equations

For capmod=0

Accumulation region

(22-65)

$$Q_g = W_{active} L_{active} C_{oxe} (V_{gs} - V_{bs} - VFBCV)$$

(22-66)

$$Q_{sub} = -Q_g$$

(22-67)

$$Q_{inv} = 0$$

Subthreshold region

(22-68)

$$Q_{sub0} = -W_{active} L_{active} C_{oxe} \frac{K_{1ox}^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{gs} - VFBCV - V_{bs})}{K_{1ox}^2}} \right)$$

(22-69)

$$Q_g = -Q_{sub0}$$

(22-70)

$$Q_{inv} = 0$$

Strong inversion

(22-71)

$$V_{dsat,cv} = \frac{V_{gs} - V_{th}}{A_{bulk}'}$$

© 2023 Cadence Design Systems, Inc.

(22-72)

$$A_{bulk}' = A_{bulk}\left(1+\left(\frac{CLC}{L_{eff}}\right)^{CLE}\right)$$

(22-73)

$$V_{TH} = VFBCV + \Phi_s + K_{1ox}\sqrt{\Phi_s - V_{bseff}}$$

Linear Region

(22-74)

$$Q_g = C_{oxe}W_{active}L_{active}\left[V_{gs} - VFBCV - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' \times V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'V_{ds}}{2}\right)}\right]$$

(22-75)

$$Q_b = C_{oxe}W_{active}L_{active}\left[VFBCV - V_{th} - \Phi_s + \frac{(1-A_{bulk}')V_{ds}}{2} - \frac{(1-A_{bulk}')A_{bulk}'V_{ds}^{\ 2}}{12\left(V_{gs}-V_{th}-\frac{A_{bulk}'V_{ds}}{2}\right)}\right]$$

50/50 Charge Partition

(22-76)

$$Q_{inv} = -C_{oxe}W_{active}L_{active}\left(V_{gs} - V_{th} - \Phi_s - \frac{A_{bulk}'V_{ds}}{2} + \frac{A_{bulk}'^2V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'V_{ds}}{2}\right)}\right)$$

(22-77)

$$Q_s = Q_d = 0.5Q_{inv}$$

© 2023 Cadence Design Systems, Inc.

40/60 Channel-Charge Partition

(22-78)

$$Q_d = -C_{oxe} W_{active} L_{active} \left(\frac{V_{gs} - V_{th}}{2} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}' V_{ds} \left[\frac{(V_{gs} - V_{th})^2}{6} - \frac{A_{bulk}' V_{ds} (V_{gs} - V_{th})}{8} + \frac{(A_{bulk}' V_{ds})^2}{40} \right]}{12 \left(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} \right)^2} \right)$$

(22-79)

$$Q_s = -(Q_g + Q_b + Q_d)$$

0/100 Partitioning

(22-80)

$$Q_d = -C_{oxe} W_{active} L_{active} \left(\frac{V_{gs} - V_{th}}{2} + \frac{A_{bulk}' V_{ds}}{4} - \frac{(A_{bulk}' V_{ds})^2}{24} \right)$$

(22-81)

$$Q_s = -(Q_g + Q_b + Q_d)$$

Saturation Region

(22-82)

$$Q_g = C_{oxe} W_{active} L_{active} \left(V_{gs} - VFBCV - \Phi_s - \frac{V_{dsat}}{3} \right)$$

© 2023 Cadence Design Systems, Inc.

(22-83)

$$Q_b = -C_{oxe} W_{active} L_{active} \left(VFBCV + \Phi_s - V_{th} + \frac{(1 - A_{bulk}') V_{dsat}}{3} \right)$$

50/50 Partitioning

(22-84)

$$Q_s = Q_d = -\frac{1}{3} C_{oxe} W_{active} L_{active} (V_{gs} - V_{th})$$

40/60 Partitioning

(22-85)

$$Q_d = -\frac{4}{15} C_{oxe} W_{active} L_{active} (V_{gs} - V_{th})$$

(22-86)

$$Q_s = -(Q_g + Q_b + Q_d)$$

0/100 Channel-Charge Partition

(22-87)

$$Q_d = 0$$

(22-88)

$$Q_s = -(Q_g + Q_b)$$

For capmod=1

(22-89)

$$Q_g = -(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub})$$

© 2023 Cadence Design Systems, Inc.

(22-90)

$$Q_b = -(Q_{acc} + Q_{sub0} + \delta Q_{sub})$$

(22-91)

$$Q_{inv} = Q_s + Q_d$$

(22-92)

$$Q_{acc} = -W_{active} L_{active} C_{oxe} \cdot (V_{FBeff} - V_{fbzb})$$

(22-93)

$$Q_{sub0} = -W_{active} L_{active} C_{oxe} \cdot \frac{K_{1ox}{}^2}{2} \cdot \left[-1 + \sqrt{1 + \frac{4(V_{gse} - V_{FBeff} - V_{gsteff} - V_{bseff})}{K_{1ox}{}^2}} \right]$$

(22-94)

$$V_{dsat,\,cv} = \frac{V_{gsteffcv}}{A_{bulk}{}'}$$

(22-95)

$$Q_{inv} = -W_{active} L_{active} C_{oxe} \cdot \left[V_{gsteff,\,cv} - \frac{1}{2} A_{bulk}{}' V_{cveff} + \frac{A_{bulk}{}'^2 V_{cveff}^2}{12 \cdot \left(V_{gsteff,\,cv} - \frac{A_{bulk}{}' V_{cveff}}{2} \right)} \right]$$

(22-96)

$$\delta Q_{sub} = W_{active} L_{active} C_{oxe} \cdot \left[\frac{1 - A_{bulk}{}'}{2} V_{cveff} - \frac{(1 - A_{bulk}{}') \cdot A_{bulk}{}' V_{cveff}^2}{12 \cdot \left(V_{gsteff,\,cv} - \frac{A_{bulk}{}' V_{cveff}}{2} \right)} \right]$$

© 2023 Cadence Design Systems, Inc.

50/50 Charge Partition

(22-97)

$$Q_S = Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2}\left[V_{gsteff,cv} - \frac{1}{2}A_{bulk}{}'V_{cveff} + \frac{A_{bulk}{}'^2V_{cveff}^2}{12\cdot\left(V_{gsteff,cv} - \frac{A_{bulk}{}'V_{cveff}}{2}\right)}\right]$$

40/60 Channel-Charge Partition

(22-98)

$$Q_S = -\frac{W_{active}L_{active}C_{oxe}}{2\left(V_{gsteff,cv} - \frac{A_{bulk}{}'V_{cveff}}{2}\right)^2}\left[V_{gsteffcv}{}^3 - \frac{4}{3}V_{gsteffcv}{}^2A_{bulk}{}'V_{cveff} + \frac{2}{3}V_{gsteff,cv}(A_{bulk}{}'V_{cveff})^2 - \frac{2}{15}(A_{bulk}{}'V_{cveff})^3\right]$$

(22-99)

$$Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2\left(V_{gsteff,cv} - \frac{A_{bulk}{}'V_{cveff}}{2}\right)^2}\left[V_{gsteff,cv}{}^3 - \frac{5}{3}V_{gsteff,cv}{}^2A_{bulk}{}'V_{cveff} + V_{gsteff,cv}(A_{bulk}{}'V_{cveff})^2 - \frac{1}{5}(A_{bulk}{}'V_{cveff})^3\right]$$

0/100 Charge Partition

(22-100)

$$Q_S = -\frac{W_{active}L_{active}C_{oxe}}{2}\cdot\left(V_{gsteff,cv} + \frac{1}{2}A_{bulk}{}'V_{cveff} - \frac{A_{bulk}{}'^2V_{cveff}^2}{12\cdot\left(V_{gsteff,cv} - \frac{A_{bulk}{}'V_{cveff}}{2}\right)}\right)$$

© 2023 Cadence Design Systems, Inc.

(22-101)

$$Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2}\cdot\left[V_{gsteff,cv} - \frac{3}{2}A_{bulk}{}'V_{cveff} + \frac{A_{bulk}{}'^2V_{cveff}^2}{4\cdot\left(V_{gsteff,cv} - \frac{A_{bulk}{}'V_{cveff}}{2}\right)}\right]$$

For capmod = 2

(22-102)

$$Q_{acc} = W_{active}L_{active}C_{oxeff}\cdot V_{gbacc}$$

(22-103)

$$V_{gbacc} = \frac{1}{2}\cdot\left[V_0 + \sqrt{V_0{}^2 + 0.08V_{fbzb}}\right]$$

(22-104)

$$V_0 = V_{fbzb} + V_{bseff} - V_{gs} - 0.02$$

(22-105)

$$V_{cveff} = V_{dsat} - \frac{1}{2}\cdot\left(V_1 + \sqrt{V_1{}^2 + 0.08V_{dsat}}\right)$$

(22-106)

$$V_1 = V_{dsat} - V_{ds} - 0.02$$

(22-107)

$$V_{dsat} = \frac{\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff}}{A_{bulk}{}'}$$

When updatelevel=1, a smooth function is applied when calculating ($V_{gsteff,\ cv}$-psi_{delta})$_{eff}$ to improve convergence behavior of the model.

(22-108)

© 2023 Cadence Design Systems, Inc.

(22-109)

$$\varphi_\delta = \Phi_s - 2\Phi_B = v_t \ln\left(\frac{V_{gsteffCV}\cdot(V_{gsteffCV}+2K_{1ox}\sqrt{2\Phi_B})}{MOIN\cdot K_{1ox}{}^2 v_t}\right)$$

(22-110)

$$Q_{sub0} = -W_{active}L_{active}C_{oxeff}\cdot\frac{K_{1ox}{}^2}{2}\left[-1+\sqrt{1+\frac{4(V_{gse}-V_{FBeff}-V_{bseffs}-V_{gsteff,cv})}{K_{1ox}{}^2}}\right]$$

(22-111)

$$Q_{inv} = -W_{active}L_{active}C_{oxeff}\cdot\left[\langle V_{gsteff,cv}-\varphi_\delta\rangle_{eff}-\frac{1}{2}A_{bulk}{}'V_{cveff}+\frac{A_{bulk}{}'^2V_{cveff}^2}{12\cdot\left((V_{gsteff,cv}-\varphi_\delta)_{eff}-\frac{A_{bulk}{}'V_{cveff}}{2}\right)}\right]$$

(22-112)

$$\delta Q_{sub} = -W_{active}L_{active}C_{oxeff}\cdot\left[\frac{1-A_{bulk}{}'}{2}V_{cveff}-\frac{(1-A_{bulk}{}')\cdot A_{bulk}{}'V_{cveff}^2}{12\cdot\left(\langle V_{gsteff,cv}-\varphi_\delta\rangle_{eff}-\frac{A_{bulk}{}'V_{cveff}}{2}\right)}\right]$$

© 2023 Cadence Design Systems, Inc.

50/50 Partitioning

(22-113)

$$Q_S = Q_D = -\frac{W_{active}L_{active}C_{oxeff}}{2}$$

$$\left[\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff} - \frac{1}{2}A_{bulk}{}'V_{cveff} + \frac{A_{bulk}{}'^2 V_{cveff}^2}{12\cdot\left(\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff} - \frac{A_{bulk}{}'V_{cveff}}{2}\right)}\right]$$

40/60 Partitioning

(22-114)

$$Q_S = -\frac{W_{active}L_{active}C_{oxeff}}{2\left(\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff} - \frac{A_{bulk}{}'V_{cveff}}{2}\right)^2}$$

$$\left[\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff}{}^3 - \frac{4}{3}\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff}{}^2 A_{bulk}{}'V_{cveff} + \right.$$

$$\left.\frac{2}{3}\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff}(A_{bulk}{}'V_{cveff})^2 - \frac{2}{15}(A_{bulk}{}'V_{cveff})^3\right]$$

(22-115)

$$Q_D = -\frac{W_{active}L_{active}C_{oxeff}}{2\left(\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff} - \frac{A_{bulk}{}'V_{cveff}}{2}\right)^2}$$

$$\left[\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff}{}^3 - \frac{5}{3}\langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff}{}^2 A_{bulk}{}'V_{cveff} + \langle V_{gsteff,cv} - \varphi_\delta\rangle_{eff}(A_{bulk}{}'V_{cveff})^2\right.$$

$$\left. - \frac{1}{5}(A_{bulk}{}'V_{cveff})^3\right]$$

© 2023 Cadence Design Systems, Inc.

0/100 Partitioning

(22-116)

$$Q_S = -\frac{W_{active}L_{active}C_{oxeff}}{2}\cdot\left[(V_{gsteff,cv}-\varphi_\delta)_{eff}+\frac{1}{2}A_{bulk}{}'V_{cveff}-\frac{A_{bulk}{}'^2V_{cveff}^2}{12\cdot\left((V_{gsteff,cv}-\varphi_\delta)_{eff}-\frac{A_{bulk}{}'V_{cveff}}{2}\right)}\right]$$

(22-117)

$$Q_D = -\frac{W_{active}L_{active}C_{oxeff}}{2}\cdot\left[(V_{gsteff,cv}-\varphi_\delta)_{eff}-\frac{3}{2}A_{bulk}{}'V_{cveff}-\frac{A_{bulk}{}'^2V_{cveff}^2}{4\cdot\left(\langle V_{gsteff,cv}-\varphi_\delta\rangle_{eff}-\frac{A_{bulk}{}'V_{dveff}}{2}\right)}\right]$$

When `updatelevel`=0,

(22-118)

$$\langle V_{gsteff,cv}-\varphi_\delta\rangle_{eff} = V_{gsteff,cv}-\varphi_\delta$$

When `updatelevel`=1, or version=4.5,

(22-119)

$$\langle V_{gsteff,cv}-\varphi_\delta\rangle_{eff} = 0.5\cdot\left[(V_{gsteff,cv}-\varphi_\delta-0.0001)+\sqrt{(V_{gsteff,cv}-\varphi_\delta-0.0001)^2+V_{gsteff,cv}\cdot 0.0004}\right]$$

© 2023 Cadence Design Systems, Inc.

Intrinsic Capacitances (with Body Bias and DIBL)

(22-120)

$$C_{(s,\,d,\,g,\,b),\,g} = \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}}$$

(22-121)

$$C_{(s,\,d,\,g,\,b),\,s} = -\frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{ds}} + \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \left(\frac{\partial V_{th}}{\partial V_{ds}} + \frac{\partial V_{th}}{\partial V_{bs}} \right)$$

(22-122)

$$C_{(s,\,d,\,g,\,b),\,d} = \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{ds}} - \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial (V_{gsteffcv})} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{ds}}$$

(22-123)

$$C_{(s,\,d,\,g,\,b),\,b} = \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{bs}} - \frac{\partial Q_{s,\,d,\,g,\,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{bs}}$$

Overlap Capacitance Models

capmod=0, Bias-independent overlap capacitance model

(22-124)

$$Q_{overlap,s} = W_{active} \cdot CGSO \cdot V_{gs}$$

(22-125)

$$Q_{overlap,d} = W_{active} \cdot CGDO \cdot V_{gd}$$

(22-126)

$$Q_{overlap,b} = L_{active} \cdot CGBO \cdot V_{gb}$$

capmod 1 and 2, Bias dependent overlap capacitance model

© 2023 Cadence Design Systems, Inc.

(22-127)

$$\frac{Q_{overlap,s}}{W_{active}} = CGSO \cdot V_{gs} + CGSL\left(V_{gs} - V_{gs,overlap} - \frac{CKAPPAS}{2}\left(-1+\sqrt{1-\frac{4V_{gs,overlap}}{CKAPPAS}}\right)\right)$$

(22-128)

$$\frac{Q_{overlap,d}}{W_{active}} = CGDO \cdot V_{gd} + CGDL\left(V_{gd} - V_{gd,overlap} - \frac{CKAPPAD}{2}\left(-1+\sqrt{1-\frac{4V_{gd,overlap}}{CKAPPAD}}\right)\right)$$

(22-129)

$$Q_{overlap,g} = -(Q_{overlap.d} + Q_{overlap,s} + CGBO \cdot L_{active} \cdot V_{gb})$$

(22-130)

$$V_{gs.overlap} = \frac{V_{gs} + \delta_1 - \sqrt{(V_{gs} + \delta_1)^2 + 4\delta_1}}{2}$$

(22-131)

$$V_{gd.overlap} = \frac{V_{gd} + \delta_1 - \sqrt{(V_{gd} + \delta_1)^2 + 4\delta_1}}{2}, \delta_1 = 0.02V$$

High Speed/RF Models

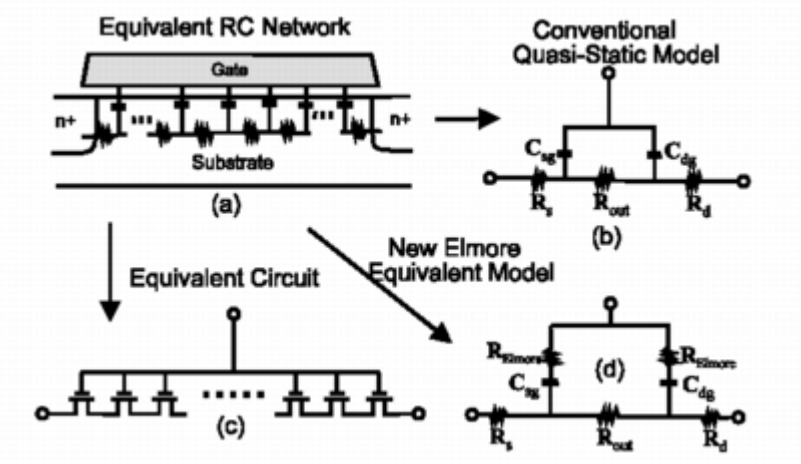
Charge-deficit Nonquasi-static (NQS) Model

BSIM4 uses two separate model selectors to turn on or off the charge-deficit NQS model in transient simulation (using ***trnqsMod***) and AC simulation (using ***acnqsMod***). The AC NQS model does not require the internal NQS charge node that is needed for the transient NQS model. The transient and AC NQS models are developed from the same fundamental physics: the channel/gate charge response to the external signal are relaxation-time (τ)

© 2023 Cadence Design Systems, Inc.

dependent and the transcapacitances and transconductances (such as G_m) for AC analysis can therefore be expressed as functions for $j\omega\tau$.

MOSGFET channel region is analogous to a bias-dependent RC distributed transmission line as shown section "a" of the figure below. In the Quasi-Static (QS) approach, the gate capacitor node is lumped with the external source and drain nodes as shown in section "b" of the figure below. This ignores the finite time for the channel charge to build-up. One way to capture the NQS effect is to represent the channel with *n* transistors in series as shown in section "c" of the figure below, but it comes at the expense of simulation time. The BSIM4 charge-deficit NQS model uses Elmore equivalent circuit to model channel charge build-up as shown in section "d" of the figure below.



The Transient Model

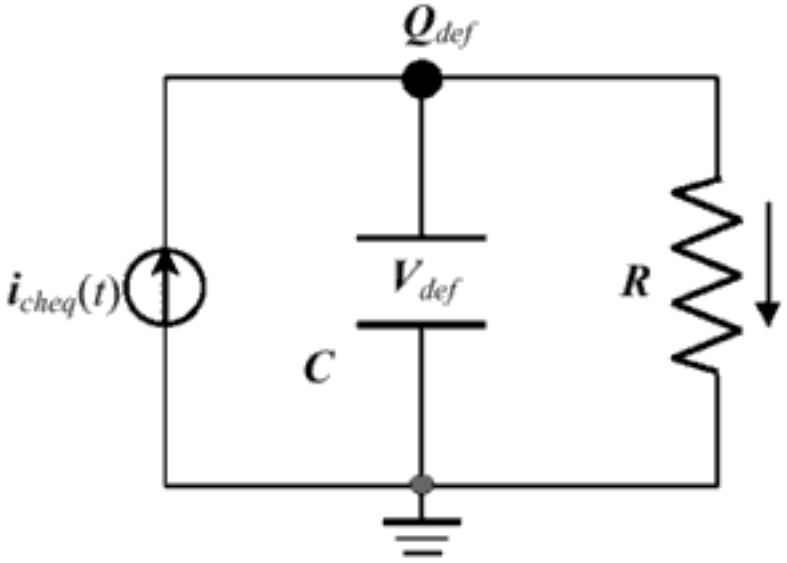
The transient charge-deficit NQS model can be turned on by setting ***trnqsMod*** = 1 and off by setting ***trnqsMod*** = 0.

The figure below shows the RC subcircuit of charge deficit NQS model for transient simulation. An internal node, $Q_{def}(t)$, is created to keep track of the amount of deficit/surplus channel charge necessary to reach equilibrium. The resistance ***R*** is determined from the RC time constant (τ) . The current source $i_{cheq}(t)$ represents the equilibrium channel charging effect. The capacitor ***C*** is the value of C_{fact} (with a typical value of 1 x 10^{-9} Farad) to improve simulation accuracy. Q_{def} now becomes:

© 2023 Cadence Design Systems, Inc.

(22-132)

$$Q_{def}(t) = V_{def} \times C_{fact}$$



Considering both the transport and charging component, the total current related to the terminals D, G, and S can be written as:

(22-133)

$$i_{D,G,S}(t) = I_{D,G,S}(DC) + \frac{\partial Q_{d,g,s}(t)}{\partial t}$$

Based on the relaxation time approach, the terminal charge and corresponding charging current are modeled by

(22-134)

$$Q_{def}(t) = Q_{cheq}(t) - Q_{ch}(t)$$

and

(22-135)

$$\frac{\partial Q_{def}(t)}{\partial t} = \frac{\partial Q_{cheq}(t)}{\partial t} - \frac{Q_{def}(t)}{\tau}$$

© 2023 Cadence Design Systems, Inc.

(22-136)

$$\frac{\partial Q_{d,g,s}(t)}{\partial t} = D, G, S_{xpart}\frac{Q_{def}(t)}{\tau}$$

where D,G,S_{xpart} are charge deficit NQS channel charge partitioning numbers for terminals D, G, and S; $D_{xpart} + S_{xpart} = 1$ and $G_{xpart} = -1$.

The transit time τ is equal to the product of R_{ii} and $W_{eff}L_{eff}C_{oxe}$, where R_{ii} is the intrinsic-input resistance given by

(22-137)

$$\frac{1}{R_{ii}} = XRCRG1 \cdot \left(\frac{I_{ds}}{V_{dseff}} + XRCRG2 \cdot \frac{W_{eff}\mu_{eff}C_{oxeff}k_BT}{qL_{eff}}\right)$$

where C_{oxeff} is the effective gate dielectric capacitance calculated from the DC model.

Note: R_{ii} considers both the drift and diffusion components of the channel conduction, each of which dominates in inversion and subthreshold regions.

The AC Mode

The small-signal AC charge-deficit NQS model can be turned on by setting ***acnqsMod*** = 1 and off by setting ***acnqsMod*** = 0.

For small signals in the frequency domain, $Q_{ch}(t)$ can be transformed into:

(22-138)

$$\Delta Q_{ch}(t) = \frac{\Delta Q_{cheq}(t)}{1 + j\omega\tau}$$

where ω is the angular frequency. It can be shown that the transcapacitances C_{gi}, C_{si}, and C_{di} (i stands for any of the G, D, S, and B terminals of the device) and the channel transconductances G_m, G_{ds}, and G_{mbs} all become complex quantities. For example, now G_m has the form of:

© 2023 Cadence Design Systems, Inc.

(22-139)

$$G_m = \frac{G_{m0}}{1+\omega^2\tau^2} + j\left(-\frac{G_{m0}\cdot\omega\tau}{1+\omega^2\tau^2}\right)$$

and

(22-140)

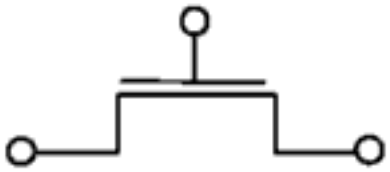
$$C_{dg} = \frac{C_{dg0}}{1+\omega^2\tau^2} + j\left(-\frac{C_{dg0}\cdot\omega\tau}{1+\omega^2\tau^2}\right)$$

The quantities above with sub "0" are known from OP (Operating Point) analysis.

Gate Electrode and Intrinsic-Input Resistance (IIR) Model

BSIM4 provides four options for modeling gate electrode resistance (bias-independent) and intrinsic-input resistance (IIR, bias-dependent). The IIR model considers the relaxation-time effect due to the distributive RC nature of the channel region, and therefore describes the first-order non-quasi-static effect. Thus, the IIR model should not be used together with the charge-deficit NQS model. The model selector ***rgateMod*** is used to choose different options.

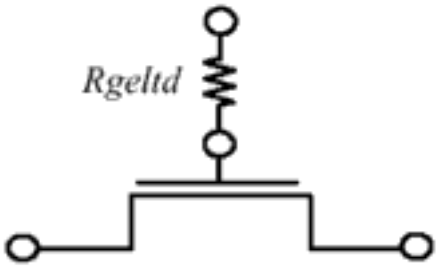
rgateMod = 0 (zero-resistance)



In this case, no gate resistance is generated.

© 2023 Cadence Design Systems, Inc.

rgateMod = 1 (constant-resistance)

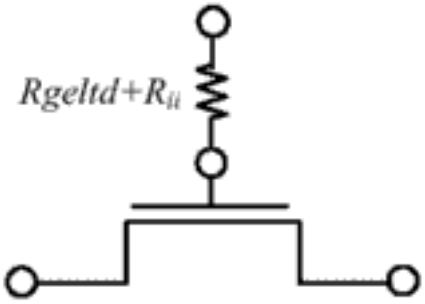


In this case, only the electrode gate resistance (bias-dependent) is generated by adding an internal gate node. Rgeltd is given by

(22-141)

$$Rgeltd = \frac{RSHG \cdot \left(XGW + \frac{W_{effcj}}{3 \cdot NGCON}\right)}{NGCON \cdot (L_{drawn} - XGL) \cdot NF}$$

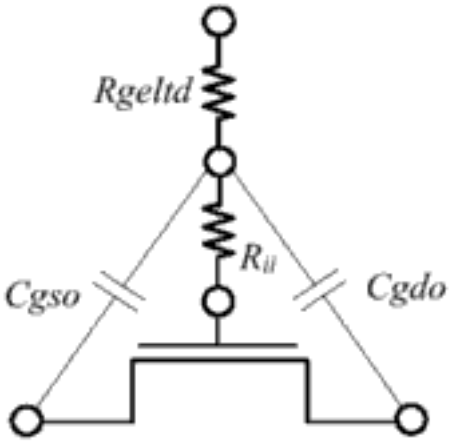
rgateMod = 2 (IIR model with variable resistance)



In this case, the gate resistance is the sum of the electrode gate resistance and the intrinsic-input resistance R_{ii}. An internal gate node will be generated. ***trnqsMod*** = 0 (default) and ***acnqsMod*** = 0 (default) should be selected for this case.

© 2023 Cadence Design Systems, Inc.

rgateMod = 3 (IIR model with two nodes)



In this case, the gate electrode resistance given is in series with the intrinsic-input resistance R_{ii} through two internal gate nodes, so that the overlap capacitance current will not pass through the intrinsic-input resistance. ***trnqsMod*** = 0 (default) and ***acnqsMod*** = 0 (default) should be selected for this case.

Substrate Resistance Network

For CMOS RF circuit simulation, it is essential to consider the high frequency coupling through the substrate. BSIM4 offers a flexible built-in substrate resistance network. This network is constructed so that little simulation efficiency penalty will result.

Model Selector and Topology

The model selector ***rbodyMod*** can be used to turn on or turn off the resistance network.

rbody = 0 (Off)

No substrate resistance network is generated at all.

rbody = 1 (On)

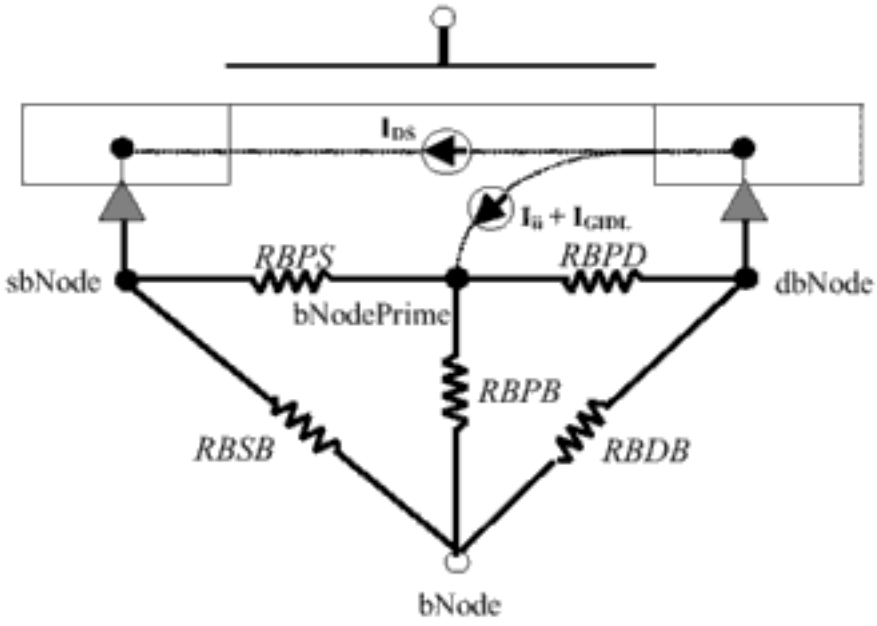
All five resistances in the substrate network as shown schematically below are present simultaneously.

A minimum conductance, *GBMIN*, is introduced in parallel with each resistance to prevent infinite resistance values which would otherwise cause poor convergence. In the following

© 2023 Cadence Design Systems, Inc.

figure, *GBMIN* is merged into each resistance to simplify the representation of the model topology.

Note: The intrinsic model substrate reference point in this case is the internal body node **bNodePrime**, into which the impact ionization current I_{ii} and the GIDL current I_{GIDL} flow.



Noise Models

The following noise sources in MOSFETs are modeled in BSIM4 for noise analysis: flicker noise (also known as 1/f noise), channel thermal noise and induced gate noise and their correlation, thermal noise due to physical resistances such as the source/ drain, gate electrode, and substrate resistances, and shot noise due to the gate dielectric tunneling current.

Flicker Noise Models

BSIM4 provides two flicker noise models: simple model and unified physical model (default model). They can be selected by *fnoimod*. Both modes come from BSIM3v3, but there are many improvements in unified physical model.

fnoiMod = 0 (simple model)

The noise density is:

© 2023 Cadence Design Systems, Inc.

(22-142)

$$S_{id}(f) = \frac{KF \cdot I_{ds}^{AF}}{C_{oxe} L_{eff}^2 f^{EF}}$$

$fnoimod = 1$ (unified model)

The total flicker noise density is:

(22-143)

$$S_{id}(f) = \frac{S_{id,inv}(f) \cdot S_{id,subvt}(f)}{S_{id,inv}(f) + S_{id,subvt}(f)}$$

The noise density in the inversion region is:

(22-144)

$$S_{id,inv}(f) = \frac{k_B T q^2 \mu_{eff} I_{ds}}{C_{ox}(L_{eff} - 2 \cdot LINTNOI)^2 A_{bulk} f^{EF} \cdot 10^{10}}$$
$$\cdot \left(NOIA \cdot \log\left(\frac{N_0 + N^*}{N_l + N^*} \right) + NOIB \cdot (N_0 - N_l) + \frac{NOIC}{2}(N_0^2 - N_l^2) \right)$$
$$+ \frac{k_B T I_{ds}^2 \Delta L_{clm}}{W_{eff} \cdot (L_{eff} - 2 \cdot LINTNOI)^2 f^{EF} \cdot 10^{10}} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + N^*)^2}$$

lintmoi is an offset to the length reduction parameter (*lint*) for flicker noise, which is introduced by BSIM4.4.

© 2023 Cadence Design Systems, Inc.

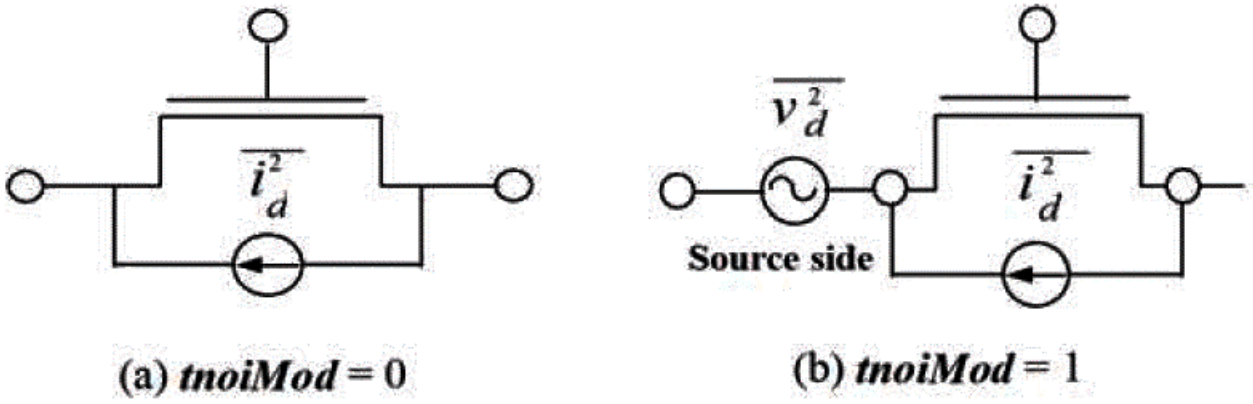
The noise density in the subthreshold region is:

(22-145)

$$S_{id,subVt}(f) = \frac{NOIA \cdot k_B T \cdot I_{ds}^2}{W_{eff} L_{eff} f^{EF} N^{*2} \cdot 10^{10}}$$

Channel Thermal Noise

BSIM4 provides two channel thermal noise models: charge-based model (default model) and the holistic model. They can be selected by *tnoimod*. The schematic for BSIM4 channel thermal noise modeling is shown as following:



(a) ***tnoiMod*** = 0 (b) ***tnoiMod*** = 1

tnoiMod = 0 (charge-based)

Charge-based model is similar to that used in BSIM3v3.2. The noise current is given by:

(22-146)

$$\overline{i_D^2} = \frac{4k_B T \Delta f}{R_{ds}(V) + \frac{L_{eff}^2}{\mu_{eff}|Q_{inv}|}} \cdot NTNOI$$

where

© 2023 Cadence Design Systems, Inc.

(22-147)

$$Q_{inv} = W_{active}L_{active}C_{oxeff} \cdot NF \cdot \left[V_{gsteff} - \frac{A_{bulk}V_{dseff}}{2} + \frac{A_{bulk}^{2}V_{dseff}^{2}}{12 \cdot \left(V_{gsteff} - \frac{A_{bulk}V_{dseff}}{2} \right)} \right]$$

tnoiMod = 1 (holistic)

In this thermal noise model, all the short-channel effects and velocity saturation effect incorporated in the IV model are automatically included, hence the name “holistic thermal noise model”. In addition, the amplification of the channel thermal noise through G_m and G_{mbs} as well as the induced-gate noise with partial correlation to the channel thermal noise are all captured in the new “noise partition” model.

The noise voltage source partitioned to the source side is given by

(22-148)

$$\overline{v_d^{\,2}} = 4k_BT \cdot \theta_{tnoi}^{\,2} \cdot \frac{V_{dseff}\Delta f}{I_{ds}}$$

The noise current source put in the channel region with gate and body amplification is given by:

(22-149)

$$\overline{i_d^{\,2}} = 4k_BT\frac{V_{dseff}\Delta f}{I_{ds}}[G_{ds} + \beta_{tnoi} \cdot (G_m + G_{mbs})]^2 - \overline{v_d^{\,2}} \cdot (G_m + G_{ds} + G_{mbs})^2 \qquad if Vds \geq Vdsat$$

where

© 2023 Cadence Design Systems, Inc.

(22-150)

$$\theta_{tnoi} = RNOIB \cdot \left[1 + TNOIB \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right]$$

$$\beta_{tnoi} = RNOIA \cdot \left[1 + TNOIA \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right]$$

Asymmetric MOS Junction Diode Models

Junction Diode IV Model

In BSIM4, there are three junction diode IV models. When the IV model selector ***dioMod*** is set to 0 ("resistance free"), the diode IV is modeled as resistance-free with or without breakdown depending on the parameter values of *XJBVS* or *XJBVD*. When ***dioMod*** is set to 1 ("breakdown-free"), the diode is modeled in the same way as in BSIM3v3 with current-limiting feature in the forward-bias region through the limiting current parameters *IJTHSFWD* or *IJTHDFWD*; diode breakdown is not modeled for ***dioMod*** = 1 and *XJBVS*, *XJBVD*, *BVS*, and *BVD* parameters all have no effect. When ***dioMod*** is set to 2 ("resistance-and-breakdown"), BSIM4 models the diode breakdown with current limiting in both forward and reverse operations. In general, setting ***dioMod*** to 1 produces fast convergence.

Note: For designs where source/body or drain/body junction is forward-biased, `diomod=0` is not recommended. Use `diomod=2` instead.

Source/Body Junction Diode

dioMod - 0 (resistance-free)

(22-151)

$$I_{bs} = I_{sbs} \left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM} \right) - 1 \right] \cdot f_{breakdown} + V_{bs} \cdot G_{min}$$

where I_{sbs} is the total saturation current consisting of the components through the gate-edge (J_{sswgs}) and isolation-edge sidewalls (J_{ssws}) and the bottom junction (J_{ss}).

(22-152)

© 2023 Cadence Design Systems, Inc.

$$I_{sbs} = A_{seff}J_{ss}(T) + R_{seff}J_{ssws}(T) + W_{effcj} \cdot NF \cdot J_{sswgs}(T)$$

where

(22-153)

$$f_{breakdown} = 1 + XJBVS \cdot \exp\left(-\frac{q \cdot (BVS + V_{bs})}{NJS \cdot k_B TNOM}\right)$$

In the above equation, if *XJBVS* = 0, no breakdown will be modeled. If *XJBVS* < 0.0, it is reset to 1.0.

dioMod = 1 (breakdown-free)

The exponential IV term is linearized at the limiting current *IJTHSFWD* in the forward-bias model only.

(22-154)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM}\right) - 1\right] + V_{bs} \cdot G_{min}$$

dioMod = 2 (resistance-and-breakdown)

Diode breakdown is always modeled. The exponential term is linearized at both the limiting current *IJTHSFWD* in the forward-bias mode and the limiting current *IJTHSREV* in the reverse-bias mode.

(22-155)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bs} \cdot G_{min}$$

for ***dioMod*** = 2, if *XJBVS* <= 0.0, it is reset to 1.0.

Drain/Body Junction Diode

The drain-side diode has the same system of equations as those for the source-side diode, but with a separate set of model parameters.

dioMod = 0 (resistance-free)

© 2023 Cadence Design Systems, Inc.

(22-156)

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bd} \cdot G_{min}$$

where I_{sbd} is the total saturation current consisting of the components through the gate-edge (J_{sswgd}) and isolation-edge sidewalls (J_{sswd}) and the bottom junction (J_{sd}),

(22-157)

$$I_{sbd} = A_{deff}J_{sd}(T) + P_{deff}J_{sswd}(T) + W_{effcj} \cdot NF \cdot J_{sswgd}(T)$$

where

(22-158)

$$f_{breakdown} = 1 + XJBVD \cdot \exp\left(-\frac{q \cdot (BVD + V_{bd})}{NJD \cdot k_B TNOM}\right)$$

In the above equation, when *XJBVD* = 0, no breakdown is modeled. If *XJBVD* < 0.0, it is reset to 1.0.

dioMod = 1 (breakdown-free)

No breakdown is modeled. The exponential IV term is linearized at the limiting current *IJTHSFWD* in the forward-bias model only.

(22-159)

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM}\right) - 1\right] + V_{bd} \cdot G_{min}$$

dioMod = 2 (resistance-and-breakdown)

Diode breakdown is always modeled. The exponential term is linearized at both the limiting current *IJTHSFWD* in the forward-bias mode and the limiting current *IJTHSFWD* in the reverse-bias mode.

(22-160)

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bd} \cdot G_{min}$$

© 2023 Cadence Design Systems, Inc.

For ***dioMod*** = 2, if *XJBVD* <= 0.0, it is reset to 1.0.

© 2023 Cadence Design Systems, Inc.

Total Junction Source/Drain Diode Including Tunneling

Total diode current including the carrier recombination and trap-assisted tunneling current in the space-charge region is modeled by:

(22-161)

$$
\begin{aligned}
I_{bs_\text{total}} &= I_{bs} \\
&- W_{effcj} \cdot NF \cdot J_{tsswgs}(T) \cdot \left[\exp\left(\frac{-V_{bs}}{NJTSSWG(T) \cdot Vtm0} \cdot \frac{VTSSWGS}{VTSSWGS - V_{bs}} \right) - 1 \right] \\
&- P_{s,\,deff} J_{tssws}(T) \left[\exp\left(\frac{-V_{bs}}{NJTSSW(T) \cdot Vtm0} \cdot \frac{VTSSWS}{VTSSWS - V_{bs}} \right) - 1 \right] \\
&- A_{s,\,deff} J_{tss}(T) \left[\exp\left(\frac{-V_{bs}}{NJTS(T) \cdot Vtm0} \cdot \frac{VTSS}{VTSS - V_{bs}} \right) - 1 \right] + g_{min} \cdot V_{bs}
\end{aligned}
$$

(22-162)

$$
\begin{aligned}
I_{bd_\text{total}} &= I_{bd} \\
&- W_{effcj} \cdot NF \cdot J_{tsswgd}(T) \cdot \left[\exp\left(\frac{-V_{bd}}{NJTSSWGD(T) \cdot Vtm0} \cdot \frac{VTSSWGD}{VTSSWGD - V_{bd}} \right) - 1 \right] \\
&- P_{s,\,deff} J_{tsswd}(T) \left[\exp\left(\frac{-V_{bd}}{NJTSSWD(T) \cdot Vtm0} \cdot \frac{VTSSWD}{VTSSWD - V_{bd}} \right) - 1 \right] \\
&- A_{d,\,deff} J_{tsd}(T) \left[\exp\left(\frac{-V_{bd}}{NJTSD(T) \cdot Vtm0} \cdot \frac{VTSD}{VTSD - V_{bd}} \right) - 1 \right] + g_{min} \cdot V_{bd}
\end{aligned}
$$

© 2023 Cadence Design Systems, Inc.

Junction Diode CV Model

Source and drain junction capacitances consist of three components: the bottom junction capacitance, sidewall junction capacitance along the isolation edge, and sidewall junction capacitance along the gate edge. An analogous set of equations are used for both sides but each side has a separate set of model parameters.

Source/Body Junction Diode

(22-163)

$$C_{bs} = A_{seff}C_{jbs} + P_{seff}C_{jbsws} + W_{effcj} \cdot NF \cdot C_{jbswgs}$$

where C_{jbs} is the unit-area bottom S/B junction capacitance, C_{jbsws} is the unit-length S/B junction sidewall capacitance along the isolation edge, and C_{jbswgs} is the unit-length S/B junction sidewall capacitance along the gate edge.

C_{jbs}

if V_{bs}< 0

(22-164)

$$C_{jbs} = CJS(T) \cdot \left(1 - \frac{V_{bs}}{PBS(T)}\right)^{-MJS}$$

otherwise

(22-165)

$$C_{jbs} = CJS(T) \cdot \left(1 + MJS \cdot \frac{V_{bs}}{PBS(T)}\right)$$

© 2023 Cadence Design Systems, Inc.

C_{jbsws}

if V_{bs}< 0

(22-166)

$$C_{jbsws} = CJSWS(T) \cdot \left(1 - \frac{V_{bs}}{PBSWS(T)}\right)^{-MJSWS}$$

otherwise

(22-167)

$$C_{jbsws} = CJSWS(T) \cdot \left(1 + MJSWS \cdot \frac{V_{bs}}{PBSWS(T)}\right)$$

C_{jbsws}

if V_{bs}< 0

(22-168)

$$C_{jbswgs} = CJSWGS(T) \cdot \left(1 - \frac{V_{bs}}{PBSWGS(T)}\right)^{-MJSWGS}$$

otherwise

(22-169)

$$C_{jbswgs} = CJSWGS(T) \cdot \left(1 + MJSWGS \cdot \frac{V_{bs}}{PBSWGS(T)}\right)$$

Drain/Body Junction Diode

(22-170)

$$C_{bd} = A_{deff}C_{jbd} + P_{deff}C_{jbswd} + W_{effcj} \cdot NF \cdot C_{jbswgd}$$

© 2023 Cadence Design Systems, Inc.

where C_{jbd} is the unit-area bottom D/B junction capacitance, C_{jbswd} is the unit-length D/B junction sidewall capacitance along the isolation edge, and C_{jbswgd} is the unit-length D/B junction sidewall capacitance along the gate edge.

C_{jbd}

if $V_{bd} < 0$

(22-171)

$$C_{jbd} = CJD(T) \cdot \left(1 - \frac{V_{bd}}{PBD(T)}\right)^{-MJD}$$

otherwise

(22-172)

$$C_{jbd} = CJD(T) \cdot \left(1 + MJD \cdot \frac{V_{bd}}{PBD(T)}\right)$$

C_{jbdsw}

f $V_{bd} < 0$

(22-173)

$$C_{jbswd} = CJSWD(T) \cdot \left(1 - \frac{V_{bd}}{PBSWD(T)}\right)^{-MJSWD}$$

otherwise

(22-174)

$$C_{jbswd} = CJSWD(T) \cdot \left(1 + MJSWD \cdot \frac{V_{bd}}{PBSWD(T)}\right)$$

© 2023 Cadence Design Systems, Inc.

C_{jbdswg}

f $V_{bd} < 0$

(22-175)

$$C_{jbswgd} = CJSWGD(T) \cdot \left(1 - \frac{V_{bd}}{PBSWGD(T)}\right)^{-MJSWD}$$

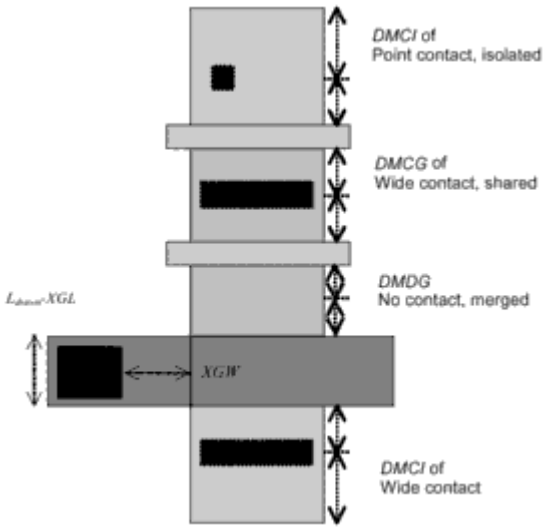
otherwise

(22-176)

$$C_{jbswgd} = CJSWGD(T) \cdot \left(1 + MJSWGD \cdot \frac{V_{bd}}{PBSWGD(T)}\right)$$

Layout Dependent Parasitics Models

The following figure shows the geometry definition for various source/drain connections and source/drain/gate contacts. The layout parameters shown in this figure will be used to calculate resistances and source/drain perimeters and areas.



© 2023 Cadence Design Systems, Inc.

Effective Junction Perimeter and Area

The source-side case is illustrated below. The same approach is used for the drain side. The effective junction perimeter is calculated by:

If (*PS* is given)

if (***perMod*** = 0)

$P_{seff} = PS$

else

(22-177)

$$P_{seff} = PS - W_{effcj} \cdot NF$$

Else

P_{seff} computed from *NF*, *DWJ*, ***geoMod***, *DMCG*, *DMCI*, *DMDG*, *DMCGT*, and *MIN*.

The effective junction area is calculated by:

If (*AS* is given)

$A_{seff} = AS$

Else

A_{seff} computed from *NF*, *DWJ*, ***geoMod***, *DMCG*, *DMCI*, *DMDG*, *DMCGT*, and *MIN*.

In the above, P_{seff} and A_{seff} will be used to calculate junction diode IV and CV. P_{seff} does not include the gate-edge perimeter.

geoMod	**End source**	**End drain**	**Note**
0	isolated	isolated	*NF=Odd*
1	isolated	shared	*NF=Odd, Even*
2	shared	isolated	*NF=Odd, Even*
3	shared	shared	*NF=Odd, Even*
4	isolated	merged	*NF=Odd*
5	shared	merged	*NF=Odd, Even*

© 2023 Cadence Design Systems, Inc.

geoMod	**End source**	**End drain**	**Note**
6	merged	isolated	*NF=Odd*
7	merged	shared	*NF=Odd, Even*
8	merged	merged	*NF=Odd*
9	sha/iso	shared	*NF=Even*
10	shared	sha/iso	*NF=Even*

Temperature Effects Models

Accurate modeling of the temperature effects on MOSFET characteristics is important to predict circuit behavior over a range of operating temperatures (*T*). The operating temperature might be different from the nominal temperature (*TNOM*) at which the BSIM4 model parameters are extracted.

Temperature Dependence of Threshold Voltage

The temperature dependence of V_{th} is modeled by:

(22-178)

$$V_{th}(T) = V_{th}(TNOM) + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff}\right) \cdot \left(\frac{T}{TNOM} - 1\right)$$

(22-179)

$$V_{fb}(T) = V_{fb}(TNOM) - KT1 \cdot \left(\frac{T}{TNOM} - 1\right)$$

(22-180)

$$VOFF(T) = VOFF(TNOM) \cdot [1 + TVOFF \cdot (T - TNOM)]$$

(22-181)

$$VFBSDOFF(T) = VFBSDOFF(TNOM) \cdot [1 + TVFBSDOFF \cdot (T - TNOM)]$$

© 2023 Cadence Design Systems, Inc.

Temperature Dependence of Mobility

(22-182)

$$U0(T) = U0(TNOM) \cdot (T/TNOM)^{UTE}$$

(22-183)

$$UA(T) = UA(TNOM) + UA1 \cdot (T/TNOM - 1)$$

(22-184)

$$UB(T) = UB(TNOM) + UB1 \cdot (T/TNOM - 1)$$

(22-185)

$$UC(T) = UC(TNOM) + UC1 \cdot (T/TNOM - 1)$$

Temperature Dependence of Saturation Velocity

(22-186)

$$v_{sat(T)} = VSAT(TNOM) - AT \cdot (T/TNOM - 1)$$

Temperature Dependence of LDD Resistance

rdsMod = 0 (internal source/drain LDD resistance)

(22-187)

$$RDSW(T) = RDSW(TNOM) + PRT \cdot \left(\frac{T}{TNOM} - 1\right)$$

(22-188)

$$RDSWMIN(T) = RDSWMIN(TNOM) + PRT \cdot \left(\frac{T}{TNOM} - 1\right)$$

© 2023 Cadence Design Systems, Inc.

rdsMod = 1 (external source/drain LDD resistance)

(22-189)

$$RDW(T) = RDW(TNOM) + PRT \cdot \left(\frac{T}{TNOM} - 1\right)$$

(22-190)

$$RDWMIN(T) = RDWMIN(TNOM) + PRT \cdot \left(\frac{T}{TNOM} - 1\right)$$

(22-191)

$$RSW(T) = RSW(TNOM) + PRT \cdot \left(\frac{T}{TNOM} - 1\right)$$

(22-192)

$$RSWMIN(T) = RSWMIN(TNOM) + PRT \cdot \left(\frac{T}{TNOM} - 1\right)$$

Temperature Dependence of Junction Diode IV

Source-side Diode

(22-193)

$$I_{sbs} = A_{seff}J_{ss}(T) + P_{seff}J_{sswgs}(T) + W_{effcj} \cdot NF \cdot J_{sswgs}(T)$$

where

(22-194)

$$J_{ss}(T) = JSS(TNOM) \cdot \exp\left(\frac{\frac{E_g(TNOM)}{v_t(TNOM)} - \frac{E_g(T)}{v_t(T)} + XTIS \cdot \ln\left(1 - \frac{T}{TNOM}\right)}{NJS}\right)$$

© 2023 Cadence Design Systems, Inc.

(22-195)

$$J_{ssws}(T) = JSSWS(TNOM) \cdot \exp\left(\frac{\frac{E_g(TNOM)}{v_t(TNOM)} - \frac{E_g(T)}{v_t(T)} + XTIS \cdot \ln\left(1 - \frac{T}{TNOM}\right)}{NJS}\right)$$

(22-196)

$$J_{sswgs}(T) = JSSWGS(TNOM) \cdot \exp\left(\frac{\frac{E_g(Tnom)}{V_t(Tnom)} - \frac{E_g(T)}{V_t(T)} + XTIS \cdot \ln\left(1 - \frac{T}{Tnom}\right)}{NJS}\right)$$

where

(22-197)

$$E_g(TNOM) = 1.16 - \frac{7.02 \times 10^{-4} TNOM^2}{TNOM + 1108}$$

(22-198)

$$E_g(T) = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

(22-199)

$$n_i = 1.45e10 \cdot \frac{TNOM}{300.15} \cdot \sqrt{\frac{TNOM}{300.15}} \cdot \exp\left[21.5565981 - \frac{qE_g(TNOM)}{2 \cdot k_B T}\right]$$

Drain-side Diode

(22-200)

$$I_{sbd} = A_{deff} J_{sd}(T) + P_{deff} J_{sswd}(T) + W_{effcj} \cdot NF \cdot J_{sswd}(T)$$

© 2023 Cadence Design Systems, Inc.

(22-201)

$$J_{sd}(T) = JSD(TNOM) \cdot \exp\left(\frac{\frac{E_g(TNOM)}{v_t(TNOM)} - \frac{E_g(T)}{v_t(T)} + XTID \cdot \ln\left(1 - \frac{T}{TNOM}\right)}{NJD}\right)$$

(22-202)

$$J_{sswd}(T) = JSSWD(TNOM) \cdot \exp\left(\frac{\frac{E_g(TNOM)}{v_t(TNOM)} - \frac{E_g(T)}{v_t(T)} + XTID \cdot \ln\left(1 - \frac{T}{TNOM}\right)}{NJD}\right)$$

Trap-assisted Tunneling and Recombination Current

(22-203)

$$J_{tsswgs,\,d}(T) = J_{tsswgs,\,d}(TNOM) \cdot \left(\sqrt{\frac{JTWEFF}{W_{effcj}}}\right) \exp\left[\frac{-Eg(TNOM)}{Vt} \cdot X_{tsswgs,\,d} \cdot \left(1 - \frac{T}{TNOM}\right)\right]$$

© 2023 Cadence Design Systems, Inc.

(22-204)

$$J_{tssws,\,d}(T) = J_{tssws,\,d}(TNOM) \cdot \exp\left[\frac{-Eg(TNOM)}{Vt} \cdot X_{tssws,\,d} \cdot \left(1 - \frac{T}{TNOM}\right)\right]$$

(22-205)

$$J_{tss,\,d}(T) = J_{tss,\,d}(TNOM) \cdot \exp\left[\frac{-Eg(TNOM)}{Vt} \cdot X_{tss,\,d} \cdot \left(1 - \frac{T}{TNOM}\right)\right]$$

(22-206)

$$NJTSSWG(T) = NJTSSWG(TNOM) \cdot \left[1 + TNJTSSWG\left(\frac{T}{TNOM} - 1\right)\right]$$

(22-207)

$$NJTSSW(T) = NJTSSW(TNOM) \cdot \left[1 + TNJTSSW\left(\frac{T}{TNOM} - 1\right)\right]$$

(22-208)

$$NJTS(T) = NJTS(TNOM) \cdot \left[1 + TNTJS\left(\frac{T}{TNOM} - 1\right)\right]$$

© 2023 Cadence Design Systems, Inc.

Temperature Dependence of Junction Diode CV

Source-Side Diode

The temperature dependences of zero-bias unit-length/area junction capacitances on the source side are modeled by

(22-209)

$$CJS(T) = CJS(TNOM) \cdot [1 + TCJ \cdot (T - TNOM)]$$

(22-210)

$$CJSWS(T) = CJSWS(TNOM) + TCJSW \cdot (T - TNOM)$$

(22-211)

$$CJSWGS(T) = CJSWGS(TNOM) \cdot [1 + TCJSWG \cdot (T - TNOM)]$$

The temperature dependences of the built-in potentials on the source side are modeled by

(22-212)

$$PBS(T) = PBS(TNOM) - TPB \cdot (T - TNOM)$$

(22-213)

$$PBSWS(T) = PBSWS(TNOM) - TPBSW \cdot (T - TNOM)$$

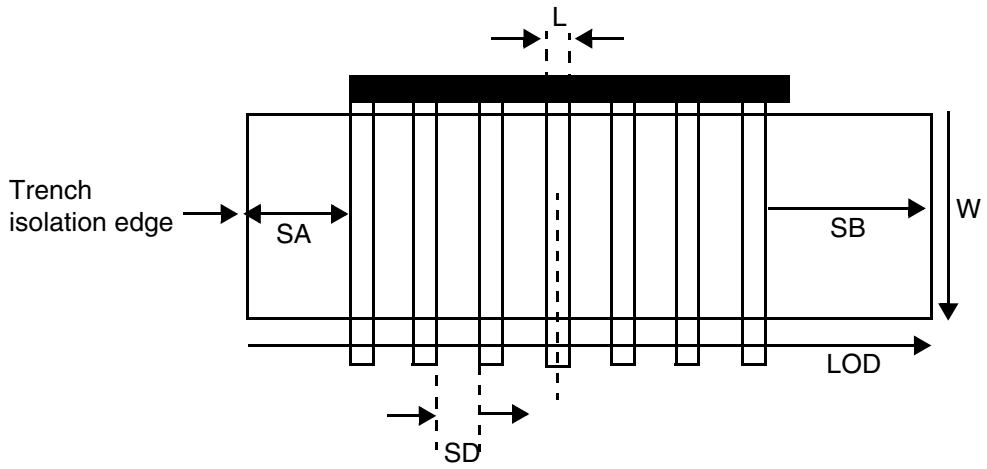
(22-214)

$$PBSWGS(T) = PBSWGS(TNOM) - TPBSWG \cdot (T - TNOM)$$

© 2023 Cadence Design Systems, Inc.

Stress Effects Models

BSIM4 considers the influence of stress on mobility, velocity saturation, threshold voltage, body effect, and DIBL effect. The following diagram displays the LOD instance geometry parameters SA and SB.



(22-215)

$$\mu_{eff} = \frac{1+\rho_{\mu eff}(SA, SB)}{1+\rho_{\mu eff}(SA_{ref}, SB_{ref})}\mu_{effo}$$

(22-216)

$$v_{sattemp} = \frac{1+KVSAT\cdot\rho_{\mu eff}(SA, SB)}{1+KVSAT\cdot\rho_{\mu eff}(SA_{ref}, SB_{ref})}v_{sattempo}$$

(22-217)

$$VTH0 = VTH0_{original} + \frac{KVTH0}{Kstress_vth0}\cdot(Inv_sa + Inv_sb - Inv_sa_{ref} - Inv_sb_{ref})$$

(22-218)

$$K2 = K2_{original} + \frac{STK2}{Kstress_vth0^{LODK2}}\cdot(Inv_sa + Inv_sb - Inv_sa_{ref} - Inv_sb_{ref})$$

© 2023 Cadence Design Systems, Inc.

(22-219)

$$ETA0 = ETA0_{original} + \frac{STETA0}{Kstress_vth0^{LODETA0}} \cdot (Inv_sa + Inv_sb - Inv_sa_{ref} - Inv_sb_{ref})$$

where

(22-220)

$$\rho_{\mu eff} = \frac{KU_0}{Kstress_\mu 0} \cdot (Inv_sa + Inv_sb)$$

(22-221)

$$K_{stress_\mu 0} = \left(1 + \frac{LKU0}{(L_{drawn} + XL)^{LLODKU0}} + \frac{WKU0}{(W_{drawn} + XW + WLOD)^{WLODKU0}} + \frac{PKU0}{(L_{drawn} + XL)^{LLODKU0} \cdot (W_{drawn} + XW + WLOD)^{WLODKU0}} \right) \cdot \left(1 + TKU0 \cdot \left(\frac{Temperature}{TNOM} - 1 \right) \right)$$

(22-222)

$$K_{stress_vth0} = \left(1 + \frac{LKVTH0}{(L_{drawn} + XL)^{LLODKVTH}} + \frac{WKVTH0}{(W_{drawn} + XW + WLOD)^{WLODKVTH}} + \frac{PKVTH0}{(L_{drawn} + XL)^{LLODKVTH} \cdot (W_{drawn} + XW + WLOD)^{WLODKVTH}} \right) \cdot \left(1 + TKU0 \cdot \left(\frac{Temperature}{TNOM} - 1 \right) \right)$$

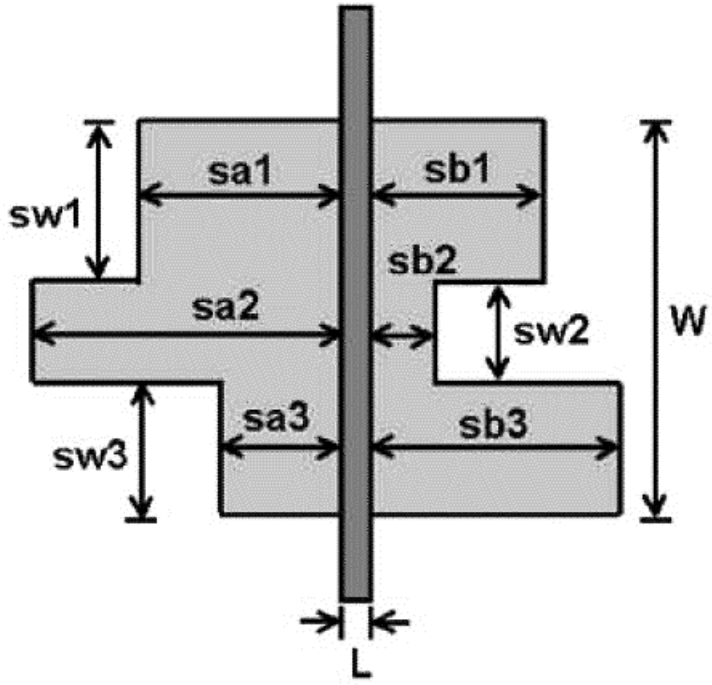
(22-223)

$$Inv_sa = \frac{1}{NF} \sum_{i=0}^{NF-1} \frac{1}{SA + 0.5 \cdot L_{drawn} + i \cdot (SD + L_{drawn})}$$

© 2023 Cadence Design Systems, Inc.

(22-224)

$$Inv_sb = \frac{1}{NF}\sum_{i=0}^{NF-1}\frac{1}{SB + 0.5\cdot L_{drawn} + i\cdot(SD + L_{drawn})}$$



For irregular LOD device like above figure, more instance parameters (swi, sai and sbi) are needed. Then,

(22-225)

$$Inv_sa = \sum_{i=1}^{n}\frac{sw_i}{W_{drawn}}\cdot\frac{1}{sa_i + 0.5\cdot L_{drawn}}$$

(22-226)

$$Inv_sb = \sum_{i=1}^{n}\frac{sw_i}{W_{drawn}}\cdot\frac{1}{sb_i + 0.5\cdot L_{drawn}}$$

© 2023 Cadence Design Systems, Inc.

Well Proximity Effect Model

Deep buried layers can affect devices located near the mask edge. Some of the ions scattered out of the edge of the photoresist are implanted in the silicon surface near the mask edge, altering the threshold voltage of those devices. BSIM4 considers the influence of well proximity effect on threshold voltage, mobility, and body effect as following:

(22-227)

$$Vth0 = Vth0_{org} + KVTH0WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC)$$

(22-228)

$$\mu_{eff} = \mu_{eff,org} \cdot (1 + KU0WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC))$$

(22-229)

$$K2 = K2_{org} + K2WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC)$$

TMIBSIM4 Model (tmibsim4)

The TSMC Model Interface (TMI) implements a modified version of the BSIM4 model, known as TMIBSIM4. You can activate the `tmibsim4` model by specifying the `tmiflag` and `tmipath` parameters as follows:

```
.options tmiflag = 1
.option tmipath = TMI_shared-library_path
```

Related Topics

BSIM4 Level-14 Model (bsim4)

Effective Oxide Thickness, Channel Length and Channel Width

Threshold Voltage Model

Channel Charge and Subthreshold Swing Models

Gate Direct Tunneling Current Model

High Speed/RF Models

© 2023 Cadence Design Systems, Inc.

Noise Models

Models and Equations in Version Updates

This topic briefly lists equations and information for various BSIM4 model versions. For more details, refer to UC Berkeley's BSIM4.64 Users' Manual

http://www-device.eecs.berkeley.edu/~bsim3/BSIM4/BSIM464/BSIM464_Manual.pdf

BSIM4 Version 4

BSIM4.4 has the following updates.

Trap-Assisted-Tunneling Current

(22-230)

$$I_{bs,d} = I_{sbs,d}\left[\exp\left(\frac{qV_{bs,d}}{NJS,D \cdot k_B T}\right) - 1\right] \cdot f_{breakdown}$$
$$-W_{effcj} \cdot NF \cdot J_{tsswgs,d}(T) \cdot \left[\exp\left(\frac{-V_{bs,d}}{NJTSSWG(T) \cdot Vtm0} \cdot \frac{VTSSWGS,D}{VTSSWGS,D - V_{bs,d}}\right) - 1\right]$$
$$- P_{s,deff} J_{tssws,d}(T)\left[\exp\left(\frac{-V_{bs,d}}{NJTSSW(T) \cdot Vtm0} \cdot \frac{VTSSWS,D}{VTSSWS,D - V_{bs,d}}\right) - 1\right]$$
$$- A_{s,deff} J_{tss,d}(T)\left[\exp\left(\frac{-V_{bs,d}}{NJTS(T) \cdot Vtm0} \cdot \frac{VTSS,D}{VTSS,D - V_{bs,d}}\right) - 1\right]$$
$$+ V_{bs,d} \cdot G_{min}$$

Flatband Voltage Offset Parameter

VFBSDOFF is an offset voltage added to the original source/drain flatband voltage which allows independent setting of V_{fbsd} to accurately model gate overlap tunneling current.

(22-231)

$$V_{fbsd} = k_B T/q \log(NGATE/NSD) + VFBSDOFF$$

© 2023 Cadence Design Systems, Inc.

Length Reduction Parameter Offset

BSIM4.4 has a new parameter LINTNOI which is an offset to the length reduction parameter (Lint) for flicker noise.

For fnoiMod=1 (unified model), the noise density in the inversion region is:

© 2023 Cadence Design Systems, Inc.

(22-232)

$$S_{id,\,inv}(f) = \frac{k_B T q^2 \mu_{eff} I_{ds}}{C_{oxe}(L_{eff}+LINTNOI)^2 A_{bulk} f^{ef}}\left(NOIA \cdot \log\left(\frac{N_0+N^*}{N_l+N^*}\right) + NOIB \cdot (N_o - N_l) + \frac{NOIC}{2}({N_0}^2 - {N_l}^2)\right) + \frac{k_B (TI_{ds}{}^2 \Delta L_{clm})}{W_{eff} \cdot (L_{eff}+LINTNOI)^2 f^{ef} \cdot 10^{10}} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot {N_l}^2}{(N_l+N^*)^2}$$

New Temperature Model

(22-233)

$$J_{tsswgs,\,d}(T) = J_{tsswgs,\,d}(TNOM) \cdot \exp\left[\frac{-Eg(TNOM)}{k_B T} \cdot X_{tsswgs,\,d} \cdot \left(1 - \frac{T}{TNOM}\right)\right]$$

(22-234)

$$J_{tssws,\,d}(T) = J_{tssws,\,d}(TNOM) \cdot \exp\left[\frac{-Eg(TNOM)}{k_B T} \cdot X_{tssws,\,d} \cdot \left(1 - \frac{T}{TNOM}\right)\right]$$

(22-235)

$$J_{tss,\,d}(T) = J_{tss,\,d}(TNOM) \cdot \exp\left[\frac{-Eg(TNOM)}{k_B T} \cdot X_{tss,\,d} \cdot \left(1 - \frac{T}{TNOM}\right)\right]$$

(22-236)

$$NJTSSWG(T) = NJTSSWG(TNOM) \cdot \left[1 + TNJTSSWG\left(\frac{T}{TNOM} - 1\right)\right]$$

(22-237)

$$NJTSSW(T) = NJTSSW(TNOM) \cdot \left[1 + TNJTSSW\left(\frac{T}{TNOM} - 1\right)\right]$$

(22-238)

$$NJTS(T) = NJTS(TNOM) \cdot \left[1 + TNTJS\left(\frac{T}{TNOM} - 1\right)\right]$$

© 2023 Cadence Design Systems, Inc.

BSIM4 Version 5

BSIM4.5.0 has the following new features:

- A mobility model which accounts for Coulomb scattering effect as well as the channel length dependence of mobility due to heavy halo-doping
- A scalable substrate resistance model (rbodyMod = 2) that is scalable with channel length, channel width, and number of fingers
- Gate resistance parameters XGW, NGCON that can now be specified as instance parameters (XGL is still a model parameter)
- Additional temperature dependence of model parameters VOFF and VFBSDOFF
- Enhanced tempMod = 2, where Vth(DITS) and gate tunneling models are functions of nominal temperature and the temperature dependence of zero-bias flat-band voltage is added
- A new instance parameter DELVTO that may be used to represent threshold voltage variation
- A new well-proximity effect model developed by CMC companies
- Igc Vbs dependence improvement with the full BSIM4 Vth model implemented

Mobility Model

Mobility Coulomb Scattering Model and Leff dependence

(22-239)

mobMod=0

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UCV_{bseff})\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)^2 + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th} + 0.0001}}\right)^2}$$

(22-240)

mobMod=1

© 2023 Cadence Design Systems, Inc.

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + \left[UA\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)^2\right](1 + UC \cdot V_{bseff}) + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th} + 0.0001}}\right)^2}$$

(22-241)

mobMod=2

$$\mu_{eff} = U0/1 + (UA + UC \cdot V_{bseff})\left[\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE}\right]^{EU} + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.0001}}\right)^2$$

where the constant C0 = 2 for NMOS and 2.5 for PMOS.

(22-242)

$$f(L_{eff}) = 1 - UP \cdot e^{-L_{eff}/(LP)}$$

Scalable Substrate Resistance Model

(22-243)

$$R_X = R_{X_HORT} \parallel R_{X_VERT} \qquad where\ R_{X_H(V)} = R_0 L^a W^{\beta} NF$$

© 2023 Cadence Design Systems, Inc.

Temperature Dependence for VOFF, VFBSDOFF

(22-244)

$$VOFF(T) = VOFF(TNOM) \cdot [1 + TVOFF \cdot (T - TNOM)]$$

(22-245)

$$VFBSDOFF(T) = VFBSDOFF(TNOM) \cdot [1 + TVFBSDOFF \cdot (T - TNOM)]$$

New Temperature Mode (TempMod = 2)

Share the same temperature equations as for TempMod=1 with the following modifications:

From

(22-246)

$$\Delta V_{th}(DITS) = -nv_t \cdot \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot (1 + e^{-DVPT1 \cdot V_{ds}})}\right)$$

To

(22-247)

$$\Delta V_{th}(DITS) = -nv_{tnom} \cdot \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot (1 + e^{-DVPT1 \cdot V_{ds}})}\right)$$

Vfbzb(T)

(22-248)

$$V_{fbzb}(T) = V_{fbzb}(TNOM) - KT1 \cdot \left(\frac{T}{TNOM} - 1\right)$$

Igate(T)

T is replaced by TNOM

© 2023 Cadence Design Systems, Inc.

DELVTO: An Instance Parameter

if vth0 is given:

(22-249)

$$Vth0 = Vth0 + DELVTO$$

if vth0 is not given,

(22-250)

$$Vfb = Vfb + DELVTO$$

(22-251)

$$Vth0 = Vfb + \Phi + k1 \times \sqrt{k1}$$

Well-Proximity Effect Modeling

Instance parameters: SCA, SCB, SCC, SC

Model parameters: WEB, WEC, KVTH0WE, K2WE, KU0WE, SCREF, WPEMOD

Model equations:

(22-252)

$$Vth0 = Vth0_{org} + KVTH0WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC)$$

(22-253)

$$K2 = K2_{ORG} + K2WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC)$$

(22-254)

$$\mu_{eff} = \mu_{eff,\,org} \cdot (1 + KU0WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC))$$

© 2023 Cadence Design Systems, Inc.

Gate Current Vbs Dependence

(22-255)

$$Igc0 = W_{eff}L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gse} \cdot V_{aux} \cdot \exp[-B \cdot TOXE(AIGC - BIGC \cdot V_{OXDEPINV}) \cdot (1 + CIGC \cdot v_{oxdepinv})]$$

For IGCMOD=1

(22-256)

$$V_{aux} = NIGC \cdot v_t \cdot \log\left(1 + \exp\left(\frac{V_{gse} - VTH\ 0}{NIGC \cdot v_t}\right)\right)$$

For IGCMOD=2

(22-257)

$$V_{aux} = NIGC \cdot v_t \cdot \log\left(1 + \exp\left(\frac{V_{gse} - VTH_\text{bsim4}}{NIGC \cdot v_t}\right)\right)$$

Implementing full BSIM4 Vth model into Igc enables the accurate prediction of Igc Vbs dependence.

BSIM4 Version 6

GISL and GIDL Leakage Module

Four new parameters have been added.

Junction Diode I-V

In BSIM4.5.0, the junction diode current due to the trap-assisted tunneling current in space-charge region has same set of parameters for both source and drain junctions.

© 2023 Cadence Design Systems, Inc.

Gate Tunneling Current

In BSIM4.5.0, the gate tunneling current in the overlapping S/D diffusion regions (IGS / IGD) share the same set of parameters for both source and drain (DLCIG, AIGSD, BIGSD, CIGSD).

In BSIM4.6.0, the parameters for IGS and IGD are separate.

- I_{GS} : DLCIG, AIGS, BIGS, CIGS
- I_{GD} : DLCIGD, AIGD, BIGD, CIGD

Mobility Model

The coulomb scattering term has been modified in BSIM4.6.0 release to avoid the possibility of non-monotonic drain current trend with respect to gate voltage.

mobMod=0

(22-258)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UCV_{bseff})\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)^2 + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.00001}}\right)^2}$$

mobMod=1

(22-259)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + \left[UA\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)^2\right](1 + UC \cdot V_{bseff}) + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.00001}}\right)^2}$$

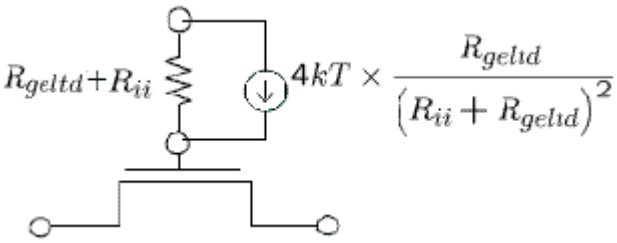
mobMod=2

(22-260)

$$\mu_{eff} = \frac{U0}{1 + (UA + UC \cdot V_{bseff})\left[\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE}\right]^{EU} + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.00001}}\right)^2}$$

© 2023 Cadence Design Systems, Inc.

Improvement to NOIMOD = 2



BSIM4 Version 6.1

C-V Model

A new VgsteffCV definition is introduced in the C-V model to improve threshold fitting. Six new parameters have been added: CVCHARGEMOD, MINVCV, LMINVCV, WMINVCV, WMINVCV, PMINVCV, and VOFFCVL.

New Material Model

A new materials model (activated by setting MTRLMOD=1) has been introduced with the following features:

- Predictive modeling of
  - Non-SiO2 insulator
  - Non-poly-Si gate
    New parameters
  - Non-silicon channel
- Improved predictive models for GIDL/GISL leakage current, mobility degradation, and short channel effects
- A model selector (MTRLMOD) is used to turn on/off all the new materials parameters and equations for backward compatibility.

© 2023 Cadence Design Systems, Inc.

New Materials Model Parameters

Model selector:

MTRLMOD : =1 activates the new-materials option and =0 (default) deactivates

For non-poly-silicon gate:

- PHIG : Gate work function
- EPSRGATE : Dielectric constant of gate relative to vacuum (= 0 deactivates poly depletion)

For non-SiO2 gate-dielectric:

- EOT : Equivalent SiO2 thickness
- VDDEOT : Gate voltage at which EOT is measured

For non-silicon channel material:

- EASUB : Electron affinity of substrate
- EPSRSUB : Dielectric constant of substrate relative to vacuum
- NI0SUB : Intrinsic carrier concentration at T=300.15K
- BG0SUB : Band-gap of substrate at T=0K
- TBGASUB : First parameter of band-gap change due to temperature
- TBGBSUB : Second parameter of band-gap change due to temperature
- ADOS : Density of states parameter to control charge centroid
- BDOS : Density of states parameter to control charge centroid

© 2023 Cadence Design Systems, Inc.

Non-Silicon Channel Material

Defines the temperature-dependent intrinsic carrier concentrations and the band gap with the new non-silicon parameters for MTRLMOD = 1.

(22-261)

$$Eg0 = BG0SUB - \frac{TBGASUB \times Tnom^2}{Tnom + TBGBSUB}$$

(22-262)

$$Eg(300.15) = BG0SUB - \frac{TBGASUB \times 300.15^2}{300.15 + TBGBSUB}$$

(22-263)

$$ni = NI0SUB \times \left(\frac{Tnom}{300.15}\right)^{3/2} \cdot e^{\frac{Eg(300.15K) - Eg0}{2V_t}}$$

(22-264)

$$Eg = BG0SUB - \frac{TBGASUB \times Temp^2}{Temp + TBGBSUB}$$

Introduces two new parameters for charge centroid for non-silicon channel materials in both I-V and C-V models.

(22-265)

$$X_{dc} = \frac{ADOS \times 1.9 \times 10^{-9}}{1 + \left(\frac{Vgsteff + (VTH0 - VFB - \phi_s)}{2toxp}\right)^{0.7 \times BDOS}}$$

© 2023 Cadence Design Systems, Inc.

Non-SiO2 Dielectric Material

For MTRLMOD = 1, use EOT (defined as the electrical oxide thickness at V_{gs} = VDDEOT) to calculate oxide thickness at flatband voltage.

(22-266)

$$Toxp = EOT - \frac{3.9}{EPSRSUB} \cdot X_{dc|Vgs = VDDEOT,\ V_{ds} = V_{bs} = 0}$$

Non-poly-Si gate Material

Poly depletion is calculated using the following equation:

(22-267)

$$V_{gse} = VFB + \Phi_s + \frac{q\varepsilon_{gate}NGATE}{coxe^2}\left(\sqrt{1 + \frac{2coxe^2(V_{gs} - VFB - \Phi_s)}{q\varepsilon_{gate}NGATE}} - 1\right)$$

where

(22-268)

$$\varepsilon_{gate} = EPSRGATE \cdot EPS0 \qquad for\ \text{MTRLMOD=1}$$
$$\varepsilon_{gate} = EPSSI \qquad for\ \text{MTRLMOD=0}$$

Setting EPSRGATE = 0 turns the poly depletion model off.

Improved Mobility Model

The new equations for the improved mobility model are given in the coming sections.

Improved GIDL/GISL Model

For MTRLMOD=1, the flat band voltage at source/drain is given in the coming sections. New equations for the GIDL and GISL model are also given.

© 2023 Cadence Design Systems, Inc.

BSIM4 Version 6.2

Width Dependent TAT Model

New Model Parameter

A new model parameter `JTWEFF` is added to describe the TAT current width dependence.

Change in Equation for Temperature Dependence of Junction Diode IV

Side Source Diode 0

(22-269)

$$I_{sbs} = A_{seff}J_{ss}(T) + P_{seff}J_{ssws}(T) + W_{effcj} \cdot NF \cdot J_{sswgs}(T)$$

where

(22-270)

$$J_{ss}(T) = JSS(TNOM) \cdot \exp\left(\frac{\frac{E_g(TNOM)}{v_t(TNOM)} - \frac{E_g(T)}{v_t(T)} + XTIS \cdot \ln\left(\frac{T}{TNOM}\right)}{NJS}\right)$$

(22-271)

$$J_{ssws}(T) = JSSWS(TNOM) \cdot \exp\left(\frac{\frac{E_g(TNOM)}{v_t(TNOM)} - \frac{E_g(T)}{v_t(T)} + XTIS \cdot \ln\left(\frac{T}{TNOM}\right)}{NJS}\right)$$

© 2023 Cadence Design Systems, Inc.

(22-272)

$$J_{sswgs}(T) = JSSWGS(TNOM)x\left(\sqrt{\frac{JTWEFF}{W_{effci}}} + 1.0\right)\exp\left(\frac{\frac{E_g(Tnom)}{V_t(Tnom)} - \frac{E_g(T)}{V_t(T)} + XTIS \cdot \ln\left(\frac{T}{Tnom}\right)}{NJS}\right)$$

where

(22-273)

$$E_g(TNOM) = 1.16 - \frac{7.02 \times 10^{-4} TNOM^2}{TNOM + 1108}$$

(22-274)

$$E_g(T) = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

(22-275)

$$n_i = 1.45e10 \cdot \frac{TNOM}{300.15} \cdot \sqrt{\frac{TNOM}{300.15}} \cdot \exp\left[21.5565981 - \frac{qE_g(TNOM)}{2 \cdot k_B T}\right]$$

High K Mobility

New Model Parameters

The following new model parameters are added:

- LUCS
- LUCSTE
- PUCS
- PUCSTE
- UCS

© 2023 Cadence Design Systems, Inc.

- UCSTE
- WUCS
- WUCSTE

The UCS parameter is temperature dependent as given below:

(22-276)

$$UCS(T) = UCS(TNOM) \cdot \left(\frac{T}{TNOM}\right)^{UCSTE}$$

New Mobility Model for High K Material

A new mobility model `mobMod=3` is added to enhance the modeling of coulomb scattering in high-k and metal gate transistors.

New Temperature Mode (tempMod = 3) for Mobility

`tempMod=3` only affects the mobility. Other parameters, such as `Rs` and `Rd` are the same as in `tempMod=2`.

Note the following:

- For `tempMod=1`, `tempMod=2` and `tempMod=3`:

(22-277)

$$U0(T) = U0(TNOM) \cdot \left(\frac{T}{TNOM}\right)^{UTE}$$

and

(22-278)

$$UCS(T) = UCS(TNOM) \cdot \left(\frac{T}{TNOM}\right)^{UCSTE}$$

- However, when `tempMod=3`:

(22-279)

$$UA(T) = UA(TNOM) \cdot \left(\frac{T}{TNOM}\right)^{UA1}$$

© 2023 Cadence Design Systems, Inc.

(22-280)

$$UB(T) = UB(TNOM) \cdot \left(\frac{T}{TNOM}\right)^{UB1}$$

(22-281)

$$UC(T) = UC(TNOM) \cdot \left(\frac{T}{TNOM}\right)^{UC1}$$

(22-282)

$$UD(T) = UD(TNOM) \cdot \left(\frac{T}{TNOM}\right)^{UD1}$$

BSIM4 Version 7.0

GIDL/GISL Model

A new model selector GIDLMOD=1 is introduced to decouple V_d from V_g through new parameters RGIDL, KGIDL and FGIDL (same for GISL).

(22-283)

$$I_{GIDL} = AGIDL \cdot W_{diod} \cdot Nf \cdot \frac{V_{ds} - RGIDL \cdot V_{gse} - EGIDL + V_{fbsd}}{3 \cdot T_{oxe}} \cdot \exp\left(-\frac{3 \cdot T_{oxe} \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL}\right) \cdot \exp\left(\frac{KGIDL}{V_{ds} - FGIDL}\right)$$

DIBL/Rout Model

A new function tanh() is introduced to capture the V_{ds} effect in long channel devices.

© 2023 Cadence Design Systems, Inc.

(22-284)

$$V_{th} = VTH0 + (K_{10x} \cdot \sqrt{\Phi_s - V_{bseff}} - K1 \cdot \sqrt{\Phi_s}) \sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox} V_{bseff}$$
$$+ K_{1ox} \left(\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1 \right) \sqrt{\Phi_s} + (K3 + K3B \cdot V_{bseff}) \frac{TOXE}{W_{eff}' + W0} \Phi_s$$
$$-0.5 \cdot \left[\frac{DVT0W}{\cosh\left(DVT1W \frac{L_{eff} W_{eff}'}{l_{tw}} \right) - 1} + \frac{DVT0}{\cosh\left(DVT1 \frac{L_{eff}}{l_t} \right) - 1} \right] (V_{bi} - \Phi_s)$$
$$- \frac{0.5}{\cosh\left(DSUB \frac{L_{eff}}{l_{t0}} \right) - 1} (ETA0 + ETAB \cdot V_{bseff}) \cdot V_{ds}$$
$$- nv_t \cdot 1n \left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot \left(1 + e^{-DVTPI \cdot V_{DS}} \right)} \right)$$
$$- \left(DVTP5 + \frac{DVTP2}{L_{eff}^{DVTP3}} \right) \cdot \tanh(DVTP4 \cdot V_{ds})$$

where DVTP2, DVTP3, DVTP4, and DVTP5 are new model parameters.

Temperature Dependence of Subthreshold Leakage Current

The new temperature dependence of subthreshold leakage current is modeled by:

(22-285)

$$Nfactor(T) = nfactor(Tnom) + tnfactor\left(\frac{T}{Tnom} - 1 \right)$$

$$ETA0(T) = ETA0(Tnom) + TETA0 * \left(\frac{T}{Tnom} - 1 \right)$$

$$voffCV(T) = voffCV * (1.0 + tvoffCV * (T - Tnom))$$

where tnfactor, TETA0, and tvoffCV are the new model parameters.

© 2023 Cadence Design Systems, Inc.

New Model Selector for MTRLMOD=0 and MTRLMOD=1 Compatibility

A new model selector MTRLCOMPATMOD=1 is introduced to make MTRLMOD=0 and MTRLMOD=1 consistent.

Physical Oxide Thickness

When MTRLMOD=1 and MTRLCOMPATMOD=1

(22-286)

$$T_{oxp} = EOT * \frac{EPSROX}{3.9} - DTOX$$

Effective Field for Mobility Calculation

(22-287)

$$E_{eff}(V_{gsteff} + 2V_{th} - 2(V_{fb} + \phi_{st})) \qquad \text{for mtrlMod} = 1$$

$$E_{eff}(V_{gsteff} + 2V_{th}) \qquad \text{for mtrlMod} = 0$$

With MTRLCOMPATMOD=1 and MTRLMOD=1

(22-288)

$$E_{eff}(V_{gsteff} + 2V_{th})$$

Enhanced Thermal Noise Model

A new thermal noise model tnoimod=2 has been implemented in SPICE3. Following new expressions have been added for drain noise (S_{id}), induced gate noise (S_{ig}) and correlation coefficient (c):

Drain Noise

(22-289)

$$S_{id} = 4kT \cdot \gamma \cdot g_{d0} \cdot (3 \cdot \beta_{noi}{}^{2})$$

© 2023 Cadence Design Systems, Inc.

Induced Gate Noise

(22-290)

$$S_{ig0} = 4kT \cdot C_0{}^2 \cdot \omega^2 \cdot \frac{\delta}{g_{d0}} \cdot \left(\frac{15 \cdot \theta_{noi}}{4}^2\right)$$

Correlation Coefficient

(22-291)

$$c = -j\sqrt{\frac{\varepsilon}{\gamma \cdot \delta}} \cdot \left(\frac{c_{tnoi}}{0.395}\right)$$

Where

(22-292)

$$\beta_{noi} = RNOIA \cdot \left[1 + TNOIA \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right] \qquad RNOIA = 0.577(\text{default})$$

$$\theta_{noi} = RNOIB \cdot \left[1 + TNOIB \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right] \qquad RNOIB = 0.5164(\text{default})$$

$$C_{tnoi} = RNOIC \cdot \left[1 + TNOIC \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right] \qquad RNOIC = 0.395(\text{default})$$

$$g_{d0} = NF \times \frac{\mu_{eff}C_{oxeff}\frac{W_{eff}}{L_{eff}}V_{gsteff}}{1 + gche \cdot R_{ds}}$$

$$C_0 = NF \times C_{oxeff}W_{eff,CV}L_{eff,CV}$$

BSIM4 Version 8.0

© 2023 Cadence Design Systems, Inc.

Mobility Models

BSIM4.80 introduces three new mobility models mobmod=4, mobmod=5, and mobmod=6. See equations 22-31, 22-32, and 22-33 for details.

Related Topics

BSIM4 Level-14 Model (bsim4)

BSIM4 Version 4

BSIM4 Version 5

BSIM4 Version 6

BSIM4 Version 6.1

BSIM4 Version 6.2

BSIM4 Version 7.0

Component Statements

This device is supported within altergroups.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

w (m)	Channel width.
l (m)	Channel length.
as (m^2)	Area of source diffusion.
ad (m^2)	Area of drain diffusion.
ps (m)	Perimeter of source diffusion.
pd (m)	Perimeter of drain diffusion.

© 2023 Cadence Design Systems, Inc.

nrd	Number of squares of drain diffusion.
nrs	Number of squares of source diffusion.
rdc=0.0 Ω	Drain contact resistance.
rsc=0.0 Ω	Source contact resistance.
sa=0.0 m	Distance between OD edge to poly from one side.
sb=0.0 m	Distance between OD edge to poly from the other side.
sd=0.0 m	Distance between neighbor fingers.
sa1=0.0 m	Distance between OD edge to poly from one side 1.
sa2=0.0 m	Distance between OD edge to poly from one side 2.
sa3=0.0 m	Distance between OD edge to poly from one side 3.
sa4=0.0 m	Distance between OD edge to poly from one side 4.
sa5=0.0 m	Distance between OD edge to poly from one side 5.
sa6=0.0 m	Distance between OD edge to poly from one side 6.
sa7=0.0 m	Distance between OD edge to poly from one side 7.
sa8=0.0 m	Distance between OD edge to poly from one side 8.
sa9=0.0 m	Distance between OD edge to poly from one side 9.
sa10=0.0 m	Distance between OD edge to poly from one side 10.
sb1=0.0 m	Distance between OD edge to poly from other side 1.
sb2=0.0 m	Distance between OD edge to poly from other side 2.
sb3=0.0 m	Distance between OD edge to poly from other side 3.
sb4=0.0 m	Distance between OD edge to poly from other side 4.
sb5=0.0 m	Distance between OD edge to poly from other side 5.
sb6=0.0 m	Distance between OD edge to poly from other side 6.
sb7=0.0 m	Distance between OD edge to poly from other side 7.
sb8=0.0 m	Distance between OD edge to poly from other side 8.
sb9=0.0 m	Distance between OD edge to poly from other side 9.
sb10=0.0 m	Distance between OD edge to poly from other side 10.
sw1=0.0 m	Width of SA1/SB1.
sw2=0.0 m	Width of SA2/SB2.

© 2023 Cadence Design Systems, Inc.

`sw3=0.0 m`	Width of SA3/SB3.
`sw4=0.0 m`	Width of SA4/SB4.
`sw5=0.0 m`	Width of SA5/SB5.
`sw6=0.0 m`	Width of SA6/SB6.
`sw7=0.0 m`	Width of SA7/SB7.
`sw8=0.0 m`	Width of SA8/SB8.
`sw9=0.0 m`	Width of SA9/SB9.
`sw10=0.0 m`	Width of SA10/SB10.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.
`m=1`	Multiplicity factor (number of MOSFETs in parallel).
`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trnqsmod`	Transient NQS model selector.
`acnqsmod`	AC small-signal NQS model selector.
`trise (C)`	Temperature rise from ambient.
`dtemp (C)`	Alias for trise.
`deltox=0 m`	Shift in gate electrical/physical equivalent oxide thickness (for both TOXE and TOXP).
`rgatemod`	Gate resistance model selector.
`rbodymod`	Substrate resistance network model selector.
`geomod`	Geometry-dependent parasitics model selector.
`stimod`	LOD stress effect model selector.
`rgeomod`	Diffusion resistance and contact model selector.
`rbpb (Ω)`	Resistance connected between bNode' and bNode.
`rbpd (Ω)`	Resistance connected between bNode' and dbNode.
`rbps (Ω)`	Resistance connected between bNode' and sbNode.
`rbdb (Ω)`	Resistance connected between dbNode and bNode.
`rbsb (Ω)`	Resistance connected between sbNode and bNode.

© 2023 Cadence Design Systems, Inc.

`nf`	Number of device fingers.
`min`	If set to 0, minimizes the number of drain or source diffusions for even numbered fingered devices.
`delvto=0.0 V`	Shift in zer0-bias threshold voltage vth0.
`mulmu0=1.0`	Mobility multiplier; alias of mulu0.
`mulvsat=1.0`	Vsat multiplier.
`mulu0=1.0`	Mobility multiplier.
`mulid0=1.0`	Ids multiplier.
`mulbeta=1.0`	Beta multiplier.
`delk1=0.0 V`	Shift in body bias coefficient k1.
`delnfct=0.0`	Shift in subthreshold swing factor nfactor.
`deleta0=0.0`	Shift in DIBL coefficient subthreshold region.
`sca=0.0`	Integral of the first distribution function for scattered well dopant.
`scb=0.0`	Integral of the second distribution function for scattered well dopant.
`scc=0.0`	Integral of the third distribution function for scattered well dopant.
`sc=0.0 m`	Distance to a single well edge.
`xgw=0.0 m`	Distance from the gate contact to the channel edge.
`ngcon=1.0`	Number of gate contacts.

Model Syntax

```
model modelName bsim4 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` and `p`.

Model Selectors & Controller

`level=14`	Model level selector for SPICE compatibility.
`version=4.21`	Model parameter "version" only accepts real number value, like 4.21 for version=4.2.1. The available versions are 4.00(4.0.0), 4.10(4.1.0), 4.20(4.2.0), 4.21(4.2.1), 4.30(4.3.0), 4.40(4.4.0), 4.50(4.5.0), 4.60(4.6.0), 4.61(4.6.1), 4.62(4.6.2), 4.63(4.6.3), 4.64(4.6.4), 4.65(4.6.5), 4.70(4.7.0), 4.80(4.8.0), 4.81(4.8.1) and 4.82(4.8.2).
`binunit=1`	Bin parameter unit selector. 1 for microns and 2 for meters.
`paramchk=1`	Switch for parameter value check. Set to 1 to turn on parameter checking.
`mobmod=0`	Mobility model selector. Valid values are between 0 and 6. Values 4, 5, and 6 are valid only since version 4.8.0.
`cvchargemod=0.0`	Capacitance charge model selector.
`mtrlmod=0.0`	Parameter for non-silicon substrate or metal gate selector.
`mtrlcompatmod=0`	New material mod backward compatibility model selector.
`rdsmod=0`	Bias-dependent source/drain resistance model selector.
`igcmod=0`	Gate-to-channel tunneling model selector.
`igbmod=0`	Gate-to-substrate tunneling model selector.
`capmod=2`	Capacitance model selector.
`rgatemod=0`	Gate resistance model selector.
`rbodymod=0`	Substrate resistance network model selector.
`trnqsmod=0`	Transient Non-quasi static model selector. Set to 1 to turn on nqs.
`acnqsmod=0`	Ac non-quasi static model selector. Set to 1 to turn on nqs.

© 2023 Cadence Design Systems, Inc.

`fnoimod=1`	Flicker noise model selector.
`tnoimod=0`	Thermal noise model selector.
`diomod=1`	Source/Drain junction diode IV model selector.
`tempmod=0`	Temperature model selector. 0 for original model and 1 for new format.
`permod=1`	Perimeter model selector.
`geomod=0`	Geometry-dependent parasitics model selector.
`stimod=0`	LOD stress effect model selector. 0 for Berkeley LOD, 1 & 2 for TSMC LOD.
`wpemod=0`	Flag for WPE model. Set WPEMOD=1 to activate this model.
`rgeomod=0`	Diffusion resistance and contact model selector. It serves as the default value of instance `rgeomod`.
`flkmod=0`	Flicker noise model.
`fullreinit=0`	Model parameter full reinit selector.
`updatelevel=0`	Model update selector. Available versions are 0, 1, and 2.
`eglev=0`	DC temperature selector.
`minr=0.001 Ω`	Minimum source/drain resistance.

Process parameters

`epsrox=3.9`	Gate dielectric constant.
`epsrgate=11.7`	Dielectric constant of gate relative to vacuum.
`epsrsub=11.7`	Dielectric constant of substrate relative to vacuum.
`eot=1.5e-9 m`	Equivalent gate oxide thickness in meters.
`toxe=3.0e-9 m`	Electrical gate equivalent oxide thickness.
`toxp=`toxem'`	Physical gate equivalent oxide thickness.
`toxm=`toxem'`	Toxe at which parameters were extracted.
`dtox=0.0 m`	Difference between electrical and physical gate oxide thickness.

© 2023 Cadence Design Systems, Inc.

xj=0.15e-6 m	Source/drain junction depth.
gamma1 (√V)	Body-effect coefficient near the surface.
gamma2 (√V)	Body-effect coefficient in the bulk.
ndep=1.7e17 cm^{-3}	Channel doping concentration at depletion edge for zero body bias.
nsub=6.0e16 cm^{-3}	Substrate doping concentration.
ngate=0.0 cm^{-3}	Poly Si gate doping concentration.
nsd=1.0e20 cm^{-3}	Source-drain doping concentration.
vbx (V)	Vbs at which the depletion region width equals XT.
xt=1.55e-7 m	Doping depth.
rsh=0.0 Ω/sqr	Source/drain sheet resistance.
rshg=0.1 Ω/sqr	Gate electrode sheet resistance.
lint=0.0 m	Lateral diffusion for one side.
wint=0.0 m	Width reduction for one side.
wl=0.0 m^wln	Length dependence of delta W.
wln=1.0	Length exponent of delta W.
ww=0.0 m^wwn	Width dependence of delta W.
wwn=1.0	Width exponent of delta W.
wwl=0.0 m^(wwn+wln)	Area dependence of delta W.
ll=0.0 m^lln	Length dependence of delta L.
lln=1.0	Length exponent of delta L.
lw=0.0 m^lwn	Width dependence of delta L.
lwn=1.0	Width exponent of delta L.
lwl=0.0 m^(lln+lwn)	Area dependence of delta L.
dwg=0.0 m/V	Gate-bias dependence of channel width.
dwb=0.0 m/√V	Body-bias dependence of channel width.

© 2023 Cadence Design Systems, Inc.

`lmlt=1.0`	Length shrink reduction factor.
`wmlt=1.0`	Width shrink reduction factor.

Threshold voltage parameters

`vtho=0.7(nmos) / -0.7(pmos) V`	Threshold voltage at Vbs=0 for long-channel devices. Alias of vth0.
`vfb=-1.0 V`	Flat-band voltage.
`vddeot=1.5(nmos) / -1.5(pmos) V`	Voltage for extraction of equivalent gate oxide thickness.
`phin=0.0 V`	Non-uniform vertical doping effect on surface potential.
`k1=0.53 V`	First-order body bias coefficient.
`k2=-0.0186`	Second-order body bias coefficient.
`k3=80.0`	Narrow width coefficient.
`k3b=0.0 1/V`	Body effect coefficient of K3.
`w0=2.5e-6 m`	Narrow width coefficient.
`lpe0=1.74e-7 m`	Lateral non-uniform doping at Vbs=0.
`lpeb=0.0 m`	Lateral non-uniform doping effect on K1.
`vbm=-3.0 V`	Maximum applied body voltage in VTH0 calculation.
`dvt0=2.2`	First coefficient of short-channel effects.
`dvt1=0.53`	Second coefficient of short-channel effects.
`dvt2=-0.032 1/V`	Body-bias coefficient of short-channel effects.
`dvtp0=0.0 m`	First coefficient of drain-induced Vth shift for long-channel pocket devices.
`dvtp1=0.0 1/V`	Second coefficient of drain-induced Vth shift for long-channel pocket devices.
`dvtp2=0.0`	Third parameter for Vth shift due to pocket.
`dvtp3=0.0`	Fourth parameter for Vth shift due to pocket.

© 2023 Cadence Design Systems, Inc.

`dvtp4=0.0`	Fifth parameter for Vth shift due to pocket.
`dvtp5=0.0`	Sixth parameter for Vth shift due to pocket.
`dvt0w=0.0`	First coefficient of narrow-width effects.
`dvt1w=5.3e6 1/m`	Second coefficient of narrow-width effects.
`dvt2w=-0.032 1/V`	Body-bias coefficient of narrow-width effects.
`a0=1.0`	Non-uniform depletion width effect coefficient.
`ags=0.0 1/V`	Gate-bias dependence of Abulk.
`b0=0.0 m`	Bulk charge coefficient due to narrow width effect.
`b1=0.0 m`	Bulk charge coefficient due to narrow width effect.
`keta=-0.047 1/V`	Body-bias coefficient for non-uniform depletion width effect.
`a1=0.0 1/V`	First non-saturation effect parameter.
`a2=1.0`	Second non-saturation factor.
`phig=4.05 eV`	The gate work function.
`ni0sub=1.45e10` cm^{-3}	Intrinsic carrier concentration at T=300.15K.
`bg0sub=1.16 eV`	Band-gap of substrate at T=0K.
`tbgasub=7.02e-4` `V/K`	First parameter of band-gap change due to temperature.
`tbgbsub=1108.0 K`	Second parameter of bandgap change due to temperature.
`ados=1.0`	Charge centroid parameter.
`bdos=1.0`	Charge centroid parameter.
`tempeot=300.15 C`	Temperature for extraction of EOT.
`leffeot=1 m`	Effective length for extraction of EOT.
`weffeot=10 m`	Effective width for extraction of EOT.

© 2023 Cadence Design Systems, Inc.

`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
`acm=12`	Area calculation method selector.
`hdif=0 m`	Length of heavily doped diffusion.
`ldif=0 m`	Lateral diffusion beyond the gate.
`rs=12.5` Ω	Source resistance.
`rd=12.5` Ω	Drain resistance.
`ld (m)`	Lateral diffusion into the channel from the source and drain diffusion.
`trd=0 1/C`	Temperature parameter for drain resistance.
`trs=0 1/C`	Temperature parameter for source resistance.

Mobility parameters

`u0=670(nmos) / 250(pmos)`	Low-field surface mobility at tnom.
`ua=1.0e-9(mobmod=0,1) / 1.0e-15 (mobmod=2) m/V`	First-order mobility reduction coefficient.
`ub=1.0e-19` m^2/V^2	

© 2023 Cadence Design Systems, Inc.

	Second-order mobility reduction coefficient.
`uc=-0.0465 1/V (mobmod=1) / -0.0465e-9 m/V`^{2} `(mobmod=0,2)`	
	Body-bias dependence of mobility.
`ud=1.0e14 /m`^{2}	Coulomb scattering factor of mobility.
`up=0.0`	Channel length linear factor of mobility.
`lp=1.0e-8 m`	Channel length exponential factor of mobility.
`eu=1.67(nmos) / 1.0(pmos)`	
	Exponent for mobility degradation of mobmod=2.
`vsat=8.0e4 m/s`	Carrier saturation velocity at tnom.
`lambda=0.0`	Velocity overshoot coefficient.
`vtl=2.0e5 m/s`	Thermal velocity.
`lc=5.0e-9 m`	Velocity back scattering coefficient.
`xn=3.0`	Velocity back scattering coefficient.
`easub=4.05 eV`	Electron affinity of substrate.
`ucs=1.67(nmos) / 1.0(pmos)`	
	Coulomb scattering exponent.
`ucste=-4.775e-3`	Temperature coefficient of coulombic mobility.

Subthreshold parameters

`voff=-0.08 V`	Threshold voltage offset.
`tvoff=0.0 V`	Temperature parameter for voff.
`ltvoff=0.0 V`	Length dependence of tvoff.
`wtvoff=0.0 V`	Width dependence of tvoff.
`ptvoff=0.0 V`	Cross-term dependence of tvoff.
`voffl=0.0 mV`	Channel-length dependence of Voff.
`minv=0.0`	Vgsteff fitting parameter for moderate inversion condition.
`nfactor=1.0`	Subthreshold swing coefficient.
`eta0=0.08`	DIBL coefficient subthreshold region.

© 2023 Cadence Design Systems, Inc.

etab=-0.07 1/V	Body-bias dependence of et0.
dsub=`drout'	DIBL effect in subthreshold region.
cit=0.0 F/m^2	Interface trap parameter for subthreshold swing.
cdsc=2.4e-4 F/m^2	Source/drain and channel coupling capacitance.
cdscb=0.0 F/m^2 V	Body-bias dependence of cdsc.
cdscd=0.0 F/m^2 V	Drain-bias dependence of cdsc.

Output resistance parameters

pclm=1.3	Channel length modulation coefficient.
pdiblc1=0.39	First coefficient of drain-induced barrier lowering.
pdiblc2=8.6e-3	Second coefficient of drain-induced barrier lowering.
pdiblcb=0.0 1/V	Body-effect coefficient for DIBL.
drout=0.56	DIBL effect on output resistance coefficient.
pscbe1=4.24e8 V/m	First coefficient of substrate current body effect.
pscbe2=1e-5 m/V	Second coefficient of substrate current body effect.
fprout=0.0 V/m	Effect of pocket implant on Rout degradation.
pvag=0.0	Gate dependence of early voltage.
delta=0.01 V	Effective drain voltage smoothing parameter.
pdits=0.0 1/V	Effect of pocket implant on Rout degradation.
pditsl=0.0 1/m	Channel-length dependence of drain-induced Vth shift on Rout.
pditsd=0.0 1/V	Vds dependence of drain-induced Vth shift on Rout.

Bias-dependent Rds parameters

rdsw=200.0 Ω μm^wr	

© 2023 Cadence Design Systems, Inc.

	Zero bias LDD resistance per unit width for RDSMOD=0.
`rdswmin=0.0 Ω µm^wr`	
	LDD resistance per unit width at high Vgs and zero Vbs for RDSMOD=0.
`rdw=100.0 Ω µm^wr`	
	Zero bias LDD resistance per unit width for RDSMOD=1.
`rdwmin=0.0 Ω µm^wr`	
	LDD resistance per unit width at high Vgs and zero Vbs for RDSMOD=1.
`rsw=100.0 Ω µm^wr`	
	Zero bias LDD resistance per unit width for RDSMOD=1.
`rswmin=0.0 Ω µm^wr`	
	LDD resistance per unit width at high Vgs and zero Vbs for RDSMOD=1.
`prwg=1 1/V`	Gate-effect coefficient for Rds.
`prwb=0.0 1/V`	
	Body-effect coefficient for Rds.
`wr=1.0`	Width offset for parasitic resistance.

Substrate current parameters

`alpha0=0.0 A m/V`	Substrate current impact ionization coefficient.
`alpha1=0.0 A/V`	Substrate current impact ionization coefficient.
`beta0=30.0 1/V`	Substrate current impact ionization exponent.

Gate-Induced drain leakage parameters

`gidlmod=0`	Parameter for GIDL selector.
`agidl=0.0 1/Ω`	Pre-exponential coefficient for GIDL.
`bgidl=2.3e9 V/m`	Exponential coefficient for GIDL.

© 2023 Cadence Design Systems, Inc.

`cgidl=0.5 V^3`	Parameter for body-bias effect on GIDL.
`egidl=0.8 V`	Fitting parameter for band bending for GIDL.
`fgidl=0.0 V`	GIDL vb parameter.
`kgidl=0.0 V`	GIDL vb parameter.
`rgidl=1.0`	GIDL vg parameter.
`agisl=agidl 1/Ω`	Pre-exponential coefficient for GISL (bsim4.6).
`bgisl=bgidl V/m`	Exponential coefficient for GISL (bsim4.6).
`cgisl=cgidl V^3`	Parameter for body-bias effect on GISL (bsim4.6).
`egisl=egidl V`	Fitting parameter for band bending for GISL (bsim4.6).
`fgisl=fgidl V`	GISL vb parameter.
`kgisl=kgidl V`	GISL vb parameter.
`rgisl=rgidl`	GISL vg parameter.

Gate Tunneling parameters

`aigbacc=0.43 F/g s/m`	Parameter for Igb in accumulation.
`bigbacc=0.054 F/g s/(m V)`	Parameter for Igb in accumulation.
`cigbacc=0.075 1/V`	Parameter for Igb in accumulation.
`nigbacc=1.0`	Parameter for Igb in accumulation.
`aigbinv=0.35 F/g s/m`	Parameter for Igb in inversion.
`bigbinv=0.03 F/g s/(m V)`	Parameter for Igb in inversion.
`cigbinv=0.006 1/V`	Parameter for Igb in inversion.
`eigbinv=1.1 V`	Parameter for Igb in inversion.

© 2023 Cadence Design Systems, Inc.

`nigbinv=3.0`	Parameter for Igb in inversion.
`aigc=0.43(nmos) / 0.31(pmos) |F/g s/m`	Parameter for Igcs and Igcd.
`bigc=0.054(nmos) / 0.024(pmos) |F/g s/(m V)`	Parameter for Igcs and Igcd.
`cigc=0.075(nmos) / 0.03(pmos) 1/V`	Parameter for Igcs and Igcd.
`aigsd=0.43(nmos) / 0.31(pmos) |F/g s/m`	Parameter for Igs and Igd.
`bigsd=0.054(nmos) / 0.024(pmos) |F/g s/(m V)`	Parameter for Igs and Igd.
`cigsd=0.075(nmos) / 0.03(pmos) 1/V`	Parameter for Igs and Igd.
`aigs=1.36e-2(nmos) / 9.80e-3(pmos) |F/g s/m`	Parameter for Igs (bsim4.6).
`bigs=1.71e-3(nmos) / 7.59e-4(pmos) |F/g s/(m V)`	Parameter for Igs (bsim4.6).
`cigs=0.075(nmos) / 0.03(pmos) 1/V`	Parameter for Igs (bsim4.6).
`aigd=1.36e-2(nmos) / 9.80e-3(pmos) |F/g s/m`	Parameter for Igd (bsim4.6).
`bigd=1.71e-3(nmos) / 7.59e-4(pmos) |F/g s/(m V)`	Parameter for Igd (bsim4.6).
`cigd=0.075(nmos) / 0.03(pmos) 1/V`	Parameter for Igd (bsim4.6).
`dlcig=`Lintm'`	Source overlap length for Igs.
`dlcigd=dlcig m`	Drain overlap length for Igd (bsim4.6).
`nigc=1.0`	Parameter for Igcs, Igcd ,Igs, and Igd.

© 2023 Cadence Design Systems, Inc.

`poxedge=1.0`	Factor for the gate oxide thickness in source/drain overlap regions.
`pigcd=1.0`	Vds dependence of Igcs and Igcd.
`ntox=1.0`	Exponent for the gate oxide ratio.
`toxref=3.0e-9 m`	Nominal gate oxide thickness for gate dielectric tunneling current model only.
`vfbsdoff=0.0 V`	S/D flatband voltage offset.
`tvfbsdoff=0.0 V`	Temperature parameter for vfbsdoff.
`ltvfbsdoff=0.0 V`	Length dependence of tvfbsdoff.
`wtvfbsdoff=0.0 V`	Width dependence of tvfbsdoff.
`ptvfbsdoff=0.0 V`	Cross-term dependence of tvfbsdoff.

Overlap capacitance parameters

`cgso (F/m)`	Non-LDD region source-gate overlap capacitance per unit channel width.
`cgdo (F/m)`	Non-LDD region drain-gate overlap capacitance per unit channel width.
`cgbo=2 Dwc Coxe F/m`	Non-LDD region drain-gate overlap capacitance per unit channel width.
`meto=0.0 m`	Metal overlap in fringing field.
`cgsl=0.0 F/m`	Overlap capacitance between gate and lightly-doped source region.
`cgdl=0.0 F/m`	Overlap capacitance between gate and lightly-doped drain region.
`ckappas=0.6 V`	Coefficient of bias-dependent overlap capacitance for the source side.
`ckappad=`ckappasV'`	Coefficient of bias-dependent overlap capacitance for the drain side.

© 2023 Cadence Design Systems, Inc.

Charge model selection parameters

`xpart=0.0`	Charge partition number. Use 0.0 for 40/60, 0.5 for 50/50, and 1.0 for 0/100.
`cf (F/m)`	Fringing field capacitance (alias=lx91).
`clc=1e-7 m`	Constant term for the short channel model.
`cle=0.6`	Exponential term for the short channel model.
`dlc=`lintm'`	Delta L for capacitance model.
`dwc=`wintm'`	Delta W for capacitance model.
`vfbcv=-1.0`	Flat-band voltage for capmod=0.
`noff=1.0`	Transition parameter.
`voffcv=0.0 V`	CV parameter in VgsteffCV for weak-to-strong inversion.
`minvcv=0.0`	Fitting parameter for moderate inversion condition.
`voffcvl=0.0 V m`	Length dependence parameter for Vth offset in CV.
`acde=1.0 m/V`	Exponential coefficient for charge thickness in CAPMOD=2 for accumulation and depletion regions.
`moin=15.0`	Exponential coefficient for charge thickness for accumulation and depletion regions.
`llc=`llm^lln'`	Length dependence of delta L for CV.
`lwc=`lwm^lwn'`	Width dependence of delta L for CV.
`lwlc=`lwlm^(lln+lwn)'`	Area dependence of delta L for CV.
`wlc=`wlm^wln'`	Length dependence of delta W for CV.
`wwc=`wwm^wwn'`	Width dependence of delta W for CV.
`wwlc=`wwlm^(wwn+wln)'`	Area dependence of delta W for CV.

Parasitic resistance parameters

`dmcg=0.0 m`	Distance from S/D contact center to the gate edge.

© 2023 Cadence Design Systems, Inc.

`dmci=`dmcgm'`	Distance from S/D contact center to the isolation edge in the channel-length direction.
`dmdg=0.0 m`	Distance from S/D contact center to the gate edge.
`dmcgt=0.0 m`	DMCG of test structures.
`dwj=`dwcm'`	Offset of the S/D junction width.
`xgw=0.0 m`	Distance from the gate contact to the channel edge.
`xgl=0.0 m`	Offset of gate length due to variations in patterning.
`xl=0.0 m`	Length variation due to masking and etching.
`xw=0.0 m`	Width variation due to masking and etching.
`ngcon=1.0`	Number of gate contacts.
`nf=1`	Number of device fingers. It serves as the default value for instance nf.
`min=0`	If set to 0, minimizes the number of drain or source diffusions for even numbered fingered devices. It serves as the default value for instance min.

Junction diode model parameters

`ijthsrev=0.1 A`	Source diode limiting current in reverse bias region.
`ijthdrev=`ijthsrevA'`	Drain diode limiting current in reverse bias region.
`ijthsfwd=0.1 A`	Source diode limiting current in forward bias region.
`ijthdfwd=`ijthsfwdA'`	Drain diode limiting current in forward bias region.
`xjbvs=1.0`	Fitting parameter for bulk-source diode breakdown.
`xjbvd='xjbvs'`	Fitting parameter for bulk-drain diode breakdown.
`bv=10.0 V`	Diode breakdown voltage. Alias of bvs.
`bvs=10.0 V`	Source diode breakdown voltage.
`bv_enable=on`	Flag to enable the breakdown of diode. on=breakdown effect enabled, off=breakdown effect disabled. Possible values are `off` and `on`.

© 2023 Cadence Design Systems, Inc.

`bvd='bvsV'`	Drain diode breakdown voltage.
`is=1.0e-14 A`	Bulk junction reverse saturation current.
`js=1.0e-4 A/m`^{2}	Bottom junction reverse saturation current density. Alias of jss.
`jss=1.0e-4 A/m`^{2}	Source bottom junction reverse saturation current density.
`jsd='jssA/m'`^{2}	Drain bottom junction reverse saturation current density.
`jsws=0.0 A/m`	Isolation-edge sidewall source junction reverse saturation current density.
`jswd='jswsA/m'`	Isolation-edge sidewall drain junction reverse saturation current density.
`jswgs=0.0 A/m`	Gate-edge sidewall source junction reverse saturation current density.
`jswgd='jswgsA/m'`	Gate-edge sidewall drain junction reverse saturation current density.
`jtss=0.0 A/m`^{2}	Source bottom trap-assisted saturation current density.
`jtsd='jtssA/m'`^{2}	Drain bottom trap-assisted saturation current density.
`jtssws=0.0 A/m`	Source isolation-edge sidewall trap-assisted saturation current density.
`jtsswd='jtsswsA/m'`	Drain isolation-edge sidewall trap-assisted saturation current density.
`jtsswgs=0.0 A/m`	Source Gate-edge isolation-edge sidewall trap-assisted saturation current density.
`jtsswgd='jtsswgsA/m'`	Drain isolation-edge sidewall trap-assisted saturation current density.
`njts=20.0`	Non-ideality factor for jtss. For TSMC diode model, default=60.0.
`njtssw=20.0`	Non-ideality factor for jtssws. For TSMC diode model, default=60.0.
`njtsswg=20`	Non-ideality factor for jtsswgs. For TSMC diode model, default=60.0.
`njtsd=njts`	Non-ideality factor for jtsd (bsim4.6).

© 2023 Cadence Design Systems, Inc.

`njtsswd=njtssw`	Non-ideality factor for jtsswd (bsim4.6).
`njtsswgd=njtsswg`	Non-ideality factor for jtsswgd (bsim4.6).
`xtss=0.02`	Power dependence of jtss on temperature.
`xtsd='xtss'`	Power dependence of jtsd on temperature.
`xtssws=0.02`	Power dependence of jtssws on temperature.
`xtsswd='xtssws'`	Power dependence of jtsswd on temperature.
`xtsswgs=0.02`	Power dependence of jtsswgs on temperature.
`xtsswgd='xtsswgs'`	Power dependence of jtsswgd on temperature.
`vtss=10.0 V`	Source bottom trap-assisted voltage dependent parameter.
`vtsd='vtssV'`	Drain bottom trap-assisted voltage dependent parameter.
`vtssws=10.0 V`	Source STI sidewall trap-assisted voltage dependent parameter.
`vtsswd='vtsswsV'`	Drain STI sidewall trap-assisted voltage dependent parameter.
`vtsswgs=10.0 V`	Source gate-edge sidewall trap-assisted voltage dependent parameter.
`vtsswgd='vtsswgsV'`	Drain gate-edge sidewall trap-assisted voltage dependent parameter.
`tnjts=0.0`	Temperature coefficient for njts.
`tnjtssw=0.0`	Temperature coefficient for njtssw.
`tnjtsswg=0.0`	Temperature coefficient for njtsswg.
`tnjtsd=tnjts`	Temperature coefficient for njtsd (bsim4.6).
`tnjtsswd=tnjtsssw`	Temperature coefficient for njtsswd (bsim4.6).
`tnjtsswgd=tnjtsswg`	Temperature coefficient for njtsswgd (bsim4.6).
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*iabstol. Possible values are `yes` and `no`.

© 2023 Cadence Design Systems, Inc.

`imelt='imaxA'`	Explosion current.
`jmelt='jmaxA/m'`^{2}	Explosion current density.
`jtweff=0.0 m`	TAT current width dependence.

TSMC junction diode model parameters

`mnr=21.0`	Fitting parameter for resistance induced non-ideality factor.
`bnr=0.0`	Fitting parameter for resistance induced non-ideality factor.
`cnr=0.0 1/V m`	Fitting parameter for resistance induced non-ideality factor.
`dnr=0.0 1/V`	Fitting parameter for resistance induced non-ideality factor.
`tmnr=0.0`	Temperature coefficient for mnr.
`tcnr=0.0`	Temperature coefficient for cnr.
`tdnr=0.0`	Temperature coefficient for dnr.
`nrfwd=1.0 A/m`^{2}	Source bottom trap-assisted saturation current density.
`jsswg=0.0`	Sidewall-gate junction reverse saturation current density.

Junction capacitance model parameters

`cj=5e-4 F/m`^{2}	Zero bias bottom junction capacitance per unit area. Alias of cjs.
`cjs=5.0e-4 F/m`^{2}	Zero bias source bottom junction capacitance per unit area.
`cjd=`\`cjsF/m'^{2}	Zero bias drain bottom junction capacitance per unit area.
`mj=1/2`	Bottom junction capacitance grading coefficient. Alias of mjs.
`mjs=1/2`	Source bottom junction capacitance grading coefficient.
`mjd=`\`mjs'	Drain bottom junction capacitance grading coefficient.
`pb=1.0 V`	Bottom junction built-in potential. Alias of pbs.
`pbs=1.0 V`	Source bottom junction built-in potential.

© 2023 Cadence Design Systems, Inc.

`pbd=`pbsV'`	Drain bottom junction built-in potential.
`fc=0.5`	Forward-bias depletion capacitance threshold.
`cjsw=5e-10 F/m`	Sidewall junction capacitance per unit periphery. Alias of cjsws.
`cjsws=5.0e-10 F/m`	Source sidewall junction capacitance per unit periphery.
`cjswd=`cjswsF/m'`	Drain sidewall junction capacitance per unit periphery.
`mjsw=0.33`	Isolation-edge sidewall junction capacitance grading coefficient. Alias of mjsws.
`mjsws=0.33`	Isolation-edge sidewall source junction capacitance grading coefficient.
`mjswd=`mjsws'`	Isolation-edge sidewall drain junction capacitance grading coefficient.
`pbsw=1.0 V`	Isolation-edge sidewall junction built-in potential. Alias of pbsws.
`pbsws=1.0 V`	Isolation-edge sidewall source junction built-in potential.
`pbswd=`pbswsV'`	Isolation-edge sidewall drain junction built-in potential.
`cjswg=`cjswF/m'`	Gate-side junction capacitance per unit width. Alias of cjswgs.
`cjswgs=`cjswsF/m'`	Gate-side source junction capacitance per unit width.
`cjswgd=`cjswgsF/m'`	Gate-side source junction capacitance per unit width.
`mjswg=`mjsw'`	Gate-edge sidewall junction grading coefficient. Alias of mjswgs.
`mjswgs=`mjsws'`	Gate-edge sidewall source junction grading coefficient.
`mjswgd=`mjswgs'`	Gate-edge sidewall junction grading coefficient.
`pbswg=`pbswV'`	Gate-edge sidewall junction built-in potential. Alias of pbswgs.
`pbswgs=`pbswsV'`	Gate-edge sidewall source junction built-in potential.
`pbswgd=`pbswgsV'`	Gate-edge sidewall drain junction built-in potential.
`fcsw=0.5`	Side-wall forward-bias depletion capacitance threshold.

© 2023 Cadence Design Systems, Inc.

Temperature effects parameters

`tnom (C)`	Parameters measurement temperature. The default value is set by using the options statement.
`trise=0.0 C`	Temperature rise from ambient; alias of dtemp. It serves as the default value for instance trise.
`ute=-1.5`	Mobility temperature exponent.
`kt1=-0.11 V`	Temperature coefficient for threshold voltage.
`kt1l=0.0 V m`	Channel length dependence of the temperature coefficient for threshold voltage.
`kt2=0.022`	Body-bias coefficient of Vth temperature effect.
`ua1=1.0e-9 m/V`	Temperature coefficient for ua. When tempmod=1, units should be 1/C.
`ub1=-1.0e-18` m^2/V^2	Temperature coefficient for ub. When tempmod=1, units should be 1/C.
`uc1=-0.056 1/V (mobmod=1) / -5.6e-11` m/V^2`(modmod=0,2)`	Temperature coefficient for uc. When tempmod=1, units should be 1/C.
`ud1=0.0` $/m^2$	Temperature coefficient of ud.
`at=3.3e4 m/s`	Temperature coefficient for vsat. When tempmod=1, units should be 1/C.
`prt=0.0 Ω m`	Temperature coefficient for Rdsw. If tempmod=1, unit of the parameter is 1/C.
`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eg=1.124519231 V`	Energy band gap.
`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.
`n=1.0`	Junction emission coefficient. Alias of njs.
`njs=1.0`	Bulk-Source junction emission coefficient.
`njd=`njs'	Bulk-Drain junction emission coefficient.

© 2023 Cadence Design Systems, Inc.

`xti=3`	Saturation current temperature exponent. Alias of xtis.
`xtis=3.0`	Bulk-Source junction saturation current temperature exponent.
`xtid=`xtis'`	Bulk-Drain junction saturation current temperature exponent.
`pta=0.0 V/C`	Temperature coefficient for pb. Alias of tpb.
`tpb=0.0 V/C`	Temperature coefficient for pb.
`ptp=0.0 V/C`	Temperature coefficient for pbsw. Alias of tpbsw.
`tpbsw=0.0 V/C`	Temperature coefficient for pbsw.
`tpbswg=0.0 V/C`	Temperature coefficient for pbswg.
`cta=0.0 1/C`	Temperature coefficient for cj. Alias of tcj.
`tcj=0.0 1/C`	Temperature coefficient for cj.
`ctp=0.0 1/C`	Temperature coefficient for cjsw. Alias of tcjsw.
`tcjsw=0.0 1/C`	Temperature coefficient for cjsw.
`tcjswg=0.0 1/C`	Temperature coefficient for cjswg.
`tnfactor=0.0`	Temperature parameter for nfactor.
`teta0=0.0`	Temperature parameter for eta0.
`tvoffcv=0.0 1/C`	Temperature parameter for tvoffcv.

LOD model parameters

`saref=1.0e-6 m`	Reference distance between od edge to poly from one side.
`sbref=1.0e-6 m`	Reference distance between od edge to poly from the other side.
`sl=2.0e-6 m`	Character length along length for stress effect.
`lsl=0.0`	Length dependence of sl.
`wsl=0.0`	Width dependence of sl.
`psl=0.0`	Cross-term dependence of sl.
`sw=2.0e-6 m`	Character length along width for stress effect.

© 2023 Cadence Design Systems, Inc.

`lsw=0.0`	Length dependence of sw.
`wsw=0.0`	Width dependence of sw.
`psw=0.0`	Cross-term dependence of sw.
`sk0=0.0`	First coefficient of stress effect.
`lsk0=0.0`	Length dependence of sk0.
`wsk0=0.0`	Width dependence of sk0.
`psk0=0.0`	Cross-term dependence of sk0.
`sk1=0.0 m`	Length coefficient of stress effect.
`lsk1=0.0`	Length dependence of sk1.
`wsk1=0.0`	Width dependence of sk1.
`psk1=0.0`	Cross-term dependence of sk1.
`sk2=0.0 m`	Width coefficient of stress effect.
`lsk2=0.0`	Length dependence of sk2.
`wsk2=0.0`	Width dependence of sk2.
`psk2=0.0`	Cross-term dependence of sk2.
`k=0.0`	Ratio of velocity/mobility changes for stress.
`lk=0.0`	Length dependence of k.
`wk=0.0`	Width dependence of k.
`pk=0.0`	Cross-term dependence of k.
`wlod=0.0 m`	Length parameter for stress effect.
`ku0=0.0 m`	Mobility degradation/enhancement coefficient for stress effect.
`kvsat=0.0 m`	Saturation velocity degradation/enhancement parameter for stress effect.
`tku0=0.0`	Temperature coefficient of ku0.
`llodku0=0.0`	Length parameter for u0 stress effect.
`wlodku0=0.0`	Width parameter for u0 stress effect.
`kvth0=0.0 V m`	Threshold shift parameter for stress effect.
`llodvth=0.0`	Length parameter for vth stress effect.

© 2023 Cadence Design Systems, Inc.

`wlodvth=0.0`	Width parameter for vth stress effect.
`stk2=0.0 m`	k2 shift factor related to vth0 change.
`lodk2=1.0`	k2 shift modification factor for stress effect.
`steta0=0.0 m`	eta0 shift factor related to vth0 change.
`lodeta0=1.0`	eta0 shift modification factor for stress effect.

WPE model parameters

`web=0.0`	Coefficient for SCB.
`wec=0.0`	Coefficient for SCC.
`kvth0we=0.0 V`	Threshold shift factor for well proximity effect.
`k2we=0.0`	k2 shift factor for well proximity effect.
`ku0we=0.0`	Mobility degradation factor for well proximity effect.
`scref=1.0e-6 m`	Reference distance to calculate SCA, SCB, and SCC.

Noise model parameters

`noia=6.25e41(nmos) / 6.188e40(pmos) s^(1-EF)/(eV m^2)`	Flicker noise parameter A.
`noib=3.125e26(nmos) / 1.5e25(pmos) s^(1-EF)/eV`	Flicker noise parameter B.
`noic=8.75e9 s^(1-EF) m^2/eV`	Flicker noise parameter C.
`em=4.1e7 V/m`	Saturation field.
`af=1.0`	Flicker noise exponent.
`ef=1.0`	Flicker noise frequency exponent.
`kf=0.0 A^(2-EF) s^(1-EF) F`	Flicker noise coefficient.
`lintnoi=0.0 m`	Lint offset for noise calculation.

© 2023 Cadence Design Systems, Inc.

`wnoi=1.0e-5 m`	Channel width at which noise parameters were extracted.
`ntnoi=1.0`	Noise factor for short-channel devices for TNOIMOD=0 only.
`tnoia=1.5`	Coefficient of channel-length dependence of total channel thermal noise.
`tnoib=3.5`	Coefficient of channel-length dependence of total channel thermal noise.
`tnoic=0.0`	Thermal noise parameter.
`rnoia=0.577`	Thermal noise coefficient.
`rnoib=0.5164`	Thermal noise coefficient.
`rnoic=0.395`	Thermal noise coefficient.
`gidlclamp=-1e-5 V`	gidl clamp value.

Substrate Network parameters

`xrcrg1=12.0`	Parameter for distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models.
`xrcrg2=1.0`	Parameter to account for the excess channel diffusion resistance for both intrinsic-input resistance and charge-deficit NQS models.
`rbpb=50.0 Ω`	Resistance connected between bNode' and bNode.
`rbpbx0=100.0 Ω`	Body resistance RBPBX scaling.
`rbpbxl=0.0`	Body resistance RBPBX L scaling.
`rbpbxw=0.0`	Body resistance RBPBX W scaling.
`rbpbxnf=0.0`	Body resistance RBPBX NF scaling.
`rbpby0=100.0 Ω`	Body resistance RBPBY scaling.
`rbpbyl=0.0`	Body resistance RBPBY L scaling.
`rbpbyw=0.0`	Body resistance RBPBY W scaling.
`rbpbynf=0.0`	Body resistance RBPBY NF scaling.
`rbpd=50.0 Ω`	Resistance connected between bNode' and dbNode.
`rbpd0=50.0 Ω`	Body resistance RBPD scaling.

© 2023 Cadence Design Systems, Inc.

`rbpdl=0.0`	Body resistance RBPD L scaling.
`rbpdw=0.0`	Body resistance RBPD W scaling.
`rbpdnf=0.0`	Body resistance RBPD NF scaling.
`rbps=50.0` Ω	Resistance connected between bNode' and sbNode.
`rbps0=50.0` Ω	Body resistance RBPS scaling.
`rbpsl=0.0`	Body resistance RBPS L scaling.
`rbpsw=0.0`	Body resistance RBPS W scaling.
`rbpsnf=0.0`	Body resistance RBPS NF scaling.
`rbdb=50.0` Ω	Resistance connected between dbNode and bNode.
`rbsb=50.0` Ω	Resistance connected between sbNode and bNode.
`rbsbx0=100.0` Ω	Body resistance RBSBX scaling.
`rbsby0=100.0` Ω	Body resistance RBSBY scaling.
`rbdbx0=100.0` Ω	Body resistance RBDBX scaling.
`rbdby0=100.0` Ω	Body resistance RBDBY scaling.
`rbsdbxl=0.0`	Body resistance RBSDBX L scaling.
`rbsdbxw=0.0`	Body resistance RBSDBX W scaling.
`rbsdbxnf=0.0`	Body resistance RBSDBX NF scaling.
`rbsdbyl=0.0`	Body resistance RBSDBY L scaling.
`rbsdbyw=0.0`	Body resistance RBSDBY W scaling.
`rbsdbynf=0.0`	Body resistance RBSDBY NF scaling.
`gbmin=1.0e-12` 1/Ω	Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to an unreasonably large substrate resistance.

Default for instance parameters

`w=5e-6 m`	Default channel width.
`l=5e-6 m`	Default channel length.

© 2023 Cadence Design Systems, Inc.

as (m^2)	Default area of source diffusion.
ad (m^2)	Default area of drain diffusion.
ps (m)	Default perimeter of source diffusion.
pd (m)	Default perimeter of drain diffusion.
nrd	Default number of squares of drain diffusion.
nrs	Default number of squares of source diffusion.
rdc=0.0 Ω	Default drain contact resistance.
rsc=0.0 Ω	Default source contact resistance.

Auto Model Selector parameters

wmax=1.0 m	Maximum channel width for which the model is valid.
wmin=0.0 m	Minimum channel width for which the model is valid.
lmax=1.0 m	Maximum channel length for which the model is valid.
lmin=0.0 m	Minimum channel length for which the model is valid.

Operating region warning control parameters

alarm=none	Forbidden operating region. Possible values are none, off, triode, sat, subth, and rev.
imax=1.0 A	Maximum allowable junction current.
jmax=1.0e8 A/m^2	Maximum allowable junction current density.
bvj=infinity V	Voltage at which junction breakdown warning is issued.
vbox=3e9 toxe V	Oxide breakdown voltage.
warn=on	Parameter to turn warnings on and off. Possible values are off and on.

© 2023 Cadence Design Systems, Inc.

Safe Operating Areas Parameters

`vds_max=infinity V`	Maximum allowed voltage across source and drain.
`vgd_max=infinity V`	Maximum allowed voltage across drain and gate.
`vgs_max=infinity V`	Maximum allowed voltage across source/bulk and gate.
`vbd_max=infinity V`	Maximum allowed voltage across drain/source and bulk.
`vbs_max=vbd_max V`	Maximum allowed voltage across source and bulk.
`vgb_max=vgs_max V`	Maximum allowed voltage across gate and bulk.
`vgdr_max=vgd_max V`	Maximum allowed reverse voltage across gate and drain.
`vgsr_max=vgs_max V`	Maximum allowed reverse voltage across gate and source.
`vgbr_max=vgb_max V`	Maximum allowed reverse voltage across gate and bulk.
`vbsr_max=vbs_max V`	Maximum allowed reverse voltage across bulk and source.
`vbdr_max=vbd_max V`	Maximum allowed reverse voltage across bulk and drain.

Length dependent parameters

`lvtho=0.0 V`	Length dependence of vtho.
`lvth0`	Length dependence of vth0.
`lvfb=0.0`	Length dependence of vfb.

© 2023 Cadence Design Systems, Inc.

`lk1=0.0 V`	Length dependence of k1.
`lk2=0.0`	Length dependence of k2.
`lk3=0.0`	Length dependence of k3.
`lk3b=0.0 1/V`	Length dependence of k3b.
`lw0=0.0 m`	Length dependence of w0.
`lgamma1=0.0 V`	Length dependence of gamma1.
`lgamma2=0.0 V`	Length dependence of gamma2.
`lvbx=0.0 V`	Length dependence of vbx.
`lvbm=0.0 V`	Length dependence of vbm.
`ldvt0=0.0`	Length dependence of dvt0.
`ldvt1=0.0`	Length dependence of dvt1.
`ldvt2=0.0 1/V`	Length dependence of dvt2.
`ldvt0w=0.0`	Length dependence of dvt0w.
`ldvt1w=0.0`	Length dependence of dvt1w.
`ldvt2w=0.0`	Length dependence of dvt2w.
`la0=0.0`	Length dependence of a0.
`lb0=0.0 m`	Length dependence of b0.
`lb1=0.0 m`	Length dependence of b1.
`la1=0.0`	Length dependence of a1.
`la2=0.0`	Length dependence of a2.
`lags=0.0 F/m`^{2} `V`	Length dependence of ags.
`lketa=0.0 1/V`	Length dependence of keta.
`lnsub=0.0 cm`$^{-3}$	Length dependence of nsub.
`lngate=0.0 cm`$^{-3}$	Length dependence of ngate.
`lxj=0.0 m`	Length dependence of xj.
`ldwg=0.0 m/V`	Length dependence of dwg.
`ldwb=0.0 m/V`	Length dependence of dwb.
`lxt=0.0 m`	Length dependence of xt.
`lrdsw=0.0` Ω µm	Length dependence of rdsw.

© 2023 Cadence Design Systems, Inc.

`lprwb=0.0 1/V`	Length dependence of prwb.
`lprwg=0.0 1/V`	Length dependence of prwg.
`lwr=0.0`	Length dependence of wr.
`lu0=0.0`	Length dependence of u0.
`lvsat=0.0 m/s`	Length dependence of vsat.
`lua=0.0 m/V`	Length dependence of ua.
`lub=0.0` m^2/V^2	Length dependence of ub.
`luc=0.0` m/V^2	Length dependence of uc.
`lud=0.0` $/m^2$	Length dependence of ud.
`lup=0.0`	Length dependence of up.
`llp=0.0 m`	Length dependence of lp.
`ldrout=0.0`	Length dependence of drout.
`lpclm=0.0`	Length dependence of pclm.
`lpdiblc1=0.0`	Length dependence of pdiblc1.
`lpdiblc2=0.0`	Length dependence of pdiblc2.
`lpdiblcb=0.0 1/V`	Length dependence of pdiblcd.
`lpscbe1=0.0 V/m`	Length dependence of pscbe1.
`lpscbe2=0.0 m/V`	Length dependence of pscbe2.
`lpvag=0.0`	Length dependence of pvag.
`ldelta=0.0 V`	Length dependence of delta.
`lcdsc=0.0` F/m^2	Length dependence of cdsc.
`lcdscb=0.0` F/m^2 `V`	Length dependence of cdscb.
`lcdscd=0.0` F/m^2 `V`	Length dependence of cdscd.
`lnfactor=0.0`	Length dependence of nfactor.
`ltnfactor=0.0`	Length dependence of tnfactor.
`lcit=0.0 F`	Length dependence of cit.
`lvoff=0.0 V`	Length dependence of voff.
`ldsub=0.0`	Length dependence of dsub.
`leta0=0.0`	Length dependence of eta0.

© 2023 Cadence Design Systems, Inc.

`lteta0=0.0`	Length dependence of teta0.
`letab=0.0 1/V`	Length dependence of etab.
`lalpha0=0.0 m/V`	Length dependence of alpha0.
`lalpha1=0.0 m/V`	Length dependence of alpha1.
`lbeta0=0.0 1/V`	Length dependence of beta0.
`lcgsl=0.0 F/m`	Length dependence of cgsl.
`lcgdl=0.0 F/m`	Length dependence of cgdl.
`lclc=0.0 m`	Length dependence of clc.
`lcle=0.0`	Length dependence of cle.
`lcf=0.0 F/m`	Length dependence of cf.
`lvfbcv=0.0`	Length dependence of vfbcv.
`lacde=0.0`	Length dependence of acde.
`lmoin=0.0`	Length dependence of moin.
`lnoff=0.0`	Length dependence of noff.
`lvoffcv=0.0`	Length dependence of voffcv.
`ltvoffcv=0.0`	Length dependence of tvoffcv.
`lminvcv=0.0`	Length dependence of minvcv.
`lkt1=0.0 V`	Length dependence of kt1.
`lkt1l=0 V m`	Length dependence of kt1l.
`lkt2=0.0`	Length dependence of kt2.
`lat=0.0 m/s`	Length dependence of at.
`lua1=0.0 m/V`	Length dependence of ua1.
`lub1=0.0` m^2/V^2	Length dependence of ub1.
`luc1=0.0` m/V^2	Length dependence of uc1.
`lud1=0.0` $/m^2$	Length dependence of ud1.
`lprt=0.0` Ω	Length dependence of prt.
`lute=0.0`	Length dependence of ute.
`lndep=0.0`	Length dependence of ndep.
`lnsd=0.0`	Length dependence of nsd.

© 2023 Cadence Design Systems, Inc.

`lphin=0.0`	Length dependence of phin.
`llpe0=0.0`	Length dependence of lpe0.
`llpeb=0.0`	Length dependence of lpeb.
`ldvtp0=0.0`	Length dependence of dvtp0.
`ldvtp1=0.0`	Length dependence of dvtp1.
`ldvtp2=0.0`	Length dependence of dvtp2.
`ldvtp3=0.0`	Length dependence of dvtp3.
`ldvtp4=0.0`	Length dependence of dvtp4.
`ldvtp5=0.0`	Length dependence of dvtp5.
`leu=0.0`	Length dependence of eu.
`lminv=0.0`	Length dependence of minv.
`lfprout=0.0`	Length dependence of fprout.
`lpdits=0.0`	Length dependence of pdits.
`lpditsd=0.0`	Length dependence of pditsd.
`lrdw=0.0`	Length dependence of rdw.
`lrsw=0.0`	Length dependence of rsw.
`lagidl=0.0`	Length dependence of agidl.
`lbgidl=0.0`	Length dependence of bgidl.
`lcgidl=0.0`	Length dependence of cgidl.
`legidl=0.0`	Length dependence of egidl.
`lfgidl=0.0`	Length dependence of fgidl.
`lkgidl=0.0`	Length dependence of kgidl.
`lrgidl=0.0`	Length dependence of rgidl.
`lfgisl=lfgidl`	Length dependence of fgisl.
`lkgisl=lkgidl`	Length dependence of kgisl.
`lrgisl=lrgidl`	Length dependence of rgisl.
`laigbacc=0.0`	Length dependence of aigbacc.
`lbigbacc=0.0`	Length dependence of bigbacc.
`lcigbacc=0.0`	Length dependence of cigbacc.

© 2023 Cadence Design Systems, Inc.

`lnigbacc=0.0`	Length dependence of nigbacc.
`laigbinv=0.0`	Length dependence of aigbinv.
`lbigbinv=0.0`	Length dependence of bigbinv.
`lcigbinv=0.0`	Length dependence of cigbinv.
`leigbinv=0.0`	Length dependence of eigbinv.
`lnigbinv=0.0`	Length dependence of nigbinv.
`laigc=0.0`	Length dependence of aigc.
`lbigc=0.0`	Length dependence of bigc.
`lcigc=0.0`	Length dependence of cigc.
`laigsd=0.0`	Length dependence of aigsd.
`lbigsd=0.0`	Length dependence of bigsd.
`lcigsd=0.0`	Length dependence of cigsd.
`lnigc=0.0`	Length dependence of nigc.
`lpoxedge=0.0`	Length dependence of poxedge.
`lpigcd=0.0`	Length dependence of pigcd.
`lntox=0.0`	Length dependence of ntox.
`lckappas=0.0`	Length dependence of ckappas.
`lckappad=0.0`	Length dependence of ckappad.
`lxrcrg1=0.0`	Length dependence of xrcrg1.
`lxrcrg2=0.0`	Length dependence of xrcrg2.
`lvfbsdoff=0.0`	Length dependence of vfbsdoff.
`llambda=0.0`	Length dependence of lambda.
`lvtl=0.0`	Length dependence of vtl.
`lxn=0.0`	Length dependence of xn.
`lkvth0we=0.0 V`	Length dependence of kvth0we.
`lk2we=0.0`	Length dependence of k2we.
`lku0we=0.0`	Length dependence of ku0we.
`lku0=0.0 m^llodku0`	Length dependence of ku0.
`lkvth0=0.0 V m^llodku0`	

© 2023 Cadence Design Systems, Inc.

	Length dependence of kvth0.
`lucs=0.0`	Length dependence of ucs.
`lucste=0.0`	Length dependence of ucste.

Width dependent parameters

`wvtho=0.0 V`	Width dependence of vtho.
`wvth0`	Width dependence of vth0.
`wvfb=0.0`	Width dependence of vfb.
`wk1=0.0 V`	Width dependence of k1.
`wk2=0.0`	Width dependence of k2.
`wk3=0.0`	Width dependence of k3.
`wk3b=0.0 1/V`	Width dependence of k3b.
`ww0=0.0 m`	Width dependence of w0.
`wgamma1=0.0 V`	Width dependence of gamma1.
`wgamma2=0.0 V`	Width dependence of gamma2.
`wvbx=0.0 V`	Width dependence of vbx.
`wvbm=0.0 V`	Width dependence of vbm.
`wdvt0=0.0`	Width dependence of dvt0.
`wdvt1=0.0`	Width dependence of dvt1.
`wdvt2=0.0 1/V`	Width dependence of dvt2.
`wdvt0w=0.0`	Width dependence of dvt0w.
`wdvt1w=0.0`	Width dependence of dvt1w.
`wdvt2w=0.0`	Width dependence of dvt2w.
`wa0=0.0`	Width dependence of a0.
`wb0=0.0 m`	Width dependence of b0.
`wb1=0.0 m`	Width dependence of b1.
`wa1=0.0`	Width dependence of a1.
`wa2=0.0`	Width dependence of a2.

© 2023 Cadence Design Systems, Inc.

wags=0.0 F/m^2 V	Width dependence of ags.
wketa=0.0 1/V	Width dependence of keta.
wnsub=0.0 cm^{-3}	Width dependence of nsub.
wngate=0.0 cm^{-3}	Width dependence of ngate.
wxj=0.0 m	Width dependence of xj.
wdwg=0.0 m/V	Width dependence of dwg.
wdwb=0.0 m/$\sqrt{V}$	Width dependence of dwb.
wxt=0.0 m	Width dependence of xt.
wrdsw=0.0 Ω μm	Width dependence of rdsw.
wprwb=0.0 1/$\sqrt{V}$	Width dependence of prwb.
wprwg=0.0 1/V	Width dependence of prwg.
wwr=0.0	Width dependence of wr.
wu0=0.0	Width dependence of u0.
wvsat=0.0 m/s	Width dependence of vsat.
wua=0.0 m/V	Width dependence of ua.
wub=0.0 m^2/V^2	Width dependence of ub.
wuc=0.0 m/V^2	Width dependence of uc.
wud=0.0 /m^2	Width dependence of ud.
wup=0.0	Width dependence of up.
wlp=0.0 m	Width dependence of lp.
wdrout=0.0	Width dependence of drout.
wpclm=0.0	Width dependence of pclm.
wpdiblc1=0.0	Width dependence of pdiblc1.
wpdiblc2=0.0	Width dependence of pdiblc2.
wpdiblcb=0.0 1/V	Width dependence of pdiblcb.
wpscbe1=0.0 V/m	Width dependence of pscbe1.
wpscbe2=0.0 m/V	Width dependence of pscbe2.
wpvag=0.0	Width dependence of pvag.
wdelta=0.0 V	Width dependence of delta.

© 2023 Cadence Design Systems, Inc.

wcdsc=0.0 F/m^2	Width dependence of cdsc.
wcdscb=0.0 F/m^2 V	Width dependence of cdscb.
wcdscd=0.0 F/m^2 V	Width dependence of cdscd.
wnfactor=0.0	Width dependence of nfactor.
wtnfactor=0.0	Width dependence of tnfactor.
wcit=0.0 F	Width dependence of cit.
wvoff=0.0 V	Width dependence of voff.
wdsub=0.0	Width dependence of dsub.
weta0=0.0	Width dependence of eta0.
wteta0=0.0	Width dependence of teta0.
wetab=0.0 1/V	Width dependence of etab.
walpha0=0.0 m/V	Width dependence of alpha0.
walpha1=0.0 m/V	Width dependence of alpha1.
wbeta0=0.0 1/V	Width dependence of beta0.
wcgsl=0.0 F/m	Width dependence of cgsl.
wcgdl=0.0 F/m	Width dependence of cgdl.
wclc=0.0 m	Width dependence of clc.
wcle=0.0	Width dependence of cle.
wcf=0.0 F/m	Width dependence of cf.
wvfbcv=0.0	Width dependence of vfbcv.
wacde=0.0	Width dependence of acde.
wmoin=0.0	Width dependence of moin.
wnoff=0.0	Width dependence of noff.
wvoffcv=0.0	Width dependence of voffcv.
wtvoffcv=0.0	Width dependence of tvoffcv.
wminvcv=0.0	Width dependence of minvcv.
wkt1=0.0 V	Width dependence of kt1.
wkt1l=0 V m	Width dependence of kt1l.
wkt2=0.0	Width dependence of kt2.

© 2023 Cadence Design Systems, Inc.

wat=0.0 m/s	Width dependence of at.
wua1=0.0 m/V	Width dependence of ua1.
wub1=0.0 m^2/V^2	Width dependence of ub1.
wuc1=0.0 m/V^2	Width dependence of uc1.
wud1=0.0 $/m^2$	Width dependence of ud1.
wprt=0.0 Ω	Width dependence of prt.
wute=0.0	Width dependence of ute.
wndep=0.0	Width dependence of ndep.
wnsd=0.0	Width dependence of nsd.
wphin=0.0	Width dependence of phin.
wlpe0=0.0	Width dependence of lpe0.
wlpeb=0.0	Width dependence of lpeb.
wdvtp0=0.0	Width dependence of dvtp0.
wdvtp1=0.0	Width dependence of dvtp1.
wdvtp2=0.0	Width dependence of dvtp2.
wdvtp3=0.0	Width dependence of dvtp3.
wdvtp4=0.0	Width dependence of dvtp4.
wdvtp5=0.0	Width dependence of dvtp5.
weu=0.0	Width dependence of eu.
wminv=0.0	Width dependence of minv.
wfprout=0.0	Width dependence of fprout.
wpdits=0.0	Width dependence of pdits.
wpditsd=0.0	Width dependence of pditsd.
wrdw=0.0	Width dependence of rdw.
wrsw=0.0	Width dependence of rsw.
wagidl=0.0	Width dependence of agidl.
wbgidl=0.0	Width dependence of bgidl.
wcgidl=0.0	Width dependence of cgidl.
wegidl=0.0	Width dependence of egidl.

© 2023 Cadence Design Systems, Inc.

wfgidl=0.0	Width dependence of fgidl.
wkgidl=0.0	Width dependence of kgidl.
wrgidl=0.0	Width dependence of rgidl.
wfgisl=wfgidl	Width dependence of fgisl.
wkgisl=wkgidl	Width dependence of kgisl.
wrgisl=wrgidl	Width dependence of rgisl.
waigbacc=0.0	Width dependence of aigbacc.
wbigbacc=0.0	Width dependence of bigbacc.
wcigbacc=0.0	Width dependence of cigbacc.
wnigbacc=0.0	Width dependence of nigbacc.
waigbinv=0.0	Width dependence of aigbinv.
wbigbinv=0.0	Width dependence of bigbinv.
wcigbinv=0.0	Width dependence of cigbinv.
weigbinv=0.0	Width dependence of eigbinv.
wnigbinv=0.0	Width dependence of nigbinv.
waigc=0.0	Width dependence of aigc.
wbigc=0.0	Width dependence of bigc.
wcigc=0.0	Width dependence of cigc.
waigsd=0.0	Width dependence of aigsd.
wbigsd=0.0	Width dependence of bigsd.
wcigsd=0.0	Width dependence of cigsd.
wnigc=0.0	Width dependence of nigc.
wpoxedge=0.0	Width dependence of poxedge.
wpigcd=0.0	Width dependence of pigcd.
wntox=0.0	Width dependence of ntox.
wckappas=0.0	Width dependence of ckappas.
wckappad=0.0	Width dependence of ckappad.
wxrcrg1=0.0	Width dependence of xrcrg1.
wxrcrg2=0.0	Width dependence of xrcrg2.

© 2023 Cadence Design Systems, Inc.

`wvfbsdoff=0.0`	Width dependence of vfbsdoff.
`wlambda=0.0`	Width dependence of lambda.
`wvtl=0.0`	Width dependence of vtl.
`wxn=0.0`	Width dependence of xn.
`wkvth0we=0.0 V`	Width dependence of kvth0we.
`wk2we=0.0`	Width dependence of k2we.
`wku0we=0.0`	Width dependence of ku0we.
`wku0=0.0 m^wlodku0`	Width dependence of ku0.
`wkvth0=0.0 V m^wlodku0`	Width dependence of kvth0.
`wucs=0.0`	Width dependence of ucs.
`wucste=0.0`	Width dependence of ucste.

Cross-term dependent parameters

`pvtho=0.0 V`	Cross-term dependence of vtho.
`pvth0`	Cross-term dependence of vth0.
`pvfb=0.0`	Cross-term dependence of vfb.
`pk1=0.0 V`	Cross-term dependence of k1.
`pk2=0.0`	Cross-term dependence of k2.
`pk3=0.0`	Cross-term dependence of k3.
`pk3b=0.0 1/V`	Cross-term dependence of k3b.
`pw0=0.0 m`	Cross-term dependence of w0.
`pgamma1=0.0 V`	Cross-term dependence of gamma1.
`pgamma2=0.0 V`	Cross-term dependence of gamma2.
`pvbx=0.0 V`	Cross-term dependence of vbx.
`pvbm=0.0 V`	Cross-term dependence of vbm.
`pdvt0=0.0`	Cross-term dependence of dvt0.
`pdvt1=0.0`	Cross-term dependence of dvt1.

© 2023 Cadence Design Systems, Inc.

pdvt2=0.0 1/V	Cross-term dependence of dvt2.
pdvt0w=0.0	Cross-term dependence of dvt0w.
pdvt1w=0.0	Cross-term dependence of dvt1w.
pdvt2w=0.0	Cross-term dependence of dvt2w.
pa0=0.0	Cross-term dependence of a0.
pb0=0.0 m	Cross-term dependence of b0.
pb1=0.0 m	Cross-term dependence of b1.
pa1=0.0	Cross-term dependence of a1.
pa2=0.0	Cross-term dependence of a2.
pags=0.0 F/m^2 V	Cross-term dependence of ags.
pketa=0.0 1/V	Cross-term dependence of keta.
pnsub=0.0 cm^{-3}	Cross-term dependence of nsub.
pngate=0.0 cm^{-3}	Cross-term dependence of ngate.
pxj=0.0 m	Cross-term dependence of xj.
pdwg=0.0 m/V	Cross-term dependence of dwg.
pdwb=0.0 m/|V	Cross-term dependence of dwb.
pxt=0.0 m	Cross-term dependence of xt.
prdsw=0.0 Ω μm	Cross-term dependence of rdsw.
pprwb=0.0 1/|V	Cross-term dependence of prwb.
pprwg=0.0 1/V	Cross-term dependence of prwg.
pwr=0.0	Cross-term dependence of wr.
pu0=0.0	Cross-term dependence of u0.
pvsat=0.0 m/s	Cross-term dependence of vsat.
pua=0.0 m/V	Cross-term dependence of ua.
pub=0.0 m^2/V^2	Cross-term dependence of ub.
puc=0.0 m/V^2	Cross-term dependence of uc.
pud=0.0 $/m^2$	Cross-term dependence of ud.
pup=0.0	Cross-term dependence of up.
plp=0.0 m	Cross-term dependence of lp.

© 2023 Cadence Design Systems, Inc.

`pdrout=0.0`	Cross-term dependence of drout.
`ppclm=0.0`	Cross-term dependence of pclm.
`ppdiblc1=0.0`	Cross-term dependence of pdiblc1.
`ppdiblc2=0.0`	Cross-term dependence of pdiblc2.
`ppdiblcb=0.0 1/V`	Cross-term dependence of pdiblcd.
`ppscbe1=0.0 V/m`	Cross-term dependence of pscbe1.
`ppscbe2=0.0 m/V`	Cross-term dependence of pscbe2.
`ppvag=0.0`	Cross-term dependence of pvag.
`pdelta=0.0 V`	Cross-term dependence of delta.
`pcdsc=0.0 F/m`^{2}	Cross-term dependence of cdsc.
`pcdscb=0.0 F/m`^{2} `V`	Cross-term dependence of cdscb.
`pcdscd=0.0 F/m`^{2} `V`	Cross-term dependence of cdscd.
`pnfactor=0.0`	Cross-term dependence of nfactor.
`ptnfactor=0.0`	Cross-term dependence of tnfactor.
`pcit=0.0 F`	Cross-term dependence of cit.
`pvoff=0.0 V`	Cross-term dependence of voff.
`pdsub=0.0`	Cross-term dependence of dsub.
`peta0=0.0`	Cross-term dependence of eta0.
`pteta0=0.0`	Cross-term dependence of teta0.
`petab=0.0 1/V`	Cross-term dependence of etab.
`palpha0=0.0 m/V`	Cross-term dependence of alpha0.
`palpha1=0.0 m/V`	Cross-term dependence of alpha1.
`pbeta0=0.0 1/V`	Cross-term dependence of beta0.
`pcgsl=0.0 F/m`	Cross-term dependence of cgsl.
`pcgdl=0.0 F/m`	Cross-term dependence of cgdl.
`pclc=0.0 m`	Cross-term dependence of clc.
`pcle=0.0`	Cross-term dependence of cle.
`pcf=0.0 F/m`	Cross-term dependence of cf.
`pvfbcv=0.0`	Cross-term dependence of vfbcv.

© 2023 Cadence Design Systems, Inc.

`pacde=0.0`	Cross-term dependence of acde.
`pmoin=0.0`	Cross-term dependence of moin.
`pnoff=0.0`	Cross-term dependence of noff.
`pvoffcv=0.0`	Cross-term dependence of voffcv.
`ptvoffcv=0.0`	Cross-term dependence of tvoffcv.
`pminvcv=0.0`	Cross-term dependence of minvcv.
`pkt1=0.0 V`	Cross-term dependence of kt1.
`pkt1l=0 V m`	Cross-term dependence of kt1l.
`pkt2=0.0`	Cross-term dependence of kt2.
`pat=0.0 m/s`	Cross-term dependence of at.
`pua1=0.0 m/V`	Cross-term dependence of ua1.
`pub1=0.0` m^2/V^2	Cross-term dependence of ub1.
`puc1=0.0` m/V^2	Cross-term dependence of uc1.
`pud1=0.0` $/m^2$	Cross-term dependence of ud1.
`pprt=0.0` Ω	Cross-term dependence of prt.
`pute=0.0`	Cross-term dependence of ute.
`pndep=0.0`	Cross-term dependence of ndep.
`pnsd=0.0`	Cross-term dependence of nsd.
`pphin=0.0`	Cross-term dependence of phin.
`plpe0=0.0`	Cross-term dependence of lpe0.
`plpeb=0.0`	Cross-term dependence of lpeb.
`pdvtp0=0.0`	Cross-term dependence of dvtp0.
`pdvtp1=0.0`	Cross-term dependence of dvtp1.
`pdvtp2=0.0`	Cross-term dependence of dvtp2.
`pdvtp3=0.0`	Cross-term dependence of dvtp3.
`pdvtp4=0.0`	Cross-term dependence of dvtp4.
`pdvtp5=0.0`	Cross-term dependence of dvtp5.
`peu=0.0`	Cross-term dependence of eu.
`pminv=0.0`	Cross-term dependence of minv.

© 2023 Cadence Design Systems, Inc.

pfprout=0.0	Cross-term dependence of fprout.
ppdits=0.0	Cross-term dependence of pdits.
ppditsd=0.0	Cross-term dependence of pditsd.
prdw=0.0	Cross-term dependence of rdw.
prsw=0.0	Cross-term dependence of rsw.
pagidl=0.0	Cross-term dependence of agidl.
pbgidl=0.0	Cross-term dependence of bgidl.
pcgidl=0.0	Cross-term dependence of cgidl.
pegidl=0.0	Cross-term dependence of egidl.
pfgidl=0.0	Cross-term dependence of fgidl.
pkgidl=0.0	Cross-term dependence of kgidl.
prgidl=0.0	Cross-term dependence of rgidl.
pfgisl=pfgidl	Cross-term dependence of fgisl.
pkgisl=pkgidl	Cross-term dependence of kgisl.
prgisl=prgidl	Cross-term dependence of rgisl.
paigbacc=0.0	Cross-term dependence of aigbacc.
pbigbacc=0.0	Cross-term dependence of bigbacc.
pcigbacc=0.0	Cross-term dependence of cigbacc.
pnigbacc=0.0	Cross-term dependence of nigbacc.
paigbinv=0.0	Cross-term dependence of aigbinv.
pbigbinv=0.0	Cross-term dependence of bigbinv.
pcigbinv=0.0	Cross-term dependence of cigbinv.
peigbinv=0.0	Cross-term dependence of eigbinv.
pnigbinv=0.0	Cross-term dependence of nigbinv.
paigc=0.0	Cross-term dependence of aigc.
pbigc=0.0	Cross-term dependence of bigc.
pcigc=0.0	Cross-term dependence of cigc.
paigsd=0.0	Cross-term dependence of aigsd.
pbigsd=0.0	Cross-term dependence of bigsd.

© 2023 Cadence Design Systems, Inc.

`pcigsd=0.0`	Cross-term dependence of cigsd.
`pnigc=0.0`	Cross-term dependence of nigc.
`ppoxedge=0.0`	Cross-term dependence of poxedge.
`ppigcd=0.0`	Cross-term dependence of pigcd.
`pntox=0.0`	Cross-term dependence of ntox.
`pckappas=0.0`	Cross-term dependence of ckappas.
`pckappad=0.0`	Cross-term dependence of ckappad.
`pxrcrg1=0.0`	Cross-term dependence of xrcrg1.
`pxrcrg2=0.0`	Cross-term dependence of xrcrg2.
`pvfbsdoff=0.0`	Cross-term dependence of Vfbsdoff.
`plambda=0.0`	Cross-term dependence of lambda.
`pvtl=0.0`	Cross-term dependence of vtl.
`pxn=0.0`	Cross-term dependence of xn.
`pkvth0we=0.0 V`	Cross-term dependence of kvth0we.
`pk2we=0.0`	Cross-term dependence of k2we.
`pku0we=0.0`	Cross-term dependence of ku0we.
`pku0=0.0 m^(llodku0+wlodku0)`	Cross-term dependence of ku0.
`pkvth0=0.0 V m^(llodku0+wlodku0)`	Cross-term dependence of kvth0.
`pucs=0.0`	Cross-term dependence of ucs.
`pucste=0.0`	Cross-term dependence of ucste.

DC-mismatch dependent parameters

`mvtwl=0.0 V m`	Threshold mismatch area dependence.
`mvtwl2=0.0 V m^1.5`	Threshold mismatch area square dependence.
`mvt0=0.0 V`	Threshold mismatch intercept.

© 2023 Cadence Design Systems, Inc.

`mbewl=0.0 m`	Beta mismatch area dependence.
`mbe0=0.0`	Beta mismatch intercept.
`mismatchmod=0`	Select mismatch mode.
`mismatchdist=0 m`	Mismatch distance.

Compatibility model parameters

`compatible=spectre`	Make device equations to be compatible with a foreign simulator. This option does not affect the input syntax. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, `tispice`, and `pspice`.

Shrink Parameters

`shrink=0`	Linear shrink parameter.
`shrink2=0`	Area shrink parameter.
`maxvdd=0.0 V`	max Vdd for the model.

Imax and Imelt

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below `imax` or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and a warning is printed out.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, the base and collector currents are composed of many exponential terms, a warning will be issued and the results become inaccurate. The junction current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

Both of these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

© 2023 Cadence Design Systems, Inc.

In BSIM4, `imax` (`jmax`) will take effect only when `diomod=3` (Spectre common diode model). Berkeley uses other model parameters, such as `ijthsfwd`, `ijthdfwd` to do limitation. For more information, see the Berkeley BSIM4 manual.

Auto Model Selection

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin` should be given. The selection criteria to choose a model is as follows:

```
lmin <= inst_length < lmax  and   wmin <= inst_width  < wmax
```

Example:

```
model ModelName ModelType {
   1:     <model parameters> lmin=2 lmax=4 wmin=1 wmax=2
   2:     <model parameters> lmin=1 lmax=2 wmin=2 wmax=4
   3:     <model parameters> lmin=2 lmax=4 wmin=4 wmax=6
}
```

Then for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

© 2023 Cadence Design Systems, Inc.

Inst Default to Model

In BSIM4, for customer convenience, some model parameters are added to serve as default values for the corresponding instance parameters (they are not Berkeley model parameters. These include: `l`, `w`, `as`, `ad`, `ps`, `pd`, `nrs`, `nrd`, `rdc`, `rsc`, `rgeomod`, `nf`, `min`, and `trise`.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`weff (m)`	Effective channel width (alias=lx62).
`leff (m)`	Effective channel length (alias=lx63).
`weffcv (m)`	Effective channel width for CV (alias=lx64).
`leffcv (m)`	Effective channel length for CV (alias=lx65).
`vfbsd (V)`	Flat band Voltage between the gate and Drain/source diffusions (alias=lx75).
`rgbi (Ω)`	Gate bias-independent resistance.
`adeff (m^2)`	Effective drain area.
`aseff (m^2)`	Effective source area.
`pdeff (m)`	Effective drain perimeter.
`pseff (m)`	Effective source perimeter.

Operating-Point Parameters

`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trise (C)`	Temperature rise from ambient.
`dtemp (C)`	Alias for `trise`.
`reversed`	Reverse mode indicator. Possible values are `yes` and `no`.
`ids (A)`	Resistive drain-to-source current. Refer to equations 22-16 and 22-43.

© 2023 Cadence Design Systems, Inc.

`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`vbs (V)`	Bulk-source voltage.
`vgd (V)`	Gate-drain voltage.
`vdb (V)`	Drain-bulk voltage.
`vgb (V)`	Gate-bulk voltage.
`vth (V)`	Threshold voltage (alias=lv9). Refer to equation 22-14.
`vdsat (V)`	Drain-source saturation voltage (alias=lv10). Refer to equations 22-37 and 22-38.
`gm (S)`	Common-source transconductance (alias=lx7). Refer to equation 13-32.
`gds (S)`	Common-source output conductance (alias=lx8). Refer to equation 13-31.
`gmbs (S)`	Body-transconductance (alias=lx9). Refer to equation 13-33.
`betaeff (A/V`^{2}`)`	Effective beta (alias LV21).
`pro_Gamma`	Gamma.
`cjd (F)`	Drain-bulk junction capacitance (alias=lx29). Refer to equations 22-171 and 22-172.
`cjs (F)`	Source-bulk junction capacitance (alias=lx28). Refer to equations 22-164 and 22-165.
`cgg (F)`	Total gate capacitance, including intrinsic, overlap and fringing components (alias=lx82). Refer to equations 22-120, 22-126, 22-127, and 22-128.
`cgd (F)`	Total gate-to-drain capacitance, including intrinsic, overlap, and fringing components (alias=lx83). Refer to equations 22-122, 22-126, 22-127, and 22-128.
`cgs (F)`	Total gate-to-source capacitance, including intrinsic, overlap, and fringing components (alias=lx84). Refer to equations 22-121, 22-126, 22-127, and 22-128.
`cgb (F)`	Total gate-to-bulk capacitance, including intrinsic and overlap components. Refer to equations 22-123, 22-126, 22-127, and 22-128.

© 2023 Cadence Design Systems, Inc.

`cdg (F)`	Total drain-to-gate capacitance, including intrinsic, overlap, and fringing components (alias=lx87). Refer to equations 22-120, 22-126, 22-127, and 22-128.
`cdd (F)`	Drain capacitance, including intrinsic, overlap, and fringing components. Refer to equations 22-122, 22-126, 22-127, and 22-128.
`cds (F)`	Total drain-to-source capacitance (alias=lx86). Refer to equations 22-121, 22-126, 22-127, and 22-128.
`cdb (F)`	Intrinsic drain-to-bulk capacitance. Refer to equation 22-123.
`csg (F)`	Total source-to-gate capacitance, including intrinsic, overlap, and fringing components. Refer to equations 22-120, 22-126, 22-127, and 22-128.
`csd (F)`	Total source-to-drain capacitance. Refer to equations 22-122, 22-126, 22-127, and 22-128.
`css (F)`	Source capacitance, including intrinsic, overlap, and fringing components. Refer to equations 22-121, 22-126, 22-127, and 22-128.
`csb (F)`	Intrinsic source-to-bulk capacitance. Refer to equation 22-123.
`cbg (F)`	Total bulk-to-gate capacitance, including intrinsic and overlap components (alias=lx88). Refer to equations 22-120, 22-126, 22-127, and 22-128.
`cbd (F)`	Intrinsic bulk-to-drain capacitance. Refer to equation 22-122.
`cbs (F)`	Intrinsic bulk-to-source capacitance. Refer to equation 22-121.
`cbb (F)`	Bulk capacitance, including intrinsic and overlap components. Refer to equations 22-123, 22-126, 22-127, and 22-128.
`covlgs (F/m)`	Gate-source overlap and fringing capacitances (alias=lv36). Refer to equations 22-124 and 22-127
`covlgd (F/m)`	Gate-drain overlap and fringing capacitances (alias=lv37). Refer to equations 22-125 and 22-128.
`covlgb (F/m)`	Gate-bulk overlap capacitances (alias=lv38). Refer to equation 22-126.

© 2023 Cadence Design Systems, Inc.

cggbo (F)	CGGBO = dQg/dVg intrinsic gate capacitance (alias=lx18). Refer to equation 22-120.
cgdbo (F)	CGDBO = -dQg/dVd intrinsic gate-to-drain capacitance (alias=lx19).Refer to equation 22-122.
cgsbo (F)	CGSBO = -dQg/dVs intrinsic gate-to-source capacitance (alias=lx20). Refer to equation 22-122.
cbgbo (F)	CBGBO = -dQb/dVg intrinsic bulk-to-gate capacitance (alias=lx21). Refer to equation 22-120.
cbdbo (F)	CBDBO = -dQb/dVd intrinsic bulk-to-drain capacitance (alias=lx22). Refer to equation 22-122.
cbsbo (F)	CBSBO = -dQb/dVs intrinsic bulk-to-source capacitance (alias=lx23). Refer to equation 22-121.
cdgbo (F)	CDGBO = -dQd/dVg intrinsic drain-to-gate capacitance (alias=lx32). Refer to equation 22-120.
cddbo (F)	CDDBO = dQd/dVd intrinsic drain capacitance (alias=lx33). Refer to equation 22-122.
cdsbo (F)	CDSBO = -dQd/dVs intrinsic drain-to-source capacitance (alias=lx34). Refer to equation 22-121.
ron (Ω)	On-resistance. Includes the parasitical rs and rd.
id (A)	Resistive drain current. The sum of the currents though D and DI node.
ig (A)	Total DC gate current.
is (A)	Total DC source current.
ib (A)	Total DC bulk current.
ibulk (A)	Resistive bulk current. The sum of the currents though B, BI, SB, and DB node.
pwr (W)	Power at op point. pwr = abs(ids * vds) + abs(ibulk * vbs).
gmoverid (1/V)	Gm/Ids.
ueff	ueff.
rdeff (Ω)	Effective drain resistance. Refer to equation 22-36.
rseff (Ω)	Effective source resistance. rseff = Rs,bias-dep + nrs * rsh + rsc/ nf. Rs, bias-dep. Refer to equation 22-36.
rgbd (Ω)	Gate bias-dependent resistance. Refer to equation 22-137.

© 2023 Cadence Design Systems, Inc.

`igidl (A)`	Gate-induced drain leakage current (alias=lx70). Refer to equation 22-55.
`igisl (A)`	Gate-induced source leakage current. Refer to equation 22-56.
`igdt (A)`	Gate Dielectric tunneling current (alias=lx71). Refer to equations 22-18, 22-19, 22-20, 22-22, and 22-23.
`igd (A)`	Gate-to-drain tunneling current (alias=lx39). Refer to equation 22-20.
`igs (A)`	Gate-to-source tunneling current (alias=lx38). Refer to equation 22-19.
`igb (A)`	Gate-to-bulk tunneling current (alias=lx66). Refer to equation 22-18.
`igbacc (A)`	Gate-to-bulk tunneling current determined by ECB (alias=lx73). Refer to equation 22-18.
`igbinv (A)`	Gate-to-bulk tunneling current determined by EVB (alias=lx74). Refer to equation 22-18.
`igcs (A)`	Gate-to-channel (source side) tunneling current (alias=lx67). Refer to equation 22-22.
`igcd (A)`	Gate-to-channel (drain side) tunneling current (alias=lx68). Refer to equation 22-23.
`isub (A)`	Substrate current (alias to LX69).
`gbs (S)`	Bulk-source diode conductance (alias=lx11).
`gbd (S)`	Bulk-drain diode conductance (alias=lx10).
`qg (Coul)`	Total gate charge, including intrinsic, overlap and fringing components.
`qd (Coul)`	Total drain charge, including intrinsic, overlap and fringing components.
`qs (Coul)`	Total source charge, including intrinsic, overlap and fringing components.
`qb (Coul)`	Total bulk charge, including intrinsic and overlap components.
`qjd (Coul)`	Drain-bulk junction charge.
`qjs (Coul)`	Source-bulk junction charge.

© 2023 Cadence Design Systems, Inc.

qgdovl (Coul)	Gate-drain overlap and fringing charge.
qgsovl (Coul)	Gate-source overlap and fringing charge.
qgi (Coul)	Intrinsic gate charge.
qdi (Coul)	Intrinsic drain charge.
qsi (Coul)	Intrinsic source charge.
qbi (Coul)	Intrinsic bulk charge.
ide (A)	Total DC drain current.
ige (A)	Total DC gate current.
ise (A)	Total DC source current.
ibe (A)	Total DC bulk current.
idb (A)	DC drain-bulk current.
isb (A)	DC source-bulk current.
vsb (V)	Source-bulk DC voltage.
gmb (S)	DC bulk transconductance.
vgt (V)	Wffective gate drive voltage including back bias and drain bias effects.
vth_drive (V)	Effective gate drive voltage including back bias and drain bias effects. Alias for Vgt
vdss (V)	Drain saturation voltage at actual bias.
vsat_marg (V)	Vds margin.
vdsat_marg (V)	Vds margin.
self_gain	Transistor self gain.
rout (Ω)	AC output resistor. The parasitical rs and rd are excluded.
beff (A/V^2)	Gain factor in saturation.
fug (Hz)	Unity current gain frequency at actual bias.
ft (Hz)	Unity current gain frequency at actual bias.
rgate (Ω)	MOS gate resistance.
vearly (V)	Equivalent early voltage.

© 2023 Cadence Design Systems, Inc.

Related Topics

BSIM4 Level-14 Model (bsim4)

Model

Model Version Update

Model Equations

Models and Equations in Version Updates

Component Statements

© 2023 Cadence Design Systems, Inc.

23

BSIM6 Model (bsim6)

BSIM6 is the new Bulk MOSFET model from the BSIM Group. The model provides excellent accuracy compared to measured data in all regions of operation. It features model symmetry valued for analog and RF applications while maintaining the strong support and performance of the BSIM model valued for all applications. The available versions for the bsim6 model are 6.00(6.0.0), 6.10(6.1.0), 6.11(6.1.1), 106.2(Bsimbulk 106.2.0), 107.0(Bsimbulk 107.0), and 107.10(Bsimbulk 107.1.0).

Note: Starting with version 106.2, BSIM6 has been renamed to BSIM-BULK. Spectre supports both master names `bsim6` and `bsimbulk`.

Related Topics

Instance

Model

Version Update and Enhancements

Model Equations

Component Statements for BSIM6

© 2023 Cadence Design Systems, Inc.

Instance

Instance Syntax

BSIM6 instance have 4 terminals. To specify BSIM6 instance element, the ModelName has to be associated with a BSIM6 model card.

```
InstanceName (d g s b) ModelName <parameter=value> ...
```

Sample Instance Statement

```
m1 (0 2 1 1) pchmod w=2u l=0.8u as=250p ad=250p pd=168p ps=168p m=1
```

Related Topics

BSIM6 Model (bsim6)

Model

Version Update and Enhancements

Model Equations

Component Statements for BSIM6

Model

Model Syntax

The following syntax specifies BSIM6 model:

```
model ModelName bsim6 | bsimbulk <parameter=value> ...
```

The third parameter, bsim6, is the master to indicate this model card is a BSIM6 model card.

Note: Starting with version 106.2, bsim6 has been renamed to bsimbulk. Spectre supports both master names.

Sample Model Statements

```
model pchmod bsim6 type=p version=6.00
model pchmod bsimbulk type=p version=102.6
```


© 2023 Cadence Design Systems, Inc.

TMI Support

The bsim6 model supports the TMI model, a modeling application programming interface that supports extensions of standard compact models.

TMI provides an alternative approach to support model equations for advanced technologies in addition to adding more macro models. It provides good flexibility as macro model and good simulation efficiency as built-in standard model at the same time.

To use the TMI for bsim6 model, you need to correctly set the TMI options and parameters. For more information on TMI options and parameters, refer to the TMI documentation.

OMI Support

Starting with the SPECTRE 21.1 release, support for the OMI model has been added in the BSIM-BULK model. OMI (Open Model Interface) is CMC standard modeling application programming interface (API) that supports extensions of standard compact models.

OMI provides an alternative approach to support model equations for advanced technologies in addition to adding more macro models. It provides flexibility as a macro model and good simulation efficiency as a built-in standard model at the same time.

To use the OMI for the BSIM-BULK model, you need to correctly set the OMI options and parameters. For more information on OMI options and parameters, refer to the OMI documentation.

Related Topics

BSIM6 Model (bsim6)

Version Update and Enhancements

Model Equations

Component Statements for BSIM6

Model Parameters

Instance Parameters

© 2023 Cadence Design Systems, Inc.

Version Update and Enhancements

Version 107 Enhancements

The following enhancements have been made in version 107:

- Kink due to large `PSATB` values.
- Enhanced Gm/Id tuning flexibility in weak inversion region.
- Flexibility of tuning `Cgg` in strong inversion for $Vds \neq 0$.
- Fixed negative `Cbg` issue for `CVMOD=0`.
- Flexibility of tuning `Cgg` in accumulation.
- Added temperature dependence for the parameter `EU`.
- Changed the default value of the parameter `LH`.
- Valid condition for `L <= LH`.
- Warning message for `FNOIMOD=1`.
- Enhanced BSIMBULK flicker noise tuning flexibility.
- Evaluation of `K2_EDGE` and `ETA0_EDGE` independent of STI stress model.
- Device type implementation in sub-surface leakage model.
- Corrected abnormal flicker noise performance when `EDGEFET=1`.
- Aligned BSIMBULK 1/f behavior with BSIM4 1/f behavior.
- Corrected implementation of sub-surface leakage model.
- Enhanced the tuning flexibility in the flicker noise model.
- Added flicker noise due to `EDGEFET`.
- Fixed discrepancy in thermal noise model.
- There will be no impact of non-zero C0 on thermal noise.
- Fixed issue caused during PSS simulation. `Esatnoi` and `Nt` parameters will be set before they are used.
- Implementation of ABULK is updated.
- `phib` and `gam` are replaced by `phibCV` and `gamCV` respectively in `CVMOD=1`.

© 2023 Cadence Design Systems, Inc.

- NDEPEDGE and its binning.
- Fixed node collapsing and updated minimum value of Rdrain/Rsource.
- GDS Op-pt definition.
- Incorrect IGBBACC behavior in the accumulation region.
- Enhancement for High Voltage modeling.
- Warning message for $U0 \leq 0$.
- Range of model parameters.
- Default value of NDEPEDGE.
- Kink in DC current due to PSATB.
- Rollback MNUD and MNUD1 from thermal noise model.
- Addressed IGBACC issue.
- Added GMIN across D-B and S-B junctions.
- Missing type in sub-surface leakage model.
- External/internal node issue in sub-surface leakage model.
- HVMOD issue- CV model.
- Secondary impact ionization in HVMOD.
- Implemented sigvds in flicker_noise.

Version 106.2 Enhancements

The following enhancements have been made in version 106.2:

- Removed all the ifdef statements from the code.
- Node collapsing has been done for the nodes t and N1 for SHMOD = 0 and TNOIMOD = 0.
- Every IF and else statement starts with begin and ends with the end statement.
- Modified the name of the parameter MULUO to MULU0.
- Name of the Variable T13 has modified to Weff_SH in the code.

© 2023 Cadence Design Systems, Inc.

- Modified Flicker noise model which can also model the flicker noise trends for Halo transistors.
- MNUD model to increase flexibility in IDS – VDS fitting.
- Improved Gamma behavior in the linear Region for `TNOIMOD = 1`.
- Modified Thermal noise model to tune NF50 in Subthreshold region and to achieve ideal trend of gamma for long channel transistors.
- Clamping added in IGD and IGS.
- Sign correction in charge calculations.
- Added Self-Heating output variables.
- Deactivated node `T` when `RTH0` or `SHMOD` or both are zero.
- Used `SRCFLAG` as the formal argument of `BSIM6RdsEndSha` and `BSIM6RdseffGeo` in place of `TYPE`.
- Modified Calculations of Geometry-dependent source/drain resistance.
- Added devsign in Operating point VTH expression.
- Limit (`Weff + WTH0`) to (`Weff + WTH0`) `> 0` in Self Heating module.
- Changes made in the macros definition.
- Module name has changed from `bsim6` to `bsimbulk`.
- Absence of CLM and velocity saturation terms in Charge expressions in manual.
- Parameter `DVTP0` has Re-Defined in Manual.
- Added binning parameters in the `EDGEFET` parameters.
- Default value of `EDGEFET` parameter has changed to 0 from 1.
- Modified the expression of built in potential.
- `DTEMP`, `MULU0`, `DELVTO` and `IDS0MULT` have modified to both instance and model parameters.
- Removed all the `ifdef` statements from the code.
- Added units and descriptions for all the parameters.
- Added modified function of `VDSX` to avoid negative GDS issue.
- Removed clamping from UCR.

© 2023 Cadence Design Systems, Inc.

- Added protection to the following parameters: `LP1`, `LP2`, `NJS`, `NJD`, `XJBV S` and `XJBV D`.

Version 6.1.1 Enhancements

The following enhancements have been made in version 6.1.1:

- Threshold voltage model for operating point information has been added.
- EDGE FET model (Subthreshold hump module) has been added.
- An External Thermal node has been added
- Mobility scaling model similar to BSIM4 has been added, which is accessible through MOBSCALE=1.
- Asymmetry Mode has been added, which is accessible through Asymmetry_mode=0/1
- Parameter DELVT0 has been added for process variation.
- Well proximity effect similar to BSIM4 has been added.
- NF is multiplied with the effective width in the thermal noise model.
- Clamping of UC has been removed.

Related Topics

BSIM6 Model (bsim6)

Instance

Model

Model Equations

Component Statements for BSIM6

© 2023 Cadence Design Systems, Inc.

Model Equations

Effective Channel Length and Width

(23-1)

$$\Delta L = LINT + \frac{LL}{(L_{new})^{LLN}} + \frac{LW}{(W_{new})^{LWN}} + \frac{LWL}{(L_{new})^{LLN} \cdot (W_{new})^{LWN}}$$

(23-2)

$$\Delta W = WINT + \frac{WL}{(W_{new})^{WLN}} + \frac{WW}{(W_{new})^{WWN}} + \frac{WWL}{(L_{new})^{WLN} \cdot (W_{new})^{WWN}}$$

(23-3)

$$\Delta L_{CV} = DLC$$

(23-4)

$$\Delta W_{CV} = DWC$$

(23-5)

$$L_{eff} = L \times LMLT + XL - 2\Delta L$$

(23-6)

$$W_{eff} = W \times WMLT + XW - 2\Delta W$$

(23-7)

$$L_{eff,\,CV} = L \times LMLT + XL - 2\Delta L_{CV}$$

(23-8)

$$W_{eff,\,CV} = W \times WMLT + XW - 2\Delta W_{CV}$$

© 2023 Cadence Design Systems, Inc.

Binning Calculations

For given L and W, each model parameter $PARAM_i$ is calculated as a function of PARAM, a length dependent term, LPARAM, width dependent term, WPARAM, and area dependent term PPARAM:

(23-9)

$$PARAM_i = PARAM + \frac{LPARAM}{L_{eff}} + \frac{WPARAM}{W_{eff}} + \frac{PPARAM}{L_{eff} \cdot W_{eff}}$$

For version 106.2:

(23-10)

$$PARAM_i = PARAM + LPARAM \cdot BINL + WPARAM \cdot BINW + PPARAM \cdot BINWL$$

For the list of binnable parameters, refer to the Components Statements section.

Global Geometrical Scaling

Following scaling formulation is used in global scaling:

(23-11)

$$PARAM[L] = PARAM \cdot \left[1 + PARAML \cdot \left(\frac{1}{L_{eff}^{PARAMLEXP}} - \frac{1}{LLONG^{PARAMLEXP}} \right) \right.$$
$$+ PARAMW \cdot \left(\frac{1}{W_{eff}^{PARAMWEXP}} - \frac{1}{WWIDE^{PARAMWEXP}} \right)$$
$$\left. + PARAMWL \cdot \left(\frac{1}{(L_{eff} \cdot W_{eff})^{PARAMWLEXP}} \right) \right]$$

Terminal Voltages

(23-12)

$$V_t = \frac{K \cdot T}{q}$$

© 2023 Cadence Design Systems, Inc.

(23-13)

$$V_g = V_g - V_b$$

(23-14)

$$V_d = V_d - V_b$$

(23-15)

$$V_s = V_s - V_b$$

(23-16)

$$V_{gs} = V_g - V_s$$

(23-17)

$$V_{gd} = V_g - V_d$$

(23-18)

$$V_{gb} = V_g - V_b$$

(23-19)

$$V_{ds} = V_d - V_s$$

(23-20)

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.01} - 0.1$$

For version 106.2:

$$V_{dsx} = \left[\frac{2}{AVDSX}.ln(1 + exp^{AVDSX.V_{DS}}) - V_{DS} - \frac{2}{AVDSX}.ln(2)\right]$$

(23-21)

$$V_{bsx} = -\left[V_s + \frac{1}{2}(V_{ds} - V_{dsx})\right]$$

© 2023 Cadence Design Systems, Inc.

Pinch-Off Potential and Normalized Charge Calculation

Pinch-Off Potential with Poly Depletion

(23-22)

$$\psi_p = \begin{cases} 1 + \left[\sqrt{\upsilon_g + \upsilon_{fb} - 1 + \left(\frac{\gamma}{2}\right)^2} - \frac{\gamma}{2}\right]^2 & \text{if } \upsilon_g - \upsilon_{fb} > \phi_b + \gamma\sqrt{\phi_b} \\ 1 + e^{-\psi_{p0}}\left[\sqrt{\upsilon_g - \upsilon_{fb} - 1 + e^{-\psi_{p0}} + \left(\frac{\gamma}{2}\right)^2} - \frac{\gamma}{2}\right]^2 & \text{if } \phi_b + \gamma\sqrt{\phi_b} \geq \upsilon_g - \upsilon_{fb} \geq 0 \\ -\ln\left[1 - \psi_{p0} + \left(\frac{\upsilon_g - \upsilon_{fb} - \psi_{p0}}{\gamma}\right)^2\right] & \text{if } \upsilon_g - \upsilon_{fb} < 0 \end{cases}$$

Note: Derivatives of ψ_p are continuous in all regions.

For version 106.2:

(23-23)

$$\psi_p = \begin{cases} -\ln\left[1 - \psi_{p0} + \left(\frac{v_g - v_{fb} - \psi_{p0}}{\gamma}\right)^2\right] & \text{if } v_g - v_{fb} < 0 \\ 1 - e^{-\psi_{p0}} + \left[\sqrt{v_g - v_{fb} - 1 + e^{-\psi_{p0}} + \left(\frac{\gamma}{2}\right)^2} - \frac{\gamma}{2}\right]^2 & \text{otherwise} \end{cases}$$

Normalized Charge Density

Inversion charge: Normalized inversion charge density at source/drain is newly derived for BSIM6, and can be obtained as follows:

(23-24)

$$\ln(q_i) = \ln\left(\frac{4n_q}{\gamma_0} \cdot \sqrt{\psi_p}\right) + 2q_i = \psi_p - 2\phi_f - \upsilon_{ch}$$

For version 106.2:

(23-25)

$$\ln(q_i) + \ln\left[\frac{2n_q}{\gamma_0}\left(q_i\frac{2n_q}{\gamma_0} + 2\sqrt{\psi_p - 2q_i}\right)\right] + 2q_i = \psi_p - 2\phi_f - v_{ch}$$

© 2023 Cadence Design Systems, Inc.

Short Channel Effects

Vt roll-off, DIBL, and Subthreshold Slope Degradation

(23-26)

$$\Delta V_{th,VDNUD} = -K2 \cdot V_{bsx}$$

For version 106.2:

(23-27)

$$\Delta V_{th,VDNUD} = K1 \cdot (\sqrt{\phi_{st} - V_{bs}} - \sqrt{\phi_{st}}) - K2 \cdot V_{bsx}$$

(23-28)

$$\Delta V_{th,DIBL} = -(ETA0 + ETAB \cdot V_{bsx}) \cdot V_{dsx}$$

(23-29)

$$\Delta V_{th,DITS} = -n\frac{KT}{q} \cdot \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot (1 + \exp(-DVTP1 \cdot V_{ds}))}\right) - \left(DVTP5 + \frac{DVTP2}{L_{eff}^{DVTP3}}\right) \cdot \tanh(DVTP4 \cdot V_{dsx})$$

(23-30)

$$\Delta V_{th,all} = \Delta V_{th,VDNUD} + \Delta V_{th,DIBL} + \Delta V_{th,DITS}$$

(23-31)

$$V_{gfb} = V_g - V_{fb} - \Delta V_{th,all}$$

Note: Short channel effect and reverse short channel effect are modeled using NDEPL1, NDELEXP1, NDEPL2, and NDEPLEXP2 parameters. Width scaling of Vth is modeled using NDEPW and NDEPWEXP parameters.

Drain Saturation Voltage

The drain saturation voltage model is calculated after the source-side charge (q_s) has been calculated. V_{dseff} is subsequently used to compute the drain-side charge (q_d).

© 2023 Cadence Design Systems, Inc.

Electric Field Calculations

(23-32)

$$E_{effs} = 10^{-8} \cdot \left(\frac{qbs + \eta \cdot qis}{\varepsilon_{ratio} \cdot Toxe} \right)$$

Drain Saturation Voltage (V_{dsat}) Calculations

(23-33)

$$D_{mobs} = 1 + (UA + UC \cdot V_{bsx}) \cdot (E_{effs})^{EU} + \frac{UD}{\left[\frac{1}{2} \cdot \left(1 + \frac{q_{is}}{q_{bs}} \right) \right]^{UCS}}$$

(23-34)

$$T_0 = \begin{cases} \dfrac{1}{1 + PSATB \cdot V_{bsx}} & PSATB \geq 0 \\ 1 - PSATB \cdot V_{bsx} & PSATB < 0 \end{cases}$$

(23-35)

$$\lambda_C = \frac{2 \cdot U0 \cdot nV_t}{(D_{mobs})^{PSAT} \cdot VSAT \cdot L_{eff}} \cdot \left[1 + PTWG \cdot \frac{10 \cdot PSATX \cdot qs \cdot T0}{10 \cdot PSATX + qs \cdot T0} \right]$$

(23-36)

$$q_{dsat} = \frac{\lambda_C}{2} \cdot \frac{q_s^2 + q_s}{1 + \frac{\lambda_C}{2} \cdot (1 + q_s)}$$

(23-37)

$$\upsilon_{dsat} = \psi_p - \frac{2\phi b}{n} - 2q_{dsat} - \ln \left[\frac{2q_{dsat} \cdot n_q}{gam} \cdot \left(\frac{2q_{dsat} \cdot n_q}{gam} + \frac{gam}{n_q - 1} \right) \right]$$

(23-38)

$$V_{dsat} = \upsilon_{dsat} \cdot nV_t$$

© 2023 Cadence Design Systems, Inc.

(23-39)

$$V_{dssat} = \upsilon_{dsat} - V_s$$

Mobility Degradation with Vertical Field

(23-40)

$$D_{mob} = 1 + (UA + UC \cdot V_{bsx}) \cdot (E_{effm})^{EU} + \frac{UD}{\left[\frac{1}{2} \cdot \left(1 + \frac{q_{ia}}{q_{ba}}\right)\right]^{UCS}}$$

Parasitic Series Resistance

Bias-Dependent Internal Series Resistance ($R_{ds}(V)$)

The internal source-drain resistance (Rds(V)) option can be invoked by setting the model selector RDSMOD=0 (internal). Following are the expressions for source/drain series resistance calculation:

(23-41)

$$T_0 = 1 + PRWG \cdot q_{ia}$$

(23-42)

$$T_1 = PRWB \cdot (\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s})$$

(23-43)

$$T_2 = \frac{1}{T0} + T_1$$

(23-44)

$$T_3 = \frac{1}{2}\left[T_2 + \sqrt{T_2^2 + 0.01}\right]$$

(23-45)

$$R_{ds}(V) = NF \cdot (R_{s,geo} + R_{d,geo} + W_{eff}^{WR}\ [RDSWMIN + RDSW \cdot T3]\ )$$

For version 106.2 (RDSMOD=2):

© 2023 Cadence Design Systems, Inc.

(23-46)

$$R_{ds}(V) = R_{s,geo} + NF \cdot \left(W_{eff}^{WR} \left[RDSWMIN + RDSW \cdot T_3 \right] \right) + R_{d,geo}$$

Bias-Dependent External Series Resistance ($R_s(V)$ & ($R_d(V)$)

The bias-dependent external resistance model is adopted from BSIM4 and can be invoked by setting model selector RDSMOD=1. BSIM4 and BSIM6 allow the source 36 extension resistance Rs(V) and the drain extension resistance Rd(V) to be external and asymmetric (i.e. here when HVMOD = 1, Rs(V) is connected between nodes S and Si1 and Rd(V) is connected between nodes D and Di1). When HVMOD = 0, Si1 and Si (Di1 and Di) will be shorted. Furthermore, Rs(V) does not have to be equal to Rd(V).

This feature makes accurate RF CMOS simulation possible.

The source/drain series resistance is the sum of a bias-independent component and a bias-dependent component.

$$V_{s1} = V(si1, bi)$$
$$V_{d1} = V(di1, bi) \quad (2.181)$$
$$V_{gs1_noswap} = V_g - V_{s1} \quad (2.182)$$
$$V_{gd1_noswap} = V_g - V_{d1} \quad (2.183)$$
$$V_{sb1_noswap} = V_{s1} \quad (2.184)$$
$$V_{db1_noswap} = V_{d1} \quad (2.185)$$
$$V_{gs,eff} = \frac{1}{2}\left[V_{gs1} - V_{fbsdr} + \sqrt{(V_{gs1_noswap} - V_{fbsdr})^2 + 10^{-2}} \right] \quad (2.186)$$
$$V_{gd,eff} = \frac{1}{2}\left[V_{gd1} - V_{fbsdr} + \sqrt{(V_{gd1_noswap} - V_{fbsdr})^2 + 10^{-2}} \right] \quad (2.187)$$
$$R_{source} = \frac{1}{W_{eff}^{WR} \cdot NF} \cdot \left(RSWMIN + RSW \cdot \left[-PRWB \cdot V_{sb1_noswap} + \frac{1}{1 + PRWG_i \cdot V_{gs,eff}} \right] \right) + R_{s,geo} \quad (2.188)$$
$$R_{drain} = \frac{1}{W_{eff}^{WR} \cdot NF} \cdot \left(RDWMIN + RDW \cdot \left[-PRWB \cdot V_{db1_noswap} + \frac{1}{1 + PRWG_i \cdot V_{gd,eff}} \right] \right) + R_{d,geo} \quad (2.189)$$

$R_{s,geo}$ and $R_{d,geo}$ are the source and drain diffusion resistances.

© 2023 Cadence Design Systems, Inc.

Sheet Resistance Model

(23-47)

$$R_{s,geo} = NRS \cdot RSHS$$
$$R_{d,geo} = NRD \cdot RSHD$$

Output Conductance

Channel Length Modulation (CLM)

(23-48)

$$M_{CLM} = 1 + C_{clm} \ln\left[1 + \frac{V_{ds} - V_{dseff}}{V_{asat}} \cdot \frac{1}{C_{clm}}\right]$$

Drain Induced Barrier Lowering (DIBL)

(23-49)

$$M_{DIBL} = \left(1 + \frac{V_{ds} - Vdseff}{VAIDBL}\right)$$

Drain Induced Threshold Shift (DITS)

(23-50)

$$M_{DITS} = \left(1 + \frac{V_{ds} - Vdseff}{VADITS}\right)$$

Substrate Current Induced Body Effect (SCBE)

(23-51)

$$M_{OC} = M_{DIBL} + M_{CLM} + M_{DITS} + M_{SCBE}$$

© 2023 Cadence Design Systems, Inc.

Velocity Saturation

Current Degradation Due to Velocity Saturation

(23-52)

$$D_{tot} = D_{mob} \cdot D_{vsat} \cdot D_r$$

Effective Mobility

(23-53)

$$\mu_{eff} = \frac{U0}{D_{tot}}$$

Drain Current Model

Without Velocity Saturation

(23-54)

$$I_{DS} = 2 \cdot n_q \cdot \mu_{eff} \cdot \frac{W_{eff}}{L_{eff}} \cdot C_{ox} \cdot nV^2{}_t \cdot [(q_s - q_{deff})(q_s + q_{deff} + 1)]$$

Including Velocity Saturation

(23-55)

$$I_{DS} = 2 \cdot n_q \cdot \mu_{eff} \cdot \frac{W_{eff}}{L_{eff}} \cdot C_{ox} \cdot nV^2{}_t \cdot [(q_s - q_{deff})(q_s + q_{deff} + 1)] \cdot M_{OC}$$

Impact Ionization Model

(23-56)

$$I_{ii} = ALPHA0 \cdot (V_{ds} - V_{dseff}) \cdot \exp\left(-\frac{BETA0}{V_{ds} - Vdseff}\right) \cdot \frac{I_{ds}}{M_{SCBE}}$$

© 2023 Cadence Design Systems, Inc.

GIDL/GISL Current Model

(23-57)

$$I_{GIDL} = AGIDL \cdot W_{eff} \cdot NF \cdot \frac{V_{ds} - V_{gse} - EGIDL}{3 \cdot Toxe} \cdot \exp\left(\frac{-3 \cdot Toxe \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL}\right) \cdot \frac{V_{db}^3}{CGIDL + V_{db}^3}$$

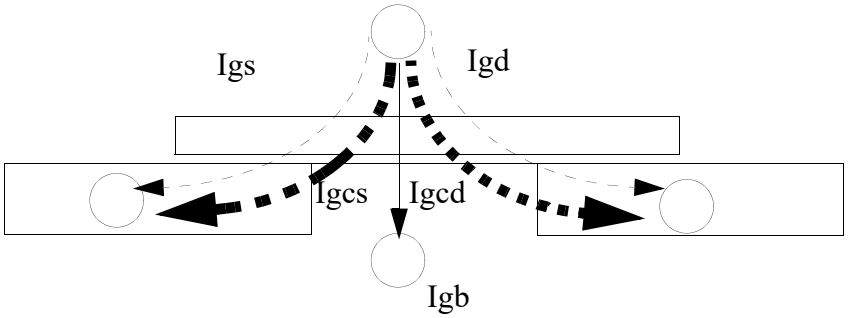
(23-58)

$$I_{GISL} = AGISL \cdot W_{eff} \cdot NF \cdot \frac{V_{ds} - V_{gde} - EGISL}{3 \cdot Toxe} \cdot \exp\left(\frac{-3 \cdot Toxe \cdot BGISL}{V_{ds} - V_{gde} - EGISL}\right) \cdot \frac{V_{sb}^3}{CGISL + V_{sb}^3}$$

I_{GIDL}/I_{GISL} can be switched off by setting GIDLMOD=0

Gate Tunneling Current Model

Figure 23-1 Schematic gate current components flowing between MOSFET terminals



Model Selectors

Two global selectors are provided to turn on or off the tunneling components. IGCMOD=1 turns on Igc, Igs, and Igd; IGBMOD=1 turns on Igb. When the selectors are set to 0, no gate tunneling currents are modeled.

Equations for Tunneling Currents

Gate-to-Substrate Current

(23-59)

© 2023 Cadence Design Systems, Inc.

$$I_{gbacc} = NF \cdot W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \cdot i_{gtemp} \cdot \exp[-B \cdot TOXE(AIGBACC - BIGBACC \cdot V_{oxacc}) \cdot (1 + CIGBAC \cdot V_{oxacc})]$$

(23-60)

$$I_{gbinv} = NF \cdot W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \cdot i_{gtemp} \cdot \exp[-B \cdot TOXE(AIGBINV - BIGBINV \cdot V_{oxdepinv}) \cdot (1 + CIGBINVV \cdot V_{oxdepinv})]$$

Gate-to-Channel Current (Igc0) and Gate-to-S/D (Igs and Igd)

(23-61)

$$I_{gc0} = NF \cdot W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gse} \cdot V_{aux} \cdot i_{gtemp} \cdot \exp[-B \cdot TOXE(AIGC - BIGC \cdot V_{oxdepinv}) \cdot (1 + CIGCV_{oxdepinv})]$$

Partition of Igc: Igc=Igcs+Igcd

(23-62)

$$I_{gcs} = I_{gc0} \cdot \frac{PIGCD \cdot V_{dseffx} + \exp(-PIGCD \cdot V_{dseffx}) - 1 + 10^{-4}}{PIGCD \cdot V^2_{dseffx} + 2 \cdot 10^{-4}}$$

(23-63)

$$I_{gcd} = I_{gc0} \cdot \frac{1 - (PIGCD \cdot V_{dseffx} + 1) \cdot \exp(-PIGCD \cdot V_{dseffx}) + 10^{-4}}{PIGCD \cdot V^2_{dseffx} + 2 \cdot 10^{-4}}$$

Igs and Igd

(23-64)

$$I_{gs} = NF \cdot W_{eff} DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gs} \cdot V_{gs}' \cdot i_{gtemp} \cdot \exp[-B \cdot TOXE \cdot POXEDGE \cdot (AIGS - BIGS \cdot V_{gs}') \cdot (1 + CIGSV_{gs}')]$$

© 2023 Cadence Design Systems, Inc.

(23-65)

$$I_{gd} = \frac{NF \cdot W_{eff} DLCIGD \cdot A \cdot T_{oxRatioEdge} \cdot V_{gd} \cdot V_{gd}' \cdot i_{gtemp}}{.\exp[-B \cdot TOXE \cdot POXEDGE \cdot (AIGD - BIGD \cdot V_{gd}') \cdot (1 + CIGSV_{gd}')]}$$

Vfbsd is the flat-band voltage between gate and source/drain diffusions calculated as:

If NGATE>0

(23-66)

$$V_{fbsd} = -devsign\left(\frac{k_B T}{q}\right)\log\left(\frac{NGATE}{NSD}\right) + VFBSDOFF$$

Else V_{fbsd}=0.0.

Gate Resistance and Body Resistance Model

Gate Electrode and Intrinsic -Input Resistance (IIR) Model

BSIM6 provides four options for modeling gate electrode resistance (bias-dependent) and intrinsic-input resistance (IIR, bias-dependent). The IIR model considers relaxation-time effect due to distributive RC nature of the channel region, and therefore describes the first-order non-quasi static effect. Thus, the IIR model should not be used together with the charge-deficit NQS model at the same time. The model selector RGATEMOD is used to choose different options.

Model Option and Schematic

RGATEMOD=0 (zero resistance). In this case, no gate resistance is generated.

RGATEMOD=1 (constant resistance). Rgeltd is given by the following equation:

(23-67)

$$R_{geltd} = \frac{RSHG \cdot \left(XGW + \frac{W_{effci}}{3 \cdot NGCON}\right)}{NGCON \cdot (L_{drawn} - XGL) \cdot NF}$$

RGATEMOD=2 (IIR model with variable resistance):

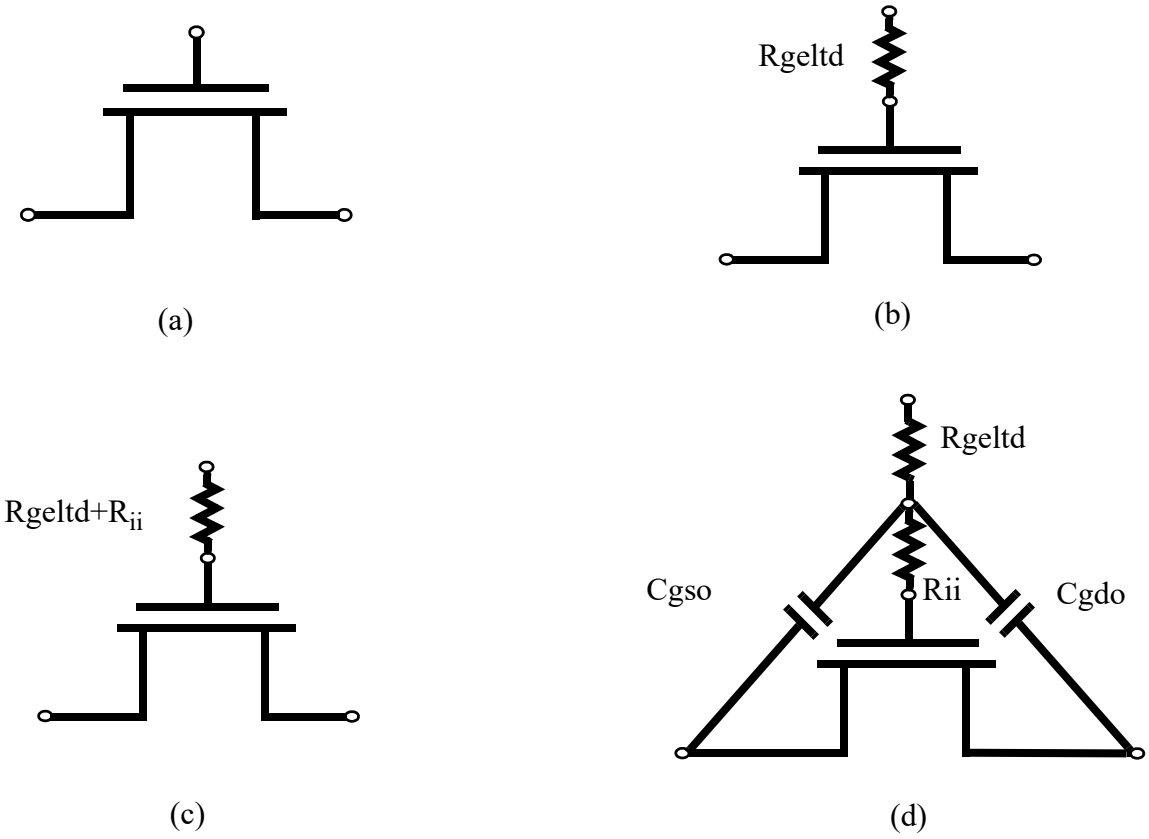
© 2023 Cadence Design Systems, Inc.

(23-68)

$$\frac{1}{R_{ii}} \approx XRCRG1.NF \cdot \left(\mu_{eff} \left(\frac{W_{eff}}{L_{eff}} \right) Cox \cdot q_{ia} + XRCRG2 \cdot \frac{W_{eff} \mu_{eff} C_{oxeff} V_t}{L_{eff}} \right)$$

RGATEMOD=3 (IIR model with two nodes):

Figure 23-2 Gate resistance network for (a) RGATEMOD=0 (b) RGATEMOD=1 (c) RGATEMOD=2 and (d) RGATEMOD=3



Substrate Resistance Network

Model Selector and Topology

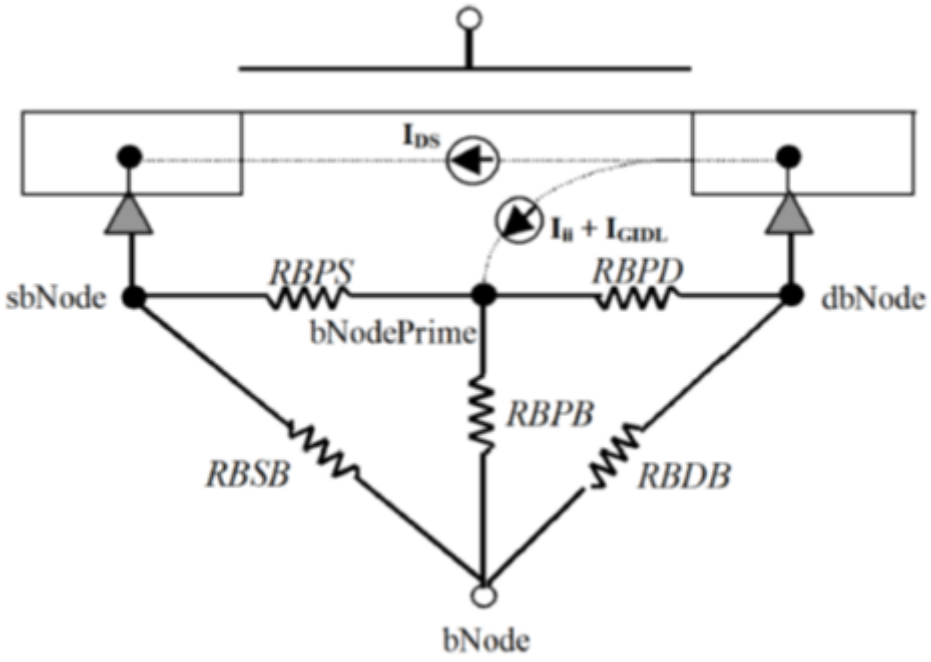
RBODYMOD=0 (Off)

RBODYMOD=1 (On)

© 2023 Cadence Design Systems, Inc.

RBODYMOD=2 (On: Scalable Substrate Network)

Figure 23-3 Topology with the substrate resistance network turned on



Noise Modeling

Noise Models in BSIM 6.0.0	Origin
Flicker noise model	BSIM4 Unified model (FNOIMOD=1)
Thermal noise (TNOIMOD=0)	BSIM4 (TNOIMOD=0)
Thermal noise (TNOIMOD=1)	BSIM4 (TNOIMOD=2)
Gate current shot noise	BSIM4 gate current noise
Noise associated with parasitic resistance	BSIM4 parasitic resistance noise

Flicker Noise Models

FNOIMOD = 1 (Flicker Noise Model): BSIM6's flicker noise model for FNOIMOD=0 is same as FNOIMOD=1 in BSIM4. The unified physical flicker noise model is smooth over all bias regions.

© 2023 Cadence Design Systems, Inc.

The physical mechanism for the flicker noise is trapping/detrapping-related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobilities in the channel. The unified flicker noise model captures this physical process. In the inversion region, the noise density is expressed as [12]

(23-69)

$$S_{id,inv}(f) = \frac{kTq^2\mu_{eff}I_{ds}}{C_{oxe}L_{effNOI}^2 f^{EF}\cdot 10^{10}}\left(NOIA\cdot log\left(\frac{N_0+N^*}{N_l+N^*}\right)\right.$$
$$\left.NOIB\cdot(N_0-N_l)+\frac{NOIC}{2}(N_0^2-N_l^2)\right)$$
$$\frac{kTI_{ds}^2\Delta L_{clm}}{W_{eff}L_{effNOI}^2 f^{EF}\cdot 10^{10}}\left(\frac{NOIA+NOIB\cdot N_l+NOIC\cdot N_l^2}{(N_l+N^*)^2}\right)$$

where $L_{effNOI} = L_{eff} - 2 \cdot LINTNOI$, μ_{eff} is the effective mobility at the given bias condition, and L_{eff} and Weff are the effective channel length and width, respectively.

The parameter Nc is the charge density at the source side given by

$$N_0 = \frac{2n_qC_{ox}V_tq_s}{q}$$

The parameter N_l is the charge density at the drain end given by

$$N_l = \frac{2n_qC_{ox}V_tq_{deff}}{q}$$

and N* is given by

$$N^* = \frac{V_t(C_{ox}+C_d+CIT)}{q}$$

where CIT is a model parameter from DC IV and C_d is the depletion capacitance.

© 2023 Cadence Design Systems, Inc.

ΔL_{clm} is the channel length reduction due to channel length modulation and given by

$$\Delta L_{clm} = litl \cdot log\left(\frac{\frac{V_{ds}-V_{dseff}}{litl} + EM}{E_{sat}}\right)$$

$$E_{sat} = \frac{2VSAT}{\mu_{eff}}$$

In the subthreshold region, the noise density is written as

(23-70)

$$S_{id,subVt}(f) = \frac{NOIA \cdot k \cdot T \cdot I^2_{ds}}{W_{eff} L_{eff} f^{EF} N^{*2} \cdot 10^{10}}$$

The total flicker noise density is

(23-71)

$$S_{id}(f) = \frac{S_{id,inv} \cdot S_{id,subVt}}{S_{id,inv} + S_{id,subVt}}$$

FNOIMOD = 1 (Flicker Noise Model for Halo Transistors): For the noise modeling, it is now assumed that the transistor is composed of two transistors, channel transistor of length L - LH and halo transistor of length LH connected in series and carries same current (IDS) as in single transistor configuration. The individual contribution of the halo and channel transistors to overall noise is obtained using small signal analysis and principle of superposition [13] [14].

Total drain current noise PSD becomes,

$$\begin{aligned} S_{ID} &= S_{ID,1} + S_{ID,2} \\ &= S_{ID,h}\left[\frac{g_{m,ch} + g_{d,ch}}{g_{m,ch} + g_{d,ch} + g_{d,h}}\right]^2 + \\ &S_{ID,ch}\left[\frac{g_{d,h}}{g_{m,ch} + g_{d,ch} + g_{d,h}}\right]^2 \\ &= S_{ID,h}.CF_h + S_{ID,ch}.CF_{ch} \end{aligned}$$

© 2023 Cadence Design Systems, Inc.

We refer to the multiplying factors to $S_{ID,h}$ and $S_{ID,ch}$ in (2.320) as contribution factors (CF). Where,

$$g_{d,ch} = 2n_q\mu C_{ox}\frac{W}{L-L_h}V_t q_{d,ch}$$
$$g_{d,h} = 2n_q\mu C_{ox}\frac{W}{L_h}V_t q_{d,h}$$
$$g_{m,ch} = 2\mu C_{ox}\frac{W}{L-L_h}V_t(q_{s,ch}-q_{d,ch})$$

To calculate $q_{d,h}$ and $q_{s,ch,}$ the fact that the same current flows in one transistor and two transistor noise equivalent configuration is used,

$$i_h = \frac{I_{DS}}{-2n_q\mu C_{ox}\frac{W}{L_h}V_t^2} = (q_{s,h}^2+q_{s,h})-(q_{d,h}^2+q_{d,h})$$
$$i_{ch} = \frac{I_{DS}}{-2n_q\mu C_{ox}\frac{W}{L-L_h}V_t^2} = (q_{s,ch}^2+q_{s,ch})-(q_{d,ch}^2+q_{d,ch})$$

where i_h and i_{ch} are the normalized drain current of halo and channel transistor respectively. Since I_{DS} is known from DC modeling, the above equations are solved for,

$$q_{d,h} = -\frac{1}{2}+\frac{1}{2}\sqrt{1+4(q_{s,h}^2+q_{s,h}-i_h)}$$
$$q_{s,ch} = -\frac{1}{2}+\frac{1}{2}\sqrt{1+4(q_{d,ch}^2+q_{d,ch}+i_{ch})}$$

Here we have used the unified model presented in for halo and channel transistors separately, where S_{ID} is expressed as

$$S_{ID,h} = \frac{kTI_{DS}^2}{\gamma fWL_h^2}\int_0^{L_h}\frac{N_{t,h}^*(E_{F_n})}{N_h^2}dx$$
$$S_{ID,ch} = \frac{kTI_{DS}^2}{\gamma fW(L-L_h)^2}\int_{L_h}^{L}\frac{N_{t,ch}^*(E_{F_n})}{N_{ch}^2}dx$$

where apparent trap density $N^*_{t,ch(h)}(E_{Fn}) = A_{ch(h)}+B_{ch(h)}N_{ch(h)}+C_{ch(h)}N^2_{ch(h)}$, A, B, C are the noise parameters, γ the tunneling parameter, *k* is the Boltzmann constant and *T* is the temperature.

© 2023 Cadence Design Systems, Inc.

Flicker Noise Tuning Flexibility

$$S_{ID,new} = \frac{S_{ID,old}}{1 + NOIA1 \cdot (qs - qdeff)^{(NOIAX)}}$$

Flicker Noise due to drain and source resistance

Flicker noise due to source resistance ($S_{id,Rs}$) is given by

$$S_{id,R_s} = \frac{KFNS * W * (\frac{I_d}{W})^{AFNS}}{f^{BFNS}}$$

Flicker noise due to drain resistance ($S_{id,Rd}$) is given by

$$S_{id,R_d} = \frac{KFND * W * (\frac{I_d}{W})^{AFND}}{f^{BFND}}$$

AFNS, BFNS, KFNS, AFND, BFND and KFND are the model parameters.

Flicker Noise due to EDGEFET (EDGEFET=1)

The Edge FET Model noise is added to the main flicker noise S_{ID}, when the parameter EDGEFET is 1

$$noia_{edge} = NOIA * NEDGE;$$

$$noib_{edge} = NOIB * NEDGE;$$

$$noic_{edge} = NOIC * NEDGE;$$

$$N_0 = \frac{2n_q C_{ox} V_t q_{s,edge}}{q}$$

© 2023 Cadence Design Systems, Inc.

The parameter N_l is the charge density at the drain end given by

$$N_l = \frac{2n_q C_{ox} V_t q_{deff,edge}}{q}$$

$$S_{id,inv,edge}(f) = \frac{kTq^2\mu_{eff} Ids_{edge}}{C_{oxe} L^2_{effNOI} f^{EF} \cdot 10^{10}} \left(noia_{edge} \cdot log\left(\frac{N0 + N^*}{N1 + N^*}\right) noib_{edge} \cdot (N_0 - N_l) + \frac{noic_{edge}}{2}(N_0^2 - N_l^2) \right) \frac{kTIds^2_{edge} \Delta L_{clm}}{W_{edge} LeffNOI^2_{edge} f^{EF} \cdot 10^{10}} \left(\frac{noia_{edge} + noib_{edge} \cdot N_l + noic_{edge} \cdot N_l^2}{(N_l + N^*)^2} \right)$$

$$S_{id,subVt,edge}(f) = \frac{noia_{edge} \cdot k \cdot T \cdot Ids^2_{edge}}{W_{edge} LeffNOI_{edge} f^{EF} N^{*2} \cdot 10^{10}}$$

$$S_{id,edge}(f) = \frac{S_{id,inv,edge} \cdot S_{id,subVt,edge}}{S_{id,inv,edge} + S_{id,subVt,edge}}$$

Channel Thermal Noise

There are two channel thermal noise models in BSIM6. One is a charge-based model (default model) similar to that used in BSIM3v3.2 and BSIM4.7.0 (TNOIMOD=0). The other is the holistic model similar to BSIM4.7.0 (TNOIMOD=2). These two models can be selected through the model selector TNOIMOD.

TNOIDMOD=0 (Charge based model): The noise current is given by:

(23-72)

$$Q_{inv} = |Q_{s,intrinsic} + Q_{s,intrinsic}| \times NFIN_{total}$$

© 2023 Cadence Design Systems, Inc.

(23-73)

$$\overline{i^2}_d = \begin{cases} NTNOI \cdot \dfrac{4kT\Delta f}{R_{ds} + \dfrac{L_{eff}^2}{\mu_{eff} Q_{inv}}} & \text{if RDSMOD=0} \\ NTNOI \cdot \dfrac{4kT\Delta f}{L_{eff}^2} \cdot \mu_{eff} Q_{inv} & \text{if RDSMOD=1} \end{cases}$$

TNOIMOD=1 (Holistic Model)

(23-74)

$$\beta_{tnoi} = RNOIA \cdot \left[1.0 + TNOIA \cdot L_{eff} \cdot \left(\frac{q_{ia}}{E_{sat,noi} L_{eff}} \right)^2 \right]$$

(23-75)

$$\theta_{tnoi} = RNOIB \cdot \left[1.0 + TNOIB \cdot L_{eff} \cdot \left(\frac{q_{ia}}{E_{sat,noi} L_{eff}} \right)^2 \right]$$

(23-76)

$$c_{tnoi} = RNOIC \cdot \left[1.0 + TNOIC \cdot L_{eff} \cdot \left(\frac{q_{ia}}{E_{sat,noi} L_{eff}} \right)^2 \right]$$

(23-77)

$$S_{id} = 4KT \cdot \mu C_{ox} \frac{W_{eff}}{L_{vsat}} V_t D_{ptwg} M_{oc} \left[\frac{q_s + q_{deff}}{2} \cdot \left(1 + \frac{\beta_{lowId}^2}{TNOIK2 + q_{ia}} \cdot \frac{V_{dseff}}{V_{dsat}} \right) + (3 \cdot \beta_{tnoi}^2) \cdot \frac{(q_s - q_{deff})^2}{12 \left(\frac{1+q_s+q_{deff}}{2} \right)} \right]$$

(23-78)

$$S_{ig} = 4KT \cdot \frac{1}{12 \cdot NF \cdot W_{eff} \mu_{eff} \cdot D_{ptwg} M_{oc} C_{ox} \cdot V_t} \frac{L_{vsat}^3}{L_{eff}^2} \cdot \left[\frac{\frac{q_s+q_{deff}}{2}}{\left(\frac{1+q_s+q_{deff}}{2} \right)^2} - \frac{6 \left(\frac{1+q_s+q_{deff}}{2} \right) (q_s - q_{deff})^2}{60 \left(\frac{1+q_s+q_{deff}}{2} \right)^4} + \frac{(q_s - q_{deff})^4}{144 \left(\frac{1+q_s+q_{deff}}{2} \right)^5} \right] \cdot \left(\frac{15}{4} \cdot \theta_{tnoi}^2 \right)$$

© 2023 Cadence Design Systems, Inc.

For version 106.2:

(23-79)

$$S_{ig} = \frac{4KT \cdot [\omega \cdot C_{ox} \cdot W \cdot NF \cdot L]^2 \cdot mig}{1 + (\omega \cdot C_{0x} \cdot L \cdot W \cdot NF \cdot mig)^2}$$

(23-80)

$$S_{ig,id} = -j\omega \cdot 4KT \cdot \mu C_{ox} D_{ptwg} M_{oc} V_t \left(\frac{L_{vsat}}{L_{eff}}\right) \cdot \left[\frac{(q_s - q_{deff})}{12\left(\frac{1+q_s+q_{deff}}{2}\right)} - \frac{(q_s - q_{deff})^3}{144\left(\frac{1+q_s+q_{deff}}{2}\right)^3}\right] \cdot \frac{c_{tnoi}}{0.395}$$

(23-81)

$$c = \frac{S_{ig,id}}{\sqrt{S_{ig}} \cdot \sqrt{S_{id}}}$$

Gate Current Shot Noise

(23-82)

$$\overline{i^2}_{gs} = 2q(I_{gcs} + I_{gs})$$

(23-83)

$$\overline{i^2}_{gd} = 2q(I_{gcd} + I_{gd})$$

(23-84)

$$\overline{i^2}_{gb} = 2qI_{gbinv}$$

Resistor Noise

The noise associated with each parasitic resistors in BSIM6 are calculated

If RDSMOD=1, then

(23-85)

$$\frac{\overline{i_{RS}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{source}}$$

© 2023 Cadence Design Systems, Inc.

(23-86)

$$\frac{\overline{i_{RD}^{2}}}{\Delta f} = 4kT \cdot \frac{1}{R_{drain}}$$

If RGATGEMOD=1, then

(23-87)

$$\frac{\overline{i_{RG}^{2}}}{\Delta f} = 4kT \cdot \frac{1}{R_{geltd}}$$

If RBODYMOD=1, then

(23-88)

$$\frac{\overline{i_{RDB}^{2}}}{\Delta f} = 4kT \cdot \frac{1}{R_{DB}}$$

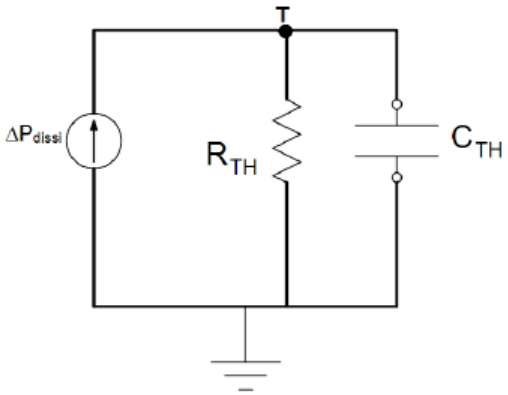
If RDSMOD=1 & HVMOD=1, then

(23-89)

$$\frac{\overline{i_{DRIFT,D}^{2}}}{\Delta f} = 4kT \cdot \frac{1}{R_{DRIFT,D}}$$

$$\frac{\overline{i_{DRIFT,S}^{2}}}{\Delta f} = 4kT \cdot \frac{1}{R_{DRIFT,S}}$$

Figure 23-4 Thermal Network for Self Heating Model



© 2023 Cadence Design Systems, Inc.

Self Heating Model

(23-90)

$$RTH = \frac{RTH0}{(WTH0 + W_{eff}) \cdot NF}$$

(23-91)

$$Cth = CTH0 \times (WTH0 + W_{eff}) \cdot NF$$

Asymmetric MOS Junction Diode Models

Junction Diode IV Model

(23-92)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{V_{bs}}{NJS \cdot V_t}\right) - 1\right] \cdot f_{breakdown} + V_{bs} \cdot G_{min}$$

(23-93)

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{V_{bd}}{NJD \cdot V_t}\right) - 1\right] \cdot f_{breakdown} + V_{bd} \cdot G_{min}$$

(23-94)

$$\begin{aligned} I_{bs_totle} = {} & I_{bs} \\ & - W_{effcj} \cdot NF \cdot J_{tsswgs}(T) \cdot \left[exp\left(\frac{-V_{bs}}{NJTSSWG(T) \cdot Vtm0} \cdot \frac{VTSSWGS}{VTSSWGS - V_{bs}}\right)\right] \\ & - P_{s,deff} J_{tssws}(T)\left[exp\left(\frac{-V_{bs}}{NJTSSW(T) \cdot Vtm0} \cdot \frac{VTSSWS}{VTSSWS - V_{bs}}\right) - 1\right] \\ & - A_{s,deff} J_{tss}(T)\left[exp\left(\frac{-V_{bs}}{NJTS(T) \cdot Vtm0} \frac{VTSS}{VTSS - V_{bs}}\right) - 1\right] + g_{min} \cdot V_{bs} \end{aligned}$$

© 2023 Cadence Design Systems, Inc.

(23-95)

$$\begin{aligned} I_{bd_totle} &= I_{bd} \\ &- W_{effcj} \cdot NF \cdot J_{tsswgd}(T) \cdot \left[exp\left(\frac{-V_{bd}}{NJTSSWGD(T) \cdot Vtm0} \cdot \frac{VTSSWGD}{VTSSWGD - V_{bd}} \right) \right] \\ &- P_{d,deff} J_{tsswd}(T) \left[exp\left(\frac{-V_{bd}}{NJTSSWD(T) \cdot Vtm0} \cdot \frac{VTSSWD}{VTSSWD - V_{bd}} \right) - 1 \right] \\ &- A_{d,deff} J_{tsd}(T) \left[exp\left(\frac{-V_{bd}}{NJTD(T) \cdot Vtm0} \frac{VTSD}{VTSD - V_{bd}} \right) - 1 \right] + g_{min} \cdot V_{bd} \end{aligned}$$

Junction Diode CV Model

(23-96)

$$C_{bs} = A_{seff} C_{jbs} + P_{seff} C_{jbssw} + W_{effcj} \cdot NF \cdot C_{jbsswg}$$

(23-97)

$$C_{jbs} = \begin{cases} CJS(T) \cdot \left(1 - \frac{V_{bs}}{PBS(T)} \right)^{-MJS} & \text{if } \frac{V_{bs}}{PBS(T)} \leq x_0 \\ CJS(T) \cdot \frac{1}{(1-x_0)^{MJS}} \cdot \left[1 + MJS \left(1 + \frac{\frac{V_{bs}}{PBS} - 1}{1 - x_0} \right) \right] & \text{otherwise} \end{cases}$$

(23-98)

$$C_{jbssw} = \begin{cases} CJSWS(T) \cdot \left(1 - \frac{V_{bs}}{PBSWS(T)} \right)^{-MJSWS} & \text{if } \frac{V_{bs}}{PBSWS(T)} \leq x_0 \\ CJSWS(T) \cdot \frac{1}{(1-x_0)^{MJSWS}} \cdot \left[1 + MJSWS \left(1 + \frac{\frac{V_{bs}}{PBSWS(T)} - 1}{1 - x_0} \right) \right] & \text{otherwise} \end{cases}$$

(23-99)

$$C_{jbsswg} = \begin{cases} CJSWGS(T) \cdot \left(1 - \frac{V_{bs}}{PBSWGS(T)} \right)^{-MJSWGS} & \text{if } \frac{V_{bs}}{PBSWGS(T)} \leq x_0 \\ CJSWGS(T) \cdot \frac{1}{(1-x_0)^{MJSWGS}} \cdot \left[1 + MJSWGS \left(1 + \frac{\frac{V_{bs}}{PBSWGS(T)} - 1}{1 - x_0} \right) \right] & \text{otherwise} \end{cases}$$

where the value of x0 is taken as 0.9.

© 2023 Cadence Design Systems, Inc.

(23-100)

$$C_{bd} = A_{deff}C_{jbd} + P_{deff}C_{jbdsw} + W_{effcj} \cdot NF \cdot C_{jbdswg}$$

(23-101)

$$C_{jbd} = \begin{cases} CJD(T) \cdot \left(1 - \frac{V_{bs}}{PBD(T)}\right)^{-MJD} & \text{if } \frac{V_{bs}}{PBD(T)} \leq x_0 \\ CJD(T) \cdot \frac{1}{(1-x_0)^{MJD}} \cdot \left[1 + MJD\left(1 + \frac{\frac{V_{bs}}{PBD}-1}{1-x_0}\right)\right] & \text{otherwise} \end{cases}$$

(23-102)

$$C_{jbdsw} = \begin{cases} CJSWD(T) \cdot \left(1 - \frac{V_{bs}}{PBSWD(T)}\right)^{-MJSWS} & \text{if } \frac{V_{bs}}{PBSWD(T)} \leq x_0 \\ CJSWD(T) \cdot \frac{1}{(1-x_0)^{MJSWD}} \cdot \left[1 + MJSWD\left(1 + \frac{\frac{V_{bs}}{PBSWD(T)}-1}{1-x_0}\right)\right] & \text{otherwise} \end{cases}$$

(23-103)

$$C_{jbdswg} = \begin{cases} CJSWGD(T) \cdot \left(1 - \frac{V_{bs}}{PBSWGD(T)}\right)^{-MJSWGD} & \text{if } \frac{V_{bs}}{PBSWGD(T)} \leq x_0 \\ CJSWGD(T) \cdot \frac{1}{(1-x_0)^{MJSWGD}} \cdot \left[1 + MJSWGD\left(1 + \frac{\frac{V_{bs}}{PBSWGD(T)}-1}{1-x_0}\right)\right] & \text{otherwise} \end{cases}$$

where the value of x0 is taken as 0.9.

Layout Dependent Parasitic Models

Effective Junction Perimeter and Area

If (PS is given)

if (**perMod**=0)

P_{seff}=PS

Else

P_{seff} computed from NF, DWJ, geoMod, DMCG, DMCI, DMDG, DMCGT, RSH, and MIN.

© 2023 Cadence Design Systems, Inc.

The effective junction area on the source side is calculated by:

If (AS is given)

A_{seff}=AS

Else

A_{seff} computed from NF, DWJ, geoMod, DMCG, DMCI, DMDG, DMCGT, RSH, and MIN.

Source/Drain Diffusion Resistance

If (number of sources NRS is given)

ELSE if (**rgeoMod**=0)

Source diffusion resistance Rsdiff is not generated.

Else

Rsdiff computed from NF, DWJ, geoMod, DMCG, DMCI, DMDG, DMCGT, RSH, and MIN.

where the number of source squares NRS is an instance parameter.

Similarly, the drain diffusion resistance is calculated by:

If (number of sources NRD is given)

ELSE if (rgeoMod=0)

Drain diffusion resistance Rddiff is not generated.

Else

Rddiff computed from NF, DWJ, geoMod, DMCG, DMCI, DMDG, DMCGT, RSH, and MIN.

Gate Electrode Resistance

(23-104)

$$R_{geltd} = \frac{RSHG \cdot \left(XGW + \frac{W_{effci}}{3NGCON}\right)}{NGCON \cdot (L_{drawn} - XGL) \cdot NF}$$

© 2023 Cadence Design Systems, Inc.

Options for Source/Drain Connections

Table 1: geoMod Options

geomod	End Source	End Drain	Note
0	isolated	isolated	NF=Odd
1	isolated	shared	NF=Odd, Even
2	shared	shared	NF=Odd, Even
3	shared	isolated	NF=Odd, Even
4	isolated	merged	NF=Odd
5	shared	merged	NF=Odd, Even
6	merged	isolated	NF=Odd
7	merged	shared	NF=Odd, Even
8	merged	merged	NF=Odd
9	sha/iso	shared	NF=Even
10	shared	sha/iso	NF=Even

Options for Source Drain Contacts

Table 2: rgeoMod Options

rgeomod	End Source contact	End Drain Contact
0	No R_{sdiff}	No R_{ddiff}
1	wide	wide
2	wide	point
3	point	wide
4	point	point
5	wide	merged
6	point	merged
7	merged	wide

© 2023 Cadence Design Systems, Inc.

8	merged	point

Temperature Dependence Models

Temperature Dependence of Threshold Voltage

The temperature dependence of V_{th} is modeled by:

(23-105)

$$V_{th}(T) = V_{th}(TNOM) + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff}\right) \cdot \left(\left(\frac{T}{TNOM}\right)^{KT1EXP} - 1\right)$$
$$V_{fb}(T) = V_{fb}(TNOM) - KT1 \cdot \left(\frac{T}{TNOM} - 1\right)$$

(23-106)

$$VFBSDOFF(T) = VFBSDOFF(TNOM) \cdot [1 + TVFBSDOFF \cdot (T - TNOM)]$$
$$NFACTOR(T) = NFACTOR(TNOM) + TFACTOR \cdot \left(\frac{T}{TNOM} - 1\right)$$

(23-107)

$$ETA0(T) = ETA0(TNOM) + TETA0\left(\frac{T}{TNOM} - 1\right)$$

Temperature Dependence of Mobility

(23-108)

$$U0(T) = U0(TNOM) \cdot (T/TNOM)^{UTE}$$

(23-109)

$$UA(T) = UA(TNOM)[1 + UA1 \cdot (T - TNOM)]$$

(23-110)

$$UC(T) = UC(TNOM)[1 + UC1 \cdot (T - TNOM)]$$

(23-111)

$$UD(T) = UD(TNOM) \cdot (T/TNOM)^{UD1}$$

© 2023 Cadence Design Systems, Inc.

(23-112)

$$UCS(T) = UCS(TNOM) \cdot (T/TNOM)^{UCSTE}$$

Temperature Dependence of Junction Diode IV

(23-113)

$$I_{sbs} = A_{seff}J_{ss}(T) + P_{seff}J_{ssws}(T) + W_{effcj} \cdot NF \cdot J_{sswgs}(T)$$

(23-114)

$$I_{sbd} = A_{deff}J_{sd}(T) + P_{deff}J_{sswd}(T) + W_{effcj} \cdot NF \cdot J_{sswgd}(T)$$

Temperature Dependence of Junction Diode CV

(23-115)

$$PBS(T) = PBS(TNOM) - TPB \cdot (T - TNOM)$$

(23-116)

$$PBSWS(T) = PBSWS(TNOM) - TPBSW \cdot (T - TNOM)$$

(23-117)

$$PBSWGS(T) = PBSWGS(TNOM) - TPBSWG \cdot (T - TNOM)$$

(23-118)

$$PBD(T) = PBD(TNOM) - TPB \cdot (T - TNOM)$$

(23-119)

$$PBSWD(T) = PBSWD(TNOM) - TPBSW \cdot (T - TNOM)$$

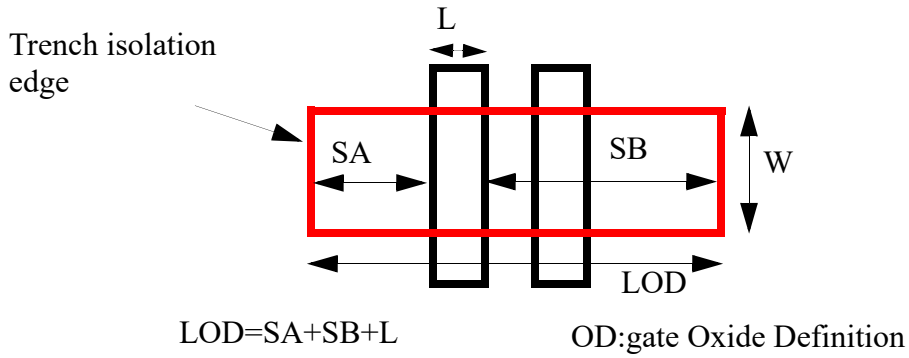
(23-120)

$$PBSWGD(T) = PBSWGD(TNOM) - TPBSWG \cdot (T - TNOM)$$

© 2023 Cadence Design Systems, Inc.

Stress Effect Model Development

Figure 23-5 Typical Layout of a MOSFET



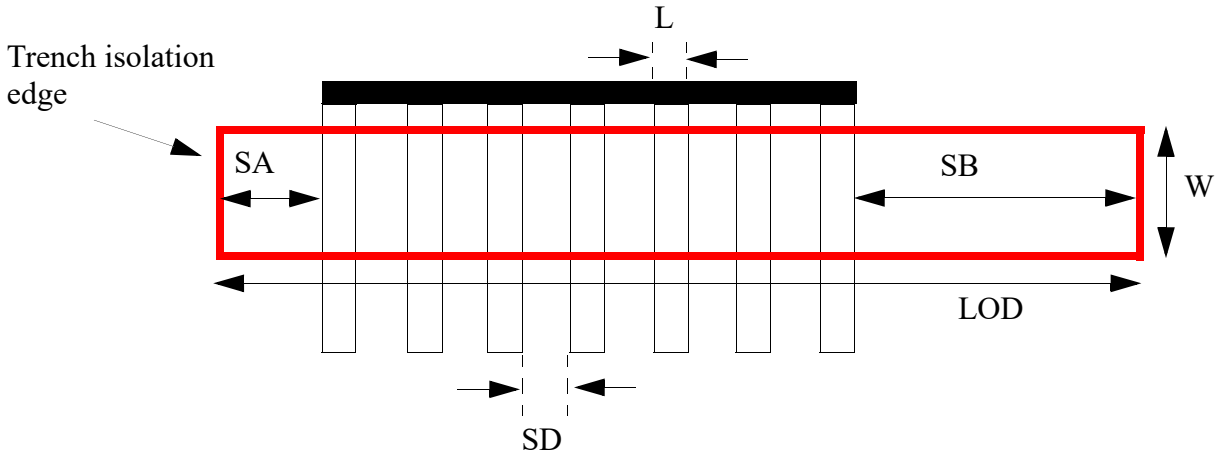
(23-121)

$$VTH0 = VTH0_{original} + \frac{KVTH0}{Kstress_vth0} \cdot (Inv_sa + Inv_sb - Inv_sa_{ref} - Inv_sb_{ref})$$

$$K2 = K2_{original} + \frac{STK2}{Kstress_vth0^{LODK2}} \cdot (Inv_sa + Inv_sb - Inv_sa_{ref} - Inv_sb_{ref})$$

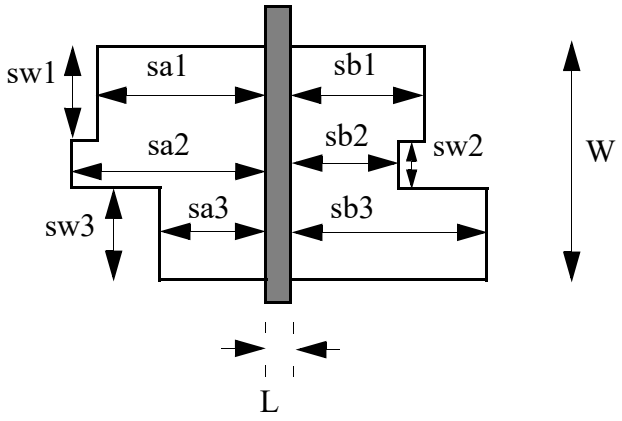
$$ETA0 = ETA0_{original} + \frac{STETA0}{Kstress_vth0^{LODETA0}} \cdot (Inv_sa + Inv_sb - Inv_sa_{ref} - Inv_sb_{ref})$$

Figure 23-6 Layout of multiple finger MOSFET



© 2023 Cadence Design Systems, Inc.

Figure 23-7 Typical layout of MOS devices with more instance parameters (swi, sai, and sbi) in addition to traditional L and W



Well Proximity Effect Model

(23-122)

$$\begin{aligned} Vth0 &= Vth0_{org} + KVTH0WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC) \\ K2 &= K2_{org} + K2WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC) \\ \mu_{eff} &= \mu_{eff,org} \cdot (1 + KU0WE \cdot (SCA + WEB \cdot SCB + WEB \cdot SCC)) \end{aligned}$$

C-V Model

Inversion Charge

(23-123)

$$q_I = n_q \cdot \left[q_s + q_d + \frac{1}{3} \cdot \frac{(q_s - q_d)^2}{1 + q_s + q_d} \right]$$

Bulk Charge

(23-124)

$$q_B = A + B + \frac{1}{3} \cdot \frac{\Delta q^2}{C^3} \cdot \left[\frac{4}{8} \cdot \left(C^2 + P.Q \right) \cdot \frac{1}{1 + q_s + q_d} + \frac{2}{\gamma_g^2} \right] - n_q \cdot \left[q_s + q_d + \frac{1}{3} \cdot \frac{(q_s - q_d)^2}{1 + q_s + q_d} \right]$$

© 2023 Cadence Design Systems, Inc.

where

(23-125)

$$P = \sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_s}{\gamma_g^2}}$$

$$Q = \sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_d}{\gamma_g^2}}$$

$$A = \frac{v_g - v_{fb} - \psi_p + 2.q_s}{1 + 2.\sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_s}{\gamma_g^2}}}$$

$$B = \frac{v_g - v_{fb} - \psi_p + 2.q_d}{1 + 2.\sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_s}{\gamma_g^2}}}$$

$$C = \sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_s}{\gamma_g^2}} + \sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_d}{\gamma_g^2}}$$

Bulk Charge with poly depletion effect, CLM and velocity saturation effects:

(23-126)

$$d_{qgeff} = (v_g - v_{fb} - \psi_p + 2.q_d)\left[\frac{2\sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_d}{\gamma_g^2}} - 1}{2\sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_d}{\gamma_g^2}} + 1}\right]$$

(23-127)

$$q_{beff} = \left[(v_g - v_{fb} - \psi_p) - 2(n_q - 1)q_d + d_{qgeff}\right]$$

(23-128)

$$q_B = \frac{1}{MDL}\left[A + B + \frac{1}{3}.\frac{\Delta q^2}{C^3} \cdot \left(\frac{4}{8} \cdot (C^2 + P.Q) \cdot \frac{1}{1 + q_s + q_d} + \frac{2}{\gamma_g^2}\right) - n_q.\left(q_s + q_d + \frac{1}{3} \cdot \frac{(q_s - q_d)^2}{1 + q_s + q_d}\right)\right] + (MDL - 1)q_{beff}$$

© 2023 Cadence Design Systems, Inc.

where

$$P = \sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_s}{\gamma_g^2}}$$
$$Q = \sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_d}{\gamma_g^2}}$$
$$A = \frac{v_g - v_{fb} - \psi_p + 2.q_s}{1 + 2.\sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_s}{\gamma_g^2}}}$$
$$B = \frac{v_g - v_{fb} - \psi_p + 2.q_d}{1 + 2.\sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_s}{\gamma_g^2}}}$$
$$C = \sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_s}{\gamma_g^2}} + \sqrt{\frac{1}{4} + \frac{v_g - v_{fb} - \psi_p + 2.q_d}{\gamma_g^2}}$$

Source and Drain Charges

(23-129)

$$Q_s = \frac{n_q}{3}\left[2 \cdot q_s + q_{deff} + \frac{1}{2} \cdot \left(1 + \frac{4}{5} \cdot q_s + \frac{6}{5} \cdot q_{deff}\right)\left(\frac{q_s - q_{deff}}{1 + q_s + q_{deff}}\right)^2\right]$$
$$Q_d = \frac{n_q}{3}\left[q_s + 2 \cdot q_{deff} + \frac{1}{2} \cdot \left(1 + \frac{6}{5} \cdot q_s + \frac{4}{5} \cdot q_{deff}\right)\left(\frac{q_s - q_{deff}}{1 + q_s + q_{deff}}\right)^2\right]$$

Bias Dependent Overlap Capacitance Model

(23-130)

$$\frac{Q_{gs,ov}}{NF \cdot W_{effCV}} = CGSO \cdot V_{gs} +$$
$$CGSL \cdot \left[V_{gs} - V_{fbsd} - V_{gs,overlap} - \frac{CKAPPAS}{2}\left(\sqrt{1 - \frac{4V_{gs,overlap}}{CKAPPAS}} - 1\right)\right]$$

(23-131)

$$\frac{Q_{gd,ov}}{NF \cdot W_{effCV}} = CGDO \cdot V_{gd} +$$
$$CGDL \cdot \left[V_{gd} - V_{fbsd} - V_{gd,overlap} - \frac{CKAPPAD}{2}\left(\sqrt{1 - \frac{4V_{gd,overlap}}{CKAPPAD}} - 1\right)\right]$$

© 2023 Cadence Design Systems, Inc.

Outer Fringing Capacitance

(23-132)

$$CF = \frac{2 \cdot EPSROX \cdot \epsilon_0}{\pi} \cdot ln[CFRCOEFF \cdot (1 + \frac{0.4e-6}{TOX})]$$

Related Topics

BSIM6 Model (bsim6)

Instance

Model

Version Update and Enhancements

Component Statements for BSIM6

© 2023 Cadence Design Systems, Inc.

Component Statements for BSIM6

This device is supported within altergroups.

Click the following links for more details about the BSIM6 model:

BSIM6 Model (bsim6)

Instance Parameters

Model Definition

Model Parameters

Output Parameters

Related Topics

© 2023 Cadence Design Systems, Inc.

Instance Parameters

m	1.0	Multiplicity factor (number of MOSFETs in parallel).
geomod	0	Geo dependent parasitics model.
rgeomod	0	Geometry-dependent source/drain resistance. 0: RSH-based, 1: Holistic.
rgatemod	0	Gate resistance model selector.
rbodymod	0	Distributed body R model.
l	(10*1.0e-6) m	Channel length.
w	(10*1.0e-6) m	Total width including fingers.
nf	1	Number of fingers.
as	0.0 m^2	Source-to-substrate junction area.
ad	0.0 m^2	Drain-to-substrate junction area.
ps	0.0 m	Source-to-substrate junction perimeter.
pd	0.0 m	Drain-to-substrate junction perimeter.
vfbsdoff	0.0 V	Flatband voltage offset parameter.
nrs	1.0	Number of squares in source.
nrd	1.0	Number of squares in drain.
minz	0	Minimize either drain or source.
xgw	0.0 m	Distance from gate contact centre to device edge.

© 2023 Cadence Design Systems, Inc.

ngcon	1	Number of gate contacts.
rbpb	50.0 Ω	Resistance between bNodePrime and bNode.
rbdb	50.0 Ω	Resistance between bNode and dbNode.
rbsb	50.0 Ω	Resistance between bNode and sbNode.
rbps	50.0 Ω	Resistance between bNodePrime and sbNode.
rbpd	50.0 Ω	Resistance between bNodePrime and dbNode.
rdb	50.0 Ω	Resistance between ddbulk node and d Node.
dtemp	0.0 C	Offset of device temperature.
trise	0.0 C	Alias of dtemp.
sa	0.0 m	Distance between OD edge and poly from one side.
sb	0.0 m	Distance between OD edge and poly from other side.
sd	0.0 m	Distance between neighboring fingers.
sca	0.0	Integration of first distribution function for scattered well dopants.
scb	0.0	Integration of second distribution function for scattered well dopants.
scc	0.0	Integration of second distribution function for scattered well dopants.
sc	0.0 m	Distance to a single well edge; if <= 0.0, turn off WPE.
isnoisy	yes	Should device generate noise.Possible values are no and yes.

© 2023 Cadence Design Systems, Inc.

sslmod	0	Sub-surface leakage drain current,0: Turn off 1: Turn on.
region	triode	Estimated operating region. Spectre outputs number (0-4) in a rawfile.Possible values are off, triode, sat, subth and breakdown.
ids0mult	1.0	Variability in drain current for miscellaneous reasons.
delvt0	0.0	Zero bias threshold voltage variation.
delvto	0.0	Aliase of delvt0.
mulu0	1.0	
muluo	1.0	Aliase of mulu0.
edgefet	1	0: Edge FET Model Off, 1: Edge FET Model ON.

Related Topics

Model Definition

Model Parameters

Output Parameters

Related Topics

Model Definition

```
model modelName bsim6 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

type	n	Transistor type.Possible values are p and n.
version	6.00	The model parameter "version" accepts only a real number value, such as 6.00 for version=6.0.0. The available versions for the bsim6 model are 6.00(6.0.0), 6.10(6.1.0), 6.11(6.1.1), 106.2(Bsimbulk 106.2.0), 107.0(Bsimbulk 107.0), and 107.10(Bsimbulk 107.1.0)..
compatible	spectre	Compatibility parameters.Possible values are spectre, spice2, spice3, cdsspice, hspice, spiceplus, eldo, sspice and mica.
gmin_compatible	spectre	Choose gmin compatibility of model, possible values are 'spectre'(default) and 'cmc'.Possible values are spectre, cmc and hspice.
vthmod	0	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'.Possible values are std and vthcc.
ivth	0.0 A	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
ivthw	0.0 m	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
ivthl	0.0 m	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
ivth_vdsmin	0.05 V	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.

© 2023 Cadence Design Systems, Inc.

vdsatmod	0	Vdsat output selector. Possible values are std, gds, and slow_gds.Possible values are std, gds and slow_gds.
vdsat_c	0.0	Coefficient for Gds based Vdsat.
vdsat_vdl	0.0	Coefficient for Gds based Vdsat.
vdsat_vadj	0.0	Coefficient for Gds based Vdsat.
minr	0.001	Minr.
cvmod	0	0: Consistent I-V/C-V, 1: Different I-V/C-V.
covmod	0	0: Use bias-independent overlap capacitances, 1: Use bias-dependent overlap capacitances.
rdsmod	0	0: Internal bias-dependent and external bias-independent S/D resistance model, 1: External S/D resistance model, 2: Internal S/D resistance model.
wpemod	0	Model flag for WPE.
asymmod	0	0: Asymmetry model turned off - forward mode parameters used, 1: Asymmetry model turned on.
gidlmod	0	0: Turn off GIDL current, 1: Turn on GIDL current.
igcmod	0	0: Turn off Igc, Igs and Igd, 1: Turn on Igc, Igs and Igd.
igbmod	0	0: Turn off Igb, 1: Turn on Igb.
tnoimod	0	Thermal noise model selector.
shmod	0	0: Self heating model selector, 1: Turn on self heating model.
mobscale	0	Mobility scaling model, 0: Old Model, 1: New Model.

© 2023 Cadence Design Systems, Inc.

tmemod	0	
xgw	0.0 m	Distance from gate contact centre to dev edge.
llong	1.0e-5 m	L of extracted long channel device.
lmlt	1.0	Length shrinking parameter.
wmlt	1.0	Width shrinking parameter.
xl	0.0 m	L offset for channel length due to mask/etch effect.
wwide	1.0e-5 m	W of extracted wide channel device.
xw	0.0 m	W offset for channel width due to mask/etch effect.
lint	0.0 m	Delta L for I-V.
ll	0.0 m^(1+lln)	Length reduction parameter.
lw	0.0 m^(1+lwn)	Length reduction parameter.
lwl	0.0 m^(1+lln +lwn)	Length reduction parameter.
lln	1.0	Length reduction parameter.
lwn	1.0	Length reduction parameter.
wint	0.0 m	Delta W for I-V.
wl	0.0 m^(1+wln)	Width reduction parameter.

© 2023 Cadence Design Systems, Inc.

ww	0.0 m^(1+wwn)	Width reduction parameter.
wwl	0.0 m^(1+wwn +wln)	Width reduction parameter.
wln	1.0	Width reduction parameter.
wwn	1.0	Width reduction parameter.
dlc	0.0 m	Delta L for C-V.
llc	0.0 m^(1+lln)	Length reduction parameter.
lwc	0.0 m^(1+lwn)	Length reduction parameter.
lwlc	0.0 m^(1+lln +lwn)	Length reduction parameter.
dwc	0.0 m	Delta W for C-V.
wlc	0.0 m^(1+wln)	Width reduction parameter.
wwc	0.0 m^(1+wwn)	Width reduction parameter.
wwlc	0.0 m^(1+wwn +wln)	Width reduction parameter.

© 2023 Cadence Design Systems, Inc.

toxe	3.0e-9 m	Effective gate dielectric thickness relative to SiO2.
toxp	3.0e-9 m	Physical gate dielectric thickness. If not given, toxp is calculated from toxe and dtox.
dtox	0.0 m	Difference between effective dielectric thickness and physical thickness.
ndep	1e24 1/m^3	Channel doping concentration for I-V.
ndepl1	0.0 m	Length dependence coefficient of ndep.
ndeplexp1	1.0	Length dependence exponent coefficient of ndep.
ndepl2	0.0 m	Length dependence of NDEP - for short channel devices.
ndeplexp2	2.0	Length dependence exponent coefficient of ndep.
ndepw	0.0 m	Width dependence coefficient of ndep.
ndepwexp	1.0	Width dependence exponent coefficient of ndep.
ndepwl	0.0 m^2	Width-length dependence coefficient of ndep.
ndepwlexp	1.0	Width-length dependence exponent coefficient of ndep.
lndep	0.0 1/m^2	Length dependence of NDEP.
wndep	0.0 1/m^2	Width dependence of NDEP.
pndep	0.0 1/m	Area dependence of NDEP.
ndepcv	1e24 1/m^3	Channel doping concentration for C-V.
ndepcvl1	0.0 m	Length dependence coefficient of ndepcv.

© 2023 Cadence Design Systems, Inc.

ndepcvlexp1	1.0	Length dependence exponent coefficient of ndepcv.
ndepcvl2	0.0 m	Length dependence coefficient of ndepcv - for short channel devices.
ndepcvlexp2	2.0	Length dependence exponent coefficient of ndepcv.
ndepcvw	0.0 m	Width dependence coefficient of ndepcv.
ndepcvwexp	1.0	Width dependence exponent coefficient of ndepcv.
ndepcvwl	0.0 m^2	Width-length dependence coefficient of ndepcv.
ndepcvwlexp	1.0	Width-length dependence exponent coefficient of ndepcv.
lndepcv	0.0 $1/m^2$	Length dependence of NDEP for C-V.
wndepcv	0.0 $1/m^2$	Width dependence of NDEP for C-V.
pndepcv	0.0 1/m	Area dependence of NDEP for C-V.
ngate	5e25 $1/m^3$	Gate doping concentration.
lngate	0.0 $1/m^2$	Length dependence of NGATE.
wngate	0.0 $1/m^2$	Width dependence of NGATE.
pngate	0.0 1/m	Area dependence of NGATE.
easub	4.05 eV	Electron affinity of substrate.
ni0sub	1.1e16 $1/m^3$	Intrinsic carrier concentration of the substrate at 300.15K.
bg0sub	1.17 eV	Bandgap of substrate at 300.15K.
epsrsub	11.9	Relative dielectric constant of the channel material.

© 2023 Cadence Design Systems, Inc.

epsrox	3.9	Relative dielectric constant of the gate dielectric.
xj	1.5e-7 m	S/D junction depth.
lxj	0.0 m^2	Length dependence of XJ.
wxj	0.0 m^2	Width dependence of XJ.
pxj	0.0 m^3	Area dependence of XJ.
vfb	(-1.0) V	Flatband voltage.
lvfb	0.0 V m	Length dependence of VFB.
wvfb	0.0 V m	Width dependence of VFB.
pvfb	0.0 V m^2	Area dependence VFB.
vfbl	0.0 m	Length dependence coefficient of VFBCV.
vfblexp	1.0	Length dependence exponent coefficient of VFBCV.
vfbw	0.0 m	Width dependence coefficient of VFBCV.
vfbwexp	1.0	Width dependence exponent coefficient of VFBCV.
vfbwl	0.0 m^2	Width-length dependence coefficient of VFBCV.
vfbwlexp	1.0	Width-length dependence exponent coefficient of VFBCV.
vfbcv	(-1.0) V	Flatband voltage for C-V.
lvfbcv	0.0 V m	Length dependence of VFBCV.
wvfbcv	0.0 V m	Width dependence of VFBCV.
pvfbcv	0.0 V	Area dependence VFBCV.

© 2023 Cadence Design Systems, Inc.

vfbcvl	0.0 m	Length dependence coefficient of vfbcv.
vfbcvlexp	1.0	Length dependence exponent coefficient of vfbcv.
vfbcvw	0.0 m	Width dependence coefficient of vfbcv.
vfbcvwexp	1.0	Width dependence exponent coefficient of vfbcv.
vfbcvwl	0.0 m^2	Width-length dependence coefficient of vfbcv.
vfbcvwlexp	1.0	Width-length dependence coefficient of vfbcv.
permod	1	Whether ps/pd (when given) include gate-edge perimeter.
dwj	0.0 m	Delta W for S/D junctions.
nsd	1e26 1/ m^3	S/D doping concentration.
lnsd	0.0 1/m^2	Length dependence of NSD.
wnsd	0.0 1/m^2	Width dependence of NSD.
pnsd	0.0 1/m	Area dependence of NSD.
delvt0	0.0	Zero bias threshold voltage variation.
dvtp0	0.0 m	First coefficient of drain-induced vth shift for long-channel pocket devices.
ldvtp0	0 m^2	Length dependence of DVTP0.
wdvtp0	0 m^2	Width dependence of DVTP0.
pdvtp0	0 m^3	Area dependence of DVTP0.
dvtp1	0.0 1/V	Second coefficient of drain-induced Vth shift for long-channel pocket devices.

© 2023 Cadence Design Systems, Inc.

ldvtp1	0 m/V	Length dependence of DVTP1.
wdvtp1	0 m/V	Width dependence of DVTP1.
pdvtp1	0 m^2/V	Area dependence of DVTP1.
dvtp2	0.0 m V	3rd parameter for vth shift due to pocket.
ldvtp2	0 m^2/V	Length dependence of DVTP2.
wdvtp2	0 m^2/V	Width dependence of DVTP2.
pdvtp2	0 m^3/V	Area dependence of DVTP2.
dvtp3	0.0	4th parameter for vth shift due to pocket.
ldvtp3	0 m	Length dependence of DVTP3.
wdvtp3	0 m	Width dependence of DVTP3.
pdvtp3	0 m^2	Area dependence of DVTP3.
dvtp4	0.0 1/V	5th parameter for vth shift due to pocket.
ldvtp4	0 m/V	Length dependence of DVTP4.
wdvtp4	0 m/V	Width dependence of DVTP4.
pdvtp4	0 m^2/V	Area dependence of DVTP4.
dvtp5	0.0 V	6th parameter for vth shift due to pocket.
ldvtp5	0 m V	Length dependence of DVTP5.
wdvtp5	0 m V	Width dependence of DVTP5.
pdvtp5	0 m^2 V	Area dependence of DVTP5.

© 2023 Cadence Design Systems, Inc.

phin	0.045 V	Non-uniform vertical doping effect on surface potential.
lphin	0.0 m V	Length dependence of PHIN.
wphin	0.0 m V	Width dependence of PHIN.
pphin	0.0 m^2 V	Area dependence of PHIN.
eta0	0.08	DIBL coefficient.
leta0	0.0 m	Length dependence of ETA0.
weta0	0.0 m	Width dependence of ETA0.
peta0	0.0 m^2	Area dependence of ETA0.
eta0r	0.08	DIBL coefficient.
leta0r	0.0 m	Length dependence of ETA0R.
weta0r	0.0 m	Width dependence of ETA0R.
peta0r	0.0 m^2	Area dependence of ETA0R.
dsub	1.0	Length scaling exponent for DIBL.
etab	(-0.07) 1/V	Body bias coefficient for subthreshold DIBL effect.
etabexp	1.0	Exponent coefficient of etab.
letab	0.0 m/V	Length dependence of ETAB.
wetab	0.0 m/V	Width dependence of ETAB.
petab	0.0 m^2/V	Area dependence of ETAB.

© 2023 Cadence Design Systems, Inc.

k1	0.0 V^0.5	First-order body-bias Vth shift due to vertical non-uniform doping.
k1l	0.0	Length dependence coefficient of K1.
k1lexp	1.0	Length dependence exponent coefficient of K1.
k1w	0.0	Width dependence coefficient of k1.
k1wexp	1.0	Width dependence exponent coefficient of K1.
k1wl	0.0	Width-length dependence coefficient of K1.
k1wlexp	1.0	Width-length dependence exponent coefficient of K1.
lk1	0.0 m V^0.5	Length dependence of K1.
wk1	0.0 m V^0.5	Width dependence of K1.
pk1	0.0 m^2 V^0.5	Area dependence of K1.
k2	0.0 V	Vth shift due to vertical non-uniform doping.
k2l	0.0 m^K2LEXP	Length dependence coefficient of k2.
k2lexp	1.0	Length dependence exponent coefficient of k2.
k2w	0.0 m^K2WEXP	Width dependence coefficient of k2.
k2wexp	1.0	Width dependence exponent coefficient of k2.
k2wl	0.0	Width-length dependence coefficient of k2.

© 2023 Cadence Design Systems, Inc.

k2wlexp	1.0	Width-length dependence exponent coefficient of k2.
lk2	0.0 m	Length dependence of K2.
wk2	0.0 m	Width dependence of K2.
pk2	0.0 m^2	Area dependence of K2.
ados	0.0	Quantum mechanical effect pre-factor switch in inversion.
bdos	1.0	Charge centroid parameter - slope of C-V curve under QME in inversion.
qm0	1.0e-3	Charge centroid parameter - starting point for QME in inversion.
etaqm	0.54	Bulk charge coefficient for charge centroid in inversion.
cit	0.0 F/m^2	Parameter for interface traps.
lcit	0.0 F/m	Length dependence of CIT.
wcit	0.0 F/m	Width dependence of CIT.
pcit	0.0 F	Area dependence of CIT.
nfactor	0.0	Subthreshold slope factor.
nfactorl	0.0 m^NFACTORLEXP	Length dependence coefficient of nfactor.
nfactorlexp	1.0	Length dependence exponent coefficient of nfactor.

© 2023 Cadence Design Systems, Inc.

nfactorw	0.0 m^NFACTORWEXP	Width dependence coefficient of nfactor.
nfactorwexp	1.0	Width dependence exponent coefficient of nfactor.
nfactorwl	0.0 m^(2 NFACTORWLEXP)	Width-length dependence coefficient of nfactor.
nfactorwlexp	1.0	Width-length dependence exponent coefficient of nfactor.
lnfactor	0.0 m	Length dependence of NFACTOR.
wnfactor	0.0 m	Width dependence of NFACTOR.
pnfactor	0.0 m^2	Area dependence of NFACTOR.
cdscd	1e-9 F/m^2 V	Drain bias sensitivity of subthreshold slope.
cdscdl	0.0 m^CDSCDLEXP	Length dependence coefficient of cdscd.
cdscdlexp	1.0	Length dependence exponent coefficient of cdscd.
lcdscd	0.0 F/m/V	Length dependence of CDSCD.
wcdscd	0.0 F/m/V	Width dependence of CDSCD.
pcdscd	0.0 F/V	Area dependence of CDSCD.
cdscdr	1e-9 F/m^2 V	Drain bias sensitivity of subthreshold slope.

© 2023 Cadence Design Systems, Inc.

cdscdlr	0.0 m^CDSCDLEXP	Length dependence coefficient of CDSCDR.
lcdscdr	0.0 F/mV	Length dependence of CDSCDR.
wcdscdr	0.0 F/mV	Width dependence of CDSCDR.
pcdscdr	0.0 F/V	Area dependence of CDSCDR.
cdscb	0.0 F/m^2V	Body-bias sensitivity of subthreshold slope.
cdscbl	0.0 m^CDSCBLEXP	Length dependence coefficient of CDSCB.
cdscblexp	1.0	Length dependence exponent coefficient of CDSCB.
lcdscb	0.0 F/m/V	Length dependence of CDSCB.
wcdscb	0.0 F/m/V	Width dependence of CDSCB.
pcdscb	0.0 F/V	Area dependence of CDSCB.
vsat	1e5 m/s	Saturation velocity.
lvsat	0.0 m^2/s	Length dependence of VSAT.
wvsat	0.0 m^2/s	Width dependence of VSAT.
pvsat	0.0 m^3/s	Area dependence of VSAT.

© 2023 Cadence Design Systems, Inc.

vsatl	0.0 m^VSATLEXP	Length dependence coefficient of VSAT.
vsatlexp	1.0	Length dependence exponent coefficient of VSAT.
vsatw	0.0 m^VSATWEXP	Width dependence coefficient of VSAT.
vsatwexp	1.0	Width dependence exponent coefficient of VSAT.
vsatwl	0.0 m^(2 VSATWLEXP)	Width-length dependence coefficient of VSAT.
vsatwlexp	1.0	Width-length dependence exponent coefficient of VSAT.
vsatr	1e5 m/s	Saturation velocity.
lvsatr	0.0 m^2/s	Length dependence of VSATR.
wvsatr	0.0 m^2/s	Width dependence of VSATR.
pvsatr	0.0 m^3/s	Area dependence of VSATR.
delta	0.125 V	Smoothing function factor for Vdsat.
ldelta	0.0 m	Length dependence of DELTA.
wdelta	0.0 m	Width dependence of DELTA.
pdelta	0.0 m^2	Area dependence of DELTA.
deltal	0.0 m^DELTALEXP	Length dependence coefficient of delta.

© 2023 Cadence Design Systems, Inc.

deltalexp	1.0	Length dependence exponent coefficient of delta.
vsatcv	1e5 m/s	VSAT parameter for C-V.
lvsatcv	0.0 m^2/s	Length dependence of VSATCV.
wvsatcv	0.0 m^2/s	Width dependence of VSATCV.
pvsatcv	0.0 m^3/s	Area dependence of VSATCV.
vsatcvl	0.0 m^VSATCVLEXP	Length dependence coefficient of VSATCV.
vsatcvlexp	1.0	Length dependence exponent coefficient of VSATCV.
vsatcvw	0.0 m^VSATCVWEXP	Width dependence coefficient of VSATCV.
vsatcvwexp	1.0	Length dependence exponent coefficient of VSATCV.
vsatcvwl	0.0 m^(2 VSATCVWLEXP)	Width-length dependence coefficient of VSATCV.
vsatcvwlexp	1.0	Width-length dependence exponent coefficient of VSATCV.
up1	0.0	Mobility channel length coefficient.
lp1	1.0e-8	Mobility channel length exponential coefficient.
up2	0.0	Mobility channel length coefficient.
lp2	1.0e-8	Mobility channel length exponential coefficient.

© 2023 Cadence Design Systems, Inc.

mulu0	1.0	Multiplication factor for low field mobility.
u0	67.0e-3 $m^2/V/s$	Low Field mobility.
u0l	0.0 m^U0LEXP	Length dependence coefficient of U0.
u0lexp	1.0	Length dependence exponential coefficient of u0.
lu0	0.0 $m^3/V/s$	Length dependence of U0.
wu0	0.0 $m^3/V/s$	Width dependence of U0.
pu0	0.0 $m^4/V/s$	Area dependence of U0.
u0r	67.0e-3 $m^2/V/s$	Reverse-mode Low Field mobility.
lu0r	0.0 $m^3/V/s$	Length dependence of U0R.
wu0r	0.0 $m^3/V/s$	Width dependence of U0R.
pu0r	0.0 $m^4/V/s$	Area dependence of U0R.
etamob	1.0	Effective field parameter (should be kept close to 1).
ua	0.001 (m/V)^EU	Mobility reduction coefficient.
ual	0.0 m^UALEXP	Length dependence coefficient of UA.

© 2023 Cadence Design Systems, Inc.

ualexp	1.0	Length dependence exponent coefficient of UA.
uaw	0.0 m^UAWEXP	Width dependence coefficient of UA.
uawexp	1.0	Width dependence exponent coefficient of UA.
uawl	0.0 m^UAWLEXP	Width-length dependence coefficient of UA.
uawlexp	1.0	Width-length dependence coefficient of UA.
lua	0.0 m (m/V)^EU	Length dependence of UA.
wua	0.0 m (m/V)^EU	Width dependence of UA.
pua	0.0 m^2 (m/V)^EU	Area dependence of UA.
uar	0.001 m/V	Reverse-mode mobility reduction coefficient.
luar	0.0 m (m/V)^EU	Length dependence of UAR.
wuar	0.0 m (m/V)^EU	Width dependence of UAR.
puar	0.0 m^2 (m/V)^EU	Area dependence of UAR.
eu	1.5	Mobility reduction exponent.
leu	0.0 m	Length dependence of EU.
weu	0.0 m	Width dependence of EU.

© 2023 Cadence Design Systems, Inc.

peu	0.0 m^2	Area dependence of EU.
eul	0.0 m^EULEXP	Length dependence coefficient of EU.
eulexp	1.0	Length dependence exponent coefficient of EU.
euw	0.0 m^EUWEXP	Width dependence coefficient of EU.
euwexp	1.0	Width dependence exponent coefficient of EU.
euwl	0.0 m^EUWLEXP	Width-length dependence coefficient of EU.
euwlexp	1.0	Width-length dependence coefficient of EU.
ud	0.001 1/m^2	Coulomb scattering parameter.
udl	0.0 m^UDLEXP	Length dependence coefficient of UD.
udlexp	1.0	Length dependence exponent coefficient of UD.
lud	0.0 m	Length dependence of UD.
wud	0.0 m	Width dependence of UD.
pud	0.0 m^2	Area dependence of UD.
udr	0.001 1/m^2	Reverse-mode Coulomb scattering parameter.
ludr	0.0 m	Length dependence of UDR.
wudr	0.0 m	Width dependence of UDR.

© 2023 Cadence Design Systems, Inc.

pudr	0.0 m^2	Area dependence of UDR.
ucs	2.0	Coulomb scattering parameter.
lucs	0.0 m	Length dependence of UCS.
wucs	0.0 m	Width dependence of UCS.
pucs	0.0 m^2	Area dependence of UCS.
ucsr	2.0	Reverse-mode Coulomb scattering parameter.
lucsr	0.0 m	Length dependence of UCSR.
wucsr	0.0 m	Width dependence of UCSR.
pucsr	0.0 m^2	Area dependence of UCSR.
uc	0.0 (m/V)^EU/V	Mobility reduction with body bias.
ucl	0.0 m^UCLEXP	Length dependence coefficient of UC.
uclexp	1.0	Length dependence exponent coefficient of UC.
ucw	0.0 m^UCWEXP	Width dependence coefficient of UC.
ucwexp	1.0	Width dependence exponent coefficient of UC.
ucwl	0.0 m^(2 UCWLEXP)	Width-length dependence coefficient of UC.
ucwlexp	1.0	Width-length dependence exponent coefficient.
luc	0.0 m (m/V)^EU/V	Length dependence of UC.

© 2023 Cadence Design Systems, Inc.

wuc	0.0 m (m/V)^EU/V	Width dependence of UC.
puc	0.0 m^2 (m/V)^EU/V	Area dependence of UC.
ucr	0.0 (m/V)^EU/V	Reverse-mode mobility reduction with body bias.
lucr	0.0 m (m/V)^EU/V	Length dependence of UCR.
wucr	0.0 m (m/V)^EU/V	Width dependence of UCR.
pucr	0.0 m^2 (m/V)^EU/V	Area dependence of UCR.
pclm	0.0	CLM pre_factor.
pclml	0.0 m^PCLMLEXP	Length dependence coefficient of PCLM.
pclmlexp	1.0	Length dependence exponent coefficient of PCLM.
lpclm	0.0 m	Length dependence of PCLM.
wpclm	0.0 m	Width dependence of PCLM.
ppclm	0.0 m^2	Area dependence of PCLM.
pclmr	0.0	Reverse-mode CLM pre-factor.

© 2023 Cadence Design Systems, Inc.

lpclmr	0.0 m	Length dependence of PCLMR.
wpclmr	0.0 m	Width dependence of PCLMR.
ppclmr	0.0 m^2	Area dependence of PCLMR.
pclmg	0.0 V	CLM pre-factor gate voltage dependence.
pclmcv	0.0	CLM parameter for C-V.
pclmcvl	0.0 m^PCLMLEXP	Length dependence coefficient of PCLMCV.
pclmcvlexp	1.0	Length dependence exponent coefficient of PCLMCV.
lpclmcv	0.0 m	Length dependence of PCLMCV.
wpclmcv	0.0 m	Width dependence of PCLMCV.
ppclmcv	0.0 m^2	Area dependence of PCLMCV.
pscbe1	4.24e8 V/m	Substrate current body-effect coefficient.
lpscbe1	0.0 V	Length dependence of PSCBE1.
wpscbe1	0.0 V	Width dependence of PSCBE1.
ppscbe1	0.0 V m	Area dependence of PSCBE1.
pscbe2	1.0e-8 m/V	Substrate current body-effect coefficient.
lpscbe2	0.0 m^2/V	Length dependence of PSCBE2.
wpscbe2	0.0 m^2/V	Width dependence of PSCBE2.

© 2023 Cadence Design Systems, Inc.

ppscbe2	0.0 m^3/V	Area dependence of PSCBE2.
pdits	0.0 1/V	Coefficient for drain-induced vth shifts.
lpdits	0.0 m/V	Length dependence of PDITS.
wpdits	0.0 m/V	Width dependence of PDITS.
ppdits	0.0 m^2/V	Area dependence of PDITS.
pditsl	0.0 1/m	L dep of drain-induced vth shifts.
pditsd	0.0 1/V	Vds dep of drain-induced vth shifts.
lpditsd	0.0 m/V	Length dependence of PDITSD.
wpditsd	0.0 m/V	Width dependence of PDITSD.
ppditsd	0.0 m^2/V	Area dependence of PDITSD.
rsh	0.0 Ω/square	Source-drain sheet resistances.
prwg	1.0 1/V	Gate bias dependence of S/D extension resistances.
lprwg	0.0 m/V	Length dependence of PRWG.
wprwg	0.0 m/V	Width dependence of PRWG.
pprwg	0.0 m^2/V	Area dependence of PRWG.
prwb	0.0 1/V	Body bias dependence of resistances.
lprwb	0.0 m/V	Length dependence of PRWB.
wprwb	0.0 m/V	Width dependence of PRWB.

© 2023 Cadence Design Systems, Inc.

pprwb	0.0 m^2/V	Area dependence of PRWB.
prwbl	0.0 m^PRWBLEXP	Length dependence coefficient of PPRWB.
prwblexp	1.0	Length dependence exponent coefficient of PPRWB.
wr	1.0	W dependence parameter of S/D extension resistances.
lwr	0.0 m	Length dependence of WR.
wwr	0.0 m	Width dependence of WR.
pwr	0.0 m^2	Area dependence of WR.
rswmin	0.0 Ω μm^WR	Source resistance per unit width at high Vgs (RDSMOD=1).
lrswmin	0.0 ohm μm^(2 WR)	Length dependence of RSWMIN.
wrswmin	0.0 ohm μm^(2 WR)	Width dependence of RSWMIN.
prswmin	0.0 ohm μm^(3 WR)	Area dependence of RSWMIN.
rsw	10.0 Ω μm^WR	Zero bias source resistance (RDSMOD=1).
lrsw	0.0 ohm μm^(2 WR)	Length dependence of RSW.

© 2023 Cadence Design Systems, Inc.

wrsw	0.0 ohm μm^(2 WR)	Width dependence of RSW.
prsw	0.0 ohm μm^(3 WR)	Area dependence of RSW.
rswl	0.0 m^RSWLEXP	Geometrical scaling of RSW (RDSMOD=1).
rswlexp	1.0	Geometrical scaling of RSW (RDSMOD=1).
rdwmin	0.0 Ω μm^WR	Drain resistance per unit width at high Vgs (RDSMOD=1).
lrdwmin	0.0 ohm μm^(2 WR)	Length dependence of RDWMIN.
wrdwmin	0.0 ohm μm^(2 WR)	Width dependence of RDWMIN.
prdwmin	0.0 ohm μm^(3 WR)	Area dependence of RDWMIN.
rdw	0.0 Ω μm^WR	Zero bias drain resistance (RDSMOD=1).
lrdw	0.0 ohm μm^(2 WR)	Length dependence of RDW.
wrdw	0.0 ohm μm^(2 WR)	Width dependence of RDW.

© 2023 Cadence Design Systems, Inc.

prdw	0.0 ohm µm^(3 WR)	Area dependence of RDW.
rdwl	0.0 m^RDWLEXP	Geometrical scaling of rdw (rdsmod=1).
rdwlexp	1.0	Geometrical scaling of rdw (rdsmod=1).
rdswmin	0.0 Ω µm^WR	S/D Resistance per unit width at high Vgs (RDSMOD=0 and RDSMOD=2).
lrdswmin	0.0 ohm µm^(2 WR)	Length dependence of RDSWMIN.
wrdswmin	0.0 ohm µm^(2 WR)	Width dependence of RDSWMIN.
prdswmin	0.0 ohm µm^(3 WR)	Area dependence of RDSWMIN.
rdsw	20.0 Ω µm^WR	Zero bias resistance (RDSMOD=0 and RDSMOD=2).
rdswl	0.0 m^RDSWLEXP	Geometrical scaling of RDSW (RDSMOD=0 and RDSMOD=2).
rdswlexp	1.0	Geometrical scaling of RDSW (RDSMOD=0 and RDSMOD=2).
lrdsw	0.0 ohm µm^(2 WR)	Length dependence of RDSW.

© 2023 Cadence Design Systems, Inc.

wrdsw	0.0 ohm µm^(2 WR)	Width dependence of RDSW.
prdsw	0.0 ohm µm^(3 WR)	Area dependence of RDSW.
psat	1.0	Gmsat variation with gate bias.
lpsat	0.0 m	Length dependence of PSAT.
wpsat	0.0 m	Width dependence of PSAT.
ppsat	0.0 m^2	Area dependence of PSAT.
psatl	0.0 m^PSATLEXP	Length dependence coefficient of PSATL.
psatlexp	1.0	Length dependence exponent coefficient of PSATLEXP.
psatb	0.0 1/V	Body bias effect on Idsat.
lpsatb	0.0 m/V	Length dependence of PSATB.
wpsatb	0.0 m/V	Width dependence of PSATB.
ppsatb	0.0 m^2/V	Area dependence of PSATB.
psatr	1.0	Reverse-mode Gmsat variation with gate bias.
lpsatr	0.0 m	Length dependence of PSATR.
wpsatr	0.0 m	Width dependence of PSATR.
ppsatr	0.0 m^2	Area dependence of PSATR.

© 2023 Cadence Design Systems, Inc.

psatx	1.0	Fine tuning of PTWG effect.
ptwg	0.0	Idsat variation with gate bias.
lptwg	0.0 m	Length dependence of PTWG.
wptwg	0.0 m	Width dependence of PTWG.
pptwg	0.0 m^2	Area dependence of PTWG.
ptwgl	0.0 m^PTWGLEXP	Length dependence coefficient of PTWG.
ptwglexp	1.0	Length dependence exponent coefficient of ptwg.
ptwgr	0.0	Reverse-mode Idsat variation with gate bias.
lptwgr	0.0 m	Length dependence of PTWGR.
wptwgr	0.0 m	Width dependence of PTWGR.
pptwgr	0.0 m^2	Area dependence of PTWGR.
ptwglr	0.0 m^PTWGLEXPR	Length dependence coefficient of PTWGR.
ptwglexpr	1.0	Length dependence exponent coefficient of PTWGR.
a1	0.0 $1/V^2$	Non-saturation effect parameter for strong inversion region.
la1	0.0 m/V^2	Length dependence of A1.
wa1	0.0 m/V^2	Width dependence of A1.

© 2023 Cadence Design Systems, Inc.

pa1	0.0 m^2/V^2	Area dependence of A1.
a11	0.0	Temperature dependence of A1.
la11	0.0 m	Length dependence of A11.
wa11	0.0 m	Width dependence of A11.
pa11	0.0 m^2	Area dependence of A11.
a2	0.0 1/V	Non-saturation effect parameter for moderate inversion region.
la2	0.0 m/V	Length dependence of A2.
wa2	0.0 m/V	Width dependence of A2.
pa2	0.0 m^2/V	Area dependence of A2.
a21	0.0	Temperature dependence of A2.
la21	0.0 m	Length dependence of A21.
wa21	0.0 m	Width dependence of A21.
pa21	0.0 m^2	Area dependence of A21.
pdiblc	0.0	Parameter for DIBL effect on rout.
pdiblc1	0.0 m^PDIBLCLEXP	Length dependence coefficient of PDIBLC.
pdiblc1exp	1.0	Length dependence exponent coefficient of PDIBLC.
lpdiblc	0.0 m	Length dependence of PDIBLC.

© 2023 Cadence Design Systems, Inc.

wpdiblc	0.0 m	Width dependence of PDIBLC.
ppdiblc	0.0 m^2	Area dependence of PDIBLC.
pdiblcr	0.0	Reverse-mode parameter for DIBL effect on rout.
pdiblclr	0.0 m^PDIBLCLEXPR	Length dependence coefficient of pdiblcr.
pdiblclexpr	1.0	Length dependence exponent coefficient of pdiblcr.
lpdiblcr	0.0 m	Length dependence of PDIBLCR.
wpdiblcr	0.0 m	Width dependence of PDIBLCR.
ppdiblcr	0.0 m^2	Area dependence of PDIBLCR.
pdiblcb	0.0 1/V	Parameter for DIBL effect on rout.
lpdiblcb	0.0 m/V	Length dependence of PDIBLCB.
wpdiblcb	0.0 m/V	Width dependence of PDIBLCB.
ppdiblcb	0.0 m^2/V	Area dependence of PDIBLCB.
pvag	1.0	Vg dependence of EARLY voltage.
lpvag	0.0 m	Length dependence of PVAG.
wpvag	0.0 m	Width dependence of PVAG.
ppvag	0.0 m^2	Area dependence of PVAG.
fprout	0.0 V/m^0.5	Gds degradation factor due to pocket implants.

© 2023 Cadence Design Systems, Inc.

fproutl	0.0 m^FPROUT LEXP	Length dependence coefficient of fprout.
fproutlexp	1.0	Length dependence exponent coefficient of FPROUT.
lfprout	0.0 V m^0.5	Length dependence of FPROUT.
wfprout	0.0 V m^0.5	Width dependence of FPROUT.
pfprout	0.0 V m^1.5	Area dependence of FPROUT.
alpha0	0.0 m/V	First parameter of Iii.
alpha0l	0.0 m^ALPHA0 LEXP	Length dependence coefficient of ALPHA0.
alpha0lexp	1.0	Length dependence exponent coefficient of ALPHA0.
lalpha0	0.0 m^2/V	Length dependence of ALPHA0.
walpha0	0.0 m^2/V	Width dependence of ALPHA0.
palpha0	0.0 m^3/V	Area dependence of ALPHA0.
beta0	0.0 1/V	Vds dependent parameter of Iii.
lbeta0	0.0 m/V	Length dependence of BETA0.
wbeta0	0.0 m/V	Width dependence of BETA0.
pbeta0	0.0 m^2/V	Area dependence of BETA0.

© 2023 Cadence Design Systems, Inc.

aigbacc	1.36e-2 (F s^2/ g)^0.5/m	Parameter for Igb in accumulation.
bigbacc	1.71e-3 (F s^2/ g)^0.5/ m/V	Parameter for Igb in accumulation.
cigbacc	0.075 1/ V	Parameter for Igb in accumulation.
nigbacc	1.0	Parameter for Igbacc slope.
aigbinv	1.11e-2 (F s^2/ g)^0.5/m	Parameter for Igb in inversion.
bigbinv	9.49e-4 (F s^2/ g)^0.5/ m/V	Parameter for Igb in inversion.
cigbinv	0.006 1/ V	Parameter for Igb in inversion.
eigbinv	1.1 V	Parameter for the Si bandgap for Igbinv.
nigbinv	3.0	Parameter for Igbinv slope.
aigc	1.36e-2 (F s^2/ g)^0.5/m	Parameter for Igc.
bigc	1.71e-3 (F s^2/ g)^0.5/ m/V	Parameter for Igc.

© 2023 Cadence Design Systems, Inc.

cigc	0.075 1/V	Parameter for Igc.
aigs	1.36e-2 (F s^2/g)^0.5/m	Parameter for Igs.
bigs	1.71e-3 (F s^2/g)^0.5/m/V	Parameter for Igs.
cigs	0.075 1/V	Parameter for Igs.
aigd	1.36e-2 (F s^2/g)^0.5/m	Parameter for Igd.
bigd	1.71e-3 (F s^2/g)^0.5/m/V	Parameter for Igd.
cigd	0.075 1/V	Parameter for Igd.
dlcig	0.0 m	Delta L for Ig model.
dlcigd	0.0 m	Delta L for Ig model.
poxedge	1.0	Factor for the gate edge tox.
ntox	1.0	Exponent for tox ratio.
toxref	3.0e-9 m	Target tox value.
pigcd	1.0	Igc, S/D partition parameter.

© 2023 Cadence Design Systems, Inc.

aigcl	0.0 m	Length dependence coefficient of aigc.
aigcw	0.0 m	Width dependence coefficient of aigc.
aigsl	0.0 m	Length dependence coefficient of aigs.
aigsw	0.0 m	Width dependence coefficient of aigs.
aigdl	0.0 m	Length dependence coefficient of aigd.
aigdw	0.0 m	Width dependence coefficient of aigd.
pigcdl	0.0 m	Length dependence coefficient of pigcd.
laigbinv	0.0 (F s^2/ g)^0.5	Length dependence of AIGBINV.
waigbinv	0.0 (F s^2/ g)^0.5	Width dependence of AIGBINV.
paigbinv	0.0 m (F s^2/ g)^0.5	Area dependence of AIGBINV.
lbigbinv	0.0 (F s^2/ g)^0.5/V	Length dependence of BIGBINV.
wbigbinv	0.0 (F s^2/ g)^0.5/V	Width dependence of BIGBINV.
pbigbinv	0.0 m (F s^2/ g)^0.5/V	Area dependence of BIGBINV.
lcigbinv	0.0 m/V	Length dependence of CIGBINV.

© 2023 Cadence Design Systems, Inc.

wcigbinv	0.0 m/V	Width dependence of CIGBINV.
pcigbinv	0.0 m^2/V	Area dependence of CIGBINV.
leigbinv	0.0 m V	Length dependence of EIGBINV.
weigbinv	0.0 m V	Width dependence of EIGBINV.
peigbinv	0.0 m^2 V	Area dependence of EIGBINV.
lnigbinv	0.0 m	Length dependence of NIGBINV.
wnigbinv	0.0 m	Width dependence of NIGBINV.
pnigbinv	0.0 m^2	Area dependence of NIGBINV.
laigbacc	0.0 (F s^2/ g)^0.5	Length dependence of AIGBACC.
waigbacc	0.0 (F s^2/ g)^0.5	Width dependence of AIGBACC.
paigbacc	0.0 m (F s^2/ g)^0.5	Area dependence of AIGBACC.
lbigbacc	0.0 (F s^2/ g)^0.5/V	Length dependence of BIGBACC.
wbigbacc	0.0 (F s^2/ g)^0.5/V	Width dependence of BIGBACC.
pbigbacc	0.0 m (F s^2/ g)^0.5/V	Area dependence of BIGBACC.

© 2023 Cadence Design Systems, Inc.

lcigbacc	0.0 m/V	Length dependence of CIGBACC.
wcigbacc	0.0 m/V	Width dependence of CIGBACC.
pcigbacc	0.0 m^2/V	Area dependence of CIGBACC.
lnigbacc	0.0 m	Length dependence of NIGBACC.
wnigbacc	0.0 m	Width dependence of NIGBACC.
pnigbacc	0.0 m^2	Area dependence of NIGBACC.
laigc	0.0 (F s^2/ g)^0.5	Length dependence of AIGC.
waigc	0.0 (F s^2/ g)^0.5	Width dependence of AIGC.
paigc	0.0 m (F s^2/ g)^0.5	Area dependence of AIGC.
lbigc	0.0 (F s^2/ g)^0.5/V	Length dependence of BIGC.
wbigc	0.0 (F s^2/ g)^0.5/V	Width dependence of BIGC.
pbigc	0.0 m (F s^2/ g)^0.5/V	Area dependence of BIGC.
lcigc	0.0 m/V	Length dependence of CIGC.
wcigc	0.0 m/V	Width dependence of CIGC.

© 2023 Cadence Design Systems, Inc.

pcigc	0.0 m^2/V	Area dependence of CIGC.
laigs	0.0 ($F s^2/g$)^0.5	Length dependence of AIGS.
waigs	0.0 ($F s^2/g$)^0.5	Width dependence of AIGS.
paigs	0.0 m ($F s^2/g$)^0.5	Area dependence of AIGS.
lbigs	0.0 ($F s^2/g$)^0.5/V	Length dependence of BIGS.
wbigs	0.0 ($F s^2/g$)^0.5/V	Width dependence of BIGS.
pbigs	0.0 m ($F s^2/g$)^0.5/V	Area dependence of BIGS.
lcigs	0.0 m/V	Length dependence of CIGS.
wcigs	0.0 m/V	Width dependence of CIGS.
pcigs	0.0 m^2/V	Area dependence of CIGS.
laigd	0.0 ($F s^2/g$)^0.5	Length dependence of AIGD.
waigd	0.0 ($F s^2/g$)^0.5	Width dependence of AIGD.

© 2023 Cadence Design Systems, Inc.

paigd	0.0 m (F s^2/ g)^0.5	Area dependence of AIGD.
lbigd	0.0 (F s^2/ g)^0.5/V	Length dependence of BIGD.
wbigd	0.0 (F s^2/ g)^0.5/V	Width dependence of BIGD.
pbigd	0.0 m (F s^2/ g)^0.5/V	Area dependence of BIGD.
lcigd	0.0 m/V	Length dependence of CIGD.
wcigd	0.0 m/V	Width dependence of CIGD.
pcigd	0.0 m^2/V	Area dependence of CIGD.
lpoxedge	0.0 m	Length dependence of POXEDGE.
wpoxedge	0.0 m	Width dependence of POXEDGE.
ppoxedge	0.0 m^2	Area dependence of POXEDGE.
ldlcig	0.0 m^2	Length dependence of DLCIG.
wdlcig	0.0 m^2	Width dependence of DLCIG.
pdlcig	0.0 m^3	Area dependence of DLCIG.
ldlcigd	0.0 m^2	Length dependence of DLCIGD.
wdlcigd	0.0 m^2	Width dependence of DLCIGD.
pdlcigd	0.0 m^3	Area dependence of DLCIGD.

© 2023 Cadence Design Systems, Inc.

lntox	0.0 m	Length dependence of NTOX.
wntox	0.0 m	Width dependence of NTOX.
pntox	0.0 m^2	Area dependence of NTOX.
agidl	0.0 V/m	Pre-exponential coefficient for GIDL.
agidll	0.0 m	Length dependence coefficient of agidl.
agidlw	0.0 m	Width dependence coefficient of agidl.
lagidl	0.0 m^2	Length dependence of AGIDL.
wagidl	0.0 m^2	Width dependence of AGIDL.
pagidl	0.0 m^3	Area dependence of AGIDL.
bgidl	2.3e9 V/m	Exponential coefficient for GIDL.
lbgidl	0.0 V	Length dependence of BGIDL.
wbgidl	0.0 V	Width dependence of BGIDL.
pbgidl	0.0 V m	Area dependence of BGIDL.
cgidl	0.5 V/m	Parameter for body-bias effect on GIDL.
lcgidl	0.0 V	Length dependence of CGIDL.
wcgidl	0.0 V	Width dependence of CGIDL.
pcgidl	0.0 V m	Area dependence of CGIDL.
egidl	0.8 V	Band bending parameter for GIDL.
legidl	0.0 V m	Length dependence of EGIDL.

© 2023 Cadence Design Systems, Inc.

wegidl	0.0 V m	Width dependence of EGIDL.
pegidl	0.0 V m^2	Area dependence of EGIDL.
agisl	0.0 V/m	Pre-exponential coefficient for GISL.
agisll	0.0 m	Length dependence coefficient of agisl.
agislw	0.0 m	Width dependence coefficient of agisl.
lagisl	0.0 m^2	Length dependence of AGISL.
wagisl	0.0 m^2	Width dependence of AGISL.
pagisl	0.0 m^3	Area dependence of AGISL.
bgisl	2.3e9 V/m	Exponential coefficient for GISL.
lbgisl	0.0 V	Length dependence of BGISL.
wbgisl	0.0 V	Width dependence of BGISL.
pbgisl	0.0 V m	Area dependence of BGISL.
cgisl	0.5 V^3	Parameter for body-bias effect on GISL.
lcgisl	0.0 V	Length dependence of CGISL.
wcgisl	0.0 V	Width dependence of CGISL.
pcgisl	0.0 V m	Area dependence of CGISL.
egisl	0.8 V	Fitting parameter for band bending for GISL.
legisl	0.0 V m	Length dependence of EGISL.
wegisl	0.0 V m	Width dependence of EGISL.

© 2023 Cadence Design Systems, Inc.

pegisl	0.0 V m^2	Area dependence of EGISL.
cf	0.0 F/m	Outer fringe capacitance.
lcf	0.0 F	Length dependence of CF.
wcf	0.0 F	Width dependence of CF.
pcf	0.0 F m	Area dependence of CF.
cfrcoeff	1.0 F/m	Coefficient for outer fringe capacitance.
cgso	0.0 F/m	Gate-to-source overlap capacitance.
cgdo	0.0 F/m	Gate-to-drain overlap capacitance.
cgbo	0.0 F/m	Gate-to-body overlap capacitance.
cgsl	0.0 F/m	Overlap capacitance between gate and lightly-doped source region.
lcgsl	0.0	Length dependence of CGSL.
wcgsl	0.0	Width dependence of CGSL.
pcgsl	0.0	Area dependence of CGSL.
cgdl	0.0 F/m	Overlap capacitance between gate and lightly-doped drain region.
lcgdl	0.0 F	Length dependence of CGDL.
wcgdl	0.0 F	Width dependence of CGDL.
pcgdl	0.0 F m	Area dependence of CGDL.
ckappas	0.6 V	Coefficient of bias-dependent overlap capacitance for the source side.

© 2023 Cadence Design Systems, Inc.

lckappas	0.0 m V	Length dependence of CKAPPAS.
wckappas	0.0 m V	Width dependence of CKAPPAS.
pckappas	0.0 m^2 V	Area dependence of CKAPPAS.
ckappad	0.6 V	Coefficient of bias-dependent overlap capacitance for the source side.
lckappad	0.0 m V	Length dependence of CKAPPAD.
wckappad	0.0 m V	Width dependence of CKAPPAD.
pckappad	0.0 m^2 V	Area dependence of CKAPPAD.
ckappad1	1.0e6	Parameter for tuning CGD.
ckappad2	1.0	Parameter for tuning CGD.
ckappas1	1.0e6	Parameter for tuning CGD.
ckappas2	1.0	Parameter for tuning CGD.
dmcg	0.0 m	Distance of mid-contact to gate edge.
dmci	0.0 m	Distance of mid-contact to isolation.
dmdg	0.0 m	Distance of mid-diffusion to gate edge.
dmcgt	0.0 m	Distance of mid-contact to gate edge in test.
xgl	0.0 m	Variation in Ldrawn.
rshg	0.1 Ω	Gate sheet resistance.
cjs	5.0e-4 F/m^2	Unit area source-side junction capacitance at zero bias.

© 2023 Cadence Design Systems, Inc.

cjd	5.0e-4 F/m^2	Unit area drain-side junction capacitance at zero bias.
cjsws	5.0e-10 F/m	Unit length source-side side-wall junction capacitance at zero bias.
cjswd	5.0e-10 F/m	Unit length drain-side side-wall junction capacitance at zero bias.
cjswgs	0.0 F/m	Unit length source-side gate side-wall junction capacitance at zero bias.
cjswgd	0.0 F/m	Unit length drain-side gate side-wall junction capacitance at zero bias.
pbs	1.0 V	Source-side bulk junction built-in potential.
pbd	1.0 V	Drain-side bulk junction built-in potential.
pbsws	1.0 V	Built-in potential for Source-side side-wall junction capacitance.
pbswd	1.0 V	Built-in potential for Drain-side side-wall junction capacitance.
pbswgs	1.0 V	Built-in potential for Source-side gate side-wall junction capacitance.
pbswgd	1.0 V	Built-in potential for Drain-side gate side-wall junction capacitance.
mjs	0.5	Source bottom junction capacitance grading coefficient.
mjd	0.5	Drain bottom junction capacitance grading coefficient.
mjsws	0.33	Source side-wall junction capacitance grading coefficient.

© 2023 Cadence Design Systems, Inc.

mjswd	0.33	Drain side-wall junction capacitance grading coefficient.
mjswgs	0.33	Source-side gate side-wall junction capacitance grading coefficient.
mjswgd	0.33	Drain-side gate side-wall junction capacitance grading coefficient.
jss	1.0e-4 A/m^2	Bottom source junction reverse saturation current density.
jsd	1.0e-4 A/m^2	Bottom drain junction reverse saturation current density.
jsws	0.0 A/m	Unit length reverse saturation current for side-wall source junction.
jswd	0.0 A/m	Unit length reverse saturation current for side-wall drain junction.
jswgs	0.0 A/m	Unit length reverse saturation current for gate-edge side-wall source junction.
jswgd	0.0 A/m	Unit length reverse saturation current for gate-edge side-wall drain junction.
njs	1.0	Source junction emission coefficient.
njd	1.0	Drain junction emission coefficient.
ijthsfwd	0.1 A	Forward source diode breakdown limiting current.
ijthdfwd	0.1 A	Forward drain diode breakdown limiting current.
ijthsrev	0.1 A	Reverse source diode breakdown limiting current.
ijthdrev	0.1 A	Reverse drain diode breakdown limiting current.

© 2023 Cadence Design Systems, Inc.

bvs	10.0 V	Source diode breakdown voltage.
bvd	10.0 V	Drain diode breakdown voltage.
xjbvs	1.0	Fitting parameter for source diode breakdown current.
xjbvd	1.0	Fitting parameter for drain diode breakdown current.
jtss	0.0 A/m	Bottom source junction trap-assisted saturation current density.
jtsd	0.0 A/m	Bottom drain junction trap-assisted saturation current density.
jtssws	0.0 A/m^2	Unit length trap-assisted saturation current for side-wall source junction.
jtsswd	0.0 A/m^2	Unit length trap-assisted saturation current for side-wall drain junction.
jtsswgs	0.0 A/m	Unit length trap-assisted saturation current for gate-edge side-wall source junction.
jtsswgd	0.0 A/m	Unit length trap-assisted saturation current for gate-edge side-wall drain junction.
jtweff	0.0 m	Trap assisted tunneling current width dependence.
njts	20.0	Non-ideality factor for jtss.
njtsd	20.0	Non-ideality factor for jtsd.
njtssw	20.0	Non-ideality factor for jtssws.
njtsswd	20.0	Non-ideality factor for jtsswd.
njtsswg	20.0	Non-ideality factor for jtsswgs.

© 2023 Cadence Design Systems, Inc.

njtsswgd	20.0	Non-ideality factor for jtsswgd.
vtss	10.0 V	Bottom source junction trap-assisted current voltage dependent parameter.
vtsd	10.0 V	Bottom drain junction trap-assisted current voltage dependent parameter.
vtssws	10.0 V	Unit length trap-assisted current voltage dependent parameter for side-wall source junction.
vtsswd	10.0 V	Unit length trap-assisted current voltage dependent parameter for side-wall drain junction.
vtsswgs	10.0 V	Unit length trap-assisted current voltage dependent parameter for gate-edge side-wall source junction.
vtsswgd	10.0 V	Unit length trap-assisted current voltage dependent parameter for gate-edge side-wall drain junction.
xrcrg1	12.0	1st fitting parameter for the bias-dependent Rg.
xrcrg2	1.0	2nd fitting parameter for the bias-dependent Rg.
gbmin	1.0e-12 1/Ω	Minimum body conductance.
rbps0	50.0 Ω	Scaling pre-factor for RBPS.
rbpsl	0.0	Length scaling parameter for RBPS.
rbpsw	0.0	Width scaling parameter for RBPS.
rbpsnf	0.0	Number of fingers scaling parameter for RBPS.
rbpd0	50.0 Ω	Scaling pre-factor for RBPD.
rbpdl	0.0	Length scaling parameter for rbpd.

© 2023 Cadence Design Systems, Inc.

rbpdw	0.0	Width scaling parameter for RBPD.
rbpdnf	0.0	Number of fingers scaling parameter for RBPD.
rbpbx0	100.0 Ω	Scaling pre-factor for RBPBX.
rbpbxl	0.0	Length scaling parameter for RBPBX.
rbpbxw	0.0	Width scaling parameter for RBPBX.
rbpbxnf	0.0	Number of fingers scaling parameter for RBPBX.
rbpby0	100.0 Ω	Scaling pre-factor for RBPBY.
rbpbyl	0.0	Length scaling parameter for RBPBY.
rbpbyw	0.0	Width scaling parameter for RBPBY.
rbpbynf	0.0	Number of fingers scaling parameter for RBPBY.
rbsbx0	100.0 Ω	Scaling pre-factor for RBSBX.
rbsby0	100.0 Ω	Scaling pre-factor for RBSBY.
rbdbx0	100.0 Ω	Scaling pre-factor for RBDBX.
rbdby0	100.0 Ω	Scaling pre-factor for RBDBY.
rbsdbxl	0.0	Length scaling parameter for RBSBX and RBDBX.
rbsdbxw	0.0	Width scaling parameter for RBSBX and RBDBX.
rbsdbxnf	0.0	Number of fingers scaling parameter for RBSBX and RBDBX.
rbsdbyl	0.0	Length scaling parameter for RBSBY and RBDBY.
rbsdbyw	0.0	Width scaling parameter for RBSBY and RBDBY.

© 2023 Cadence Design Systems, Inc.

rbsdbynf	0.0	Number of fingers scaling parameter for RBSBY and RBDBY.
ef	1.0	Flicker noise frequency exponent.
em	4.1e7 V/m	Saturation field.
noia	6.250e40 s^(1-EF)/(eV)^1/m^3	Flicker noise parameter A.
noib	3.125e25 s^(1-EF)/(eV)^1/m	Flicker noise parameter B.
noic	8.750e8 s^(1-EF) m/(eV)^1	Flicker noise parameter C.
lintnoi	0.0 m	Length reduction parameter offset.
ntnoi	1.0	Noise factor for short-channel devices for TNOIMOD=0 only.
rnoia	0.577	Noise parameter for TNOIMOD = 1.
rnoib	0.5164	Noise parameter for TNOIMOD = 1.
rnoic	0.395	Noise parameter for TNOIMOD = 1.
tnoia	0.0	Noise parameter for TNOIMOD = 1. the default value has been changed to 1.5 since v107.0..
tnoib	0.0	Noise parameter for TNOIMOD = 1. the default value has been changed to 3.5 since v107.0..

© 2023 Cadence Design Systems, Inc.

tnoic	0.0	Noise correlation coefficient for TNOIMOD = 1.
binunit	1	Unit of L and W for Binning. 1: micro-meter, 0: default.
dlbin	0.0	Length reduction parameter for binning.
dwbin	0.0	Width reduction parameter for binning.
tnom	27.0 C	Temperature at which the model was extracted.
tbgasub	4.73e-4 eV/K	Bandgap temperature coefficient.
tbgbsub	636.0 K	Bandgap temperature coefficient.
tnfactor	0.0	Temperature exponent for nfactor.
ute	(-1.5)	Mobility temperature exponent.
lute	0.0 m	Length dependence of UTE.
wute	0.0 m	Width dependence of UTE.
pute	0.0 m^2	Area dependence of UTE.
utel	0.0 m	Length scaling parameter for UTE.
ua1	1.0e-3 m/V	Temperature coefficient for UA.
lua1	0.0 m^2/V	Length dependence of UA1.
wua1	0.0 m^2/V	Width dependence of UA1.
pua1	0.0 m^3/V	Area dependence of UA1.
ua1l	0.0 m	Length scaling parameter for UA1.

© 2023 Cadence Design Systems, Inc.

uc1	0.056e-9 1/K	Temperature coefficient for UC.
luc1	0.0 m/K	Length dependence of UC1.
wuc1	0.0 m/K	Width dependence of UC1.
puc1	0.0 m^2/K	Area dependence of UC1.
ud1	0.0 1/m^2	Temperature coefficient for ud.
lud1	0.0 1/m	Length dependence of UD1.
wud1	0.0 1/m	Width dependence of UD1.
pud1	0.0	Area dependence of UD1.
ud1l	0.0 m	Length scaling parameter for UD1.
ucste	(-4.775e-3)	Temperature coefficient for UCS.
lucste	0.0 m	Length dependence of UCSTE.
wucste	0.0 m	Width dependence of UCSTE.
pucste	0.0 m^2	Area dependence of UCSTE.
teta0	0.0	Temperature coefficient for eta0.
prt	0.0 Ω m	Temperature coefficient for resistance.
lprt	0.0 m	Length dependence of PRT.
wprt	0.0 m	Width dependence of PRT.
pprt	0.0 m^2	Area dependence of PRT.

© 2023 Cadence Design Systems, Inc.

at	(-1.56e-3) m/s	Temperature coefficient for saturation velocity.
lat	0.0 m^2/s	Length dependence of AT.
wat	0.0 m^2/s	Width dependence of AT.
pat	0.0 m^3/s	Area dependence of AT.
atl	0.0 m	Length Scaling parameter for AT.
tdelta	0.0 1/K	Temperature coefficient for DELTA.
ptwgt	0.0 1/K	Temperature coefficient for PTWG.
lptwgt	0.0 m/K	Length dependence of PTWGT.
wptwgt	0.0 m/K	Width dependence of PTWGT.
pptwgt	0.0 m^2/K	Area dependence of PTWGT.
ptwgtl	0.0 m	Length scaling parameter for ptwgt.
kt1	(-0.11) V	Temperature coefficient for vth.
kt1exp	1.0	Temperature coefficient for Vth.
kt11	0.0 V m	Temperature coefficient for vth.
lkt1	0.0 V m	Length dependence of KT1.
wkt1	0.0 V m	Width dependence of KT1.
pkt1	0.0 V m^2	Area dependence of KT1.
kt2	0.022	Temperature coefficient for Vth.

© 2023 Cadence Design Systems, Inc.

lkt2	0.0 m	Length dependence of KT2.
wkt2	0.0 m	Width dependence of KT2.
pkt2	0.0 m^2	Area dependence of KT2.
iit	0.0	Temperature coefficient for BETA0.
liit	0.0 m	Length dependence of IIT.
wiit	0.0 m	Width dependence of IIT.
piit	0.0 m^2	Area dependence of IIT.
igt	2.5	Gate current temperature dependence.
ligt	0.0 m	Length dependence of IGT.
wigt	0.0 m	Width dependence of IGT.
pigt	0.0 m^2	Area dependence of IGT.
tgidl	0.0 1/K	Temperature coefficient for GIDL/GISL.
ltgidl	0.0 m/K	Length dependence of TGIDL.
wtgidl	0.0 m/K	Width dependence of TGIDL.
ptgidl	0.0 m^2/K	Area dependence of TGIDL.
tcj	0.0 1/K	Temperature coefficient for cjs/cjd.
tcjsw	0.0 1/K	Temperature coefficient for cjsws/cjswd.
tcjswg	0.0 1/K	Temperature coefficient for cjswgs/cjswgd.
tpb	0.0 V/K	Temperature coefficient for pbs/pbd.

© 2023 Cadence Design Systems, Inc.

tpbsw	0.0 V/K	Temperature coefficient for pbsws/pbswd.
tpbswg	0.0 V/K	Temperature coefficient for pbswgs/pbswgd.
xtis	3.0	Source junction current temperature exponent.
xtid	3.0	Drain junction current temperature exponent.
xtss	0.02	Power dependence of JTSS on temperature.
xtsd	0.02	Power dependence of JTSD on temperature.
xtssws	0.02	Power dependence of JTSSWS on temperature.
xtsswd	0.02	Power dependence of JTSSWD on temperature.
xtsswgs	0.02	Power dependence of JTSSWGS on temperature.
xtsswgd	0.02	Power dependence of JTSSWGD on temperature.
tnjts	0.0	Temperature coefficient for njts.
tnjtsd	0.0	Temperature coefficient for njtsd.
tnjtssw	0.0	Temperature coefficient for njtssw.
tnjtsswd	0.0	Temperature coefficient for njtsswd.
tnjtsswg	0.0	Temperature coefficient for njtsswg.
tnjtsswgd	0.0	Temperature coefficient for njtsswgd.
rth0	0.0 m K/W	Thermal resistance.
cth0	1.0e-5 s W/(m K)	Thermal capacitance.

© 2023 Cadence Design Systems, Inc.

wth0	0.0 m	Width dependence coefficient for Rth and Cth.
saref	1.0e-6 m	Reference distance between OD edge from Poly from one side.
sbref	1.0e-6 m	Reference distance between OD edge from Poly from other side.
wlod	0.0 m	Width parameter for stress effect.
ku0	0.0 m	Mobility degradation/enhancement parameter for stress effect.
kvsat	0.0 m	Saturation velocity degradation/enhancement parameter for stress effect.
tku0	0.0	Temperature coefficient for ku0.
lku0	0.0 m^LLODKU0	Length dependence of KU0.
wku0	0.0 m^WLODKU0	Width dependence of KU0.
pku0	0.0 m^(LLODKU0+WLODKU0)	Cross-term dependence of KU0.
llodku0	0.0	Length parameter for U0 stress effect.
wlodku0	0.0	Width parameter for U0 stress effect.
kvth0	0.0 V m	Threshold shift parameter for stress effect.

© 2023 Cadence Design Systems, Inc.

lkvth0	0.0 m^LLODKU0	Length dependence of KVTH0.
wkvth0	0.0 m^WLODKU0	Width dependence of KVTH0.
pkvth0	0.0 m^(LLODKU0+WLODKU0)	Cross-term dependence of KVTH0.
llodvth	0.0	Length parameter for vth stress effect.
wlodvth	0.0	Width parameter for vth stress effect.
stk2	0.0 m	K2 shift factor related to vth change.
lodk2	0.0	K2 shift modification factor for stress effect.
steta0	0.0 m	ETA0 shift related to vth0 change.
lodeta0	0.0	ETA0 modification foator for stress effect.
web	0.0	Coefficient for SCB (> 0).
wec	0.0	Coefficient for SCC (> 0).
kvth0we	0.0 V	Threshold shift factor for well proximity effect.
lkvth0we	0.0 m	Length dependence of KVTH0WE.
wkvth0we	0.0 m	Width dependence of KVTH0WE.
pkvth0we	0.0 m^2	Area dependence of KVTH0WE.
k2we	0.0	K2 shift factor for well proximity effect.

© 2023 Cadence Design Systems, Inc.

lk2we	0.0 m	Length dependence of K2WE.
wk2we	0.0 m	Width dependence of K2WE.
pk2we	0.0 m^2	Area dependence of K2WE.
ku0we	0.0	Mobility degradation factor for well proximity effect.
lku0we	0.0 m	Length dependence of KU0WE.
wku0we	0.0 m	Width dependence of KU0WE.
pku0we	0.0 m^2	Area dependence of KU0WE.
scref	1.0e-6 m	Reference distance to calculate SCA,SCB and SCC (< 0).
edgefet	1	0: Edge FET Model OFF, 1: Edge FET Model ON.
wedge	10.0e-9 m	Edge FET width.
lwedge	0.0 m^2	Length dependence of WEDGE.
wwedge	0.0 m^2	Width dependence of WEDGE.
pwedge	0.0 m^3	Area dependence dependence of WEDGE.
dgammaedge	0.0	Different in body-bias coefficient between Edge-FET and Main-FET.
ldgammaedge	0.0 m	Length dependence of DGAMMAEDGE.
wdgammaedge	0.0 m	Width dependence of DGAMMAEDGE.
pdgammaedge	0.0 m^2	Area dependence dependence of DGAMMAEDGE.
dgammaedgel	0.0	L dependence parameter for DGAMMA.

© 2023 Cadence Design Systems, Inc.

dgammaedgelexp	1.0	Exponent of L dependence parameter for DGAMMA.
dvtedge	0.0	Vth shift for Edge FET.
ldvtedge	0.0 m	Length dependence of DVTEDGE.
wdvtedge	0.0 m	Width dependence of DVTEDGE.
pdvtedge	0.0 m^2	Area dependence dependence of DVTEDGE.
nfactoredge	0.0	NFACTOR for Edge FET.
citedge	0.0 F/m^2	CIT for Edge FET.
cdscdedge	1e-9 $F/m^2/V$	CDSCD for Edge FET.
cdscbedge	0.0 $F/m^2/V$	CDSCB for Edge FET.
eta0edge	0.08	DIBL parameter for edge FET.
etabedge	(-0.07) 1/V	ETAB for edge FET.
kt1edge	(-0.11) V	Temperature dependence parameter of threshold voltage for edge FET.
kt1ledge	0.0 V m	Temperature dependence parameter of threshold voltage for edge FET.
kt2edge	0.022	Temperature dependence parameter of threshold voltage for edge FET.
kt1expedge	1.0	Temperature dependence parameter of threshold voltage for edge device.

© 2023 Cadence Design Systems, Inc.

tnfactoredge	0.0	Temperature dependence parameter of subthreshold slope factor for edge.
teta0edge	0.0	Temperature dependence parameter of DIBL parameter for edge FET.
dvt0edge	2.2	First coefficient of SCE effect on Vth for Edge FET.
dvt1edge	0.53	Second coefficient of SCE effect on Vth for Edge FET.
dvt2edge	0.0 1/V	Body-bias coefficient for SCE effect for Edge FET.
noisemethod	option noisemethod	1:subckt; 0:noign.
geomod	0	Geometry-dependent parasitics model.
rgeomod	0	Geometry-dependent source/drain resistance. 0: RSH-based, 1: Holistic.
rgatemod	0	Gate resistance model selector.
rbodymod	0	Distributed body R model.
l	1.0e-5 m	Default channel length.
w	1.0e-5 m	Default total width including fingers.
nf	1	Number of fingers. It serves as the default value of instance nf.
dtemp	0.0 C	Offset of device temperature.
delvto	0.0	Zero bias threshold voltage variation.
ids0mult	1.0	Variability in drain current for miscellaneous reasons.

© 2023 Cadence Design Systems, Inc.

lmin	0.0 m	Minimum channel length for which the model is valid.
lmax	1.0 m	Maximum channel length for which the model is valid.
wmin	0.0 m	Minimum channel width for which the model is valid.
wmax	1.0 m	Maximum channel width for which the model is valid.
vds_max	infinity V	Maximum allowed voltage across source and drain.
vgd_max	infinity V	Maximum allowed voltage across drain and gate.
vgs_max	infinity V	Maximum allowed voltage across source/bulk and gate.
vbd_max	infinity V	Maximum allowed voltage across drain/source and bulk.
vbs_max	infinity V	Maximum allowed voltage across source and bulk.
vgb_max	infinity V	Maximum allowed voltage across gate and bulk.
vgdr_max	infinity V	Maximum allowed reverse voltage across gate and drain.
vgsr_max	infinity V	Maximum allowed reverse voltage across gate and source.
vgbr_max	infinity V	Maximum allowed reverse voltage across gate and bulk.
vbsr_max	infinity V	Maximum allowed reverse voltage across bulk and source.

© 2023 Cadence Design Systems, Inc.

vbdr_max	infinity V	Maximum allowed reverse voltage across bulk and drain.
vfbsdoff	0.0	S/D flatband voltage offset.
rbpb	50.0 Ω	Resistance between bNodePrime and bNode.
rbdb	50.0 Ω	Resistance between bNode and dbNode.
rbsb	50.0 Ω	Resistance between bNode and sbNode.
rbps	50.0 Ω	Resistance between bNodePrime and sbNode.
rbpd	50.0 Ω	Resistance between bNodePrime and bNode.
ngcon	1	Number of gate contacts.
mvtwl	0.0 V m	Threshold mismatch area dependence.
mvtwl2	0.0 V m^1.5	Threshold mismatch area square dependence.
mvt0	0.0 V	Threshold mismatch intercept.
mbewl	0.0 m	Beta mismatch area dependence.
mbe0	0.0	Beta mismatch intercept.
mismatchmod	0	Select mismatch mode. The available modes are 0, 1, 2 and 3.
mismatchdist	0.0	Mismatch Distance.
igclamp	1	Model flag for Ig clamping.
gkinkmod	1	Model flag.
vdsxmod	1	Model flag.

© 2023 Cadence Design Systems, Inc.

avdsx	20	Smoothing parameter in Vdsx in Vbsx.
rnoik	0.0	Exponential coeff. for enhanced correlated thermal noise.
tnoik	1.0	Exponential coeff. for enhanced correlated thermal noise.
retacvd	0.0	The impact of Vds on vgfbCV.
lretacvd	0.0	Length dependence of RETACVD.
wretacvd	0.0	Width dependence of RETACVD.
pretacvd	0.0	Area dependence of RETACVD.
retacvd1	0.0	Temperature coefficient for RETACVD.
lretacvd1	0.0	Length dependence of RETACVD1.
wretacvd1	0.0	Width dependence of RETACVD1.
pretacvd1	0.0	Area dependence of RETACVD1.
k0	0.0	Non-saturation effect parameter for strong inversion region.
lk0	0.0 m	Length dependence of K0.
wk0	0.0 m	Width dependence of K0.
pk0	0.0 m^2	Area dependence of K0.
k01	0.0 1/K	Temperature coefficient for K0.
lk01	0.0 m/K	Length dependence of K01.
wk01	0.0 m/K	Width dependence of K01.

© 2023 Cadence Design Systems, Inc.

pk01	0.0 m^2/K	Area dependence of K01.
m0	1.0	offset of non-saturation effect parameter for strong inversion region.
lm0	0.0 m	Length dependence of M0.
wm0	0.0 m	Width dependence of M0.
pm0	0.0 m^2	Area dependence of M0.
m01	0.0 1/K	Temperature coefficient for M0.
lm01	0.0 m/K	Length dependence of M01.
wm01	0.0 m/K	Width dependence of M01.
pm01	0.0 m^2/K	Area dependence of M01.
b0	0.0	Non-saturation effect parameter for strong inversion region.
lb0	0.0	Length dependence of B0.
wb0	0.0	Width dependence of B0.
pb0	0.0	Area dependence of B0.
b01	0.0	Temperature coefficient for B0.
lb01	0.0	Length dependence of B01.
wb01	0.0	Width dependence of B01.
pb01	0.0	Area dependence of B01.
b1	0.0	Non-saturation effect parameter for strong inversion region.

© 2023 Cadence Design Systems, Inc.

lb1	0.0	Length dependence of B1.
wb1	0.0	Width dependence of B1.
pb1	0.0	Area dependence of B1.
b11	0.0	Temperature coefficient for B1.
lb11	0.0	Length dependence of B11.
wb11	0.0	Width dependence of B11.
pb11	0.0	Area dependence of B11.
b2	1.0	Non-saturation effect parameter for strong inversion region.
lb2	0.0	Length dependence of B2.
wb2	0.0	Width dependence of B2.
pb2	0.0	Area dependence of B2.
b21	0.0	Temperature coefficient for B2.
lb21	0.0	Length dependence of B21.
wb21	0.0	Width dependence of B21.
pb21	0.0	Area dependence of B21.
ssl0	4.0e2 A/m	Temperature-and doping-independent parameter for sub-surface leakage drain current.
ssl1	3.36e8 1/m	Temperature-and doping-independent parameter for gate length for sub-surface leakage drain current.
ssl2	0.185	Fitting parameter for sub-surface leakage drain current: barrier height.

© 2023 Cadence Design Systems, Inc.

ssl3	0.3 V	Fitting parameter for sub-surface leakage drain current: gate voltage effect.
ssl4	1.4 1/V	Fitting parameter for sub-surface leakage drain current: gate voltage effect.
ssl5	0 1/V	Fitting parameter for sub-surface leakage drain current: gate voltage effect.
sslexp1	0.490	Fitting exponent for SSL doping effect.
sslexp2	1.42	Fitting exponent for SSL temperature.
lnfactoredge	0.0 m	Length dependence of NFACTOREDGE.
wnfactoredge	0.0 m	Width dependence of NFACTOREDGE.
pnfactoredge	0.0 m^2	Area dependence of NFACTOREDGE.
lcitedge	0.0 F/m	Length dependence of CITEDGE.
wcitedge	0.0 F/m	Width dependence of CITEDGE.
pcitedge	0.0 F	Area dependence of CITEDGE.
lcdscdedge	0.0 F/m/V	Length dependence of CDSCDEDGE.
wcdscdedge	0.0 F/m/V	Width dependence of CDSCDEDGE.
pcdscdedge	0.0 F/V	Area dependence of CDSCDEDGE.
lcdscbedge	0.0 F/m/V	Length dependence of CDSCBEDGE.
wcdscbedge	0.0 F/m/V	Width dependence of CDSCBEDGE.

© 2023 Cadence Design Systems, Inc.

pcdscbedge	0.0 F/V	Area dependence of CDSCBEDGE.
leta0edge	0.0 m	Length dependence of ETA0EDGE.
weta0edge	0.0 m	Width dependence of ETA0EDGE.
peta0edge	0.0 m^2	Area dependence of ETA0EDGE.
letabedge	0.0 m/V	Length dependence of ETABEDGE.
wetabedge	0.0 m/V	Width dependence of ETABEDGE.
petabedge	0.0 m^2/V	Area dependence of ETABEDGE.
lkt1edge	0.0 V m	Length dependence of KT1EDGE.
wkt1edge	0.0 V m	Width dependence of KT1EDGE.
pkt1edge	0.0 V m^2	Area dependence of KT1EDGE.
lkt1ledge	0.0 V m^2	Length dependence of KT1LEDGE.
wkt1ledge	0.0 V m^2	Width dependence of KT1LEDGE.
pkt1ledge	0.0 V m^3	Area dependence of KT1LEDGE.
lkt2edge	0.0 m	Length dependence of KT2EDGE.
wkt2edge	0.0 m	Width dependence of KT2EDGE.
pkt2edge	0.0 m^2	Area dependence of KT2EDGE.
lkt1expedge	0.0 m	Length dependence of KT1EXPEDGE.
wkt1expedge	0.0 m	Width dependence of KT1EXPEDGE.
pkt1expedge	0.0 m^2	Area dependence of KT1EXPEDGE.

© 2023 Cadence Design Systems, Inc.

ltnfactoredge	0.0 m	Length dependence of TNFACTOREDGE.
wtnfactoredge	0.0 m	Width dependence of TNFACTOREDGE.
ptnfactoredge	0.0 m^2	Area dependence of TNFACTOREDGE.
lteta0edge	0.0 m	Length dependence of TETA0EDGE.
wteta0edge	0.0 m	Width dependence of TETA0EDGE.
pteta0edge	0.0 m^2	Area dependence of TETA0EDGE.
k2edge	0.0 V	Vth shift due to Vertical Non-uniform doping.
lk2edge	0.0 m	Length dependence of K2EDGE.
wk2edge	0.0 m	Width dependence of K2EDGE.
pk2edge	0.0 m^2	Area dependence of K2EDGE.
kvth0edge	0.0 V m	Threshold Shift parameter for stress effect.
lkvth0edge	0.0 m^LLODKU0	Length dependence of KVTH0EDGE.
wkvth0edge	0.0 m^WLODKU0	Width dependence of KVTH0EDGE.
pkvth0edge	0.0 m^(LLODKU0+WLODKU0)	Area dependence of KVTH0EDGE.
stk2edge	0.0 m	K2 shift factor related to Vth change.
lstk2edge	0.0 m^2	Length dependence of STK2EDGE.

© 2023 Cadence Design Systems, Inc.

wstk2edge	0.0 m^2	Width dependence of STK2EDGE.
pstk2edge	0.0 m^3	Area dependence of STK2EDGE.
steta0edge	0.0 m	ETA0 shift related to Vth0 change.
lsteta0edge	0.0 m^2	Length dependence of STETA0EDGE.
wsteta0edge	0.0 m^2	Width dependence of STETA0EDGE.
psteta0edge	0.0 m^3	Area dependence of STETA0EDGE.
nedge	1	Flicker noise parameter for edge fet transistor.
noia1_edge	0.0	Flicker noise fitting parameter in strong inversionfor edge fet transistor.
noiax_edge	1.0	Flicker noise fitting parameter in strong inversionfor edge fet transistor.
lp	1.0e-5 m	Length scaling parameter for thermal noise.
lh	(30*1.0e-9) m	Length of Halo transistor.
noia2	noias^(1-EF)/(eV)^1/m^3	Flicker noise parameter A for Halo.
hndep	ndep 1/m^3	Halo doping concentration for I-V.
fnoimod	0	Flicker noise model selector.
tnoik2	0.1 1/m	Empirical parameter for sensitivity of RNOIK.

© 2023 Cadence Design Systems, Inc.

ags	0.00	Coefficient of Source Charge dependence in AbulkIV for Id-Vd flexibility.
lags	0.00	Length dependence of AGS.
wags	0.00	Width dependence of AGS.
pags	0.00	Area dependence of AGS.
lags1	0.00	Length dependence of AGS1.
wags1	0.00	Width dependence of AGS1.
pags1	0.00	Area dependence of AGS1.
a0	0.00	Coefficient of depletion width dependence in AbulkIV for Id-Vd flexibility.
la0	0.00	Length dependence of A0.
wa0	0.00	Width dependence of A0.
pa0	0.00	Area dependence of A0.
keta	0.00	Coefficient of back-bias dependence in AbulkIV for Id-Vd flexibility.
lketa	0.00	Length dependence of KETA.
wketa	0.00	Width dependence of KETA.
pketa	0.00	Area dependence of KETA.
agscv	0.00	Coefficient of Source Charge dependence in AbulkCV for Capacitance flexibility.
lagscv	0.00	Length dependence of AGSCV.
wagscv	0.00	Width dependence of AGSCV.

© 2023 Cadence Design Systems, Inc.

pagscv	0.00	Area dependence of AGSCV.
a0cv	0.00	Coefficient of depletion width dependence in AbulkCV for Capacitance flexibility.
la0cv	0.00	Length dependence of A0CV.
wa0cv	0.00	Width dependence of A0V.
pa0cv	0.00	Area dependence of A0CV.
ketacv	0.00	Coefficient of back-bias dependence in AbulkCV for Capacitance flexibility.
lketacv	0.00	Length dependence of KETACV.
wketacv	0.00	Width dependence of KETACV.
pketacv	0.00	Area dependence of KETACV.
deltacv	0.125	Smoothing function factor for VdsatCV.
ldeltacv	0.0 m	Length dependence of DELTACV.
wdeltacv	0.0 m	Width dependence of DELTACV.
pdeltacv	0.0 m^2	Area dependence of DELTACV.
deltalcv	0.0 m^DELTALEXPCV	Length dependence coefficient of DELTACV.
deltalexpcv	1.0	Length dependence exponent coefficient of DELTACV.
tdeltacv	0.0 1/K	Temperature coefficient for DELTACV.
atcv	(-1.56e-3) m/s	Temperature coefficient for CV saturation velocity.

© 2023 Cadence Design Systems, Inc.

latcv	0.0 m^2/s	Length dependence of ATCV.
watcv	0.0 m^2/s	Width dependence of ATCV.
patcv	0.0 m^3/s	Area dependence of ATCV.
atlcv	0.0 m	Length Scaling parameter for ATCV.
submod	0	0: The equations using B0, B1 and B2 are OFF, other: The equations using B0, B1 and B2 are ON.
psatbmod	0	0: clamping for PSATB OFF, other: clamping for PSATB ON.
cvsatmod	0	0: Tunability for Cgg@vds!=0 OFF, other: Tunability for Cgg@vds!=0 ON.
voffmod	0	0: Tuning flexibility for GmOvId OFF, other: enhancement ON.
tempmod	0	0: Temperature dependence on ATCV OFF, other: enhancement ON.
flkmod	0	0: Flicker noise enhancement OFF, other: enhancement ON.
flkmnudmod	0	0: Flicker noise enhancement due to MNUD1 and MNUD OFF, other: enhancement ON.
flkedgemod	0	0: Flicker noise enhancement due to EDGEFET OFF, other: enhancement due to EDGEFET ON.
tnoimnudmod	0	0: Thermal noise enhancement due to MNUD and MNUD1 OFF, other: enhancement due to MNUD and MNUD1 ON.
vfbaccmod	0	0: VFB for CV acc OFF, other: VFB for CV acc ON.

© 2023 Cadence Design Systems, Inc.

abulkmod	0	0: Binable Abulk effect OFF, other: Binable Abulk effect ON.
phibcvmod	0	0: phib in CVMOD=1 is changed, other: phib with NDEPCV is used only in CVMOD=1.
warnmod	0	0: Keep original warning message, other: change the specific warning message.
nsatmod	1	1: backward compatible model to 106.2 with TSMC Model Enhancement Mode, other: clamping Nsat by 0.0 with Smooth2 function.
cvaccmod	0	0: CV acc OFF, other: VFB for CV acc ON.
subleakmod	0	correction of the sub-surface leakage, 0: Turn off 1: Turn on.
tnoienmod	0	thermal noise tuning enhancement, 0: Turn Off 1: Turn On.
xnoiw	0.0	for thermal noise tuning flexibilty.
xnoik	0.0	for thermal noise tuning flexibilty.
igbaccenmod	0	Igbacc enhancement mode (0: Turn Off 1: Turn On.
kaccoff	0.0	Vgs offset to fine tune the shape of Igbacc.
lkaccoff	0.0	Length dependence of KACCOFF.
wkaccoff	0.0	Width dependence of KACCOFF.
pkaccoff	0.0	Area dependence of KACCOFF.
kacccon	0.01	
lkacccon	0.0	

© 2023 Cadence Design Systems, Inc.

wkacccon	0.0	
pkacccon	0.0	
eigbacc	0.0	Parameter to adjust Igbacc.
leigbacc	0.0	Length dependence of EIGBACC.
weigbacc	0.0	Width dependence of EIGBACC.
peigbacc	0.0	Area dependence of EIGBACC.
eigbacc2	0.0	Parameter to fine tune the shape of Igbacc.
leigbacc2	0.0	Length dependence of EIGBACC2.
weigbacc2	0.0	Width dependence of EIGBACC2.
peigbacc2	0.0	Area dependence of EIGBACC2.
welledgemod	0	0: Well effect on edge mosfet OFF, other: enhancement ON.
minrdsmod	0	Minimum RD/RS mode, 0: Turn off, 1: Turn on.
kvth0edgewe	0.0	Threshold Shift parameter due to Well proximity in EDGEFET.
lkvth0edgewe	0.0 m	Length dependence of KVTH0EDGEWE.
wkvth0edgewe	0.0 m	Width dependence of KVTH0EDGEWE.
pkvth0edgewe	0.0 m^2	Area dependence of KVTH0EDGEWE.
k2edgewe	0.0	Vth shift due to Vertical Non-uniform doping due to Well proximity in EDGEFET.
lk2edgewe	0.0 m	Length dependence of K2EDGEWE.

© 2023 Cadence Design Systems, Inc.

wk2edgewe	0.0 m	Width dependence of K2EDGEWE.
pk2edgewe	0.0 m^2	Area dependence of K2EDGEWE.
abulk	1.0	For flexibility of tuning Cgg in strong inversion.
c0	0.0 V	Lateral NUD1 voltage parameter.
lc0	0.0 V	Length dependence of C0.
wc0	0.0 V	Width dependence of C0.
pc0	0.0 V	Area dependence of C0.
c01	0.0 V/K	Temperature dependence of C0.
lc01	0.0 V/K	Length dependence of C01.
wc01	0.0 V/K	Width dependence of C01.
pc01	0.0 V/K	Area dependence of C01.
c0si	1.0	Correction factor for strong inversion used in Mnud1.
lc0si	0.0 V	Length dependence of C0SI.
wc0si	0.0 V	Width dependence of C0SI.
pc0si	0.0 V	Area dependence of C0SI.
c0si1	0.0 /K	Temperature dependence of C0SI.
lc0si1	0.0 V	Length dependence of C0SI1.
wc0si1	0.0 V	Width dependence of C0SI1.
pc0si1	0.0 V	Area dependence of C0SI1.

© 2023 Cadence Design Systems, Inc.

c0sisat	0.0	Correction factor for saturation used in Mnud1.
lc0sisat	0.0 V	Length dependence of C0SISAT.
wc0sisat	0.0 V	Width dependence of C0SISAT.
pc0sisat	0.0 V	Area dependence of C0SISAT.
c0sisat1	0.0	Temperature dependence of C0SISAT.
lc0sisat1	0.0 V	Length dependence of C0SISAT1.
wc0sisat1	0.0 V	Width dependence of C0SISAT1.
pc0sisat1	0.0 V	Area dependence of C0SISAT1.
hvmod	0	High Voltage series resistance model, 0: Turn Off 1: Turn On.
hvcap	0	High Voltage capacitance model. 0: Turn Off 1: Turn On.
hvcaps	0	High Voltage capacitance model at source side. 0: Turn Off 1: Turn On.
rbodyhvmod	0	High Voltage drain and body resistance model, 0: Turn Off 1: Turn On.
iimod	0	Flag for impact ionization in the drift region 0: Turn-Off, 1: Turn On.
vcovd	0.0 V	
pcovd	0.0	
vcovs	0.0 V	
pcovs	0.0	

© 2023 Cadence Design Systems, Inc.

ndriftd	5.0e16 per m^2	Charge density in the drift region.
vdrift	1.0e5 m/ sec	Saturation velocity in the drift region.
ptwghv	0.0	VDRIFT variation with gate bias.
ptwghv1	0.0	VDRIFT variation with gate bias.
psatxhv	60.0	Fine tuning of PTWGDR effect.
mdrift	1.0	Non-linear resistance parameter.
ndrifts	5.0e16 per m^2	Charge density in the source side drift region.
rdlcw	100.0 Ω µm^WR	'R'esistance of the 'D'rain side drift region at 'L'ow 'C'urrent.
rslcw	0 Ω µm^WR	'R'esistance of the 'S'ource side drift region at 'L'ow 'C'urrent.
pdrwb	0	Body bias dependence of the drift region resistance.
vfbdrift	(-1) V	Flat-band voltage of the drift region.
vfbov	(-1) V	Flat-band voltage of the overlap region.
lover	(500*1.0 e-9) m	Overlap region length.
loveracc	(500*1.0 e-9) m	Drift region length.
ndr	1e24 1/ m^3	Drift region doping.

© 2023 Cadence Design Systems, Inc.

slhv	0	Parameter and Flag for controlling slope of accumulation region capacitance. 0: Turn-Off, 1: Turn On.
slhv1	1.0	Parameter for slope of the accumulation capacitance.
alphadr	0.0 m/V	First parameter of Iii in the drift region.
betadr	0.0 1/V	Second parameter of Iii in the drift region.
prthv	0.0	Temperature coefficient for drift resistance.
athv	0 m/s	Temperature coefficient for drift region saturation velocity.
hvfactor	1e-3	
drii1	1.0	Parameter for carrier concentration for Impact Ionization in the the drift.
drii2	5 V	Saturation voltage ~ Esat * L.
deltaii	0.5 V	Smoothing parameter.
asymp	0.6	Parameter for Asymmetry mode.
drb1	0.0	Parameter for body-bias dependence in HVMOD.
drb2	0.0	Parameter for body-bias dependence in HVMOD.
rdvds	8 V	Parameter for Idriftsat variation with drain voltage.
gadrift	0	Parameter for Idriftsat variation with drain voltage.
xpart	0.0	Drain-Body Diode partitioning in RBODYHVMOD.
ags1	1.0	qs nonlinear term for Id-Vd flexibility.

© 2023 Cadence Design Systems, Inc.

eu1	0.0	Temperature coefficient for EU.
leu1	0.0	Length dependence of EU1.
weu1	0.0	Width dependence of EU1.
peu1	0.0	Area dependence of EU1.
qrnois	1.0	Correction factor for flicker noise due to qs.
lqrnois	0.0	Length dependence of QRNOIS.
wqrnois	0.0	Width dependence of QRNOIS.
pqrnois	0.0	Area dependence of QRNOIS.
qrnoid	1.0	Correction factor for flicker noise due to qdeff.
lqrnoid	0.0	Length dependence of QRNOID.
wqrnoid	0.0	Width dependence of QRNOID.
pqrnoid	0.0	Area dependence of QRNOID.
noia1	0.0 s^(1-EF)/(eV)^1/m^3	Flicker noise parameter A.
noiax	1.0e-5	Correction factor for flicker noise.
bfns	1.0	Flicker noise frequency exponent for Source Resistance.
bfnd	1.0	Flicker noise frequency exponent for Drain Resistance.
kfns	0.0	Flicker noise coefficient for Source Resistance.

© 2023 Cadence Design Systems, Inc.

kfnd	0.0	Flicker noise coefficient for Drain Resistance.
afns	2.0	Flicker noise coefficient for Source Resistance.
afnd	2.0	Flicker noise coefficient for Drain Resistance.
delvfbacc	0.0	VFB shift at accumulation region.
dlcacc	0.0 m	Delta L for CV acc.
llcacc	0.0 m^(1+LLN)	Length reduction parameter.
lwcacc	0.0 m^(1+LWN)	Length reduction parameter.
lwlcacc	0.0 m^(1+LWN+LLN)	Length reduction parameter.
dwcacc	0.0 m	Delta W for CV acc.
wlcacc	0.0 m^(1+WLN)	Width reduction parameter.
wwcacc	0.0 m^(1+WWN)	Width reduction parameter.
wwlcacc	0.0 m^(1+WWN+WLN)	Width reduction parameter.
naedge	1.0	Flicker noise parameter A ratio for EDGEFET.
nbedge	1.0	Flicker noise parameter B ratio for EDGEFET.

© 2023 Cadence Design Systems, Inc.

ncedge	1.0	Flicker noise parameter C ratio for EDGEFET.
sslmod	0	Sub-Surface Leakage Drain Current,0: Turn off 1: Turn on.
ndepedge	1e24 $1/m^2$	EDGEFET NDEP.
lndepedge	0.0 $1/m^2$	Length dependence of EDGEFET NDEP.
wndepedge	0.0 $1/m^2$	Width dependence of EDGEFET NDEP.
pndepedge	0.0 1/m	Area dependence of EDGEFET NDEP .
fnoik	0.0	a offset for flicker.
kfrs	0.0	a factor for Rs.
kfrd	0.0	a factor for Rd.
kfds	0.0	a factor for drain-source terminals.
afrs	2.0	a factor of ids for Rs.
afrd	2.0	a factor of ids for Rd.
afds	2.0	a factor of ids between drain and source terminals.
efrs	1.0	an index for Rs.
efrd	1.0	an index for Rd.
efds	1.0	an index between drain and source terminals.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`weff`	`(m)`	Effective channel width.
`leff`	`(m)`	Effective channel length.
`tempeff`	`(C)`	Effective temperature for a single device.
`meff`		Effective multiplicity factor (m-factor).

Related Topics

BSIM6 Model (bsim6)

Instance

Model

Version Update and Enhancements

Model Equations

Instance Parameters

Model Definition

© 2023 Cadence Design Systems, Inc.

24

PSP102 Model

PSP102 is a compact MOSFET model intended for digital, analog and RF designs. It is jointly developed by NXP Semiconductors Research and Arizona State University, and is a surface-potential based MOS model containing all relevant physical effects (mobility reduction, velocity saturation, DIBL, gate current, lateral doping gradient effects, STI stress, and so forth), to model present-day and upcoming deep-submicron bulk CMOS technologies. The JUNCAP2 source/drain junction model is an integrated part of PSP102.

PSP102 not only gives an accurate description of currents, charges, and their first order derivatives (i.e. transconductance, conductance and capacitances), but also of the higher order derivatives, resulting in an accurate description of electrical distortion behavior. The latter is especially important for analog and RF circuit design. The model, furthermore, gives an accurate description of the noise behavior of MOSFETs.

For a full description of the PSP102 model, refer to http://pspmodel.asu.edu.

Related Topics

Model Usage

History and Development

Structure of PSP102

Geometrical Scaling and Stress Model for Intrinsic MOSFET

Model Equations

Non-Quasi-Static (NQS) RF Model

Component Statements for PSP102 Models

© 2023 Cadence Design Systems, Inc.

Model Usage

Instance Syntax

PSP102 instance has 4 terminals. The ModelName has to be associated with a PSP102 model card.

```
InstanceName (d g s b) PSP102ModelName <parameter=value>
```

Sample Instance Statement

```
q1 (v1 v2 v3 v4) psp102_mod w=1e-6 l=0.5e-6
```

Model Syntax

The following syntax specifies PSP102 model:

```
model ModelName psp102 parameter=value ...
```

The third parameter, `psp102`, is the master to indicate this model card is a PSP102 model card.

Version and Master Name

- Versions 102.2, 102.2.1, 102.3, 102.3.2, 102.3.3, 102.3.4, 102.4, and 102.5 are supported.
- There are 7 master names - psp102, psp1020, psp1021, psp102e, pspnqs1020, pspnqs1021 and pspnqs102e
- psp1020 is global model without NQS effect. psp1021 is bin model without NQS effect. psp102e is local model without NQS effect. pspnqs1020 is global model with NQS effect. pspnqs1021 is bin model with NQS effect. pspnqs102e is local model with NQS effect.
- Master name psp102 is a general name for PSP102, and it covers 6 psp102 **masternames** mentioned above. The relation between psp102 and other six masters is listed in the following table:

psp1020	psp102(binmod=0 geomod=1 swnqs=0)
psp1021	psp102(binmod=1 geomod=0/1 swnqs=0)
psp102e	psp102(binmod=0 geomod=0 swnqs=0)

© 2023 Cadence Design Systems, Inc.

pspnqs1020	psp102(binmod=0 geomod=1 swnqs=0)
pspnqs1021	psp102(binmod=1 geomod=0/1 swnqs=0)
pspnqs102e	psp102(binmod=0 geomod=0 swnqs=0)

Sample Model Statements

Example: PSP102.2

```
model psp102_mod psp102 type=n version=102.2
+tr = 25 swigate = 0
+binmod=0 geomod=1 swnqs=9 swgidl = 1 swjuncap = 3
```

Example: PSP102.3

```
model psp102_mod psp102 type=n version=102.3
+tr = 25 swigate = 0
+binmod=0 geomod=1 swnqs=9 swgidl = 1 swjuncap = 3
```

Related Topics

PSP102 Model

History and Development

Structure of PSP102

Geometrical Scaling and Stress Model for Intrinsic MOSFET

Model Equations

Non-Quasi-Static (NQS) RF Model

Component Statements for PSP102 Models

© 2023 Cadence Design Systems, Inc.

History and Development

PSP100

1. PSP100 is released by NXP in April 2005
2. PSP100 is supported in MMSIM 6.0.2 in Dec 2005

PSP101 (SiMKit2.3)

1. PSP101 is supported in MMISIM 6.1 in June 2006
2. PSP101 is not backward compatible with PSP100

Changes

- A complete set of binning scaling rules has been added as a phenomenological alternative to the physics-based geometrical scaling rules.
- BSIM-like instance parameters AS, AD, PS, and PD were added for the junction model.
- To avoid confusion between zeros and "O"s, zeros no longer occur in parameter names. They have all been replaced by "O"s.
- Some global parameter names have an additional "O" in their names in order to avoid duplicate names in the global and local model.

PSP102.0 (SiMKit2.3.2)

PSP102.0 is supported in MMSIM6.1.1 in Dec 2006

Changes

- The value for LG when SWJUNCAP = 2 was corrected.
- The clipping/limiting behavior of NP has been made more transparent.
- A minor numerical issue has been resolved.
- The scaling rule for DPHIB is now correctly implemented.
- A coding bug in JUNCAP has been corrected.

© 2023 Cadence Design Systems, Inc.

- A coding bug in the stress model (involving parameter PKVTHO) has been corrected.
- The parameters LVARW and WVARL have been removed from the binning model in order to ensure continuity of parameters across bin boundaries.

PSP102.1 (SiMKit2.4)

PSP102.1 is supported in MMSIM6.2 in June 2007

Changes

- Added clipping boundaries for SWNQS
- Several minor changes and improvements in model implementation
- Solved bug in stress model
- Solved bug in JUNCAP2
- Included preliminary implementation of PSP-NQS in SiMKit.

PSP102.1.1 (SiMKit2.5)

PSP102.1.1 is released in MMSIM6.2.1 in Dec 2007

PSP102.2

VerilogA code for PSP102.2 is released in Oct 2007

Changes

- Add parameters EPSROX (electrical or local), EPSROXO (geometrical or global), POEPSROX (binning) representing relative dielectric constant of gate oxide.
- Added a Well Proximity Effect model
- Added instance parameters DELVTO (threshold voltage shift parameter) and FACTUO (zero-field mobility pre-factor) to the electrical (or local), geometrical (or global) and binning model.
- Added NF (number of fingers) support to geometrical (or global) and binning model.
- Extended the stress model to support NF.

© 2023 Cadence Design Systems, Inc.

- Added substrate resistance network and external gate resistance.
- Added geometry scaling for gate resistance in global and binning model.
- Integration of JUNCAP express into PSP. PSP is equipped with a switch-parameter SWJUNEXP.

PSP102.2.1 (SiMKit4.0.1)

Implemented in MMSIM7.0.1 in June 2008

Changes

- Minor implementation change in juncap initInstance
- Fix issue in calculation of vfmin (juncap initInstance).
- Add clipping for fbbt-variables to nonnegative values (juncap initModel)
- Fix noise calculation for parasitic resistances
- Solved issue with Gmin for Vds<0
- Corrected error in expression for OP-variable cjssti

PSP102.3 (SiMKit3.1.2)

Implemented in MMSIM7.1.0 in Dec 2008

Changes

- Addition of asymmetric junction model. The new parameter SWJUNASYM is a flag.
- Addition of flicker noise frequency exponent parameter EF (local model), EFO (global model) and POEF (binning model).
- Addition of parameters LINTNOI and ALPNOI to the global model, to increase the flexibility of the length scaling of the flicker noise.
- Some minor bug-fixes and implementation changes.

PSP102.3.2 (SiMKit3.2)

Implemented in MMSIM7.1.1 in June 2009

© 2023 Cadence Design Systems, Inc.

Changes

- Fixed bug in JUNCAP2-model, involving FJUNQ-based selection-criterion in JUNCAPexpress charge model.
- Some minor implementation changes.

PSP102.3.3 (SiMKit3.3)

Implemented in MMSIM7.2 in Dec 2009. Since MMSIM7.2, version control and master name psp102 are supported.

Changes

- Added value of gate resistance to OP-output
- Minor bug fix in conditional for SP-calculation of overlap areas.

PSP102.3.4 (SiMKit3.4)

Implemented in MMSIM10.1 in June 2010.

Changes

- Modified implementation of the asymmetrical junction model to improve simulation speed of the verilog-A code
- Modified scaling of the MULT-scaling factor
- Minor bug fix for the output of sfl, sqrtsfw, and fknee

PSP102.4 (SiMKit4.01)

Implemented in MMSIM13.1 in September 2013.

Changes

The implementation of the thermal noise model has been improved in version 102.4. As a result, better convergence for some noise analysis could be expected in this version.

- A bug in the sign of the correlation coefficient for negative `Vds` has been resolved

© 2023 Cadence Design Systems, Inc.

- Gummel symmetry of `Sid` at high frequency has been improved
- The number of `white_noise` sources has been reduced and the noise voltage values in the noise subcircuit have been scaled to more physical values

PSP102.5

Implemented in MMSIM 14.1 in October 2014.

Changes

The main enhancements in the PSP102.5 version include the following:

- Excess noise model has been added.
- Minor numerical issue in avalanche current calculation (occurring when A4 is large and the body is forward biased) has been solved.
- Missing T-scaling in OP-output variables `lp_bgidl` and `lp_bgidld` has been fixed.

Related Topics

PSP102 Model

Model Usage

Structure of PSP102

Geometrical Scaling and Stress Model for Intrinsic MOSFET

Model Equations

Non-Quasi-Static (NQS) RF Model

Component Statements for PSP102 Models

Structure of PSP102

The PSP model has a hierarchical structure, similar to that of MOS Model 11 and SP. This means that there is a strict separation of the geometry scaling in the global model and the model equations in the local model.

© 2023 Cadence Design Systems, Inc.

As a consequence, PSP can be used at either one of two levels.

- Global level One uses a global parameter set, which describes a whole geometry range. Combined with instance parameters (such as L and W), a local parameter set is internally generated and further processed at the local level in the same way as a custom-made local parameter set.
- Local level One uses a custom-made local parameter set to simulate a transistor with a specific geometry. Temperature scaling is included at this level.

The set of parameters which occur in the equations for the various electrical quantities is called the local parameter set. In PSP, temperature scaling parameters are included in the local parameter set. Each of these parameters can be determined by purely electrical measurements. As a consequence, a local parameter set gives a complete description of the electrical properties of a device of one particular geometry.

Since most of these parameters scale with geometry, all transistors of a particular process can be described by a (larger) set of parameters, called the global parameter set. This set contains all local parameters for a long/wide device plus a number of sensitivity coefficients. From the global parameter set, you can obtain a local parameter set for a specific device by applying a set of scaling rules. For more information, see **Calculation of Transistor Geometry**. The geometric properties of that specific device (such as its length and width) enter these scaling rules as instance parameters.

PSP is preferably used at the global level when designing a circuit in a specific technology for which a global parameter set is available. On the other hand, using PSP at local level can be helpful during parameter extraction.

As an option, it is possible to deal with the modification of transistor properties due to stress. In PSP, this is implemented by an additional set of transformation rules, which are optionally applied to the intermediate local parameter set generated at the global level. The parameters associated with the stress model are consequently part of the global parameter set.

© 2023 Cadence Design Systems, Inc.

The model structure described above is schematically depicted in the following figure.

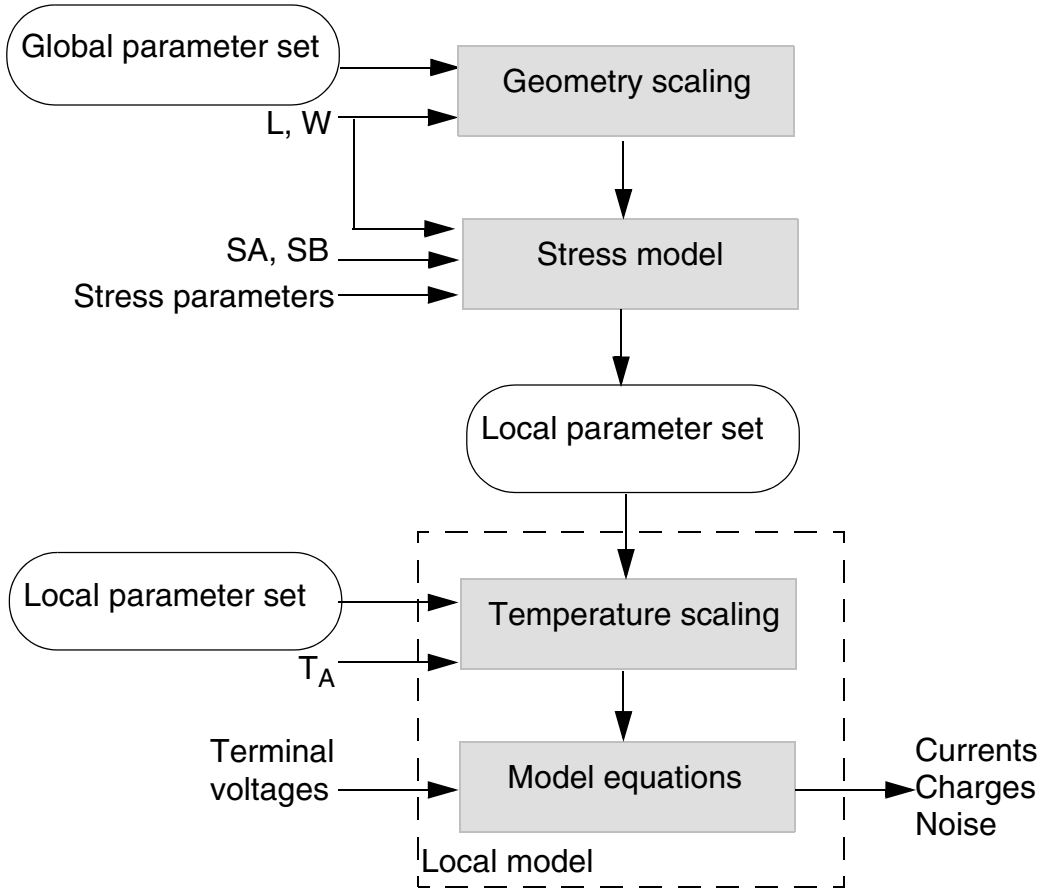


Figure 24-1 Schematic Overview of the PSP Model Structure

The JUNCAP2 model is implemented in such a way that the same set of JUNCAP2 parameters can be used at both the global and the local level.

Related Topics

PSP102 Model

Model Usage

History and Development

Geometrical Scaling and Stress Model for Intrinsic MOSFET

© 2023 Cadence Design Systems, Inc.

Model Equations

Non-Quasi-Static (NQS) RF Model

Component Statements for PSP102 Models

Geometrical Scaling and Stress Model for Intrinsic MOSFET

The physical geometry scaling rules of PSP have been developed to give a good description over the whole geometry range of CMOS technologies. The parameters for which no scaling rules are specified appear in both the list for the physical geometrical scaling rules and the list for the electrical model and can be copied. When the stress model is used, only the parameters for which shifts or multiplication factors are defined in Parameter Modification due to Stress Effects are affected.

Geometrical Scaling Rules

Calculation of Transistor Geometry

$$L_{EN} = 10^{-6}$$

$$W_{EN} = 10^{-6}$$

$$\Delta L_{PS} = LVAR0 \cdot \left(1 + LVARL \cdot \frac{L_{EN}}{L}\right) \cdot \left(1 + LVARW \cdot \frac{W_{EN}}{W}\right)$$

$$\Delta W_{OD} = WVAR0 \cdot \left(1 + WVARL \cdot \frac{L_{EN}}{L}\right) \cdot \left(1 + WVARW \cdot \frac{W_{EN}}{W}\right)$$

$$L_E = L - \Delta L = L + \Delta L_{PS} - 2 \cdot LAP$$

$$W_E = W - \Delta W = W + \Delta W_{OD} - 2 \cdot WOT$$

© 2023 Cadence Design Systems, Inc.

Note: L_E and W_E cannot be smaller than 10^{-9} after calculation.

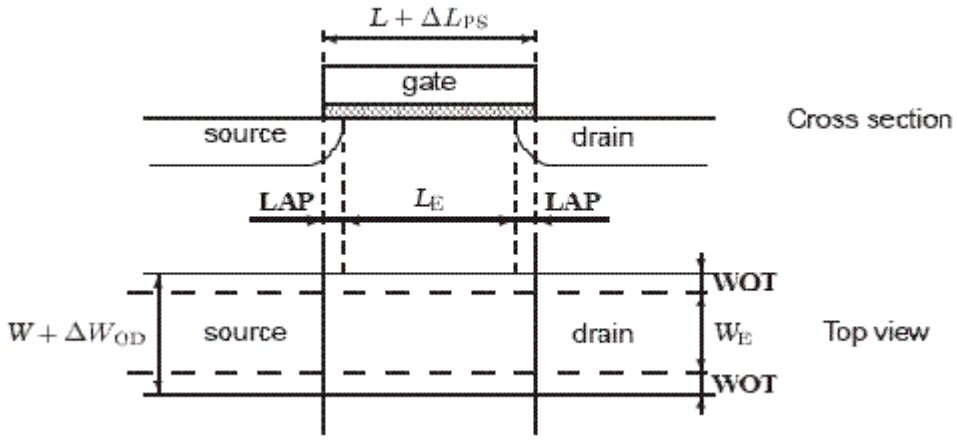


Figure 24-2 Dimensions of a MOS Transistor

© 2023 Cadence Design Systems, Inc.

Calculation of Geometry-Dependent Parameters using Physical Scaling Rules

Calculation of Process Parameters

$$VFB = VFB0 \cdot \left(1 + VFBL \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + VFBW \cdot \frac{W_{EN}}{W_E}\right) \cdot \left(1 + VFBLW \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}\right)$$

$$STVFB = STVFB0 \cdot \left(1 + STVFBL \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + STVFBW \cdot \frac{W_{EN}}{W_E}\right) \cdot \left(1 + STVFBLW \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}\right)$$

$$NSUB0e = NSUB0 \cdot MAX\left(\left[1 + NSUB0W \cdot \frac{W_{EN}}{W_E} \cdot \ln\left(1 + \frac{W_E}{WSEG}\right)\right], 10^{-3}\right)$$

$$NPCKe = NPCK \cdot MAX\left(\left[1 + NPCK \cdot \frac{W_{EN}}{W_E} \cdot \ln\left(1 + \frac{W_E}{WSEGP}\right)\right], 10^{-3}\right)$$

© 2023 Cadence Design Systems, Inc.

$$LPCKe = LPCK \cdot MAX\left(\left[1 + LPCKW \cdot \frac{W_{EN}}{W_E} \cdot \ln\left(1 + \frac{W_E}{WSEGP}\right)\right], 10^{-3}\right)$$

$$a = 7.5 \cdot 10^{10}$$

$$b = \sqrt{NSUB0e + 0.5 \cdot NPVCKe} - \sqrt{NSUB0e}$$

$$NP = NP0 \cdot \left(1 + NPL \cdot \frac{L_{EN}}{L_E}\right)$$

$$NSUB = \begin{cases} NSUB0e + NPCKe \cdot \left[2 - \frac{L_E}{LPCKe}\right] & \text{for } L_E < LPCKe \\ NSUB0e + NPCKe \cdot \frac{LPCKe}{L_E} & \text{for } LPCKe \le L_E \le LPCKe \\ \left[\sqrt{NSUB0e} + a \cdot \ln\left(1 + 2 \cdot \frac{LPCKe}{L_E} \cdot \left[\exp\left(\frac{b}{a}\right) - 1\right]\right)\right]^2 & \text{for } L_E > 2*LPCKe \end{cases}$$

$$CT = \left(CT0 + CTL \cdot \left[\frac{L_{EN}}{L_E}\right]^{CTLEXP}\right) \cdot \left(1 + CTW \cdot \frac{W_{EN}}{W_E}\right)$$

Calculation of Lateral Gradient Factor Parameters

$$F0 = 1 - F0L1 \cdot \frac{L_{EN}}{L_E} - F0L2 \cdot \left[\frac{L_{EN}}{L_E}\right]^2$$

$$AF = \left(AF0 + AFL \cdot \left[\frac{L_{EN}}{L_E}\right]^{AFLEXP}\right) \cdot \left(1 + AFW \cdot \frac{W_{EN}}{W_E}\right)$$

$$BF = BFL \cdot \left[\frac{L_{EN}}{L_E}\right]^2$$

© 2023 Cadence Design Systems, Inc.

Calculation of Mobility Parameters

$$FBETle = FBET1 \cdot \left(1 + FBET1W \cdot \frac{W_{EN}}{W_E}\right)$$

$$LPle = LP1 \cdot MAX\left(\left[1 + LP1W \cdot \frac{W_{EN}}{W_E}\right], 10^{-3}\right)$$

$$G_{P,E} = 1 + FBETle \cdot \frac{LPle}{L_E} \cdot \left[1 - \exp\left(-\frac{L_E}{LPle}\right)\right] + FBET2 \cdot \frac{LP2}{L_E} \cdot \left[1 - \exp\left(-\frac{L_E}{LP2}\right)\right]$$

$$G_{W,E} = 1 + BETW1 \cdot \frac{W_{EN}}{W_E} + BETW2 \cdot \frac{W_{EN}}{W_E} \cdot \ln\left(1 + \frac{W_E}{WBET}\right)$$

$$BETN = \frac{U0}{G_{P,E}} \cdot \frac{W_E}{L_E} \cdot G_{W,E}$$

$$STBET = STBET0 \cdot \left(1 + STBETL \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + STBETW \cdot \frac{W_{EN}}{W_E}\right) \cdot 1 + STBETLW \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}$$

$$MUE = MUE0 \cdot \left[1 + MUEW \cdot \frac{W_{EN}}{W_E}\right]$$

$$XCOR = XCOR0 \cdot \left(1 + XCORL \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + XCORW \cdot \frac{W_{EN}}{LW_E}\right) \cdot \left(1 + XCORLW \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}\right)$$

$$CS = CS0 \cdot \left[1 + CSW \cdot \frac{W_{EN}}{W_E}\right]$$

© 2023 Cadence Design Systems, Inc.

Calculation of Series Resistance Parameters

$$RS = RSW1 \cdot \frac{W_{EN}}{W_E} \cdot \left[1 + RSW2 \cdot \frac{W_{EN}}{W_E}\right]$$

Calculation of Velocity Saturation Parameters

$$THESAT = \left(THESAT0 + THESATL \cdot \frac{G_{W,E}}{G_{P,E}} \cdot \left[\frac{L_{EN}}{L_E}\right]^{THESATLEXP}\right) \cdot \left(1 + THESATW \cdot \frac{w_{EN}}{w_E}\right)$$

$$STTHESAT = STTHESAT0 \cdot \left(1 + STTHESATL \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + STTHESATW \cdot \frac{W_{EN}}{W_E}\right) \cdot \left(1 + STTHESATLW \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}\right)$$

Calculation of Saturation Voltage Parameters

$$AX = \frac{AX0}{1 + AXL \cdot \frac{L_{EN}}{L_E}}$$

Calculation of Channel Length Modulation (CLM) Parameters

$$ALP = ALPL \cdot \left[\frac{L_{EN}}{L_E}\right]^{ALPLEXP} \cdot \left(1 + ALPW \cdot \frac{W_{EN}}{W_E}\right)$$

$$ALP1 = \frac{ALP1L1 \cdot \left[\frac{L_{EN}}{L_E}\right]^{ALP1LEXP}}{1 + ALP1L2 \cdot \left[\frac{L_{EN}}{L_E}\right]^{ALP1LEXP+1}} \cdot \left(1 + ALP1W \cdot \frac{W_{EN}}{W_E}\right)$$

© 2023 Cadence Design Systems, Inc.

$$ALP2 = ALP20 \cdot \frac{1 + ALP2W \cdot \frac{W_{EN}}{W_E}}{1 + ALPL \cdot \frac{L_{EN}}{L_E}}$$

Calculation of Impact Ionization (II) Parameters

$$A1 = A10 \cdot \left(1 + A1L \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + A1W \cdot \frac{W_{EN}}{W_E}\right)$$

$$A3 = A30 \cdot \left(1 + A3L \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + A3W \cdot \frac{W_{EN}}{W_E}\right)$$

$$A4 = A40 \cdot \left(1 + A4W \cdot \frac{W_{EN}}{W_E}\right)$$

Calculation of Gate Current Parameters

$$IGINV = IGINVLW \cdot \frac{W_E \cdot L_E}{W_{EN} \cdot L_{EN}}$$

$$IGOV = IGOVW \cdot \frac{W_E \cdot LOV}{W_{EN} \cdot L_{EN}}$$

Calculation of Gate-Induced Drain Leakage (GIDL) Parameters

$$AGIDL = AGIDLLW \cdot \frac{W_E \cdot LOV}{W_{EN} \cdot L_{EN}}$$

Calculation of Charge Model Parameters

$$COX = \varepsilon_{OX} \cdot \frac{W_E \cdot L_E}{TOX}$$

© 2023 Cadence Design Systems, Inc.

$$CGOV = \varepsilon_{OX} \cdot \frac{W_E \cdot LOV}{TOXOV}$$

$$CGBOV = CGBOVL \cdot \frac{L + \Delta L_{PS}}{L_{EN}}$$

$$IFK = IFKW \cdot \frac{W_E}{W_{EN}}$$

$$CFR = CFRW \cdot \frac{W + \Delta W_{OD}}{W_{EN}}$$

Calculation of Noise Model Parameters

$$NFA = NFALW \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}$$

$$NFB = NFBLW \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}$$

$$NFC = NFCLW \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}$$

Parameter Modification due to Stress Effects

The stress model of BSIM4.4.0 has been adopted in PSP without any modifications. The PSP parameters affected are BETN, THESAT, VFB, AF, and CF.

© 2023 Cadence Design Systems, Inc.

Layout Effects for Regular Shapes

$$Inv_sa = \frac{1}{SA + 0.5 \cdot L}$$

$$Inv_sb = \frac{1}{SB + 0.5 \cdot L}$$

$$Inv_sa_{ref} = \frac{1}{SAREF + 0.5 \cdot L}$$

$$Inv_sb_{ref} = \frac{1}{SBREF + 0.5 \cdot L}$$

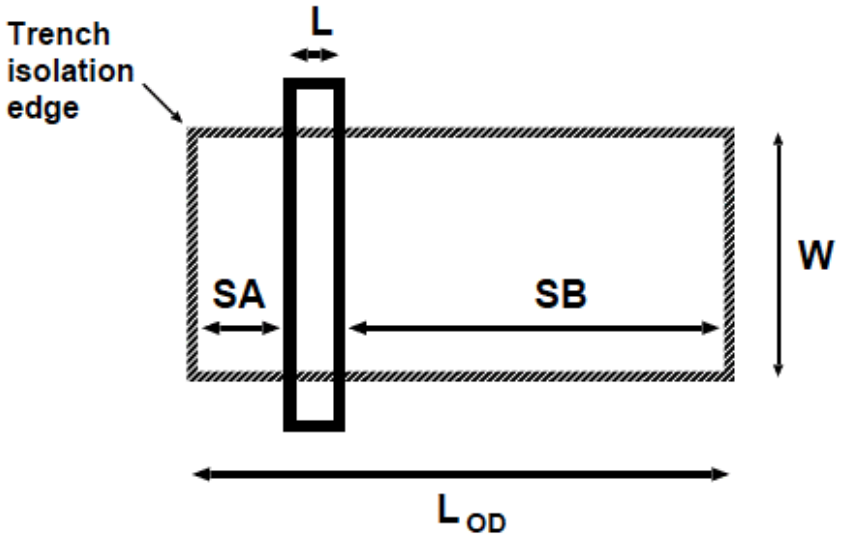


Figure 24-3 Typical layout of a MOSFET. LOD = SA + SB + L, where OD is gate oxide definition

© 2023 Cadence Design Systems, Inc.

Layout Effects for Irregular Shapes

For irregular shapes, the following effective values for **SA** and **SB** are to be used. You have to provide these values manually or by a layout extraction tool.

$$\frac{1}{SAEFF + 0.5 \cdot L} = \sum_{i=1}^{n} \frac{SWi}{W} \cdot \frac{1}{SAi + 0.5 \cdot L}$$

$$\frac{1}{SABFF + 0.5 \cdot L} = \sum_{i=1}^{n} \frac{SWi}{W} \cdot \frac{1}{SAB + 0.5 \cdot L}$$

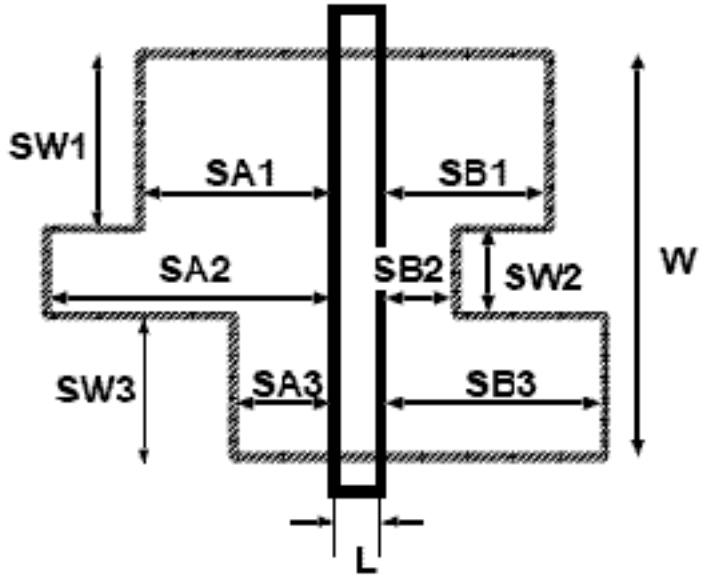


Figure: A typical layout of MOS devices with more instance parameters (SWi, SAi and SBi) in addition to the traditional L and W)

© 2023 Cadence Design Systems, Inc.

Calculation of Parameter Modifications

Mobility-Related Equations

$$Kstress_u0 = \left(1 + \frac{LKU0}{(L + \Delta L_{PS})^{LLODKU0}} + \frac{WKU0}{(W + \Delta W_{OD} + WLOD)^{WLODKU0}} + \frac{PKU0}{(L + \Delta L_{PS})^{LLODKU0} \cdot (W + \Delta W_{OD} + WLOD)^{WLODKU0}}\right) \cdot \left(1 + TKU0 \cdot \left(\frac{T_{KD}}{T_{KR}} - 1\right)\right)$$

$$\rho\beta = \frac{KU0}{Kstress_u0} \cdot (Inv_sa + Inv_sb)$$

$$\rho\beta, ref = \frac{KU0}{Kstress_u0} \cdot (Inv_sa_{ref} + Inv_sb_{ref})$$

$$BETN = \frac{1 + \rho\beta}{1 + \rho\beta, ref} \cdot BETN_{ref}$$

$$THESAT = \frac{1 + \rho\beta}{1 + \rho\beta, ref} + \frac{1 + KVSAT \cdot \rho\beta, ref}{1 + KVSAT \cdot \rho\beta} \cdot THESAT_{ref}$$

© 2023 Cadence Design Systems, Inc.

Threshold-Voltage-Related Equations

$$Kstress_vth0 = 1 + \frac{LKVTH0}{(L + \Delta L_{PS})^{LLODKVTH}} + \frac{WKVTH0}{(W + \Delta W_{OD} + WLOD)^{WLODKVTH}} + \frac{PKU0}{(L + \Delta L_{PS})^{LLODVTH} \cdot (W + \Delta W_{OD} + WLOD)^{WLODVTH}}$$

$$\Delta Inv_s = Inv_sa + Inv_sb - Inv_sa_{ref} - Inv_sb_{ref}$$

$$VFB = VFB_{ref} + KVTH0 \cdot \frac{\Delta Inv_s}{Kstress_vth0}$$

$$AF = AF_{ref} + STK2 \cdot \frac{\Delta Inv_s}{Kstress_vth0^{LODK2}}$$

$$CF = CF_{ref} + STETA0 \cdot \frac{\Delta Inv_s}{Kstress_vth0^{LODETA0}}$$

Well Proximity Effects

The well proximity effect (WPE) model from BSIM4.5.0 has been adopted in PSP with two changes relative to BSIM4.5.0:

- In the original BSIM parameter names all zeros have been replaced by ‘O’s in order to comply with PSP naming convention.
- The BSIM parameter K2WE is not available in PSP. Except for some trivial conversion of parameters BSIM-PSP, WPE parameters from BSIM can be used directly in PSP.

The local PSP parameters affected by the WPE equations are VFB and BETN.

After modification of the local parameters by the WPE equations, clipping is applied according to the *Intrinsic Parameters for the model* section.

- If SCA, SCB, SCC and SC are all set to 0, the WPE equations are not computed.
- The WPE equations are calculated when SWGEO = 1 or 2.

© 2023 Cadence Design Systems, Inc.

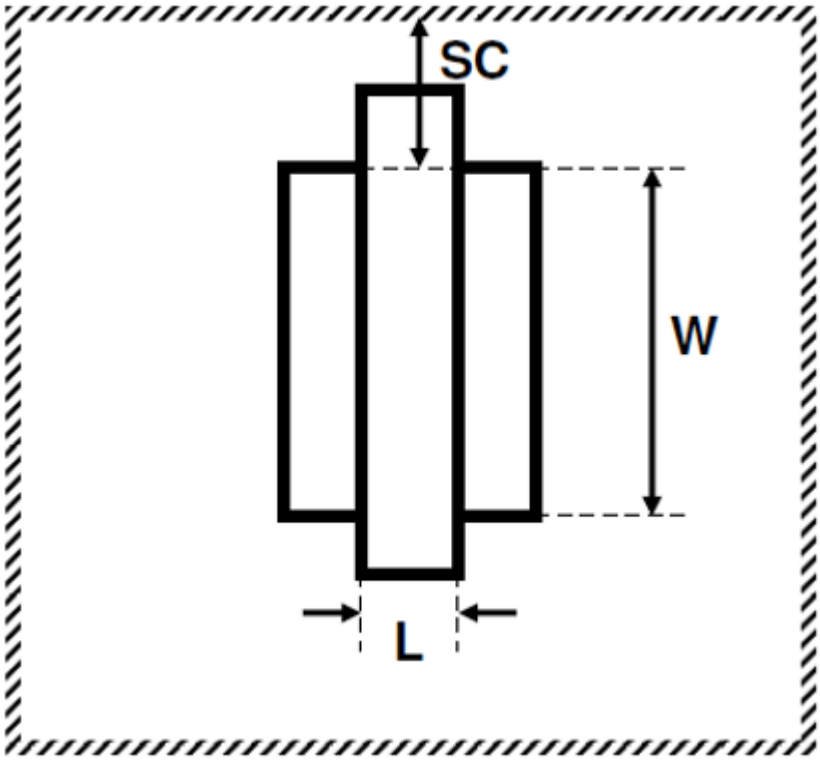
Parameters for Pre-layout Simulation

If SCA = SCB = SCC = 0 and SC > 0, SCA, SCB, and SCC will be computed from SC as shown below. Here, SC should be taken as the distance to the nearest well edge (see figure below). If any of the parameters SCA, SCB, or SCC are positive, all three values as supplied will be used and SC will be ignored.

If SCA = SCB = SCC = 0 and SC > 0

$$\mathrm{SCA} = \frac{\mathrm{SCREF}^2}{W_\mathrm{f}} \cdot \left(\frac{1}{\mathrm{SC}} - \frac{1}{\mathrm{SC} + W_\mathrm{f}} \right)$$

The following figure shows a layout of MOS devices for pre-layout simulation using estimated value for SC.



© 2023 Cadence Design Systems, Inc.

$$\mathbf{SCB} = \frac{1}{W_f \cdot \mathbf{SCREF}} \cdot \left[\frac{\mathbf{SCREF}}{10} \cdot \mathbf{SC} \cdot \exp\left(-10 \cdot \frac{\mathbf{SC}}{\mathbf{SCREF}}\right) + \frac{\mathbf{SCREF}^2}{100} \cdot \exp\left(-10 \cdot \frac{\mathbf{SC}}{\mathbf{SCRE}\right.\right.$$

$$\left. - \frac{\mathbf{SCREF}}{10} \cdot (\mathbf{SC} + W_f) \cdot \exp\left(-10 \cdot \frac{\mathbf{SC} + W_f}{\mathbf{SCREF}}\right)\right.$$

$$\left. - \frac{\mathbf{SCREF}}{10} \cdot (\mathbf{SC} + W_f) \cdot \exp\left(-10 \cdot \frac{\mathbf{SC} + W_f}{\mathbf{SCREF}}\right)\right.$$

$$\left. - \frac{\mathbf{SCREF}^2}{100} \cdot \exp\left(-10 \cdot \frac{\mathbf{SC} + W_f}{\mathbf{SCREF}}\right)\right]$$

$$\mathbf{SCC} = \frac{1}{W_f \cdot \mathbf{SCREF}} \cdot \left[\frac{\mathbf{SCREF}}{20} \cdot \mathbf{SC} \cdot \exp\left(-20 \cdot \frac{\mathbf{SC}}{\mathbf{SCREF}}\right) + \frac{\mathbf{SCREF}^2}{400} \cdot \exp\left(-20 \cdot \frac{\mathbf{SC}}{\mathbf{SCRE}\right.\right.$$

$$\left. - \frac{\mathbf{SCREF}}{20} \cdot (\mathbf{SC} + W_f) \cdot \exp\left(-20 \cdot \frac{\mathbf{SC} + W_f}{\mathbf{SCREF}}\right)\right.$$

Calculation of Parameter Modifications

The calculation of Kvthowe and Kuowe is given in sections for Global Model or Binning Model.

$$\mathbf{VFB} = \mathbf{VFB}_{\mathrm{ref}} + K_{\mathrm{vthowe}} \cdot (\mathbf{SCA} + \mathbf{WEB} \cdot \mathbf{SCB} + \mathbf{WEC} \cdot \mathbf{SCC})$$

$$\mathbf{BETN} = \mathbf{BETN}_{\mathrm{ref}} \cdot [1 + K_{\mathrm{uowe}} \cdot (\mathbf{SCA} + \mathbf{WEB} \cdot \mathbf{SCB} + \mathbf{WEC} \cdot \mathbf{SCC})]$$

© 2023 Cadence Design Systems, Inc.

Asymmetric Junctions

From PSP 102.3 onward, asymmetric junction can be modeled in PSP. This includes asymmetric source-bulk and drain-bulk junctions, GIDL/GISL, overlap gate currents, overlap capacitances and outer fringe capacitances. The asymmetric junction model can be switched on by using the parameter SWJUNASYM. If SWJUNASYM = 1, the new parameters for the drain side are used all together. Those whose values are not explicitly specified in the model card are set to their default value, not to their counterparts for the source side. In other words, it is not possible to activate the parameters for the drain side on a one-by-one basis. The physical scaling and binning rules to calculate the related local parameters for the drain side are given separately in this chapter.

If SWJUNASYM = 0, the related parameters for the drain side are ignored. Effectively, the following assignments are applied before evaluation of the calculations described in the next section.

If SWJUNASYM = 0:

$$\mathrm{TOXOVD} = \mathrm{TOXOV}$$

$$\mathrm{NOVD} = \mathrm{NOV}$$

$$\mathrm{AGIDLD} = \mathrm{AGIDL}$$

$$\mathrm{BGIDLD} = \mathrm{BGIDL}$$

$$\mathrm{STBGIDLD} = \mathrm{STBGIDL}$$

$$\mathrm{CGIDLD} = \mathrm{CGIDL}$$

$$\mathrm{IGOVD} = \mathrm{IGOV}$$

$$\mathrm{CGOVD} = \mathrm{CGOV}$$

$$\mathrm{CFRD} = \mathrm{CFR}$$

Related Topics

PSP102 Model

© 2023 Cadence Design Systems, Inc.

Model Usage

History and Development

BSIM4 Level-14 Model (bsim4)

Model Equations

Non-Quasi-Static (NQS) RF Model

Component Statements for PSP102 Models

Model Equations

Calculation of Internal Parameters (including Temperature Scaling)

Calculation of Transistor Temperature

$$T_{KR} = T_0 + TR$$

$$T_{KD} = T_0 + T_A + DTA$$

$$\Delta T = T_{KD} - T_{KR}$$

$$\phi_T = \frac{k_B \cdot T_{KD}}{q}$$

© 2023 Cadence Design Systems, Inc.

Calculation of Local Process Parameters

$$\phi^*_T = \phi_T \cdot \left(1 + CT \cdot \frac{T_{KR}}{T_{KD}}\right)$$

$$V_{FB} = VFB + STVFB \cdot \Delta T$$

$$E_g/q = 1.179 - 9.025 \cdot 10^{-5} \cdot T_{KD} - 3.05 \cdot 10^{-7} \cdot {T_{KD}}^2$$

$$r_T = (1.045 + 4.5 \cdot 10^{-4} \cdot T_{KD}) \cdot (0.523 + 1.4 \cdot 10^{-3} \cdot T_{KD} - 1.48 \cdot 10^{-6} \cdot {T_{KD}}^2)$$

$$n_i = 2.5 \cdot 10^{25} \cdot {rT}^{3/4} \cdot (T_{KD}/300)^{3/2} \cdot \exp\left(-\frac{E_g/q}{2 \cdot \phi_T}\right)$$

$$\phi_B^{cl} = MAX(2 \cdot \phi_T \cdot \ln[(NSUB)/n_i], 0.05)$$

$$C_{ox} = \varepsilon_{ox}/(TOX)$$

$$\gamma_0 = \sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot NSUB/C_{ox}}$$

$$G_0^{cl} = \gamma_0/(\sqrt{\phi_T})$$

Calculation of Polysilicon Depletion Parameter

$$kp = \begin{cases} \text{if } NP \le 1 \text{ or } NP \ge 10^{28} & \{kp = 0 \\ \text{if } 1 < NP < 10^{28} & \begin{cases} NP_1 = MAX(NP, 8 \cdot 10^7/TOX^2) \\ NP_2 = MAX(NP_1, 3 \cdot 10^2) \\ kp = (2 \cdot \phi_T \cdot C_{ox}^2)/(q \cdot \varepsilon_{Si} \cdot NP^2) \end{cases} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Calculation of Quantum-Mechanical Correction Parameters

$$q_{lim} = 10 \cdot \phi_T$$

$$q_q = \begin{cases} 0.4 \cdot QMC \cdot QM_N \cdot C_{ox}^{2/3} & for\ NMOS \\ 0.4 \cdot QMC \cdot QM_p \cdot C_{ox}^{2/3} & for\ \text{PMOS} \end{cases}$$

$$q_{b0} = \gamma_0 \cdot \sqrt{\phi_B^{cl}}$$

$$\phi_B = \phi_B^{cl} + 0.75 \cdot q_q \cdot q_{b0}^{2/3}$$

$$G_0 = G_0^{cl} \cdot (1 + q_q \cdot q_{b0}^{-2/3})$$

$$\phi_X = 0.95 \cdot \phi_B$$

$$a_\phi = 2.5 \cdot 10^{-5} \cdot \phi_b^2$$

$$\phi^*_X = MAXA(\phi_X, 0, a_\phi) = 0.95000658 \cdot |\phi_B|$$

Calculation of Local Process Parameters in Gate Overlap Regions

$$\gamma_{ov} = \sqrt{2 \cdot q \cdot \varepsilon_{Si} \cdot NOV} \cdot (TOXOV)/\varepsilon_{ox}$$

$$G_{ov} = \gamma_{ov}/(\sqrt{\phi_T})$$

$$\xi_{ov} = 1 + G_{ov}/(\sqrt{2})$$

$$x_{mrgov} = 10^{-5} \cdot \xi_{ov}$$

Calculation of Lateral Gradient Factor Parameters

$$B_f = MIN\left(BF, \frac{1 - F0}{F0 + 0.01}\right)$$

© 2023 Cadence Design Systems, Inc.

Calculation of Mobility Parameters

$$\beta = BETN \cdot C_{ox} \cdot (T_{KR}/T_{KD})^{STBET}$$

$$\theta_{\mu} = THEMU \cdot (T_{KR}/T_{KD})^{STTHEMU}$$

$$\mu_E = MUE \cdot (T_{KR}/T_{KD})^{STMUE}$$

$$X_{cor} = XCOR \cdot (T_{KR}/T_{KD})^{STXCOR}$$

$$C_S = CS \cdot (T_{KR}/T_{KD})^{STCS}$$

$$E_{eff0} = 10^{-8} \cdot C_{ox}/\varepsilon_{Si}$$

$$\eta_{\mu} = \begin{cases} 1/2 & for\ \text{NMOS} \\ 1/3 & for\ \text{PMOS} \end{cases}$$

Calculation of Series Resistance Parameters

$$R_s = RS \cdot (T_{KR}/T_{KD})^{STRS}$$

$$\theta_R = 2 \cdot \beta \cdot R_s$$

Calculation of Velocity Saturation Parameter

$$\theta_{sat} = A2 \cdot (T_{KR}/T_{KD})^{STTHESAT}$$

Calculation of Impact-Ionization Parameter

$$\alpha_2 = A2 \cdot (T_{KD}/T_{KR})^{STA2}$$

© 2023 Cadence Design Systems, Inc.

Calculation of Gate Current Parameters

$$I_{GINV} = IGINV \cdot (T_{KD}/T_{KR})^{STIG}$$

$$I_{GOV} = A2IGOV \cdot (T_{KD}/T_{KR})^{STIG}$$

$$B = \frac{4}{3} \cdot \frac{TOX}{h} \cdot \sqrt{2 \cdot q \cdot m_0 \cdot CHIB} = 6.830909 \cdot 10^9 \cdot TOX \cdot \sqrt{CHIB}$$

$$B_{ov} = B \cdot (TOXOV)/(TOX)$$

$$GC_q = \begin{cases} -0.99 \cdot \dfrac{GC2}{2 \cdot GC3} & if\ GC3 < 0 \\ 0 & if\ GC3 \geq 0 \end{cases}$$

$$\alpha_b = \frac{E_g/q + \phi_B}{2}$$

$$D_{ch} = GC0 \cdot \phi^*_T$$

$$D_{ov} = GC0 \cdot \phi_T$$

Calculation of Gate–Induced Drain Leakage Parameters

$$A_{GIDL} = AGIDL \cdot \left(\frac{2 \cdot 10^{-9}}{TOXOV}\right)^2$$

$$B_{GIDL} = BGIDL \cdot MAX([1 + STBGIDL \cdot \Delta T], 0) \cdot \left(\frac{TOXOV}{2 \cdot 10^{-9}}\right)$$

Calculation of Noise Parameter

$$N_T = FNT \cdot 4 \cdot k_B \cdot T_{KD}$$

© 2023 Cadence Design Systems, Inc.

Calculation of Additional Internal Parameters

$$x_1 = 1.25$$

$$x_{g1} = \chi_1 + G_{ov} \cdot \sqrt{\exp(-\chi_1) + \chi_1 - 1}$$

Conditioning of Terminal Voltages

$$V^*_{GB} = V_{GS} + V_{SB} - V_{FB}$$

$$x_g = V^*_{GB} / \phi^*_T$$

$$V^*_{SB} = MAXA(V_{SB} + \phi_X, 0, a_\phi) - \phi^*_X$$

$$V^*_{DB} = V_{DS} + V^*_{SB}$$

Bias-Dependent Body Factor

$$D_{nsub} = DNSUB \cdot MAXA(0, V_{GS} + V_{SB} - VNSUB, NSLP)$$

$$G = G_0 \cdot \sqrt{1 + D_{nsub}}$$

© 2023 Cadence Design Systems, Inc.

Lateral Gradient Factor

$$V_{dsx} = \sqrt{V_{DS}^{\ 2} + 0.010.01}$$

$$V_{sbx} = V^{*}_{SB} + \frac{V_{DS} - V_{dsx}}{2}$$

$$V_{sbx1} = MAXA(V_{sbx}, 0, 10^{-4})$$

$$F_{DIBL} = CF \cdot V_{dsx} \cdot (1 + CF \cdot V_{dsx}) \cdot (1 + CFB \cdot V_{sbx})$$

$$f_0 = \frac{F0}{1 + AF \cdot V_{sbx} + B_f \cdot V_{sbx1} + F_{DIBL}} + 0.01$$

$$B_t = (f_0 - 0.01) \cdot B_f \cdot \phi^{*}_{X}$$

$$\tilde{x_0} = \frac{\phi_B + V_{sbx}}{\phi^{*}_{T}}$$

$$x_{gc} = MAXA(\chi_g, 0, 50)$$

$$x_{subf} = \frac{\chi_{gc}^{2}}{\chi_{gc} + \frac{G^2 \times f_0}{2} + G \cdot \sqrt{B_t \cdot \chi_{gc}^{2} + f_0 \cdot \chi_{gc} + \left(\frac{G \cdot f_0}{2}\right)^2}}$$

$$\eta f = MINA(\chi_{subf}, \tilde{\chi_0} + 3, 5)$$

$$a_f = (\chi_{gc} - \eta_f)^2 - G^2 \cdot \eta_f \cdot (f_0 + B_t \cdot \eta_f)$$

$$c_f = 2 \cdot (\chi_{gc} - \eta_f) + G^2 \cdot (f_0 + 2 \cdot B_t \cdot \eta_f)$$

$$\tau = \tilde{\chi}_0 - \eta_f + \ln(a_f / G^2)$$

$$x_f = \sigma\left(\frac{a_f}{1 - B_t \cdot G^2}, \frac{c_f}{1 - B_t \cdot G^2}, \tau, \eta_f\right)$$

$$f = f_0 + B_t \cdot \chi_f$$

© 2023 Cadence Design Systems, Inc.

Surface Potential at Source Side and Related Variables

$$G_f = G \cdot \sqrt{f}$$

$$\xi = 1 + G_f/(\sqrt{2})$$

$$x_{ns} = \frac{\phi_B + V^*_{SB}}{\phi^*_T}$$

$$\Delta_{ns} = \exp(-\chi_{ns})/f$$

$$x_{mrg} = 10^{-5} \cdot \xi$$

$$\text{if } x_g < -x_{mrg} \quad \begin{cases} y_g = -x_g \\ z = 1.25 \cdot y_g/\xi \\ \eta = \left[z + 10 - \sqrt{(z-6)^2 + 64}\right]/2 \\ a = (y_g - \eta)^2 + G_f^2 \cdot (\eta + 1) \\ c = 2 \cdot (y_g - \eta) - G_f^2 \\ \tau = -\eta + \ln(a/G_f^2) \\ y_0 = \sigma_1(a, c, \tau, \eta) \\ \Delta_0 = EXP(y_0) \\ p = 2 \cdot (y_g - y_0) + G_f^2 \cdot [\Delta_0 - 1 + \Delta_{ns} \cdot (1 - \chi'(y_0) - 1/\Delta_0)] \\ q = (y_g - y_0)^2 + G_f^2 \cdot [y_0 - \Delta_0 + 1 + \Delta_{ns} \cdot (1 + \chi(y_0) - 1/\Delta_0 - 2 \cdot y_0)] \\ x_s = -y_0 - \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot \left\{2 - G_f^2 \cdot [\Delta_0 + \Delta_{ns} \cdot (1/\Delta_0 - x^n(y_0))]\right\}}} \end{cases}$$

$$\text{if } |x_g| \le x_{mrg} \quad \left\{x_s = \frac{x_g}{\xi}, \left[1 + G_f \cdot x_g \cdot \frac{1 - \Delta_{ns}}{\xi^2 \cdot 6 \cdot \sqrt{2}}\right]\right.$$

© 2023 Cadence Design Systems, Inc.

$$
\text{if } x_g > x_{mrg} = \begin{cases}
\hat{x}_{g1} = x_1 + G_f \cdot \sqrt{\exp(-x_1) + x_1 - 1} \\
\bar{x} = \frac{x_g}{\xi} \cdot [1 + x_g \cdot (\xi \cdot x_1 - \hat{x}_{g1})/x_{g1}^2] \\
x_0 = x_g + G_f^2/2 - G_f \cdot \sqrt{x_g + G_f^2/4 - 1 + \exp(-\bar{x})} \\
b_x = x_{ns} + 0.5 + 2.5 \cdot f \\
\eta = MINA(x_0, b_x, 5) - \left(b_x - \sqrt{b_x^2 + 5}\right)/2 \\
a = (x_g - \eta)^2 - G_f^2 \cdot [\exp(-\eta) + \eta - 1 - \Delta_{ns} - (\eta + 1 + \chi(\eta))] \\
b = 1 - G_f^2 \cdot [\exp(-\eta) - \Delta_{ns} \cdot x^n(\eta)] \\
c = 2 \cdot (x_g - n) + G_f^2 \cdot [1 - \exp(-\eta) - \Delta_{ns} \cdot (1 + x'(\eta))] \\
\tau = x_{ns} - \eta + \ln(a/G^2) \\
y_0 = a_2(a, b, c, \tau, \eta) \\
\Delta_0 = \exp(y_0) \\
p = 2 \cdot (x_g - y_0) + G_f^2 \cdot [1 - 1/\Delta_0 + \Delta_{ns} \cdot (\Delta_0 - 1 - (y_0))] \\
x_s = \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot \left\{2 - G_f^2 \cdot [1/\Delta_0 + \Delta_{ns} \cdot (\Delta_0 - x^n(y_0))]\right\}}}
\end{cases}
$$

The values of E_s, D_s, and P_s are calculated only for $x_g>0$.

$$E_s = \exp(-x_s)$$

$$D_s = [1/E_s - x_s - 1 - x(x_s)] \cdot \Delta_{ns}$$

$$P_s = x_s - 1 + E_s$$

$$x_{gs} = \begin{cases} x_g - x_s & \text{for } x_g \le 0 \\ G_f \cdot \sqrt{D_s + P_s} & \text{for } x_g > 0 \end{cases}$$

$$\psi_{ss} = \phi^*_T \cdot x_s$$

© 2023 Cadence Design Systems, Inc.

Drain Saturation Voltage

All the equations in this sections have been calculated for $x_g>0$.

$$q_{is} = \frac{G_f^2 \cdot \phi^*_T \cdot D_s}{x_{gs} + G_f \cdot \sqrt{P_s}}$$

$$\alpha_s = 1 + \frac{G_f \cdot (1 - E_s)}{2 \cdot \sqrt{P_s}}$$

$$q_{bs} = \phi^*_T \cdot G_f \cdot \sqrt{P_s}$$

$$\rho_s = \theta_R \cdot \frac{1 + RSB \cdot V_{sbx}}{1 + RSG \cdot q_{is}} \cdot q_{is}$$

$$\mu_x = \frac{1 + X_{cor} \cdot V_{sbx}}{1 + 0.2 \cdot X_{cor} \cdot V_{sbx}}$$

$$E_{effs,s} = E_{eff0} \cdot (q_{bs} + \eta_\mu \cdot q_{is})$$

$$G_{mob,s} = \frac{1 + (\mu_E \cdot E_{eff,s})^{\theta_\mu} + C_S \cdot \left(\frac{q_{bs}}{q_{is} + q_{bs}}\right)^2 + \rho_s}{\mu_x}$$

$$w_{sat,s} = \frac{100 \cdot q_{is} \cdot (1 + THESATB \cdot V_{sbx})}{100 + q_{is} \cdot (1 + THESATB \cdot V_{sbx})}$$

$$\theta^*_{sat,s} = \frac{\theta_{sat,s}}{G_{mob,s}} \cdot (1 + THESATG \cdot w_{sat,s})$$

$$\phi_\infty = q_{is}/\alpha_s + \phi^*_T$$

© 2023 Cadence Design Systems, Inc.

$$y_{sat} = \begin{cases} \theta^*_{sat,s} \cdot \phi_\infty / (\sqrt{2}) & \text{for NMOS} \\ \dfrac{\theta^*_{sat,s} \cdot \phi_\infty / (\sqrt{2})}{\sqrt{1 + \theta^*_{sat,s} \cdot \phi_\infty / (\sqrt{2})}} & \text{for PMOS} \end{cases}$$

$$\phi_2 = \frac{\phi^*_T \cdot G_f^2 \cdot D_s \cdot SO}{a_{sat} + \sqrt{a_{sat}^2 - G_f^2 \cdot D_s \cdot SO}}$$

$$\phi_{sat} = \frac{2 \cdot \phi_0 \cdot \phi_2}{\phi_0 + \phi_2 + \sqrt{(\phi_0 + \phi_2)^2 - 3.96 \cdot \phi_0 \cdot \phi_2}}$$

$$V_{dsat} = \phi_{sat} - \phi^*_T \cdot \ln\left[1 + \frac{\phi_{sat} \cdot (\phi_{sat} - 2 \cdot a_{sat} \cdot \phi^*_T)}{G_f^2 \cdot D_s \cdot \phi_T^{*2}}\right]$$

$$V_{dse} = \frac{V_{DS}}{[1 + (V_{DS}/V_{dsat})^{AX}]^{1/(AX)}}$$

© 2023 Cadence Design Systems, Inc.

Surface Potential at Drain Side and Related Variables

$$x_{nd} = \frac{\phi_B + V^*_{SB} + V_{dse}}{\phi^*_T}$$

$$k_{ds} = \exp(-V_{dse}/\phi^*_T)$$

$$if\ x_g \le x_{mrg} \qquad \left\{ x_d = \frac{x_g}{\xi} \cdot \left[1 + G_f \cdot x_g \cdot \frac{1 - \Delta_{nd}}{\xi^2 \cdot 6 \cdot \sqrt{2}} \right] \right.$$

© 2023 Cadence Design Systems, Inc.

$$\text{if } x_g > x_{mrg} \quad \begin{cases} b_x = x_{nd} + 0.5 + 2.5 \cdot f \\ \eta = MINA(x_0, b_x, 5) - \left(b_x - \sqrt{b_x^2 + 5}\right)/2 \\ a = (x_g - \eta)^2 - G_f^2 \cdot [\exp(-\eta) + \eta - 1 - \Delta_{nd} \cdot (\eta + 1 + x(\eta))] \\ b = 1 - G_f^2/2 \cdot [\exp(-\eta) - \Delta_{nd} \cdot x^n(\eta)] \\ c = 2 \cdot (x_g - \eta) + G_f^2 \cdot [1 - \exp(-\eta) - \Delta_{nd} \cdot (1 + x'(\eta))] \\ \tau = x_{nd} - \eta + \ln\langle a/G^2 \rangle \\ y_0 = \sigma_2(a, b, c, \tau, \eta) \\ \Delta_0 = \exp(y_0) \\ p = 2 \cdot (x_g - y_0) + G_f^2 \cdot [1 - 1/\Delta_0 + \Delta_{nd} \cdot (\Delta_0 - 1 - x'(y_0))] \\ q = (x_g - y_0)^2 - G_f^2 \cdot [y_0 + 1/\Delta_0 - 1 + \Delta_{nd} \cdot (\Delta_0 - y_0 - 1 - x'(y_0))] \\ x_d = y_0 + \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot \left\{2 - G_f^2 \cdot [1/\Delta_0 + \Delta_{nd} \cdot (\Delta_0 - x^n(y_0))]\right\}}} \end{cases}$$

$$x_{ds} = x_d - x_s$$

$$\text{if } x_{ds} < 10^{-10} \quad \begin{cases} p = 2 \cdot x_{gs} + G_f^2 \cdot [1 - E_s + \Delta_{nd} \cdot (1/E_s - 1 - x'(x_s))] \\ q = G_f^2 \cdot (1 - k_{ds}) \cdot D_s \\ \xi = 1 - G_f^2 \cdot [E_s + \Delta_{nd}(1/E_s - x^n(x_s))] \\ x_{ds} = \dfrac{2 \cdot q}{p + \sqrt{p^2 - 4 \cdot \xi \cdot q}} \\ x_d = x_s + x_{ds} \end{cases}$$

$$E_d = \exp(-x_d)$$

$$D_d = (1/E_d - x_d - 1 - (x_d)) \cdot \Delta_{nd}$$

$$\Delta\psi = \phi_T^* \cdot x_{ds}$$

$$\psi_{sd} = \phi_T^* \cdot x_d$$

© 2023 Cadence Design Systems, Inc.

Mid-Point Surface Potential and Related Variables

$$if\ x_g > 0 \quad \begin{cases} x_m = (x_s + x_d)/2 \\ E_m = \sqrt{E_s \cdot E_d + 10^{-40}} \\ \bar{D} = (D_s + D_d)/2 \\ D_m = \bar{D} + x_{ds}^2/8 \cdot (E_m - 2/G_f^2) \\ P_m = x_m - 1 + E_m \\ x_{gm} = G_f \cdot \sqrt{D_m + P_m} \end{cases}$$

$$if\ x_g \le 0 \quad \begin{cases} x_m = x_s \\ x_{gm} = x_g - x_s \end{cases}$$

Polysilicon Depletion

The equations in this section are only calculated for $k_P > 0$ and $x_g > 0$ (otherwise $\eta_p = 1$).

$$x_m^{(0)} = x_m \ , D_m^{(0)} = D_m \ , E_m^{(0)} = E_m \ , \Delta\psi^{(0)} = \Delta\psi$$

$$d_0 = 1 - E_m^{(0)} + 2 \cdot X_{gm}/G_f^2$$

$$\eta_p = 1/(\sqrt{1 + kp \cdot x_{gm}})$$

$$x_{pm} = kp \cdot \left[\frac{\eta_p \cdot x_{gm}}{1 + \eta_p}\right] \cdot \frac{D_m^{(0)}}{D_m^{(0)} + P_m}$$

$$p = 2 \cdot (x_{gm} - x_{pm}) + G_f^2 \cdot (1 - E_m^{(0)} + D_m^{(0)})$$

$$q = x_{pm} \cdot (x_{pm} - 2 \cdot x_{gm})$$

$$\xi_p = 1 - G_f^2/2 \cdot (E_m^{(0)} + D_m^{(0)})$$

© 2023 Cadence Design Systems, Inc.

$$u_p = \frac{p \cdot q}{p^2 - \xi_p \cdot q}$$

$$x_m = x_m^{(0)} + u_p$$

$$E_m = E_m^{(0)} \cdot \exp(-u_p)$$

$$D_m = D_m^{(0)} \cdot \exp(-u_p)$$

$$P_m = x_m - 1 + E_m$$

$$x_{gm} = G_f \cdot \sqrt{D_m + P_m}$$

$$\Delta\psi = \Delta\psi^{(0)} \cdot \frac{\exp(u_p) \cdot [\bar{D} + d_0]}{1 - E_m + 2 \cdot x_{gm} \cdot \eta_p / G_f^2 + \exp(u_p) \cdot \bar{D}}$$

Potential Mid-Point Inversion Charge and Related Variables

The equations in this section are only calculated for $x_g > 0$.

$$q_{im} = \frac{G_f^2 \cdot \phi_T^* \cdot D_m}{x_{gm} + G_f \cdot \sqrt{P_m}}$$

$$\alpha_m = \eta_p + \frac{G_f \cdot (1 - E_m)}{2 \cdot \sqrt{P_m}}$$

$$q_{im}^* = q_{im} + \phi_T^* \cdot \alpha_m$$

$$q_{bm} = \phi_T^* \cdot G_f \cdot \sqrt{P_m}$$

© 2023 Cadence Design Systems, Inc.

Series Resistance

$$\rho = \theta_R \cdot \frac{1 + RSB \cdot V_{sbx}}{1 + RSG \cdot q_{im}} \cdot q_{im}$$

Mobility Reduction

$$E_{eff} = E_{eff0} \cdot (q_{bm} + \eta_\mu \cdot q_{im})$$

$$G_{mob} = \frac{1 + (\mu_E \cdot E_{eff})^{\theta_\mu} + C_S \cdot \left(\frac{q_{bm}}{q_{im} + q_{bm}}\right) + \rho}{\mu_x}$$

Drain-Source Channel Current

Channel Length Modulation

$$R_1 = q_{im} / q_{im}^*$$

$$R_2 = \phi_T^* \cdot \alpha_m / q_{im}^*$$

$$\Delta L / L = ALP \cdot \frac{V_{DS}}{V_{DS} + \phi_T^*} \cdot \ln\left(1 + \frac{V_{DS} - \Delta\psi}{VP}\right)$$

$$G_{\Delta L} = \frac{1}{1 + \Delta L/L + (\Delta L/L)^2}$$

$$\Delta L_1 / L = \left[ALP + \frac{ALP1}{q_m^*} \cdot R_1 + ALP2 \cdot q_{bm} \cdot R_2^2\right] \cdot \frac{V_{DS}}{V_{DS} + \phi_T^*} \cdot \ln\left(1 + \frac{V_{DS} - \Delta\psi}{VP}\right)$$

$$F_{\Delta L} = 1 + \Delta L_1 / L + (\Delta L_1 / L)^2$$

© 2023 Cadence Design Systems, Inc.

Velocity Saturation

$$w_{sat} = \frac{100 \cdot q_{im} \cdot (1 + THESATB \cdot V_{sbx})}{100 + q_{im} \cdot (1 + THESATB \cdot V_{sbx})}$$

$$\theta^*_{sat} = \frac{\theta_{sat}}{G_{mob} \cdot G_{\Delta L}} \cdot (1 + THESATG \cdot w_{sat})$$

$$z_{sat} = \begin{cases} (\theta^*_{sat} \cdot \Delta\psi)^2 & for\ \text{NMOS} \\ \dfrac{(\theta^*_{sat} \cdot \Delta\psi)^2}{1 + \theta^*_{sat} \cdot \Delta\psi} & for\ \text{PMOS} \end{cases}$$

$$G_{vsat} = \frac{G_{mob} \cdot G_{\Delta L}}{2} \cdot (1 + \sqrt{1 + 2 \cdot z_{sat}})$$

Drain-Source Channel Current

$$I_{DS} = \begin{cases} 0 & for\ x_g \le 0 \\ \beta \cdot F_{\Delta L} \cdot \dfrac{q^*_{im}}{G_{vsat}} \cdot \Delta\psi & for\ x_g > 0 \end{cases}$$

Variables for Calculation of Intrinsic Charges and Gate Current

The equations in this section are calculated only for $x_g > 0$.

$$V_{oxm} = \theta^*_T \cdot x_{gm}$$

$$\alpha'_m = \alpha_m \cdot \left[1 + \frac{z_{sat}}{2} \cdot \left(\frac{G_{mob} \cdot G_{\Delta L}}{G_{vsat}}\right)^2\right]$$

$$H = \frac{G_{mob} \cdot G_{\Delta L}}{G_{vsat}} \cdot \frac{q^*_{im}}{\alpha'_m}$$

© 2023 Cadence Design Systems, Inc.

Impact Ionization or Weak-Avalanche

The equations in this section are calculated when SWIMPACT = 1 and only for $x_g > 0$.

$$a^*_2 = a_2 \cdot [1 + A4 \cdot (\sqrt{V^*_{SB} + \phi_B} - \sqrt{\phi_B})]$$

$$\Delta V_{sat} = V_{DS} - A3 \cdot \Delta\psi$$

$$M_{av1} = \begin{cases} 0 & for\ \Delta V_{sat} \le 0 \\ A1 \cdot \Delta V_{sat} \cdot \exp(\Delta\psi) & for\ \Delta V_{sat} > 0 \end{cases}$$

$$I_{av1} = M_{av1} \cdot I_{DS}$$

© 2023 Cadence Design Systems, Inc.

Surface Potential in Gate Overlap Regions

$$x_{ov}(x_g) = \begin{cases} \text{if } x_g < -x_{mrgov} \\ \text{if } |x_g| < x_{mrgov} \end{cases} \begin{cases} y_g = -x_g \\ z = x_1 \cdot y_g / \xi_{ov} \\ \eta = \left[z + 10 - \sqrt{(z-6)^2 + 64} \right] / 2 \\ a = (y_g - \eta)^2 + G_{ov}^2 \cdot (\eta + 1) \\ c = 2 \cdot (y_g - \eta) - G_{ov}^2 \\ \tau = -\eta + \ln(a / G_{ov}^2) \\ y_0 = \sigma_1(a, c, \tau, \eta) \\ \Delta_0 = \exp(y_0) \\ p = 2 \cdot (y_g - y_0) + G_{ov}^2 \cdot (\Delta_0 - 1) \\ q = (y_g - y_0)^2 + G_{ov}^2 \cdot (y_0 - \Delta_0 + 1) \\ x_{ov} = \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot (2 - G_{ov}^2 \cdot \Delta_0)}} \\ \{ x_{ov} = x_g / \xi_{ov} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$x_{ov}(x_g) = \begin{cases} \text{if } x_g < -x_{mrgov} & \begin{cases} y_g = -x_g \\ z = x_1 \cdot y_g / \xi_{ov} \\ \eta = \left[z + 10 - \sqrt{(z-6)^2 + 64} \right] / 2 \\ a = (y_g - \eta)^2 + G_{ov}^2 \cdot (\eta + 1) \\ c = 2 \cdot (y_g - \eta) - G_{ov}^2 \\ \tau = -\eta + \ln(a / G_{ov}^2) \\ y_0 = \sigma_1(a, c, \tau, \eta) \\ \Delta_0 = \exp(y_0) \\ p = 2 \cdot (y_g - y_0) + G_{ov}^2 \cdot (\Delta_0 - 1) \\ q = (y_g - y_0)^2 + G_{ov}^2 \cdot (y_0 - \Delta_0 + 1) \\ x_{ov} = \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot (2 - G_{ov}^2 \cdot \Delta_0)}} \end{cases} \\ \text{if } |x_g| < x_{mrgov} & \{ x_{ov} = x_g / \xi_{ov} \\ \text{if } x_g > x_{mrgov} & \begin{cases} \bar{x} = x_g / \xi_{ov} \cdot [1 + x_g \cdot (\xi_{ov} \cdot x_1 - x_{g1}) / x_{g1}^2] \\ w = 1 - \exp(-\bar{x}) \\ x_0 = x_g + G_{ov}^2 / 2 - G_{ov} \cdot \sqrt{x_g + G_{ov}^2 / 4 - w} \\ p = 2 \cdot (x_g - x_0) + G_{ov}^2 \cdot (1 + \Delta_0) \\ q = (x_g - x_0)^2 - G_{ov}^2 \cdot (x_0 + \Delta_0 - 1) \\ x_{ov} = x_0 + \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot (2 - G_{ov}^2 \cdot \Delta_0)}} \end{cases} \end{cases}$$

$$\psi_{sov} = -\phi_T \cdot x_{ov}\left(-\frac{V_{GS}}{\phi_T} \right)$$

$$\psi_{dov} = -\phi_T \cdot x_{ov}\left(-\frac{V_{GS} - V_{DS}}{\phi_T} \right)$$

© 2023 Cadence Design Systems, Inc.

$$V_{ov0} = V_{GS} - \Psi_{sov}$$

$$V_{ovL} = V_{GS} - V_{DS} - \Psi_{dov}$$

Gate Current

The equations in this section are calculated when SWIGATE = 1.

Source/Drain Gate Overlap Current

The gate tunneling currents in both gate/source and gate/drain overlap are given by:

$$I_{Gov}(V_{GX}, \Psi_{ov}, V_{ov}) = \begin{cases} V^*_{ov} = \sqrt{V_{ov}^2 + 10^{-6}} \\ \Psi_{tov} = MINA(0, V_{ov} + D_{ov}, 0.01) \\ z_g = \begin{cases} MINA\left(\frac{V^*_{ov}}{CHIB}, GC_Q, 10^{-6}\right) & for\ GC3 < 0 \\ \frac{V^*_{ov}}{CHIB} & for\ GC3 \geq 0 \end{cases} \\ \Delta_{Siov} = \exp\left(\frac{3.0 \cdot \phi_T + \Psi_{ov} + \Psi_{tov}}{\phi_T}\right) \\ F_{Sov} = \ln\left[\frac{1 + \Delta_{Siov}}{1 + \Delta_{Siov} \cdot \exp(-V_{GX}/\phi_T)}\right] \\ I_{GOV} = I_{GOV} \cdot F_{Sov} \cdot \exp\left(B_{ov} \cdot \left[-\frac{3}{2} + z_g \cdot (GC2 + GC3 \cdot z_g)\right]\right) \end{cases}$$

$$I_{GSov} = I_{GOV}(V_{GS}, \Psi_{sov}, V_{ovo})$$

$$I_{GDov} = I_{GOV}(V_{GS} - V_{DS}, \Psi_{dov}, V_{ovL})$$

© 2023 Cadence Design Systems, Inc.

Gate-Channel Current

$$V_m = V^*_{SB} + \phi^*_T \cdot \left[x_m - x_s - \ln\left(\frac{1 + \exp(V_{dse}/\phi^*_T)}{2} \right) \right]$$

$$\psi_T = MINA(0, V_{oxm} + D_{ch}, 0.01)$$

$$V^*_{oxm} = \sqrt{V^2_{oxm} + 10^{-6}}$$

$$z_g = \begin{cases} MINA\left(\frac{V^*_{oxm}}{CHIB}, GC_Q, 10^{-6} \right) & for\ GC3 < 0 \\ \frac{V^*_{oxm}}{CHIB} & for\ GC3 \geq 0 \end{cases}$$

$$\Delta_{Si} = \exp\left(x_m - \frac{\alpha_b + V_m - \psi_t}{\phi^*_T} \right)$$

$$F_S = \ln\left[\frac{1 + \Delta_{Si}}{1 + \Delta_{Si} \cdot \exp\left(-\frac{V_{HS} + V_{SB} - V_m}{\phi^*_T} \right)} \right]$$

$$I_{GCO} = I_{GINV} \cdot F_S \cdot \exp\left(B \cdot \left[-\frac{3}{2} + z_g \cdot (GC2 + GC3 \cdot z_g) \right] \right)$$

$$if\ x_g > 0 \quad \begin{cases} u_0 = CHIB/[B \cdot (GC2 + 2 \cdot GC3 \cdot z_g)] \\ x = \Delta\psi/(2 \cdot u_0) \\ b = u_0/H \\ B_b = b \cdot (1 - b)/2 \\ A_g = 1/2 - 3 \cdot B_g \\ p_{gc} = (1 - b) \cdot \frac{\sinh(x)}{x} + b \cdot \cosh(x) \\ p_{gd} = \frac{p_{gc}}{2} - B_g \cdot \sinh(x) - A_g \cdot \frac{\sinh(x)}{x} \cdot \left[\coth(x) - \frac{1}{x} \right] \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$if\ x_g \le 0 \qquad \begin{cases} p_{gc} = 1 \\ p_{gd} = 1/2 \end{cases}$$

$$\text{M}\ S_g = \frac{1}{2} \cdot \left(1 + \frac{x_g}{\sqrt{x^2 + 10^{-6}}}\right)$$

$$I_{GC} = I_{GCO} \cdot p_{gc} \cdot S_g$$

$$I_{GCD} = I_{GCO} \cdot p_{gd} \cdot S_g$$

$$I_{GSD} = I_{GC} - I_{GCD}$$

$$I_{GB} = I_{GCO} \cdot p_{gc} \cdot (1 - S_g)$$

Gate-Induced Drain/Source Leakage Current

The equations in this section are calculated when SWGIDL = 1.

$$I_{gixl(V_{ov}, V)} = \begin{cases} V_{tov} = \sqrt{V_{ov}^2 + CGIDL^2 \cdot V^2 + 10^{-6}} \\ t = V \cdot V_{tov} \cdot V_{ov} \\ I_{gixl} = \begin{cases} -A_{GIDL} \cdot t \cdot \exp\left(-\dfrac{B_{GIDL}}{V_{tov}}\right) & for\ V_{ov} > 0 \\ 0 & for\ V_{ov} \ge 0 \end{cases} \end{cases}$$

$$I_{gisl} = I_{gixl}(V_{ov0}, V_{SB})$$

$$I_{gidl} = I_{gixl}(V_{ovl}, V_{DS} + V_{SB})$$

© 2023 Cadence Design Systems, Inc.

Total Terminal Currents

$$I_D = I_{DS} + I_{avl} - I_{GDOV} - I_{GCD} + I_{gidl}$$

$$I_S = -I_{DS} - I_{GSov} - I_{GCS} + I_{gisl}$$

$$I_G = I_{GC} + I_{GB} + I_{GDov} + I_{GSov}$$

$$I_B = -I_{avl} - I_{GB} - I_{gidl} - I_{gisl}$$

Quantum-Mechanical Corrections

$$q_{eff} = \begin{cases} V_{oxm} & for\ x_g \le 0 \\ q_{bm} + \eta_\mu \cdot q_m & for\ x_g > 0 \end{cases}$$

$$C_{OX}^{qm} = \begin{cases} COX & for\ q_q = \\ \dfrac{COX}{1 + q_q / (qeff^2 + qlim^2)^{1/6}} & for\ q_q > 0 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Intrinsic Charge Model

$$if\ x_g > 0 \quad \begin{cases} F_1 = \Delta\psi/(2\cdot H) \\ q\Delta L = (1-G_{\Delta L})\cdot(q_{im}-\alpha_{am}\cdot\Delta\psi/2) \\ q^*{}_{\Delta L} = q\Delta L\cdot(1+G_{\Delta L}) \\ Q_G^{(i)} = C_{OX}^{qm}\cdot\left[V_{oxm}+\dfrac{\eta_p\cdot\Delta\psi}{2}\cdot\left(\dfrac{G_{\Delta L}}{3}\cdot F_j+G_{\Delta L}-1\right)\right] \\ Q_I^{(i)} = -C_{OX}^{qm}\cdot\left[G_{\Delta L}\cdot\left(q_{im}+\dfrac{\alpha\cdot\Delta\psi}{6}\cdot F_j\right)+q\Delta L\right] \\ Q_D^{(i)} = \dfrac{C_{OX}^{qm}}{2}\cdot\left[G_{\Delta L}^2\cdot\left(q_{im}+\dfrac{\alpha\cdot\Delta\psi}{6}\cdot\left[\dfrac{F_j^2}{5}+F_j-1\right]\right)+q^*{}_{\Delta L}\right] \end{cases}$$

$$if\ x_g \le 0 \quad \begin{cases} Q_G^{(i)} = C_{OX}^{qm}\cdot V_{oxm} \\ Q_I^{(i)} = 0 \\ Q_D^{(i)} = 0 \end{cases}$$

$$Q_S^{(i)} = Q_I^{(i)} - Q_D^{(i)}$$

$$Q_B^{(i)} = Q_I^{(i)} - Q_G^{(i)}$$

Extrinsic Charge Model

The charges of the source and drain overlap regions

$$Q_{sov} = CGOV\cdot(V_{GS}-\psi_{sov})$$

$$Q_{dov} = CGOV\cdot(V_{GS}-V_{DS}-\psi_{dov})$$

The charge of the bulk overlap region

$$Q_{bov} = CGBOV\cdot(V_{GS}-V_{SB})$$

© 2023 Cadence Design Systems, Inc.

Inner fringe charge correction

$$\Delta Q_S = IFK \cdot (1 + IFC \cdot V^*_{SB}) \cdot \sqrt{MAXA(IFVBI + V^*_{SB} - \psi_{ss}, 0, 10^{-3})}$$

$$\Delta Q_D = IFK \cdot (1 + IFC \cdot V^*_{DB}) \cdot \sqrt{MAXA(IFVBI + V^*_{DB} - \psi_{sd}, 0, 10^{-3})}$$

$$\Delta Q_G = -\Delta Q_S - \Delta Q_D$$

Outer fringe charge

$$Q_{ofs} = CFR \cdot V_{GS}$$

$$Q_{ofd} = CFR \cdot (V_{GS} - V_{DS})$$

Total Terminal Charges

$$Q_G = Q_G^{(i)} + Q_{sov} + Q_{dov} + \Delta Q_G + Q_{ofs} + Q_{ofd} + Q_{bov}$$

$$Q_s = Q_S^{(i)} - Q_{sov} + \Delta Q_S - Q_{ofs}$$

$$Q_D = Q_D^{(i)} - Q_{dov} + \Delta Q_D - Q_{ofd}$$

$$Q_B = Q_B^{(i)} - Q_{bov}$$

© 2023 Cadence Design Systems, Inc.

Noise Model

The equations in this section are only calculated for $x_g > 0$. In these equations f_{op} represents the operation frequency of the transistor and $j = -1^{1/2}$.

$$N^* = \frac{C_{ox}}{q} \cdot \alpha_m \cdot \phi_T$$

$$N^*_m = \frac{C_{ox}}{q} \cdot q^*_m$$

$$\Delta N = \frac{C_{ox}}{q} \cdot \alpha_m \cdot \Delta\psi$$

$$S_{fl} = \frac{q \cdot \phi_T^2 \cdot \beta \cdot I_{DS}}{f_{op} \cdot C_{ox} \cdot G_{vsat} \cdot N^*} \cdot \left[(NFA - NFB \cdot N^* + NFC \cdot N^{*2}) \cdot \ln\left(\frac{N^*_m + \Delta N/2}{N^*_m - \Delta N/2}\right) + (NFB + NFC \cdot N^*_m - 2 \cdot N^*) \cdot \Delta N \right]$$

$$H_0 = \frac{q^*_{im}}{\alpha_m}$$

$$t_1 = \frac{q_{im}}{q^*_{im}}$$

$$t_2 = \left(\frac{\Delta\psi}{2 \cdot H_0}\right)^2$$

$$R = \frac{H_0}{H} - 1$$

$$l_c = 1 - 12 \cdot t_2 \cdot R$$

$$g_{ideal} = \frac{\beta \cdot q^*_{im}}{G_{vsat}} \cdot F_{\Delta L}$$

$$C_{Geff} = \left(\frac{G_{vsat}}{G_{mob} \cdot G_{\Delta L}}\right)^2 \cdot COX \cdot \eta_p$$

$$m_{id} = \frac{g_{ideal}}{l_c^2} \cdot [t_1 + 12 \cdot t_2 - 24 \cdot (1 + t_1) \cdot t_2 \cdot R]$$

$$S_{th} = N_T \cdot m_{id}$$

$$m_{ig} = \frac{1}{l_c^2 \cdot g_{ideal}} \cdot \left[\frac{t_1}{12} - t_2 \cdot \left(t_1 + \frac{1}{5} - 12 \cdot t_2\right) - \frac{8}{5} \cdot t_2 \cdot (t_1 + 1 - 12 \cdot t_2) \cdot R\right]$$

© 2023 Cadence Design Systems, Inc.

$$S_{ig} = N_T \cdot \frac{(2 \cdot \pi \cdot f_{op} \cdot C_{Geff})^2 \cdot m_{ig}}{1 + (2 \cdot \pi \cdot f_{op} \cdot C_{Geff} \cdot m_{ig})^2}$$

$$m_{igid} = \frac{\sqrt{t_2}}{l_c^2} \cdot \left[1 - 12 \cdot t_2 - \left(t_1 + \frac{96}{5} \cdot t_2 - 12 \cdot t_1 \cdot t_2\right) \cdot R\right]$$

$$S_{igth} = N_T \cdot \frac{2 \cdot \pi \cdot j \cdot f_{op} \cdot C_{Geff} \cdot m_{igid}}{1 + 2 \cdot \pi \cdot j \cdot f_{op} \cdot C_{Geff} \cdot m_{ig}}$$

Gate Current Shot Noise

$$S_{hotgs} = 2 \cdot q \cdot I_{js}$$

$$S_{hotgd} = 2 \cdot q \cdot (I_{GCD} + I_{GDov})$$

Avalanche Current Shot Noise

$$S_{jnoise} = 2 \cdot q \cdot (1 + M_{avl}) \cdot I_{avl}$$

$$D_{jnoise} = 2 \cdot q \cdot (1 + M_{avl}) \cdot I_{avl} + I_{jd}$$

Related Topics

PSP102 Model

Model Usage

History and Development

Structure of PSP102

Geometrical Scaling and Stress Model for Intrinsic MOSFET

Non-Quasi-Static (NQS) RF Model

© 2023 Cadence Design Systems, Inc.

Component Statements for PSP102 Models

© 2023 Cadence Design Systems, Inc.

Non-Quasi-Static (NQS) RF Model

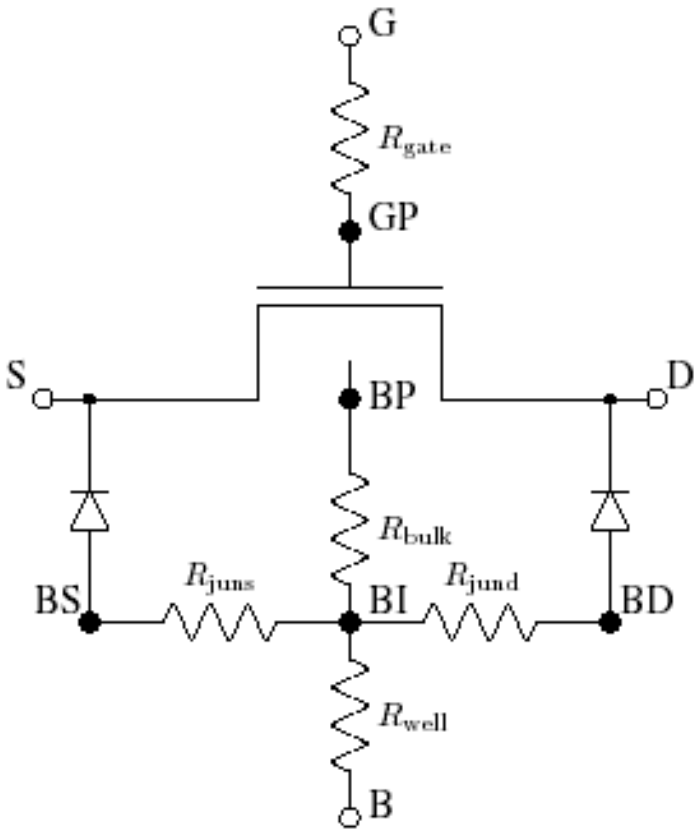
For high-frequency modeling and fast transient simulations, a special version of the PSP model is available, which enables the simulation of non-quasi-static (NQS) effects, and includes several parasitic resistances.

$$\begin{cases} \frac{dQ_1}{dt} = f_1(Q1, \ldots, Q_N) \\ \frac{dQ_N}{dt} = f_N(Q1, \ldots, Q_N) \end{cases}$$

Q_i is the charge density at the i-th collocation point and f_i are functions, which contain the complete PSP-charge model.

© 2023 Cadence Design Systems, Inc.

Parasitics Circuit



$$S_{R_G} = 4 \cdot k_B \cdot T_{KD} \cdot R_{gate}$$

$$S_{R_{BULK}} = 4 \cdot k_B \cdot T_{KD} \cdot R_{bulk}$$

$$S_{R_{WELL}} = 4 \cdot k_B \cdot T_{KD} \cdot R_{well}$$

$$S_{R_{JUNS}} = 4 \cdot k_B \cdot T_{KD} \cdot R_{juns}$$

$$S_{R_{JUND}} = 4 \cdot k_B \cdot T_{KD} \cdot R_{jund}$$

© 2023 Cadence Design Systems, Inc.

Additional NQS and RF Parameters

The PSP-NQS model has a few additional parameters, which are described in the tables below. The allowed values for the parameter SWNQS are 0, 1, 2, 3, 5, and 9. If SWNQS = 0, then NQS effects are switched off, i.e. the intrinsic MOS model is identical to the standard PSP-model (however, the parasitics-circuit is still in place). If SWNQS is nonzero, it indicates the number of collocation points to be used in the NQS-calculations. A higher value increases the accuracy, but leads to an increased computational burden.

Additional Parameters for Global NQS Model

Name	Unit	Default	Min	Max	Description
SWNQS	–	0	0	9	Switch for NQS effects / number of collocation points
MUNQSO	–	1	–	–	Relative mobility for NQS modeling
RGO	–	10^{-3}	–	–	Gate resistance R_{gate}
RBULKO	–	10^{-3}	–	–	Bulk resistance R_{bulk}
RWELLO	–	10^{-3}	–	–	Well resistance R_{well}
RJUNSO	–	10^{-3}	–	–	Source-side bulk resistance R_{juns}
RJUNDO	–	10^{-3}	–	–	Drain-side bulk resistance R_{jund}

Geometrical Scaling Rules for the NQS RF Model

Although the parasitic resistances are (in general) dependent on geometry, the actual form of this dependency is be strongly influenced by the device layout. For this reason, L and W dependence of these resistances is currently not included in PSP; the correct values must be supplied manually for each geometry.

The following (trivial) scaling rules are included for the NQS-model.

$$MUNQS = MUNQSO$$

$$RG = RGO$$

$$RBULK = RBULKO$$

$$RWELL = RWELLO$$

© 2023 Cadence Design Systems, Inc.

$$RJUNS = RJUNSO$$

$$RJUND = RJUNDO$$

Equations for the NQS RF Model

In this section, y denotes the (normalized) position along the channel ($y = 0$ is source side, $y = 1$ is drain side), while x denotes the surface potential (normalized to ϕ*T) at a certain position.

In PSP 101.0 and before, only SWNQS=0,1,2,3,5,9 are allowed.

$$n = SWNQS + 1$$

$$h = 1/n$$

Initial Values

$$A_{i,j} = 0 \qquad for 0 \le i, j \le n$$

$$v_i = 0 \qquad for 0 \le i \le n$$

First Loop

$$\left.\begin{array}{l} p = 2 + v_{i-1}/2 \\ v_i = -1/(2 \cdot p) \\ A_{i,i-1} = 1/h \\ A_{i,i} = -2/h \\ A_{i,i+1} = 1/h \\ A_{i,j} = \frac{1}{p} \cdot (3 \cdot A_{i,j}/h - A_{i-1,j/2}) \end{array}\right\} \begin{array}{l} for j = 0 \ldots n \\ \\ \\ \\ \\ \\ \end{array} \left.\begin{array}{l} \\ \\ \\ \\ \\ \\ \end{array}\right\} for i = 1 \ldots (n-1)$$

Second Loop (Back Substitution)

$$A_{i,j} = v_i \cdot A_{i+1,j} + A_{i,j} \qquad for\ j = 0 \ldots n \} \qquad for\ i = (n-1) \ldots 0$$

© 2023 Cadence Design Systems, Inc.

Position Independent Quantities

$$If\ x_g > 0 \begin{cases} y_m = \frac{1}{2} \cdot \left(1 + \frac{\Delta\psi}{4 \cdot H}\right) \\ p_d = \frac{x_{gm}}{x_g - x_m} \\ G_P = G / p_d \end{cases}$$

$$If\ x_g \le 0 \begin{cases} y_m = \frac{1}{2} \\ p_d = 1 \\ G_P = G / p_d \end{cases}$$

$$a_p = 1 + G_p / \sqrt{2}$$

$$p_{mrg} = 10^{-5} \cdot a_p$$

Position Dependent Surface Potential and Charge

Interpolated (quasi-static) surface potential along the channel:

$$\psi(y) = x_m + \frac{H}{\phi_T^*} \cdot \left(1 - \sqrt{1 - \frac{2 \cdot \Delta\psi}{H} \cdot (y - y_m)}\right)$$

© 2023 Cadence Design Systems, Inc.

Normalized bulk-charge and its first two derivatives as functions of surface potential:

$$q_b(x) = -\mathrm{sgn}(x) \cdot G_p \cdot \sqrt{\exp(-x) + x - 1}$$

$$q'_b(x) = \frac{G_P^2 \cdot [1 - \exp(-x)]}{2 \cdot q_b(x)}$$

$$q''_b(x) = q'_b(x) - \frac{q'_b(x)^2 - G_P^2/2}{qb(x)}$$

© 2023 Cadence Design Systems, Inc.

$$II_{(x_g)} = \begin{cases} \text{if } x_g < -p_{mrg} & \begin{cases} y_g = -x_g \\ z = 1.25 \cdot y_g / a_p \\ \eta = \left[z + 10 - \sqrt{(z-6)^2 + 64} \right] / 2 \\ a = (y_g - \eta)^2 + G_P^2 \cdot (\eta + 1) \\ c = 2 \cdot (y_g - \eta) - G_P^2 \\ r = -\eta + \ln(a / G_P^2) \\ y_0 = \sigma_1(a, c, \tau, \eta) \\ \Delta_0 = \exp(y_0) \\ \xi = 1 - G_P^2 \cdot \Delta_0 / 2 \\ p = 2 \cdot (y_g - y_0) + G_P^2 \cdot (\Delta_0 - 1) \\ q = (y_g - y_0)^2 + G_P^2 \cdot (y_0 - \Delta_0 + 1) \\ II = -y_0 - \dfrac{2 \cdot q}{p + \sqrt{p^2 - 4 \cdot q \cdot \xi}} \end{cases} \\ \text{if } |x_g| \le -p_{mrg} & \left\{ II = \dfrac{x_g}{a_p} \right. \\ \text{if } x_g > x_{mrg} & \begin{cases} \hat{x}_{g1} = x_1 + G \cdot \sqrt{\exp(-x_1) + x_1 - 1} \\ \bar{x} = \dfrac{x_g}{a_p} \cdot [1 + x_g \cdot (x_g + a_p / \hat{x}_{g1} - 1) / \hat{x}_{g1}] \\ x_0 = x_g + G_P^2/2 - G_P \cdot \sqrt{x_g + G_P^2/4 - 1 + \exp(-\bar{x})} \\ \Delta_0 = \exp(-x_0) \\ \xi = 1 - G_P^2 \cdot \Delta_0 / 2 \\ p = 2 \cdot (x_g - x_0) + G_P^2 \cdot (1 - \Delta_0) \\ q = (x_g - x_0)^2 - G_P^2 \cdot (x_0 + \Delta_0 - 1) \\ II = x_0 + \dfrac{2 \cdot q}{p + \sqrt{p^2 - 4 \cdot q \cdot \xi}} \end{cases} \end{cases}$$

$$X(x_g, q_{inv}) = II(x_g + q_{inv} / p_d)$$

© 2023 Cadence Design Systems, Inc.

Auxiliary Functions

$$q(x) = -p_d \cdot (x_g - x) - q_b(x)$$

$$\psi(q, q_{x1}) = \frac{q}{q_{x1}} - 1$$

$$\phi(q, q_{x1}, q_{x2}) = \left(1 - \frac{q \cdot q_{x2}}{q_{x1}^2}\right) / q_{x1}$$

Normalized right-hand-side of continuity equation

$$f(x_g, q, q', q'') = \begin{cases} x_z = X(x_g, q) \\ q_{x1} = \frac{\partial q}{\partial x}(x_z) = p_d - q'_b(x_z) \\ q_{x2} = \frac{\partial^2 q}{\partial x^2}(x_z) = q''_b(x_z) \\ f_0 = \psi(q, q_{z1}) \cdot q'' + \phi(q, q_{z1}, q_{z2}) \cdot q'^2 \\ x_{y1} = \frac{\partial x_z}{\partial y} = (q')/q_{x1} \\ z_{sat} = \begin{cases} (\theta^*_{sat} \cdot \phi^*_T \cdot x_{y1})^2 \\ \dfrac{(\theta^*_{sat} \cdot \phi^*_T \cdot x_{y1})^2}{1 + \theta^*_{sat} \cdot \Delta\psi} \end{cases} \\ \varsigma = \sqrt{1 + 2 \cdot z_{sat}} \\ F_{vsat} = 2/(1 + \varsigma) \\ f = F_{vsat} \cdot \left[f_0 - F_{vsat} \cdot \frac{z_{sat}}{\varsigma} \cdot \psi(q, q_{x1}) \cdot (q'' + x_{y1}^2 \cdot q''_b(x_z)) \right] \end{cases}$$

$$T_{norm} = \frac{MUNQS \cdot \phi^*_T \cdot \beta}{C^{qm}_{OX} \cdot G_{mob} \cdot G_{\Delta L}}$$

© 2023 Cadence Design Systems, Inc.

Cubic Spline Interpolation

$$q''_0 = 0$$

$$q''_n = 0$$

$$q''_i = \sum_{j=0}^{n} A_{i_j} \cdot q_i \qquad for\ 1 \le i \le n-1$$

$$q'_i = \frac{q_{i+1} - q_i}{h} - \frac{h}{6} \cdot (2 \cdot q''_i \cdot q''_{i+1}) \qquad for\ 1 \le i \le n-1$$

Continuity Equation

$$x_{i,0} = \psi(i \cdot h)$$

$$q_{i,0} = q(x_{i,0})$$

$x_{0,0}=x_s$ and $x_{n,0}=x_d$. Also, these values coincide with those in the quasi-static part of PSP.

The core of the NQS-model is the solution of q(y, t) from the charge continuity equation along the channel. By approximating the y-dependence by a cubic spline through a number of collocation points, the problem is reduced to solving the $q_i(t)$ from the following set of coupled differential equations.

$$\begin{cases} \frac{\partial_{qi}}{\partial t}(t) + T_{norm} \cdot f\left(x_g, q_i(t), \frac{\partial_{qi}}{\partial y}(t), \frac{\partial^2 qi}{\partial y^2}(t)\right) = 0 \\ q_i(0) = q_{i,0} \end{cases} \qquad for\ 1 \le i \le n$$

The boundary points $q_0(t) = q(x_s) = q_{is}$ and $q_n(t) = q(x_d) = q_{id}$ remain fixed to their quasi-static values; they are not solved from the equation above.

© 2023 Cadence Design Systems, Inc.

Non-Quasi-State Terminal Charges

$$S_0 = \sum_{i=1}^{n-1} q_i$$

$$S_2 = \sum_{i=1}^{n-1} q''_i$$

$$q_I^{NQS} = \int_0^1 q(y)dy = h \cdot S_0 + \frac{h}{2} \cdot (u_0 + u_n) - \frac{h^3}{12} \cdot S_2$$

$$U_0 = \sum_{i=1}^{n-1} i \cdot q_i$$

$$U_2 = \sum_{i=1}^{n-1} i \cdot q''_i$$

$$q_D^{NQS} = \int_0^1 q(y)dy = h^2 \cdot U_0 + \frac{h^2}{6} \cdot [q_0 + (3n-1)u_n] - \frac{h^4}{12} \cdot U_2$$

$$q_S^{NQS} = q_I^{NQS} - q_D^{NQS}$$

Currently, only SWNQS = 0; 1; 2; 3; 5; 9 are allowed. For odd values of SWNQS, the gate charge is integrated along the channel using Simpson's rule. If SWNQS = 2, Simpson's 3=8-rule is used.

- If SWNQS is odd (that is, n is even),

$$q_G^{NQS} = pd \cdot \left[x_g - \frac{h}{3} \cdot \left(X(x_g, q_0) + 4 \cdot \sum_{i=1}^{n/2} X(x_g, q2i-1) + 2 \cdot \sum_{i=1}^{n/2-1} X(x_g, q2i) + X(x_g, q_n) \right) \right]$$

- If SWNQS =2 (that is, n=3),

$$q_G^{NQS} = pd \cdot \left[x_g - \frac{3 \cdot h}{8} \cdot (X(x_{g,q0}) + 3 \cdot X(x_{g,q1}) + 3 \cdot X(x_{g,q2}) + X(x_{g,q3})) \right]$$

© 2023 Cadence Design Systems, Inc.

Converting back to conventional units:

$$Q_S^{NQS} = C_{OX}^{qm} \cdot \phi_T^* \cdot q_S^{NQS}$$

$$Q_D^{NQS} = C_{OX}^{qm} \cdot \phi_T^* \cdot q_D^{NQS}$$

$$Q_G^{NQS} = C_{OX}^{qm} \cdot \phi_T^* \cdot q_G^{NQS}$$

$$Q_B^{NQS} = -(Q_S^{NQS} + Q_D^{NQS} + Q_G^{NQS})$$

Related Topics

PSP102 Model

Model Usage

History and Development

Structure of PSP102

Geometrical Scaling and Stress Model for Intrinsic MOSFET

Model Equations

Component Statements for PSP102 Models

© 2023 Cadence Design Systems, Inc.

Component Statements for PSP102 Models

Click the following topics to read about the components statements for the various PSP102 models:

PSP MOSFET Model (PSP102)

PSP MOSFET Model (psp1020)

PSP MOSFET Model (psp1021)

PSP local MOSFET Model (psp102e)

PSP NQS MOSFET Model (pspnqs1020)

PSP NQS MOSFET Model (pspnqs1021)

PSP NQS local MOSFET Model (pspnqs102e)

PSP MOSFET Model (PSP102)

This is SiMKit 3.1.2.

This device is supported within altergroups.

This device is dynamically loaded from the shared object `/<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so`.

Instance Definition

```
InstanceName (d g s b) PSP102ModelName <parameter=value> ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`l=10e-6 m`	Design length.
`w=10e-6 m`	Design width.
`sa=0.0 m`	Distance between OD-edge and poly from one side.
`sb=0.0 m`	Distance between OD-edge and poly from other side.
`sd=0.0 m`	Distance between neighboring fingers.
`sca=0.0`	Integral of the first distribution function for scattered well dopants.
`scb=0.0`	Integral of the second distribution function for scattered well dopants.
`scc=0.0`	Integral of the third distribution function for scattered well dopants.
`sc=0.0 m`	Distance between OD-edge and nearest well edge.
`delvto=0.0 V`	Threshold voltage shift parameter.
`factuo=1.0`	Zero-field mobility pre-factor.
`absource=1E-12 m`^{2}	Bottom area of source junction.
`lssource=1E-6 m`	STI-edge length of source junction.
`lgsource=1E-6 m`	Gate-edge length of source junction.
`abdrain=1E-12 m`^{2}	Bottom area of drain junction.
`lsdrain=1E-6 m`	STI-edge length of drain junction.
`lgdrain=1E-6 m`	Gate-edge length of drain junction.
`as=1E-12 m`^{2}	Bottom area of source junction.
`ps=1E-6 m`	Perimeter of source junction.
`ad=1E-12 m`^{2}	Bottom area of drain junction.
`pd=1E-6 m`	Perimeter of drain junction.
`mulid0=1`	Ids multiplier.
`mult=1.0`	Number of devices in parallel.
`nf=1.0`	Number of fingers.
`ngcon=1.0`	Number of gate contacts.

© 2023 Cadence Design Systems, Inc.

`xgw=1.0E-7 m`	Distance from the gate contact to the channel edge.
`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trise=0.0 K`	Temperature rise from ambient.
`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Definition

```
model modelName psp102 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

`level=102`	Model level.
`type=n`	Channel type parameter. Possible values are `n`: NMOS and `p`: PMOS.
`tr=value of tnom C`	Nominal (reference) temperature.
`swnqs=0`	Flag for NQS, 0,off, 1, 2, 3, 5, or 9,number of collocation points.
`swigate=0`	Flag for gate current, 0,turn off IG.
`swimpact=0`	Flag for impact ionization current, 0,turn off II.
`swgidl=0`	Flag for GIDL current, 0,turn off IGIDL.
`swjuncap=0`	Flag for juncap, 0,turn off juncap.
`swjunasym=0`	Flag for asymmetric junctions; 0,symmetric, 1,asymmetric.
`qmc=1.0`	Quantum-mechanical correction factor.
`version=102.32`	This parameter accepts only a real number values, for example, use 102.21 for the 102.2.1 version. The available versions are 102.2, 102.21(102.2.1), 102.3, 102.32 (102.3.2), 102.33 (102.3.3), 102.34 (102.3.4), 102.4 (102.4.0) and 102.5 (102.5.0).
`geomod=1`	1 for geometrical model and 0 for electrical model.
`binmod=0`	1 for bin model and 0 for non-bin model.
`scalelev=102`	102 for local, 1020 for global model and 1021 for bin model.
`compatible=spectre`	Compatibility parameter. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`vfb=(-1.0) V`	Flatband voltage at TR.
`stvfb=5.0e-4 V/K`	Temperature dependence of VFB.
`tox=2.0e-09 m`	Gate oxide thickness.
`epsrox=3.9`	Relative permittivity of gate dielectric.
`neff=5.0e+23` m^{-3}	Effective substrate doping.
`vnsub=0.0 V`	Effective doping bias-dependence parameter.
`nslp=0.05 V`	Effective doping bias-dependence parameter.

© 2023 Cadence Design Systems, Inc.

`dnsub=0.0 V^-1`	Effective doping bias-dependence parameter.
`dphib=0.0 V`	Offset parameter for PHIB.
`np=1.0e+26 m^-3`	Gate poly-silicon doping.
`ct=0.0`	Interface states factor.
`toxov=2.0e-09 m`	Overlap oxide thickness.
`toxovd=2.0e-09 m`	Overlap oxide thickness for drain side.
`nov=5.0e+25 m^-3`	Effective doping of overlap region.
`novd=5.0e+25 m^-3`	Effective doping of overlap region for drain side.
`cf=0.0`	DIBL-parameter.
`cfb=0.0 V^-1`	Back bias dependence of CF.
`betn=7e-2 m^2/V/s`	Channel aspect ratio times zero-field mobility.
`stbet=1.0`	Temperature dependence of BETN.
`mue=0.5 m/V`	Mobility reduction coefficient at TR.
`stmue=0.0`	Temperature dependence of MUE.
`themu=1.5`	Mobility reduction exponent at TR.
`stthemu=1.5`	Temperature dependence of THEMU.
`cs=0.0`	Coulomb scattering parameter at TR.
`stcs=0.0`	Temperature dependence of CS.
`xcor=0.0 V^-1`	Non-universality factor.
`stxcor=0.0`	Temperature dependence of XCOR.
`feta=1.0`	Effective field parameter.
`rs=30 Ω`	Series resistance at TR.
`strs=1.0`	Temperature dependence of RS.
`rsb=0.0 V^-1`	Back-bias dependence of series resistance.
`rsg=0.0 V^-1`	Gate-bias dependence of series resistance.
`thesat=1.0 V^-1`	Velocity saturation parameter at TR.
`stthesat=1.0`	Temperature dependence of THESAT.
`thesatb=0.0 V^-1`	Back-bias dependence of velocity saturation.
`thesatg=0.0 V^-1`	Gate-bias dependence of velocity saturation.

© 2023 Cadence Design Systems, Inc.

ax=3.0	Linear/saturation transition factor.
alp=0.01	CLM pre-factor.
alp1=0.00 V	CLM enhancement factor above threshold.
alp2=0.00 V^-1	CLM enhancement factor below threshold.
vp=0.05 V	CLM logarithm dependence factor.
a1=1.0	Impact-ionization pre-factor.
a2=10.0 V	Impact-ionization exponent at TR.
sta2=0.0 V	Temperature dependence of A2.
a3=1.0	Saturation-voltage dependence of impact-ionization.
a4=0.0 V^-0.5	Back-bias dependence of impact-ionization.
gco=0.0	Gate tunneling energy adjustment.
iginv=0.0 A	Gate channel current pre-factor.
igov=0.0 A	Gate overlap current pre-factor.
igovd=0.0 A	Gate overlap current pre-factor for drain side.
stig=2.0	Temperature dependence of IGINV and IGOV.
gc2=0.375	Gate current slope factor.
gc3=0.063	Gate current curvature factor.
chib=3.1 V	Tunneling barrier height.
agidl=0.0 A/V^3	GIDL pre-factor.
agidld=0.0 A/V^3	GIDL pre-factor for drain side.
bgidl=41.0 V	GIDL probability factor at TR.
bgidld=41.0 V	GIDL probability factor at TR for drain side.
stbgidl=0.0 V/K	Temperature dependence of BGIDL.
stbgidld=0.0 V/K	Temperature dependence of BGIDL for drain side.
cgidl=0.0	Back-bias dependence of GIDL.
cgidld=0.0	Back-bias dependence of GIDL for drain side.
cox=1.0e-14 F	Oxide capacitance for intrinsic channel.
cgov=1.0e-15 F	Oxide capacitance for gate-drain/source overlap.
cgovd=1.0e-15 F	Oxide capacitance for gate-drain overlap.

© 2023 Cadence Design Systems, Inc.

`cgbov=0.0 F`	Oxide capacitance for gate-bulk overlap.
`cfr=0.0 F`	Outer fringe capacitance.
`cfrd=0.0 F`	Outer fringe capacitance for drain side.
`fnt=1.0`	Thermal noise coefficient.
`fntexc=0.0`	Excess noise coefficient.
`nfa=8.0e+22 V^-1/m`^{4}	First coefficient of flicker noise.
`nfb=3.0e+07 V^-1/m`^{2}	Second coefficient of flicker noise.
`nfc=0.0 V^-1`	Third coefficient of flicker noise.
`ef=1.0`	Flicker noise frequency exponent.
`munqs=1.0`	Relative mobility for NQS modelling.
`rg=0.0` Ω	Gate resistance.
`rbulk=0.0` Ω	Bulk resistance between node BP and BI.
`rwell=0.0` Ω	Well resistance between node BI and B.
`rjuns=0.0` Ω	Source-side bulk resistance between node BI and BS.
`rjund=0.0` Ω	Drain-side bulk resistance between node BI and BD.
`lvaro=0.0 m`	Geometry-independent difference between actual and programmed gate length.
`lvarl=0.0`	Length dependence of LVAR.
`lvarw=0.0`	Width dependence of LVAR.
`lap=0.0 m`	Effective channel length reduction per side.
`wvaro=0.0 m`	Geometry-independent difference between actual and programmed field-oxide opening.
`wvarl=0.0`	Length dependence of WVAR.
`wvarw=0.0`	Width dependence of WVAR.
`wot=0.0 m`	Effective channel width reduction per side.
`dlq=0.0 m`	Effective channel length reduction for CV.
`dwq=0.0 m`	Effective channel width reduction for CV.

© 2023 Cadence Design Systems, Inc.

`vfbo=(-1.0) V`	Geometry-independent flat-band voltage at TR.
`vfbl=0.0`	Length dependence of flat-band voltage.
`vfbw=0.0`	Width dependence of flat-band voltage.
`vfblw=0.0`	Area dependence of flat-band voltage.
`stvfbo=5e-4 V/K`	Geometry-independent temperature dependence of VFB.
`stvfbl=0.0`	Length dependence of temperature dependence of VFB.
`stvfbw=0.0`	Width dependence of temperature dependence of VFB.
`stvfblw=0.0`	Area dependence of temperature dependence of VFB.
`toxo=2e-9 m`	Gate oxide thickness.
`epsroxo=3.9`	Relative permittivity of gate dielectric.
`nsubo=3e23` m^{-3}	Geometry-independent substrate doping.
`nsubw=0.0`	Width dependence of background doping NSUBO due to segregation.
`wseg=1e-8 m`	Character length of segregation of background doping NSUBO.
`npck=1e24` m^{-3}	Pocket doping level.
`npckw=0.0`	Width dependence of pocket doping NPCK due to segregation.
`wsegp=1e-8 m`	Character length of segregation of pocket doping NPCK.
`lpck=1e-8 m`	Character length of lateral doping profile.
`lpckw=0.0`	Width dependence of character length of lateral doping profile.
`fol1=0.0`	First length dependence coefficient for short channel body effect.
`fol2=0.0`	Second length dependence coefficient for short channel body effect.
`vnsubo=0.0 V`	Effective doping bias-dependence parameter.
`nslpo=0.05 V`	Effective doping bias-dependence parameter.
`dnsubo=0.0 V^-1`	Effective doping bias-dependence parameter.
`dphibo=0.0 V`	Geometry-independent offset of PHIB.
`dphibl=0.0 V`	Length dependence offset of PHIB.

© 2023 Cadence Design Systems, Inc.

`dphiblexp=1.0`	Exponent for length dependence of offset of PHIB.
`dphibw=0.0`	Width dependence of offset of PHIB.
`dphiblw=0.0`	Area dependence of offset of PHIB.
`npo=1e26 m^-3`	Geometry-independent gate poly-silicon doping.
`npl=0.0`	Length dependence of gate poly-silicon doping.
`cto=0.0`	Geometry-independent interface states factor.
`ctl=0.0`	Length dependence of interface states factor.
`ctlexp=1.0`	Exponent for length dependence of interface states factor.
`ctw=0.0`	Width dependence of interface states factor.
`ctlw=0.0`	Area dependence of interface states factor.
`toxovo=2e-9 m`	Overlap oxide thickness.
`toxovdo=2e-9 m`	Overlap oxide thickness for drain side.
`lov=0 m`	Overlap length for gate/drain and gate/source overlap capacitance.
`lovd=0 m`	Overlap length for gate/drain overlap capacitance.
`novo=5e25 m^-3`	Effective doping of overlap region.
`novdo=5e25 m^-3`	Effective doping of overlap region for drain side.
`cfl=0.0`	Length dependence of DIBL-parameter.
`cflexp=2.0`	Exponent for length dependence of CF.
`cfw=0.0`	Width dependence of CF.
`cfbo=0.0 V^-1`	Back-bias dependence of CF.
`uo=5e-2 m^2/V/s`	Zero-field mobility at TR.
`fbet1=0.0`	Relative mobility decrease due to first lateral profile.
`fbet1w=0.0`	Width dependence of relative mobility decrease due to first lateral profile.
`lp1=1e-8 m`	Mobility-related characteristic length of first lateral profile.
`lp1w=0.0`	Width dependence of mobility-related characteristic length of first lateral profile.
`fbet2=0.0`	Relative mobility decrease due to second lateral profile.
`lp2=1e-8 m`	Mobility-related characteristic length of second lateral profile.

© 2023 Cadence Design Systems, Inc.

betw1=0.0	First higher-order width scaling coefficient of BETN.
betw2=0.0	Second higher-order width scaling coefficient of BETN.
wbet=1e-9 m	Characteristic width for width scaling of BETN.
stbeto=1.0	Geometry-independent temperature dependence of BETN.
stbetl=0.0	Length dependence of temperature dependence of BETN.
stbetw=0.0	Width dependence of temperature dependence of BETN.
stbetlw=0.0	Area dependence of temperature dependence of BETN.
mueo=0.5 m/V	Geometry-independent mobility reduction coefficient at TR.
muew=0.0	Width dependence of mobility reduction coefficient at TR.
stmueo=0.0	Temperature dependence of MUE.
themuo=1.5	Mobility reduction exponent at TR.
stthemuo=1.5	Temperature dependence of THEMU.
cso=0.0	Geometry-independent coulomb scattering parameter at TR.
csl=0.0	Length dependence of CS.
cslexp=0.0	Exponent for length dependence of CS.
csw=0.0	Width dependence of CS.
cslw=0.0	Area dependence of CS.
stcso=0.0	Temperature dependence of CS.
xcoro=0.0 V^-1	Geometry-independent non-universality parameter.
xcorl=0.0	Length dependence of non-universality parameter.
xcorw=0.0	Width dependence of non-universality parameter.
xcorlw=0.0	Area dependence of non-universality parameter.
stxcoro=0.0	Temperature dependence of XCOR.
fetao=1.0	Effective field parameter.
rsw1=2.5e3 Ω	Source/drain series resistance for 1 um wide channel at TR.
rsw2=0.0	Higher-order width scaling of RS.
strso=1.0	Temperature dependence of RS.
rsbo=0.0 V^-1	Back-bias dependence of series resistance.
rsgo=0.0 V^-1	Gate-bias dependence of series resistance.

© 2023 Cadence Design Systems, Inc.

`thesato=0.0 V^-1`	Geometry-independent velocity saturation parameter at TR.
`thesatl=0.05 V^-1`	Length dependence of THESAT.
`thesatlexp=1.0`	Exponent for length dependence of THESAT.
`thesatw=0.0`	Width dependence of velocity saturation parameter.
`thesatlw=0.0`	Area dependence of velocity saturation parameter.
`stthesato=1.0`	Geometry-independent temperature dependence of THESAT.
`stthesatl=0.0`	Length dependence of temperature dependence of THESAT.
`stthesatw=0.0`	Width dependence of temperature dependence of THESAT.
`stthesatlw=0.0`	Area dependence of temperature dependence of THESAT.
`thesatbo=0.0 V^-1`	Back-bias dependence of velocity saturation.
`thesatgo=0.0 V^-1`	Gate-bias dependence of velocity saturation.
`axo=18`	Geometry-independent linear/saturation transition factor.
`axl=0.4`	Length dependence of AX.
`alpl=5e-4`	Length dependence of ALP.
`alplexp=1.0`	Exponent for length dependence of ALP.
`alpw=0.0`	Width dependence of ALP.
`alp1l1=0.0 V`	Length dependence of CLM enhancement factor above threshold.
`alp1lexp=0.5`	Exponent for length dependence of ALP1.
`alp1l2=0.0`	Second_order length dependence of ALP1.
`alp1w=0.0`	Width dependence of ALP1.
`alp2l1=0.0 V^-1`	Length dependence of CLM enhancement factor below threshold.
`alp2lexp=0.5`	Exponent for length dependence of ALP2.
`alp2l2=0.0`	Second_order length dependence of ALP2.
`alp2w=0.0`	Width dependence of ALP2.
`vpo=0.05 V`	CLM logarithmic dependence parameter.
`a1o=1.0`	Geometry-independent impact-ionization pre-factor.
`a1l=0.0`	Length dependence of A1.

© 2023 Cadence Design Systems, Inc.

a1w=0.0	Width dependence of A1.
a2o=10 V	Impact-ionization exponent at TR.
sta2o=0.0 V	Temperature dependence of A2.
a3o=1.0	Geometry-independent saturation-voltage dependence of II.
a3l=0.0	Length dependence of A3.
a3w=0.0	Width dependence of A3.
a4o=0.0 V^-0.5	Geometry-independent back-bias dependence of II.
a4l=0.0	Length dependence of A4.
a4w=0.0	Width dependence of A4.
gcoo=0.0	Gate tunneling energy adjustment.
iginvlw=0.0 A	Gate channel current pre-factor for 1 um^2 channel area.
igovw=0.0 A	Gate overlap current pre-factor for 1 um wide channel.
igovdw=0.0 A	Gate overlap current pre-factor for 1 um wide channel for drain side.
stigo=2.0	Temperature dependence of IGINV and IGOV.
gc2o=0.375	Gate current slope factor.
gc3o=0.063	Gate current curvature factor.
chibo=3.1 V	Tunneling barrier height.
agidlw=0.0 A/V^3	Width dependence of GIDL pre-factor.
agidldw=0.0 A/V^3	Width dependence of GIDL pre-factor for drain side.
bgidlo=41 V	GIDL probability factor at TR.
bgidldo=41 V	GIDL probability factor at TR for drain side.
stbgidlo=0.0 V/K	Temperature dependence of BGIDL.
stbgidldo=0.0 V/K	Temperature dependence of BGIDL for drain side.
cgidlo=0.0	Back-bias dependence of GIDL.
cgidldo=0.0	Back-bias dependence of GIDL for drain side.
cgbovl=0.0 F	Oxide capacitance for gate-bulk overlap for 1 um long channel.
cfrw=0.0 F	Outer fringe capacitance for 1 um wide channel.
cfrdw=0.0 F	Outer fringe capacitance for 1 um wide channel for drain side.

© 2023 Cadence Design Systems, Inc.

`fnto=1.0`	Thermal noise coefficient.
`fntexcl=0.0`	Length dependence coefficient of excess noise.
`nfalw=8e22 V^-1/m`^{4}	First coefficient of flicker noise for 1 um^2 channel area.
`nfblw=3e7 V^-1/m`^{2}	Second coefficient of flicker noise for 1 um^2 channel area.
`nfclw=0.0 V^-1`	Third coefficient of flicker noise for 1 um^2 channel area.
`efo=1.0`	Flicker noise frequency exponent.
`lintnoi=0.0 m`	Length offset for flicker noise.
`alpnoi=2.0`	Exponent for length offset for flicker noise.
`dta=0 K`	Temperature offset w.r.t. ambient circuit temperature.
`kvthoweo=0`	Geometrical independent threshold shift parameter.
`kvthowel=0`	Length dependent threshold shift parameter.
`kvthowew=0`	Width dependent threshold shift parameter.
`kvthowelw=0`	Area dependent threshold shift parameter.
`kuoweo=0`	Geometrical independent mobility degradation factor.
`kuowel=0`	Length dependent mobility degradation factor.
`kuowew=0`	Width dependent mobility degradation factor.
`kuowelw=0`	Area dependent mobility degradation factor.
`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.
`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
`vgb_max=infinity V`	

© 2023 Cadence Design Systems, Inc.

	Maximum allowed voltage cross gate and bulk.
`vgdr_max=vgd_max V`	
	Maximum allowed reverse voltage cross gate and drain.
`vgsr_max=vgs_max V`	
	Maximum allowed reverse voltage cross gate and source.
`vgbr_max=vgb_max V`	
	Maximum allowed reverse voltage cross gate and bulk.
`vbsr_max=vbs_max V`	
	Maximum allowed reverse voltage cross source and bulk.
`vbdr_max=vbd_max V`	
	Maximum allowed reverse voltage cross source/drain and bulk.
`munqso=1.0`	Relative mobility for NQS modelling.
`rgo=0.0 Ω`	Gate resistance.
`rbulko=0.0 Ω`	Bulk resistance between node BP and BI.
`rwello=0.0 Ω`	Well resistance between node BI and B.
`rjunso=0.0 Ω`	Source-side bulk resistance between node BI and BS.
`rjundo=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
`rint=0.0 Ω/Sqr`	Contact resistance between silicide and ploy.
`rvpoly=0.0 Ω/Sqr`	
	Vertical poly resistance.
`rshg=0.0 Ω/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0.0 m`	Silicide extension over the physical gate length.
`saref=1.0e-6 m`	Reference distance between OD-edge and poly from one side.
`sbref=1.0e-6 m`	Reference distance between OD-edge and poly from other side.
`wlod=0 m`	Width parameter.
`kuo=0 m`	Mobility degradation/enhancement coefficient.
`kvsat=0 m`	Saturation velocity degradation/enhancement coefficient.

© 2023 Cadence Design Systems, Inc.

`tkuo=0`	Temperature dependence of KUO.
`lkuo=0 m^LLODKUO`	Length dependence of KUO.
`wkuo=0 m^WLODKUO`	Width dependence of KUO.
`pkuo=0 m^(LLODKUO+WLODKUO)`	Cross-term dependence of KUO.
`llodkuo=0`	Length parameter for UO stress effect.
`wlodkuo=0`	Width parameter for UO stress effect.
`kvtho=0 Vm`	Threshold shift parameter.
`lkvtho=0 m^LLODVTH`	Length dependence of KVTHO.
`wkvtho=0 m^WLODVTH`	Width dependence of KVTHO.
`pkvtho=0 m^(LLODVTH+WLODVTH)`	Cross-term dependence of KVTHO.
`llodvth=0`	Length parameter for VTH-stress effect.
`wlodvth=0`	Width parameter for VTH-stress effect.
`stetao=0 m`	eta0 shift factor related to VTHO change.
`lodetao=1.0`	eta0 shift modification factor for stress effect.
`scref=10e-6 m`	Distance between OD-edge and well edge of a reference device.
`web=0`	Coefficient for SCB.
`wec=0`	Coefficient for SCC.
`imax=1000 A`	Maximum current up to which forward current behaves exponentially.
`trj=21 C`	Reference temperature.
`cjorbot=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.
`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.
`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.
`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
`idsatrbot=1E-12 Am`$^{-2}$	Saturation current density at the reference temperature of bottom component for source-bulk junction.
`idsatrsti=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
`idsatrgat=1E-18 Am^-1`	

© 2023 Cadence Design Systems, Inc.

	Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
csrhbot=1E2 Am^{-3}	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
csrhsti=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
csrhgat=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.
xjunsti=100E-9 m	Junction depth of STI-edge component for source-bulk junction.
xjungat=100E-9 m	Junction depth of gate-edge component for source-bulk junction.
ctatbot=1E2 Am^{-3}	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
ctatsti=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
ctatgat=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
mefftatbot=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
mefftatsti=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
mefftatgat=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
cbbtbot=1E-12 AV^{-3}	
	Band-to-band tunneling prefactor of bottom component for source-bulk junction.
cbbtsti=1E-18 $AV^{-3}m$	

© 2023 Cadence Design Systems, Inc.

	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
`cbbtgat=1E-18 AV-3m`	
	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
`fbbtrbot=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.
`fbbtrsti=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
`fbbtrgat=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
`stfbbtbot=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
`stfbbtsti=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
`stfbbtgat=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
`vbrbot=10 V`	Breakdown voltage of bottom component for source-bulk junction.
`vbrsti=10 V`	Breakdown voltage of STI-edge component for source-bulk junction.
`vbrgat=10 V`	Breakdown voltage of gate-edge component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component for source-bulk junction.
`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
`cjorbotd=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.
`cjorstid=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.
`cjorgatd=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.
`vbirbotd=1 V`	Built-in voltage at the reference temperature of bottom component for drain-bulk junction.
`vbirstid=1 V`	Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.
`vbirgatd=1 V`	Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.
`pbotd=0.5`	Grading coefficient of bottom component for drain-bulk junction.
`pstid=0.5`	Grading coefficient of STI-edge component for drain-bulk junction.
`pgatd=0.5`	Grading coefficient of gate-edge component for drain-bulk junction.
`phigbotd=1.16 V`	Zero-temperature bandgap voltage of bottom component for drain-bulk junction.
`phigstid=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.
`phiggatd=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

idsatrbotd=1E-12 Am^{-2}	Saturation current density at the reference temperature of bottom component for drain-bulk junction.
idsatrstid=1E-18 Am^-1	Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.
idsatrgatd=1E-18 Am^-1	Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.
csrhbotd=1E2 Am^{-3}	Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.
csrhstid=1E-4 Am^{-2}	Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
csrhgatd=1E-4 Am^{-2}	Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
xjunstid=100E-9 m	Junction depth of STI-edge component for drain-bulk junction.
xjungatd=100E-9 m	Junction depth of gate-edge component for drain-bulk junction.
ctatbotd=1E2 Am^{-3}	Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
ctatstid=1E-4 Am^{-2}	Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
ctatgatd=1E-4 Am^{-2}	Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`mefftatbotd=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
`mefftatstid=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.
`mefftatgatd=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
`cbbtbotd=1E-12 AV`$^{-3}$	Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
`cbbtstid=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.
`cbbtgatd=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.
`fbbtrbotd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.
`fbbtrstid=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.
`fbbtrgatd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.
`stfbbtbotd=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.
`stfbbtstid=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`stfbbtgatd=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.
`vbrbotd=10 V`	Breakdown voltage of bottom component for drain-bulk junction.
`vbrstid=10 V`	Breakdown voltage of STI-edge component for drain-bulk junction.
`vbrgatd=10 V`	Breakdown voltage of gate-edge component for drain-bulk junction.
`pbrbotd=4 V`	Breakdown onset tuning parameter of bottom component for drain-bulk junction.
`pbrstid=4 V`	Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.
`pbrgatd=4 V`	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
`swjunexp=0.0`	Flag for JUNCAP express. Valid values are: ■ `0`: for full mode ■ `1`: for express model.
`vjunref=2.5`	The maximum source-bulk junction voltage; usually about 2*VSUP.
`fjunq=0.03`	Fraction below which source-bulk junction capacitance components are considered negligible.
`vjunrefd=2.5`	The maximum drain-bulk junction voltage; usually about 2*VSUP.
`fjunqd=0.03`	Fraction below which drain-bulk junction capacitance components are considered negligible.
`povfb=(-1) V`	Coefficient for the geometry-independent part of VFB.
`plvfb=0.0 V`	Coefficient for the length dependence of VFB.
`pwvfb=0.0 V`	Coefficient for the width dependence of VFB.
`plwvfb=0.0 V`	Coefficient for the length times width dependence of VFB.
`postvfb=0.0005 V/K`	Coefficient for the geometry-independent part of STVFB.

© 2023 Cadence Design Systems, Inc.

`plstvfb=0.0 V/K`	Coefficient for the length dependence of STVFB.
`pwstvfb=0.0 V/K`	Coefficient for the width dependence of STVFB.
`plwstvfb=0.0 V/K`	Coefficient for the length times width dependence of STVFB.
`potox=2E-09 m`	Coefficient for the geometry-independent part of TOX.
`poepsrox=3.9`	Coefficient for the geometry-independent part of EPSOX.
`poneff=5E+23 m^-3`	Coefficient for the geometry-independent part of NEFF.
`plneff=0.0 m^-3`	Coefficient for the length dependence of NEFF.
`pwneff=0.0 m^-3`	Coefficient for the width dependence of NEFF.
`plwneff=0.0 m^-3`	Coefficient for the length times width dependence of NEFF.
`povnsub=0 V`	Coefficient for the geometry-independent part of VNSUB.
`ponslp=0.05 V`	Coefficient for the geometry-independent part of NSLP.
`podnsub=0 V^-1`	Coefficient for the geometry-independent part of DNSUB.
`podphib=0 V`	Coefficient for the geometry-independent part of DPHIB.
`pldphib=0.0 V`	Coefficient for the length dependence of DPHIB.
`pwdphib=0.0 V`	Coefficient for the width dependence of DPHIB.
`plwdphib=0.0 V`	Coefficient for the length times width dependence of DPHIB.
`ponp=1E+26 m^-3`	Coefficient for the geometry-independent part of NP.
`plnp=0.0 m^-3`	Coefficient for the length dependence of NP.
`pwnp=0.0 m^-3`	Coefficient for the width dependence of NP.
`plwnp=0.0 m^-3`	Coefficient for the length times width dependence of NP.
`poct=0`	Coefficient for the geometry-independent part of CT.
`plct=0.0`	Coefficient for the length dependence of CT.
`pwct=0.0`	Coefficient for the width dependence of CT.
`plwct=0.0`	Coefficient for the length times width dependence of CT.
`potoxov=2E-09 m`	Coefficient for the geometry-independent part of TOXOV.
`potoxovd=2E-09 m`	Coefficient for the geometry-independent part of TOXOV for drain side.
`ponov=5E+25 m^-3`	Coefficient for the geometry-independent part of NOV.
`plnov=0.0 m^-3`	Coefficient for the length dependence of NOV.

© 2023 Cadence Design Systems, Inc.

pwnov=0.0 m^{-3}	Coefficient for the width dependence of NOV.
plwnov=0.0 m^{-3}	Coefficient for the length times width dependence of NOV.
ponovd=5E+25 m^{-3}	Coefficient for the geometry-independent part of NOV for drain side.
plnovd=0.0 m^{-3}	Coefficient for the length dependence of NOV for drain side.
pwnovd=0.0 m^{-3}	Coefficient for the width dependence of NOV for drain side.
plwnovd=0.0 m^{-3}	Coefficient for the length times width dependence of NOV for drain side.
pocf=0	Coefficient for the geometry-independent part of CF.
plcf=0.0	Coefficient for the length dependence of CF.
pwcf=0.0	Coefficient for the width dependence of CF.
plwcf=0.0	Coefficient for the length times width dependence of CF.
pocfb=0 V^-1	Coefficient for the geometry-independent part of CFB.
pobetn=0.07 $m^2/V/s$	Coefficient for the geometry-independent part of BETN.
plbetn=0.0 $m^2/V/s$	Coefficient for the length dependence of BETN.
pwbetn=0.0 $m^2/V/s$	Coefficient for the width dependence of BETN.
plwbetn=0.0 $m^2/V/s$	Coefficient for the length times width dependence of BETN.
postbet=1	Coefficient for the geometry-independent part of STBET.
plstbet=0.0	Coefficient for the length dependence of STBET.
pwstbet=0.0	Coefficient for the width dependence of STBET.
plwstbet=0.0	Coefficient for the length times width dependence of STBET.
pomue=0.5 m/V	Coefficient for the geometry-independent part of MUE.
plmue=0.0 m/V	Coefficient for the length dependence of MUE.
pwmue=0.0 m/V	Coefficient for the width dependence of MUE.
plwmue=0.0 m/V	Coefficient for the length times width dependence of MUE.

© 2023 Cadence Design Systems, Inc.

`postmue=0`	Coefficient for the geometry-independent part of STMUE.
`pothemu=1.5`	Coefficient for the geometry-independent part of THEMU.
`postthemu=1.5`	Coefficient for the geometry-independent part of STTHEMU.
`pocs=0`	Coefficient for the geometry-independent part of CS.
`plcs=0.0`	Coefficient for the length dependence of CS.
`pwcs=0.0`	Coefficient for the width dependence of CS.
`plwcs=0.0`	Coefficient for the length times width dependence of CS.
`postcs=0`	Coefficient for the geometry-independent part of STCS.
`poxcor=0 V^-1`	Coefficient for the geometry-independent part of XCOR.
`plxcor=0.0 V^-1`	Coefficient for the length dependence of XCOR.
`pwxcor=0.0 V^-1`	Coefficient for the width dependence of XCOR.
`plwxcor=0.0 V^-1`	Coefficient for the length times width dependence of XCOR.
`postxcor=0`	Coefficient for the geometry-independent part of STXCOR.
`pofeta=1`	Coefficient for the geometry-independent part of FETA.
`pors=30 Ω`	Coefficient for the geometry-independent part of RS.
`plrs=0.0 Ω`	Coefficient for the length dependence of RS.
`pwrs=0.0 Ω`	Coefficient for the width dependence of RS.
`plwrs=0.0 Ω`	Coefficient for the length times width dependence of RS.
`postrs=1`	Coefficient for the geometry-independent part of STRS.
`porsb=0 V^-1`	Coefficient for the geometry-independent part of RSB.
`porsg=0 V^-1`	Coefficient for the geometry-independent part of RSG.
`pothesat=1 V^-1`	Coefficient for the geometry-independent part of THESAT.
`plthesat=0.0 V^-1`	Coefficient for the length dependence of THESAT.
`pwthesat=0.0 V^-1`	Coefficient for the width dependence of THESAT.
`plwthesat=0.0 V^-1`	Coefficient for the length times width dependence of THESAT.
`postthesat=1`	Coefficient for the geometry-independent part of STTHESAT.
`plstthesat=0.0`	Coefficient for the length dependence of STTHESAT.
`pwstthesat=0.0`	Coefficient for the width dependence of STTHESAT.

© 2023 Cadence Design Systems, Inc.

`plwstthesat=0.0`	Coefficient for the length times width dependence of STTHESAT.
`pothesatb=0 V^-1`	Coefficient for the geometry-independent part of THESATB.
`plthesatb=0.0 V^-1`	Coefficient for the length dependence of THESATB.
`pwthesatb=0.0 V^-1`	Coefficient for the width dependence of THESATB.
`plwthesatb=0.0 V^-1`	Coefficient for the length times width dependence of THESATB.
`pothesatg=0 V^-1`	Coefficient for the geometry-independent part of THESATG.
`plthesatg=0.0 V^-1`	Coefficient for the length dependence of THESATG.
`pwthesatg=0.0 V^-1`	Coefficient for the width dependence of THESATG.
`plwthesatg=0.0 V^-1`	Coefficient for the length times width dependence of THESATG.
`poax=3`	Coefficient for the geometry-independent part of AX.
`plax=0.0`	Coefficient for the length dependence of AX.
`pwax=0.0`	Coefficient for the width dependence of AX.
`plwax=0.0`	Coefficient for the length times width dependence of AX.
`poalp=0.01`	Coefficient for the geometry-independent part of ALP.
`plalp=0.0`	Coefficient for the length dependence of ALP.
`pwalp=0.0`	Coefficient for the width dependence of ALP.
`plwalp=0.0`	Coefficient for the length times width dependence of ALP.
`poalp1=0 V`	Coefficient for the geometry-independent part of ALP1.
`plalp1=0.0 V`	Coefficient for the length dependence of ALP1.
`pwalp1=0.0 V`	Coefficient for the width dependence of ALP1.
`plwalp1=0.0 V`	Coefficient for the length times width dependence of ALP1.

© 2023 Cadence Design Systems, Inc.

`poalp2=0 V^-1`	Coefficient for the geometry-independent part of ALP2.
`plalp2=0.0 V^-1`	Coefficient for the length dependence of ALP2.
`pwalp2=0.0 V^-1`	Coefficient for the width dependence of ALP2.
`plwalp2=0.0 V^-1`	Coefficient for the length times width dependence of ALP2.
`povp=0.05 V`	Coefficient for the geometry-independent part of VP.
`poa1=1`	Coefficient for the geometry-independent part of A1.
`pla1=0.0`	Coefficient for the length dependence of A1.
`pwa1=0.0`	Coefficient for the width dependence of A1.
`plwa1=0.0`	Coefficient for the length times width dependence of A1.
`poa2=10 V`	Coefficient for the geometry-independent part of A2.
`posta2=0 V`	Coefficient for the geometry-independent part of STA2.
`poa3=1`	Coefficient for the geometry-independent part of A3.
`pla3=0.0`	Coefficient for the length dependence of A3.
`pwa3=0.0`	Coefficient for the width dependence of A3.
`plwa3=0.0`	Coefficient for the length times width dependence of A3.
`poa4=0 V^-0.5`	Coefficient for the geometry-independent part of A4.
`pla4=0.0 V^-0.5`	Coefficient for the length dependence of A4.
`pwa4=0.0 V^-0.5`	Coefficient for the width dependence of A4.
`plwa4=0.0 V^-0.5`	Coefficient for the length times width dependence of A4.
`pogco=0`	Coefficient for the geometry-independent part of GCO.
`poiginv=0 A`	Coefficient for the geometry-independent part of IGINV.
`pliginv=0.0 A`	Coefficient for the length dependence of IGINV.
`pwiginv=0.0 A`	Coefficient for the width dependence of IGINV.
`plwiginv=0.0 A`	Coefficient for the length times width dependence of IGINV.
`poigov=0 A`	Coefficient for the geometry-independent part of IGOV.
`pligov=0.0 A`	Coefficient for the length dependence of IGOV.
`pwigov=0.0 A`	Coefficient for the width dependence of IGOV.
`plwigov=0.0 A`	Coefficient for the length times width dependence of IGOV.

© 2023 Cadence Design Systems, Inc.

`poigovd=0 A`	Coefficient for the geometry-independent part of IGOV for drain side.
`pligovd=0.0 A`	Coefficient for the length dependence of IGOV for drain side.
`pwigovd=0.0 A`	Coefficient for the width dependence of IGOV for drain side.
`plwigovd=0.0 A`	Coefficient for the length times width dependence of IGOV for drain side.
`postig=2`	Coefficient for the geometry-independent part of STIG.
`pogc2=0.375`	Coefficient for the geometry-independent part of GC2.
`pogc3=0.063`	Coefficient for the geometry-independent part of GC3.
`pochib=3.1 V`	Coefficient for the geometry-independent part of CHIB.
`poagidl=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL.
`plagidl=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL.
`pwagidl=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL.
`plwagidl=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL.
`poagidld=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL for drain side.
`plagidld=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL for drain side.
`pwagidld=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL for drain side.
`plwagidld=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL for drain side.
`pobgidl=41 V`	Coefficient for the geometry-independent part of BGIDL.
`pobgidld=41 V`	Coefficient for the geometry-independent part of BGIDL for drain side.
`postbgidl=0 V/K`	Coefficient for the geometry-independent part of STBGIDL.
`postbgidld=0 V/K`	Coefficient for the geometry-independent part of STBGIDL for drain side.
`pocgidl=0`	Coefficient for the geometry-independent part of CGIDL.

© 2023 Cadence Design Systems, Inc.

`pocgidld=0`	Coefficient for the geometry-independent part of CGIDL for drain side.
`pocox=1E-14 F`	Coefficient for the geometry-independent part of COX.
`plcox=0.0 F`	Coefficient for the length dependence of COX.
`pwcox=0.0 F`	Coefficient for the width dependence of COX.
`plwcox=0.0 F`	Coefficient for the length times width dependence of COX.
`pocgov=1E-15 F`	Coefficient for the geometry-independent part of CGOV.
`plcgov=0.0 F`	Coefficient for the length dependence of CGOV.
`pwcgov=0.0 F`	Coefficient for the width dependence of CGOV.
`plwcgov=0.0 F`	Coefficient for the length times width dependence of CGOV.
`pocgovd=1E-15 F`	Coefficient for the geometry-independent part of CGOV for drain side.
`plcgovd=0.0 F`	Coefficient for the length dependence of CGOV for drain side.
`pwcgovd=0.0 F`	Coefficient for the width dependence of CGOV for drain side.
`plwcgovd=0.0 F`	Coefficient for the length times width dependence of CGOV for drain side.
`pocgbov=0 F`	Coefficient for the geometry-independent part of CGBOV.
`plcgbov=0.0 F`	Coefficient for the length dependence of CGBOV.
`pwcgbov=0.0 F`	Coefficient for the width dependence of CGBOV.
`plwcgbov=0.0 F`	Coefficient for the length times width dependence of CGBOV.
`pocfr=0 F`	Coefficient for the geometry-independent part of CFR.
`plcfr=0.0 F`	Coefficient for the length dependence of CFR.
`pwcfr=0.0 F`	Coefficient for the width dependence of CFR.
`plwcfr=0.0 F`	Coefficient for the length times width dependence of CFR.
`pocfrd=0 F`	Coefficient for the geometry-independent part of CFR for drain side.
`plcfrd=0.0 F`	Coefficient for the length dependence of CFR for drain side.
`pwcfrd=0.0 F`	Coefficient for the width dependence of CFR for drain side.
`plwcfrd=0.0 F`	Coefficient for the length times width dependence of CFR for drain side.

© 2023 Cadence Design Systems, Inc.

`pofnt=1`	Coefficient for the geometry-independent part of FNT.
`pofntexc=0.0`	Coefficient for the geometry-independent part of FNTEXC.
`plfntexc=0.0`	Coefficient for the length dependence of FNTEXC.
`pwfntexc=0.0`	Coefficient for the width dependence of FNTEXC.
`plwfntexc=0.0`	Coefficient for the length times width dependence of FNTEXC.
`ponfa=8E+22` V^{-1}/m^4	Coefficient for the geometry-independent part of NFA.
`plnfa=0.0` V^{-1}/m^4	Coefficient for the length dependence of NFA.
`pwnfa=0.0` V^{-1}/m^4	Coefficient for the width dependence of NFA.
`plwnfa=0.0` V^{-1}/m^4	Coefficient for the length times width dependence of NFA.
`ponfb=3E+07` V^{-1}/m^2	Coefficient for the geometry-independent part of NFB.
`plnfb=0.0` V^{-1}/m^2	Coefficient for the length dependence of NFB.
`pwnfb=0.0` V^{-1}/m^2	Coefficient for the width dependence of NFB.
`plwnfb=0.0` V^{-1}/m^2	Coefficient for the length times width dependence of NFB.
`ponfc=0` V^{-1}	Coefficient for the geometry-independent part of NFC.
`plnfc=0.0` V^{-1}	Coefficient for the length dependence of NFC.
`pwnfc=0.0` V^{-1}	Coefficient for the width dependence of NFC.
`plwnfc=0.0` V^{-1}	Coefficient for the length times width dependence of NFC.
`poef=1.0`	Coefficient for the flicker noise frequency exponent.
`pokvthowe=0`	Coefficient for the geometry-independent part of KVTHOWE.
`plkvthowe=0`	Coefficient for the length dependence part of KVTHOWE.
`pwkvthowe=0`	Coefficient for the width dependence part of KVTHOWE.

© 2023 Cadence Design Systems, Inc.

`plwkvthowe=0`	Coefficient for the length times width dependence part of KVTHOWE.
`pokuowe=0`	Coefficient for the geometry-independent part of KUOWE.
`plkuowe=0`	Coefficient for the length dependence part of KUOWE.
`pwkuowe=0`	Coefficient for the width dependence part of KUOWE.
`plwkuowe=0`	Coefficient for the length times width dependence part of KUOWE.
`lmin=0 m`	Dummy parameter to label binning set.
`lmax=1.0 m`	Dummy parameter to label binning set.
`wmin=0 m`	Dummy parameter to label binning set.
`wmax=1.0 m`	Dummy parameter to label binning set.
`w=10e-6 m`	Default width.
`l=10e-6 m`	Default length.
`nf=1`	Number of fingers, It served as the default value of instance nf.
`mvt=0.0`	DCmatch parameter.
`mvto=0.0`	DCmatch parameter.
`mbe=0.0`	DCmatch parameter.
`mbeo=0.0`	DCmatch parameter.
`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
`noisemethod=oldcmi`	

© 2023 Cadence Design Systems, Inc.

	Induced gate noise implementation. Possible values are `oldcmi`, `subckt`, `newcmi`, and `noign`.

Output Parameters

`weff (m)`	Effective channel width for geometrical models.
`leff (m)`	Effective channel length for geometrical models.
`lp_vfb (V)`	Local parameter VFB after T-scaling and clipping.
`lp_stvfb (V/K)`	Local parameter STVFB after clipping.
`lp_tox (m)`	Local parameter TOX after clipping.
`lp_epsrox`	Local parameter EPSROX after clipping.
`lp_neff (m^-3)`	Local parameter NEFF after clipping.
`lp_vnsub (V)`	Local parameter VNSUB after clipping.
`lp_nslp (V)`	Local parameter NSLP after clipping.
`lp_dnsub (V^-1)`	Local parameter DNSUB after clipping.
`lp_dphib (V)`	Local parameter DPHIB after clipping.
`lp_np (m^-3)`	Local parameter NP after clipping.
`lp_ct`	Local parameter CT after clipping.
`lp_toxov (m)`	Local parameter TOXOV after clipping.
`lp_toxovd (m)`	Local parameter TOXOVD after clipping.
`lp_nov (m^-3)`	Local parameter NOV after clipping.
`lp_novd (m^-3)`	Local parameter NOVD after clipping.
`lp_cf`	Local parameter CF after clipping.
`lp_cfb (V^-1)`	Local parameter CFB after clipping.
`lp_betn (m^2/(V s))`	Local parameter BETN after T-scaling and clipping.
`lp_stbet`	Local parameter STBET after clipping.
`lp_mue (m/V)`	Local parameter MUE after T-scaling and clipping.

© 2023 Cadence Design Systems, Inc.

lp_stmue	Local parameter STMUE after clipping.
lp_themu	Local parameter THEMU after T-scaling and clipping.
lp_stthemu	Local parameter STTHEMU after clipping.
lp_cs	Local parameter CS after T-scaling and clipping.
lp_stcs	Local parameter STCS after clipping.
lp_xcor (V^-1)	Local parameter XCOR after T-scaling and clipping.
lp_stxcor	Local parameter STXCOR after clipping.
lp_feta	Local parameter FETA after clipping.
lp_rs (Ω)	Local parameter RS after T-scaling and clipping.
lp_strs	Local parameter STRS after clipping.
lp_rsb (V^-1)	Local parameter RSB after clipping.
lp_rsg (V^-1)	Local parameter RSG after clipping.
lp_thesat (V^-1)	Local parameter THESAT after T-scaling and clipping.
lp_stthesat	Local parameter STTHESAT after clipping.
lp_thesatb (V^-1)	Local parameter THESATB after clipping.
lp_thesatg (V^-1)	Local parameter THESATG after clipping.
lp_ax	Local parameter AX after clipping.
lp_alp	Local parameter ALP after clipping.
lp_alp1 (V)	Local parameter ALP1 after clipping.
lp_alp2 (V^-1)	Local parameter ALP2 after clipping.
lp_vp (V)	Local parameter VP after clipping.
lp_a1	Local parameter A1 after clipping.
lp_a2 (V)	Local parameter A2 after T-scaling and clipping.
lp_sta2	Local parameter STA2 after clipping.
lp_a3	Local parameter A3 after clipping.
lp_a4 (1/V)	

© 2023 Cadence Design Systems, Inc.

	Local parameter A4 after clipping.
lp_gco	Local parameter GCO after clipping.
lp_iginv (A)	Local parameter IGINV after T-scaling and clipping.
lp_igov (A)	Local parameter IGOV after T-scaling and clipping.
lp_igovd (A)	Local parameter IGOVD after T-scaling and clipping.
lp_stig	Local parameter STIG after clipping.
lp_gc2	Local parameter GC2 after clipping.
lp_gc3	Local parameter GC3 after clipping.
lp_chib (V)	Local parameter CHIB after clipping.
lp_agidl (A/V^3)	
	Local parameter AGIDL after clipping.
lp_agidld (A/V^3)	
	Local parameter AGIDLD after clipping.
lp_bgidl (V)	Local parameter BGIDL after T-scaling and clipping.
lp_bgidld (V)	Local parameter BGIDLD after T-scaling and clipping.
lp_stbgidl (V/K)	
	Local parameter STBGIDL after clipping.
lp_stbgidld (V/K)	
	Local parameter STBGIDLD after clipping.
lp_cgidl	Local parameter CGIDL after clipping.
lp_cgidld	Local parameter CGIDLD after clipping.
lp_cox (F)	Local parameter COX after clipping.
lp_cgov (F)	Local parameter CGOV after clipping.
lp_cgovd (F)	Local parameter CGOVD after clipping.
lp_cgbov (F)	Local parameter CGBOV after clipping.
lp_cfr (F)	Local parameter CFR after clipping.
lp_cfrd (F)	Local parameter CFRD after clipping.
lp_fnt	Local parameter FNT after clipping.
lp_fntexc	Local parameter FNTEXC after clipping.

© 2023 Cadence Design Systems, Inc.

lp_nfa (1/(V m^4))	
	Local parameter NFA after clipping.
lp_nfb (1/(V m^2))	
	Local parameter NFB after clipping.
lp_nfc (V^-1)	Local parameter NFC after clipping.
lp_ef	Local parameter EF after clipping.
lp_rg (Ω)	Local parameter RG after clipping.
lp_rbulk (Ω)	Local parameter RBULK after clipping.
lp_rwell (Ω)	Local parameter RWELL after clipping.
lp_rjuns (Ω)	Local parameter RJUNS after clipping.
lp_rjund (Ω)	Local parameter RJUND after clipping.
lp_munqs	Local parameter MUNQS after clipping.
cjosbot (F)	Bottom component of total zero-bias source junction capacitance at device temperature.
cjossti (F)	STI-edge component of total zero-bias source junction capacitance at device temperature.
cjosgat (F)	Gate-edge component of total zero-bias source junction capacitance at device temperature.
vbisbot (V)	Built-in voltage of source-side bottom junction at device temperature.
vbissti (V)	Built-in voltage of source-side STI-edge junction at device temperature.
vbisgat (V)	Built-in voltage of source-side gate-edge junction at device temperature.
idsatsbot (A)	Total source-side bottom junction saturation current.
idsatssti (A)	Total source-side STI-edge junction saturation current.
idsatsgat (A)	Total source-side gate-edge junction saturation current.
cjosbotd (F)	Bottom component of total zero-bias drain junction capacitance at device temperature.
cjosstid (F)	STI-edge component of total zero-bias drain junction capacitance at device temperature.

© 2023 Cadence Design Systems, Inc.

`cjosgatd (F)`	Gate-edge component of total zero-bias drain junction capacitance at device temperature.
`vbisbotd (V)`	Built-in voltage of drain-side bottom junction at device temperature.
`vbisstid (V)`	Built-in voltage of drain-side STI-edge junction at device temperature.
`vbisgatd (V)`	Built-in voltage of drain-side gate-edge junction at device temperature.
`idsatsbotd (A)`	Total drain-side bottom junction saturation current.
`idsatsstid (A)`	Total drain-side STI-edge junction saturation current.
`idsatsgatd (A)`	Total drain-side gate-edge junction saturation current.
`lv1 (m)`	Alias of l.
`lv2 (m)`	Alias of w.
`lv3 (m^2)`	Alias of ad.
`lv4 (m^2)`	Alias of as.
`lv11 (m)`	Alias of pd.
`lv12 (m)`	Alias of ps.
`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`dtsh (K)`	Device temperature rise due to self-heating.
`ctype`	Flag for channel type.
`sdint`	Flag for source-drain interchange.
`is (A)`	External DC current at source terminal.
`ise (A)`	Total source current.
`ig (A)`	External DC current at gate terminal.

© 2023 Cadence Design Systems, Inc.

ige (A)	Total gate current.
id (A)	External DC current at drain terminal.
ide (A)	Total drain current.
ib (A)	Total bulk current.
ibe (A)	Total bulk current.
ids (A)	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
idb (A)	Drain to bulk current.
isb (A)	Source to bulk current.
igs (A)	Gate-source tunneling current.
igd (A)	Gate-drain tunneling current.
igb (A)	Gate-bulk tunneling current.
igcs (A)	Gate-channel tunneling current (source component).
igcd (A)	Gate-channel tunneling current (drain component).
iavl (A)	Substrate current due to weak avalanche.
igisl (A)	Gate-induced source leakage current.
igidl (A)	Gate-induced drain leakage current.
ijs (A)	Total source junction current.
ijsbot (A)	Source junction current (bottom component).
ijsgat (A)	Source junction current (gate-edge component).
ijssti (A)	Source junction current (STI-edge component).
ijd (A)	Total drain junction current.
ijdbot (A)	Drain junction current (bottom component).
ijdgat (A)	Drain junction current (gate-edge component).
ijdsti (A)	Drain junction current (STI-edge component).
qg (Coul)	Intrinsic gate charge.
qd (Coul)	Intrinsic drain charge.
qb (Coul)	Intrinsic bulk charge.
qs (Coul)	Intrinsic source charge.

© 2023 Cadence Design Systems, Inc.

qgs_ov (Coul)	Overlap charge for gate-source.
qgd_ov (Coul)	Overlap charge for gate-drain.
qfgs (Coul)	Sum of outerFringe and overlap for gate-source.
qfgd (Coul)	Sum of outerFringe and overlap for gate-drain.
qgb_ov (Coul)	Gate-bulk overlap charge.
qjun_s (Coul)	Junction charge on source side.
qjun_d (Coul)	Junction charge on drain side.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vgd (V)	External gate-drain DC voltage.
vsb (V)	Source-bulk voltage.
vdb (V)	External drain-bulk DC voltage.
vth0 (V)	Zero-bias threshold voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back bias effects.
vth (V)	Threshold voltage including back bias and drain bias effects.
vth_drive (V)	Gate overdrive voltage including back-bias, drain bias effects.
vgt (V)	Effective gate drive voltage including back bias and drain bias effects.
vdss (V)	Drain saturation voltage at actual bias.
vdsat (V)	Drain saturation voltage.
vdsat_marg (V)	Saturation margin with respect to Vdsat for Drain voltage.
vsat (V)	Saturation limit.
pwr (W)	Power at op point.
gm (1/Ω)	Transconductance.
gmb (1/Ω)	Substrate transconductance.
go (1/Ω)	Output conductance.
gds (1/Ω)	Output conductance.
gjs (1/Ω)	Source junction conductance.

© 2023 Cadence Design Systems, Inc.

gjd (1/Ω)	Drain junction conductance.
cdd (F)	Drain capacitance.
cdg (F)	Drain-gate capacitance.
cds (F)	Drain-source capacitance.
cdb (F)	Drain-bulk capacitance.
cgd (F)	Gate-drain capacitance.
cgg (F)	Gate capacitance.
cgs (F)	Gate-source capacitance.
cgb (F)	Gate-bulk capacitance.
csd (F)	Source-drain capacitance.
csg (F)	Source-gate capacitance.
css (F)	Source capacitance.
csb (F)	Source-bulk capacitance.
cbd (F)	Bulk-drain capacitance.
cbg (F)	Bulk-gate capacitance.
cbs (F)	Bulk-source capacitance.
cbb (F)	Bulk capacitance.
co (F)	Output Drain-Source capacitance.
cm (F)	Capacitance element 1 for QS model.
cmb (F)	Capacitance element 2 for QS model.
cmx (F)	Capacitance element 3 for QS model.
tau1 (s)	Time constant related to NQS first frequency pole.
fqslim (Hz)	QS model frequency limit.
cgsol (F)	Total gate-source overlap capacitance.
cgdol (F)	Total gate-drain overlap capacitance.
cgbol (F)	Total gate-bulk overlap capacitance.
cjs (F)	Total source junction capacitance.
cjsbot (F)	Source junction capacitance (bottom component).
cjsgat (F)	Source junction capacitance (gate-edge component).

© 2023 Cadence Design Systems, Inc.

cjssti (F)	Source junction capacitance (STI-edge component).
cjd (F)	Total drain junction capacitance.
cjdbot (F)	Drain junction capacitance (bottom component).
cjdgat (F)	Drain junction capacitance (gate-edge component).
cjdsti (F)	Drain junction capacitance (STI-edge component).
lpoly (m)	Length of poly.
self_gain	Gm/Go ratio (MOSFET self-gain).
u	Transistor gain.
rout (Ω)	Small-signal output resistance.
vearly (V)	Equivalent Early voltage.
ft (Hz)	Unity gain frequency at actual bias.
beff (A/V^2)	Gain factor.
gmoveri (1/V)	Transconductance efficiency.
fug (Hz)	Unity gain frequency at actual bias.
rgate (Ω)	Gate resistance.
rg (Ω)	Gate resistance.
sfl (A^2/Hz)	Flicker noise current spectral density at 1 Hz.
sqrtsff (V/$\sqrt{}$Hz)	Input-referred RMS white noise voltage spectral density at 1 kHz.
sqrtsfw (V/$\sqrt{}$Hz)	Input-referred RMS white noise voltage spectral density.
sid (A^2/Hz)	White noise current spectral density.
sig (A^2/Hz)	Induced gate noise current spectral density at 1 Hz.
cigid	Imaginary part of correlation coefficient between Sig and Sid.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
sigs (A^2/Hz)	Gate-source current noise spectral density.
sigd (A^2/Hz)	Gate-drain current noise spectral density.
siavl (A^2/Hz)	Impact ionization current noise spectral density.

© 2023 Cadence Design Systems, Inc.

ssi (A^2/Hz)	Total source junction current noise spectral density.
sdi (A^2/Hz)	Total drain junction current noise spectral density.
tk (K)	Device Temperature.
vbs (V)	Bulk-source voltage.
lv9 (V)	Alias of vth.
lv10 (V)	Alias of vdss.
lv36 (F)	Alias of cgsol.
lv37 (F)	Alias of cgdol.
lv38 (F)	Alias of cgbol.
lv51 (m)	Alias of tox.
lx4 (A)	Alias of ids.
lx3 (V)	Alias of vds.
lx2 (V)	Alias of vgs.
lx7 (1/Ω)	Alias of gm.
lx8 (1/Ω)	Alias of gds.
lx9 (1/Ω)	Alias of gmb.
lx33 (F)	Alias of cdd.
lx32 (F)	Alias of cdg.
lx34 (F)	Alias of cds.
lx19 (F)	Alias of cgd.
lx18 (F)	Alias of cgg.
lx20 (F)	Alias of cgs.
lx22 (F)	Alias of cbd.
lx21 (F)	Alias of cbg.
lx23 (F)	Alias of cbs.
lx5 (A)	Alias of ijs.
lx6 (A)	Alias of ijd.
lx28 (F)	Alias of cjs.
lx29 (F)	Alias of cjd.

© 2023 Cadence Design Systems, Inc.

`lx38 (A)`	Alias of igs.
`lx39 (A)`	Alias of igd.
`lx66 (A)`	Alias of igb.
`lx67 (A)`	Alias of igcs.
`lx68 (A)`	Alias of igcd.
`lx110 (A)`	Alias of igisl.
`lx47 (A)`	Alias of igidl.
`lx60 (F)`	Alias of csd.
`lx59 (F)`	Alias of csg.
`lx58 (F)`	Alias of css.
`lx12 (Coul)`	Alias of Qb including overlap charge.
`lx14 (Coul)`	Alias of Qg including overlap charge.
`lx16 (Coul)`	Alias of Qd including overlap charge.
`lx83 (F)`	Alias of cgd including overlap cap.
`lx84 (F)`	Alias of cgs including overlap cap.
`OPdef`	1: Device Physics notation. 2: Circuit Simulator notation.
`SDop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.

Related Topics

PSP102 Model

Component Statements for PSP102 Models

PSP MOSFET Model (psp1020)

PSP MOSFET Model (psp1021)

PSP local MOSFET Model (psp102e)

PSP NQS MOSFET Model (pspnqs1020)

PSP NQS MOSFET Model (pspnqs1021)

© 2023 Cadence Design Systems, Inc.

PSP NQS local MOSFET Model (pspnqs102e)

PSP MOSFET Model (psp1020)

This is SiMKit 4.0.1.

This device is supported within altergroups.

This device is dynamically loaded from the shared object `/<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so`.

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`l=10e-6 m`	Design length.
`w=10e-6 m`	Design width.
`sa=0.0 m`	Distance between OD-edge and poly from one side.
`sb=0.0 m`	Distance between OD-edge and poly from other side.
`sd=0.0 m`	Distance between neighboring fingers.
`sca=0.0`	Integral of the first distribution function for scattered well dopants.
`scb=0.0`	Integral of the second distribution function for scattered well dopants.
`scc=0.0`	Integral of the third distribution function for scattered well dopants.
`sc=0.0 m`	Distance between OD-edge and nearest well edge.
`delvto=0.0 V`	Threshold voltage shift parameter.
`factuo=1.0`	Zero-field mobility pre-factor.
`absource=1E-12 m`^{2}	Bottom area of source junction.
`lssource=1E-6 m`	STI-edge length of source junction.

© 2023 Cadence Design Systems, Inc.

`lgsource=1E-6 m`	Gate-edge length of source junction.
`abdrain=1E-12 m`^{2}	Bottom area of drain junction.
`lsdrain=1E-6 m`	STI-edge length of drain junction.
`lgdrain=1E-6 m`	Gate-edge length of drain junction.
`as=1E-12 m`^{2}	Bottom area of source junction.
`ps=1E-6 m`	Perimeter of source junction.
`ad=1E-12 m`^{2}	Bottom area of drain junction.
`pd=1E-6 m`	Perimeter of drain junction.
`mulid0=1`	Ids multiplier.
`mult=1.0`	Number of devices in parallel.
`nf=1.0`	Number of fingers.
`ngcon=1.0`	Number of gate contacts.
`xgw=1.0E-7 m`	Distance from the gate contact to the channel edge.
`region=triode`	Estimated operating region. Spectre outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trise=0.0 K`	Temperature rise from ambient.
`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Definition

```
model modelName psp1020 parameter=value ...
```

Model Parameters

`level=102`	Model level.
`type=n`	Channel type parameter. Specify n for NMOS and p for PMOS. Possible values are `n` and `p`.
`tr=value of tnom C`	Nominal (reference) temperature.

© 2023 Cadence Design Systems, Inc.

`swnqs=0`	Flag for NQS. 0 means off. Numbers 1, 2, 3, 5, or 9 refer to collocation points.
`swigate=0`	Flag for gate current. 0 means turn off IG.
`swimpact=0`	Flag for impact ionization current. 0 means turn off impact ionization.
`swgidl=0`	Flag for GIDL current. means turn off IGIDL.
`swjuncap=0`	Flag for juncap. 0 means turn off juncap.
`swjunasym=0`	Flag for asymmetric junctions. 0 means symmetric, and 1 means asymmetric.
`qmc=1.0`	Quantum-mechanical correction factor.
`version=102.32`	Model parameter "version" accepts only a real number value, like 102.21 for version=102.2.1. The available versions are 102.2, 102.21(102.2.1), 102.3, 102.32(102.3.2), 102.33(102.3.3), 102.34(102.3.4), 102.4(102.4.0), and 102.5(102.5.0).
`geomod=1`	1 for geometrical model and 0 for electrical model.
`binmod=0`	1 for bin model and 0 for non-bin model.
`scalelev=102`	102 for local, 1020 for global model and 1021 for bin model.
`compatible=spectre`	Compatibility parameter. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`lvaro=0.0 m`	Geometry-independent difference between actual and programmed gate length.
`lvarl=0.0`	Length dependence of LVAR.
`lvarw=0.0`	Width dependence of LVAR.
`lap=0.0 m`	Effective channel length reduction per side.
`wvaro=0.0 m`	Geometry-independent difference between actual and programmed field-oxide opening.
`wvarl=0.0`	Length dependence of WVAR.
`wvarw=0.0`	Width dependence of WVAR.
`wot=0.0 m`	Effective channel width reduction per side.
`dlq=0.0 m`	Effective channel length reduction for CV.

© 2023 Cadence Design Systems, Inc.

`dwq=0.0 m`	Effective channel width reduction for CV.
`vfbo=(-1.0) V`	Geometry-independent flat-band voltage at TR.
`vfbl=0.0`	Length dependence of flat-band voltage.
`vfbw=0.0`	Width dependence of flat-band voltage.
`vfblw=0.0`	Area dependence of flat-band voltage.
`stvfbo=5e-4 V/K`	Geometry-independent temperature dependence of VFB.
`stvfbl=0.0`	Length dependence of temperature dependence of VFB.
`stvfbw=0.0`	Width dependence of temperature dependence of VFB.
`stvfblw=0.0`	Area dependence of temperature dependence of VFB.
`toxo=2e-9 m`	Gate oxide thickness.
`epsroxo=3.9`	Relative permittivity of gate dielectric.
`nsubo=3e23` m^{-3}	Geometry-independent substrate doping.
`nsubw=0.0`	Width dependence of background doping NSUBO due to segregation.
`wseg=1e-8 m`	Character length of segregation of background doping NSUBO.
`npck=1e24` m^{-3}	Pocket doping level.
`npckw=0.0`	Width dependence of pocket doping NPCK due to segregation.
`wsegp=1e-8 m`	Character length of segregation of pocket doping NPCK.
`lpck=1e-8 m`	Character length of lateral doping profile.
`lpckw=0.0`	Width dependence of character length of lateral doping profile.
`fol1=0.0`	First length dependence coefficient for short channel body effect.
`fol2=0.0`	Second length dependence coefficient for short channel body effect.
`vnsubo=0.0 V`	Effective doping bias-dependence parameter.
`nslpo=0.05 V`	Effective doping bias-dependence parameter.
`dnsubo=0.0 V^-1`	Effective doping bias-dependence parameter.
`dphibo=0.0 V`	Geometry-independent offset of PHIB.

© 2023 Cadence Design Systems, Inc.

`dphibl=0.0 V`	Length dependence offset of PHIB.
`dphiblexp=1.0`	Exponent for length dependence of offset of PHIB.
`dphibw=0.0`	Width dependence of offset of PHIB.
`dphiblw=0.0`	Area dependence of offset of PHIB.
`npo=1e26 m^-3`	Geometry-independent gate poly-silicon doping.
`npl=0.0`	Length dependence of gate poly-silicon doping.
`cto=0.0`	Geometry-independent interface states factor.
`ctl=0.0`	Length dependence of interface states factor.
`ctlexp=1.0`	Exponent for length dependence of interface states factor.
`ctw=0.0`	Width dependence of interface states factor.
`ctlw=0.0`	Area dependence of interface states factor.
`toxovo=2e-9 m`	Overlap oxide thickness.
`toxovdo=2e-9 m`	Overlap oxide thickness for drain side.
`lov=0 m`	Overlap length for gate/drain and gate/source overlap capacitance.
`lovd=0 m`	Overlap length for gate/drain overlap capacitance.
`novo=5e25 m^-3`	Effective doping of overlap region.
`novdo=5e25 m^-3`	Effective doping of overlap region for drain side.
`cfl=0.0`	Length dependence of DIBL-parameter.
`cflexp=2.0`	Exponent for length dependence of CF.
`cfw=0.0`	Width dependence of CF.
`cfbo=0.0 V^-1`	Back-bias dependence of CF.
`uo=5e-2 m^2/V/s`	Zero-field mobility at TR.
`fbet1=0.0`	Relative mobility decrease due to first lateral profile.
`fbet1w=0.0`	Width dependence of relative mobility decrease due to first lateral profile.
`lp1=1e-8 m`	Mobility-related characteristic length of first lateral profile.
`lp1w=0.0`	Width dependence of mobility-related characteristic length of first lateral profile.
`fbet2=0.0`	Relative mobility decrease due to second lateral profile.

© 2023 Cadence Design Systems, Inc.

`lp2=1e-8 m`	Mobility-related characteristic length of second lateral profile.
`betw1=0.0`	First higher-order width scaling coefficient of BETN.
`betw2=0.0`	Second higher-order width scaling coefficient of BETN.
`wbet=1e-9 m`	Characteristic width for width scaling of BETN.
`stbeto=1.0`	Geometry-independent temperature dependence of BETN.
`stbetl=0.0`	Length dependence of temperature dependence of BETN.
`stbetw=0.0`	Width dependence of temperature dependence of BETN.
`stbetlw=0.0`	Area dependence of temperature dependence of BETN.
`mueo=0.5 m/V`	Geometry-independent mobility reduction coefficient at TR.
`muew=0.0`	Width dependence of mobility reduction coefficient at TR.
`stmueo=0.0`	Temperature dependence of MUE.
`themuo=1.5`	Mobility reduction exponent at TR.
`stthemuo=1.5`	Temperature dependence of THEMU.
`cso=0.0`	Geometry-independent coulomb scattering parameter at TR.
`csl=0.0`	Length dependence of CS.
`cslexp=0.0`	Exponent for length dependence of CS.
`csw=0.0`	Width dependence of CS.
`cslw=0.0`	Area dependence of CS.
`stcso=0.0`	Temperature dependence of CS.
`xcoro=0.0 V^-1`	Geometry-independent non-universality parameter.
`xcorl=0.0`	Length dependence of non-universality parameter.
`xcorw=0.0`	Width dependence of non-universality parameter.
`xcorlw=0.0`	Area dependence of non-universality parameter.
`stxcoro=0.0`	Temperature dependence of XCOR.
`fetao=1.0`	Effective field parameter.
`rsw1=2.5e3 Ω`	Source/drain series resistance for 1 um wide channel at TR.
`rsw2=0.0`	Higher-order width scaling of RS.
`strso=1.0`	Temperature dependence of RS.
`rsbo=0.0 V^-1`	Back-bias dependence of series resistance.

© 2023 Cadence Design Systems, Inc.

`rsgo=0.0 V^-1`	Gate-bias dependence of series resistance.
`thesato=0.0 V^-1`	Geometry-independent velocity saturation parameter at TR.
`thesatl=0.05 V^-1`	Length dependence of THESAT.
`thesatlexp=1.0`	Exponent for length dependence of THESAT.
`thesatw=0.0`	Width dependence of velocity saturation parameter.
`thesatlw=0.0`	Area dependence of velocity saturation parameter.
`stthesato=1.0`	Geometry-independent temperature dependence of THESAT.
`stthesatl=0.0`	Length dependence of temperature dependence of THESAT.
`stthesatw=0.0`	Width dependence of temperature dependence of THESAT.
`stthesatlw=0.0`	Area dependence of temperature dependence of THESAT.
`thesatbo=0.0 V^-1`	Back-bias dependence of velocity saturation.
`thesatgo=0.0 V^-1`	Gate-bias dependence of velocity saturation.
`axo=18`	Geometry-independent linear/saturation transition factor.
`axl=0.4`	Length dependence of AX.
`alpl=5e-4`	Length dependence of ALP.
`alplexp=1.0`	Exponent for length dependence of ALP.
`alpw=0.0`	Width dependence of ALP.
`alp1l1=0.0 V`	Length dependence of CLM enhancement factor above threshold.
`alp1lexp=0.5`	Exponent for length dependence of ALP1.
`alp1l2=0.0`	Second_order length dependence of ALP1.
`alp1w=0.0`	Width dependence of ALP1.
`alp2l1=0.0 V^-1`	Length dependence of CLM enhancement factor below threshold.
`alp2lexp=0.5`	Exponent for length dependence of ALP2.
`alp2l2=0.0`	Second_order length dependence of ALP2.
`alp2w=0.0`	Width dependence of ALP2.
`vpo=0.05 V`	CLM logarithmic dependence parameter.
`a1o=1.0`	Geometry-independent impact-ionization pre-factor.

© 2023 Cadence Design Systems, Inc.

a1l=0.0	Length dependence of A1.
a1w=0.0	Width dependence of A1.
a2o=10 V	Impact-ionization exponent at TR.
sta2o=0.0 V	Temperature dependence of A2.
a3o=1.0	Geometry-independent saturation-voltage dependence of II.
a3l=0.0	Length dependence of A3.
a3w=0.0	Width dependence of A3.
a4o=0.0 V^-0.5	Geometry-independent back-bias dependence of II.
a4l=0.0	Length dependence of A4.
a4w=0.0	Width dependence of A4.
gcoo=0.0	Gate tunneling energy adjustment.
iginvlw=0.0 A	Gate channel current pre-factor for 1 um^2 channel area.
igovw=0.0 A	Gate overlap current pre-factor for 1 um wide channel.
igovdw=0.0 A	Gate overlap current pre-factor for 1 um wide channel for drain side.
stigo=2.0	Temperature dependence of IGINV and IGOV.
gc2o=0.375	Gate current slope factor.
gc3o=0.063	Gate current curvature factor.
chibo=3.1 V	Tunneling barrier height.
agidlw=0.0 A/V^3	Width dependence of GIDL pre-factor.
agidldw=0.0 A/V^3	Width dependence of GIDL pre-factor for drain side.
bgidlo=41 V	GIDL probability factor at TR.
bgidldo=41 V	GIDL probability factor at TR for drain side.
stbgidlo=0.0 V/K	Temperature dependence of BGIDL.
stbgidldo=0.0 V/K	Temperature dependence of BGIDL for drain side.
cgidlo=0.0	Back-bias dependence of GIDL.
cgidldo=0.0	Back-bias dependence of GIDL for drain side.
cgbovl=0.0 F	Oxide capacitance for gate-bulk overlap for 1 um long channel.

© 2023 Cadence Design Systems, Inc.

`cfrw=0.0 F`	Outer fringe capacitance for 1 um wide channel.
`cfrdw=0.0 F`	Outer fringe capacitance for 1 um wide channel for drain side.
`fnto=1.0`	Thermal noise coefficient.
`fntexcl=0.0`	Length dependence coefficient of excess noise.
`nfalw=8e22 V^-1/m`^{4}	First coefficient of flicker noise for 1 um^2 channel area.
`nfblw=3e7 V^-1/m`^{2}	Second coefficient of flicker noise for 1 um^2 channel area.
`nfclw=0.0 V^-1`	Third coefficient of flicker noise for 1 um^2 channel area.
`efo=1.0`	Flicker noise frequency exponent.
`lintnoi=0.0 m`	Length offset for flicker noise.
`alpnoi=2.0`	Exponent for length offset for flicker noise.
`dta=0 K`	Temperature offset w.r.t. ambient circuit temperature.
`kvthoweo=0`	Geometrical independent threshold shift parameter.
`kvthowel=0`	Length dependent threshold shift parameter.
`kvthowew=0`	Width dependent threshold shift parameter.
`kvthowelw=0`	Area dependent threshold shift parameter.
`kuoweo=0`	Geometrical independent mobility degradation factor.
`kuowel=0`	Length dependent mobility degradation factor.
`kuowew=0`	Width dependent mobility degradation factor.
`kuowelw=0`	Area dependent mobility degradation factor.
`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.

© 2023 Cadence Design Systems, Inc.

`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.
`vgbr_max=vgb_max V`	Maximum allowed reverse voltage cross gate and bulk.
`vbsr_max=vbs_max V`	Maximum allowed reverse voltage cross source and bulk.
`vbdr_max=vbd_max V`	Maximum allowed reverse voltage cross source/drain and bulk.
`munqso=1.0`	Relative mobility for NQS modelling.
`rgo=0.0 Ω`	Gate resistance.
`rbulko=0.0 Ω`	Bulk resistance between node BP and BI.
`rwello=0.0 Ω`	Well resistance between node BI and B.
`rjunso=0.0 Ω`	Source-side bulk resistance between node BI and BS.
`rjundo=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
`rint=0.0 Ω/Sqr`	Contact resistance between silicide and ploy.
`rvpoly=0.0 Ω/Sqr`	Vertical poly resistance.
`rshg=0.0 Ω/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0.0 m`	Silicide extension over the physical gate length.
`saref=1.0e-6 m`	Reference distance between OD-edge and poly from one side.
`sbref=1.0e-6 m`	Reference distance between OD-edge and poly from other side.
`wlod=0 m`	Width parameter.

© 2023 Cadence Design Systems, Inc.

`kuo=0 m`	Mobility degradation/enhancement coefficient.
`kvsat=0 m`	Saturation velocity degradation/enhancement coefficient.
`tkuo=0`	Temperature dependence of KUO.
`lkuo=0 m^LLODKUO`	Length dependence of KUO.
`wkuo=0 m^WLODKUO`	Width dependence of KUO.
`pkuo=0 m^(LLODKUO+WLODKUO)`	Cross-term dependence of KUO.
`llodkuo=0`	Length parameter for UO stress effect.
`wlodkuo=0`	Width parameter for UO stress effect.
`kvtho=0 Vm`	Threshold shift parameter.
`lkvtho=0 m^LLODVTH`	Length dependence of KVTHO.
`wkvtho=0 m^WLODVTH`	Width dependence of KVTHO.
`pkvtho=0 m^(LLODVTH+WLODVTH)`	Cross-term dependence of KVTHO.
`llodvth=0`	Length parameter for VTH-stress effect.
`wlodvth=0`	Width parameter for VTH-stress effect.
`stetao=0 m`	eta0 shift factor related to VTHO change.
`lodetao=1.0`	eta0 shift modification factor for stress effect.
`scref=10e-6 m`	Distance between OD-edge and well edge of a reference device.
`web=0`	Coefficient for SCB.
`wec=0`	Coefficient for SCC.
`imax=1000 A`	Maximum current up to which forward current behaves exponentially.
`trj=21 C`	reference temperature.
`cjorbot=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.
`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.
`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.
`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
`idsatrbot=1E-12` Am^{-2}	Saturation current density at the reference temperature of bottom component for source-bulk junction.
`idsatrsti=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
`idsatrgat=1E-18 Am^-1`	

© 2023 Cadence Design Systems, Inc.

	Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
csrhbot=1E2 Am^{-3}	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
csrhsti=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
csrhgat=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.
xjunsti=100E-9 m	Junction depth of STI-edge component for source-bulk junction.
xjungat=100E-9 m	Junction depth of gate-edge component for source-bulk junction.
ctatbot=1E2 Am^{-3}	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
ctatsti=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
ctatgat=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
mefftatbot=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
mefftatsti=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
mefftatgat=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
cbbtbot=1E-12 AV^{-3}	
	Band-to-band tunneling prefactor of bottom component for source-bulk junction.
cbbtsti=1E-18 $AV^{-3}m$	

© 2023 Cadence Design Systems, Inc.

	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
`cbbtgat=1E-18 AV-3m`	
	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
`fbbtrbot=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.
`fbbtrsti=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
`fbbtrgat=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
`stfbbtbot=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
`stfbbtsti=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
`stfbbtgat=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
`vbrbot=10 V`	Breakdown voltage of bottom component for source-bulk junction.
`vbrsti=10 V`	Breakdown voltage of STI-edge component for source-bulk junction.
`vbrgat=10 V`	Breakdown voltage of gate-edge component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component for source-bulk junction.
`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
`cjorbotd=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.
`cjorstid=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.
`cjorgatd=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.
`vbirbotd=1 V`	Built-in voltage at the reference temperature of bottom component for drain-bulk junction.
`vbirstid=1 V`	Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.
`vbirgatd=1 V`	Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.
`pbotd=0.5`	Grading coefficient of bottom component for drain-bulk junction.
`pstid=0.5`	Grading coefficient of STI-edge component for drain-bulk junction.
`pgatd=0.5`	Grading coefficient of gate-edge component for drain-bulk junction.
`phigbotd=1.16 V`	Zero-temperature bandgap voltage of bottom component for drain-bulk junction.
`phigstid=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.
`phiggatd=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.
`idsatrbotd=1E-12 Am`$^{-2}$	

© 2023 Cadence Design Systems, Inc.

	Saturation current density at the reference temperature of bottom component for drain-bulk junction.
`idsatrstid=1E-18 Am^-1`	
	Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.
`idsatrgatd=1E-18 Am^-1`	
	Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.
`csrhbotd=1E2 Am`$^{-3}$	
	Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.
`csrhstid=1E-4 Am`$^{-2}$	
	Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
`csrhgatd=1E-4 Am`$^{-2}$	
	Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
`xjunstid=100E-9 m`	Junction depth of STI-edge component for drain-bulk junction.
`xjungatd=100E-9 m`	Junction depth of gate-edge component for drain-bulk junction.
`ctatbotd=1E2 Am`$^{-3}$	
	Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
`ctatstid=1E-4 Am`$^{-2}$	
	Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
`ctatgatd=1E-4 Am`$^{-2}$	
	Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.
`mefftatbotd=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
`mefftatstid=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`mefftatgatd=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
`cbbtbotd=1E-12 AV`$^{-3}$	Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
`cbbtstid=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.
`cbbtgatd=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.
`fbbtrbotd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.
`fbbtrstid=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.
`fbbtrgatd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.
`stfbbtbotd=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.
`stfbbtstid=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.
`stfbbtgatd=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.
`vbrbotd=10 V`	Breakdown voltage of bottom component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`vbrstid=10 V`	Breakdown voltage of STI-edge component for drain-bulk junction.
`vbrgatd=10 V`	Breakdown voltage of gate-edge component for drain-bulk junction.
`pbrbotd=4 V`	Breakdown onset tuning parameter of bottom component for drain-bulk junction.
`pbrstid=4 V`	Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.
`pbrgatd=4 V`	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
`swjunexp=0.0`	Flag for JUNCAP express. Specify 0 for full model and 1 for express model.
`vjunref=2.5`	The maximum source-bulk junction voltage; usually about 2*VSUP.
`fjunq=0.03`	Fraction below which source-bulk junction capacitance components are considered negligible.
`vjunrefd=2.5`	The maximum drain-bulk junction voltage; usually about 2*VSUP.
`fjunqd=0.03`	Fraction below which drain-bulk junction capacitance components are considered negligible.
`mvto=0.0`	DCmatch parameter.
`mbeo=0.0`	DCmatch parameter.
`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.

© 2023 Cadence Design Systems, Inc.

noisemethod=oldcmi	Induced gate noise implementation. Possible values are oldcmi, subckt, newcmi, and noign.

Output Parameters

weff (m)	Effective channel width for geometrical models.
leff (m)	Effective channel length for geometrical models.
lv1 (m)	Alias of l.
lv2 (m)	Alias of w.
lv3 (m^2)	Alias of ad.
lv4 (m^2)	Alias of as.
lv11 (m)	Alias of pd.
lv12 (m)	Alias of ps.

Operating-Point Parameters

region=triode	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are off, triode, sat, subth, and breakdown.
dtsh (K)	Device temperature rise due to self-heating.
ctype	Flag for channel type.
sdint	Flag for source-drain interchange.
is (A)	External DC current at source terminal.
ise (A)	Total source current.
ig (A)	External DC current at gate terminal.
ige (A)	Total gate current.
id (A)	External DC current at drain terminal.
ide (A)	Total drain current.
ib (A)	Total bulk current.
ibe (A)	Total bulk current.

© 2023 Cadence Design Systems, Inc.

`ids (A)`	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
`idb (A)`	Drain to bulk current.
`isb (A)`	Source to bulk current.
`igs (A)`	Gate-source tunneling current.
`igd (A)`	Gate-drain tunneling current.
`igb (A)`	Gate-bulk tunneling current.
`igcs (A)`	Gate-channel tunneling current (source component).
`igcd (A)`	Gate-channel tunneling current (drain component).
`iavl (A)`	Substrate current due to weak avalanche.
`igisl (A)`	Gate-induced source leakage current.
`igidl (A)`	Gate-induced drain leakage current.
`ijs (A)`	Total source junction current.
`ijsbot (A)`	Source junction current (bottom component).
`ijsgat (A)`	Source junction current (gate-edge component).
`ijssti (A)`	Source junction current (STI-edge component).
`ijd (A)`	Total drain junction current.
`ijdbot (A)`	Drain junction current (bottom component).
`ijdgat (A)`	Drain junction current (gate-edge component).
`ijdsti (A)`	Drain junction current (STI-edge component).
`qg (Coul)`	Intrinsic gate charge.
`qd (Coul)`	Intrinsic drain charge.
`qb (Coul)`	Intrinsic bulk charge.
`qs (Coul)`	Intrinsic source charge.
`qgs_ov (Coul)`	Overlap charge for gate-source.
`qgd_ov (Coul)`	Overlap charge for gate-drain.
`qfgs (Coul)`	Sum of outerFringe and overlap for gate-source.
`qfgd (Coul)`	Sum of outerFringe and overlap for gate-drain.
`qgb_ov (Coul)`	Gate-bulk overlap charge.

© 2023 Cadence Design Systems, Inc.

qjun_s (Coul)	Junction charge on source side.
qjun_d (Coul)	Junction charge on drain side.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vgd (V)	External gate-drain DC voltage.
vsb (V)	Source-bulk voltage.
vdb (V)	External drain-bulk DC voltage.
vth0 (V)	Zero-bias threshold voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back bias effects.
vth (V)	Threshold voltage including back bias and drain bias effects.
vth_drive (V)	Gate overdrive voltage including back-bias, drain bias effects.
vgt (V)	Effective gate drive voltage including back bias and drain bias effects.
vdss (V)	Drain saturation voltage at actual bias.
vdsat (V)	Drain saturation voltage.
vdsat_marg (V)	Saturation margin with respect to Vdsat for Drain voltage.
vsat (V)	Saturation limit.
pwr (W)	Power at op point.
gm (1/Ω)	Transconductance.
gmb (1/Ω)	Substrate transconductance.
go (1/Ω)	Output conductance.
gds (1/Ω)	Output conductance.
gjs (1/Ω)	Source junction conductance.
gjd (1/Ω)	Drain junction conductance.
cdd (F)	Drain capacitance.
cdg (F)	Drain-gate capacitance.
cds (F)	Drain-source capacitance.
cdb (F)	Drain-bulk capacitance.

© 2023 Cadence Design Systems, Inc.

cgd (F)	Gate-drain capacitance.
cgg (F)	Gate capacitance.
cgs (F)	Gate-source capacitance.
cgb (F)	Gate-bulk capacitance.
csd (F)	Source-drain capacitance.
csg (F)	Source-gate capacitance.
css (F)	Source capacitance.
csb (F)	Source-bulk capacitance.
cbd (F)	Bulk-drain capacitance.
cbg (F)	Bulk-gate capacitance.
cbs (F)	Bulk-source capacitance.
cbb (F)	Bulk capacitance.
co (F)	Output Drain-Source capacitance.
cm (F)	Capacitance element 1 for QS model.
cmb (F)	Capacitance element 2 for QS model.
cmx (F)	Capacitance element 3 for QS model.
tau1 (s)	Time constant related to NQS first frequency pole.
fqslim (Hz)	QS model frequency limit.
cgsol (F)	Total gate-source overlap capacitance.
cgdol (F)	Total gate-drain overlap capacitance.
cgbol (F)	Total gate-bulk overlap capacitance.
cjs (F)	Total source junction capacitance.
cjsbot (F)	Source junction capacitance (bottom component).
cjsgat (F)	Source junction capacitance (gate-edge component).
cjssti (F)	Source junction capacitance (STI-edge component).
cjd (F)	Total drain junction capacitance.
cjdbot (F)	Drain junction capacitance (bottom component).
cjdgat (F)	Drain junction capacitance (gate-edge component).
cjdsti (F)	Drain junction capacitance (STI-edge component).

© 2023 Cadence Design Systems, Inc.

lpoly (m)	Length of poly.
self_gain	Gm/Go ratio (MOSFET self-gain).
u	Transistor gain.
rout (Ω)	Small-signal output resistance.
vearly (V)	Equivalent Early voltage.
ft (Hz)	Unity gain frequency at actual bias.
beff (A/V^2)	Gain factor.
gmoveri (1/V)	Transconductance efficiency.
fug (Hz)	Unity gain frequency at actual bias.
rgate (Ω)	Gate resistance.
rg (Ω)	Gate resistance.
sfl (A^2/Hz)	Flicker noise current spectral density at 1 Hz.
sqrtsff (V/$\sqrt{}$Hz)	Input-referred RMS white noise voltage spectral density at 1 kHz.
sqrtsfw (V/$\sqrt{}$Hz)	Input-referred RMS white noise voltage spectral density.
sid (A^2/Hz)	White noise current spectral density.
sig (A^2/Hz)	Induced gate noise current spectral density at 1 Hz.
cigid	Imaginary part of correlation coefficient between Sig and Sid.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
sigs (A^2/Hz)	Gate-source current noise spectral density.
sigd (A^2/Hz)	Gate-drain current noise spectral density.
siavl (A^2/Hz)	Impact ionization current noise spectral density.
ssi (A^2/Hz)	Total source junction current noise spectral density.
sdi (A^2/Hz)	Total drain junction current noise spectral density.
vbs (V)	Bulk-source voltage.
lv9 (V)	Alias of vth.
lv10 (V)	Alias of vdss.

© 2023 Cadence Design Systems, Inc.

lv36 (F)	Alias of cgsol.
lv37 (F)	Alias of cgdol.
lv38 (F)	Alias of cgbol.
lv51 (m)	Alias of tox.
lx4 (A)	Alias of ids.
lx3 (V)	Alias of vds.
lx2 (V)	Alias of vgs.
lx7 (1/Ω)	Alias of gm.
lx8 (1/Ω)	Alias of gds.
lx9 (1/Ω)	Alias of gmb.
lx33 (F)	Alias of cdd.
lx32 (F)	Alias of cdg.
lx34 (F)	Alias of cds.
lx19 (F)	Alias of cgd.
lx18 (F)	Alias of cgg.
lx20 (F)	Alias of cgs.
lx22 (F)	Alias of cbd.
lx21 (F)	Alias of cbg.
lx23 (F)	Alias of cbs.
lx5 (A)	Alias of ijs.
lx6 (A)	Alias of ijd.
lx28 (F)	Alias of cjs.
lx29 (F)	Alias of cjd.
lx38 (A)	Alias of igs.
lx39 (A)	Alias of igd.
lx66 (A)	Alias of igb.
lx67 (A)	Alias of igcs.
lx68 (A)	Alias of igcd.
lx110 (A)	Alias of igisl.

© 2023 Cadence Design Systems, Inc.

`lx47 (A)`	Alias of igidl.
`lx60 (F)`	Alias of csd.
`lx59 (F)`	Alias of csg.
`lx58 (F)`	Alias of css.
`lx12 (Coul)`	Alias of Qb including overlap charge.
`lx14 (Coul)`	Alias of Qg including overlap charge.
`lx16 (Coul)`	Alias of Qd including overlap charge.
`lx83 (F)`	Alias of cgd including overlap cap.
`lx84 (F)`	Alias of cgs including overlap cap.
`OPdef`	1: Device Physics notation. 2: Circuit Simulator notation.
`SDop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.

Related Topics

PSP102 Model

Component Statements for PSP102 Models

PSP MOSFET Model (PSP102)

PSP MOSFET Model (psp1021)

PSP local MOSFET Model (psp102e)

PSP NQS MOSFET Model (pspnqs1020)

PSP NQS MOSFET Model (pspnqs1021)

PSP NQS local MOSFET Model (pspnqs102e)

PSP MOSFET Model (psp1021)

This is SiMKit 4.0.1.

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`l=10e-6 m`	Design length.
`w=10e-6 m`	Design width.
`sa=0.0 m`	Distance between OD-edge and poly from one side.
`sb=0.0 m`	Distance between OD-edge and poly from other side.
`sd=0.0 m`	Distance between neighboring fingers.
`sca=0.0`	Integral of the first distribution function for scattered well dopants.
`scb=0.0`	Integral of the second distribution function for scattered well dopants.
`scc=0.0`	Integral of the third distribution function for scattered well dopants.
`sc=0.0 m`	Distance between OD-edge and nearest well edge.
`delvto=0.0 V`	Threshold voltage shift parameter.
`factuo=1.0`	Zero-field mobility pre-factor.
`absource=1E-12 m`^{2}	Bottom area of source junction.
`lssource=1E-6 m`	STI-edge length of source junction.
`lgsource=1E-6 m`	Gate-edge length of source junction.
`abdrain=1E-12 m`^{2}	Bottom area of drain junction.
`lsdrain=1E-6 m`	STI-edge length of drain junction.
`lgdrain=1E-6 m`	Gate-edge length of drain junction.
`as=1E-12 m`^{2}	Bottom area of source junction.
`ps=1E-6 m`	Perimeter of source junction.

© 2023 Cadence Design Systems, Inc.

`ad=1E-12 m`^{2}	Bottom area of drain junction.
`pd=1E-6 m`	Perimeter of drain junction.
`mulid0=1`	Ids multiplier.
`mult=1.0`	Number of devices in parallel.
`nf=1.0`	Number of fingers.
`ngcon=1.0`	Number of gate contacts.
`xgw=1.0E-7 m`	Distance from the gate contact to the channel edge.
`region=triode`	Estimated operating region. Spectre outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trise=0.0 K`	Temperature rise from ambient.
`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Definition

```
model modelName psp1021 parameter=value ...
```

Model Parameters

`level=102`	Model level.
`type=n`	Channel type parameter. Specify n for NMOS and p for PMOS. Possible values are `n` and `p`.
`tr=value of tnom C`	Nominal (reference) temperature.
`swnqs=0`	Flag for NQS. 0 means off. Numbers 1, 2, 3, 5, or 9 refer to collocation points.
`swigate=0`	Flag for gate current. 0 means turn off IG.
`swimpact=0`	Flag for impact ionization current. 0 means turn off impact ionization.
`swgidl=0`	Flag for GIDL current. 0 means turn off IGIDL.
`swjuncap=0`	Flag for juncap. 0 means turn off juncap.

© 2023 Cadence Design Systems, Inc.

`swjunasym=0`	Flag for asymmetric junctions. 0 means symmetric,and means asymmetric.
`qmc=1.0`	Quantum-mechanical correction factor.
`version=102.32`	Model parameter "version" accepts only real number value, like 102.21 for version=102.2.1. The available versions are 102.2, 102.21(102.2.1), 102.3, 102.32(102.3.2), 102.33(102.3.3), 102.34(102.3.4), 102.4(102.4.0), and 102.5(102.5.0).
`geomod=1`	1 for geometrical model and 0 for electrical model.
`binmod=0`	1 for bin model and 0 for non-bin model.
`scalelev=102`	102 for local, 1020 for global model and 1021 for bin model.
`compatible=spectre`	Compatibility parameter. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`lvaro=0.0 m`	Geometry-independent difference between actual and programmed gate length.
`lvarl=0.0`	Length dependence of LVAR.
`lap=0.0 m`	Effective channel length reduction per side.
`wvaro=0.0 m`	Geometry-independent difference between actual and programmed field-oxide opening.
`wvarw=0.0`	Width dependence of WVAR.
`wot=0.0 m`	Effective channel width reduction per side.
`dlq=0.0 m`	Effective channel length reduction for CV.
`dwq=0.0 m`	Effective channel width reduction for CV.
`povfb=(-1) V`	Coefficient for the geometry-independent part of VFB.
`plvfb=0.0 V`	Coefficient for the length dependence of VFB.
`pwvfb=0.0 V`	Coefficient for the width dependence of VFB.
`plwvfb=0.0 V`	Coefficient for the length times width dependence of VFB.
`postvfb=0.0005 V/K`	Coefficient for the geometry-independent part of STVFB.
`plstvfb=0.0 V/K`	Coefficient for the length dependence of STVFB.
`pwstvfb=0.0 V/K`	Coefficient for the width dependence of STVFB.

© 2023 Cadence Design Systems, Inc.

`plwstvfb=0.0 V/K`	Coefficient for the length times width dependence of STVFB.
`potox=2E-09 m`	Coefficient for the geometry-independent part of TOX.
`poepsrox=3.9`	Coefficient for the geometry-independent part of EPSOX.
`poneff=5E+23 m^-3`	Coefficient for the geometry-independent part of NEFF.
`plneff=0.0 m^-3`	Coefficient for the length dependence of NEFF.
`pwneff=0.0 m^-3`	Coefficient for the width dependence of NEFF.
`plwneff=0.0 m^-3`	Coefficient for the length times width dependence of NEFF.
`povnsub=0 V`	Coefficient for the geometry-independent part of VNSUB.
`ponslp=0.05 V`	Coefficient for the geometry-independent part of NSLP.
`podnsub=0 V^-1`	Coefficient for the geometry-independent part of DNSUB.
`podphib=0 V`	Coefficient for the geometry-independent part of DPHIB.
`pldphib=0.0 V`	Coefficient for the length dependence of DPHIB.
`pwdphib=0.0 V`	Coefficient for the width dependence of DPHIB.
`plwdphib=0.0 V`	Coefficient for the length times width dependence of DPHIB.
`ponp=1E+26 m^-3`	Coefficient for the geometry-independent part of NP.
`plnp=0.0 m^-3`	Coefficient for the length dependence of NP.
`pwnp=0.0 m^-3`	Coefficient for the width dependence of NP.
`plwnp=0.0 m^-3`	Coefficient for the length times width dependence of NP.
`poct=0`	Coefficient for the geometry-independent part of CT.
`plct=0.0`	Coefficient for the length dependence of CT.
`pwct=0.0`	Coefficient for the width dependence of CT.
`plwct=0.0`	Coefficient for the length times width dependence of CT.
`potoxov=2E-09 m`	Coefficient for the geometry-independent part of TOXOV.
`potoxovd=2E-09 m`	Coefficient for the geometry-independent part of TOXOV for drain side.
`ponov=5E+25 m^-3`	Coefficient for the geometry-independent part of NOV.
`plnov=0.0 m^-3`	Coefficient for the length dependence of NOV.
`pwnov=0.0 m^-3`	Coefficient for the width dependence of NOV.
`plwnov=0.0 m^-3`	Coefficient for the length times width dependence of NOV.

© 2023 Cadence Design Systems, Inc.

ponovd=5E+25 m^{-3}	Coefficient for the geometry-independent part of NOV for drain side.
plnovd=0.0 m^{-3}	Coefficient for the length dependence of NOV for drain side.
pwnovd=0.0 m^{-3}	Coefficient for the width dependence of NOV for drain side.
plwnovd=0.0 m^{-3}	Coefficient for the length times width dependence of NOV for drain side.
pocf=0	Coefficient for the geometry-independent part of CF.
plcf=0.0	Coefficient for the length dependence of CF.
pwcf=0.0	Coefficient for the width dependence of CF.
plwcf=0.0	Coefficient for the length times width dependence of CF.
pocfb=0 V^-1	Coefficient for the geometry-independent part of CFB.
pobetn=0.07 $m^2/V/s$	Coefficient for the geometry-independent part of BETN.
plbetn=0.0 $m^2/V/s$	Coefficient for the length dependence of BETN.
pwbetn=0.0 $m^2/V/s$	Coefficient for the width dependence of BETN.
plwbetn=0.0 $m^2/V/s$	Coefficient for the length times width dependence of BETN.
postbet=1	Coefficient for the geometry-independent part of STBET.
plstbet=0.0	Coefficient for the length dependence of STBET.
pwstbet=0.0	Coefficient for the width dependence of STBET.
plwstbet=0.0	Coefficient for the length times width dependence of STBET.
pomue=0.5 m/V	Coefficient for the geometry-independent part of MUE.
plmue=0.0 m/V	Coefficient for the length dependence of MUE.
pwmue=0.0 m/V	Coefficient for the width dependence of MUE.
plwmue=0.0 m/V	Coefficient for the length times width dependence of MUE.
postmue=0	Coefficient for the geometry-independent part of STMUE.
pothemu=1.5	Coefficient for the geometry-independent part of THEMU.

© 2023 Cadence Design Systems, Inc.

postthemu=1.5	Coefficient for the geometry-independent part of STTHEMU.
pocs=0	Coefficient for the geometry-independent part of CS.
plcs=0.0	Coefficient for the length dependence of CS.
pwcs=0.0	Coefficient for the width dependence of CS.
plwcs=0.0	Coefficient for the length times width dependence of CS.
postcs=0	Coefficient for the geometry-independent part of STCS.
poxcor=0 V^-1	Coefficient for the geometry-independent part of XCOR.
plxcor=0.0 V^-1	Coefficient for the length dependence of XCOR.
pwxcor=0.0 V^-1	Coefficient for the width dependence of XCOR.
plwxcor=0.0 V^-1	Coefficient for the length times width dependence of XCOR.
postxcor=0	Coefficient for the geometry-independent part of STXCOR.
pofeta=1	Coefficient for the geometry-independent part of FETA.
pors=30 Ω	Coefficient for the geometry-independent part of RS.
plrs=0.0 Ω	Coefficient for the length dependence of RS.
pwrs=0.0 Ω	Coefficient for the width dependence of RS.
plwrs=0.0 Ω	Coefficient for the length times width dependence of RS.
postrs=1	Coefficient for the geometry-independent part of STRS.
porsb=0 V^-1	Coefficient for the geometry-independent part of RSB.
porsg=0 V^-1	Coefficient for the geometry-independent part of RSG.
pothesat=1 V^-1	Coefficient for the geometry-independent part of THESAT.
plthesat=0.0 V^-1	Coefficient for the length dependence of THESAT.
pwthesat=0.0 V^-1	Coefficient for the width dependence of THESAT.
plwthesat=0.0 V^-1	Coefficient for the length times width dependence of THESAT.
postthesat=1	Coefficient for the geometry-independent part of STTHESAT.
plstthesat=0.0	Coefficient for the length dependence of STTHESAT.
pwstthesat=0.0	Coefficient for the width dependence of STTHESAT.
plwstthesat=0.0	Coefficient for the length times width dependence of STTHESAT.

© 2023 Cadence Design Systems, Inc.

`pothesatb=0 V^-1`	Coefficient for the geometry-independent part of THESATB.
`plthesatb=0.0 V^-1`	Coefficient for the length dependence of THESATB.
`pwthesatb=0.0 V^-1`	Coefficient for the width dependence of THESATB.
`plwthesatb=0.0 V^-1`	Coefficient for the length times width dependence of THESATB.
`pothesatg=0 V^-1`	Coefficient for the geometry-independent part of THESATG.
`plthesatg=0.0 V^-1`	Coefficient for the length dependence of THESATG.
`pwthesatg=0.0 V^-1`	Coefficient for the width dependence of THESATG.
`plwthesatg=0.0 V^-1`	Coefficient for the length times width dependence of THESATG.
`poax=3`	Coefficient for the geometry-independent part of AX.
`plax=0.0`	Coefficient for the length dependence of AX.
`pwax=0.0`	Coefficient for the width dependence of AX.
`plwax=0.0`	Coefficient for the length times width dependence of AX.
`poalp=0.01`	Coefficient for the geometry-independent part of ALP.
`plalp=0.0`	Coefficient for the length dependence of ALP.
`pwalp=0.0`	Coefficient for the width dependence of ALP.
`plwalp=0.0`	Coefficient for the length times width dependence of ALP.
`poalp1=0 V`	Coefficient for the geometry-independent part of ALP1.
`plalp1=0.0 V`	Coefficient for the length dependence of ALP1.
`pwalp1=0.0 V`	Coefficient for the width dependence of ALP1.
`plwalp1=0.0 V`	Coefficient for the length times width dependence of ALP1.
`poalp2=0 V^-1`	Coefficient for the geometry-independent part of ALP2.

© 2023 Cadence Design Systems, Inc.

`plalp2=0.0 V^-1`	Coefficient for the length dependence of ALP2.
`pwalp2=0.0 V^-1`	Coefficient for the width dependence of ALP2.
`plwalp2=0.0 V^-1`	Coefficient for the length times width dependence of ALP2.
`povp=0.05 V`	Coefficient for the geometry-independent part of VP.
`poa1=1`	Coefficient for the geometry-independent part of A1.
`pla1=0.0`	Coefficient for the length dependence of A1.
`pwa1=0.0`	Coefficient for the width dependence of A1.
`plwa1=0.0`	Coefficient for the length times width dependence of A1.
`poa2=10 V`	Coefficient for the geometry-independent part of A2.
`posta2=0 V`	Coefficient for the geometry-independent part of STA2.
`poa3=1`	Coefficient for the geometry-independent part of A3.
`pla3=0.0`	Coefficient for the length dependence of A3.
`pwa3=0.0`	Coefficient for the width dependence of A3.
`plwa3=0.0`	Coefficient for the length times width dependence of A3.
`poa4=0 V^-0.5`	Coefficient for the geometry-independent part of A4.
`pla4=0.0 V^-0.5`	Coefficient for the length dependence of A4.
`pwa4=0.0 V^-0.5`	Coefficient for the width dependence of A4.
`plwa4=0.0 V^-0.5`	Coefficient for the length times width dependence of A4.
`pogco=0`	Coefficient for the geometry-independent part of GCO.
`poiginv=0 A`	Coefficient for the geometry-independent part of IGINV.
`pliginv=0.0 A`	Coefficient for the length dependence of IGINV.
`pwiginv=0.0 A`	Coefficient for the width dependence of IGINV.
`plwiginv=0.0 A`	Coefficient for the length times width dependence of IGINV.
`poigov=0 A`	Coefficient for the geometry-independent part of IGOV.
`pligov=0.0 A`	Coefficient for the length dependence of IGOV.
`pwigov=0.0 A`	Coefficient for the width dependence of IGOV.
`plwigov=0.0 A`	Coefficient for the length times width dependence of IGOV.
`poigovd=0 A`	Coefficient for the geometry-independent part of IGOV for drain side.

© 2023 Cadence Design Systems, Inc.

`pligovd=0.0 A`	Coefficient for the length dependence of IGOV for drain side.
`pwigovd=0.0 A`	Coefficient for the width dependence of IGOV for drain side.
`plwigovd=0.0 A`	Coefficient for the length times width dependence of IGOV for drain side.
`postig=2`	Coefficient for the geometry-independent part of STIG.
`pogc2=0.375`	Coefficient for the geometry-independent part of GC2.
`pogc3=0.063`	Coefficient for the geometry-independent part of GC3.
`pochib=3.1 V`	Coefficient for the geometry-independent part of CHIB.
`poagidl=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL.
`plagidl=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL.
`pwagidl=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL.
`plwagidl=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL.
`poagidld=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL for drain side.
`plagidld=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL for drain side.
`pwagidld=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL for drain side.
`plwagidld=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL for drain side.
`pobgidl=41 V`	Coefficient for the geometry-independent part of BGIDL.
`pobgidld=41 V`	Coefficient for the geometry-independent part of BGIDL for drain side.
`postbgidl=0 V/K`	Coefficient for the geometry-independent part of STBGIDL.
`postbgidld=0 V/K`	Coefficient for the geometry-independent part of STBGIDL for drain side.
`pocgidl=0`	Coefficient for the geometry-independent part of CGIDL.
`pocgidld=0`	Coefficient for the geometry-independent part of CGIDL for drain side.

© 2023 Cadence Design Systems, Inc.

pocox=1E-14 F	Coefficient for the geometry-independent part of COX.
plcox=0.0 F	Coefficient for the length dependence of COX.
pwcox=0.0 F	Coefficient for the width dependence of COX.
plwcox=0.0 F	Coefficient for the length times width dependence of COX.
pocgov=1E-15 F	Coefficient for the geometry-independent part of CGOV.
plcgov=0.0 F	Coefficient for the length dependence of CGOV.
pwcgov=0.0 F	Coefficient for the width dependence of CGOV.
plwcgov=0.0 F	Coefficient for the length times width dependence of CGOV.
pocgovd=1E-15 F	Coefficient for the geometry-independent part of CGOV for drain side.
plcgovd=0.0 F	Coefficient for the length dependence of CGOV for drain side.
pwcgovd=0.0 F	Coefficient for the width dependence of CGOV for drain side.
plwcgovd=0.0 F	Coefficient for the length times width dependence of CGOV for drain side.
pocgbov=0 F	Coefficient for the geometry-independent part of CGBOV.
plcgbov=0.0 F	Coefficient for the length dependence of CGBOV.
pwcgbov=0.0 F	Coefficient for the width dependence of CGBOV.
plwcgbov=0.0 F	Coefficient for the length times width dependence of CGBOV.
pocfr=0 F	Coefficient for the geometry-independent part of CFR.
plcfr=0.0 F	Coefficient for the length dependence of CFR.
pwcfr=0.0 F	Coefficient for the width dependence of CFR.
plwcfr=0.0 F	Coefficient for the length times width dependence of CFR.
pocfrd=0 F	Coefficient for the geometry-independent part of CFR for drain side.
plcfrd=0.0 F	Coefficient for the length dependence of CFR for drain side.
pwcfrd=0.0 F	Coefficient for the width dependence of CFR for drain side.
plwcfrd=0.0 F	Coefficient for the length times width dependence of CFR for drain side.
pofnt=1	Coefficient for the geometry-independent part of FNT.
pofntexc=0.0	Coefficient for the geometry-independent part of FNTEXC.

© 2023 Cadence Design Systems, Inc.

`plfntexc=0.0`	Coefficient for the length dependence of FNTEXC.
`pwfntexc=0.0`	Coefficient for the width dependence of FNTEXC.
`plwfntexc=0.0`	Coefficient for the length times width dependence of FNTEXC.
`ponfa=8E+22 V^-1/m`^{4}	Coefficient for the geometry-independent part of NFA.
`plnfa=0.0 V^-1/m`^{4}	Coefficient for the length dependence of NFA.
`pwnfa=0.0 V^-1/m`^{4}	Coefficient for the width dependence of NFA.
`plwnfa=0.0 V^-1/m`^{4}	Coefficient for the length times width dependence of NFA.
`ponfb=3E+07 V^-1/m`^{2}	Coefficient for the geometry-independent part of NFB.
`plnfb=0.0 V^-1/m`^{2}	Coefficient for the length dependence of NFB.
`pwnfb=0.0 V^-1/m`^{2}	Coefficient for the width dependence of NFB.
`plwnfb=0.0 V^-1/m`^{2}	Coefficient for the length times width dependence of NFB.
`ponfc=0 V^-1`	Coefficient for the geometry-independent part of NFC.
`plnfc=0.0 V^-1`	Coefficient for the length dependence of NFC.
`pwnfc=0.0 V^-1`	Coefficient for the width dependence of NFC.
`plwnfc=0.0 V^-1`	Coefficient for the length times width dependence of NFC.
`poef=1.0`	Coefficient for the flicker noise frequency exponent.
`dta=0 K`	Temperature offset w.r.t. ambient circuit temperature.
`pokvthowe=0`	Coefficient for the geometry-independent part of KVTHOWE.
`plkvthowe=0`	Coefficient for the length dependence part of KVTHOWE.
`pwkvthowe=0`	Coefficient for the width dependence part of KVTHOWE.

© 2023 Cadence Design Systems, Inc.

`plwkvthowe=0`	Coefficient for the length times width dependence part of KVTHOWE.
`pokuowe=0`	Coefficient for the geometry-independent part of KUOWE.
`plkuowe=0`	Coefficient for the length dependence part of KUOWE.
`pwkuowe=0`	Coefficient for the width dependence part of KUOWE.
`plwkuowe=0`	Coefficient for the length times width dependence part of KUOWE.
`lmin=0 m`	Dummy parameter to label binning set.
`lmax=1.0 m`	Dummy parameter to label binning set.
`wmin=0 m`	Dummy parameter to label binning set.
`wmax=1.0 m`	Dummy parameter to label binning set.
`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.
`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.
`vgbr_max=vgb_max V`	Maximum allowed reverse voltage cross gate and bulk.
`vbsr_max=vbs_max V`	

© 2023 Cadence Design Systems, Inc.

	Maximum allowed reverse voltage cross source and bulk.
`vbdr_max=vbd_max V`	
	Maximum allowed reverse voltage cross source/drain and bulk.
`munqso=1.0`	Relative mobility for NQS modelling.
`rgo=0.0 Ω`	Gate resistance.
`rbulko=0.0 Ω`	Bulk resistance between node BP and BI.
`rwello=0.0 Ω`	Well resistance between node BI and B.
`rjunso=0.0 Ω`	Source-side bulk resistance between node BI and BS.
`rjundo=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
`rint=0.0 Ω/Sqr`	Contact resistance between silicide and ploy.
`rvpoly=0.0 Ω/Sqr`	
	Vertical poly resistance.
`rshg=0.0 Ω/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0.0 m`	Silicide extension over the physical gate length.
`saref=1.0e-6 m`	Reference distance between OD-edge and poly from one side.
`sbref=1.0e-6 m`	Reference distance between OD-edge and poly from other side.
`wlod=0 m`	Width parameter.
`kuo=0 m`	Mobility degradation/enhancement coefficient.
`kvsat=0 m`	Saturation velocity degradation/enhancement coefficient.
`tkuo=0`	Temperature dependence of KUO.
`lkuo=0 m^LLODKUO`	Length dependence of KUO.
`wkuo=0 m^WLODKUO`	Width dependence of KUO.
`pkuo=0 m^(LLODKUO+WLODKUO)`	
	Cross-term dependence of KUO.
`llodkuo=0`	Length parameter for UO stress effect.
`wlodkuo=0`	Width parameter for UO stress effect.

© 2023 Cadence Design Systems, Inc.

`kvtho=0 Vm`	Threshold shift parameter.
`lkvtho=0 m^LLODVTH`	Length dependence of KVTHO.
`wkvtho=0 m^WLODVTH`	Width dependence of KVTHO.
`pkvtho=0 m^(LLODVTH+WLODVTH)`	Cross-term dependence of KVTHO.
`llodvth=0`	Length parameter for VTH-stress effect.
`wlodvth=0`	Width parameter for VTH-stress effect.
`stetao=0 m`	eta0 shift factor related to VTHO change.
`lodetao=1.0`	eta0 shift modification factor for stress effect.
`scref=10e-6 m`	Distance between OD-edge and well edge of a reference device.
`web=0`	Coefficient for SCB.
`wec=0`	Coefficient for SCC.
`imax=1000 A`	Maximum current up to which forward current behaves exponentially.
`trj=21 C`	reference temperature.
`cjorbot=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.
`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.
`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.
`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
`idsatrbot=1E-12` Am^{-2}	Saturation current density at the reference temperature of bottom component for source-bulk junction.
`idsatrsti=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
`idsatrgat=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
`csrhbot=1E2` Am^{-3}	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
`csrhsti=1E-4` Am^{-2}	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
`csrhgat=1E-4` Am^{-2}	

© 2023 Cadence Design Systems, Inc.

	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.
`xjunsti=100E-9 m`	Junction depth of STI-edge component for source-bulk junction.
`xjungat=100E-9 m`	Junction depth of gate-edge component for source-bulk junction.
`ctatbot=1E2 Am`$^{-3}$	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
`ctatsti=1E-4 Am`$^{-2}$	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
`ctatgat=1E-4 Am`$^{-2}$	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
`mefftatbot=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
`mefftatsti=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
`mefftatgat=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
`cbbtbot=1E-12 AV`$^{-3}$	Band-to-band tunneling prefactor of bottom component for source-bulk junction.
`cbbtsti=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
`cbbtgat=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
`fbbtrbot=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.
`fbbtrsti=1E9 Vm^-1`	

© 2023 Cadence Design Systems, Inc.

	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
`fbbtrgat=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
`stfbbtbot=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
`stfbbtsti=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
`stfbbtgat=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
`vbrbot=10 V`	Breakdown voltage of bottom component for source-bulk junction.
`vbrsti=10 V`	Breakdown voltage of STI-edge component for source-bulk junction.
`vbrgat=10 V`	Breakdown voltage of gate-edge component for source-bulk junction.
`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component for source-bulk junction.
`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
`cjorbotd=1E-3 Fm`$^{-2}$	
	Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.
`cjorstid=1E-9 Fm^-1`	
	Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`cjorgatd=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.
`vbirbotd=1 V`	Built-in voltage at the reference temperature of bottom component for drain-bulk junction.
`vbirstid=1 V`	Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.
`vbirgatd=1 V`	Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.
`pbotd=0.5`	Grading coefficient of bottom component for drain-bulk junction.
`pstid=0.5`	Grading coefficient of STI-edge component for drain-bulk junction.
`pgatd=0.5`	Grading coefficient of gate-edge component for drain-bulk junction.
`phigbotd=1.16 V`	Zero-temperature bandgap voltage of bottom component for drain-bulk junction.
`phigstid=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.
`phiggatd=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.
`idsatrbotd=1E-12 Am`$^{-2}$	Saturation current density at the reference temperature of bottom component for drain-bulk junction.
`idsatrstid=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.
`idsatrgatd=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.
`csrhbotd=1E2 Am`$^{-3}$	Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

csrhstid=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
csrhgatd=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
xjunstid=100E-9 m	Junction depth of STI-edge component for drain-bulk junction.
xjungatd=100E-9 m	Junction depth of gate-edge component for drain-bulk junction.
ctatbotd=1E2 Am^{-3}	
	Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
ctatstid=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
ctatgatd=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.
mefftatbotd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
mefftatstid=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.
mefftatgatd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
cbbtbotd=1E-12 AV^{-3}	
	Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
cbbtstid=1E-18 $AV^{-3}m$	
	Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.
cbbtgatd=1E-18 $AV^{-3}m$	
	Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`fbbtrbotd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.
`fbbtrstid=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.
`fbbtrgatd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.
`stfbbtbotd=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.
`stfbbtstid=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.
`stfbbtgatd=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.
`vbrbotd=10 V`	Breakdown voltage of bottom component for drain-bulk junction.
`vbrstid=10 V`	Breakdown voltage of STI-edge component for drain-bulk junction.
`vbrgatd=10 V`	Breakdown voltage of gate-edge component for drain-bulk junction.
`pbrbotd=4 V`	Breakdown onset tuning parameter of bottom component for drain-bulk junction.
`pbrstid=4 V`	Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.
`pbrgatd=4 V`	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
`swjunexp=0.0`	Flag for JUNCAP express. Specify 0 for full model and 1 for express model.

© 2023 Cadence Design Systems, Inc.

`vjunref=2.5`	The maximum source-bulk junction voltage; usually about 2*VSUP.
`fjunq=0.03`	Fraction below which source-bulk junction capacitance components are considered negligible.
`vjunrefd=2.5`	The maximum drain-bulk junction voltage; usually about 2*VSUP.
`fjunqd=0.03`	Fraction below which drain-bulk junction capacitance components are considered negligible.
`mvto=0.0`	DCmatch parameter.
`mbeo=0.0`	DCmatch parameter.
`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
`noisemethod=oldcmi`	Induced gate noise implementation. Possible values are `oldcmi`, `subckt`, `newcmi`, and `noign`.

Output Parameters

`weff (m)`	Effective channel width for geometrical models.
`leff (m)`	Effective channel length for geometrical models.
`lv1 (m)`	Alias of l.
`lv2 (m)`	Alias of w.
`lv3 ($m^2$)`	Alias of ad.

© 2023 Cadence Design Systems, Inc.

lv4 (m^2)	Alias of as.
lv11 (m)	Alias of pd.
lv12 (m)	Alias of ps.

Operating-Point Parameters

region=triode	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are off, triode, sat, subth, and breakdown.
dtsh (K)	Device temperature rise due to self-heating.
ctype	Flag for channel type.
sdint	Flag for source-drain interchange.
is (A)	External DC current at source terminal.
ise (A)	Total source current.
ig (A)	External DC current at gate terminal.
ige (A)	Total gate current.
id (A)	External DC current at drain terminal.
ide (A)	Total drain current.
ib (A)	Total bulk current.
ibe (A)	Total bulk current.
ids (A)	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
idb (A)	Drain to bulk current.
isb (A)	Source to bulk current.
igs (A)	Gate-source tunneling current.
igd (A)	Gate-drain tunneling current.
igb (A)	Gate-bulk tunneling current.
igcs (A)	Gate-channel tunneling current (source component).
igcd (A)	Gate-channel tunneling current (drain component).
iavl (A)	Substrate current due to weak avalanche.

© 2023 Cadence Design Systems, Inc.

igisl (A)	Gate-induced source leakage current.
igidl (A)	Gate-induced drain leakage current.
ijs (A)	Total source junction current.
ijsbot (A)	Source junction current (bottom component).
ijsgat (A)	Source junction current (gate-edge component).
ijssti (A)	Source junction current (STI-edge component).
ijd (A)	Total drain junction current.
ijdbot (A)	Drain junction current (bottom component).
ijdgat (A)	Drain junction current (gate-edge component).
ijdsti (A)	Drain junction current (STI-edge component).
qg (Coul)	Intrinsic gate charge.
qd (Coul)	Intrinsic drain charge.
qb (Coul)	Intrinsic bulk charge.
qs (Coul)	Intrinsic source charge.
qgs_ov (Coul)	Overlap charge for gate-source.
qgd_ov (Coul)	Overlap charge for gate-drain.
qfgs (Coul)	Sum of outerFringe and overlap for gate-source.
qfgd (Coul)	Sum of outerFringe and overlap for gate-drain.
qgb_ov (Coul)	Gate-bulk overlap charge.
qjun_s (Coul)	Junction charge on source side.
qjun_d (Coul)	Junction charge on drain side.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vgd (V)	External gate-drain DC voltage.
vsb (V)	Source-bulk voltage.
vdb (V)	External drain-bulk DC voltage.
vth0 (V)	Zero-bias threshold voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back bias effects.

© 2023 Cadence Design Systems, Inc.

vth (V)	Threshold voltage including back bias and drain bias effects.
vth_drive (V)	Gate overdrive voltage including back-bias, drain bias effects.
vgt (V)	Effective gate drive voltage including back bias and drain bias effects.
vdss (V)	Drain saturation voltage at actual bias.
vdsat (V)	Drain saturation voltage.
vdsat_marg (V)	Saturation margin with respect to Vdsat for Drain voltage.
vsat (V)	Saturation limit.
pwr (W)	Power at op point.
gm (1/Ω)	Transconductance.
gmb (1/Ω)	Substrate transconductance.
go (1/Ω)	Output conductance.
gds (1/Ω)	Output conductance.
gjs (1/Ω)	Source junction conductance.
gjd (1/Ω)	Drain junction conductance.
cdd (F)	Drain capacitance.
cdg (F)	Drain-gate capacitance.
cds (F)	Drain-source capacitance.
cdb (F)	Drain-bulk capacitance.
cgd (F)	Gate-drain capacitance.
cgg (F)	Gate capacitance.
cgs (F)	Gate-source capacitance.
cgb (F)	Gate-bulk capacitance.
csd (F)	Source-drain capacitance.
csg (F)	Source-gate capacitance.
css (F)	Source capacitance.
csb (F)	Source-bulk capacitance.
cbd (F)	Bulk-drain capacitance.
cbg (F)	Bulk-gate capacitance.

© 2023 Cadence Design Systems, Inc.

cbs (F)	Bulk-source capacitance.
cbb (F)	Bulk capacitance.
co (F)	Output Drain-Source capacitance.
cm (F)	Capacitance element 1 for QS model.
cmb (F)	Capacitance element 2 for QS model.
cmx (F)	Capacitance element 3 for QS model.
tau1 (s)	Time constant related to NQS first frequency pole.
fqslim (Hz)	QS model frequency limit.
cgsol (F)	Total gate-source overlap capacitance.
cgdol (F)	Total gate-drain overlap capacitance.
cgbol (F)	Total gate-bulk overlap capacitance.
cjs (F)	Total source junction capacitance.
cjsbot (F)	Source junction capacitance (bottom component).
cjsgat (F)	Source junction capacitance (gate-edge component).
cjssti (F)	Source junction capacitance (STI-edge component).
cjd (F)	Total drain junction capacitance.
cjdbot (F)	Drain junction capacitance (bottom component).
cjdgat (F)	Drain junction capacitance (gate-edge component).
cjdsti (F)	Drain junction capacitance (STI-edge component).
lpoly (m)	Length of poly.
self_gain	Gm/Go ratio (MOSFET self-gain).
u	Transistor gain.
rout (Ω)	Small-signal output resistance.
vearly (V)	Equivalent Early voltage.
ft (Hz)	Unity gain frequency at actual bias.
beff (A/V^2)	Gain factor.
gmoveri (1/V)	Transconductance efficiency.
fug (Hz)	Unity gain frequency at actual bias.
rgate (Ω)	Gate resistance.

© 2023 Cadence Design Systems, Inc.

`rg (Ω)`	Gate resistance.
`sfl (A²/Hz)`	Flicker noise current spectral density at 1 Hz.
`sqrtsff (V/√Hz)`	Input-referred RMS white noise voltage spectral density at 1 kHz.
`sqrtsfw (V/√Hz)`	Input-referred RMS white noise voltage spectral density.
`sid (A²/Hz)`	White noise current spectral density.
`sig (A²/Hz)`	Induced gate noise current spectral density at 1 Hz.
`cigid`	Imaginary part of correlation coefficient between Sig and Sid.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`sigs (A²/Hz)`	Gate-source current noise spectral density.
`sigd (A²/Hz)`	Gate-drain current noise spectral density.
`siavl (A²/Hz)`	Impact ionization current noise spectral density.
`ssi (A²/Hz)`	Total source junction current noise spectral density.
`sdi (A²/Hz)`	Total drain junction current noise spectral density.
`vbs (V)`	Bulk-source voltage.
`lv9 (V)`	Alias of vth.
`lv10 (V)`	Alias of vdss.
`lv36 (F)`	Alias of cgsol.
`lv37 (F)`	Alias of cgdol.
`lv38 (F)`	Alias of cgbol.
`lv51 (m)`	Alias of tox.
`lx4 (A)`	Alias of ids.
`lx3 (V)`	Alias of vds.
`lx2 (V)`	Alias of vgs.
`lx7 (1/Ω)`	Alias of gm.
`lx8 (1/Ω)`	Alias of gds.
`lx9 (1/Ω)`	Alias of gmb.

© 2023 Cadence Design Systems, Inc.

lx33 (F)	Alias of cdd.
lx32 (F)	Alias of cdg.
lx34 (F)	Alias of cds.
lx19 (F)	Alias of cgd.
lx18 (F)	Alias of cgg.
lx20 (F)	Alias of cgs.
lx22 (F)	Alias of cbd.
lx21 (F)	Alias of cbg.
lx23 (F)	Alias of cbs.
lx5 (A)	Alias of ijs.
lx6 (A)	Alias of ijd.
lx28 (F)	Alias of cjs.
lx29 (F)	Alias of cjd.
lx38 (A)	Alias of igs.
lx39 (A)	Alias of igd.
lx66 (A)	Alias of igb.
lx67 (A)	Alias of igcs.
lx68 (A)	Alias of igcd.
lx110 (A)	Alias of igisl.
lx47 (A)	Alias of igidl.
lx60 (F)	Alias of csd.
lx59 (F)	Alias of csg.
lx58 (F)	Alias of css.
lx12 (Coul)	Alias of Qb including overlap charge.
lx14 (Coul)	Alias of Qg including overlap charge.
lx16 (Coul)	Alias of Qd including overlap charge.
lx83 (F)	Alias of cgd including overlap cap.
lx84 (F)	Alias of cgs including overlap cap.
OPdef	1: Device Physics notation. 2: Circuit Simulator notation.

© 2023 Cadence Design Systems, Inc.

`SDop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.

Related Topics

PSP102 Model

Component Statements for PSP102 Models

PSP MOSFET Model (PSP102)

PSP MOSFET Model (psp1020)

PSP local MOSFET Model (psp102e)

PSP NQS MOSFET Model (pspnqs1020)

PSP NQS MOSFET Model (pspnqs1021)

PSP NQS local MOSFET Model (pspnqs102e)

PSP local MOSFET Model (psp102e)

This is SiMKit 4.0.1.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`delvto=0.0 V`	Threshold voltage shift parameter.
`factuo=1.0`	Zero-field mobility pre-factor.
`absource=1E-12 m`^{2}	

© 2023 Cadence Design Systems, Inc.

	Bottom area of source junction.
`lssource=1E-6 m`	STI-edge length of source junction.
`lgsource=1E-6 m`	Gate-edge length of source junction.
`abdrain=1E-12 m`^{2}	Bottom area of drain junction.
`lsdrain=1E-6 m`	STI-edge length of drain junction.
`lgdrain=1E-6 m`	Gate-edge length of drain junction.
`as=1E-12 m`^{2}	Bottom area of source junction.
`ps=1E-6 m`	Perimeter of source junction.
`ad=1E-12 m`^{2}	Bottom area of drain junction.
`pd=1E-6 m`	Perimeter of drain junction.
`mulid0=1`	Ids multiplier.
`jw=1E-6 m`	Gate-edge length of source/drain junction.
`mult=1.0`	Number of devices in parallel.
`region=triode`	Estimated operating region. Spectre outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trise=0.0 K`	Temperature rise from ambient.
`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Definition

```
model modelName psp102e parameter=value ...
```

Model Parameters

`level=102`	Model level.
`type=n`	Channel type parameter. Specify n for NMOS and p for PMOS. Possible values are `n` and `p`.
`tr=value of tnom C`	Nominal (reference) temperature.

© 2023 Cadence Design Systems, Inc.

`swnqs=0`	Flag for NQS. 0 means off. Numbers 1, 2, 3, 5, or 9 refer to collocation points.
`swigate=0`	Flag for gate current. 0 means turn off IG.
`swimpact=0`	Flag for impact ionization current. 0 means turn off impact ionization.
`swgidl=0`	Flag for GIDL current. 0 means turn off IGIDL.
`swjuncap=0`	Flag for juncap. 0 means turn off juncap.
`swjunasym=0`	Flag for asymmetric junctions. 0 means symmetric, and 1 means asymmetric.
`qmc=1.0`	Quantum-mechanical correction factor.
`version=102.32`	Model parameter "version" accepts only real number value, like 102.21 for version=102.2.1. The available versions are 102.2, 102.21(102.2.1), 102.3, 102.32(102.3.2), 102.33(102.3.3), 102.34(102.3.4), 102.4(102.4.0), and 102.5(102.5.0).
`geomod=1`	1 for geometrical model and 0 for electrical model.
`binmod=0`	1 for bin model and 0 for non-bin model.
`scalelev=102`	102 for local, 1020 for global model and 1021 for bin model.
`compatible=spectre`	Compatibility parameter. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`vfb=(-1.0) V`	Flatband voltage at TR.
`stvfb=5.0e-4 V/K`	Temperature dependence of VFB.
`tox=2.0e-09 m`	Gate oxide thickness.
`epsrox=3.9`	Relative permittivity of gate dielectric.
`neff=5.0e+23` m^{-3}	Effective substrate doping.
`vnsub=0.0 V`	Effective doping bias-dependence parameter.
`nslp=0.05 V`	Effective doping bias-dependence parameter.
`dnsub=0.0 V^-1`	Effective doping bias-dependence parameter.
`dphib=0.0 V`	Offset parameter for PHIB.
`np=1.0e+26` m^{-3}	Gate poly-silicon doping.
`ct=0.0`	Interface states factor.

© 2023 Cadence Design Systems, Inc.

`toxov=2.0e-09 m`	Overlap oxide thickness.
`toxovd=2.0e-09 m`	Overlap oxide thickness for drain side.
`nov=5.0e+25` m^{-3}	Effective doping of overlap region.
`novd=5.0e+25` m^{-3}	Effective doping of overlap region for drain side.
`cf=0.0`	DIBL-parameter.
`cfb=0.0 V^-1`	Back bias dependence of CF.
`betn=7e-2` $m^2/V/s$	Channel aspect ratio times zero-field mobility.
`stbet=1.0`	Temperature dependence of BETN.
`mue=0.5 m/V`	Mobility reduction coefficient at TR.
`stmue=0.0`	Temperature dependence of MUE.
`themu=1.5`	Mobility reduction exponent at TR.
`stthemu=1.5`	Temperature dependence of THEMU.
`cs=0.0`	Coulomb scattering parameter at TR.
`stcs=0.0`	Temperature dependence of CS.
`xcor=0.0 V^-1`	Non-universality factor.
`stxcor=0.0`	Temperature dependence of XCOR.
`feta=1.0`	Effective field parameter.
`rs=30 Ω`	Series resistance at TR.
`strs=1.0`	Temperature dependence of RS.
`rsb=0.0 V^-1`	Back-bias dependence of series resistance.
`rsg=0.0 V^-1`	Gate-bias dependence of series resistance.
`thesat=1.0 V^-1`	Velocity saturation parameter at TR.
`stthesat=1.0`	Temperature dependence of THESAT.
`thesatb=0.0 V^-1`	Back-bias dependence of velocity saturation.
`thesatg=0.0 V^-1`	Gate-bias dependence of velocity saturation.
`ax=3.0`	Linear/saturation transition factor.
`alp=0.01`	CLM pre-factor.
`alp1=0.00 V`	CLM enhancement factor above threshold.
`alp2=0.00 V^-1`	CLM enhancement factor below threshold.

© 2023 Cadence Design Systems, Inc.

`vp=0.05 V`	CLM logarithm dependence factor.
`a1=1.0`	Impact-ionization pre-factor.
`a2=10.0 V`	Impact-ionization exponent at TR.
`sta2=0.0 V`	Temperature dependence of A2.
`a3=1.0`	Saturation-voltage dependence of impact-ionization.
`a4=0.0 V^-0.5`	Back-bias dependence of impact-ionization.
`gco=0.0`	Gate tunneling energy adjustment.
`iginv=0.0 A`	Gate channel current pre-factor.
`igov=0.0 A`	Gate overlap current pre-factor.
`igovd=0.0 A`	Gate overlap current pre-factor for drain side.
`stig=2.0`	Temperature dependence of IGINV and IGOV.
`gc2=0.375`	Gate current slope factor.
`gc3=0.063`	Gate current curvature factor.
`chib=3.1 V`	Tunneling barrier height.
`agidl=0.0 A/V`^{3}	GIDL pre-factor.
`agidld=0.0 A/V`^{3}	GIDL pre-factor for drain side.
`bgidl=41.0 V`	GIDL probability factor at TR.
`bgidld=41.0 V`	GIDL probability factor at TR for drain side.
`stbgidl=0.0 V/K`	Temperature dependence of BGIDL.
`stbgidld=0.0 V/K`	Temperature dependence of BGIDL for drain side.
`cgidl=0.0`	Back-bias dependence of GIDL.
`cgidld=0.0`	Back-bias dependence of GIDL for drain side.
`cox=1.0e-14 F`	Oxide capacitance for intrinsic channel.
`cgov=1.0e-15 F`	Oxide capacitance for gate-drain/source overlap.
`cgovd=1.0e-15 F`	Oxide capacitance for gate-drain overlap.
`cgbov=0.0 F`	Oxide capacitance for gate-bulk overlap.
`cfr=0.0 F`	Outer fringe capacitance.
`cfrd=0.0 F`	Outer fringe capacitance for drain side.
`fnt=1.0`	Thermal noise coefficient.

© 2023 Cadence Design Systems, Inc.

`fntexc=0.0`	Excess noise coefficient.
`nfa=8.0e+22 V^-1/m`^{4}	First coefficient of flicker noise.
`nfb=3.0e+07 V^-1/m`^{2}	Second coefficient of flicker noise.
`nfc=0.0 V^-1`	Third coefficient of flicker noise.
`ef=1.0`	Flicker noise frequency exponent.
`munqs=1.0`	Relative mobility for NQS modelling.
`rg=0.0 Ω`	Gate resistance.
`rbulk=0.0 Ω`	Bulk resistance between node BP and BI.
`rwell=0.0 Ω`	Well resistance between node BI and B.
`rjuns=0.0 Ω`	Source-side bulk resistance between node BI and BS.
`rjund=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
`imax=1000 A`	Maximum current up to which forward current behaves exponentially.
`trj=21 C`	reference temperature.
`cjorbot=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.
`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.
`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.
`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
`idsatrbot=1E-12 Am`$^{-2}$	Saturation current density at the reference temperature of bottom component for source-bulk junction.
`idsatrsti=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
`idsatrgat=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
`csrhbot=1E2 Am`$^{-3}$	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
`csrhsti=1E-4 Am`$^{-2}$	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
`csrhgat=1E-4 Am`$^{-2}$	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.
`xjunsti=100E-9 m`	Junction depth of STI-edge component for source-bulk junction.
`xjungat=100E-9 m`	Junction depth of gate-edge component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`ctatbot=1E2 Am^-3`	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
`ctatsti=1E-4 Am^-2`	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
`ctatgat=1E-4 Am^-2`	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
`mefftatbot=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
`mefftatsti=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
`mefftatgat=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
`cbbtbot=1E-12 AV^-3`	Band-to-band tunneling prefactor of bottom component for source-bulk junction.
`cbbtsti=1E-18 AV^-3m`	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
`cbbtgat=1E-18 AV^-3m`	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
`fbbtrbot=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.
`fbbtrsti=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
`fbbtrgat=1E9 Vm^-1`	

© 2023 Cadence Design Systems, Inc.

	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
stfbbtbot=(-1E-3) K^-1	
	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
stfbbtsti=(-1E-3) K^-1	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
stfbbtgat=(-1E-3) K^-1	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
vbrbot=10 V	Breakdown voltage of bottom component for source-bulk junction.
vbrsti=10 V	Breakdown voltage of STI-edge component for source-bulk junction.
vbrgat=10 V	Breakdown voltage of gate-edge component for source-bulk junction.
pbrbot=4 V	Breakdown onset tuning parameter of bottom component for source-bulk junction.
pbrsti=4 V	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
pbrgat=4 V	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
cjorbotd=1E-3 Fm^{-2}	
	Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.
cjorstid=1E-9 Fm^-1	
	Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.
cjorgatd=1E-9 Fm^-1	

© 2023 Cadence Design Systems, Inc.

	Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.
`vbirbotd=1 V`	Built-in voltage at the reference temperature of bottom component for drain-bulk junction.
`vbirstid=1 V`	Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.
`vbirgatd=1 V`	Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.
`pbotd=0.5`	Grading coefficient of bottom component for drain-bulk junction.
`pstid=0.5`	Grading coefficient of STI-edge component for drain-bulk junction.
`pgatd=0.5`	Grading coefficient of gate-edge component for drain-bulk junction.
`phigbotd=1.16 V`	Zero-temperature bandgap voltage of bottom component for drain-bulk junction.
`phigstid=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.
`phiggatd=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.
`idsatrbotd=1E-12 Am`$^{-2}$	Saturation current density at the reference temperature of bottom component for drain-bulk junction.
`idsatrstid=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.
`idsatrgatd=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.
`csrhbotd=1E2 Am`$^{-3}$	Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.
`csrhstid=1E-4 Am`$^{-2}$	

© 2023 Cadence Design Systems, Inc.

	Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
csrhgatd=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
xjunstid=100E-9 m	Junction depth of STI-edge component for drain-bulk junction.
xjungatd=100E-9 m	Junction depth of gate-edge component for drain-bulk junction.
ctatbotd=1E2 Am^{-3}	
	Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
ctatstid=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
ctatgatd=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.
mefftatbotd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
mefftatstid=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.
mefftatgatd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
cbbtbotd=1E-12 AV^{-3}	
	Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
cbbtstid=1E-18 $AV^{-3}m$	
	Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.
cbbtgatd=1E-18 $AV^{-3}m$	
	Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.
fbbtrbotd=1E9 Vm^-1	

© 2023 Cadence Design Systems, Inc.

	Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.
`fbbtrstid=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.
`fbbtrgatd=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.
`stfbbtbotd=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.
`stfbbtstid=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.
`stfbbtgatd=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.
`vbrbotd=10 V`	Breakdown voltage of bottom component for drain-bulk junction.
`vbrstid=10 V`	Breakdown voltage of STI-edge component for drain-bulk junction.
`vbrgatd=10 V`	Breakdown voltage of gate-edge component for drain-bulk junction.
`pbrbotd=4 V`	Breakdown onset tuning parameter of bottom component for drain-bulk junction.
`pbrstid=4 V`	Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.
`pbrgatd=4 V`	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
`swjunexp=0.0`	Flag for JUNCAP express. Specify 0 for full model and 1 for express model.
`vjunref=2.5`	The maximum source-bulk junction voltage; usually about 2*VSUP.

© 2023 Cadence Design Systems, Inc.

`fjunq=0.03`	Fraction below which source-bulk junction capacitance components are considered negligible.
`vjunrefd=2.5`	The maximum drain-bulk junction voltage; usually about 2*VSUP.
`fjunqd=0.03`	Fraction below which drain-bulk junction capacitance components are considered negligible.
`dta=0 K`	Temperature offset w.r.t. ambient circuit temperature.
`mvt=0.0`	DCmatch parameter.
`mbe=0.0`	DCmatch parameter.
`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.
`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.
`vgbr_max=vgb_max V`	Maximum allowed reverse voltage cross gate and bulk.
`vbsr_max=vbs_max V`	Maximum allowed reverse voltage cross source and bulk.
`vbdr_max=vbd_max V`	

© 2023 Cadence Design Systems, Inc.

	Maximum allowed reverse voltage cross source/drain and bulk.
`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
`noisemethod=oldcmi`	Induced gate noise implementation. Possible values are `oldcmi`, `subckt`, `newcmi`, and `noign`.

Output Parameters

`weff (m)`	Effective channel width for geometrical models.
`leff (m)`	Effective channel length for geometrical models.
`lv1 (m)`	Alias of l.
`lv2 (m)`	Alias of w.
`lv3 ($m^2$)`	Alias of ad.
`lv4 ($m^2$)`	Alias of as.
`lv11 (m)`	Alias of pd.
`lv12 (m)`	Alias of ps.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`dtsh (K)`	Device temperature rise due to self-heating.
`ctype`	Flag for channel type.
`sdint`	Flag for source-drain interchange.
`is (A)`	External DC current at source terminal.
`ise (A)`	Total source current.
`ig (A)`	External DC current at gate terminal.
`ige (A)`	Total gate current.
`id (A)`	External DC current at drain terminal.
`ide (A)`	Total drain current.
`ib (A)`	Total bulk current.
`ibe (A)`	Total bulk current.
`ids (A)`	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
`idb (A)`	Drain to bulk current.
`isb (A)`	Source to bulk current.
`igs (A)`	Gate-source tunneling current.
`igd (A)`	Gate-drain tunneling current.
`igb (A)`	Gate-bulk tunneling current.
`igcs (A)`	Gate-channel tunneling current (source component).
`igcd (A)`	Gate-channel tunneling current (drain component).
`iavl (A)`	Substrate current due to weak avalanche.
`igisl (A)`	Gate-induced source leakage current.
`igidl (A)`	Gate-induced drain leakage current.
`ijs (A)`	Total source junction current.
`ijsbot (A)`	Source junction current (bottom component).

© 2023 Cadence Design Systems, Inc.

ijsgat (A)	Source junction current (gate-edge component).
ijssti (A)	Source junction current (STI-edge component).
ijd (A)	Total drain junction current.
ijdbot (A)	Drain junction current (bottom component).
ijdgat (A)	Drain junction current (gate-edge component).
ijdsti (A)	Drain junction current (STI-edge component).
qg (Coul)	Intrinsic gate charge.
qd (Coul)	Intrinsic drain charge.
qb (Coul)	Intrinsic bulk charge.
qs (Coul)	Intrinsic source charge.
qgs_ov (Coul)	Overlap charge for gate-source.
qgd_ov (Coul)	Overlap charge for gate-drain.
qfgs (Coul)	Sum of outerFringe and overlap for gate-source.
qfgd (Coul)	Sum of outerFringe and overlap for gate-drain.
qgb_ov (Coul)	Gate-bulk overlap charge.
qjun_s (Coul)	Junction charge on source side.
qjun_d (Coul)	Junction charge on drain side.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vgd (V)	External gate-drain DC voltage.
vsb (V)	Source-bulk voltage.
vdb (V)	External drain-bulk DC voltage.
vth0 (V)	Zero-bias threshold voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back bias effects.
vth (V)	Threshold voltage including back bias and drain bias effects.
vth_drive (V)	Gate overdrive voltage including back-bias, drain bias effects.
vgt (V)	Effective gate drive voltage including back bias and drain bias effects.

© 2023 Cadence Design Systems, Inc.

vdss (V)	Drain saturation voltage at actual bias.
vdsat (V)	Drain saturation voltage.
vdsat_marg (V)	Saturation margin with respect to Vdsat for Drain voltage.
vsat (V)	Saturation limit.
pwr (W)	Power at op point.
gm (1/Ω)	Transconductance.
gmb (1/Ω)	Substrate transconductance.
go (1/Ω)	Output conductance.
gds (1/Ω)	Output conductance.
gjs (1/Ω)	Source junction conductance.
gjd (1/Ω)	Drain junction conductance.
cdd (F)	Drain capacitance.
cdg (F)	Drain-gate capacitance.
cds (F)	Drain-source capacitance.
cdb (F)	Drain-bulk capacitance.
cgd (F)	Gate-drain capacitance.
cgg (F)	Gate capacitance.
cgs (F)	Gate-source capacitance.
cgb (F)	Gate-bulk capacitance.
csd (F)	Source-drain capacitance.
csg (F)	Source-gate capacitance.
css (F)	Source capacitance.
csb (F)	Source-bulk capacitance.
cbd (F)	Bulk-drain capacitance.
cbg (F)	Bulk-gate capacitance.
cbs (F)	Bulk-source capacitance.
cbb (F)	Bulk capacitance.
co (F)	Output Drain-Source capacitance.
cm (F)	Capacitance element 1 for QS model.

© 2023 Cadence Design Systems, Inc.

cmb (F)	Capacitance element 2 for QS model.
cmx (F)	Capacitance element 3 for QS model.
tau1 (s)	Time constant related to NQS first frequency pole.
fqslim (Hz)	QS model frequency limit.
cgsol (F)	Total gate-source overlap capacitance.
cgdol (F)	Total gate-drain overlap capacitance.
cgbol (F)	Total gate-bulk overlap capacitance.
cjs (F)	Total source junction capacitance.
cjsbot (F)	Source junction capacitance (bottom component).
cjsgat (F)	Source junction capacitance (gate-edge component).
cjssti (F)	Source junction capacitance (STI-edge component).
cjd (F)	Total drain junction capacitance.
cjdbot (F)	Drain junction capacitance (bottom component).
cjdgat (F)	Drain junction capacitance (gate-edge component).
cjdsti (F)	Drain junction capacitance (STI-edge component).
lpoly (m)	Length of poly.
self_gain	Gm/Go ratio (MOSFET self-gain).
u	Transistor gain.
rout (Ω)	Small-signal output resistance.
vearly (V)	Equivalent Early voltage.
ft (Hz)	Unity gain frequency at actual bias.
beff (A/V^2)	Gain factor.
gmoveri (1/V)	Transconductance efficiency.
fug (Hz)	Unity gain frequency at actual bias.
rgate (Ω)	Gate resistance.
rg (Ω)	Gate resistance.
sfl (A^2/Hz)	Flicker noise current spectral density at 1 Hz.
sqrtsff (V/ Hz)	

© 2023 Cadence Design Systems, Inc.

	Input-referred RMS white noise voltage spectral density at 1 kHz.
`sqrtsfw (V/Hz)`	
	Input-referred RMS white noise voltage spectral density.
`sid (A^2/Hz)`	White noise current spectral density.
`sig (A^2/Hz)`	Induced gate noise current spectral density at 1 Hz.
`cigid`	Imaginary part of correlation coefficient between Sig and Sid.
`fknee (Hz)`	Cross-over frequency above which white noise is dominant.
`sigs (A^2/Hz)`	Gate-source current noise spectral density.
`sigd (A^2/Hz)`	Gate-drain current noise spectral density.
`siavl (A^2/Hz)`	Impact ionization current noise spectral density.
`ssi (A^2/Hz)`	Total source junction current noise spectral density.
`sdi (A^2/Hz)`	Total drain junction current noise spectral density.
`vbs (V)`	Bulk-source voltage.
`lv9 (V)`	Alias of vth.
`lv10 (V)`	Alias of vdss.
`lv36 (F)`	Alias of cgsol.
`lv37 (F)`	Alias of cgdol.
`lv38 (F)`	Alias of cgbol.
`lv51 (m)`	Alias of tox.
`lx4 (A)`	Alias of ids.
`lx3 (V)`	Alias of vds.
`lx2 (V)`	Alias of vgs.
`lx7 (1/Ω)`	Alias of gm.
`lx8 (1/Ω)`	Alias of gds.
`lx9 (1/Ω)`	Alias of gmb.
`lx33 (F)`	Alias of cdd.
`lx32 (F)`	Alias of cdg.
`lx34 (F)`	Alias of cds.

© 2023 Cadence Design Systems, Inc.

`lx19 (F)`	Alias of cgd.
`lx18 (F)`	Alias of cgg.
`lx20 (F)`	Alias of cgs.
`lx22 (F)`	Alias of cbd.
`lx21 (F)`	Alias of cbg.
`lx23 (F)`	Alias of cbs.
`lx5 (A)`	Alias of ijs.
`lx6 (A)`	Alias of ijd.
`lx28 (F)`	Alias of cjs.
`lx29 (F)`	Alias of cjd.
`lx38 (A)`	Alias of igs.
`lx39 (A)`	Alias of igd.
`lx66 (A)`	Alias of igb.
`lx67 (A)`	Alias of igcs.
`lx68 (A)`	Alias of igcd.
`lx110 (A)`	Alias of igisl.
`lx47 (A)`	Alias of igidl.
`lx60 (F)`	Alias of csd.
`lx59 (F)`	Alias of csg.
`lx58 (F)`	Alias of css.
`lx12 (Coul)`	Alias of Qb including overlap charge.
`lx14 (Coul)`	Alias of Qg including overlap charge.
`lx16 (Coul)`	Alias of Qd including overlap charge.
`lx83 (F)`	Alias of cgd including overlap cap.
`lx84 (F)`	Alias of cgs including overlap cap.
`OPdef`	1: Device Physics notation. 2: Circuit Simulator notation.
`SDop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.

© 2023 Cadence Design Systems, Inc.

Related Topics

PSP102 Model

Component Statements for PSP102 Models

PSP MOSFET Model (PSP102)

PSP MOSFET Model (psp1020)

PSP MOSFET Model (psp1021)

PSP local MOSFET Model (psp102e)

PSP NQS MOSFET Model (pspnqs1020)

PSP NQS MOSFET Model (pspnqs1021)

PSP NQS local MOSFET Model (pspnqs102e)

© 2023 Cadence Design Systems, Inc.

PSP NQS MOSFET Model (pspnqs1020)

This is SiMKit 4.0.1.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`l=10e-6 m`	Design length.
`w=10e-6 m`	Design width.
`sa=0.0 m`	Distance between OD-edge and poly from one side.
`sb=0.0 m`	Distance between OD-edge and poly from other side.
`sd=0.0 m`	Distance between neighboring fingers.
`sca=0.0`	Integral of the first distribution function for scattered well dopants.
`scb=0.0`	Integral of the second distribution function for scattered well dopants.
`scc=0.0`	Integral of the third distribution function for scattered well dopants.
`sc=0.0 m`	Distance between OD-edge and nearest well edge.
`delvto=0.0 V`	Threshold voltage shift parameter.
`factuo=1.0`	Zero-field mobility pre-factor.
`absource=1E-12 m`^{2}	Bottom area of source junction.
`lssource=1E-6 m`	STI-edge length of source junction.
`lgsource=1E-6 m`	Gate-edge length of source junction.
`abdrain=1E-12 m`^{2}	Bottom area of drain junction.

© 2023 Cadence Design Systems, Inc.

`lsdrain=1E-6 m`	STI-edge length of drain junction.
`lgdrain=1E-6 m`	Gate-edge length of drain junction.
`as=1E-12 m`^{2}	Bottom area of source junction.
`ps=1E-6 m`	Perimeter of source junction.
`ad=1E-12 m`^{2}	Bottom area of drain junction.
`pd=1E-6 m`	Perimeter of drain junction.
`mulid0=1`	Ids multiplier.
`mult=1.0`	Number of devices in parallel.
`nf=1.0`	Number of fingers.
`ngcon=1.0`	Number of gate contacts.
`xgw=1.0E-7 m`	Distance from the gate contact to the channel edge.
`region=triode`	Estimated operating region. Spectre outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trise=0.0 K`	Temperature rise from ambient.
`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Definition

```
model modelName pspnqs1020 parameter=value ...
```

Model Parameters

`level=102`	Model level.
`type=n`	Channel type parameter. Specify n for NMOS and p for PMOS. Possible values are `n` and `p`.
`tr=value of tnom C`	Nominal (reference) temperature.
`swnqs=0`	Flag for NQS. 0 means off. Numbers 1, 2, 3, 5, or 9 refer to collocation points.
`swigate=0`	Flag for gate current. 0 means turn off IG.

© 2023 Cadence Design Systems, Inc.

`swimpact=0`	Flag for impact ionization current. 0 means turn off impact ionization.
`swgidl=0`	Flag for GIDL current. 0 means turn off IGIDL.
`swjuncap=0`	Flag for juncap. 0 means turn off juncap.
`swjunasym=0`	Flag for asymmetric junctions; 0,symmetric, 1,asymmetric.
`qmc=1.0`	Quantum-mechanical correction factor.
`version=102.32`	Model parameter "version" accepts only a real number value, like 102.21 for version=102.2.1. The available versions are 102.2, 102.21(102.2.1), 102.3, 102.32(102.3.2), 102.33(102.3.3), 102.34(102.3.4), 102.4(102.4.0), and 102.5(102.5.0).
`geomod=1`	1 for geometrical model and 0 for electrical model.
`binmod=0`	1 for bin model and 0 for non-bin model.
`scalelev=102`	102 for local, 1020 for global model and 1021 for bin model.
`compatible=spectre`	Compatibility parameter. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`lvaro=0.0 m`	Geometry-independent difference between actual and programmed gate length.
`lvarl=0.0`	Length dependence of LVAR.
`lvarw=0.0`	Width dependence of LVAR.
`lap=0.0 m`	Effective channel length reduction per side.
`wvaro=0.0 m`	Geometry-independent difference between actual and programmed field-oxide opening.
`wvarl=0.0`	Length dependence of WVAR.
`wvarw=0.0`	Width dependence of WVAR.
`wot=0.0 m`	Effective channel width reduction per side.
`dlq=0.0 m`	Effective channel length reduction for CV.
`dwq=0.0 m`	Effective channel width reduction for CV.
`vfbo=(-1.0) V`	Geometry-independent flat-band voltage at TR.
`vfbl=0.0`	Length dependence of flat-band voltage.
`vfbw=0.0`	Width dependence of flat-band voltage.

© 2023 Cadence Design Systems, Inc.

`vfblw=0.0`	Area dependence of flat-band voltage.
`stvfbo=5e-4 V/K`	Geometry-independent temperature dependence of VFB.
`stvfbl=0.0`	Length dependence of temperature dependence of VFB.
`stvfbw=0.0`	Width dependence of temperature dependence of VFB.
`stvfblw=0.0`	Area dependence of temperature dependence of VFB.
`toxo=2e-9 m`	Gate oxide thickness.
`epsroxo=3.9`	Relative permittivity of gate dielectric.
`nsubo=3e23` m^{-3}	Geometry-independent substrate doping.
`nsubw=0.0`	Width dependence of background doping NSUBO due to segregation.
`wseg=1e-8 m`	Character length of segregation of background doping NSUBO.
`npck=1e24` m^{-3}	Pocket doping level.
`npckw=0.0`	Width dependence of pocket doping NPCK due to segregation.
`wsegp=1e-8 m`	Character length of segregation of pocket doping NPCK.
`lpck=1e-8 m`	Character length of lateral doping profile.
`lpckw=0.0`	Width dependence of character length of lateral doping profile.
`fol1=0.0`	First length dependence coefficient for short channel body effect.
`fol2=0.0`	Second length dependence coefficient for short channel body effect.
`vnsubo=0.0 V`	Effective doping bias-dependence parameter.
`nslpo=0.05 V`	Effective doping bias-dependence parameter.
`dnsubo=0.0 V^-1`	Effective doping bias-dependence parameter.
`dphibo=0.0 V`	Geometry-independent offset of PHIB.
`dphibl=0.0 V`	Length dependence offset of PHIB.
`dphiblexp=1.0`	Exponent for length dependence of offset of PHIB.
`dphibw=0.0`	Width dependence of offset of PHIB.
`dphiblw=0.0`	Area dependence of offset of PHIB.

© 2023 Cadence Design Systems, Inc.

`npo=1e26 m^-3`	Geometry-independent gate poly-silicon doping.
`npl=0.0`	Length dependence of gate poly-silicon doping.
`cto=0.0`	Geometry-independent interface states factor.
`ctl=0.0`	Length dependence of interface states factor.
`ctlexp=1.0`	Exponent for length dependence of interface states factor.
`ctw=0.0`	Width dependence of interface states factor.
`ctlw=0.0`	Area dependence of interface states factor.
`toxovo=2e-9 m`	Overlap oxide thickness.
`toxovdo=2e-9 m`	Overlap oxide thickness for drain side.
`lov=0 m`	Overlap length for gate/drain and gate/source overlap capacitance.
`lovd=0 m`	Overlap length for gate/drain overlap capacitance.
`novo=5e25 m^-3`	Effective doping of overlap region.
`novdo=5e25 m^-3`	Effective doping of overlap region for drain side.
`cfl=0.0`	Length dependence of DIBL-parameter.
`cflexp=2.0`	Exponent for length dependence of CF.
`cfw=0.0`	Width dependence of CF.
`cfbo=0.0 V^-1`	Back-bias dependence of CF.
`uo=5e-2 m^2/V/s`	Zero-field mobility at TR.
`fbet1=0.0`	Relative mobility decrease due to first lateral profile.
`fbet1w=0.0`	Width dependence of relative mobility decrease due to first lateral profile.
`lp1=1e-8 m`	Mobility-related characteristic length of first lateral profile.
`lp1w=0.0`	Width dependence of mobility-related characteristic length of first lateral profile.
`fbet2=0.0`	Relative mobility decrease due to second lateral profile.
`lp2=1e-8 m`	Mobility-related characteristic length of second lateral profile.
`betw1=0.0`	First higher-order width scaling coefficient of BETN.
`betw2=0.0`	Second higher-order width scaling coefficient of BETN.
`wbet=1e-9 m`	Characteristic width for width scaling of BETN.

© 2023 Cadence Design Systems, Inc.

`stbeto=1.0`	Geometry-independent temperature dependence of BETN.
`stbetl=0.0`	Length dependence of temperature dependence of BETN.
`stbetw=0.0`	Width dependence of temperature dependence of BETN.
`stbetlw=0.0`	Area dependence of temperature dependence of BETN.
`mueo=0.5 m/V`	Geometry-independent mobility reduction coefficient at TR.
`muew=0.0`	Width dependence of mobility reduction coefficient at TR.
`stmueo=0.0`	Temperature dependence of MUE.
`themuo=1.5`	Mobility reduction exponent at TR.
`stthemuo=1.5`	Temperature dependence of THEMU.
`cso=0.0`	Geometry-independent coulomb scattering parameter at TR.
`csl=0.0`	Length dependence of CS.
`cslexp=0.0`	Exponent for length dependence of CS.
`csw=0.0`	Width dependence of CS.
`cslw=0.0`	Area dependence of CS.
`stcso=0.0`	Temperature dependence of CS.
`xcoro=0.0 V^-1`	Geometry-independent non-universality parameter.
`xcorl=0.0`	Length dependence of non-universality parameter.
`xcorw=0.0`	Width dependence of non-universality parameter.
`xcorlw=0.0`	Area dependence of non-universality parameter.
`stxcoro=0.0`	Temperature dependence of XCOR.
`fetao=1.0`	Effective field parameter.
`rsw1=2.5e3 Ω`	Source/drain series resistance for 1 um wide channel at TR.
`rsw2=0.0`	Higher-order width scaling of RS.
`strso=1.0`	Temperature dependence of RS.
`rsbo=0.0 V^-1`	Back-bias dependence of series resistance.
`rsgo=0.0 V^-1`	Gate-bias dependence of series resistance.
`thesato=0.0 V^-1`	Geometry-independent velocity saturation parameter at TR.
`thesatl=0.05 V^-1`	Length dependence of THESAT.
`thesatlexp=1.0`	Exponent for length dependence of THESAT.

© 2023 Cadence Design Systems, Inc.

`thesatw=0.0`	Width dependence of velocity saturation parameter.
`thesatlw=0.0`	Area dependence of velocity saturation parameter.
`stthesato=1.0`	Geometry-independent temperature dependence of THESAT.
`stthesatl=0.0`	Length dependence of temperature dependence of THESAT.
`stthesatw=0.0`	Width dependence of temperature dependence of THESAT.
`stthesatlw=0.0`	Area dependence of temperature dependence of THESAT.
`thesatbo=0.0 V^-1`	Back-bias dependence of velocity saturation.
`thesatgo=0.0 V^-1`	Gate-bias dependence of velocity saturation.
`axo=18`	Geometry-independent linear/saturation transition factor.
`axl=0.4`	Length dependence of AX.
`alpl=5e-4`	Length dependence of ALP.
`alplexp=1.0`	Exponent for length dependence of ALP.
`alpw=0.0`	Width dependence of ALP.
`alp1l1=0.0 V`	Length dependence of CLM enhancement factor above threshold.
`alp1lexp=0.5`	Exponent for length dependence of ALP1.
`alp1l2=0.0`	Second_order length dependence of ALP1.
`alp1w=0.0`	Width dependence of ALP1.
`alp2l1=0.0 V^-1`	Length dependence of CLM enhancement factor below threshold.
`alp2lexp=0.5`	Exponent for length dependence of ALP2.
`alp2l2=0.0`	Second_order length dependence of ALP2.
`alp2w=0.0`	Width dependence of ALP2.
`vpo=0.05 V`	CLM logarithmic dependence parameter.
`a1o=1.0`	Geometry-independent impact-ionization pre-factor.
`a1l=0.0`	Length dependence of A1.
`a1w=0.0`	Width dependence of A1.
`a2o=10 V`	Impact-ionization exponent at TR.
`sta2o=0.0 V`	Temperature dependence of A2.

© 2023 Cadence Design Systems, Inc.

a3o=1.0	Geometry-independent saturation-voltage dependence of II.
a3l=0.0	Length dependence of A3.
a3w=0.0	Width dependence of A3.
a4o=0.0 V^-0.5	Geometry-independent back-bias dependence of II.
a4l=0.0	Length dependence of A4.
a4w=0.0	Width dependence of A4.
gcoo=0.0	Gate tunneling energy adjustment.
iginvlw=0.0 A	Gate channel current pre-factor for 1 um^2 channel area.
igovw=0.0 A	Gate overlap current pre-factor for 1 um wide channel.
igovdw=0.0 A	Gate overlap current pre-factor for 1 um wide channel for drain side.
stigo=2.0	Temperature dependence of IGINV and IGOV.
gc2o=0.375	Gate current slope factor.
gc3o=0.063	Gate current curvature factor.
chibo=3.1 V	Tunneling barrier height.
agidlw=0.0 A/V^3	Width dependence of GIDL pre-factor.
agidldw=0.0 A/V^3	Width dependence of GIDL pre-factor for drain side.
bgidlo=41 V	GIDL probability factor at TR.
bgidldo=41 V	GIDL probability factor at TR for drain side.
stbgidlo=0.0 V/K	Temperature dependence of BGIDL.
stbgidldo=0.0 V/K	Temperature dependence of BGIDL for drain side.
cgidlo=0.0	Back-bias dependence of GIDL.
cgidldo=0.0	Back-bias dependence of GIDL for drain side.
cgbovl=0.0 F	Oxide capacitance for gate-bulk overlap for 1 um long channel.
cfrw=0.0 F	Outer fringe capacitance for 1 um wide channel.
cfrdw=0.0 F	Outer fringe capacitance for 1 um wide channel for drain side.
fnto=1.0	Thermal noise coefficient.
fntexcl=0.0	Length dependence coefficient of excess noise.

© 2023 Cadence Design Systems, Inc.

`nfalw=8e22 V^-1/m`^{4}	
	First coefficient of flicker noise for 1 um^2 channel area.
`nfblw=3e7 V^-1/m`^{2}	
	Second coefficient of flicker noise for 1 um^2 channel area.
`nfclw=0.0 V^-1`	Third coefficient of flicker noise for 1 um^2 channel area.
`efo=1.0`	Flicker noise frequency exponent.
`lintnoi=0.0 m`	Length offset for flicker noise.
`alpnoi=2.0`	Exponent for length offset for flicker noise.
`dta=0 K`	Temperature offset w.r.t. ambient circuit temperature.
`kvthoweo=0`	Geometrical independent threshold shift parameter.
`kvthowel=0`	Length dependent threshold shift parameter.
`kvthowew=0`	Width dependent threshold shift parameter.
`kvthowelw=0`	Area dependent threshold shift parameter.
`kuoweo=0`	Geometrical independent mobility degradation factor.
`kuowel=0`	Length dependent mobility degradation factor.
`kuowew=0`	Width dependent mobility degradation factor.
`kuowelw=0`	Area dependent mobility degradation factor.
`vds_max=infinity V`	
	Maximum allowed voltage cross source and drain.
`vgd_max=infinity V`	
	Maximum allowed voltage cross gate and drain.
`vgs_max=infinity V`	
	Maximum allowed voltage cross gate and source/bulk.
`vbd_max=infinity V`	
	Maximum allowed voltage cross source/drain and bulk.
`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
`vgb_max=infinity V`	
	Maximum allowed voltage cross gate and bulk.
`vgdr_max=vgd_max V`	

© 2023 Cadence Design Systems, Inc.

	Maximum allowed reverse voltage cross gate and drain.
`vgsr_max=vgs_max V`	
	Maximum allowed reverse voltage cross gate and source.
`vgbr_max=vgb_max V`	
	Maximum allowed reverse voltage cross gate and bulk.
`vbsr_max=vbs_max V`	
	Maximum allowed reverse voltage cross source and bulk.
`vbdr_max=vbd_max V`	
	Maximum allowed reverse voltage cross source/drain and bulk.
`munqso=1.0`	Relative mobility for NQS modelling.
`rgo=0.0 Ω`	Gate resistance.
`rbulko=0.0 Ω`	Bulk resistance between node BP and BI.
`rwello=0.0 Ω`	Well resistance between node BI and B.
`rjunso=0.0 Ω`	Source-side bulk resistance between node BI and BS.
`rjundo=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
`rint=0.0 Ω/Sqr`	Contact resistance between silicide and ploy.
`rvpoly=0.0 Ω/Sqr`	
	Vertical poly resistance.
`rshg=0.0 Ω/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0.0 m`	Silicide extension over the physical gate length.
`saref=1.0e-6 m`	Reference distance between OD-edge and poly from one side.
`sbref=1.0e-6 m`	Reference distance between OD-edge and poly from other side.
`wlod=0 m`	Width parameter.
`kuo=0 m`	Mobility degradation/enhancement coefficient.
`kvsat=0 m`	Saturation velocity degradation/enhancement coefficient.
`tkuo=0`	Temperature dependence of KUO.
`lkuo=0 m^LLODKUO`	Length dependence of KUO.

© 2023 Cadence Design Systems, Inc.

`wkuo=0 m^WLODKUO`	Width dependence of KUO.
`pkuo=0 m^(LLODKUO+WLODKUO)`	Cross-term dependence of KUO.
`llodkuo=0`	Length parameter for UO stress effect.
`wlodkuo=0`	Width parameter for UO stress effect.
`kvtho=0 Vm`	Threshold shift parameter.
`lkvtho=0 m^LLODVTH`	Length dependence of KVTHO.
`wkvtho=0 m^WLODVTH`	Width dependence of KVTHO.
`pkvtho=0 m^(LLODVTH+WLODVTH)`	Cross-term dependence of KVTHO.
`llodvth=0`	Length parameter for VTH-stress effect.
`wlodvth=0`	Width parameter for VTH-stress effect.
`stetao=0 m`	eta0 shift factor related to VTHO change.
`lodetao=1.0`	eta0 shift modification factor for stress effect.
`scref=10e-6 m`	Distance between OD-edge and well edge of a reference device.
`web=0`	Coefficient for SCB.
`wec=0`	Coefficient for SCC.
`imax=1000 A`	Maximum current up to which forward current behaves exponentially.
`trj=21 C`	reference temperature.
`cjorbot=1E-3 Fm^-2`	Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.
`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.
`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.
`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
`idsatrbot=1E-12 Am^-2`	Saturation current density at the reference temperature of bottom component for source-bulk junction.
`idsatrsti=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
`idsatrgat=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
`csrhbot=1E2 Am^-3`	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
`csrhsti=1E-4 Am^-2`	

© 2023 Cadence Design Systems, Inc.

	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
csrhgat=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.
xjunsti=100E-9 m	Junction depth of STI-edge component for source-bulk junction.
xjungat=100E-9 m	Junction depth of gate-edge component for source-bulk junction.
ctatbot=1E2 Am^{-3}	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
ctatsti=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
ctatgat=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
mefftatbot=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
mefftatsti=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
mefftatgat=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
cbbtbot=1E-12 AV^{-3}	
	Band-to-band tunneling prefactor of bottom component for source-bulk junction.
cbbtsti=1E-18 $AV^{-3}m$	
	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
cbbtgat=1E-18 $AV^{-3}m$	
	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
fbbtrbot=1E9 Vm^-1	

© 2023 Cadence Design Systems, Inc.

	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.
`fbbtrsti=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
`fbbtrgat=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
`stfbbtbot=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
`stfbbtsti=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
`stfbbtgat=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
`vbrbot=10 V`	Breakdown voltage of bottom component for source-bulk junction.
`vbrsti=10 V`	Breakdown voltage of STI-edge component for source-bulk junction.
`vbrgat=10 V`	Breakdown voltage of gate-edge component for source-bulk junction.
`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component for source-bulk junction.
`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
`cjorbotd=1E-3` Fm^{-2}	
	Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`cjorstid=1E-9 Fm^-1`

Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.

`cjorgatd=1E-9 Fm^-1`

Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.

`vbirbotd=1 V` Built-in voltage at the reference temperature of bottom component for drain-bulk junction.

`vbirstid=1 V` Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.

`vbirgatd=1 V` Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.

`pbotd=0.5` Grading coefficient of bottom component for drain-bulk junction.

`pstid=0.5` Grading coefficient of STI-edge component for drain-bulk junction.

`pgatd=0.5` Grading coefficient of gate-edge component for drain-bulk junction.

`phigbotd=1.16 V` Zero-temperature bandgap voltage of bottom component for drain-bulk junction.

`phigstid=1.16 V` Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.

`phiggatd=1.16 V` Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.

`idsatrbotd=1E-12` Am^{-2}

Saturation current density at the reference temperature of bottom component for drain-bulk junction.

`idsatrstid=1E-18 Am^-1`

Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.

`idsatrgatd=1E-18 Am^-1`

Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

csrhbotd=1E2 Am^{-3}	Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.
csrhstid=1E-4 Am^{-2}	Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
csrhgatd=1E-4 Am^{-2}	Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
xjunstid=100E-9 m	Junction depth of STI-edge component for drain-bulk junction.
xjungatd=100E-9 m	Junction depth of gate-edge component for drain-bulk junction.
ctatbotd=1E2 Am^{-3}	Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
ctatstid=1E-4 Am^{-2}	Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
ctatgatd=1E-4 Am^{-2}	Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.
mefftatbotd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
mefftatstid=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.
mefftatgatd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
cbbtbotd=1E-12 AV^{-3}	Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
cbbtstid=1E-18 $AV^{-3}m$	Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`cbbtgatd=1E-18 AV-3m`

Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.

`fbbtrbotd=1E9 Vm^-1`

Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.

`fbbtrstid=1E9 Vm^-1`

Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.

`fbbtrgatd=1E9 Vm^-1`

Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.

`stfbbtbotd=(-1E-3) K^-1`

Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.

`stfbbtstid=(-1E-3) K^-1`

Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.

`stfbbtgatd=(-1E-3) K^-1`

Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.

`vbrbotd=10 V` Breakdown voltage of bottom component for drain-bulk junction.

`vbrstid=10 V` Breakdown voltage of STI-edge component for drain-bulk junction.

`vbrgatd=10 V` Breakdown voltage of gate-edge component for drain-bulk junction.

`pbrbotd=4 V` Breakdown onset tuning parameter of bottom component for drain-bulk junction.

`pbrstid=4 V` Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`pbrgatd=4 V`	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
`swjunexp=0.0`	Flag for JUNCAP express. Specify 0 for full model and 1 for express model.
`vjunref=2.5`	The maximum source-bulk junction voltage; usually about 2*VSUP.
`fjunq=0.03`	Fraction below which source-bulk junction capacitance components are considered negligible.
`vjunrefd=2.5`	The maximum drain-bulk junction voltage; usually about 2*VSUP.
`fjunqd=0.03`	Fraction below which drain-bulk junction capacitance components are considered negligible.
`mvto=0.0`	DCmatch parameter.
`mbeo=0.0`	DCmatch parameter.
`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
`noisemethod=oldcmi`	Induced gate noise implementation. Possible values are `oldcmi`, `subckt`, `newcmi`, and `noign`.

Output Parameters

`weff (m)`	Effective channel width for geometrical models.

© 2023 Cadence Design Systems, Inc.

`leff (m)`	Effective channel length for geometrical models.
`lv1 (m)`	Alias of l.
`lv2 (m)`	Alias of w.
`lv3 ($m^2$)`	Alias of ad.
`lv4 ($m^2$)`	Alias of as.
`lv11 (m)`	Alias of pd.
`lv12 (m)`	Alias of ps.

Operating-Point Parameters

`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`dtsh (K)`	Device temperature rise due to self-heating.
`ctype`	Flag for channel type.
`sdint`	Flag for source-drain interchange.
`is (A)`	External DC current at source terminal.
`ise (A)`	Total source current.
`ig (A)`	External DC current at gate terminal.
`ige (A)`	Total gate current.
`id (A)`	External DC current at drain terminal.
`ide (A)`	Total drain current.
`ib (A)`	Total bulk current.
`ibe (A)`	Total bulk current.
`ids (A)`	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
`idb (A)`	Drain to bulk current.
`isb (A)`	Source to bulk current.
`igs (A)`	Gate-source tunneling current.
`igd (A)`	Gate-drain tunneling current.

© 2023 Cadence Design Systems, Inc.

igb (A)	Gate-bulk tunneling current.
igcs (A)	Gate-channel tunneling current (source component).
igcd (A)	Gate-channel tunneling current (drain component).
iavl (A)	Substrate current due to weak avalanche.
igisl (A)	Gate-induced source leakage current.
igidl (A)	Gate-induced drain leakage current.
ijs (A)	Total source junction current.
ijsbot (A)	Source junction current (bottom component).
ijsgat (A)	Source junction current (gate-edge component).
ijssti (A)	Source junction current (STI-edge component).
ijd (A)	Total drain junction current.
ijdbot (A)	Drain junction current (bottom component).
ijdgat (A)	Drain junction current (gate-edge component).
ijdsti (A)	Drain junction current (STI-edge component).
qg (Coul)	Intrinsic gate charge.
qd (Coul)	Intrinsic drain charge.
qb (Coul)	Intrinsic bulk charge.
qs (Coul)	Intrinsic source charge.
qgs_ov (Coul)	Overlap charge for gate-source.
qgd_ov (Coul)	Overlap charge for gate-drain.
qfgs (Coul)	Sum of outerFringe and overlap for gate-source.
qfgd (Coul)	Sum of outerFringe and overlap for gate-drain.
qgb_ov (Coul)	Gate-bulk overlap charge.
qjun_s (Coul)	Junction charge on source side.
qjun_d (Coul)	Junction charge on drain side.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vgd (V)	External gate-drain DC voltage.
vsb (V)	Source-bulk voltage.

© 2023 Cadence Design Systems, Inc.

vdb (V)	External drain-bulk DC voltage.
vth0 (V)	Zero-bias threshold voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back bias effects.
vth (V)	Threshold voltage including back bias and drain bias effects.
vth_drive (V)	Gate overdrive voltage including back-bias, drain bias effects.
vgt (V)	Effective gate drive voltage including back bias and drain bias effects.
vdss (V)	Drain saturation voltage at actual bias.
vdsat (V)	Drain saturation voltage.
vdsat_marg (V)	Saturation margin with respect to Vdsat for Drain voltage.
vsat (V)	Saturation limit.
pwr (W)	Power at op point.
gm (1/Ω)	Transconductance.
gmb (1/Ω)	Substrate transconductance.
go (1/Ω)	Output conductance.
gds (1/Ω)	Output conductance.
gjs (1/Ω)	Source junction conductance.
gjd (1/Ω)	Drain junction conductance.
cdd (F)	Drain capacitance.
cdg (F)	Drain-gate capacitance.
cds (F)	Drain-source capacitance.
cdb (F)	Drain-bulk capacitance.
cgd (F)	Gate-drain capacitance.
cgg (F)	Gate capacitance.
cgs (F)	Gate-source capacitance.
cgb (F)	Gate-bulk capacitance.
csd (F)	Source-drain capacitance.
csg (F)	Source-gate capacitance.

© 2023 Cadence Design Systems, Inc.

`css (F)`	Source capacitance.
`csb (F)`	Source-bulk capacitance.
`cbd (F)`	Bulk-drain capacitance.
`cbg (F)`	Bulk-gate capacitance.
`cbs (F)`	Bulk-source capacitance.
`cbb (F)`	Bulk capacitance.
`co (F)`	Output Drain-Source capacitance.
`cm (F)`	Capacitance element 1 for QS model.
`cmb (F)`	Capacitance element 2 for QS model.
`cmx (F)`	Capacitance element 3 for QS model.
`tau1 (s)`	Time constant related to NQS first frequency pole.
`fqslim (Hz)`	QS model frequency limit.
`cgsol (F)`	Total gate-source overlap capacitance.
`cgdol (F)`	Total gate-drain overlap capacitance.
`cgbol (F)`	Total gate-bulk overlap capacitance.
`cjs (F)`	Total source junction capacitance.
`cjsbot (F)`	Source junction capacitance (bottom component).
`cjsgat (F)`	Source junction capacitance (gate-edge component).
`cjssti (F)`	Source junction capacitance (STI-edge component).
`cjd (F)`	Total drain junction capacitance.
`cjdbot (F)`	Drain junction capacitance (bottom component).
`cjdgat (F)`	Drain junction capacitance (gate-edge component).
`cjdsti (F)`	Drain junction capacitance (STI-edge component).
`lpoly (m)`	Length of poly.
`self_gain`	Gm/Go ratio (MOSFET self-gain).
`u`	Transistor gain.
`rout (Ω)`	Small-signal output resistance.
`vearly (V)`	Equivalent Early voltage.
`ft (Hz)`	Unity gain frequency at actual bias.

© 2023 Cadence Design Systems, Inc.

beff (A/V^2)	Gain factor.
gmoveri (1/V)	Transconductance efficiency.
fug (Hz)	Unity gain frequency at actual bias.
rgate (Ω)	Gate resistance.
rg (Ω)	Gate resistance.
sfl (A^2/Hz)	Flicker noise current spectral density at 1 Hz.
sqrtsff (V/$\sqrt{Hz}$)	Input-referred RMS white noise voltage spectral density at 1 kHz.
sqrtsfw (V/$\sqrt{Hz}$)	Input-referred RMS white noise voltage spectral density.
sid (A^2/Hz)	White noise current spectral density.
sig (A^2/Hz)	Induced gate noise current spectral density at 1 Hz.
cigid	Imaginary part of correlation coefficient between Sig and Sid.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
sigs (A^2/Hz)	Gate-source current noise spectral density.
sigd (A^2/Hz)	Gate-drain current noise spectral density.
siavl (A^2/Hz)	Impact ionization current noise spectral density.
ssi (A^2/Hz)	Total source junction current noise spectral density.
sdi (A^2/Hz)	Total drain junction current noise spectral density.
vbs (V)	Bulk-source voltage.
lv9 (V)	Alias of vth.
lv10 (V)	Alias of vdss.
lv36 (F)	Alias of cgsol.
lv37 (F)	Alias of cgdol.
lv38 (F)	Alias of cgbol.
lv51 (m)	Alias of tox.
lx4 (A)	Alias of ids.
lx3 (V)	Alias of vds.

© 2023 Cadence Design Systems, Inc.

lx2 (V)	Alias of vgs.
lx7 (1/Ω)	Alias of gm.
lx8 (1/Ω)	Alias of gds.
lx9 (1/Ω)	Alias of gmb.
lx33 (F)	Alias of cdd.
lx32 (F)	Alias of cdg.
lx34 (F)	Alias of cds.
lx19 (F)	Alias of cgd.
lx18 (F)	Alias of cgg.
lx20 (F)	Alias of cgs.
lx22 (F)	Alias of cbd.
lx21 (F)	Alias of cbg.
lx23 (F)	Alias of cbs.
lx5 (A)	Alias of ijs.
lx6 (A)	Alias of ijd.
lx28 (F)	Alias of cjs.
lx29 (F)	Alias of cjd.
lx38 (A)	Alias of igs.
lx39 (A)	Alias of igd.
lx66 (A)	Alias of igb.
lx67 (A)	Alias of igcs.
lx68 (A)	Alias of igcd.
lx110 (A)	Alias of igisl.
lx47 (A)	Alias of igidl.
lx60 (F)	Alias of csd.
lx59 (F)	Alias of csg.
lx58 (F)	Alias of css.
lx12 (Coul)	Alias of Qb including overlap charge.
lx14 (Coul)	Alias of Qg including overlap charge.

© 2023 Cadence Design Systems, Inc.

`lx16 (Coul)`	Alias of Qd including overlap charge.
`lx83 (F)`	Alias of cgd including overlap cap.
`lx84 (F)`	Alias of cgs including overlap cap.
`OPdef`	1: Device Physics notation. 2: Circuit Simulator notation.
`SDop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.

Related Topics

PSP102 Model

Component Statements for PSP102 Models

PSP MOSFET Model (PSP102)

PSP MOSFET Model (psp1020)

PSP local MOSFET Model (psp102e)

PSP NQS MOSFET Model (pspnqs1020)

PSP NQS MOSFET Model (pspnqs1021)

PSP NQS local MOSFET Model (pspnqs102e)

© 2023 Cadence Design Systems, Inc.

PSP NQS MOSFET Model (pspnqs1021)

This is SiMKit 4.0.1.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`l=10e-6 m`	Design length.
`w=10e-6 m`	Design width.
`sa=0.0 m`	Distance between OD-edge and poly from one side.
`sb=0.0 m`	Distance between OD-edge and poly from other side.
`sd=0.0 m`	Distance between neighboring fingers.
`sca=0.0`	Integral of the first distribution function for scattered well dopants.
`scb=0.0`	Integral of the second distribution function for scattered well dopants.
`scc=0.0`	Integral of the third distribution function for scattered well dopants.
`sc=0.0 m`	Distance between OD-edge and nearest well edge.
`delvto=0.0 V`	Threshold voltage shift parameter.
`factuo=1.0`	Zero-field mobility pre-factor.
`absource=1E-12 m`^{2}	Bottom area of source junction.
`lssource=1E-6 m`	STI-edge length of source junction.
`lgsource=1E-6 m`	Gate-edge length of source junction.
`abdrain=1E-12 m`^{2}	Bottom area of drain junction.

© 2023 Cadence Design Systems, Inc.

`lsdrain=1E-6 m`	STI-edge length of drain junction.
`lgdrain=1E-6 m`	Gate-edge length of drain junction.
`as=1E-12 m^2`	Bottom area of source junction.
`ps=1E-6 m`	Perimeter of source junction.
`ad=1E-12 m^2`	Bottom area of drain junction.
`pd=1E-6 m`	Perimeter of drain junction.
`mulid0=1`	Ids multiplier.
`mult=1.0`	Number of devices in parallel.
`nf=1.0`	Number of fingers.
`ngcon=1.0`	Number of gate contacts.
`xgw=1.0E-7 m`	Distance from the gate contact to the channel edge.
`region=triode`	Estimated operating region. Spectre outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trise=0.0 K`	Temperature rise from ambient.
`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Definition

```
model modelName pspnqs1021 parameter=value ...
```

Model Parameters

`level=102`	Model level.
`type=n`	Channel type parameter. Possible values are `n`: NMOS and `p`: PMOS.
`tr=value of tnom C`	Nominal (reference) temperature.
`swnqs=0`	Flag for NQS. 0 means off. Numbers1, 2, 3, 5, or 9 refer to collocation points.
`swigate=0`	Flag for gate current. 0 means turn off IG.

© 2023 Cadence Design Systems, Inc.

swimpact=0	Flag for impact ionization current. 0 means turn off impact ionization.
swgidl=0	Flag for GIDL current. 0 means turn off IGIDL.
swjuncap=0	Flag for juncap, 0 means turn off juncap.
swjunasym=0	Flag for asymmetric junctions. 0 means symmetric, and 1 means asymmetric.
qmc=1.0	Quantum-mechanical correction factor.
version=102.32	This parameter accepts only a real number values, for example, use 102.21 for the 102.2.1 version. The available versions are 102.2, 102.21(102.2.1), 102.3, 102.32 (102.3.2), 102.33 (102.3.3), 102.34 (102.3.4), 102.4 (102.4.0) and 102.5 (102.5.0).
geomod=1	1 for geometrical model and 0 for electrical model.
binmod=0	1 for bin model and 0 for non-bin model.
scalelev=102	102 for local, 1020 for global model and 1021 for bin model.
compatible=spectre	Compatibility parameter. Possible values are spectre, spice2, spice3, cdsspice, spiceplus, eldo, sspice, and mica.
lvaro=0.0 m	Geometry-independent difference between actual and programmed gate length.
lvarl=0.0	Length dependence of LVAR.
lap=0.0 m	Effective channel length reduction per side.
wvaro=0.0 m	Geometry-independent difference between actual and programmed field-oxide opening.
wvarw=0.0	Width dependence of WVAR.
wot=0.0 m	Effective channel width reduction per side.
dlq=0.0 m	Effective channel length reduction for CV.
dwq=0.0 m	Effective channel width reduction for CV.
povfb=(-1) V	Coefficient for the geometry-independent part of VFB.
plvfb=0.0 V	Coefficient for the length dependence of VFB.
pwvfb=0.0 V	Coefficient for the width dependence of VFB.
plwvfb=0.0 V	Coefficient for the length times width dependence of VFB.

© 2023 Cadence Design Systems, Inc.

`postvfb=0.0005 V/K`	Coefficient for the geometry-independent part of STVFB.
`plstvfb=0.0 V/K`	Coefficient for the length dependence of STVFB.
`pwstvfb=0.0 V/K`	Coefficient for the width dependence of STVFB.
`plwstvfb=0.0 V/K`	Coefficient for the length times width dependence of STVFB.
`potox=2E-09 m`	Coefficient for the geometry-independent part of TOX.
`poepsrox=3.9`	Coefficient for the geometry-independent part of EPSOX.
`poneff=5E+23 m`$^{-3}$	Coefficient for the geometry-independent part of NEFF.
`plneff=0.0 m`$^{-3}$	Coefficient for the length dependence of NEFF.
`pwneff=0.0 m`$^{-3}$	Coefficient for the width dependence of NEFF.
`plwneff=0.0 m`$^{-3}$	Coefficient for the length times width dependence of NEFF.
`povnsub=0 V`	Coefficient for the geometry-independent part of VNSUB.
`ponslp=0.05 V`	Coefficient for the geometry-independent part of NSLP.
`podnsub=0 V^-1`	Coefficient for the geometry-independent part of DNSUB.
`podphib=0 V`	Coefficient for the geometry-independent part of DPHIB.
`pldphib=0.0 V`	Coefficient for the length dependence of DPHIB.
`pwdphib=0.0 V`	Coefficient for the width dependence of DPHIB.
`plwdphib=0.0 V`	Coefficient for the length times width dependence of DPHIB.
`ponp=1E+26 m`$^{-3}$	Coefficient for the geometry-independent part of NP.
`plnp=0.0 m`$^{-3}$	Coefficient for the length dependence of NP.
`pwnp=0.0 m`$^{-3}$	Coefficient for the width dependence of NP.
`plwnp=0.0 m`$^{-3}$	Coefficient for the length times width dependence of NP.
`poct=0`	Coefficient for the geometry-independent part of CT.
`plct=0.0`	Coefficient for the length dependence of CT.
`pwct=0.0`	Coefficient for the width dependence of CT.
`plwct=0.0`	Coefficient for the length times width dependence of CT.
`potoxov=2E-09 m`	Coefficient for the geometry-independent part of TOXOV.
`potoxovd=2E-09 m`	Coefficient for the geometry-independent part of TOXOV for drain side.

© 2023 Cadence Design Systems, Inc.

ponov=5E+25 m^{-3}	Coefficient for the geometry-independent part of NOV.
plnov=0.0 m^{-3}	Coefficient for the length dependence of NOV.
pwnov=0.0 m^{-3}	Coefficient for the width dependence of NOV.
plwnov=0.0 m^{-3}	Coefficient for the length times width dependence of NOV.
ponovd=5E+25 m^{-3}	Coefficient for the geometry-independent part of NOV for drain side.
plnovd=0.0 m^{-3}	Coefficient for the length dependence of NOV for drain side.
pwnovd=0.0 m^{-3}	Coefficient for the width dependence of NOV for drain side.
plwnovd=0.0 m^{-3}	Coefficient for the length times width dependence of NOV for drain side.
pocf=0	Coefficient for the geometry-independent part of CF.
plcf=0.0	Coefficient for the length dependence of CF.
pwcf=0.0	Coefficient for the width dependence of CF.
plwcf=0.0	Coefficient for the length times width dependence of CF.
pocfb=0 V^-1	Coefficient for the geometry-independent part of CFB.
pobetn=0.07 $m^2/V/s$	Coefficient for the geometry-independent part of BETN.
plbetn=0.0 $m^2/V/s$	Coefficient for the length dependence of BETN.
pwbetn=0.0 $m^2/V/s$	Coefficient for the width dependence of BETN.
plwbetn=0.0 $m^2/V/s$	Coefficient for the length times width dependence of BETN.
postbet=1	Coefficient for the geometry-independent part of STBET.
plstbet=0.0	Coefficient for the length dependence of STBET.
pwstbet=0.0	Coefficient for the width dependence of STBET.
plwstbet=0.0	Coefficient for the length times width dependence of STBET.
pomue=0.5 m/V	Coefficient for the geometry-independent part of MUE.
plmue=0.0 m/V	Coefficient for the length dependence of MUE.

© 2023 Cadence Design Systems, Inc.

`pwmue=0.0 m/V`	Coefficient for the width dependence of MUE.
`plwmue=0.0 m/V`	Coefficient for the length times width dependence of MUE.
`postmue=0`	Coefficient for the geometry-independent part of STMUE.
`pothemu=1.5`	Coefficient for the geometry-independent part of THEMU.
`postthemu=1.5`	Coefficient for the geometry-independent part of STTHEMU.
`pocs=0`	Coefficient for the geometry-independent part of CS.
`plcs=0.0`	Coefficient for the length dependence of CS.
`pwcs=0.0`	Coefficient for the width dependence of CS.
`plwcs=0.0`	Coefficient for the length times width dependence of CS.
`postcs=0`	Coefficient for the geometry-independent part of STCS.
`poxcor=0 V^-1`	Coefficient for the geometry-independent part of XCOR.
`plxcor=0.0 V^-1`	Coefficient for the length dependence of XCOR.
`pwxcor=0.0 V^-1`	Coefficient for the width dependence of XCOR.
`plwxcor=0.0 V^-1`	Coefficient for the length times width dependence of XCOR.
`postxcor=0`	Coefficient for the geometry-independent part of STXCOR.
`pofeta=1`	Coefficient for the geometry-independent part of FETA.
`pors=30 Ω`	Coefficient for the geometry-independent part of RS.
`plrs=0.0 Ω`	Coefficient for the length dependence of RS.
`pwrs=0.0 Ω`	Coefficient for the width dependence of RS.
`plwrs=0.0 Ω`	Coefficient for the length times width dependence of RS.
`postrs=1`	Coefficient for the geometry-independent part of STRS.
`porsb=0 V^-1`	Coefficient for the geometry-independent part of RSB.
`porsg=0 V^-1`	Coefficient for the geometry-independent part of RSG.
`pothesat=1 V^-1`	Coefficient for the geometry-independent part of THESAT.
`plthesat=0.0 V^-1`	Coefficient for the length dependence of THESAT.
`pwthesat=0.0 V^-1`	Coefficient for the width dependence of THESAT.
`plwthesat=0.0 V^-1`	Coefficient for the length times width dependence of THESAT.
`postthesat=1`	Coefficient for the geometry-independent part of STTHESAT.

© 2023 Cadence Design Systems, Inc.

`plstthesat=0.0`	Coefficient for the length dependence of STTHESAT.
`pwstthesat=0.0`	Coefficient for the width dependence of STTHESAT.
`plwstthesat=0.0`	Coefficient for the length times width dependence of STTHESAT.
`pothesatb=0 V^-1`	Coefficient for the geometry-independent part of THESATB.
`plthesatb=0.0 V^-1`	Coefficient for the length dependence of THESATB.
`pwthesatb=0.0 V^-1`	Coefficient for the width dependence of THESATB.
`plwthesatb=0.0 V^-1`	Coefficient for the length times width dependence of THESATB.
`pothesatg=0 V^-1`	Coefficient for the geometry-independent part of THESATG.
`plthesatg=0.0 V^-1`	Coefficient for the length dependence of THESATG.
`pwthesatg=0.0 V^-1`	Coefficient for the width dependence of THESATG.
`plwthesatg=0.0 V^-1`	Coefficient for the length times width dependence of THESATG.
`poax=3`	Coefficient for the geometry-independent part of AX.
`plax=0.0`	Coefficient for the length dependence of AX.
`pwax=0.0`	Coefficient for the width dependence of AX.
`plwax=0.0`	Coefficient for the length times width dependence of AX.
`poalp=0.01`	Coefficient for the geometry-independent part of ALP.
`plalp=0.0`	Coefficient for the length dependence of ALP.
`pwalp=0.0`	Coefficient for the width dependence of ALP.
`plwalp=0.0`	Coefficient for the length times width dependence of ALP.
`poalp1=0 V`	Coefficient for the geometry-independent part of ALP1.
`plalp1=0.0 V`	Coefficient for the length dependence of ALP1.

© 2023 Cadence Design Systems, Inc.

pwalp1=0.0 V	Coefficient for the width dependence of ALP1.
plwalp1=0.0 V	Coefficient for the length times width dependence of ALP1.
poalp2=0 V^-1	Coefficient for the geometry-independent part of ALP2.
plalp2=0.0 V^-1	Coefficient for the length dependence of ALP2.
pwalp2=0.0 V^-1	Coefficient for the width dependence of ALP2.
plwalp2=0.0 V^-1	Coefficient for the length times width dependence of ALP2.
povp=0.05 V	Coefficient for the geometry-independent part of VP.
poa1=1	Coefficient for the geometry-independent part of A1.
pla1=0.0	Coefficient for the length dependence of A1.
pwa1=0.0	Coefficient for the width dependence of A1.
plwa1=0.0	Coefficient for the length times width dependence of A1.
poa2=10 V	Coefficient for the geometry-independent part of A2.
posta2=0 V	Coefficient for the geometry-independent part of STA2.
poa3=1	Coefficient for the geometry-independent part of A3.
pla3=0.0	Coefficient for the length dependence of A3.
pwa3=0.0	Coefficient for the width dependence of A3.
plwa3=0.0	Coefficient for the length times width dependence of A3.
poa4=0 V^-0.5	Coefficient for the geometry-independent part of A4.
pla4=0.0 V^-0.5	Coefficient for the length dependence of A4.
pwa4=0.0 V^-0.5	Coefficient for the width dependence of A4.
plwa4=0.0 V^-0.5	Coefficient for the length times width dependence of A4.
pogco=0	Coefficient for the geometry-independent part of GCO.
poiginv=0 A	Coefficient for the geometry-independent part of IGINV.
pliginv=0.0 A	Coefficient for the length dependence of IGINV.
pwiginv=0.0 A	Coefficient for the width dependence of IGINV.
plwiginv=0.0 A	Coefficient for the length times width dependence of IGINV.
poigov=0 A	Coefficient for the geometry-independent part of IGOV.
pligov=0.0 A	Coefficient for the length dependence of IGOV.
pwigov=0.0 A	Coefficient for the width dependence of IGOV.

© 2023 Cadence Design Systems, Inc.

`plwigov=0.0 A`	Coefficient for the length times width dependence of IGOV.
`poigovd=0 A`	Coefficient for the geometry-independent part of IGOV for drain side.
`pligovd=0.0 A`	Coefficient for the length dependence of IGOV for drain side.
`pwigovd=0.0 A`	Coefficient for the width dependence of IGOV for drain side.
`plwigovd=0.0 A`	Coefficient for the length times width dependence of IGOV for drain side.
`postig=2`	Coefficient for the geometry-independent part of STIG.
`pogc2=0.375`	Coefficient for the geometry-independent part of GC2.
`pogc3=0.063`	Coefficient for the geometry-independent part of GC3.
`pochib=3.1 V`	Coefficient for the geometry-independent part of CHIB.
`poagidl=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL.
`plagidl=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL.
`pwagidl=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL.
`plwagidl=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL.
`poagidld=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL for drain side.
`plagidld=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL for drain side.
`pwagidld=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL for drain side.
`plwagidld=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL for drain side.
`pobgidl=41 V`	Coefficient for the geometry-independent part of BGIDL.
`pobgidld=41 V`	Coefficient for the geometry-independent part of BGIDL for drain side.
`postbgidl=0 V/K`	Coefficient for the geometry-independent part of STBGIDL.
`postbgidld=0 V/K`	Coefficient for the geometry-independent part of STBGIDL for drain side.

© 2023 Cadence Design Systems, Inc.

`pocgidl=0`	Coefficient for the geometry-independent part of CGIDL.
`pocgidld=0`	Coefficient for the geometry-independent part of CGIDL for drain side.
`pocox=1E-14 F`	Coefficient for the geometry-independent part of COX.
`plcox=0.0 F`	Coefficient for the length dependence of COX.
`pwcox=0.0 F`	Coefficient for the width dependence of COX.
`plwcox=0.0 F`	Coefficient for the length times width dependence of COX.
`pocgov=1E-15 F`	Coefficient for the geometry-independent part of CGOV.
`plcgov=0.0 F`	Coefficient for the length dependence of CGOV.
`pwcgov=0.0 F`	Coefficient for the width dependence of CGOV.
`plwcgov=0.0 F`	Coefficient for the length times width dependence of CGOV.
`pocgovd=1E-15 F`	Coefficient for the geometry-independent part of CGOV for drain side.
`plcgovd=0.0 F`	Coefficient for the length dependence of CGOV for drain side.
`pwcgovd=0.0 F`	Coefficient for the width dependence of CGOV for drain side.
`plwcgovd=0.0 F`	Coefficient for the length times width dependence of CGOV for drain side.
`pocgbov=0 F`	Coefficient for the geometry-independent part of CGBOV.
`plcgbov=0.0 F`	Coefficient for the length dependence of CGBOV.
`pwcgbov=0.0 F`	Coefficient for the width dependence of CGBOV.
`plwcgbov=0.0 F`	Coefficient for the length times width dependence of CGBOV.
`pocfr=0 F`	Coefficient for the geometry-independent part of CFR.
`plcfr=0.0 F`	Coefficient for the length dependence of CFR.
`pwcfr=0.0 F`	Coefficient for the width dependence of CFR.
`plwcfr=0.0 F`	Coefficient for the length times width dependence of CFR.
`pocfrd=0 F`	Coefficient for the geometry-independent part of CFR for drain side.
`plcfrd=0.0 F`	Coefficient for the length dependence of CFR for drain side.
`pwcfrd=0.0 F`	Coefficient for the width dependence of CFR for drain side.

© 2023 Cadence Design Systems, Inc.

`plwcfrd=0.0 F`	Coefficient for the length times width dependence of CFR for drain side.
`pofnt=1`	Coefficient for the geometry-independent part of FNT.
`pofntexc=0.0`	Coefficient for the geometry-independent part of FNTEXC.
`plfntexc=0.0`	Coefficient for the length dependence of FNTEXC.
`pwfntexc=0.0`	Coefficient for the width dependence of FNTEXC.
`plwfntexc=0.0`	Coefficient for the length times width dependence of FNTEXC.
`ponfa=8E+22 V^-1/m`^{4}	Coefficient for the geometry-independent part of NFA.
`plnfa=0.0 V^-1/m`^{4}	Coefficient for the length dependence of NFA.
`pwnfa=0.0 V^-1/m`^{4}	Coefficient for the width dependence of NFA.
`plwnfa=0.0 V^-1/m`^{4}	Coefficient for the length times width dependence of NFA.
`ponfb=3E+07 V^-1/m`^{2}	Coefficient for the geometry-independent part of NFB.
`plnfb=0.0 V^-1/m`^{2}	Coefficient for the length dependence of NFB.
`pwnfb=0.0 V^-1/m`^{2}	Coefficient for the width dependence of NFB.
`plwnfb=0.0 V^-1/m`^{2}	Coefficient for the length times width dependence of NFB.
`ponfc=0 V^-1`	Coefficient for the geometry-independent part of NFC.
`plnfc=0.0 V^-1`	Coefficient for the length dependence of NFC.
`pwnfc=0.0 V^-1`	Coefficient for the width dependence of NFC.
`plwnfc=0.0 V^-1`	Coefficient for the length times width dependence of NFC.
`poef=1.0`	Coefficient for the flicker noise frequency exponent.
`dta=0 K`	Temperature offset w.r.t. ambient circuit temperature.

© 2023 Cadence Design Systems, Inc.

`pokvthowe=0`	Coefficient for the geometry-independent part of KVTHOWE.
`plkvthowe=0`	Coefficient for the length dependence part of KVTHOWE.
`pwkvthowe=0`	Coefficient for the width dependence part of KVTHOWE.
`plwkvthowe=0`	Coefficient for the length times width dependence part of KVTHOWE.
`pokuowe=0`	Coefficient for the geometry-independent part of KUOWE.
`plkuowe=0`	Coefficient for the length dependence part of KUOWE.
`pwkuowe=0`	Coefficient for the width dependence part of KUOWE.
`plwkuowe=0`	Coefficient for the length times width dependence part of KUOWE.
`lmin=0 m`	Dummy parameter to label binning set.
`lmax=1.0 m`	Dummy parameter to label binning set.
`wmin=0 m`	Dummy parameter to label binning set.
`wmax=1.0 m`	Dummy parameter to label binning set.
`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.
`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.

© 2023 Cadence Design Systems, Inc.

`vgbr_max=vgb_max V`	
	Maximum allowed reverse voltage cross gate and bulk.
`vbsr_max=vbs_max V`	
	Maximum allowed reverse voltage cross source and bulk.
`vbdr_max=vbd_max V`	
	Maximum allowed reverse voltage cross source/drain and bulk.
`munqso=1.0`	Relative mobility for NQS modelling.
`rgo=0.0 Ω`	Gate resistance.
`rbulko=0.0 Ω`	Bulk resistance between node BP and BI.
`rwello=0.0 Ω`	Well resistance between node BI and B.
`rjunso=0.0 Ω`	Source-side bulk resistance between node BI and BS.
`rjundo=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
`rint=0.0 Ω/Sqr`	Contact resistance between silicide and ploy.
`rvpoly=0.0 Ω/Sqr`	
	Vertical poly resistance.
`rshg=0.0 Ω/Sqr`	Gate electrode diffusion sheet resistance.
`dlsil=0.0 m`	Silicide extension over the physical gate length.
`saref=1.0e-6 m`	Reference distance between OD-edge and poly from one side.
`sbref=1.0e-6 m`	Reference distance between OD-edge and poly from other side.
`wlod=0 m`	Width parameter.
`kuo=0 m`	Mobility degradation/enhancement coefficient.
`kvsat=0 m`	Saturation velocity degradation/enhancement coefficient.
`tkuo=0`	Temperature dependence of KUO.
`lkuo=0 m^LLODKUO`	Length dependence of KUO.
`wkuo=0 m^WLODKUO`	Width dependence of KUO.
`pkuo=0 m^(LLODKUO+WLODKUO)`	
	Cross-term dependence of KUO.

© 2023 Cadence Design Systems, Inc.

`llodkuo=0`	Length parameter for UO stress effect.
`wlodkuo=0`	Width parameter for UO stress effect.
`kvtho=0 Vm`	Threshold shift parameter.
`lkvtho=0 m^LLODVTH`	Length dependence of KVTHO.
`wkvtho=0 m^WLODVTH`	Width dependence of KVTHO.
`pkvtho=0 m^(LLODVTH+WLODVTH)`	Cross-term dependence of KVTHO.
`llodvth=0`	Length parameter for VTH-stress effect.
`wlodvth=0`	Width parameter for VTH-stress effect.
`stetao=0 m`	eta0 shift factor related to VTHO change.
`lodetao=1.0`	eta0 shift modification factor for stress effect.
`scref=10e-6 m`	Distance between OD-edge and well edge of a reference device.
`web=0`	Coefficient for SCB.
`wec=0`	Coefficient for SCC.
`imax=1000 A`	Maximum current up to which forward current behaves exponentially.
`trj=21 C`	reference temperature.
`cjorbot=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.
`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.
`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.
`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
`idsatrbot=1E-12 Am`$^{-2}$	Saturation current density at the reference temperature of bottom component for source-bulk junction.
`idsatrsti=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
`idsatrgat=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
`csrhbot=1E2 Am`$^{-3}$	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
`csrhsti=1E-4 Am`$^{-2}$	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
`csrhgat=1E-4 Am`$^{-2}$	

© 2023 Cadence Design Systems, Inc.

	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.
`xjunsti=100E-9 m`	Junction depth of STI-edge component for source-bulk junction.
`xjungat=100E-9 m`	Junction depth of gate-edge component for source-bulk junction.
`ctatbot=1E2 Am^-3`	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
`ctatsti=1E-4 Am^-2`	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
`ctatgat=1E-4 Am^-2`	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
`mefftatbot=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
`mefftatsti=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
`mefftatgat=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
`cbbtbot=1E-12 AV^-3`	Band-to-band tunneling prefactor of bottom component for source-bulk junction.
`cbbtsti=1E-18 AV^-3m`	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
`cbbtgat=1E-18 AV^-3m`	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
`fbbtrbot=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.
`fbbtrsti=1E9 Vm^-1`	

© 2023 Cadence Design Systems, Inc.

	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
`fbbtrgat=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
`stfbbtbot=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
`stfbbtsti=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
`stfbbtgat=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
`vbrbot=10 V`	Breakdown voltage of bottom component for source-bulk junction.
`vbrsti=10 V`	Breakdown voltage of STI-edge component for source-bulk junction.
`vbrgat=10 V`	Breakdown voltage of gate-edge component for source-bulk junction.
`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component for source-bulk junction.
`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
`cjorbotd=1E-3 Fm`$^{-2}$	
	Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`cjorstid=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.
`cjorgatd=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.
`vbirbotd=1 V`	Built-in voltage at the reference temperature of bottom component for drain-bulk junction.
`vbirstid=1 V`	Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.
`vbirgatd=1 V`	Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.
`pbotd=0.5`	Grading coefficient of bottom component for drain-bulk junction.
`pstid=0.5`	Grading coefficient of STI-edge component for drain-bulk junction.
`pgatd=0.5`	Grading coefficient of gate-edge component for drain-bulk junction.
`phigbotd=1.16 V`	Zero-temperature bandgap voltage of bottom component for drain-bulk junction.
`phigstid=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.
`phiggatd=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.
`idsatrbotd=1E-12 Am`$^{-2}$	Saturation current density at the reference temperature of bottom component for drain-bulk junction.
`idsatrstid=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.
`idsatrgatd=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

csrhbotd=1E2 Am^{-3}	
	Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.
csrhstid=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
csrhgatd=1E-4 Am^{-2}	
	Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
xjunstid=100E-9 m	Junction depth of STI-edge component for drain-bulk junction.
xjungatd=100E-9 m	Junction depth of gate-edge component for drain-bulk junction.
ctatbotd=1E2 Am^{-3}	
	Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
ctatstid=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
ctatgatd=1E-4 Am^{-2}	
	Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.
mefftatbotd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
mefftatstid=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.
mefftatgatd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
cbbtbotd=1E-12 AV^{-3}	
	Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
cbbtstid=1E-18 $AV^{-3}m$	
	Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`cbbtgatd=1E-18 AV-3m`

Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.

`fbbtrbotd=1E9 Vm^-1`

Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.

`fbbtrstid=1E9 Vm^-1`

Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.

`fbbtrgatd=1E9 Vm^-1`

Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.

`stfbbtbotd=(-1E-3) K^-1`

Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.

`stfbbtstid=(-1E-3) K^-1`

Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.

`stfbbtgatd=(-1E-3) K^-1`

Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.

`vbrbotd=10 V` Breakdown voltage of bottom component for drain-bulk junction.

`vbrstid=10 V` Breakdown voltage of STI-edge component for drain-bulk junction.

`vbrgatd=10 V` Breakdown voltage of gate-edge component for drain-bulk junction.

`pbrbotd=4 V` Breakdown onset tuning parameter of bottom component for drain-bulk junction.

`pbrstid=4 V` Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`pbrgatd=4 V`	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
`swjunexp=0.0`	Flag for JUNCAP express. Specify 0 for full model and 1 for express model.
`vjunref=2.5`	The maximum source-bulk junction voltage; usually about 2*VSUP.
`fjunq=0.03`	Fraction below which source-bulk junction capacitance components are considered negligible.
`vjunrefd=2.5`	The maximum drain-bulk junction voltage; usually about 2*VSUP.
`fjunqd=0.03`	Fraction below which drain-bulk junction capacitance components are considered negligible.
`mvto=0.0`	DCmatch parameter.
`mbeo=0.0`	DCmatch parameter.
`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
`noisemethod=oldcmi`	Induced gate noise implementation. Possible values are `oldcmi`, `subckt`, `newcmi`, and `noign`.

Output Parameters

`weff (m)`	Effective channel width for geometrical models.

© 2023 Cadence Design Systems, Inc.

`leff (m)`	Effective channel length for geometrical models.
`lv1 (m)`	Alias of l.
`lv2 (m)`	Alias of w.
`lv3 ($m^2$)`	Alias of ad.
`lv4 ($m^2$)`	Alias of as.
`lv11 (m)`	Alias of pd.
`lv12 (m)`	Alias of ps.

Operating-Point Parameters

`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`dtsh (K)`	Device temperature rise due to self-heating.
`ctype`	Flag for channel type.
`sdint`	Flag for source-drain interchange.
`is (A)`	External DC current at source terminal.
`ise (A)`	Total source current.
`ig (A)`	External DC current at gate terminal.
`ige (A)`	Total gate current.
`id (A)`	External DC current at drain terminal.
`ide (A)`	Total drain current.
`ib (A)`	Total bulk current.
`ibe (A)`	Total bulk current.
`ids (A)`	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
`idb (A)`	Drain to bulk current.
`isb (A)`	Source to bulk current.
`igs (A)`	Gate-source tunneling current.
`igd (A)`	Gate-drain tunneling current.

© 2023 Cadence Design Systems, Inc.

igb (A)	Gate-bulk tunneling current.
igcs (A)	Gate-channel tunneling current (source component).
igcd (A)	Gate-channel tunneling current (drain component).
iavl (A)	Substrate current due to weak avalanche.
igisl (A)	Gate-induced source leakage current.
igidl (A)	Gate-induced drain leakage current.
ijs (A)	Total source junction current.
ijsbot (A)	Source junction current (bottom component).
ijsgat (A)	Source junction current (gate-edge component).
ijssti (A)	Source junction current (STI-edge component).
ijd (A)	Total drain junction current.
ijdbot (A)	Drain junction current (bottom component).
ijdgat (A)	Drain junction current (gate-edge component).
ijdsti (A)	Drain junction current (STI-edge component).
qg (Coul)	Intrinsic gate charge.
qd (Coul)	Intrinsic drain charge.
qb (Coul)	Intrinsic bulk charge.
qs (Coul)	Intrinsic source charge.
qgs_ov (Coul)	Overlap charge for gate-source.
qgd_ov (Coul)	Overlap charge for gate-drain.
qfgs (Coul)	Sum of outerFringe and overlap for gate-source.
qfgd (Coul)	Sum of outerFringe and overlap for gate-drain.
qgb_ov (Coul)	Gate-bulk overlap charge.
qjun_s (Coul)	Junction charge on source side.
qjun_d (Coul)	Junction charge on drain side.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vgd (V)	External gate-drain DC voltage.
vsb (V)	Source-bulk voltage.

© 2023 Cadence Design Systems, Inc.

vdb (V)	External drain-bulk DC voltage.
vth0 (V)	Zero-bias threshold voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back bias effects.
vth (V)	Threshold voltage including back bias and drain bias effects.
vth_drive (V)	Gate overdrive voltage including back-bias, drain bias effects.
vgt (V)	Effective gate drive voltage including back bias and drain bias effects.
vdss (V)	Drain saturation voltage at actual bias.
vdsat (V)	Drain saturation voltage.
vdsat_marg (V)	Saturation margin with respect to Vdsat for Drain voltage.
vsat (V)	Saturation limit.
pwr (W)	Power at op point.
gm (1/Ω)	Transconductance.
gmb (1/Ω)	Substrate transconductance.
go (1/Ω)	Output conductance.
gds (1/Ω)	Output conductance.
gjs (1/Ω)	Source junction conductance.
gjd (1/Ω)	Drain junction conductance.
cdd (F)	Drain capacitance.
cdg (F)	Drain-gate capacitance.
cds (F)	Drain-source capacitance.
cdb (F)	Drain-bulk capacitance.
cgd (F)	Gate-drain capacitance.
cgg (F)	Gate capacitance.
cgs (F)	Gate-source capacitance.
cgb (F)	Gate-bulk capacitance.
csd (F)	Source-drain capacitance.
csg (F)	Source-gate capacitance.

© 2023 Cadence Design Systems, Inc.

`css (F)`	Source capacitance.
`csb (F)`	Source-bulk capacitance.
`cbd (F)`	Bulk-drain capacitance.
`cbg (F)`	Bulk-gate capacitance.
`cbs (F)`	Bulk-source capacitance.
`cbb (F)`	Bulk capacitance.
`co (F)`	Output Drain-Source capacitance.
`cm (F)`	Capacitance element 1 for QS model.
`cmb (F)`	Capacitance element 2 for QS model.
`cmx (F)`	Capacitance element 3 for QS model.
`tau1 (s)`	Time constant related to NQS first frequency pole.
`fqslim (Hz)`	QS model frequency limit.
`cgsol (F)`	Total gate-source overlap capacitance.
`cgdol (F)`	Total gate-drain overlap capacitance.
`cgbol (F)`	Total gate-bulk overlap capacitance.
`cjs (F)`	Total source junction capacitance.
`cjsbot (F)`	Source junction capacitance (bottom component).
`cjsgat (F)`	Source junction capacitance (gate-edge component).
`cjssti (F)`	Source junction capacitance (STI-edge component).
`cjd (F)`	Total drain junction capacitance.
`cjdbot (F)`	Drain junction capacitance (bottom component).
`cjdgat (F)`	Drain junction capacitance (gate-edge component).
`cjdsti (F)`	Drain junction capacitance (STI-edge component).
`lpoly (m)`	Length of poly.
`self_gain`	Gm/Go ratio (MOSFET self-gain).
`u`	Transistor gain.
`rout (Ω)`	Small-signal output resistance.
`vearly (V)`	Equivalent Early voltage.
`ft (Hz)`	Unity gain frequency at actual bias.

© 2023 Cadence Design Systems, Inc.

beff (A/V^2)	Gain factor.
gmoveri (1/V)	Transconductance efficiency.
fug (Hz)	Unity gain frequency at actual bias.
rgate (Ω)	Gate resistance.
rg (Ω)	Gate resistance.
sfl (A^2/Hz)	Flicker noise current spectral density at 1 Hz.
sqrtsff (V/$\sqrt{}$Hz)	Input-referred RMS white noise voltage spectral density at 1 kHz.
sqrtsfw (V/$\sqrt{}$Hz)	Input-referred RMS white noise voltage spectral density.
sid (A^2/Hz)	White noise current spectral density.
sig (A^2/Hz)	Induced gate noise current spectral density at 1 Hz.
cigid	Imaginary part of correlation coefficient between Sig and Sid.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
sigs (A^2/Hz)	Gate-source current noise spectral density.
sigd (A^2/Hz)	Gate-drain current noise spectral density.
siavl (A^2/Hz)	Impact ionization current noise spectral density.
ssi (A^2/Hz)	Total source junction current noise spectral density.
sdi (A^2/Hz)	Total drain junction current noise spectral density.
vbs (V)	Bulk-source voltage.
lv9 (V)	Alias of vth.
lv10 (V)	Alias of vdss.
lv36 (F)	Alias of cgsol.
lv37 (F)	Alias of cgdol.
lv38 (F)	Alias of cgbol.
lv51 (m)	Alias of tox.
lx4 (A)	Alias of ids.
lx3 (V)	Alias of vds.

© 2023 Cadence Design Systems, Inc.

lx2 (V)	Alias of vgs.
lx7 (1/Ω)	Alias of gm.
lx8 (1/Ω)	Alias of gds.
lx9 (1/Ω)	Alias of gmb.
lx33 (F)	Alias of cdd.
lx32 (F)	Alias of cdg.
lx34 (F)	Alias of cds.
lx19 (F)	Alias of cgd.
lx18 (F)	Alias of cgg.
lx20 (F)	Alias of cgs.
lx22 (F)	Alias of cbd.
lx21 (F)	Alias of cbg.
lx23 (F)	Alias of cbs.
lx5 (A)	Alias of ijs.
lx6 (A)	Alias of ijd.
lx28 (F)	Alias of cjs.
lx29 (F)	Alias of cjd.
lx38 (A)	Alias of igs.
lx39 (A)	Alias of igd.
lx66 (A)	Alias of igb.
lx67 (A)	Alias of igcs.
lx68 (A)	Alias of igcd.
lx110 (A)	Alias of igisl.
lx47 (A)	Alias of igidl.
lx60 (F)	Alias of csd.
lx59 (F)	Alias of csg.
lx58 (F)	Alias of css.
lx12 (Coul)	Alias of Qb including overlap charge.
lx14 (Coul)	Alias of Qg including overlap charge.

© 2023 Cadence Design Systems, Inc.

`lx16 (Coul)`	Alias of Qd including overlap charge.
`lx83 (F)`	Alias of cgd including overlap cap.
`lx84 (F)`	Alias of cgs including overlap cap.
`OPdef`	1: Device Physics notation. 2: Circuit Simulator notation.
`SDop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.

Related Topics

PSP102 Model

Component Statements for PSP102 Models

PSP MOSFET Model (PSP102)

PSP MOSFET Model (psp1020)

PSP MOSFET Model (psp1021)

PSP local MOSFET Model (psp102e)

PSP NQS MOSFET Model (pspnqs1020)

PSP NQS local MOSFET Model (pspnqs102e)

© 2023 Cadence Design Systems, Inc.

PSP NQS local MOSFET Model (pspnqs102e)

This is SiMKit 4.0.1.

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

`delvto=0.0 V`	Threshold voltage shift parameter.
`factuo=1.0`	Zero-field mobility pre-factor.
`absource=1E-12 m`^{2}	Bottom area of source junction.
`lssource=1E-6 m`	STI-edge length of source junction.
`lgsource=1E-6 m`	Gate-edge length of source junction.
`abdrain=1E-12 m`^{2}	Bottom area of drain junction.
`lsdrain=1E-6 m`	STI-edge length of drain junction.
`lgdrain=1E-6 m`	Gate-edge length of drain junction.
`as=1E-12 m`^{2}	Bottom area of source junction.
`ps=1E-6 m`	Perimeter of source junction.
`ad=1E-12 m`^{2}	Bottom area of drain junction.
`pd=1E-6 m`	Perimeter of drain junction.
`mulid0=1`	Ids multiplier.
`jw=1E-6 m`	Gate-edge length of source/drain junction.
`mult=1.0`	Number of devices in parallel.
`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.

© 2023 Cadence Design Systems, Inc.

`trise=0.0 K`	Temperature rise from ambient.
`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Definition

```
model modelName pspnqs102e parameter=value ...
```

Model Parameters

`level=102`	Model level.
`type=n`	Channel type parameter. Specify n for NMOS and p for PMOS. Possible values are `n` and `p`.
`tr=value of tnom C`	Nominal (reference) temperature.
`swnqs=0`	Flag for NQS. 0 means off. Numbers 1, 2, 3, 5, or 9 refer to collocation points.
`swigate=0`	Flag for gate current. 0 means turn off IG.
`swimpact=0`	Flag for impact ionization current. 0 means turn off impact ionization.
`swgidl=0`	Flag for GIDL current. 0 means turn off IGIDL.
`swjuncap=0`	Flag for juncap. 0 means turn off juncap.
`swjunasym=0`	Flag for asymmetric junctions. 0 means symmetric, and 1 means asymmetric.
`qmc=1.0`	Quantum-mechanical correction factor.
`version=102.32`	Model parameter "version" accepts only real number value, like 102.21 for version=102.2.1. The available versions are 102.2, 102.21(102.2.1), 102.3, 102.32(102.3.2), 102.33(102.3.3), 102.34(102.3.4), 102.4(102.4.0), and 102.5(102.5.0).
`geomod=1`	1 for geometrical model and 0 for electrical model.
`binmod=0`	1 for bin model and 0 for non-bin model.
`scalelev=102`	102 for local, 1020 for global model and 1021 for bin model.

© 2023 Cadence Design Systems, Inc.

`compatible=spectre`	Compatibility parameter. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`vfb=(-1.0) V`	Flatband voltage at TR.
`stvfb=5.0e-4 V/K`	Temperature dependence of VFB.
`tox=2.0e-09 m`	Gate oxide thickness.
`epsrox=3.9`	Relative permittivity of gate dielectric.
`neff=5.0e+23` m^{-3}	Effective substrate doping.
`vnsub=0.0 V`	Effective doping bias-dependence parameter.
`nslp=0.05 V`	Effective doping bias-dependence parameter.
`dnsub=0.0 V^-1`	Effective doping bias-dependence parameter.
`dphib=0.0 V`	Offset parameter for PHIB.
`np=1.0e+26` m^{-3}	Gate poly-silicon doping.
`ct=0.0`	Interface states factor.
`toxov=2.0e-09 m`	Overlap oxide thickness.
`toxovd=2.0e-09 m`	Overlap oxide thickness for drain side.
`nov=5.0e+25` m^{-3}	Effective doping of overlap region.
`novd=5.0e+25` m^{-3}	Effective doping of overlap region for drain side.
`cf=0.0`	DIBL-parameter.
`cfb=0.0 V^-1`	Back bias dependence of CF.
`betn=7e-2` $m^2/V/s$	Channel aspect ratio times zero-field mobility.
`stbet=1.0`	Temperature dependence of BETN.
`mue=0.5 m/V`	Mobility reduction coefficient at TR.
`stmue=0.0`	Temperature dependence of MUE.
`themu=1.5`	Mobility reduction exponent at TR.
`stthemu=1.5`	Temperature dependence of THEMU.
`cs=0.0`	Coulomb scattering parameter at TR.
`stcs=0.0`	Temperature dependence of CS.
`xcor=0.0 V^-1`	Non-universality factor.

© 2023 Cadence Design Systems, Inc.

`stxcor=0.0`	Temperature dependence of XCOR.
`feta=1.0`	Effective field parameter.
`rs=30 Ω`	Series resistance at TR.
`strs=1.0`	Temperature dependence of RS.
`rsb=0.0 V^-1`	Back-bias dependence of series resistance.
`rsg=0.0 V^-1`	Gate-bias dependence of series resistance.
`thesat=1.0 V^-1`	Velocity saturation parameter at TR.
`stthesat=1.0`	Temperature dependence of THESAT.
`thesatb=0.0 V^-1`	Back-bias dependence of velocity saturation.
`thesatg=0.0 V^-1`	Gate-bias dependence of velocity saturation.
`ax=3.0`	Linear/saturation transition factor.
`alp=0.01`	CLM pre-factor.
`alp1=0.00 V`	CLM enhancement factor above threshold.
`alp2=0.00 V^-1`	CLM enhancement factor below threshold.
`vp=0.05 V`	CLM logarithm dependence factor.
`a1=1.0`	Impact-ionization pre-factor.
`a2=10.0 V`	Impact-ionization exponent at TR.
`sta2=0.0 V`	Temperature dependence of A2.
`a3=1.0`	Saturation-voltage dependence of impact-ionization.
`a4=0.0 V^-0.5`	Back-bias dependence of impact-ionization.
`gco=0.0`	Gate tunneling energy adjustment.
`iginv=0.0 A`	Gate channel current pre-factor.
`igov=0.0 A`	Gate overlap current pre-factor.
`igovd=0.0 A`	Gate overlap current pre-factor for drain side.
`stig=2.0`	Temperature dependence of IGINV and IGOV.
`gc2=0.375`	Gate current slope factor.
`gc3=0.063`	Gate current curvature factor.
`chib=3.1 V`	Tunneling barrier height.
`agidl=0.0 A/V`^{3}	GIDL pre-factor.

© 2023 Cadence Design Systems, Inc.

`agidld=0.0 A/V`^{3}	GIDL pre-factor for drain side.
`bgidl=41.0 V`	GIDL probability factor at TR.
`bgidld=41.0 V`	GIDL probability factor at TR for drain side.
`stbgidl=0.0 V/K`	Temperature dependence of BGIDL.
`stbgidld=0.0 V/K`	Temperature dependence of BGIDL for drain side.
`cgidl=0.0`	Back-bias dependence of GIDL.
`cgidld=0.0`	Back-bias dependence of GIDL for drain side.
`cox=1.0e-14 F`	Oxide capacitance for intrinsic channel.
`cgov=1.0e-15 F`	Oxide capacitance for gate-drain/source overlap.
`cgovd=1.0e-15 F`	Oxide capacitance for gate-drain overlap.
`cgbov=0.0 F`	Oxide capacitance for gate-bulk overlap.
`cfr=0.0 F`	Outer fringe capacitance.
`cfrd=0.0 F`	Outer fringe capacitance for drain side.
`fnt=1.0`	Thermal noise coefficient.
`fntexc=0.0`	Excess noise coefficient.
`nfa=8.0e+22 V^-1/m`^{4}	First coefficient of flicker noise.
`nfb=3.0e+07 V^-1/m`^{2}	Second coefficient of flicker noise.
`nfc=0.0 V^-1`	Third coefficient of flicker noise.
`ef=1.0`	Flicker noise frequency exponent.
`munqs=1.0`	Relative mobility for NQS modelling.
`rg=0.0` Ω	Gate resistance.
`rbulk=0.0` Ω	Bulk resistance between node BP and BI.
`rwell=0.0` Ω	Well resistance between node BI and B.
`rjuns=0.0` Ω	Source-side bulk resistance between node BI and BS.
`rjund=0.0` Ω	Drain-side bulk resistance between node BI and BD.
`imax=1000 A`	Maximum current up to which forward current behaves exponentially.

© 2023 Cadence Design Systems, Inc.

`trj=21 C`	reference temperature.
`cjorbot=1E-3 Fm^-2`	Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.
`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.
`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.
`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.
`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
`idsatrbot=1E-12 Am^-2`	Saturation current density at the reference temperature of bottom component for source-bulk junction.
`idsatrsti=1E-18 Am^-1`	

© 2023 Cadence Design Systems, Inc.

	Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
`idsatrgat=1E-18 Am^-1`	
	Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
`csrhbot=1E2 Am`$^{-3}$	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
`csrhsti=1E-4 Am`$^{-2}$	
	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
`csrhgat=1E-4 Am`$^{-2}$	
	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.
`xjunsti=100E-9 m`	Junction depth of STI-edge component for source-bulk junction.
`xjungat=100E-9 m`	Junction depth of gate-edge component for source-bulk junction.
`ctatbot=1E2 Am`$^{-3}$	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
`ctatsti=1E-4 Am`$^{-2}$	
	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
`ctatgat=1E-4 Am`$^{-2}$	
	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
`mefftatbot=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
`mefftatsti=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
`mefftatgat=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
`cbbtbot=1E-12 AV`$^{-3}$	

© 2023 Cadence Design Systems, Inc.

	Band-to-band tunneling prefactor of bottom component for source-bulk junction.
`cbbtsti=1E-18 AV-3m`	
	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
`cbbtgat=1E-18 AV-3m`	
	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
`fbbtrbot=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.
`fbbtrsti=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
`fbbtrgat=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
`stfbbtbot=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
`stfbbtsti=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
`stfbbtgat=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
`vbrbot=10 V`	Breakdown voltage of bottom component for source-bulk junction.
`vbrsti=10 V`	Breakdown voltage of STI-edge component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

`vbrgat=10 V`	Breakdown voltage of gate-edge component for source-bulk junction.
`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component for source-bulk junction.
`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
`cjorbotd=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.
`cjorstid=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.
`cjorgatd=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.
`vbirbotd=1 V`	Built-in voltage at the reference temperature of bottom component for drain-bulk junction.
`vbirstid=1 V`	Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.
`vbirgatd=1 V`	Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.
`pbotd=0.5`	Grading coefficient of bottom component for drain-bulk junction.
`pstid=0.5`	Grading coefficient of STI-edge component for drain-bulk junction.
`pgatd=0.5`	Grading coefficient of gate-edge component for drain-bulk junction.
`phigbotd=1.16 V`	Zero-temperature bandgap voltage of bottom component for drain-bulk junction.
`phigstid=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`phiggatd=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.
`idsatrbotd=1E-12 Am^-2`	Saturation current density at the reference temperature of bottom component for drain-bulk junction.
`idsatrstid=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.
`idsatrgatd=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.
`csrhbotd=1E2 Am^-3`	Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.
`csrhstid=1E-4 Am^-2`	Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
`csrhgatd=1E-4 Am^-2`	Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
`xjunstid=100E-9 m`	Junction depth of STI-edge component for drain-bulk junction.
`xjungatd=100E-9 m`	Junction depth of gate-edge component for drain-bulk junction.
`ctatbotd=1E2 Am^-3`	Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
`ctatstid=1E-4 Am^-2`	Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
`ctatgatd=1E-4 Am^-2`	Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

`mefftatbotd=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
`mefftatstid=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.
`mefftatgatd=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
`cbbtbotd=1E-12 AV`$^{-3}$	Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
`cbbtstid=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.
`cbbtgatd=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.
`fbbtrbotd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.
`fbbtrstid=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.
`fbbtrgatd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.
`stfbbtbotd=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.
`stfbbtstid=(-1E-3) K^-1`	Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

stfbbtgatd=(-1E-3) K^-1	Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.
vbrbotd=10 V	Breakdown voltage of bottom component for drain-bulk junction.
vbrstid=10 V	Breakdown voltage of STI-edge component for drain-bulk junction.
vbrgatd=10 V	Breakdown voltage of gate-edge component for drain-bulk junction.
pbrbotd=4 V	Breakdown onset tuning parameter of bottom component for drain-bulk junction.
pbrstid=4 V	Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.
pbrgatd=4 V	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
swjunexp=0.0	Flag for JUNCAP express. Specify 0 for full model and 1 for express model.
vjunref=2.5	The maximum source-bulk junction voltage; usually about 2*VSUP.
fjunq=0.03	Fraction below which source-bulk junction capacitance components are considered negligible.
vjunrefd=2.5	The maximum drain-bulk junction voltage; usually about 2*VSUP.
fjunqd=0.03	Fraction below which drain-bulk junction capacitance components are considered negligible.
dta=0 K	Temperature offset w.r.t. ambient circuit temperature.
mvt=0.0	DCmatch parameter.
mbe=0.0	DCmatch parameter.
vds_max=infinity V	Maximum allowed voltage cross source and drain.
vgd_max=infinity V	Maximum allowed voltage cross gate and drain.

© 2023 Cadence Design Systems, Inc.

`vgs_max=infinity V`	
	Maximum allowed voltage cross gate and source/bulk.
`vbd_max=infinity V`	
	Maximum allowed voltage cross source/drain and bulk.
`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
`vgb_max=infinity V`	
	Maximum allowed voltage cross gate and bulk.
`vgdr_max=vgd_max V`	
	Maximum allowed reverse voltage cross gate and drain.
`vgsr_max=vgs_max V`	
	Maximum allowed reverse voltage cross gate and source.
`vgbr_max=vgb_max V`	
	Maximum allowed reverse voltage cross gate and bulk.
`vbsr_max=vbs_max V`	
	Maximum allowed reverse voltage cross source and bulk.
`vbdr_max=vbd_max V`	
	Maximum allowed reverse voltage cross source/drain and bulk.
`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
`noisemethod=oldcmi`	

© 2023 Cadence Design Systems, Inc.

	Induced gate noise implementation. Possible values are `oldcmi`, `subckt`, `newcmi`, and `noign`.

Output Parameters

`weff (m)`	Effective channel width for geometrical models.
`leff (m)`	Effective channel length for geometrical models.
`lv1 (m)`	Alias of l.
`lv2 (m)`	Alias of w.
`lv3 ($m^2$)`	Alias of ad.
`lv4 ($m^2$)`	Alias of as.
`lv11 (m)`	Alias of pd.
`lv12 (m)`	Alias of ps.

Operating-Point Parameters

`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`dtsh (K)`	Device temperature rise due to self-heating.
`ctype`	Flag for channel type.
`sdint`	Flag for source-drain interchange.
`is (A)`	External DC current at source terminal.
`ise (A)`	Total source current.
`ig (A)`	External DC current at gate terminal.
`ige (A)`	Total gate current.
`id (A)`	External DC current at drain terminal.
`ide (A)`	Total drain current.
`ib (A)`	Total bulk current.
`ibe (A)`	Total bulk current.

© 2023 Cadence Design Systems, Inc.

ids (A)	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
idb (A)	Drain to bulk current.
isb (A)	Source to bulk current.
igs (A)	Gate-source tunneling current.
igd (A)	Gate-drain tunneling current.
igb (A)	Gate-bulk tunneling current.
igcs (A)	Gate-channel tunneling current (source component).
igcd (A)	Gate-channel tunneling current (drain component).
iavl (A)	Substrate current due to weak avalanche.
igisl (A)	Gate-induced source leakage current.
igidl (A)	Gate-induced drain leakage current.
ijs (A)	Total source junction current.
ijsbot (A)	Source junction current (bottom component).
ijsgat (A)	Source junction current (gate-edge component).
ijssti (A)	Source junction current (STI-edge component).
ijd (A)	Total drain junction current.
ijdbot (A)	Drain junction current (bottom component).
ijdgat (A)	Drain junction current (gate-edge component).
ijdsti (A)	Drain junction current (STI-edge component).
qg (Coul)	Intrinsic gate charge.
qd (Coul)	Intrinsic drain charge.
qb (Coul)	Intrinsic bulk charge.
qs (Coul)	Intrinsic source charge.
qgs_ov (Coul)	Overlap charge for gate-source.
qgd_ov (Coul)	Overlap charge for gate-drain.
qfgs (Coul)	Sum of outerFringe and overlap for gate-source.
qfgd (Coul)	Sum of outerFringe and overlap for gate-drain.
qgb_ov (Coul)	Gate-bulk overlap charge.

© 2023 Cadence Design Systems, Inc.

qjun_s (Coul)	Junction charge on source side.
qjun_d (Coul)	Junction charge on drain side.
vds (V)	Drain-source voltage.
vgs (V)	Gate-source voltage.
vgd (V)	External gate-drain DC voltage.
vsb (V)	Source-bulk voltage.
vdb (V)	External drain-bulk DC voltage.
vth0 (V)	Zero-bias threshold voltage.
vto (V)	Zero-bias threshold voltage.
vts (V)	Threshold voltage including back bias effects.
vth (V)	Threshold voltage including back bias and drain bias effects.
vth_drive (V)	Gate overdrive voltage including back-bias, drain bias effects.
vgt (V)	Effective gate drive voltage including back bias and drain bias effects.
vdss (V)	Drain saturation voltage at actual bias.
vdsat (V)	Drain saturation voltage.
vdsat_marg (V)	Saturation margin with respect to Vdsat for Drain voltage.
vsat (V)	Saturation limit.
pwr (W)	Power at op point.
gm (1/Ω)	Transconductance.
gmb (1/Ω)	Substrate transconductance.
go (1/Ω)	Output conductance.
gds (1/Ω)	Output conductance.
gjs (1/Ω)	Source junction conductance.
gjd (1/Ω)	Drain junction conductance.
cdd (F)	Drain capacitance.
cdg (F)	Drain-gate capacitance.
cds (F)	Drain-source capacitance.
cdb (F)	Drain-bulk capacitance.

© 2023 Cadence Design Systems, Inc.

cgd (F)	Gate-drain capacitance.
cgg (F)	Gate capacitance.
cgs (F)	Gate-source capacitance.
cgb (F)	Gate-bulk capacitance.
csd (F)	Source-drain capacitance.
csg (F)	Source-gate capacitance.
css (F)	Source capacitance.
csb (F)	Source-bulk capacitance.
cbd (F)	Bulk-drain capacitance.
cbg (F)	Bulk-gate capacitance.
cbs (F)	Bulk-source capacitance.
cbb (F)	Bulk capacitance.
co (F)	Output Drain-Source capacitance.
cm (F)	Capacitance element 1 for QS model.
cmb (F)	Capacitance element 2 for QS model.
cmx (F)	Capacitance element 3 for QS model.
tau1 (s)	Time constant related to NQS first frequency pole.
fqslim (Hz)	QS model frequency limit.
cgsol (F)	Total gate-source overlap capacitance.
cgdol (F)	Total gate-drain overlap capacitance.
cgbol (F)	Total gate-bulk overlap capacitance.
cjs (F)	Total source junction capacitance.
cjsbot (F)	Source junction capacitance (bottom component).
cjsgat (F)	Source junction capacitance (gate-edge component).
cjssti (F)	Source junction capacitance (STI-edge component).
cjd (F)	Total drain junction capacitance.
cjdbot (F)	Drain junction capacitance (bottom component).
cjdgat (F)	Drain junction capacitance (gate-edge component).
cjdsti (F)	Drain junction capacitance (STI-edge component).

© 2023 Cadence Design Systems, Inc.

lpoly (m)	Length of poly.
self_gain	Gm/Go ratio (MOSFET self-gain).
u	Transistor gain.
rout (Ω)	Small-signal output resistance.
vearly (V)	Equivalent Early voltage.
ft (Hz)	Unity gain frequency at actual bias.
beff (A/V^2)	Gain factor.
gmoveri (1/V)	Transconductance efficiency.
fug (Hz)	Unity gain frequency at actual bias.
rgate (Ω)	Gate resistance.
rg (Ω)	Gate resistance.
sfl (A^2/Hz)	Flicker noise current spectral density at 1 Hz.
sqrtsff (V/$\sqrt{}$Hz)	Input-referred RMS white noise voltage spectral density at 1 kHz.
sqrtsfw (V/$\sqrt{}$Hz)	Input-referred RMS white noise voltage spectral density.
sid (A^2/Hz)	White noise current spectral density.
sig (A^2/Hz)	Induced gate noise current spectral density at 1 Hz.
cigid	Imaginary part of correlation coefficient between Sig and Sid.
fknee (Hz)	Cross-over frequency above which white noise is dominant.
sigs (A^2/Hz)	Gate-source current noise spectral density.
sigd (A^2/Hz)	Gate-drain current noise spectral density.
siavl (A^2/Hz)	Impact ionization current noise spectral density.
ssi (A^2/Hz)	Total source junction current noise spectral density.
sdi (A^2/Hz)	Total drain junction current noise spectral density.
vbs (V)	Bulk-source voltage.
lv9 (V)	Alias of vth.
lv10 (V)	Alias of vdss.

© 2023 Cadence Design Systems, Inc.

lv36 (F)	Alias of cgsol.
lv37 (F)	Alias of cgdol.
lv38 (F)	Alias of cgbol.
lv51 (m)	Alias of tox.
lx4 (A)	Alias of ids.
lx3 (V)	Alias of vds.
lx2 (V)	Alias of vgs.
lx7 (1/Ω)	Alias of gm.
lx8 (1/Ω)	Alias of gds.
lx9 (1/Ω)	Alias of gmb.
lx33 (F)	Alias of cdd.
lx32 (F)	Alias of cdg.
lx34 (F)	Alias of cds.
lx19 (F)	Alias of cgd.
lx18 (F)	Alias of cgg.
lx20 (F)	Alias of cgs.
lx22 (F)	Alias of cbd.
lx21 (F)	Alias of cbg.
lx23 (F)	Alias of cbs.
lx5 (A)	Alias of ijs.
lx6 (A)	Alias of ijd.
lx28 (F)	Alias of cjs.
lx29 (F)	Alias of cjd.
lx38 (A)	Alias of igs.
lx39 (A)	Alias of igd.
lx66 (A)	Alias of igb.
lx67 (A)	Alias of igcs.
lx68 (A)	Alias of igcd.
lx110 (A)	Alias of igisl.

© 2023 Cadence Design Systems, Inc.

`lx47 (A)`	Alias of igidl.
`lx60 (F)`	Alias of csd.
`lx59 (F)`	Alias of csg.
`lx58 (F)`	Alias of css.
`lx12 (Coul)`	Alias of Qb including overlap charge.
`lx14 (Coul)`	Alias of Qg including overlap charge.
`lx16 (Coul)`	Alias of Qd including overlap charge.
`lx83 (F)`	Alias of cgd including overlap cap.
`lx84 (F)`	Alias of cgs including overlap cap.
`OPdef`	1: Device Physics notation. 2: Circuit Simulator notation.
`SDop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.

Related Topics

PSP102 Model

Component Statements for PSP102 Models

PSP MOSFET Model (PSP102)

PSP MOSFET Model (PSP102)

PSP MOSFET Model (psp1020)

PSP MOSFET Model (psp1021)

PSP local MOSFET Model (psp102e)

PSP NQS MOSFET Model (pspnqs1020)

PSP NQS MOSFET Model (pspnqs1021)

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

25

PSP103 Model

PSP103 is a compact MOSFET model intended for digital, analog and RF designs. It is jointly developed by NXP Semiconductors Research and Arizona State University, and is a surface-potential based MOS model containing all relevant physical effects (mobility reduction, velocity saturation, DIBL, gate current, lateral doping gradient effects, STI stress, and so forth), to model present-day and upcoming deep-submicron bulk CMOS technologies. The JUNCAP2 source/drain junction model is an integrated part of PSP103.

PSP103 not only gives an accurate description of currents, charges, and their first order derivatives (i.e. transconductance, conductance and capacitances), but also of the higher order derivatives, resulting in an accurate description of electrical distortion behavior. The latter is especially important for analog and RF circuit design. The model, furthermore, gives an accurate description of the noise behavior of MOSFETs.

For a full description of the PSP103 model, see http://pspmodel.asu.edu.

This chapter contains the following information:

- Model Usage on page 1821
  - Instance Syntax on page 1821
  - Model Syntax on page 1821
- Model History and Development on page 1822
- Reference on page 1825
  - Model Description on page 1825
  - Geometry Scaling and Stress Model for Intrinsic MOSFET on page 1825
  - PSP 103 Model Equations on page 1855
  - Non-quasi-static RF model on page 1891
  - Instance Parameters on page 1976
  - Model Parameters on page 1902

© 2023 Cadence Design Systems, Inc.

- Parameter Index on page 2035

© 2023 Cadence Design Systems, Inc.

Model Usage

Instance Syntax

PSP103 instance has 4 or 5 terminals. The `ModelName` has to be associated with a PSP103 model card.

```
InstanceName (d g s b [t]) PSP103ModelName <parameter=value>
```

Sample Instance Statement

```
q1(v1 v2 v3 v4) psp103_mod w=1e-6 1=0.5e-6
```

Model Syntax

The following syntax specifies PSP103 model:

```
model ModelName psp103 parameter=value ...
```

The third parameter, “psp103”, is the master to indicate this model card is a PSP103 model card.

Version and Master Name

1. Versions 103.0, 103.1, 103.1.1, 103.2, 103.3, 103.4, 103.5, and 103.6, 103.7are supported
2. There are three master names - psp103, psp103t, and pspnqs103 (for QS, self-heating, and NQS respectively)

   Self-heating and NQS effects can be invoked in the master name `psp103` by setting the SHE or NQS parameters in the model card.

Sample Model Statement

Example PSP103.0

```
model psp103_mod psp103 type=n version=103.0
+tr = 25 swigate = 0
+binmod=0 geomod=1 swnqs=9 swgidl = 1 swjuncap = 3
```

Example PSP103.1

```
model psp103_mod psp103 type=n version=103.1
```


© 2023 Cadence Design Systems, Inc.

```
+tr = 25 swigate = 0
+binmod=0 geomod=1 swnqs=9 swgidl = 1 swjuncap = 3
```

Model History and Development

PSP103.0 (SiMKit3.2)

- Implemented in MMSIM7.1.1 in June 2009

PSP103.1 (SiMKit3.3)

- Implemented in MMSIM7.2 in December 2010

Changes

- Added external sheet resistance RSHD for drain diffusion (used when SWJUNASYM=1)
- Extended NUD model to allow retrograde profiles (GFACNUD>1)
- Added value of gate resistance to OP-output
- Bug fix and minor implementation change in NUD-model
- Minor bug fix in conditional for SP-calculation of overlap areas

PSP103.1.1 (SiMKit3.4)

- Implemented in MMSIM10.1 in June 2010

Changes

- Modified implementation of the asymmetrical junction model to improve simulation speed of the verilog-A code.
- Modified implementation of the MULT-scaling factor.
- Modified implementation of the NUD model.
- Modified implementation of the stand-alone JUNCAP2 model.
- Minor bug fix for the output of sfl, sqrtsfw, and fknee

© 2023 Cadence Design Systems, Inc.

PSP103.2 (SiMKit4.0.1)

- Implemented in MMSIM12.1.1 in May 2013

Changes

- Introduction of self heating. The self heating version has an additional temperature terminal `dt`, thermal resistance RTH, and thermal capacitance CTH. Geometry scaling rules for RTH and CTH, as well as temperature dependence of RTH are also provided.
- Implementation of the thermal noise model has been improved:
  - A bug in the sign of the correlation coefficient for negative `Vds` has been fixed
  - Gummel symmetry of `Sid` at high frequencies has been improved
  - Number of `white_noise` sources has been reduced and the noise voltage values in the noise-subcircuit have been scaled to more physical values (simulation results are not affected).
- The calculation of the surface potential in the gate-diffusion overlap region has been simplified to improve simulation speed of verilog-A code.
- The expression for `qlim2` in QM correction has been modified to avoid unphysical behavior when oxide thickness is large. This modification is relevant for high-k dielectrics.
- Minor bugs in the calculation of OP-output variables have been fixed.
- Minor implementation changes have been made.
- Few OP-output variables have been added.

PSP103.3

- Implemented in MMSIM13.1 ISR10 in July 2014

Changes

- Excess noise, important for sub-100 nm channel lengths has been added. This is backward-compatible with PSP103.2 version.
- Following new parameters have been added:
  - FNTEXC (local model)

© 2023 Cadence Design Systems, Inc.

- FNTEXCL (global model)
- POFNTEXC, PLFNTEXC, PWFNTEXC, and PLWFNTEXC (binning model)

- Missing T-scaling in OP output variables `lp_bgidl` and `lp_bgidld` has been fixed.

PSP103.4

- Implemented in MMSIM15.1 ISR15 in Feb 2017

Changes

- Addition of edge MOSFET for modeling of subthreshold hump effect.
- New model parameter SWIGN to active/disable the induced gate noise.
- New parameters for modeling of short channel effects on subthreshold slope.
- New local and global parameters for DIBL
- Minor bug fixes.
- Minor implementation changes have been made.
- New OP-output variables for edge transistor.

PSP103.5

- Implemented in SPECTRE16.1ISR6 in May 2017

Changes

- New mobility parameters for coulomb scattering effect: THECS, STTHECS (local model), THECSO, STTHECSO (global model), and POTHECS, POSTTHECS (binning model).
- New parameters added for quadratic temperature dependence of flatband voltage: ST2VFB (local model), ST2VFBO (global model), and POST2VFB (binning model).

PSP103.6

- Implemented in SPECTRE18.1in June 2018. PSP103.6 is backward compatible with PSP103.5.

© 2023 Cadence Design Systems, Inc.

Changes

- Induced gate noise: clipped value of `migid` using the correlation factor `c_igid`.
- Thermal noise of edge transistor is fixed to avoid possible division by zero during the calculation of redge.
- New model for interface states; improved gm/Id in weak inversion.
- Addition of new parameter for exponent for channel length dependence of edge transistor substrate doping: NSUBEDGELEXP
- Minimum values of local parameters NOV and NOVD in the global mode is now in line with minimum values of local model parameters.

PSP103.7

PSP 103.7 is backwards compatible with PSP 103.6.

Changes

- Gate leakage currents: Addition of parameters for overlaps gate leakage currents CG2OV, CG3OV (local model), CG2OVO, CG3OVO (global model), and POCG2OV, POCG3OV (binning model).
- Charge partitioning: Addition of new switch parameter SWQPART to modify the charge partitioning between the drain and the source.
- Charge model in saturation by setting SWQSAT=1. Parameters added for charge model to improve CV description in saturation.

Reference

Model Description

Geometry Scaling and Stress Model for Intrinsic MOSFET

The physical geometry scaling rules of PSP have been developed to give a good description over the whole geometry range of CMOS technologies. As an alternative, the binning-rules can be used to allow for a more phenomenological geometry dependency.

© 2023 Cadence Design Systems, Inc.

Note: The user has to choose between the two options; the geometrical scaling rules and the binning scaling rules cannot be used at the same time. In both cases, the result is a local parameter set (for a transistor of the specified L and W), which is fed into the local model.

Stress and well proximity effects are included in PSP. Use of the stress model and/or well proximity effect model leads to modification of some of the local parameters calculated from the geometrical or binning scaling rules.

Geometrical scaling rules

The physical scaling rules to calculate the local parameters from a global parameter set are given in this section.

Note:

- After calculation of the local parameters (and possible application of the stress equations), clipping is applied according to Section “Intrinsic Parameters” for the model.
- The geometrical scaling equations are only calculated when SWGEO = 1.

Effective length and width

$$W_f = \frac{W}{\mathbf{NF}}$$

$$L_{\mathrm{EN}} = 10^{-6}$$

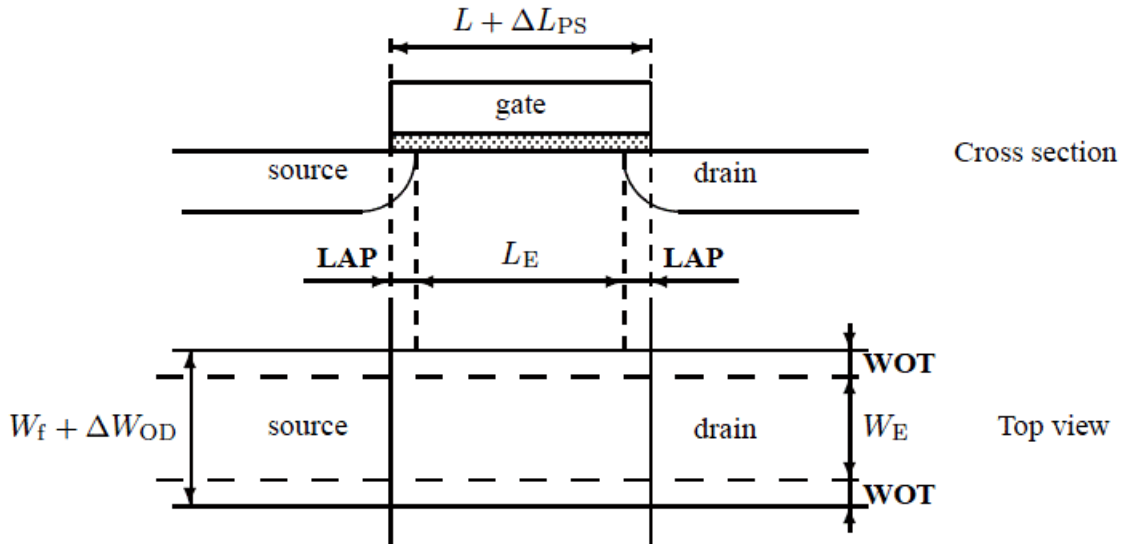
$$W_{\mathrm{EN}} = 10^{-6}$$

$$\Delta L_{\mathrm{PS}} = \mathbf{LVARO} \cdot \left(1 + \mathbf{LVARL} \cdot \frac{L_{\mathrm{EN}}}{L}\right) \cdot \left(1 + \mathbf{LVARW} \cdot \frac{W_{\mathrm{EN}}}{W_f}\right)$$

$$\Delta W_{\mathrm{OD}} = \mathbf{WVARO} \cdot \left(1 + \mathbf{WVARL} \cdot \frac{L_{\mathrm{EN}}}{L}\right) \cdot \left(1 + \mathbf{WVARW} \cdot \frac{W_{\mathrm{EN}}}{W_f}\right)$$

© 2023 Cadence Design Systems, Inc.

Figure 25-1 Specification of the dimensions of a MOS transistor



$$L_E = L - \Delta L = L + \Delta L_{PS} - 2 \cdot \mathbf{LAP}$$

$$W_E = W_f - \Delta W = W_f + \Delta W_{OD} - 2 \cdot \mathbf{WOT}$$

$$L_{E,CV} = L + \Delta L_{PS} - 2 \cdot \mathbf{LAP} + \mathbf{DLQ}$$

$$W_{E,CV} = W_f + \Delta W_{OD} - 2 \cdot \mathbf{WOT} + \mathbf{DWQ}$$

$$L_{G,CV} = L + \Delta L_{PS} + \mathbf{DLQ}$$

$$W_{G,CV} = W_f + \Delta W_{OD} + \mathbf{DWQ}$$

Note: If the calculated LE, WE, LE,CV, WE,CV, LG,CV, or WG,CV is smaller than 1 nm (10?9 m), the value is clipped to this lower bound of 1 nm.

Process Parameters

$$\mathbf{VFB} = \mathbf{VFBO} + \mathbf{VFBL} \cdot \frac{L_{EN}}{L_E} + \mathbf{VFBW} \cdot \frac{W_{EN}}{W_E} + \mathbf{VFBLW} \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}$$

$$\mathbf{STVFB} = \mathbf{STVFBO} + \mathbf{STVFBL} \cdot \frac{L_{EN}}{L_E} + \mathbf{STVFBW} \cdot \frac{W_{EN}}{W_E} + \mathbf{STVFBLW} \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}$$

$$\mathbf{TOX} = \mathbf{TOXO}$$

$$\mathbf{EPSROX} = \mathbf{EPSROXO}$$

© 2023 Cadence Design Systems, Inc.

$$N_{subo,eff} = \mathbf{NSUBO} \cdot \mathrm{MAX}\left(\left[1 + \mathbf{NSUBW} \cdot \frac{W_{EN}}{W_E} \cdot \ln\left(1 + \frac{W_E}{\mathbf{WSEC}}\right)\right], 10^{-3}\right)$$

$$N_{pck,eff} = \mathbf{NPCK} \cdot \mathrm{MAX}\left(\left[1 + \mathbf{NPCKW} \cdot \frac{W_{EN}}{W_E} \cdot \ln\left(1 + \frac{W_E}{\mathbf{WSEGP}}\right)\right], 10^{-3}\right)$$

$$L_{pck,eff} = \mathbf{LPCK} \cdot \mathrm{MAX}\left(\left[1 + \mathbf{LPCKW} \cdot \frac{W_{EN}}{W_E} \cdot \ln\left(1 + \frac{W_E}{\mathbf{WSEGP}}\right)\right], 10^{-3}\right)$$

$$a = 7.5 \cdot 10^{10}$$

$$b = \sqrt{N_{subo,eff} + 0.5 \cdot N_{pck,eff}} - \sqrt{N_{subo,eff}}$$

$$N_{sub} = \begin{cases} N_{subo,eff} + N_{pck,eff} \cdot \left[2 - \frac{L_E}{L_{pck,eff}}\right] & \text{for } L_E < L_{pck,eff} \\ N_{subo,eff} + N_{pck,eff} \cdot \frac{L_{pck,eff}}{L_E} & \text{for } L_{pck,eff} \le L_E \le 2 \cdot L_{pck,eff} \\ \left[\sqrt{N_{subo,eff}} + a \cdot \ln\left(1 + 2 \cdot \frac{L_{pck,eff}}{L_E} \cdot \left[\exp\left(\frac{b}{a}\right) - 1\right]\right)\right]^2 & \text{for } L_E > 2 \cdot L_{pck,eff} \end{cases}$$

$$\mathbf{NEFF} = N_{sub} \cdot \left(1 - \mathbf{FOL1} \cdot \frac{L_{EN}}{L_E} - \mathbf{FOL2} \cdot \left[\frac{L_{EN}}{L_E}\right]^2\right)$$

$$\mathbf{FACNEFFAC} = \mathbf{FACNEFFACO} + \mathbf{FACNEFFACL} \cdot \frac{L_{EN}}{L_E} + \mathbf{FACNEFFACW} \cdot \frac{W_{EN}}{W_E} + \mathbf{FACNEFFACLW} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathbf{GFACNUD} = \mathbf{GFACNUDO} + \mathbf{GFACNUDL} \cdot \left[\frac{L_{EN}}{L_E}\right]^{\mathbf{GFACNUDLEXP}} + \mathbf{GFACNUDW} \cdot \frac{W_{EN}}{W_E} + \mathbf{GFACNUDLW} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathbf{VSBNUD} = \mathbf{VSBNUDO}$$

$$\mathbf{DVSBNUD} = \mathbf{DVSBNUDO}$$

$$\mathbf{VNSUB} = \mathbf{VNSUBO}$$

$$\mathbf{NSLP} = \mathbf{NSLPO}$$

$$\mathbf{DNSUB} = \mathbf{DNSUBO}$$

© 2023 Cadence Design Systems, Inc.

$$\mathbf{DPHIB} = \mathbf{DPHIBO} + \mathbf{DPHIBL} \cdot \left[\frac{L_{EN}}{L_E}\right]^{\mathbf{DPHIBLEXP}} + \mathbf{DPHIBW} \cdot \frac{W_{EN}}{W_E} + \mathbf{DPHIBLW} \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}$$

$$\mathbf{DELVTAC} = \mathbf{DELVTACO} + \mathbf{DELVTACL} \cdot \left[\frac{L_{EN}}{L_E}\right]^{\mathbf{DELVTACLEXP}} + \mathbf{DELVTACW} \cdot \frac{W_{EN}}{W_E} + \mathbf{DELVTACLW} \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}$$

$$\mathbf{NP} = \mathbf{NPO} \cdot \mathrm{MAX}\left(10^{-6}, 1 + \mathbf{NPL} \cdot \frac{L_{EN}}{L_E}\right)$$

$$\mathbf{CT} = \left(\mathbf{CTO} + \mathbf{CTL} \cdot \left[\frac{L_{EN}}{L_E}\right]^{\mathbf{CTLEXP}}\right) \cdot \left(1 + \mathbf{CTW} \cdot \frac{W_{EN}}{W_E}\right) \cdot \left(1 + \mathbf{CTLW} \cdot \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E}\right)$$

$$\mathbf{TOXOV} = \mathbf{TOXOVO}$$

$$\mathbf{TOXOVD} = \mathbf{TOXOVDO}$$

$$\mathbf{NOV} = \mathbf{NOVO}$$

$$\mathbf{NOVD} = \mathbf{NOVDO}$$

DIBL Parameters

$$\mathbf{CF} = \mathbf{CFL} \cdot \left[\frac{L_{EN}}{L_E}\right]^{\mathbf{CFLEXP}} \cdot \left(1 + \mathbf{CFW} \cdot \frac{W_{EN}}{W_E}\right)$$

$$\mathbf{CFB} = \mathbf{CFBO}$$

$$F_{\beta 1,\mathrm{eff}} = \mathbf{FBET1} \cdot \left(1 + \mathbf{FBET1W} \cdot \frac{W_{EN}}{W_E}\right)$$

$$L_{P1,\mathrm{eff}} = \mathbf{LP1} \cdot \mathrm{MAX}\left(\left[1 + \mathbf{LP1W} \cdot \frac{W_{EN}}{W_E}\right], 10^{-3}\right)$$

$$G_{P,E} = 1 + F_{\beta 1,\mathrm{eff}} \cdot \frac{L_{P1,\mathrm{eff}}}{L_E} \cdot \left[1 - \exp\left(-\frac{L_E}{L_{P1,\mathrm{eff}}}\right)\right] + \mathbf{FBET2} \cdot \frac{\mathbf{LP2}}{L_E} \cdot \left[1 - \exp\left(-\frac{L_E}{\mathbf{LP2}}\right)\right]$$

$$G_{W,E} = 1 + \mathbf{BETW1} \cdot \frac{W_{EN}}{W_E} + \mathbf{BETW2} \cdot \frac{W_{EN}}{W_E} \cdot \ln\left(1 + \frac{W_E}{\mathbf{WBET}}\right)$$

© 2023 Cadence Design Systems, Inc.

$$\mathbf{BETN} = \frac{\mathbf{UO}}{G_{\mathrm{P,E}}} \cdot \frac{W_{\mathrm{E}}}{L_{\mathrm{E}}} \cdot G_{\mathrm{W,E}}$$

$$\mathbf{STBET} = \mathbf{STBETO} + \mathbf{STBETL} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{STBETW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{STBETLW} \cdot \frac{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}$$

$$\mathbf{MUE} = \mathbf{MUEO} \cdot \left[1 + \mathbf{MUEW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}}\right]$$

$$\mathbf{STMUE} = \mathbf{STMUEO}$$

$$\mathbf{THEMU} = \mathbf{THEMUO}$$

$$\mathbf{STTHEMU} = \mathbf{STTHEMUO}$$

$$\mathbf{CS} = \left(\mathbf{CSO} + \mathbf{CSL} \cdot \left[\frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}\right]^{\mathbf{CSLEXP}}\right) \cdot \left(1 + \mathbf{CSW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}}\right) \cdot \left(1 + \mathbf{CSLW} \cdot \frac{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}\right)$$

$$\mathbf{STCS} = \mathbf{STCSO}$$

$$\mathbf{XCOR} = \mathbf{XCORO} \cdot \left(1 + \mathbf{XCORL} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}\right) \cdot \left(1 + \mathbf{XCORW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}}\right) \cdot \left(1 + \mathbf{XCORLW} \cdot \frac{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}\right)$$

$$\mathbf{STXCOR} = \mathbf{STXCORO}$$

$$\mathbf{FETA} = \mathbf{FETAO}$$

Series Resistance Parameters

$$\mathbf{RS} = \mathbf{RSW1} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} \cdot \left[1 + \mathbf{RSW2} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}}\right]$$

$$\mathbf{STRS} = \mathbf{STRSO}$$

$$\mathbf{RSB} = \mathbf{RSBO}$$

$$\mathbf{RSG} = \mathbf{RSGO}$$

© 2023 Cadence Design Systems, Inc.

Velocity Saturation Parameters

$$\mathrm{THESAT} = \left(\mathrm{THESATO} + \mathrm{THESATL} \cdot \frac{G_{\mathrm{W,E}}}{G_{\mathrm{P,E}}} \cdot \left[\frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}\right]^{\mathrm{THESATLEXP}}\right) \cdot \left(1 + \mathrm{THESATW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}}\right) \cdot \left(1 + \mathrm{THESATLW} \cdot \frac{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}\right)$$

$$\mathrm{STTHESAT} = \mathrm{STTHESATO} + \mathrm{STTHESATL} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathrm{STTHESATW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathrm{STTHESATLW} \cdot \frac{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}$$

$$\mathrm{THESATB} = \mathrm{THESATBO}$$

$$\mathrm{THESATG} = \mathrm{THESATGO}$$

Saturation Voltage Parameter

$$\mathrm{AX} = \frac{\mathrm{AXO}}{1 + \mathrm{AXL} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}}$$

Channel Length Modulation (CLM) Parameters

$$\mathrm{ALP} = \mathrm{ALPL} \cdot \left[\frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}\right]^{\mathrm{ALPLEXP}} \cdot \left(1 + \mathrm{ALPW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}}\right)$$

$$\mathrm{ALP1} = \frac{\mathrm{ALP1L1} \cdot \left[\frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}\right]^{\mathrm{ALP1LEXP}}}{1 + \mathrm{ALP1L2} \cdot \left[\frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}\right]^{\mathrm{ALP1LEXP}+1}} \cdot \left(1 + \mathrm{ALP1W} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}}\right)$$

$$\mathrm{ALP2} = \frac{\mathrm{ALP2L1} \cdot \left[\frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}\right]^{\mathrm{ALP2LEXP}}}{1 + \mathrm{ALP2L2} \cdot \left[\frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}}\right]^{\mathrm{ALP2LEXP}+1}} \cdot \left(1 + \mathrm{ALP2W} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}}\right)$$

$$\mathrm{VP} = \mathrm{VPO}$$

© 2023 Cadence Design Systems, Inc.

Impact Ionization (II) Parameters

$$\mathbf{A1} = \mathbf{A1O} \cdot \left(1 + \mathbf{A1L} \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + \mathbf{A1W} \cdot \frac{W_{EN}}{W_E}\right)$$

$$\mathbf{A2} = \mathbf{A2O}$$

$$\mathbf{STA2} = \mathbf{STA2O}$$

$$\mathbf{A3} = \mathbf{A3O} \cdot \left(1 + \mathbf{A3L} \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + \mathbf{A3W} \cdot \frac{W_{EN}}{W_E}\right)$$

$$\mathbf{A4} = \mathbf{A4O} \cdot \left(1 + \mathbf{A4L} \cdot \frac{L_{EN}}{L_E}\right) \cdot \left(1 + \mathbf{A4W} \cdot \frac{W_{EN}}{W_E}\right)$$

Gate Current Parameters

$$\mathbf{GCO} = \mathbf{GCOO}$$

$$\mathbf{IGINV} = \mathbf{IGINVLW} \cdot \frac{W_E \cdot L_E}{W_{EN} \cdot L_{EN}}$$

$$\mathbf{IGOV} = \mathbf{IGOVW} \cdot \frac{W_E \cdot \mathbf{LOV}}{W_{EN} \cdot L_{EN}}$$

$$\mathbf{IGOVD} = \mathbf{IGOVDW} \cdot \frac{W_E \cdot \mathbf{LOVD}}{W_{EN} \cdot L_{EN}}$$

$$\mathbf{STIG} = \mathbf{STIGO}$$

$$\mathbf{GC2} = \mathbf{GC2O}$$

$$\mathbf{GC3} = \mathbf{GC3O}$$

$$\mathbf{CHIB} = \mathbf{CHIBO}$$

© 2023 Cadence Design Systems, Inc.

Gate-Induced Drain Leakage (GIDL) Parameters

$$\mathbf{AGIDL} = \mathbf{AGIDLW} \cdot \frac{W_{\mathrm{E}} \cdot \mathbf{LOV}}{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}$$

$$\mathbf{AGIDLD} = \mathbf{AGIDLDW} \cdot \frac{W_{\mathrm{E}} \cdot \mathbf{LOVD}}{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}$$

$$\mathbf{BGIDL} = \mathbf{BGIDLO}$$

$$\mathbf{BGIDLD} = \mathbf{BGIDLDO}$$

$$\mathbf{STBGIDL} = \mathbf{STBGIDLO}$$

$$\mathbf{STBGIDLD} = \mathbf{STBGIDLDO}$$

$$\mathbf{CGIDL} = \mathbf{CGIDLO}$$

$$\mathbf{CGIDLD} = \mathbf{CGIDLDO}$$

Charge Model Parameters

$$\mathbf{COX} = \epsilon_{\mathrm{ox}} \cdot \frac{W_{\mathrm{E,CV}} \cdot L_{\mathrm{E,CV}}}{\mathbf{TOX}}$$

$$\mathbf{CGOV} = \epsilon_{\mathrm{ox}} \cdot \frac{W_{\mathrm{E,CV}} \cdot \mathbf{LOV}}{\mathbf{TOXOV}}$$

$$\mathbf{CGOVD} = \epsilon_{\mathrm{ox}} \cdot \frac{W_{\mathrm{E,CV}} \cdot \mathbf{LOVD}}{\mathbf{TOXOVD}}$$

$$\mathbf{CGBOV} = \mathbf{CGBOVL} \cdot \frac{L_{\mathrm{G,CV}}}{L_{\mathrm{EN}}}$$

$$\mathbf{CFR} = \mathbf{CFRW} \cdot \frac{W_{\mathrm{G,CV}}}{W_{\mathrm{EN}}}$$

$$\mathbf{CFRD} = \mathbf{CFRDW} \cdot \frac{W_{\mathrm{G,CV}}}{W_{\mathrm{EN}}}$$

© 2023 Cadence Design Systems, Inc.

Noise Model Parameters

$$L_{\mathrm{noi}} = \mathrm{MAX}\left(1 - \frac{2 \cdot \mathbf{LINTNOI}}{L_{\mathrm{E}}}, 10^{-3}\right)$$

$$L_{\mathrm{red}} = \frac{1}{L_{\mathrm{noi}}^{\mathbf{ALPNOI}}}$$

$$\mathbf{NFA} = L_{\mathrm{red}} \cdot \mathbf{NFALW} \cdot \frac{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}$$

$$\mathbf{NFB} = L_{\mathrm{red}} \cdot \mathbf{NFBLW} \cdot \frac{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}$$

$$\mathbf{NFC} = L_{\mathrm{red}} \cdot \mathbf{NFCLW} \cdot \frac{W_{\mathrm{EN}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{E}} \cdot L_{\mathrm{E}}}$$

$$\mathbf{EF} = \mathbf{EFO}$$

WPE Parameters

$$K_{\mathrm{vthowe}} = \mathbf{KVTHOWEO} + \mathbf{KVTHOWEL} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{KVTHOWEW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{KVTHOWELW} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$K_{\mathrm{uowe}} = \mathbf{KUOWEO} + \mathbf{KUOWEL} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{KUOWEW} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{KUOWELW} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

Note: The parameter equations described in the above section are for Global Model. The equations for the Binning Model are described in the next section with similar headings and names.

Binning Equations

The binning equations are provided as a (phenomenological) alternative to the physical scaling equations for computing local parameters. The physical geometrical scaling rules have been developed to give a good description over the whole geometry range of CMOS technologies. For processes under development, however, it is sometimes useful to have more flexible scaling relation s. In that case on could opt for a binning strategy, where the accuracy with geometry is mostly determined by the number of bins used. The physical scaling rules of Section 3.2 are generally not suitable for binning strategies, since they may result in discontinuities in local parameter values at the bin boundaries. Consequently, special

© 2023 Cadence Design Systems, Inc.

binning geometrical scaling relations have been developed, which guarantee continuity of the resulting local model parameters at the bin boundaries.

Note: The binning equations are only calculated when SWGEO = 2.

Only four different types of binning scaling rules are used, which are based on first order developments of the geometrical scaling rules in terms of LE, 1/LE, WE, and 1/WE (examples below are for a fictitious parameter YYY):

1. Type I

$$\mathbf{YYY} = \mathbf{POYYY} + \mathbf{PLYYY} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWYYY} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWYYY} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

2. Type II

$$\mathbf{YYY} = \mathbf{POYYY} + \mathbf{PLYYY} \cdot \frac{L_{\mathrm{E}}}{L_{\mathrm{EN}}} + \mathbf{PWYYY} \cdot \frac{W_{\mathrm{E}}}{W_{\mathrm{EN}}} + \mathbf{PLWYYY} \cdot \frac{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}$$

3. Type III

$$\mathbf{YYY} = \mathbf{POYYY} + \mathbf{PLYYY} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWYYY} \cdot \frac{W_{\mathrm{E}}}{W_{\mathrm{EN}}} + \mathbf{PLWYYY} \cdot \frac{W_{\mathrm{E}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{EN}} \cdot L_{\mathrm{E}}}$$

4. Type IV (no binning)

$$\mathbf{YYY} = \mathbf{POYYY}$$

In Table 23.1 a survey of the binning type used for each local parameter is given. In some cases where the geometrical scaling rule is constant, the binning rule is chosen to be more flexible.

When using the binning rules above, the binning parameters for one bin can be directly calculated from the local parameter sets of the four corner devices of the bin. This results in a separate parameter set for each bin. The binning scheme ensures that the local parameters are reproduced at the bin corners and that no humps occur in the local parameter values across bin boundaries.

Note: After calculation of the local parameters from the binning rules (and possible applications of the stress equations and well proximity equations), clipping is applied according to Intrinsic Parameters for the model.

© 2023 Cadence Design Systems, Inc.

Table 25-1 Overview of local parameters and binnings type. the third column indicates whether there is a physical geometrical scaling rule for the local parameters.

#	parameter	physical scaling	binning	#	parameter	physical scaling	binning
0	VFB	yes	type I	40	THESATG	no	type I
1	STVFB	yes	type I	41	AX	yes	type I
2	TOX	no	no	42	ALP	yes	type I
3	EPSROX	no	no	43	ALP1	yes	type I
4	NEFF	yes	type I	44	ALP2	yes	type I
5	FACNEFFAC	yes	type I	45	VP	no	no
6	GFACNUD	yes	type I	46	A1	yes	type I
7	VSBNUD	no	no	47	A2	no	no
8	DVSBNUD	no	no	48	STA2	no	no
9	VNSUB	no	no	49	A3	yes	type I
10	NSLP	no	no	50	A4	yes	type I
11	DNSUB	no	no	51	GCO	no	no
12	DPHIB	yes	type I	52	IGINV	yes	type II
13	DELVTAC	yes	type I	53	IGOV	yes	type III
14	NP	yes	type I	54	IGOVD	yes	type III
15	CT	yes	type I	55	STIG	no	no
16	TOXOV	no	no	56	GC2	no	no
17	TOXOVD	no	no	57	GC3	no	no
18	NOV	no	type I	58	CHIB	no	no
19	NOVD	no	Type I	59	AGIDL	yes	type III
20	CF	yes	type I	60	AGIDLD	yes	type III
21	CFB	no	no	61	BGIDL	no	no
22	BETN	yes	type III	62	BGIDLD	no	no
23	STBET	yes	type I	63	STBGIDL	no	no
24	MUE	yes	type I	64	STBGIDLD	no	no
25	STMUE	no	no	65	CGIDL	no	no
26	THEMU	no	no	66	CGIDLD	no	no
27	STTHEMU	no	no	67	COX	yes	type II
28	CS	yes	type I	68	CGOV	yes	type III
29	STCS	no	no	69	CGOVD	yes	type III
30	XCOR	yes	type I	70	CGBOV	yes	type II
31	STXCOR	no	no	71	CFR	yes	type III
32	FETA	no	no	72	CFRD	yes	type III
33	RS	yes	type I	73	FNT	no	no
34	STRS	no	no	74	NFA	yes	type I
35	RSB	no	no	75	NFB	yes	type I
36	RSG	no	no	76	NFC	yes	type I
37	THESAT	yes	type I	77	EF	no	no
38	STTHESAT	yes	type I	78	DTA	no	no
39	THESATB	no	type I				

© 2023 Cadence Design Systems, Inc.

Effective length and width

$$L_{EN} = 10^{-6}$$

$$W_{EN} = 10^{-6}$$

$$\Delta L_{PS} = \mathbf{LVARO} \cdot \left(1 + \mathbf{LVARL} \cdot \frac{L_{EN}}{L}\right)$$

$$\Delta W_{OD} = \mathbf{WVARO} \cdot \left(1 + \mathbf{WVARW} \cdot \frac{W_{EN}}{W_f}\right)$$

$$L_E = L - \Delta L = L + \Delta L_{PS} - 2 \cdot \mathbf{LAP}$$

$$W_E = W_f - \Delta W = W_f + \Delta W_{OD} - 2 \cdot \mathbf{WOT}$$

$$L_{E,CV} = L + \Delta L_{PS} - 2 \cdot \mathbf{LAP} + \mathbf{DLQ}$$

$$W_{E,CV} = W_f + \Delta W_{OD} - 2 \cdot \mathbf{WOT} + \mathbf{DWQ}$$

$$L_{G,CV} = L + \Delta L_{PS} + \mathbf{DLQ}$$

$$W_{G,CV} = W_f + \Delta W_{OD} + \mathbf{DWQ}$$

Note: If the calculated L_E, W_E, $L_{E,CV}$, $W_{E,CV}$, $L_{G,CV}$, or $W_{G,CV}$ is smaller than 1 nm ($10^{?9}$ m), the value is clipped to this lower bound of 1 nm.

© 2023 Cadence Design Systems, Inc.

Process Parameters

$$\mathbf{VFB} = \mathbf{POVFB} + \mathbf{PLVFB} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWVFB} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWVFB} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{STVFB} = \mathbf{POSTVFB} + \mathbf{PLSTVFB} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWSTVFB} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWSTVFB} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{TOX} = \mathbf{POTOX}$$

$$\mathbf{EPSROX} = \mathbf{POEPSROX}$$

$$\mathbf{NEFF} = \mathbf{PONEFF} + \mathbf{PLNEFF} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWNEFF} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWNEFF} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{FACNEFFAC} = \mathbf{POFACNEFFAC} + \mathbf{PLFACNEFFAC} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWFACNEFFAC} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWFACNEFFAC} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

© 2023 Cadence Design Systems, Inc.

$$\mathrm{GFACNUD} = \mathrm{POGFACNUD} + \mathrm{PLGFACNUD} \cdot \frac{L_{EN}}{L_E} + \mathrm{PWGFACNUD} \cdot \frac{W_{EN}}{W_E} + \mathrm{PLWGFACNUD} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathrm{VSBNUD} = \mathrm{POVSBNUD}$$

$$\mathrm{DVSBNUD} = \mathrm{PODVSBNUD}$$

$$\mathrm{VNSUB} = \mathrm{POVNSUB}$$

$$\mathrm{NSLP} = \mathrm{PONSLP}$$

$$\mathrm{DNSUB} = \mathrm{PODNSUB}$$

$$\mathrm{DPHIB} = \mathrm{PODPHIB} + \mathrm{PLDPHIB} \cdot \frac{L_{EN}}{L_E} + \mathrm{PWDPHIB} \cdot \frac{W_{EN}}{W_E} + \mathrm{PLWDPHIB} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathrm{DELVTAC} = \mathrm{PODELVTAC} + \mathrm{PLDELVTAC} \cdot \frac{L_{EN}}{L_E} + \mathrm{PWDELVTAC} \cdot \frac{W_{EN}}{W_E} + \mathrm{PLWDELVTAC} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathrm{NP} = \mathrm{PONP} + \mathrm{PLNP} \cdot \frac{L_{EN}}{L_E} + \mathrm{PWNP} \cdot \frac{W_{EN}}{W_E} + \mathrm{PLWNP} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathrm{CT} = \mathrm{POCT} + \mathrm{PLCT} \cdot \frac{L_{EN}}{L_E} + \mathrm{PWCT} \cdot \frac{W_{EN}}{W_E} + \mathrm{PLWCT} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathrm{TOXOV} = \mathrm{POTOXOV}$$

$$\mathrm{TOXOVD} = \mathrm{POTOXOVD}$$

$$\mathrm{NOV} = \mathrm{PONOV} + \mathrm{PLNOV} \cdot \frac{L_{EN}}{L_E} + \mathrm{PWNOV} \cdot \frac{W_{EN}}{W_E} + \mathrm{PLWNOV} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathrm{NOVD} = \mathrm{PONOVD} + \mathrm{PLNOVD} \cdot \frac{L_{EN}}{L_E} + \mathrm{PWNOVD} \cdot \frac{W_{EN}}{W_E} + \mathrm{PLWNOVD} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

DIBL Parameters

$$\mathrm{CF} = \mathrm{POCF} + \mathrm{PLCF} \cdot \frac{L_{EN}}{L_E} + \mathrm{PWCF} \cdot \frac{W_{EN}}{W_E} + \mathrm{PLWCF} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E}$$

$$\mathrm{CFB} = \mathrm{POCFB}$$

© 2023 Cadence Design Systems, Inc.

Mobility Parameters

$$\mathbf{BETN} = \frac{W_\mathrm{E}}{L_\mathrm{E}} \cdot \left(\mathbf{POBETN} + \mathbf{PLBETN} \cdot \frac{L_\mathrm{EN}}{L_\mathrm{E}} + \mathbf{PWBETN} \cdot \frac{W_\mathrm{EN}}{W_\mathrm{E}} + \mathbf{PLWBETN} \cdot \frac{L_\mathrm{EN} \cdot W_\mathrm{EN}}{L_\mathrm{E} \cdot W_\mathrm{E}} \right)$$

$$\mathbf{STBET} = \mathbf{POSTBET} + \mathbf{PLSTBET} \cdot \frac{L_\mathrm{EN}}{L_\mathrm{E}} + \mathbf{PWSTBET} \cdot \frac{W_\mathrm{EN}}{W_\mathrm{E}} + \mathbf{PLWSTBET} \cdot \frac{L_\mathrm{EN} \cdot W_\mathrm{EN}}{L_\mathrm{E} \cdot W_\mathrm{E}}$$

$$\mathbf{MUE} = \mathbf{POMUE} + \mathbf{PLMUE} \cdot \frac{L_\mathrm{EN}}{L_\mathrm{E}} + \mathbf{PWMUE} \cdot \frac{W_\mathrm{EN}}{W_\mathrm{E}} + \mathbf{PLWMUE} \cdot \frac{L_\mathrm{EN} \cdot W_\mathrm{EN}}{L_\mathrm{E} \cdot W_\mathrm{E}}$$

$$\mathbf{STMUE} = \mathbf{POSTMUE}$$

$$\mathbf{THEMU} = \mathbf{POTHEMU}$$

$$\mathbf{STTHEMU} = \mathbf{POSTTHEMU}$$

$$\mathbf{CS} = \mathbf{POCS} + \mathbf{PLCS} \cdot \frac{L_\mathrm{EN}}{L_\mathrm{E}} + \mathbf{PWCS} \cdot \frac{W_\mathrm{EN}}{W_\mathrm{E}} + \mathbf{PLWCS} \cdot \frac{L_\mathrm{EN} \cdot W_\mathrm{EN}}{L_\mathrm{E} \cdot W_\mathrm{E}}$$

$$\mathbf{STCS} = \mathbf{POSTCS}$$

$$\mathbf{XCOR} = \mathbf{POXCOR} + \mathbf{PLXCOR} \cdot \frac{L_\mathrm{EN}}{L_\mathrm{E}} + \mathbf{PWXCOR} \cdot \frac{W_\mathrm{EN}}{W_\mathrm{E}} + \mathbf{PLWXCOR} \cdot \frac{L_\mathrm{EN} \cdot W_\mathrm{EN}}{L_\mathrm{E} \cdot W_\mathrm{E}}$$

$$\mathbf{STXCOR} = \mathbf{POSTXCOR}$$

$$\mathbf{FETA} = \mathbf{POFETA}$$

© 2023 Cadence Design Systems, Inc.

Series Resistance Parameters

$$\mathbf{RS} = \mathbf{PORS} + \mathbf{PLRS} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWRS} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWRS} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{STRS} = \mathbf{POSTRS}$$

$$\mathbf{RSB} = \mathbf{PORSB}$$

$$\mathbf{RSG} = \mathbf{PORSG}$$

Velocity Saturation Parameters

$$\mathbf{THESAT} = \mathbf{POTHESAT} + \mathbf{PLTHESAT} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWTHESAT} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWTHESAT} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{STTHESAT} = \mathbf{POSTTHESAT} + \mathbf{PLSTTHESAT} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWSTTHESAT} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWSTTHESAT} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{THESATB} = \mathbf{POTHESATB} + \mathbf{PLTHESATB} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWTHESATB} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWTHESATB} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{THESATG} = \mathbf{POTHESATG} + \mathbf{PLTHESATG} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWTHESATG} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWTHESATG} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

© 2023 Cadence Design Systems, Inc.

Saturation Voltage Parameters

$$\mathbf{AX} = \mathbf{POAX} + \mathbf{PLAX} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWAX} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWAX} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

Channel Length Modulation (CLM) Parameters

$$\mathbf{ALP} = \mathbf{POALP} + \mathbf{PLALP} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWALP} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWALP} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{ALP1} = \mathbf{POALP1} + \mathbf{PLALP1} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWALP1} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWALP1} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{ALP2} = \mathbf{POALP2} + \mathbf{PLALP2} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWALP2} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWALP2} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{VP} = \mathbf{POVP}$$

Impact Ionization (II) Parameters

$$\mathbf{A1} = \mathbf{POA1} + \mathbf{PLA1} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWA1} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWA1} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{A2} = \mathbf{POA2}$$

$$\mathbf{STA2} = \mathbf{POSTA2}$$

$$\mathbf{A3} = \mathbf{POA3} + \mathbf{PLA3} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWA3} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWA3} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{A4} = \mathbf{POA4} + \mathbf{PLA4} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWA4} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWA4} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

© 2023 Cadence Design Systems, Inc.

Gate Current Parameters

$$\mathbf{GCO} = \mathbf{POGCO}$$

$$\mathbf{IGINV} = \mathbf{POIGINV} + \mathbf{PLIGINV} \cdot \frac{L_\mathrm{E}}{L_\mathrm{EN}} + \mathbf{PWIGINV} \cdot \frac{W_\mathrm{E}}{W_\mathrm{EN}} + \mathbf{PLWIGINV} \cdot \frac{L_\mathrm{E} \cdot W_\mathrm{E}}{L_\mathrm{EN} \cdot W_\mathrm{EN}}$$

$$\mathbf{IGOV} = \mathbf{POIGOV} + \mathbf{PLIGOV} \cdot \frac{L_\mathrm{EN}}{L_\mathrm{E}} + \mathbf{PWIGOV} \cdot \frac{W_\mathrm{E}}{W_\mathrm{EN}} + \mathbf{PLWIGOV} \cdot \frac{W_\mathrm{E} \cdot L_\mathrm{EN}}{W_\mathrm{EN} \cdot L_\mathrm{E}}$$

$$\mathbf{IGOVD} = \mathbf{POIGOVD} + \mathbf{PLIGOVD} \cdot \frac{L_\mathrm{EN}}{L_\mathrm{E}} + \mathbf{PWIGOVD} \cdot \frac{W_\mathrm{E}}{W_\mathrm{EN}} + \mathbf{PLWIGOVD} \cdot \frac{W_\mathrm{E} \cdot L_\mathrm{EN}}{W_\mathrm{EN} \cdot L_\mathrm{E}}$$

$$\mathbf{STIG} = \mathbf{POSTIG}$$

$$\mathbf{GC2} = \mathbf{POGC2}$$

$$\mathbf{GC3} = \mathbf{POGC3}$$

$$\mathbf{CHIB} = \mathbf{POCHIB}$$

© 2023 Cadence Design Systems, Inc.

Gate Induced Drain Leakage (GIDL) Parameters

$$\mathbf{AGIDL} = \mathbf{POAGIDL} + \mathbf{PLAGIDL} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWAGIDL} \cdot \frac{W_{\mathrm{E}}}{W_{\mathrm{EN}}} + \mathbf{PLWAGIDL} \cdot \frac{W_{\mathrm{E}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{EN}} \cdot L_{\mathrm{E}}}$$

$$\mathbf{AGIDLD} = \mathbf{POAGIDLD} + \mathbf{PLAGIDLD} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWAGIDLD} \cdot \frac{W_{\mathrm{E}}}{W_{\mathrm{EN}}} + \mathbf{PLWAGIDLD} \cdot \frac{W_{\mathrm{E}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{EN}} \cdot L_{\mathrm{E}}}$$

$$\mathbf{BGIDL} = \mathbf{POBGIDL}$$

$$\mathbf{BGIDLD} = \mathbf{POBGIDLD}$$

$$\mathbf{STBGIDL} = \mathbf{POSTBGIDL}$$

$$\mathbf{STBGIDLD} = \mathbf{POSTBGIDLD}$$

$$\mathbf{CGIDL} = \mathbf{POCGIDL}$$

$$\mathbf{CGIDLD} = \mathbf{POCGIDLD}$$

© 2023 Cadence Design Systems, Inc.

Charge Model Parameters

$$\mathbf{COX} = \mathbf{POCOX} + \mathbf{PLCOX} \cdot \frac{L_{\mathrm{E,CV}}}{L_{\mathrm{EN}}} + \mathbf{PWCOX} \cdot \frac{W_{\mathrm{E,CV}}}{W_{\mathrm{EN}}} + \mathbf{PLWCOX} \cdot \frac{L_{\mathrm{E,CV}} \cdot W_{\mathrm{E,CV}}}{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}$$

$$\mathbf{CGOV} = \mathbf{POCGOV} + \mathbf{PLCGOV} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E,CV}}} + \mathbf{PWCGOV} \cdot \frac{W_{\mathrm{E,CV}}}{W_{\mathrm{EN}}} + \mathbf{PLWCGOV} \cdot \frac{W_{\mathrm{E,CV}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{EN}} \cdot L_{\mathrm{E,CV}}}$$

$$\mathbf{CGOVD} = \mathbf{POCGOVD} + \mathbf{PLCGOVD} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E,CV}}} + \mathbf{PWCGOVD} \cdot \frac{W_{\mathrm{E,CV}}}{W_{\mathrm{EN}}} + \mathbf{PLWCGOVD} \cdot \frac{W_{\mathrm{E,CV}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{EN}} \cdot L_{\mathrm{E,CV}}}$$

$$\mathbf{CGBOV} = \mathbf{POCGBOV} + \mathbf{PLCGBOV} \cdot \frac{L_{\mathrm{G,CV}}}{L_{\mathrm{EN}}} + \mathbf{PWCGBOV} \cdot \frac{W_{\mathrm{G,CV}}}{W_{\mathrm{EN}}} + \mathbf{PLWCGBOV} \cdot \frac{L_{\mathrm{G,CV}} \cdot W_{\mathrm{G,CV}}}{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}$$

$$\mathbf{CFR} = \mathbf{POCFR} + \mathbf{PLCFR} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{G,CV}}} + \mathbf{PWCFR} \cdot \frac{W_{\mathrm{G,CV}}}{W_{\mathrm{EN}}} + \mathbf{PLWCFR} \cdot \frac{W_{\mathrm{G,CV}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{EN}} \cdot L_{\mathrm{G,CV}}}$$

$$\mathbf{CFRD} = \mathbf{POCFRD} + \mathbf{PLCFRD} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{G,CV}}} + \mathbf{PWCFRD} \cdot \frac{W_{\mathrm{G,CV}}}{W_{\mathrm{EN}}} + \mathbf{PLWCFRD} \cdot \frac{W_{\mathrm{G,CV}} \cdot L_{\mathrm{EN}}}{W_{\mathrm{EN}} \cdot L_{\mathrm{G,CV}}}$$

© 2023 Cadence Design Systems, Inc.

Noise Model Parameters

$$\mathbf{FNT} = \mathbf{POFNT}$$

$$\mathbf{NFA} = \mathbf{PONFA} + \mathbf{PLNFA} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWNFA} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWNFA} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{NFB} = \mathbf{PONFB} + \mathbf{PLNFB} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWNFB} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWNFB} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{NFC} = \mathbf{PONFC} + \mathbf{PLNFC} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWNFC} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWNFC} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$\mathbf{EF} = \mathbf{POEF}$$

WPE Parameters

$$K_{\mathrm{vthowe}} = \mathbf{POKVTHOWE} + \mathbf{PLKVTHOWE} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWKVTHOWE} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWKVTHOWE} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

$$K_{\mathrm{uowe}} = \mathbf{POKUOWE} + \mathbf{PLKUOWE} \cdot \frac{L_{\mathrm{EN}}}{L_{\mathrm{E}}} + \mathbf{PWKUOWE} \cdot \frac{W_{\mathrm{EN}}}{W_{\mathrm{E}}} + \mathbf{PLWKUOWE} \cdot \frac{L_{\mathrm{EN}} \cdot W_{\mathrm{EN}}}{L_{\mathrm{E}} \cdot W_{\mathrm{E}}}$$

Parasitic resistances

PSP model contains a network of parasitic elements: a gate resistance, two diffusion resistances for source and drain, and four bulk resistances.

Note: The junction diodes are no longer directly connected to the bulk terminal of the intrinsic MOS-transistor.

The complete circuit is shown in Figure 25-2. At this moment, only the gate resistance is scaled with geometry (facilitating the implementation of multi-finger devices).

© 2023 Cadence Design Systems, Inc.

Note: The resistance equations are calculated when **SWGEO** = 1 or 2.

$$L_{\mathrm{f}} = L + \Delta L_{\mathrm{PS}}$$

$$L_{\mathrm{sil,f}} = L_{\mathrm{f}} + \mathbf{DLSIL}$$

$$W_{\mathrm{E,f}} = W_{\mathrm{f}} + \Delta W_{\mathrm{OD}}$$

$$X_{\mathrm{GWE}} = \mathbf{XGW} - 0.5 \cdot \Delta W_{\mathrm{OD}}$$

$$\mathbf{RG} = \mathbf{RGO} + \frac{1}{\mathbf{NF}} \cdot \left[\frac{\mathbf{RSHG} \cdot \left(\frac{W_{\mathrm{E,f}}}{3 \cdot \mathbf{NGCON}} + X_{\mathrm{GWE}} \right)}{\mathbf{NGCON} \cdot L_{\mathrm{sil,f}}} + \frac{\mathbf{RINT} + \mathbf{RVPOLY}}{W_{\mathrm{E,f}} \cdot L_{\mathrm{f}}} \right]$$

$$\mathbf{RSE} = \mathbf{NRS} \cdot \mathbf{RSH}$$

$$\mathbf{RDE} = \mathbf{NRD} \cdot \mathbf{RSH}$$

$$\mathbf{RBULK} = \mathbf{RBULKO}$$

$$\mathbf{RWELL} = \mathbf{RWELLO}$$

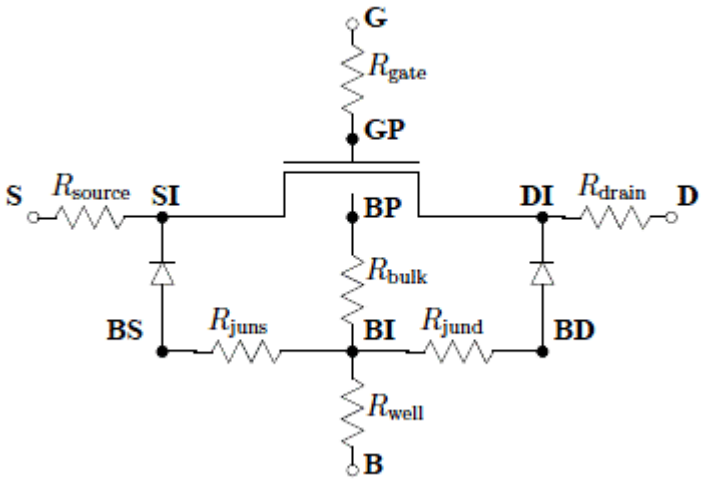
$$\mathbf{RJUNS} = \mathbf{RJUNSO}$$

$$\mathbf{RJUND} = \mathbf{RJUNDO}$$

Note: The values of Lf, Lsil,f , WE,f and XGWE are clipped to a minimum value of 1 nm. The calculated local parameters are subject to the boundaries specified in next section.

© 2023 Cadence Design Systems, Inc.

Figure 25-2 Parasitics Circuit



Stress effects

The stress model of BSIM4.4.0 has been adopted in PSP without any modifications, except for two changes:

1. In the original BSIM parameter names all zeros have been replaced by “O”s, in order to comply with PSP conventions.
2. The BSIM parameters STK2 and LODK2 are not available in PSP. Some trivial conversion of parameters BSIM-PSP is still necessary.

The local PSP parameters affected by the stress equations are **BETN**, **THESAT**, **VFB**, and **CF**. Calculation of **SA** and **SB** for irregular layouts is given separately.

Note:

- After modification of the local parameters by the stress equations, clipping is applied according to Section “Intrinsic Parameters for the model”.
- If both SA and SB are set to 0, the stress-equations are not computed.
- The stress equations are calculated when SWGEO = 1 or 2.

© 2023 Cadence Design Systems, Inc.

Layout effects for multi-finger devices

For multi-finger devices, effective values SA_{eff} and SB_{eff} for the instance parameters are calculated.

$$\frac{1}{\mathbf{SA}_{\text{eff}} + 0.5 \cdot L} = \frac{1}{\mathbf{NF}} \cdot \sum_{i=0}^{\mathbf{NF}-1} \frac{1}{\mathbf{SA} + 0.5 \cdot L + i \cdot (\mathbf{SD} + L)}$$

$$\frac{1}{\mathbf{SB}_{\text{eff}} + 0.5 \cdot L} = \frac{1}{\mathbf{NF}} \cdot \sum_{i=0}^{\mathbf{NF}-1} \frac{1}{\mathbf{SB} + 0.5 \cdot L + i \cdot (\mathbf{SD} + L)}$$

Layout effects for regular shapes

$$R_{\text{A}} = \frac{1}{\mathbf{SA}_{\text{eff}} + 0.5 \cdot L}$$

$$R_{\text{B}} = \frac{1}{\mathbf{SB}_{\text{eff}} + 0.5 \cdot L}$$

$$R_{\text{A,ref}} = \frac{1}{\mathbf{SAREF} + 0.5 \cdot L}$$

$$R_{\text{B,ref}} = \frac{1}{\mathbf{SBREF} + 0.5 \cdot L}$$

© 2023 Cadence Design Systems, Inc.

Figure 25-3 A typical layout of multi-finger devices with additional instance parameters SD.

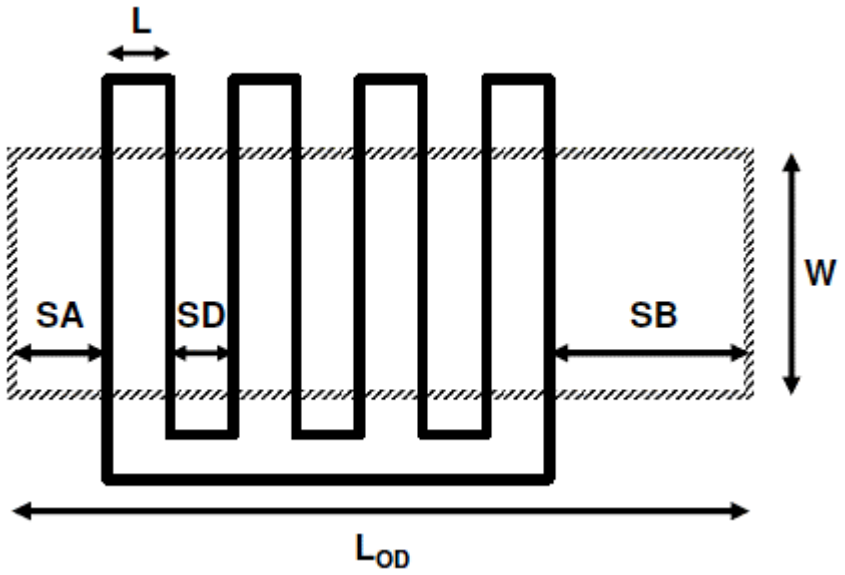
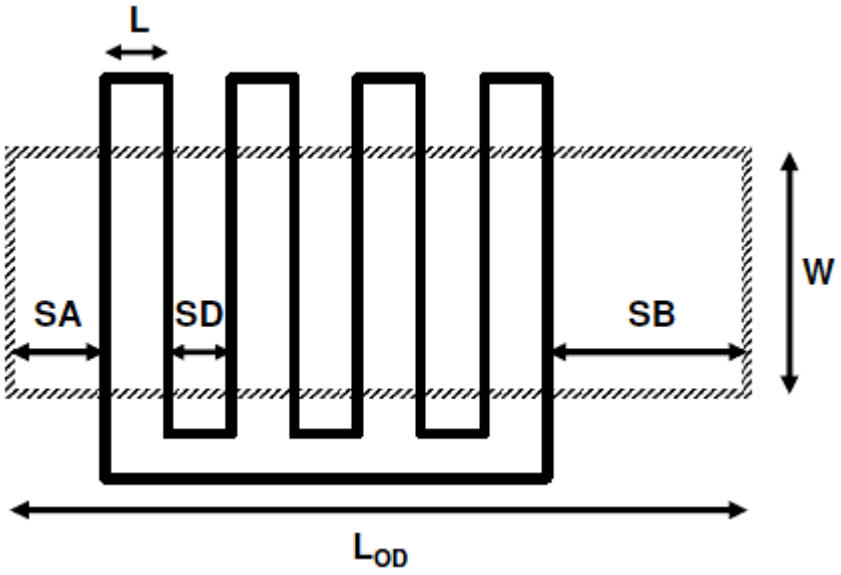


Figure 25-4 Typical layout of a MOSFET. LOD = SA + SB + L, where OD is the active region definition.



© 2023 Cadence Design Systems, Inc.

Parameter Modifications

Mobility related equations

$$K_{\mathrm{u0}} = \left(1 + \frac{\mathbf{LKUO}}{(L + \Delta L_{\mathrm{PS}})^{\mathbf{LLODKUO}}} + \frac{\mathbf{WKUO}}{(W_{\mathrm{f}} + \Delta W_{\mathrm{OD}} + \mathbf{WLOD})^{\mathbf{WLODKUO}}} + \frac{\mathbf{PKUO}}{(L + \Delta L_{\mathrm{PS}})^{\mathbf{LLODKUO}} \cdot (W_{\mathrm{f}} + \Delta W_{\mathrm{OD}} + \mathbf{WLOD})^{\mathbf{WLODKUO}}}\right) \cdot \left[1 + \mathbf{TKUO} \cdot \left(\frac{T_{\mathrm{KD}}}{T_{\mathrm{KR}}} - 1\right)\right]$$

$$\rho_{\beta} = \frac{\mathbf{KUO}}{K_{\mathrm{u0}}} \cdot (R_{\mathrm{A}} + R_{\mathrm{B}})$$

$$\rho_{\beta,\mathrm{ref}} = \frac{\mathbf{KUO}}{K_{\mathrm{u0}}} \cdot (R_{\mathrm{A,ref}} + R_{\mathrm{B,ref}})$$

$$\mathbf{BETN} = \frac{1 + \rho_{\beta}}{1 + \rho_{\beta,\mathrm{ref}}} \cdot \mathbf{BETN}_{\mathrm{ref}}$$

$$\mathbf{THESAT} = \frac{1 + \rho_{\beta}}{1 + \rho_{\beta,\mathrm{ref}}} \cdot \frac{1 + \mathbf{KVSAT} \cdot \rho_{\beta,\mathrm{ref}}}{1 + \mathbf{KVSAT} \cdot \rho_{\beta}} \cdot \mathbf{THESAT}_{\mathrm{ref}}$$

© 2023 Cadence Design Systems, Inc.

Threshold Voltage related equations

$$K_{\mathrm{vth0}} = 1 + \frac{\mathbf{LKVTHO}}{(L + \Delta L_{\mathrm{PS}})^{\mathbf{LLODVTH}}} + \frac{\mathbf{WKVTHO}}{(W_{\mathrm{f}} + \Delta W_{\mathrm{OD}} + \mathbf{WLOD})^{\mathbf{WLODVTH}}} + \frac{\mathbf{PKVTHO}}{(L + \Delta L_{\mathrm{PS}})^{\mathbf{LLODVTH}} \cdot (W_{\mathrm{f}} + \Delta W_{\mathrm{OD}} + \mathbf{WLOD})^{\mathbf{WLODVTH}}}$$

$$\Delta R = R_{\mathrm{A}} + R_{\mathrm{B}} - R_{\mathrm{A,ref}} - R_{\mathrm{B,ref}}$$

$$\mathbf{VFB} = \mathbf{VFB}_{\mathrm{ref}} + \mathbf{KVTHO} \cdot \frac{\Delta R}{K_{\mathrm{vth0}}}$$

$$\mathbf{CF} = \mathbf{CF}_{\mathrm{ref}} + \mathbf{STETAO} \cdot \frac{\Delta R}{K_{\mathrm{vth0}}^{\mathbf{LODETAO}}}$$

Well proximity effects

The well proximity effect (WPE) model from BSIM4.5.0 has been adopted in PSP with two changes relative to BSIM4.5.0: (1) in the original BSIM parameter names all zeros have been replaced by `O's in order to comply with PSP naming convention and (2) the BSIM parameter K2WE is not available in PSP. Except for some trivial conversion of parameters BSIM-PSP, WPE parameters from BSIM can be used directly in PSP.

The local PSP parameters affected by the WPE equations are VFB and BETN.

Note:

- After modification of the local parameters by the WPE equations, clipping is applied according to Section “Intrinsic Parameters for the model”.
- If SCA, SCB, SCC and SC are all set to 0, the WPE equations are not computed.
- The WPE equations are calculated when SWGEO = 1 or 2.

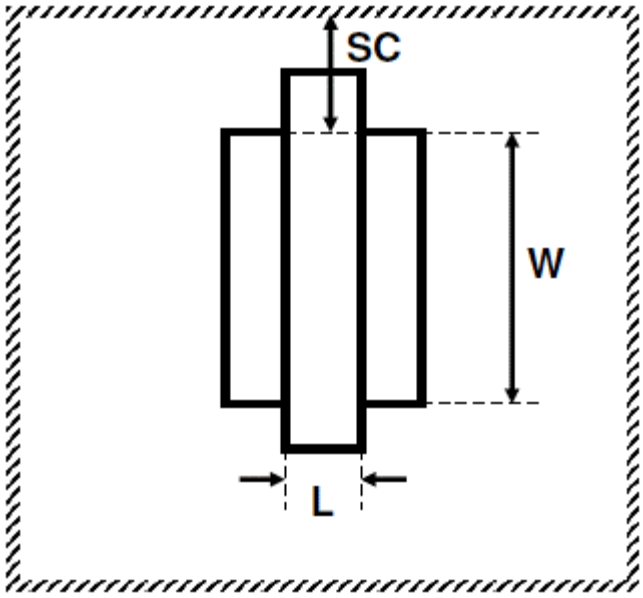
Parameters for pre-layout simulation

If **SCA** = **SCB** = **SCC** = 0 and **SC** > 0, **SCA**, **SCB**, and **SCC** will be computed from **SC** as shown below. Here, **SC** should be taken as the distance to the nearest well edge (see Figure below). If any of the parameters **SCA**, **SCB**, or **SCC** is positive, all three values as supplied will be used and **SC** will be ignored.

© 2023 Cadence Design Systems, Inc.

If **SCA** = **SCB** = **SCC** = 0 and **SC** > 0

Figure 25-5 A layout of MOS devices for pre-layout simulation using estimated value for SC.



$$\mathbf{SCB} = \frac{1}{W_f \cdot \mathbf{SCREF}} \cdot \left[\frac{\mathbf{SCREF}}{10} \cdot \mathbf{SC} \cdot \exp\left(-10 \cdot \frac{\mathbf{SC}}{\mathbf{SCREF}}\right) + \frac{\mathbf{SCREF}^2}{100} \cdot \exp\left(-10 \cdot \frac{\mathbf{SC}}{\mathbf{SCREF}}\right) \right.$$

$$- \frac{\mathbf{SCREF}}{10} \cdot (\mathbf{SC} + W_f) \cdot \exp\left(-10 \cdot \frac{\mathbf{SC} + W_f}{\mathbf{SCREF}}\right)$$

$$\left. - \frac{\mathbf{SCREF}}{10} \cdot (\mathbf{SC} + W_f) \cdot \exp\left(-10 \cdot \frac{\mathbf{SC} + W_f}{\mathbf{SCREF}}\right) \right.$$

$$\left. - \frac{\mathbf{SCREF}^2}{100} \cdot \exp\left(-10 \cdot \frac{\mathbf{SC} + W_f}{\mathbf{SCREF}}\right) \right]$$

$$\mathbf{SCC} = \frac{1}{W_f \cdot \mathbf{SCREF}} \cdot \left[\frac{\mathbf{SCREF}}{20} \cdot \mathbf{SC} \cdot \exp\left(-20 \cdot \frac{\mathbf{SC}}{\mathbf{SCREF}}\right) + \frac{\mathbf{SCREF}^2}{400} \cdot \exp\left(-20 \cdot \frac{\mathbf{SC}}{\mathbf{SCREF}}\right) \right.$$

$$\left. - \frac{\mathbf{SCREF}}{20} \cdot (\mathbf{SC} + W_f) \cdot \exp\left(-20 \cdot \frac{\mathbf{SC} + W_f}{\mathbf{SCREF}}\right) \right.$$

© 2023 Cadence Design Systems, Inc.

Calculation of parameter modifications

The calculation of K_{vthowe} and K_{uowe} is given in Sections for Global Model or Binning Model.

$$\mathbf{VFB} = \mathbf{VFB}_{\mathrm{ref}} + K_{\mathrm{vthowe}} \cdot (\mathbf{SCA} + \mathbf{WEB} \cdot \mathbf{SCB} + \mathbf{WEC} \cdot \mathbf{SCC})$$

$$\mathbf{BETN} = \mathbf{BETN}_{\mathrm{ref}} \cdot [1 + K_{\mathrm{uowe}} \cdot (\mathbf{SCA} + \mathbf{WEB} \cdot \mathbf{SCB} + \mathbf{WEC} \cdot \mathbf{SCC})]$$

Asymmetric junctions

From PSP 102.3 onwards, asymmetric junction can be modeled in PSP. This includes asymmetric source-bulk and drain-bulk junctions, GIDL/GISL, overlap gate currents, overlap capacitances and outer fringe capacitances. The asymmetric junction model can be switched on by means of the parameter SWJUNASYM.

Note: If SWJUNASYM = 1, the new parameters for the drain side are used all together.

Those whose values are not explicitly specified in the model card are set to their default value, not to their counterparts for the source side. In other words, it is not possible to activate the parameters for the drain side on a one-by-one basis. The physical scaling and binning rules to calculate the related local parameters for the drain side are given separately in this chapter.

© 2023 Cadence Design Systems, Inc.

If **SWJUNASYM** = 0, the related parameters for the drain side are ignored. Effectively, the following assignments are applied before evaluation of the calculations described in the next section.

If SWJUNASYM = 0:

TOXOVD = TOXOV

NOVD = NOV

AGIDLD = AGIDL

BGIDLD = BGIDL

STBGIDLD = STBGIDL

CGIDLD = CGIDL

IGOVD = IGOV

CGOVD = CGOV

CFRD = CFR

RSHD = RSH

PSP 103 Model Equations

Internal Parameters (including Temperature Scaling)

In this section, bias-independent internal parameters are calculated, including temperature scaling. These parameters are computed from local parameters. Local parameters are (as usual) denoted by capital characters in bold font, whereas the internal parameters are denoted by symbols in bold font.

© 2023 Cadence Design Systems, Inc.

Transistor temperature

$$T_{\mathrm{KR}} = T_0 + \mathbf{TR}$$

$$T_{\mathrm{KD}} = T_0 + T_{\mathrm{A}} + \mathbf{DTA}$$

$$\Delta T = T_{\mathrm{KD}} - T_{\mathrm{KR}}$$

$$\phi_{\mathbf{T}} = \frac{k_{\mathrm{B}} \cdot T_{\mathrm{KD}}}{q}$$

© 2023 Cadence Design Systems, Inc.

Local process parameters

$$\phi_{\mathbf{T}}^{*} = \phi_{\mathbf{T}} \cdot \left(1 + \mathbf{CT} \cdot \frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}}\right)$$

$$V_{\mathbf{FB}} = \mathbf{VFB} + \mathbf{STVFB} \cdot \Delta T \cdot \left(1 + \mathbf{ST2VFB} \cdot \Delta T\right) + \mathbf{DELVTO}$$

$$E_{\mathrm{g}}/q = 1.179 - 9.025 \cdot 10^{-5} \cdot T_{\mathrm{KD}} - 3.05 \cdot 10^{-7} \cdot {T_{\mathrm{KD}}}^{2}$$

$$r_{\mathrm{T}} = \left(1.045 + 4.5 \cdot 10^{-4} \cdot T_{\mathrm{KD}}\right) \cdot \left(0.523 + 1.4 \cdot 10^{-3} \cdot T_{\mathrm{KD}} - 1.48 \cdot 10^{-6} \cdot {T_{\mathrm{KD}}}^{2}\right)$$

$$n_{\mathrm{i}} = 2.5 \cdot 10^{25} \cdot {r_{\mathrm{T}}}^{3/4} \cdot \left(T_{\mathrm{KD}}/300\right)^{3/2} \cdot \exp\left(-\frac{E_{\mathrm{g}}/q}{2 \cdot \phi_{\mathbf{T}}}\right)$$

$$\phi_{\mathrm{B,dc}}^{\mathrm{cl}} = \mathrm{MAX}\left(\mathbf{DPHIB} + 2 \cdot \phi_{\mathbf{T}} \cdot \ln\left[\mathbf{NEFF}/n_{\mathrm{i}}\right], 0.05\right)$$

$$N_{\mathrm{eff,ac}} = \mathrm{MIN}[\mathrm{MAX}(\mathbf{FACNEFFAC} \cdot \mathbf{NEFF}, 10^{20}), 10^{26}]$$

$$\phi_{\mathrm{B,ac}}^{\mathrm{cl}} = \mathrm{MAX}\left(\mathbf{DPHIB} + \mathbf{DELVTAC} + 2 \cdot \phi_{\mathbf{T}} \cdot \ln\left[N_{\mathrm{eff,ac}}/n_{\mathrm{i}}\right], 0.05\right)$$

$$\epsilon_{\mathrm{ox}} = \mathbf{EPSROX} \cdot \epsilon_{0}$$

$$C_{\mathrm{ox}} = \epsilon_{\mathrm{ox}}/\mathbf{TOX}$$

$$\epsilon_{\mathrm{Si}} = \epsilon_{\mathrm{r,Si}} \cdot \epsilon_{0}$$

$$\gamma_{0,\mathrm{dc}} = \sqrt{2 \cdot q \cdot \epsilon_{\mathrm{Si}} \cdot \mathbf{NEFF}}/C_{\mathrm{ox}}$$

$$\gamma_{0,\mathrm{ac}} = \sqrt{2 \cdot q \cdot \epsilon_{\mathrm{Si}} \cdot N_{\mathrm{eff,ac}}}/C_{\mathrm{ox}}$$

$$G_{0,\mathrm{dc}}^{\mathrm{cl}} = \gamma_{0,\mathrm{dc}}/\sqrt{\phi_{\mathbf{T}}}$$

$$G_{0,\mathrm{ac}}^{\mathrm{cl}} = \gamma_{0,\mathrm{ac}}/\sqrt{\phi_{\mathbf{T}}}$$

© 2023 Cadence Design Systems, Inc.

Polysilicon depletion parameter

$$k_{\mathbf{P}} = \begin{cases} \text{if } \mathbf{NP} = 0 & \left\{ k_{\mathbf{P}} = 0 \right. \\ \text{if } \mathbf{NP} > 0 & \begin{cases} \mathrm{NP}_1 = \mathrm{MAX}(\mathbf{NP},\, 8 \cdot 10^7 / \mathbf{TOX}^2) \\ \mathrm{NP}_2 = \mathrm{MAX}(\mathrm{NP}_1,\, 5 \cdot 10^{24}) \\ k_{\mathbf{P}} = 2 \cdot \phi_{\mathbf{T}} \cdot C_{\mathrm{ox}}^2 / (q \cdot \epsilon_{\mathrm{Si}} \cdot \mathrm{NP}_2) \end{cases} \end{cases}$$

Quantum-mechanical correction parameters

$$q_{\mathbf{lin}} = 10 \cdot \phi_{\mathbf{T}}$$

$$q_{\mathbf{q}} = \begin{cases} 0.4 \cdot \mathbf{QMC} \cdot QM_{\mathrm{N}} \cdot C_{\mathrm{ox}}^{2/3} & \text{for NMOS} \\ 0.4 \cdot \mathbf{QMC} \cdot QM_{\mathrm{P}} \cdot C_{\mathrm{ox}}^{2/3} & \text{for PMOS} \end{cases}$$

$$q_{\mathrm{b0,dc}} = \gamma_{0,\mathrm{dc}} \cdot \sqrt{\phi_{\mathrm{B,dc}}^{\mathrm{cl}}}$$

$$q_{\mathrm{b0,ac}} = \gamma_{0,\mathrm{ac}} \cdot \sqrt{\phi_{\mathrm{B,ac}}^{\mathrm{cl}}}$$

$$\phi_{\mathbf{B},\mathrm{dc}} = \phi_{\mathrm{B,dc}}^{\mathrm{cl}} + 0.75 \cdot q_{\mathbf{q}} \cdot q_{\mathrm{b0,dc}}^{2/3}$$

$$\phi_{\mathbf{B},\mathrm{ac}} = \phi_{\mathrm{B,ac}}^{\mathrm{cl}} + 0.75 \cdot q_{\mathbf{q}} \cdot q_{\mathrm{b0,ac}}^{2/3}$$

$$G_{\mathbf{0},\mathrm{dc}} = G_{0,\mathrm{dc}}^{\mathrm{cl}} \cdot \left(1 + q_{\mathbf{q}} \cdot q_{\mathrm{b0,dc}}^{-1/3}\right)$$

$$G_{\mathbf{0},\mathrm{ac}} = G_{0,\mathrm{ac}}^{\mathrm{cl}} \cdot \left(1 + q_{\mathbf{q}} \cdot q_{\mathrm{b0,ac}}^{-1/3}\right)$$

© 2023 Cadence Design Systems, Inc.

VSB-clipping parameters

$$\phi_{\mathrm{X,dc}} = 0.95 \cdot \phi_{\mathrm{B,dc}}$$

$$\phi_{\mathrm{X,ac}} = 0.95 \cdot \phi_{\mathrm{B,ac}}$$

$$a_{\phi,\mathrm{dc}} = 2.5 \cdot 10^{-3} \cdot \phi^2_{\mathrm{B,dc}}$$

$$a_{\phi,\mathrm{ac}} = 2.5 \cdot 10^{-3} \cdot \phi^2_{\mathrm{B,ac}}$$

$$b_{\phi,\mathrm{dc}} = 2.5 \cdot 10^{-3} \cdot \phi^2_{\mathrm{B,dc}}$$

$$b_{\phi,\mathrm{ac}} = 2.5 \cdot 10^{-3} \cdot \phi^2_{\mathrm{B,ac}}$$

$$\phi^{\star}_{\mathrm{X,dc}} = 0.5 \cdot \sqrt{b_{\phi,\mathrm{dc}}}$$

$$\phi^{\star}_{\mathrm{X,ac}} = 0.5 \cdot \sqrt{b_{\phi,\mathrm{ac}}}$$

$$\phi^{\dagger}_{\mathrm{X,dc}} = \mathrm{MINA}\left(\phi_{\mathrm{X,dc}} - \phi^{\star}_{\mathrm{X,dc}},\, 0,\, a_{\phi,\mathrm{dc}}\right)$$

$$\phi^{\dagger}_{\mathrm{X,ac}} = \mathrm{MINA}\left(\phi_{\mathrm{X,ac}} - \phi^{\star}_{\mathrm{X,ac}},\, 0,\, a_{\phi,\mathrm{ac}}\right)$$

NUD parameters

$$\mathrm{u_{s1}} = \sqrt{\mathrm{VSBNUD} + \phi_{\mathrm{B}}} - \sqrt{\phi_{\mathrm{B}}}$$

$$\mathrm{u_{s21}} = \sqrt{\mathrm{DVSBNUD} + \phi_{\mathrm{B}}} - \sqrt{\phi_{\mathrm{B}}} - \mathrm{u_{s1}}$$

© 2023 Cadence Design Systems, Inc.

Local process parameters in gate overlap region

$$\gamma_{\mathrm{ov}} = \sqrt{2 \cdot q \cdot \epsilon_{\mathrm{Si}} \cdot \mathbf{NOV}} \cdot \mathbf{TOXOV} / \epsilon_{\mathrm{ox}}$$

$$\gamma_{\mathrm{dov}} = \sqrt{2 \cdot q \cdot \epsilon_{\mathrm{Si}} \cdot \mathbf{NOVD}} \cdot \mathbf{TOXOVD} / \epsilon_{\mathrm{ox}}$$

$$\boldsymbol{G_{\mathrm{ov}}} = \gamma_{\mathrm{ov}} / \sqrt{\boldsymbol{\phi_{\mathrm{T}}}}$$

$$\boldsymbol{G_{\mathrm{dov}}} = \gamma_{\mathrm{dov}} / \sqrt{\boldsymbol{\phi_{\mathrm{T}}}}$$

$$\boldsymbol{\xi_{\mathrm{ov}}} = 1 + \boldsymbol{G_{\mathrm{ov}}} / \sqrt{2}$$

$$\boldsymbol{\xi_{\mathrm{dov}}} = 1 + \boldsymbol{G_{\mathrm{dov}}} / \sqrt{2}$$

$$\boldsymbol{x_{\mathrm{mrgov}}} = 10^{-5} \cdot \boldsymbol{\xi_{\mathrm{ov}}}$$

$$\boldsymbol{x_{\mathrm{mrgdov}}} = 10^{-5} \cdot \boldsymbol{\xi_{\mathrm{dov}}}$$

© 2023 Cadence Design Systems, Inc.

Mobility parameters

$$\beta = \mathbf{FACTUO} \cdot \mathbf{BETN} \cdot C_{\mathrm{ox}} \cdot (T_{\mathrm{KR}}/T_{\mathrm{KD}})^{\mathbf{STBET}}$$

$$\theta_{\mu} = \mathbf{THEMU} \cdot (T_{\mathrm{KR}}/T_{\mathrm{KD}})^{\mathbf{STTHEMU}}$$

$$\mu_{\mathrm{E}} = \mathbf{MUE} \cdot (T_{\mathrm{KR}}/T_{\mathrm{KD}})^{\mathbf{STMUE}}$$

$$X_{\mathbf{cor}} = \mathbf{XCOR} \cdot (T_{\mathrm{KR}}/T_{\mathrm{KD}})^{\mathbf{STXCOR}}$$

$$C_{\mathrm{S}} = \mathbf{CS} \cdot (T_{\mathrm{KR}}/T_{\mathrm{KD}})^{\mathbf{STCS}}$$

$$E_{\mathbf{eff0}} = 10^{-8} \cdot C_{\mathrm{ox}}/\epsilon_{\mathrm{Si}}$$

$$\eta_{\mu} = \begin{cases} 1/2 \cdot \mathbf{FETA} & \text{for NMOS} \\ 1/3 \cdot \mathbf{FETA} & \text{for PMOS} \end{cases}$$

$$\eta_{\mu,\mathrm{ac}} = \begin{cases} 1/2 & \text{for NMOS} \\ 1/3 & \text{for PMOS} \end{cases}$$

$$\theta_{cs} = \mathbf{THECS} \cdot (T_{\mathrm{KR}}/T_{\mathrm{KD}})^{\mathbf{STTHECS}}$$

Series resistance parameter

$$R_{\mathrm{s}} = \mathbf{RS} \cdot (T_{\mathrm{KR}}/T_{\mathrm{KD}})^{\mathbf{STRS}}$$

$$\theta_{\mathrm{R}} = 2 \cdot \beta \cdot R_{\mathrm{s}}$$

Velocity saturation parameter

$$\theta_{\mathbf{sat}} = \mathbf{THESAT} \cdot (T_{\mathrm{KR}}/T_{\mathrm{KD}})^{\mathbf{STTHESAT}}$$

© 2023 Cadence Design Systems, Inc.

Impact-ionization parameter

$$a_2 = \mathbf{A2} \cdot (T_{\mathrm{KD}}/T_{\mathrm{KR}})^{\mathbf{STA2}}$$

Gate current parameters

$$I_{\mathrm{GINV}} = \mathbf{IGINV} \cdot (T_{\mathrm{KD}}/T_{\mathrm{KR}})^{\mathbf{STIG}}$$

$$I_{\mathrm{GOV}} = \mathbf{IGOV} \cdot (T_{\mathrm{KD}}/T_{\mathrm{KR}})^{\mathbf{STIG}}$$

$$I_{\mathrm{GOVD}} = \mathbf{IGOVD} \cdot (T_{\mathrm{KD}}/T_{\mathrm{KR}})^{\mathbf{STIG}}$$

$$B = \frac{4}{3} \cdot \frac{\mathbf{TOX}}{\hbar} \cdot \sqrt{2 \cdot q \cdot m_0 \cdot \mathbf{CHIB}} = 6.830909 \cdot 10^9 \cdot \mathbf{TOX} \cdot \sqrt{\mathbf{CHIB}}$$

$$B_{\mathrm{ov}} = B \cdot \mathbf{TOXOV}/\mathbf{TOX}$$

$$B_{\mathrm{ovd}} = B \cdot \mathbf{TOXOVD}/\mathbf{TOX}$$

$$GC_{\mathrm{Q}} = \begin{cases} -0.99 \cdot \dfrac{\mathbf{GC2}}{2 \cdot \mathbf{GC3}} & \text{for } \mathbf{GC3} < 0 \\ 0 & \text{for } \mathbf{GC3} \geq 0 \end{cases}$$

$$\alpha_{\mathrm{b}} = \frac{E_{\mathrm{g}}/q + \phi_{\mathbf{B}}}{2}$$

$$D_{\mathrm{ch}} = \mathbf{GCO} \cdot \phi_{\mathbf{T}}^{*}$$

$$D_{\mathrm{ov}} = \mathbf{GCO} \cdot \phi_{\mathbf{T}}$$

© 2023 Cadence Design Systems, Inc.

Gate-induced drain leakage parameters

$$A_{\mathrm{GIDL}} = \mathbf{AGIDL} \cdot \left(\frac{2 \cdot 10^{-9}}{\mathbf{TOXOV}}\right)^2$$

$$A_{\mathrm{GIDLD}} = \mathbf{AGIDLD} \cdot \left(\frac{2 \cdot 10^{-9}}{\mathbf{TOXOVD}}\right)^2$$

$$B_{\mathrm{GIDL}} = \mathbf{BGIDL} \cdot \mathrm{MAX}\left(\left[1 + \mathbf{STBGIDL} \cdot \Delta T\right], 0\right) \cdot \left(\frac{\mathbf{TOXOV}}{2 \cdot 10^{-9}}\right)$$

$$B_{\mathrm{GIDLD}} = \mathbf{BGIDLD} \cdot \mathrm{MAX}\left(\left[1 + \mathbf{STBGIDLD} \cdot \Delta T\right], 0\right) \cdot \left(\frac{\mathbf{TOXOVD}}{2 \cdot 10^{-9}}\right)$$

Noise parameter

$$N_{\mathrm{T}} = \mathbf{FNT} \cdot 4 \cdot k_{\mathrm{B}} \cdot T_{\mathrm{KD}}$$

Additional internal parameters

$$x_1 = 1.25$$

$$x_{\mathrm{gl}} = x_1 + G_{\mathrm{ov}} \cdot \sqrt{\exp(-x_1) + x_1 - 1}$$

$$x_{\mathrm{dgl}} = x_1 + G_{\mathrm{dov}} \cdot \sqrt{\exp(-x_1) + x_1 - 1}$$

Current Model

In this section, the current model equations of the PSP-model are given. Use is made of the applied terminal bias values VGS, VDS and VSB, the local parameters listed in Section 'Intrinsic Parameters for the model', and the internal parameters introduced in previous section. Local parameters are denoted by capital characters in bold font, whereas internal (bias-independent) parameters are denoted by symbols in bold font.

© 2023 Cadence Design Systems, Inc.

Depending on the value of the parameters SWNUD and SWDELVTAC, the surface potential (at source- and drain-side of the channel) and associated computations may be evaluated twice: once for the dc-characteristics and a second time for the ac-characteristics of the model. Details are given below.

Conditioning of Terminal Voltages

$$V_{\mathrm{dsx}} = \sqrt{{V_{\mathrm{DS}}}^2 + 0.01} - 0.1$$

$$\phi_{\mathrm{V,dc}} = \mathrm{MINA}\left(V_{\mathrm{SB}},\, V_{\mathrm{SB}} + V_{\mathrm{DS}},\, \boldsymbol{b}_{\boldsymbol{\phi},\mathrm{dc}}\right) + \boldsymbol{\phi}_{\mathbf{X},\mathrm{dc}}$$

$$\phi_{\mathrm{V,ac}} = \mathrm{MINA}\left(V_{\mathrm{SB}},\, V_{\mathrm{SB}} + V_{\mathrm{DS}},\, \boldsymbol{b}_{\boldsymbol{\phi},\mathrm{ac}}\right) + \boldsymbol{\phi}_{\mathbf{X},\mathrm{ac}}$$

$$V^{*}_{\mathrm{SB,dc}} = V_{\mathrm{SB}} - \mathrm{MINA}\left(\phi_{\mathrm{V}},\, 0,\, \boldsymbol{a}_{\boldsymbol{\phi},\mathrm{dc}}\right) + \overset{*}{\boldsymbol{\phi}}_{\mathbf{X},\mathrm{dc}}$$

$$V^{*}_{\mathrm{SB,ac}} = V_{\mathrm{SB}} - \mathrm{MINA}\left(\phi_{\mathrm{V}},\, 0,\, \boldsymbol{a}_{\boldsymbol{\phi},\mathrm{ac}}\right) + \overset{*}{\boldsymbol{\phi}}_{\mathbf{X},\mathrm{ac}}$$

Nonuniform doping effect. are only evaluated when

. **SWNUD** $\neq 0$ and **GFACNUD** $\neq 1$:

$$V_{\mathrm{mB}} = V^{*}_{\mathrm{SB}} + 0.5 \cdot \left(V_{\mathrm{DS}} - V_{\mathrm{dsx}}\right)$$

$$u_{\mathrm{s}} = \sqrt{V_{\mathrm{mB}} + \boldsymbol{\phi}_{\mathbf{B}}} - \sqrt{\boldsymbol{\phi}_{\mathbf{B}}}$$

$$p = 2 \cdot \frac{u_{\mathrm{s}} - \mathbf{u_{s1}}}{\mathbf{u_{s21}}} - 1$$

$$u_{\mathrm{s,nud}} = u_{\mathrm{s}} - 0.25 \cdot (1 - \mathbf{GFACNUD}) \cdot \mathbf{u_{s21}} \cdot \left\{p + \sqrt{p^2 + \left[\ln(2)\right]^2}\right\}$$

$$V_{\mathrm{mB,nud}} = \left(u_{\mathrm{s,nud}} + 2 \cdot \sqrt{\boldsymbol{\phi}_{\mathbf{B}}}\right) \cdot u_{\mathrm{s,nud}}$$

$$V^{\mathrm{nud}}_{\mathrm{SB}} = V_{\mathrm{mB,nud}} - 0.5 \cdot \left(V_{\mathrm{DS}} - V_{\mathrm{dsx}}\right)$$

$$V^{*}_{\mathrm{SB,dc}} = V^{\mathrm{nud}}_{\mathrm{SB}}$$

The surface potential (at source- and drain-side of the channel) and associated computations are evaluated using

$$V^{*}_{\mathrm{SB}} = V^{*}_{\mathrm{SB,dc}},\ \boldsymbol{\phi}_{\mathbf{B}} = \boldsymbol{\phi}_{\mathbf{B},\mathrm{dc}},\ \text{and}\ \boldsymbol{G}_{\mathbf{0}} = \boldsymbol{G}_{\mathbf{0},\mathrm{dc}}.$$

© 2023 Cadence Design Systems, Inc.

If SWNUD = 1 or SWDELVTAC = 1, calculations are done a second time using

$$V_{\mathrm{SB}}^{*} = V_{\mathrm{SB,ac}}^{*}, \quad \phi_{\mathbf{B}} = \phi_{\mathbf{B},\mathrm{ac}}, \text{ and } G_{\mathbf{0}} = G_{\mathbf{0},\mathrm{ac}}.$$

$$V_{\mathrm{DB}}^{*} = V_{\mathrm{DS}} + V_{\mathrm{SB}}^{*}$$

$$V_{\mathrm{sbx}} = V_{\mathrm{SB}}^{*} + \frac{V_{\mathrm{DS}} - V_{\mathrm{dsx}}}{2}$$

Drain-induced barrier lowering:

$$\Delta V_{\mathrm{G}} = \mathbf{CF} \cdot V_{\mathrm{dsx}} \cdot (1 + \mathbf{CFB} \cdot V_{\mathrm{sbx}})$$

$$V_{\mathrm{GB}}^{*} = V_{\mathrm{GS}} + V_{\mathrm{SB}}^{*} + \Delta V_{\mathrm{G}} - \boldsymbol{V_{\mathbf{FB}}}$$

$$x_{\mathrm{g}} = V_{\mathrm{GB}}^{*} / \phi_{\mathbf{T}}^{*}$$

Bias-Dependent Body Factor

$$D_{\mathrm{nsub}} = \mathbf{DNSUB} \cdot \mathrm{MAXA}(0,\, V_{\mathrm{GS}} + V_{\mathrm{SB}} - \mathbf{VNSUB},\, \mathbf{NSLP})$$

$$G = \boldsymbol{G_{\mathbf{0}}} \cdot \sqrt{1 + D_{\mathrm{nsub}}}$$

© 2023 Cadence Design Systems, Inc.

Surface Potential at Source Side and Related Variables

$$\xi = 1 + G/\sqrt{2}$$

$$x_{\mathrm{ns}} = \frac{\phi_{\mathbf{B}} + V^{*}_{\mathrm{SB}}}{\phi^{*}_{\mathbf{T}}}$$

$$\Delta_{\mathrm{ns}} = \exp\left(-x_{\mathrm{ns}}\right)$$

$$x_{\mathrm{mrg}} = 10^{-5} \cdot \xi$$

© 2023 Cadence Design Systems, Inc.

$$\textbf{if } x_g < -x_{mrg} \begin{cases} y_g = -x_g \\ z = 1.25 \cdot y_g/\xi \\ \eta = \left[z + 10 - \sqrt{(z-6)^2 + 64}\right]/2 \\ a = (y_g - \eta)^2 + G^2 \cdot (\eta + 1) \\ c = 2 \cdot (y_g - \eta) - G^2 \\ \tau = -\eta + \ln\left(a/G^2\right) \\ y_0 = \sigma_1(a,\, c,\, \tau,\, \eta) \\ \Delta_0 = \exp\left(y_0\right) \\ p = 2 \cdot (y_g - y_0) + G^2 \cdot [\Delta_0 - 1 + \Delta_{ns} \cdot (1 - \chi'(y_0) - 1/\Delta_0)] \\ q = (y_g - y_0)^2 + G^2 \cdot [y_0 - \Delta_0 + 1 + \Delta_{ns} \cdot (1 + \chi(y_0) - 1/\Delta_0 - 2 \cdot y_0)] \\ x_s = -y_0 - \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot \{2 - G^2 \cdot [\Delta_0 + \Delta_{ns} \cdot (1/\Delta_0 - \chi''(y_0))]\}}} \end{cases}$$

$$\textbf{if } |x_g| \le x_{mrg} \begin{cases} x_s = \dfrac{x_g}{\xi} \cdot \left[1 + G \cdot x_g \cdot \dfrac{1 - \Delta_{ns}}{\xi^2 \cdot 6 \cdot \sqrt{2}}\right] \end{cases}$$

$$\textbf{if } x_g > x_{mrg} \begin{cases} \hat{x}_{g1} = x_1 + G \cdot \sqrt{\exp(-x_1) + x_1 - 1} \\ \bar{x} = \dfrac{x_g}{\xi} \cdot \left[1 + x_g \cdot (\xi \cdot x_1 - \hat{x}_{g1})/\hat{x}_{g1}^2\right] \\ x_0 = x_g + G^2/2 - G \cdot \sqrt{x_g + G^2/4 - 1 + \exp(-\bar{x})} \\ b_x = x_{ns} + 3 \\ \eta = \mathrm{MINA}(x_0,\, b_x,\, 5) - \left(b_x - \sqrt{b_x^2 + 5}\right)/2 \\ a = (x_g - \eta)^2 - G^2 \cdot [\exp(-\eta) + \eta - 1 - \Delta_{ns} \cdot (\eta + 1 + \chi(\eta))] \\ b = 1 - G^2/2 \cdot [\exp(-\eta) - \Delta_{ns} \cdot \chi''(\eta)] \\ c = 2 \cdot (x_g - \eta) + G^2 \cdot [1 - \exp(-\eta) - \Delta_{ns} \cdot (1 + \chi'(\eta))] \\ \tau = x_{ns} - \eta + \ln\left(a/G^2\right) \\ y_0 = \sigma_2(a,\, b,\, c,\, \tau,\, \eta) \\ \Delta_0 = \exp\left(y_0\right) \\ p = 2 \cdot (x_g - y_0) + G^2 \cdot [1 - 1/\Delta_0 + \Delta_{ns} \cdot (\Delta_0 - 1 - \chi'(y_0))] \\ q = (x_g - y_0)^2 - G^2 \cdot [y_0 + 1/\Delta_0 - 1 + \Delta_{ns} \cdot (\Delta_0 - y_0 - 1 - \chi(y_0))] \\ x_s = y_0 + \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot \{2 - G^2 \cdot [1/\Delta_0 + \Delta_{ns} \cdot (\Delta_0 - \chi''(y_0))]\}}} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Calculations are only done for $x_g > 0$.

$$E_s = \exp(-x_s)$$

$$D_s = [1/E_s - x_s - 1 - \chi(x_s)] \cdot \Delta_{ns}$$

$$P_s = x_s - 1 + E_s$$

$$x_{gs} = \begin{cases} x_g - x_s & \text{for } x_g \le 0 \\ G \cdot \sqrt{D_s + P_s} & \text{for } x_g > 0 \end{cases}$$

$$\psi_{ss} = \dot{\phi_T} \cdot x_s$$

© 2023 Cadence Design Systems, Inc.

Drain Saturation Voltage

Calculations are only done for $x_g > 0$.

$$q_{is} = \frac{G^2 \cdot \phi_T^* \cdot D_s}{x_{gs} + G \cdot \sqrt{P_s}}$$

$$\alpha_s = 1 + \frac{G \cdot (1 - E_s)}{2 \cdot \sqrt{P_s}}$$

$$q_{bs} = \phi_T^* \cdot G \cdot \sqrt{P_s}$$

$$\rho_b = \begin{cases} 1 + \mathbf{RSB} \cdot V_{sbx} & \text{for } \mathbf{RSB} \geq 0 \\ \dfrac{1}{1 - \mathbf{RSB} \cdot V_{sbx}} & \text{for } \mathbf{RSB} < 0 \end{cases}$$

$$\rho_{g,s} = \begin{cases} \dfrac{1}{1 + \mathbf{RSG} \cdot q_{is}} & \text{for } \mathbf{RSG} \geq 0 \\ 1 - \mathbf{RSG} \cdot q_{is} & \text{for } \mathbf{RSG} < 0 \end{cases}$$

$$\rho_s = \theta_R \cdot \rho_b \cdot \rho_{g,s} \cdot q_{is}$$

$$\mu_x = \frac{1 + X_{cor} \cdot V_{sbx}}{1 + 0.2 \cdot X_{cor} \cdot V_{sbx}}$$

$$E_{eff,s} = E_{eff0} \cdot (q_{bs} + \eta_\mu \cdot q_{is})$$

$$G_{mob,s} = \frac{1 + (\mu_E \cdot E_{eff,s})^{\theta_\mu} + C_S \cdot \left(\dfrac{q_{bs}}{q_{is} + q_{bs}}\right)^2 + \rho_s}{\mu_x}$$

$$\xi_{tb} = \begin{cases} 1 + \mathbf{THESATB} \cdot V_{sbx} & \text{for } \mathbf{THESATB} \geq 0 \\ \dfrac{1}{1 - \mathbf{THESATB} \cdot V_{sbx}} & \text{for } \mathbf{THESATB} < 0 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$w_{\mathrm{sat,s}} = \frac{100 \cdot q_{\mathrm{is}} \cdot \xi_{\mathrm{tb}}}{100 + q_{\mathrm{is}} \cdot \xi_{\mathrm{tb}}}$$

$$\theta^{*}_{\mathrm{sat,s}} = \begin{cases} \dfrac{\boldsymbol{\theta_{\mathrm{sat}}}}{G_{\mathrm{mob,s}}} \cdot (1 + \mathbf{THESATG} \cdot w_{\mathrm{sat,s}}) & \text{for } \mathbf{THESATG} \geq 0 \\ \dfrac{\boldsymbol{\theta_{\mathrm{sat}}}}{G_{\mathrm{mob,s}}} \cdot \dfrac{1}{1 - \mathbf{THESATG} \cdot w_{\mathrm{sat,s}}} & \text{for } \mathbf{THESATG} < 0 \end{cases}$$

$$\phi_{\infty} = q_{\mathrm{is}}/\alpha_{\mathrm{s}} + \phi^{*}_{\mathbf{T}}$$

$$y_{\mathrm{sat}} = \begin{cases} \theta^{*}_{\mathrm{sat,s}} \cdot \phi_{\infty}/\sqrt{2} & \text{for NMOS} \\ \dfrac{\theta^{*}_{\mathrm{sat,s}} \cdot \phi_{\infty}/\sqrt{2}}{\sqrt{1 + \theta^{*}_{\mathrm{sat,s}} \cdot \phi_{\infty}/\sqrt{2}}} & \text{for PMOS} \end{cases}$$

$$z_{\mathrm{a}} = \frac{2}{1 + \sqrt{1 + 4 \cdot y_{\mathrm{sat}}}}$$

$$\phi_0 = \phi_{\infty} \cdot z_{\mathrm{a}} \cdot \left[1 + 0.86 \cdot z_{\mathrm{a}} \cdot y_{\mathrm{sat}} \cdot \frac{1 - z_{\mathrm{a}}^2 \cdot y_{\mathrm{sat}}}{1 + 4 \cdot z_{\mathrm{a}}^3 \cdot y_{\mathrm{sat}}^2}\right]$$

$$a_{\mathrm{sat}} = x_{\mathrm{gs}} + G^2/2$$

$$\phi_2 = \frac{\phi^{*}_{\mathbf{T}} \cdot 0.98 \cdot G^2 \cdot D_{\mathrm{s}}}{a_{\mathrm{sat}} + \sqrt{a_{\mathrm{sat}}^2 - 0.98 \cdot G^2 \cdot D_{\mathrm{s}}}}$$

$$\phi_{\mathrm{sat}} = \frac{2 \cdot \phi_0 \cdot \phi_2}{\phi_0 + \phi_2 + \sqrt{(\phi_0 + \phi_2)^2 - 3.96 \cdot \phi_0 \cdot \phi_2}}$$

$$V_{\mathrm{dsat}} = \phi_{\mathrm{sat}} - \phi^{*}_{\mathbf{T}} \cdot \ln\left[1 + \frac{\phi_{\mathrm{sat}} \cdot \left(\phi_{\mathrm{sat}} - 2 \cdot a_{\mathrm{sat}} \cdot \phi^{*}_{\mathbf{T}}\right)}{G^2 \cdot D_{\mathrm{s}} \cdot {\phi^{*}_{\mathbf{T}}}^2}\right]$$

$$V_{\mathrm{dse}} = \frac{V_{\mathrm{DS}}}{\left[1 + (V_{\mathrm{DS}}/V_{\mathrm{dsat}})^{\mathbf{AX}}\right]^{1/\mathbf{AX}}}$$

© 2023 Cadence Design Systems, Inc.

Surface Potential at Drain Side and Related Variables

Calculations are only done for $x_g > 0$.

$$x_{\mathrm{nd}} = \frac{\phi_{\mathbf{B}} + V^{*}_{\mathrm{SB}} + V_{\mathrm{dse}}}{\phi^{*}_{\mathbf{T}}}$$

$$k_{\mathrm{ds}} = \exp\left(-V_{\mathrm{dse}}/\phi^{*}_{\mathbf{T}}\right)$$

$$\Delta_{\mathrm{nd}} = \Delta_{\mathrm{ns}} \cdot k_{\mathrm{ds}}$$

$$\textbf{if } x_{\mathrm{g}} \le x_{\mathrm{mrg}} \left\{ \; x_{\mathrm{d}} = \frac{x_{\mathrm{g}}}{\xi} \cdot \left[1 + G \cdot x_{\mathrm{g}} \cdot \frac{1 - \Delta_{\mathrm{nd}}}{\xi^2 \cdot 6 \cdot \sqrt{2}}\right]\right.$$

$$\textbf{if } x_{\mathrm{g}} > x_{\mathrm{mrg}} \left\{ \begin{array}{l} b_{\mathrm{x}} = x_{\mathrm{nd}} + 3.0 \\ \eta = \mathrm{MINA}(x_0,\, b_{\mathrm{x}},\, 5) - \left(b_{\mathrm{x}} - \sqrt{b_{\mathrm{x}}^2 + 5}\right)/2 \\ a = (x_{\mathrm{g}} - \eta)^2 - G^2 \cdot [\exp(-\eta) + \eta - 1 - \Delta_{\mathrm{nd}} \cdot (\eta + 1 + \chi(\eta))] \\ b = 1 - G^2/2 \cdot [\exp(-\eta) - \Delta_{\mathrm{nd}} \cdot \chi''(\eta)] \\ c = 2 \cdot (x_{\mathrm{g}} - \eta) + G^2 \cdot [1 - \exp(-\eta) - \Delta_{\mathrm{nd}} \cdot (1 + \chi'(\eta))] \\ \tau = x_{\mathrm{nd}} - \eta + \ln\left(a/G^2\right) \\ y_0 = \sigma_2(a,\, b,\, c,\, \tau,\, \eta) \\ \Delta_0 = \exp\left(y_0\right) \\ p = 2 \cdot (x_{\mathrm{g}} - y_0) + G^2 \cdot [1 - 1/\Delta_0 + \Delta_{\mathrm{nd}} \cdot (\Delta_0 - 1 - \chi'(y_0))] \\ q = (x_{\mathrm{g}} - y_0)^2 - G^2 \cdot [y_0 + 1/\Delta_0 - 1 + \Delta_{\mathrm{nd}} \cdot (\Delta_0 - y_0 - 1 - \chi(y_0))] \\ x_{\mathrm{d}} = y_0 + \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot \{2 - G^2 \cdot [1/\Delta_0 + \Delta_{\mathrm{nd}} \cdot (\Delta_0 - \chi''(y_0))]\}}} \end{array}\right.$$

$$x_{\mathrm{ds}} = x_{\mathrm{d}} - x_{\mathrm{s}}$$

$$\textbf{if } x_{\mathrm{ds}} < 10^{-10} \left\{ \begin{array}{l} p = 2 \cdot x_{\mathrm{gs}} + G^2 \cdot [1 - E_{\mathrm{s}} + \Delta_{\mathrm{nd}} \cdot (1/E_{\mathrm{s}} - 1 - \chi'(x_{\mathrm{s}}))] \\ q = G^2 \cdot (1 - k_{\mathrm{ds}}) \cdot D_{\mathrm{s}} \\ \xi = 1 - G^2/2 \cdot [E_{\mathrm{s}} + \Delta_{\mathrm{nd}}\,(1/E_{\mathrm{s}} - \chi''(x_{\mathrm{s}}))] \\ x_{\mathrm{ds}} = \dfrac{2 \cdot q}{p + \sqrt{p^2 - 4 \cdot \xi \cdot q}} \\ x_{\mathrm{d}} = x_{\mathrm{s}} + x_{\mathrm{ds}} \end{array}\right.$$

$$E_{\mathrm{d}} = \exp\left(-x_{\mathrm{d}}\right)$$

$$D_{\mathrm{d}} = (1/E_{\mathrm{d}} - x_{\mathrm{d}} - 1 - \chi(x_{\mathrm{d}})) \cdot \Delta_{\mathrm{nd}}$$

$$\Delta\psi = \phi^{*}_{\mathbf{T}} \cdot x_{\mathrm{ds}}$$

$$\psi_{\mathrm{sd}} = \phi^{*}_{\mathbf{T}} \cdot x_{\mathrm{d}}$$

© 2023 Cadence Design Systems, Inc.

Mid-Point Surface Potential and Related Variables

$$\textbf{if } x_{\mathrm{g}} > 0 \begin{cases} x_{\mathrm{m}} = \left(x_{\mathrm{s}} + x_{\mathrm{d}}\right)/2 \\ E_{\mathrm{m}} = \sqrt{E_{\mathrm{s}} \cdot E_{\mathrm{d}}} \\ \bar{D} = \left(D_{\mathrm{s}} + D_{\mathrm{d}}\right)/2 \\ D_{\mathrm{m}} = \bar{D} + x_{\mathrm{ds}}^2/8 \cdot \left(E_{\mathrm{m}} - 2/G^2\right) \\ P_{\mathrm{m}} = x_{\mathrm{m}} - 1 + E_{\mathrm{m}} \\ x_{\mathrm{gm}} = G \cdot \sqrt{D_{\mathrm{m}} + P_{\mathrm{m}}} \end{cases}$$

$$\textbf{if } x_{\mathrm{g}} \leq 0 \begin{cases} x_{\mathrm{m}} = x_{\mathrm{s}} \\ x_{\mathrm{gm}} = x_{\mathrm{g}} - x_{\mathrm{s}} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Polysilicon Depletion

Calculations are only done for $k_P > 0$ and $x_g > 0$ (otherwise $np = 1$):

$$x_{\mathrm{m}}^{(0)} = x_{\mathrm{m}}, \qquad x_{\mathrm{ds}}^{(0)} = x_{\mathrm{ds}}, \qquad D_{\mathrm{m}}^{(0)} = D_{\mathrm{m}}, \qquad E_{\mathrm{m}}^{(0)} = E_{\mathrm{m}},$$

$$d_0 = 1 - E_{\mathrm{m}}^{(0)} + 2 \cdot x_{\mathrm{gm}}/G^2$$

$$\eta_{\mathrm{p}} = 1/\sqrt{1 + \boldsymbol{k_P} \cdot x_{\mathrm{gm}}}$$

$$x_{\mathrm{pm}} = \boldsymbol{k_P} \cdot \left[\frac{\eta_{\mathrm{p}} \cdot x_{\mathrm{gm}}}{1 + \eta_{\mathrm{p}}}\right]^2 \cdot \frac{D_{\mathrm{m}}^{(0)}}{D_{\mathrm{m}}^{(0)} + P_{\mathrm{m}}}$$

$$p = 2 \cdot (x_{\mathrm{gm}} - x_{\mathrm{pm}}) + G^2 \cdot \left(1 - E_{\mathrm{m}}^{(0)} + D_{\mathrm{m}}^{(0)}\right)$$

$$q = x_{\mathrm{pm}} \cdot (x_{\mathrm{pm}} - 2 \cdot x_{\mathrm{gm}})$$

$$\xi_{\mathrm{p}} = 1 - G^2/2 \cdot \left(E_{\mathrm{m}}^{(0)} + D_{\mathrm{m}}^{(0)}\right)$$

$$u_{\mathrm{p}} = \frac{p \cdot q}{p^2 - \xi_{\mathrm{p}} \cdot q}$$

$$x_{\mathrm{m}} = x_{\mathrm{m}}^{(0)} + u_{\mathrm{p}}$$

$$E_{\mathrm{m}} = E_{\mathrm{m}}^{(0)} \cdot \exp(-u_{\mathrm{p}})$$

$$D_{\mathrm{m}} = D_{\mathrm{m}}^{(0)} \cdot \exp(u_{\mathrm{p}})$$

$$P_{\mathrm{m}} = x_{\mathrm{m}} - 1 + E_{\mathrm{m}}$$

$$x_{\mathrm{gm}} = G \cdot \sqrt{D_{\mathrm{m}} + P_{\mathrm{m}}}$$

$$x_{\mathrm{ds}} = x_{\mathrm{ds}}^{(0)} \cdot \frac{\exp(u_{\mathrm{p}}) \cdot [\bar{D} + d_0]}{1 - E_{\mathrm{m}} + 2 \cdot x_{\mathrm{gm}} \cdot \eta_{\mathrm{p}}/G^2 + \exp(u_{\mathrm{p}}) \cdot \bar{D}}$$

$$\Delta\psi = \phi_{\mathbf{T}}^{*} \cdot x_{\mathrm{ds}}$$

© 2023 Cadence Design Systems, Inc.

Potential Mid-Point Inversion Charge and Related Variables

Calculations are only done for $x_g > 0$.

$$q_{\mathrm{im}} = \frac{G^2 \cdot \phi_{\mathbf{T}}^{*} \cdot D_{\mathrm{m}}}{x_{\mathrm{gm}} + G \cdot \sqrt{P_{\mathrm{m}}}}$$

$$\alpha_{\mathrm{m}} = \eta_{\mathrm{p}} + \frac{G \cdot (1 - E_{\mathrm{m}})}{2 \cdot \sqrt{P_{\mathrm{m}}}}$$

$$q_{\mathrm{im}}^{*} = q_{\mathrm{im}} + \phi_{\mathbf{T}}^{*} \cdot \alpha_{\mathrm{m}}$$

$$q_{\mathrm{bm}} = \phi_{\mathbf{T}}^{*} \cdot G \cdot \sqrt{P_{\mathrm{m}}}$$

Series resistance:

$$\rho_{\mathrm{g}} = \begin{cases} \dfrac{1}{1 + \mathbf{RSG} \cdot q_{\mathrm{im}}} & \text{for } \mathbf{RSG} \geq 0 \\ 1 - \mathbf{RSG} \cdot q_{\mathrm{im}} & \text{for } \mathbf{RSG} < 0 \end{cases}$$

$$\rho_{\mathrm{s}} = \boldsymbol{\theta}_{\mathbf{R}} \cdot \rho_{\mathrm{b}} \cdot \rho_{\mathrm{g}} \cdot q_{\mathrm{im}}$$

Mobility reduction:

$$E_{\mathrm{eff}} = \boldsymbol{E}_{\mathbf{eff0}} \cdot \left(q_{\mathrm{bm}} + \boldsymbol{\eta}_{\boldsymbol{\mu}} \cdot q_{\mathrm{im}}\right)$$

$$q_{\mathrm{eff1}} = q_{\mathrm{bm}} + \boldsymbol{\eta}_{\boldsymbol{\mu},ac} \cdot q_{\mathrm{im}}$$

$$G_{\mathrm{mob}} = \frac{1 + \left(\boldsymbol{\mu}_{\mathbf{E}} \cdot E_{\mathrm{eff}}\right)^{\boldsymbol{\theta}_{\boldsymbol{\mu}}} + C_{\mathbf{S}} \cdot \left(\frac{q_{\mathrm{bm}}}{q_{\mathrm{im}} + q_{\mathrm{bm}}}\right)^2 + \rho}{\mu_{\mathrm{x}}}$$

Drain Source Channel Current

Calculations are only done for $x_g > 0$

© 2023 Cadence Design Systems, Inc.

Channel Length Modulation

$$R_1 = q_{\mathrm{im}}/q^*_{\mathrm{im}}$$

$$R_2 = \phi^*_{\mathbf{T}} \cdot \alpha_{\mathrm{m}}/q^*_{\mathrm{im}}$$

$$T_1 = \ln\left(\frac{1+\dfrac{V_{\mathrm{DS}}-\Delta\psi}{\mathbf{VP}}}{1+\dfrac{V_{\mathrm{dse}}-\Delta\psi}{\mathbf{VP}}}\right)$$

$$T_2 = \ln\left(1+\frac{V_{\mathrm{dsx}}}{\mathbf{VP}}\right)$$

$$\Delta L/L = \mathbf{ALP} \cdot T_1$$

$$G_{\Delta L} = \frac{1}{1+\Delta L/L+(\Delta L/L)^2}$$

$$\Delta L_1/L = \left[\mathbf{ALP}+\frac{\mathbf{ALP1}}{q^*_{\mathrm{im}}} \cdot R_1\right] \cdot T_1 + \mathbf{ALP2} \cdot q_{\mathrm{bm}} \cdot R_2^2 \cdot T_2$$

$$F_{\Delta L} = \left[1+\Delta L_1/L+(\Delta L_1/L)^2\right] \cdot G_{\Delta L}$$

© 2023 Cadence Design Systems, Inc.

Velocity Saturation

$$w_{\mathrm{sat}} = \frac{100 \cdot q_{\mathrm{im}} \cdot \xi_{\mathrm{tb}}}{100 + q_{\mathrm{im}} \cdot \xi_{\mathrm{tb}}}$$

$$\theta^{*}_{\mathrm{sat}} = \begin{cases} \dfrac{\boldsymbol{\theta_{\mathrm{sat}}}}{G_{\mathrm{mob,s}} \cdot G_{\Delta L}} \cdot (1 + \mathbf{THESATG} \cdot w_{\mathrm{sat}}) & \text{for } \mathbf{THESATG} \geq 0 \\ \dfrac{\boldsymbol{\theta_{\mathrm{sat}}}}{G_{\mathrm{mob,s}} \cdot G_{\Delta L}} \cdot \dfrac{1}{1 - \mathbf{THESATG} \cdot w_{\mathrm{sat}}} & \text{for } \mathbf{THESATG} < 0 \end{cases}$$

$$z_{\mathrm{sat}} = \begin{cases} (\theta^{*}_{\mathrm{sat}} \cdot \Delta\psi)^2 & \text{for NMOS} \\ \dfrac{(\theta^{*}_{\mathrm{sat}} \cdot \Delta\psi)^2}{1 + \theta^{*}_{\mathrm{sat}} \cdot \Delta\psi} & \text{for PMOS} \end{cases}$$

$$G_{\mathrm{vsat}} = \frac{G_{\mathrm{mob}} \cdot G_{\Delta L}}{2} \cdot \left(1 + \sqrt{1 + 2 \cdot z_{\mathrm{sat}}}\right)$$

Auxiliary Variables for Calculation of Intrinsic Charges and Gate Current. are only calculated for $x_g > 0$.

$$V_{\mathrm{oxm}} = \phi^{\dagger}_{\mathbf{T}} \cdot x_{\mathrm{gm}}$$

$$\alpha'_{\mathrm{m}} = \alpha_{\mathrm{m}} \cdot \left[1 + \frac{z_{\mathrm{sat}}}{2} \cdot \left(\frac{G_{\mathrm{mob}} \cdot G_{\Delta L}}{G_{\mathrm{vsat}}}\right)^2\right]$$

$$H = \frac{G_{\mathrm{mob}} \cdot G_{\Delta L}}{G_{\mathrm{vsat}}} \cdot \frac{q^{*}_{\mathrm{im}}}{\alpha'_{\mathrm{m}}}$$

In the remainder of this section, some variables (e.g. x_g) are labeled 'dc' or 'ac' (e.g., $x_{g,dc}$ or $x_{g,ac}$). Variables labeled `dc' result from the first evaluation some calculations. For variables labeled 'ac', there are two possibilities. If **SWNUD** = 1 or **SWDELVTAC** = 1, their values result from the second evaluation od the same equations. In any other case, their value is equal to their 'dc'-counterpart.

© 2023 Cadence Design Systems, Inc.

This applies to the following variables:

$$x_{\mathrm{g}},\ q_{\mathrm{eff1}},\ V_{\mathrm{oxm}},\ q_{\mathrm{im}},\ q^{*}_{\mathrm{im}},\ \alpha_{\mathrm{m}}\ ,\ \Delta\psi,\ G_{\Delta L},\ F_{\Delta L},\ H,\ \eta_{\mathrm{p}},\ G_{\mathrm{vsat}},\ V_{\mathrm{dse}},\ \ G_{\mathrm{mob}},\ x_{\mathrm{m}},\ G,\ x_{\mathrm{gm}},\ \theta^{*}_{\mathrm{sat}}.$$

Drain source channel current

$$I_{\mathrm{DS}} = \begin{cases} 0 & \text{for } x_{\mathrm{g,dc}} \le 0 \\ \beta \cdot F_{\Delta L,\mathrm{dc}} \cdot \dfrac{q^{*}_{\mathrm{im,dc}}}{G_{\mathrm{vsat,dc}}} \cdot \Delta\psi_{\mathrm{dc}} & \text{for } x_{\mathrm{g,dc}} > 0 \end{cases}$$

Impact Ionization or Weak-Avalanche

The equations in this section are only calculated when **SWIMPACT** = 1 and x_g > 0.

$$a^{*}_{2} = a_2 \cdot \left[1 + \mathbf{A4} \cdot \left(\sqrt{V^{*}_{\mathrm{SB,dc}} + \phi_{\mathrm{B}}} - \sqrt{\phi_{\mathrm{B}}}\right)\right]$$

$$\Delta V_{\mathrm{sat}} = V_{\mathrm{DS}} - \mathbf{A3} \cdot \Delta\psi_{\mathrm{dc}}$$

$$M_{\mathrm{avl}} = \begin{cases} 0 & \text{for } \Delta V_{\mathrm{sat}} \le 0 \\ \mathbf{A1} \cdot \Delta V_{\mathrm{sat}} \cdot \exp\left(-\dfrac{a^{*}_{2}}{\Delta V_{\mathrm{sat}}}\right) & \text{for } \Delta V_{\mathrm{sat}} > 0 \end{cases}$$

$$I_{\mathrm{avl}} = M_{\mathrm{avl}} \cdot I_{\mathrm{DS}}$$

© 2023 Cadence Design Systems, Inc.

Surface Potential in Gate Overlap Regions

$$
x_{\mathrm{sov}}\left(x_{\mathrm{g}}\right)=\begin{cases}
\text{if } x_{\mathrm{g}}<-x_{\mathbf{mrgov}} \begin{cases}
y_{\mathrm{g}}=-x_{\mathrm{g}} \\
z=x_{\mathbf{1}}\cdot y_{\mathrm{g}}/\xi_{\mathbf{ov}} \\
\eta=\left[z+10-\sqrt{(z-6)^2+64}\right]\Big/2 \\
a=\left(y_{\mathrm{g}}-\eta\right)^2+G_{\mathbf{ov}}^2\cdot(\eta+1) \\
c=2\cdot\left(y_{\mathrm{g}}-\eta\right)-G_{\mathbf{ov}}^2 \\
\tau=-\eta+\ln\left(a/G_{\mathbf{ov}}^2\right) \\
y_0=\sigma_1(a,\,c,\,\tau,\,\eta) \\
\Delta_0=\exp\left(y_0\right) \\
p=2\cdot\left(y_{\mathrm{g}}-y_0\right)+G_{\mathbf{ov}}^2\cdot\left(\Delta_0-1\right) \\
q=\left(y_{\mathrm{g}}-y_0\right)^2+G_{\mathbf{ov}}^2\cdot\left(y_0-\Delta_0+1\right) \\
x_{\mathrm{sov}}=-y_0-\dfrac{2\cdot q}{p+\sqrt{p^2-2\cdot q\cdot\left(2-G_{\mathbf{ov}}^2\cdot\Delta_0\right)}}
\end{cases} \\
\text{if } \left|x_{\mathrm{g}}\right|<x_{\mathbf{mrgov}} \left\{ x_{\mathrm{sov}}=x_{\mathrm{g}}/\xi_{\mathbf{ov}} \right. \\
\text{if } x_{\mathrm{g}}>x_{\mathbf{mrgov}} \begin{cases}
\bar{x}=x_{\mathrm{g}}/\xi_{\mathbf{ov}}\cdot\left[1+x_{\mathrm{g}}\cdot\left(\xi_{\mathbf{ov}}\cdot x_{\mathbf{1}}-x_{\mathbf{gl}}\right)/x_{\mathbf{gl}}^2\right] \\
\omega=1-\exp\left(-\bar{x}\right) \\
x_0=x_{\mathrm{g}}+G_{\mathbf{ov}}^2/2-G_{\mathbf{ov}}\cdot\sqrt{x_{\mathrm{g}}+G_{\mathbf{ov}}^2/4-\omega} \\
\Delta_0=\exp\left(-x_0\right) \\
p=2\cdot\left(x_{\mathrm{g}}-x_0\right)+G_{\mathbf{ov}}^2\cdot\left(1-\Delta_0\right) \\
q=\left(x_{\mathrm{g}}-x_0\right)^2-G_{\mathbf{ov}}^2\cdot\left(x_0+\Delta_0-1\right) \\
x_{\mathrm{sov}}=x_0+\dfrac{2\cdot q}{p+\sqrt{p^2-2\cdot q\cdot\left(2-G_{\mathbf{ov}}^2\cdot\Delta_0\right)}}
\end{cases}
\end{cases}
$$

© 2023 Cadence Design Systems, Inc.

$$
x_{\mathrm{dov}}\left(x_{\mathrm{g}}\right)=\begin{cases}
\text{if } x_{\mathrm{g}}<-\boldsymbol{x_{\mathrm{mrgdov}}} \begin{cases}
y_{\mathrm{g}}=-x_{\mathrm{g}} \\
z=\boldsymbol{x_1}\cdot y_{\mathrm{g}}/\boldsymbol{\xi_{\mathrm{dov}}} \\
\eta=\left[z+10-\sqrt{(z-6)^2+64}\right]\Big/2 \\
a=\left(y_{\mathrm{g}}-\eta\right)^2+\boldsymbol{G_{\mathrm{dov}}^2}\cdot(\eta+1) \\
c=2\cdot\left(y_{\mathrm{g}}-\eta\right)-\boldsymbol{G_{\mathrm{dov}}^2} \\
\tau=-\eta+\ln\left(a/\boldsymbol{G_{\mathrm{dov}}^2}\right) \\
y_0=\sigma_1(a,\,c,\,\tau,\,\eta) \\
\Delta_0=\exp\left(y_0\right) \\
p=2\cdot\left(y_{\mathrm{g}}-y_0\right)+\boldsymbol{G_{\mathrm{dov}}^2}\cdot\left(\Delta_0-1\right) \\
q=\left(y_{\mathrm{g}}-y_0\right)^2+\boldsymbol{G_{\mathrm{dov}}^2}\cdot\left(y_0-\Delta_0+1\right) \\
x_{\mathrm{dov}}=-y_0-\dfrac{2\cdot q}{p+\sqrt{p^2-2\cdot q\cdot\left(2-\boldsymbol{G_{\mathrm{dov}}^2}\cdot\Delta_0\right)}}
\end{cases} \\
\text{if } \left|x_{\mathrm{g}}\right|<\boldsymbol{x_{\mathrm{mrgdov}}} \left\{ x_{\mathrm{dov}}=x_{\mathrm{g}}/\boldsymbol{\xi_{\mathrm{dov}}} \right. \\
\text{if } x_{\mathrm{g}}>\boldsymbol{x_{\mathrm{mrgdov}}} \begin{cases}
\bar{x}=x_{\mathrm{g}}/\boldsymbol{\xi_{\mathrm{dov}}}\cdot\left[1+x_{\mathrm{g}}\cdot\left(\boldsymbol{\xi_{\mathrm{dov}}}\cdot\boldsymbol{x_1}-\boldsymbol{x_{\mathrm{dgl}}}\right)/\boldsymbol{x_{\mathrm{dgl}}^2}\right] \\
\omega=1-\exp\left(-\bar{x}\right) \\
x_0=x_{\mathrm{g}}+\boldsymbol{G_{\mathrm{dov}}^2}/2-\boldsymbol{G_{\mathrm{dov}}}\cdot\sqrt{x_{\mathrm{g}}+\boldsymbol{G_{\mathrm{dov}}^2}/4-\omega} \\
\Delta_0=\exp\left(-x_0\right) \\
p=2\cdot\left(x_{\mathrm{g}}-x_0\right)+\boldsymbol{G_{\mathrm{dov}}^2}\cdot\left(1-\Delta_0\right) \\
q=\left(x_{\mathrm{g}}-x_0\right)^2-\boldsymbol{G_{\mathrm{dov}}^2}\cdot\left(x_0+\Delta_0-1\right) \\
x_{\mathrm{dov}}=x_0+\dfrac{2\cdot q}{p+\sqrt{p^2-2\cdot q\cdot\left(2-\boldsymbol{G_{\mathrm{dov}}^2}\cdot\Delta_0\right)}}
\end{cases}
\end{cases}
$$

$$
\psi_{\mathrm{sov}}=-\boldsymbol{\phi_{\mathrm{T}}}\cdot x_{\mathrm{sov}}\left(-\frac{V_{\mathrm{GS}}}{\boldsymbol{\phi_{\mathrm{T}}}}\right)
$$

$$
\psi_{\mathrm{dov}}=-\boldsymbol{\phi_{\mathrm{T}}}\cdot x_{\mathrm{dov}}\left(-\frac{V_{\mathrm{GS}}-V_{\mathrm{DS}}}{\boldsymbol{\phi_{\mathrm{T}}}}\right)
$$

$$
V_{\mathrm{ov}_0}=V_{\mathrm{GS}}-\psi_{\mathrm{sov}}
$$

$$
V_{\mathrm{ov}_{\mathrm{L}}}=V_{\mathrm{GS}}-V_{\mathrm{DS}}-\psi_{\mathrm{dov}}
$$

© 2023 Cadence Design Systems, Inc.

Gate Current

The equations in this Section are only calculated when **SWIGATE** = 1.

Source/Drain gate overlap current

$$I_{\mathrm{GSov}}(V_{\mathrm{GX}},\,\psi_{\mathrm{ov}},\,V_{\mathrm{ov}}) = \begin{cases} V_{\mathrm{ov}}^{*} = \sqrt{V_{\mathrm{ov}}^{2} + 10^{-6}} \\ \psi_{\mathrm{tov}} = \mathrm{MINA}\,(0,\,V_{\mathrm{ov}} + \boldsymbol{D_{\mathrm{ov}}},\,0.01) \\ z_{\mathrm{g}} = \begin{cases} \mathrm{MINA}\left(\dfrac{V_{\mathrm{ov}}^{*}}{\mathbf{CHIB}},\,\boldsymbol{GC_{\mathrm{Q}}},\,10^{-6}\right) & \text{for } \mathbf{GC3} < 0 \\ \dfrac{V_{\mathrm{ov}}^{*}}{\mathbf{CHIB}} & \text{for } \mathbf{GC3} \geq 0 \end{cases} \\ \Delta_{\mathrm{Siov}} = \exp\left(\dfrac{3.0 \cdot \boldsymbol{\phi_{\mathrm{T}}} + \psi_{\mathrm{ov}} + \psi_{\mathrm{tov}}}{\boldsymbol{\phi_{\mathrm{T}}}}\right) \\ F_{\mathrm{Sov}} = \ln\left[\dfrac{1 + \Delta_{\mathrm{Siov}}}{1 + \Delta_{\mathrm{Siov}} \cdot \exp\left(-V_{\mathrm{GX}}/\boldsymbol{\phi_{\mathrm{T}}}\right)}\right] \\ I_{\mathrm{Gov}} = \boldsymbol{I_{\mathrm{GOV}}} \cdot F_{\mathrm{Sov}} \cdot \\ \qquad \exp\left(\boldsymbol{B_{\mathrm{ov}}} \cdot \left[-\dfrac{3}{2} + z_{\mathrm{g}} \cdot (\mathbf{GC2} + \mathbf{GC3} \cdot z_{\mathrm{g}})\right]\right) \end{cases}$$

$$I_{\mathrm{GDov}}(V_{\mathrm{GX}},\,\psi_{\mathrm{ov}},\,V_{\mathrm{ov}}) = \begin{cases} V_{\mathrm{ov}}^{*} = \sqrt{V_{\mathrm{ov}}^{2} + 10^{-6}} \\ \psi_{\mathrm{tov}} = \mathrm{MINA}\,(0,\,V_{\mathrm{ov}} + \boldsymbol{D_{\mathrm{ov}}},\,0.01) \\ z_{\mathrm{g}} = \begin{cases} \mathrm{MINA}\left(\dfrac{V_{\mathrm{ov}}^{*}}{\mathbf{CHIB}},\,\boldsymbol{GC_{\mathrm{Q}}},\,10^{-6}\right) & \text{for } \mathbf{GC3} < 0 \\ \dfrac{V_{\mathrm{ov}}^{*}}{\mathbf{CHIB}} & \text{for } \mathbf{GC3} \geq 0 \end{cases} \\ \Delta_{\mathrm{Siov}} = \exp\left(\dfrac{3.0 \cdot \boldsymbol{\phi_{\mathrm{T}}} + \psi_{\mathrm{ov}} + \psi_{\mathrm{tov}}}{\boldsymbol{\phi_{\mathrm{T}}}}\right) \\ F_{\mathrm{Sov}} = \ln\left[\dfrac{1 + \Delta_{\mathrm{Siov}}}{1 + \Delta_{\mathrm{Siov}} \cdot \exp\left(-V_{\mathrm{GX}}/\boldsymbol{\phi_{\mathrm{T}}}\right)}\right] \\ I_{\mathrm{Gov}} = \boldsymbol{I_{\mathrm{GOVD}}} \cdot F_{\mathrm{Sov}} \cdot \\ \qquad \exp\left(\boldsymbol{B_{\mathrm{dov}}} \cdot \left[-\dfrac{3}{2} + z_{\mathrm{g}} \cdot (\mathbf{GC2} + \mathbf{GC3} \cdot z_{\mathrm{g}})\right]\right) \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$I_{\mathrm{GSov}} = I_{\mathrm{GSov}}\left(V_{\mathrm{GS}},\, \psi_{\mathrm{sov}},\, V_{\mathrm{ov_0}}\right)$$

$$I_{\mathrm{GDov}} = I_{\mathrm{GDov}}\left(V_{\mathrm{GS}} - V_{\mathrm{DS}},\, \psi_{\mathrm{dov}},\, V_{\mathrm{ov_L}}\right)$$

Gate-channel current:

$$V_{\mathrm{m}} = V^{*}_{\mathrm{SB,dc}} + \phi^{*}_{\mathbf{T}} \cdot \left[\frac{x_{\mathrm{ds,dc}}}{2} - \ln\left(\frac{1+\exp(x_{\mathrm{ds,dc}} - V_{\mathrm{dse,dc}}/\phi^{*}_{\mathbf{T}})}{2}\right)\right]$$

$$\psi_{\mathrm{t}} = \mathrm{MINA}\left(0,\, V_{\mathrm{oxm,dc}} + \boldsymbol{D_{\mathbf{ch}}},\, 0.01\right)$$

$$V^{*}_{\mathrm{oxm}} = \sqrt{V^{2}_{\mathrm{oxm,dc}} + 10^{-6}}$$

$$z_{\mathrm{g}} = \begin{cases} \mathrm{MINA}\left(\dfrac{V^{*}_{\mathrm{oxm}}}{\mathbf{CHIB}},\, \boldsymbol{GC_{\mathbf{Q}}},\, 10^{-6}\right) & \textbf{for GC3} < 0 \\ \dfrac{V^{*}_{\mathrm{oxm}}}{\mathbf{CHIB}} & \textbf{for GC3} \geq 0 \end{cases}$$

$$\Delta_{\mathrm{Si}} = \exp\left(x_{\mathrm{m,dc}} - \frac{\boldsymbol{\alpha_{\mathbf{b}}} + V_{\mathrm{m}} - \psi_{\mathrm{t}}}{\phi^{*}_{\mathbf{T}}}\right)$$

$$F_{\mathrm{S}} = \ln\left[\frac{1+\Delta_{\mathrm{Si}}}{1+\Delta_{\mathrm{Si}}\cdot\exp\left(-\dfrac{V_{\mathrm{GS}} + V^{*}_{\mathrm{SB,dc}} - V_{\mathrm{m}}}{\phi^{*}_{\mathbf{T}}}\right)}\right]$$

$$I_{\mathrm{GCO}} = \boldsymbol{I_{\mathbf{GINV}}} \cdot F_{\mathrm{S}} \cdot \exp\left(B \cdot \left[-3/2 + z_{\mathrm{g}} \cdot (\mathbf{GC2} + \mathbf{GC3} \cdot z_{\mathrm{g}})\right]\right)$$

$$\text{if } x_{\mathrm{g,dc}} > 0 \begin{cases} u_0 = \mathbf{CHIB}/\left[B \cdot (\mathbf{GC2} + 2 \cdot \mathbf{GC3} \cdot z_{\mathrm{g}})\right] \\ x = \Delta\psi_{\mathrm{dc}}/\left(2 \cdot u_0\right) \\ b = u_0/H_{\mathrm{dc}} \\ B_{\mathrm{g}} = b \cdot (1-b)/2 \\ A_{\mathrm{g}} = 1/2 - 3 \cdot B_{\mathrm{g}} \\ p_{\mathrm{gc}} = (1-b) \cdot \dfrac{\sinh(x)}{x} + b \cdot \cosh(x) \\ p_{\mathrm{gd}} = \dfrac{p_{\mathrm{gc}}}{2} - B_{\mathrm{g}} \cdot \sinh(x) - A_{\mathrm{g}} \cdot \dfrac{\sinh(x)}{x} \cdot \left[\coth(x) \left| - \dfrac{1}{x}\right.\right] \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$\textbf{if } x_{\mathrm{g,dc}} \le 0 \begin{cases} p_{\mathrm{gc}} = 1 \\ p_{\mathrm{gd}} = 1/2 \end{cases}$$

$$S_{\mathrm{g}} = \frac{1}{2} \cdot \left(1 + \frac{x_{\mathrm{g,dc}}}{\sqrt{x_{\mathrm{g,dc}}^2 + 10^{-6}}} \right)$$

$$I_{\mathrm{GC}} = I_{\mathrm{GCO}} \cdot p_{\mathrm{gc}} \cdot S_{\mathrm{g}}$$

$$I_{\mathrm{GCD}} = I_{\mathrm{GCO}} \cdot p_{\mathrm{gd}} \cdot S_{\mathrm{g}}$$

$$I_{\mathrm{GCS}} = I_{\mathrm{GC}} - I_{\mathrm{GCD}}$$

$$I_{\mathrm{GB}} = I_{\mathrm{GCO}} \cdot p_{\mathrm{gc}} \cdot (1 - S_{\mathrm{g}})$$

© 2023 Cadence Design Systems, Inc.

Gate-Induced Drain/Source Leakage Current

The equations in this section are only calculated when **SWGIDL** = 1.

$$I_{\mathrm{gisl}}(V_{\mathrm{ov}}, V) = \begin{cases} V_{\mathrm{tov}} = \sqrt{V_{\mathrm{ov}}^2 + \mathbf{CGIDL}^2 \cdot V^2 + 10^{-6}} \\ t = V \cdot V_{\mathrm{tov}} \cdot V_{\mathrm{ov}} \\ I_{\mathrm{gisl}} = \begin{cases} -\mathbf{A_{GIDL}} \cdot t \cdot \exp\left(-\dfrac{\mathbf{B_{GIDL}}}{V_{\mathrm{tov}}}\right) & \text{for } V_{\mathrm{ov}} < 0 \\ 0 & \text{for } V_{\mathrm{ov}} \geq 0 \end{cases} \end{cases}$$

$$I_{\mathrm{gidl}}(V_{\mathrm{ov}}, V) = \begin{cases} V_{\mathrm{tov}} = \sqrt{V_{\mathrm{ov}}^2 + \mathbf{CGIDLD}^2 \cdot V^2 + 10^{-6}} \\ t = V \cdot V_{\mathrm{tov}} \cdot V_{\mathrm{ov}} \\ I_{\mathrm{gidl}} = \begin{cases} -\mathbf{A_{GIDLD}} \cdot t \cdot \exp\left(-\dfrac{\mathbf{B_{GIDLD}}}{V_{\mathrm{tov}}}\right) & \text{for } V_{\mathrm{ov}} < 0 \\ 0 & \text{for } V_{\mathrm{ov}} \geq 0 \end{cases} \end{cases}$$

$$I_{\mathrm{gisl}} = I_{\mathrm{gisl}}(V_{\mathrm{ov}_0}, V_{\mathrm{SB}})$$

$$I_{\mathrm{gidl}} = I_{\mathrm{gidl}}(V_{\mathrm{ovL}}, V_{\mathrm{DS}} + V_{\mathrm{SB}})$$

Total Terminal Currents

$$I_{\mathrm{D}} = I_{\mathrm{DS}} + I_{\mathrm{avl}} - I_{\mathrm{GDov}} - I_{\mathrm{GCD}} + I_{\mathrm{gidl}}$$

$$I_{\mathrm{S}} = -I_{\mathrm{DS}} - I_{\mathrm{GSov}} - I_{\mathrm{GCS}} + I_{\mathrm{gisl}}$$

$$I_{\mathrm{G}} = I_{\mathrm{GC}} + I_{\mathrm{GB}} + I_{\mathrm{GDov}} + I_{\mathrm{GSov}}$$

$$I_{\mathrm{B}} = -I_{\mathrm{avl}} - I_{\mathrm{GB}} - I_{\mathrm{gidl}} - I_{\mathrm{gisl}}$$

© 2023 Cadence Design Systems, Inc.

Charge Model

In this section, the charge model equations of the PSP-model are given. Use is made of the applied terminal bias values VGS, VDS and VSB, the local parameters listed in section “Intrinsic Parameters” and the internal parameters introduced in the Model Equations section. The parameters are denoted by capital characters in bold font, whereas internal (bias-independent) parameters are denoted by symbols in bold font.

Quantum-Mechanical Corrections

$$q_{\mathrm{eff,ac}} = \begin{cases} V_{\mathrm{oxm,ac}} & \text{for } x_{\mathrm{g,ac}} \leq 0 \\ q_{\mathrm{eff1},ac} & \text{for } x_{\mathrm{g,ac}} > 0 \end{cases}$$

$$C_{\mathrm{OX}}^{\mathrm{qm}} = \begin{cases} \mathbf{COX} & \text{for } q_{\mathbf{q}} = 0 \\ \dfrac{\mathbf{COX}}{1 + q_{\mathbf{q}} / ({q_{\mathrm{eff,ac}}}^2 + {q_{\mathbf{lim}}}^2)^{1/6}} & \text{for } q_{\mathbf{q}} > 0 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Intrinsic Charge Model

$$\text{if } x_{\mathrm{g}} > 0 \begin{cases} F_{\mathrm{j}} = \Delta\psi_{\mathrm{ac}} / \left(2 \cdot H_{\mathrm{ac}}\right) \\ q_{\Delta L} = \left(1 - G_{\Delta L,\mathrm{ac}}\right) \cdot \left(q_{\mathrm{im,ac}} - \alpha_{\mathrm{m,ac}} \cdot \Delta\psi_{\mathrm{ac}}/2\right) \\ q^{*}_{\Delta L} = q_{\Delta L,\mathrm{ac}} \cdot \left(1 + G_{\Delta L,\mathrm{ac}}\right) \\ Q_{\mathrm{G}}^{(i)} = C_{\mathrm{OX}}^{\mathrm{qm}} \cdot \left[V_{\mathrm{oxm,ac}} + \dfrac{\eta_{\mathrm{p,ac}} \cdot \Delta\psi_{\mathrm{ac}}}{2} \cdot \left(\dfrac{G_{\Delta L,\mathrm{ac}}}{3} \cdot F_{\mathrm{j}} + G_{\Delta L,\mathrm{ac}} - 1\right)\right] \\ Q_{\mathrm{I}}^{(i)} = -C_{\mathrm{OX}}^{\mathrm{qm}} \cdot \left[G_{\Delta L,\mathrm{ac}} \cdot \left(q_{\mathrm{im,ac}} + \dfrac{\alpha_{\mathrm{m,ac}} \cdot \Delta\psi_{\mathrm{ac}}}{6} \cdot F_{\mathrm{j}}\right) + q_{\Delta L,\mathrm{ac}}\right] \\ Q_{\mathrm{D}}^{(i)} = -\dfrac{C_{\mathrm{OX}}^{\mathrm{qm}}}{2} \cdot \left[G_{\Delta L,\mathrm{ac}}^{2} \cdot \left(q_{\mathrm{im,ac}} + \dfrac{\alpha_{\mathrm{m,ac}} \cdot \Delta\psi_{\mathrm{ac}}}{6} \cdot \left[\dfrac{F_{\mathrm{j}}^{2}}{5} + F_{\mathrm{j}} - 1\right]\right) + q^{*}_{\Delta L}\right] \end{cases}$$

$$\text{if } x_{\mathrm{g}} \leq 0 \begin{cases} Q_{\mathrm{G}}^{(i)} = C_{\mathrm{OX}}^{\mathrm{qm}} \cdot V_{\mathrm{oxm,ac}} \\ Q_{\mathrm{I}}^{(i)} = 0 \\ Q_{\mathrm{D}}^{(i)} = 0 \end{cases}$$

$$Q_{\mathrm{S}}^{(i)} = Q_{\mathrm{I}}^{(i)} - Q_{\mathrm{D}}^{(i)}$$

$$Q_{\mathrm{B}}^{(i)} = -Q_{\mathrm{I}}^{(i)} - Q_{\mathrm{G}}^{(i)}$$

© 2023 Cadence Design Systems, Inc.

Extrinsic Charge Model

The charges of the source and drain overlap regions:

$$Q_{\mathrm{sov}} = \mathbf{CGOV} \cdot (V_{\mathrm{GS}} - \psi_{\mathrm{sov}})$$

$$Q_{\mathrm{dov}} = \mathbf{CGOVD} \cdot (V_{\mathrm{GS}} - V_{\mathrm{DS}} - \psi_{\mathrm{dov}})$$

The charge of the bulk overlap region

$$Q_{\mathrm{bov}} = \mathbf{CGBOV} \cdot (V_{\mathrm{GS}} + V_{\mathrm{SB}})$$

Outer fringe charge:

$$Q_{\mathrm{ofs}} = \mathbf{CFR} \cdot V_{\mathrm{GS}}$$

$$Q_{\mathrm{ofd}} = \mathbf{CFRD} \cdot (V_{\mathrm{GS}} - V_{\mathrm{DS}})$$

Total Terminal Charges

$$Q_{\mathrm{G}} = Q_{\mathrm{G}}^{(i)} + Q_{\mathrm{sov}} + Q_{\mathrm{dov}} + Q_{\mathrm{ofs}} + Q_{\mathrm{ofd}} + Q_{\mathrm{bov}}$$

$$Q_{\mathrm{S}} = Q_{\mathrm{S}}^{(i)} - Q_{\mathrm{sov}} - Q_{\mathrm{ofs}}$$

$$Q_{\mathrm{D}} = Q_{\mathrm{D}}^{(i)} - Q_{\mathrm{dov}} - Q_{\mathrm{ofd}}$$

$$Q_{\mathrm{B}} = Q_{\mathrm{B}}^{(i)} - Q_{\mathrm{bov}}$$

© 2023 Cadence Design Systems, Inc.

Noise Model

Equations are only calculated for $x_g > 0$. In these equations f_{op} represents the operation frequency of the transistor and $j = \sqrt{-1}$

$$N^* = \frac{C_{\mathrm{ox}}}{q} \cdot \alpha_{\mathrm{m,dc}} \cdot \phi_{\mathbf{T}}$$

$$N^*_{\mathrm{m}} = \frac{C_{\mathrm{ox}}}{q} \cdot q^*_{\mathrm{im,dc}}$$

$$\Delta N = \frac{C_{\mathrm{ox}}}{q} \cdot \alpha_{\mathrm{m,dc}} \cdot \Delta\psi_{\mathrm{dc}}$$

$$S_{\mathrm{fl}} = \frac{q \cdot \phi_{\mathbf{T}}^2 \cdot \beta \cdot I_{\mathrm{DS}}}{(f_{\mathrm{op}})^{\mathbf{EF}} \cdot C_{\mathrm{ox}} \cdot G_{\mathrm{vsat,dc}} \cdot N^*} \cdot \left[(\mathbf{NFA} - \mathbf{NFB} \cdot N^* + \mathbf{NFC} \cdot N^{*2}) \cdot \ln\left(\frac{N^*_{\mathrm{m}} + \Delta N/2}{N^*_{\mathrm{m}} - \Delta N/2}\right) + \left(\mathbf{NFB} + \mathbf{NFC} \cdot [N^*_{\mathrm{m}} - 2 \cdot N^*]\right) \cdot \Delta N \right]$$

© 2023 Cadence Design Systems, Inc.

$$H_0 = \frac{q^*_{\mathrm{im,dc}}}{\alpha_{\mathrm{m,dc}}}$$

$$t_1 = \frac{q_{\mathrm{im,dc}}}{q^*_{\mathrm{im,dc}}}$$

$$t_2 = \left(\frac{\Delta\psi_{\mathrm{dc}}}{12 \cdot H_0}\right)^2$$

$$R = \frac{H_0}{H} - 1$$

$$l_{\mathrm{c}} = 1 - 12 \cdot t_2 \cdot R$$

$$g_{\mathrm{ideal}} = \frac{\beta \cdot q^*_{\mathrm{im,dc}}}{G_{\mathrm{vsat,dc}}} \cdot F_{\Delta L,\mathrm{dc}}$$

$$C_{\mathrm{Geff}} = \left(\frac{G_{\mathrm{vsat,ac}}}{G_{\mathrm{mob,ac}} \cdot G_{\Delta L,\mathrm{ac}}}\right)^2 \cdot C^{\mathrm{qm}}_{\mathrm{OX}} \cdot \eta_{\mathrm{p,ac}}$$

$$m_{\mathrm{id}} = \frac{g_{\mathrm{ideal}}}{l_{\mathrm{c}}^2} \cdot [t_1 + 12 \cdot t_2 - 24 \cdot (1 + t_1) \cdot t_2 \cdot R]$$

$$S_{th} = N_I \cdot m_{id}$$

$$m_{\mathrm{ig}} = \frac{1}{l_{\mathrm{c}}^2 \cdot g_{\mathrm{ideal}}} \cdot \left[\frac{t_1}{12} - t_2 \cdot \left(t_1 + \frac{1}{5} - 12 \cdot t_2\right) - \frac{8}{5} \cdot t_2 \cdot (t_1 + 1 - 12 \cdot t_2) \cdot R\right]$$

$$S_{\mathrm{ig}} = \boldsymbol{N_{\mathrm{T}}} \cdot \frac{(2 \cdot \pi \cdot f_{\mathrm{op}} \cdot C_{\mathrm{Geff}})^2 \cdot m_{\mathrm{ig}}}{1 + (2 \cdot \pi \cdot f_{\mathrm{op}} \cdot C_{\mathrm{Geff}} \cdot m_{\mathrm{ig}})^2}$$

$$m_{\mathrm{igid}} = \frac{\sqrt{t_2}}{l_{\mathrm{c}}^2} \cdot \left[1 - 12 \cdot t_2 - \left(t_1 + \frac{96}{5} \cdot t_2 - 12 \cdot t_1 \cdot t_2\right) \cdot R\right]$$

$$S_{\mathrm{ig}th} = \boldsymbol{N_{\mathrm{T}}} \cdot \frac{2 \cdot \pi \cdot j \cdot f_{\mathrm{op}} \cdot C_{\mathrm{Geff}} \cdot m_{\mathrm{igid}}}{1 + 2 \cdot \pi \cdot j \cdot f_{\mathrm{op}} \cdot C_{\mathrm{Geff}} \cdot m_{\mathrm{ig}}}$$

© 2023 Cadence Design Systems, Inc.

Noise Source

$$Sthd = N_T \times m_{id}$$

$$igig = N_T \times m_{ig}$$

If correlation noise is turned on,

$$idid = N_T \times m_{id} \times (1 - c_igid^2)$$

If correlation noise is turned off,

$$idid = N_T \times m_{id}$$

Gate current shot noise

$$S_{hotgs} = 2 \cdot q \cdot (I_{GCS} + I_{GSov})$$

$$S_{hotgd} = 2 \cdot q \cdot (I_{GCD} + I_{GDov})$$

Avalanche current shot noise

$$S_{jnoise} = 2 \cdot q \cdot I_{js}$$

$$D_{jnoise} = 2 \cdot q \cdot ((1 + M_{avl}) \cdot I_{avl} + I_{jd})$$

© 2023 Cadence Design Systems, Inc.

Thermal noise for parasitic resistances

$$S_{\mathrm{R_G}} = 4 \cdot k_{\mathrm{B}} \cdot T_{\mathrm{KD}} / R_{\mathrm{gate}}$$

$$S_{\mathrm{R_{BULK}}} = 4 \cdot k_{\mathrm{B}} \cdot T_{\mathrm{KD}} / R_{\mathrm{bulk}}$$

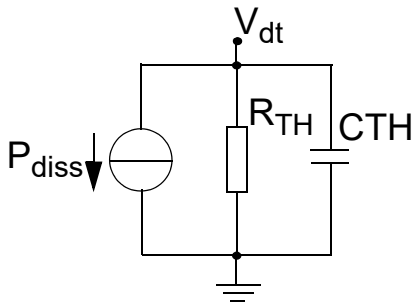
$$S_{\mathrm{R_{WELL}}} = 4 \cdot k_{\mathrm{B}} \cdot T_{\mathrm{KD}} / R_{\mathrm{well}}$$

$$S_{\mathrm{R_{JUNS}}} = 4 \cdot k_{\mathrm{B}} \cdot T_{\mathrm{KD}} / R_{\mathrm{juns}}$$

$$S_{\mathrm{R_{JUND}}} = 4 \cdot k_{\mathrm{B}} \cdot T_{\mathrm{KD}} / R_{\mathrm{jund}}$$

Self Heating

The figure below shows the simple thermal network that is implemented in PSP.



The current that reflects the power dissipation is given by:

$$Pdiss = I_{DS} \cdot V_{DS} + I_{impact} \cdot (V_{DS} + V_{SB}) + \frac{V_{SIS}^2}{R_{source}} + \frac{V_{DID}^2}{R_{drain}}$$

If Rth<10^{-3}, Pdiss=0. This can be used to switch off self heating.

The built-in thermal network of PSP can be bypassed (for example, replace it with an externally-connected thermal network) by setting CTH=0 and assigning a large value to RTH.

© 2023 Cadence Design Systems, Inc.

Non-quasi-static RF model

For high-frequency modeling and fast transient simulations, a special version of the PSP model is available, which enables the simulation of non-quasi-static (NQS) effects, and includes several parasitic resistances.

NQS-effects

In the PSP-NQS model, NQS-effects are introduced by applying the one-dimensional current continuity equation ($\partial_I/\partial_y \times \alpha - \partial_p/\partial_t$) to the channel. A full numerical solution of this equation is too inefficient for compact modeling, therefore an approximate technique is used. The channel is partitioned into N + 1 sections of equal length by assigning N equidistant collocation points. The charge density (per unit channel area) along the channel is then approximated by a cubic spline through these collocation points, assuring that both the charge and its first and second spatial derivatives are continuous a long the channel. Within this approximation, the current continuity equation reduces to a system of N coupled first order ordinary differential equations, from which the channel charge at each collocation point can be found:

$$\begin{cases} \dfrac{\mathrm{d}Q_1}{\mathrm{d}t} &= f_1(Q_1,\ldots,Q_N) \\ \vdots & \vdots \\ \dfrac{\mathrm{d}Q_N}{\mathrm{d}t} &= f_N(Q_1,\ldots,Q_N) \end{cases}$$

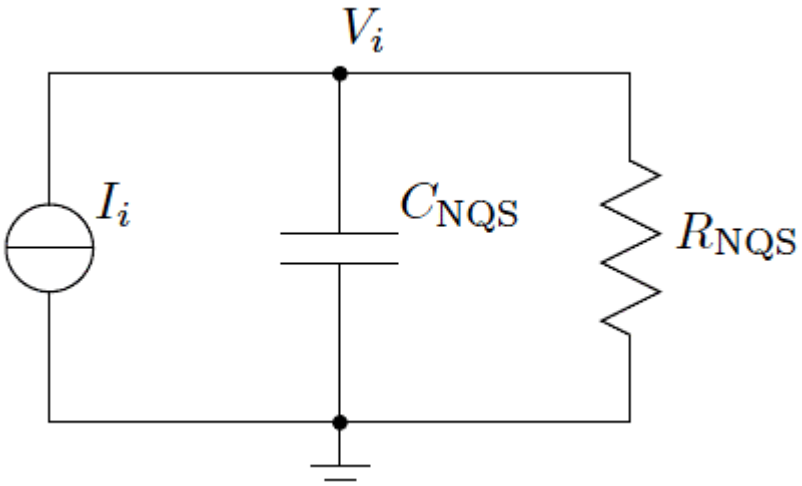
Here, Q_i is the charge density at the i-th collocation point and fi are functions, which contain the complete PSP-charge model. These equations are implemented by the definition of appropriate subcircuits (see left part of figure below) and solved by the circuit simulator. Finally, the four terminal charges are calculated from the channel charges, using the Ward-Dutton partitioning scheme for the source and drain charges.

NQS Model Equations

In this section, several symbols and notations are used which were defined in Section 4. Moreover, y denotes the (normalized) position along the channel (y = 0 is source side, y = 1 is drain side), while x denotes the surface potential (normalized to φ*T) at a certain position.

© 2023 Cadence Design Systems, Inc.

Figure 25-6 The subcircuit used to solve one of the differential equations



The current is set to $I_i = C_{NQS} \cdot f(V_1, \ldots, V_N)$, where the voltage V_i represents the charge density Q_i at the i-th collocation point and is solved by the circuit simulator. N of these circuits are defined and they are coupled through the dependence of Ii on the voltages of the other circuits. The resistance R_{NQS} has a large value and is present only for convergence purposes. Right: The full network of parasitic elements in the PSP-NQS model. The large full dots indicate the five additional internal nodes.

Internal constants

Equations in this section are independent of bias conditions and time. Consequently, they have to be computed only once.

Note: In PSP only **SWNQS** = 0, 1, 2, 3, 5, 9 are allowed.

$$n = \mathbf{SWNQS} + 1$$

$$h = 1/n$$

The matrix A is a square (n + 1) × (n + 1)-matrix with elements $A_{i,j}$ ($0 \le i, i \le n$), which are used in equations. They are computed using the following algorithm:

© 2023 Cadence Design Systems, Inc.

Initial values

$$A_{i,j} = 0 \qquad \text{for } 0 \le i, j \le n$$

$$v_i = 0 \qquad \text{for } 0 \le i \le n$$

First loop

$$\left.\begin{aligned} p &= 2 + v_{i-1}/2 \\ v_i &= -1/(2 \cdot p) \\ A_{i,i-1} &= 1/h \\ A_{i,i} &= -2/h \\ A_{i,i+1} &= 1/h \\ A_{i,j} &= \frac{1}{p} \cdot (3 \cdot A_{i,j}/h - A_{i-1,j}/2) \end{aligned} \right\} \text{for } j = 0 \ldots n \Bigg\} \text{for } i = 1 \ldots (n-1)$$

Second loop (back substitution)

$$A_{i,j} = v_i \cdot A_{i+1,j} + A_{i,j} \qquad \text{for } j = 0 \ldots n \Bigg\} \text{for } i = (n-1) \ldots 0$$

Position independent quantities

© 2023 Cadence Design Systems, Inc.

The following quantities depend on the bias conditions, but are constant along the channel:

$$\text{if } x_{\mathrm{g,ac}} > 0 \begin{cases} y_{\mathrm{m}} = \dfrac{1}{2} \cdot \left(1 + \dfrac{\Delta\psi_{\mathrm{ac}}}{4 \cdot H_{\mathrm{ac}}}\right) \\ p_{\mathrm{d}} = \dfrac{x_{\mathrm{gm,ac}}}{x_{\mathrm{g,ac}} - x_{\mathrm{m,ac}}} \\ G_{\mathrm{p}} = G_{\mathrm{ac}} / p_{\mathrm{d}} \end{cases}$$

$$\text{if } x_{\mathrm{g,ac}} \leq 0 \begin{cases} y_{\mathrm{m}} = 1/2 \\ p_{\mathrm{d}} = 1 \\ G_{\mathrm{p}} = G_{\mathrm{ac}} \end{cases}$$

$$a_{\mathrm{p}} = 1 + G_{\mathrm{p}} / \sqrt{2}$$

$$p_{\mathrm{mrg}} = 10^{-5} \cdot a_{\mathrm{p}}$$

Position dependent surface potential and charge

Interpolated (quasi-static) surface potential along the channel:

$$\Psi(y) = x_{\mathrm{m,ac}} + \frac{H_{\mathrm{ac}}}{\phi_{\mathbf{T}}^{*}} \cdot \left(1 - \sqrt{1 - \frac{2 \cdot \Delta\psi_{\mathrm{ac}}}{H_{\mathrm{ac}}} \cdot (y - y_{\mathrm{m}})}\right)$$

© 2023 Cadence Design Systems, Inc.

Normalized bulk-charge and its first two derivatives as functions of surface potential:

$$q_{\mathrm{b}}(x) = -\mathrm{sgn}(x) \cdot G_{\mathrm{p}} \cdot \sqrt{\exp(-x) + x - 1}$$

$$q'_{\mathrm{b}}(x) = \frac{G_{\mathrm{p}}^2 \cdot [1 - \exp(-x)]}{2 \cdot q_{\mathrm{b}}(x)}$$

$$q''_{\mathrm{b}}(x) = -q'_{\mathrm{b}}(x) - \frac{q'_{\mathrm{b}}(x)^2 - G_{\mathrm{p}}^2/2}{q_{\mathrm{b}}(x)}$$

© 2023 Cadence Design Systems, Inc.

Surface potential as a function of normalized inversion charge

$$\Pi(x_{\mathrm{g}}) = \begin{cases} \text{if } x_{\mathrm{g}} < -p_{\mathrm{mrg}} & \begin{cases} y_{\mathrm{g}} = -x_{\mathrm{g}} \\ z = 1.25 \cdot y_{\mathrm{g}}/a_{\mathrm{p}} \\ \eta = \left[z + 10 - \sqrt{(z-6)^2 + 64}\right]/2 \\ a = (y_{\mathrm{g}} - \eta)^2 + G_{\mathrm{p}}^2 \cdot (\eta + 1) \\ c = 2 \cdot (y_{\mathrm{g}} - \eta) - G_{\mathrm{p}}^2 \\ \tau = -\eta + \ln\left(a/G_{\mathrm{p}}^2\right) \\ y_0 = \sigma_1(a,\, c,\, \tau,\, \eta) \\ \Delta_0 = \exp(y_0) \\ \xi = 1 - G_{\mathrm{p}}^2 \cdot \Delta_0/2 \\ p = 2 \cdot (y_{\mathrm{g}} - y_0) + G_{\mathrm{p}}^2 \cdot (\Delta_0 - 1) \\ q = (y_{\mathrm{g}} - y_0)^2 + G_{\mathrm{p}}^2 \cdot (y_0 - \Delta_0 + 1) \\ \Pi = -y_0 - \dfrac{2 \cdot q}{p + \sqrt{p^2 - 4 \cdot q \cdot \xi}} \end{cases} \\ \text{if } |x_{\mathrm{g}}| \le p_{\mathrm{mrg}} & \Pi = \dfrac{x_{\mathrm{g}}}{a_{\mathrm{p}}} \\ \text{if } x_{\mathrm{g}} > p_{\mathrm{mrg}} & \begin{cases} \hat{x}_{\mathrm{g1}} = x_{\mathbf{1}} + G_{\mathrm{p}} \cdot \sqrt{\exp(-x_{\mathbf{1}}) + x_{\mathbf{1}} - 1} \\ \bar{x} = \dfrac{x_{\mathrm{g}}}{a_{\mathrm{p}}} \cdot \left[1 + x_{\mathrm{g}} \cdot (x_{\mathbf{1}} \cdot a_{\mathrm{p}}/\hat{x}_{\mathrm{g1}} - 1)/\hat{x}_{\mathrm{g1}}\right] \\ x_0 = x_{\mathrm{g}} + G_{\mathrm{p}}^2/2 - G_{\mathrm{p}} \cdot \sqrt{x_{\mathrm{g}} + G_{\mathrm{p}}^2/4 - 1 + \exp(-\bar{x})} \\ \Delta_0 = \exp(-x_0) \\ \xi = 1 - G_{\mathrm{p}}^2 \cdot \Delta_0/2 \\ p = 2 \cdot (x_{\mathrm{g}} - x_0) + G_{\mathrm{p}}^2 \cdot (1 - \Delta_0) \\ q = (x_{\mathrm{g}} - x_0)^2 - G_{\mathrm{p}}^2 \cdot (x_0 + \Delta_0 - 1) \\ \Pi = x_0 + \dfrac{2 \cdot q}{p + \sqrt{p^2 - 4 \cdot q \cdot \xi}} \end{cases} \end{cases}$$

$$X(x_{\mathrm{g}}, q_{\mathrm{inv}}) = \Pi(x_{\mathrm{g}} + q_{\mathrm{inv}}/p_{\mathrm{d}})$$

© 2023 Cadence Design Systems, Inc.

Auxiliary functions

$$q(x) = -p_{\mathrm{d}} \cdot (x_{\mathrm{g}} - x) - q_{\mathrm{b}}(x)$$

$$\psi(q, q_{x1}) = \frac{q}{q_{x1}} - 1$$

$$\phi(q, q_{x1}, q_{x2}) = \left(1 - \frac{q \cdot q_{x2}}{q_{x1}^2}\right) / q_{x1}$$

Normalized right-hand side of continuity equation

$$f(x_{\mathrm{g}}, q, q', q'') = \left\{ \begin{array}{l} x_{\mathrm{z}} = X(x_{\mathrm{g}}, q) \\ q_{x1} = \dfrac{\partial q}{\partial x}(x_{\mathrm{z}}) = p_{\mathrm{d}} - q_{\mathrm{b}}'(x_{\mathrm{z}}) \\ q_{x2} = \dfrac{\partial^2 q}{\partial x^2}(x_{\mathrm{z}}) = q_{\mathrm{b}}''(x_{\mathrm{z}}) \\ f_0 = \psi(q, q_{x1}) \cdot q'' + \phi(q, q_{x1}, q_{x2}) \cdot q'^2 \\ x_{y1} = \dfrac{\partial x_{\mathrm{z}}}{\partial y} = q' / q_{x1} \\ z_{\mathrm{sat}} = \left\{ \begin{array}{ll} \left(\theta^*_{\mathrm{sat,ac}} \cdot \phi^{\dagger}_{\mathbf{T}} \cdot x_{y1}\right)^2 & \text{for NMOS} \\ \dfrac{\left(\theta^*_{\mathrm{sat,ac}} \cdot \phi^{\dagger}_{\mathbf{T}} \cdot x_{y1}\right)^2}{1 + \theta^*_{\mathrm{sat,ac}} \cdot \Delta\psi_{\mathrm{ac}}} & \text{for PMOS} \end{array} \right. \\ \zeta = \sqrt{1 + 2 \cdot z_{\mathrm{sat}}} \\ F_{\mathrm{vsat}} = 2/(1 + \zeta) \\ f = F_{\mathrm{vsat}} \cdot \left[f_0 - F_{\mathrm{vsat}} \cdot \dfrac{z_{\mathrm{sat}}}{\zeta} \cdot \psi(q, q_{x1}) \cdot (q'' + x_{y1}^2 \cdot q_{\mathrm{b}}''(x_{\mathrm{z}})) \right] \end{array} \right.$$

Normalization constant:

$$T_{\mathrm{norm}} = \frac{\mathbf{MUNQS} \cdot \phi^{\dagger}_{\mathbf{T}} \cdot \beta}{C^{\mathrm{qm}}_{\mathrm{OX}}} \cdot G_{\mathrm{mob,ac}} \cdot G_{\Delta L,\mathrm{ac}}$$

© 2023 Cadence Design Systems, Inc.

Cubic spline interpolation

Using cubic spline interpolation, the spatial derivatives $\frac{\partial_{qi}}{\partial_y} \cdot (t)$ and $\frac{\partial^2 qi}{\partial_{y^2}} \cdot (t)$ can be expressed as functions of $q_i(t)$.

$$q_0'' = 0$$

$$q_n'' = 0$$

$$q_i'' = \sum_{j=0}^{n} A_{i,j} \cdot q_i \qquad \text{for } 1 \le i \le n-1$$

$$q_i' = \frac{q_{i+1} - q_i}{h} - \frac{h}{6} \cdot (2 \cdot q_i'' + q_{i+1}'') \qquad \text{for } 1 \le i \le n-1$$

Continuity equation

Initial value for the q_i $(0 \le i \le n)$. These values are used for the DC operating point.

$$x_{i,0} = \Psi(i \cdot h)$$

$$q_{i,0} = q(x_{i,0})$$

Note: $x_{0,0} = x_s$ and $x_{n,0} = x_d$. Moreover, these values coincide with those in the quasi-static part of PSP.

The core of the NQS-model is the solution of q(y, t) from the charge continuity equation along the channel. By approximating the y-dependence by a cubic spline through a number of collocation points, the problem is reduced to solving the $q_i(t)$ from the following set of coupled differential equations.

$$\begin{cases} \frac{\partial q_i}{\partial t}(t) + T_{\text{norm}} \cdot f\left(x_{\text{g,ac}},\, q_i(t),\, \frac{\partial q_i}{\partial y}(t),\, \frac{\partial^2 q_i}{\partial y^2}(t)\right) = 0 & \text{for } 1 \le i \le n-1 \\ q_i(0) = q_{i,0} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

The boundary points $q_0(t) = q(x_s) = q_{is}$ and $q_n(t) = q(x_d) = q_{id}$ remain fixed to their quasi-static values; they are not solved from the equation above. The set of differential equations defined above is solved by the circuit simulator via the subcircuits shown in the left part of Figure 25-6.

Non-quasi-static terminal charges

Once the q_i are known, the NQS terminal charges can be computed:

$$S_0 = \sum_{i=1}^{n-1} q_i$$

$$S_2 = \sum_{i=1}^{n-1} q_i''$$

$$q_{\mathrm{I}}^{\mathrm{NQS}} = \int_0^1 q(y)\,\mathrm{d}y = h \cdot S_0 + \frac{h}{2} \cdot (u_0 + u_n) - \frac{h^3}{12} \cdot S_2$$

$$U_0 = \sum_{i=1}^{n-1} i \cdot q_i$$

$$U_2 = \sum_{i=1}^{n-1} i \cdot q_i''$$

$$q_{\mathrm{D}}^{\mathrm{NQS}} = \int_0^1 y \cdot q(y)\,\mathrm{d}y = h^2 \cdot U_0 + \frac{h^2}{6} \cdot [q_0 + (3n-1)u_n] - \frac{h^4}{12} \cdot U_2$$

$$q_{\mathrm{S}}^{\mathrm{NQS}} = q_{\mathrm{I}}^{\mathrm{NQS}} - q_{\mathrm{D}}^{\mathrm{NQS}}$$

Currently, only **SWNQS** = 0, 1, 2, 3, 5, 9 are allowed. For odd values of **SWNQS** the gate charge is integrated along the channel using Simpson's Rule. If **SWNQS** = 2, Simpson's 3/8-rule is used.

© 2023 Cadence Design Systems, Inc.

If **SWNQS** is odd (that is, n is even):

$$q_{\mathrm{G}}^{\mathrm{NQS}} = p_{\mathrm{d}} \cdot \left[x_{\mathrm{g,ac}} - \frac{h}{3} \cdot \left(X(x_{\mathrm{g,ac}}, q_0) + 4 \cdot \sum_{i=1}^{n/2} X(x_{\mathrm{g,ac}}, q_{2i-1}) + 2 \cdot \sum_{i=1}^{n/2-1} X(x_{\mathrm{g,ac}}, q_{2i}) + X(x_{\mathrm{g,ac}}, q_n) \right) \right]$$

If **SWNQS** = 2 (that is, n = 3):

$$q_{\mathrm{G}}^{\mathrm{NQS}} = p_{\mathrm{d}} \cdot \left[x_{\mathrm{g,ac}} - \frac{3 \cdot h}{8} \cdot (X(x_{\mathrm{g,ac}}, q_0) + 3 \cdot X(x_{\mathrm{g,ac}}, q_1) + 3 \cdot X(x_{\mathrm{g,ac}}, q_2) + X(x_{\mathrm{g,ac}}, q_3)) \right]$$

Converting back to conventional units:

$$Q_{\mathrm{S}}^{\mathrm{NQS}} = C_{\mathrm{OX}}^{\mathrm{qm}} \cdot \phi_{\mathbf{T}}^{*} \cdot q_{\mathrm{S}}^{\mathrm{NQS}}$$

$$Q_{\mathrm{D}}^{\mathrm{NQS}} = C_{\mathrm{OX}}^{\mathrm{qm}} \cdot \phi_{\mathbf{T}}^{*} \cdot q_{\mathrm{D}}^{\mathrm{NQS}}$$

$$Q_{\mathrm{G}}^{\mathrm{NQS}} = C_{\mathrm{OX}}^{\mathrm{qm}} \cdot \phi_{\mathbf{T}}^{*} \cdot q_{\mathrm{G}}^{\mathrm{NQS}}$$

$$Q_{\mathrm{B}}^{\mathrm{NQS}} = -(Q_{\mathrm{S}}^{\mathrm{NQS}} + Q_{\mathrm{D}}^{\mathrm{NQS}} + Q_{\mathrm{G}}^{\mathrm{NQS}})$$

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

1	`l=10e-6 m`	Design length.
2	`w=10e-6 m`	Design width.
3	`sa=0.0 m`	Distance between OD-edge and poly from one side.
4	`sb=0.0 m`	Distance between OD-edge and poly from other side.
5	`sd=0.0 m`	Distance between neighboring fingers.
6	`sca=0.0`	Integral of the first distribution function for scattered well dopants.
7	`scb=0.0`	Integral of the second distribution function for scattered well dopants.
8	`scc=0.0`	Integral of the third distribution function for scattered well dopants.
9	`sc=0.0 m`	Distance between OD-edge and nearest well edge.
10	`nf=1`	Number of fingers.
11	`ngcon=1.0`	Number of gate contacts.
12	`xgw=1.0E-7 m`	Distance from the gate contact to the channel edge.
13	`nrs=0.0`	Number of squares of source diffusion.
14	`nrd=0.0`	Number of squares of drain diffusion.
15	`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
16	`trise=0.0 K`	Temperature rise from ambient.
17	`jw=1E-6 m`	Gate-edge length of source/drain junction.
18	`delvto=0.0 V`	Threshold voltage shift parameter.
19	`factuo=1.0`	Zero-field mobility pre-factor.
20	`delvtoedge=0.0 V`	Threshold voltage shift parameter of edge transistor.
21	`factuoedge=1.0`	Zero-field mobility pre-factor of edge transistor.
22	`absource=1E-12` m^2	Bottom area of source junction.
23	`lssource=1E-6 m`	STI-edge length of source junction.
24	`lgsource=1E-6 m`	Gate-edge length of source junction.

© 2023 Cadence Design Systems, Inc.

25	abdrain=1E-12 m^2	Bottom area of drain junction.
26	lsdrain=1E-6 m	STI-edge length of drain junction.
27	lgdrain=1E-6 m	Gate-edge length of drain junction.
28	as=1E-12 m^2	Bottom area of source junction.
29	ps=1E-6 m	Perimeter of source junction.
30	ad=1E-12 m^2	Bottom area of drain junction.
31	pd=1E-6 m	Perimeter of drain junction.
32	mult=1.0	Number of devices in parallel.
33	mulid0=1	Ids multiplier.
34	m=1.0	Multiplicity factor.
35	ifactor=1.0	Multiplier for current.
36	cfactor=1.0	Multiplier for depletion capacitance.
37	isnoisy=yes	Should device generate noise. Possible values are yes and no.

Model Definition

```
model modelName psp103 parameter=value ...
```

Model Parameters

1	level=103	Model level.
2	type=n	Channel type parameter, n=NMOS p=PMOS. Possible values are n and p.
3	tr=value of tnom C	Nominal (reference) temperature.
4	tref=value of tnom C	Nominal (reference) temperature.
5	swnqs=0	Flag for NQS. 0 means off. 1, 2, 3, 5, or 9, number of collocation points.
6	swgeo=1	Flag for geometrical model, 0=local, 1=global, 2=binning.

© 2023 Cadence Design Systems, Inc.

7	`swigate=0`	Flag for gate current, 0 means turn off gate current.
8	`swimpact=0`	Flag for impact ionization current. 0 means turn off impact ionization.
9	`swgidl=0`	Flag for GIDL current. 0 means turn off IGIDL.
10	`swjuncap=0`	Flag for juncap, 0,turn off juncap.
11	`swjunasym=0`	Flag for asymmetric junctions; 0 means symmetric, 1 means asymmetric.
12	`swnud=0`	Flag for NUD-effect. Possible values are: `0`: off `1`: on `2`: on+CV-correction.
13	`swedge=0.0`	Flag for drain current of edge transistors. Possible values are `0=off` and `1=on`.
14	`swdelvtac=0`	Flag for separate capacitance calculation. Possible values are `0`: off and `1`: on.
15	`swign=1.0`	Flag for induced gate noise. `0` means off and `1` means on.
16	`swfix=0`	Flag for fixes introduced in PSP103.8.2.
17	`qmc=1.0`	Quantum-mechanical correction factor.
18	`version=103.0`	This parameter accepts only a real number values, for example, use 103.11 for the 103.1.1 version. The available versions are 103.0, 103.1, 103.11 (103.1.1), 103.2, 103.3, 103.4, 103.5, 103.6, and 103.7.
19	`minr=0.0`	Minimum resistance.
20	`mvt=0.0`	DCmatch parameter.
21	`mvto=0.0`	DCmatch parameter.
22	`mbe=0.0`	DCmatch parameter.
23	`mbeo=0.0`	DCmatch parameter.
24	`vfb=-1.0 V`	Flat band voltage at TR.
25	`stvfb=5.0e-4 V/K`	Temperature dependence of VFB.
26	`tox=2.0e-09 m`	Gate oxide thickness.

© 2023 Cadence Design Systems, Inc.

27	epsrox=3.9	Relative permittivity of gate dielectric.
28	neff=5.0e+23 m^{-3}	Effective substrate doping.
29	facneffac=1.0	Pre-factor for effective substrate doping in separate charge calculation.
30	gfacnud=1.0	Bodyfactor change due to NUD-effect.
31	vsbnud=0.0 V	Lower Vsb value for NUD-effect.
32	dvsbnud=1.0 V	Vsb-range for NUD-effect.
33	vnsub=0.0 V	Effective doping bias-dependence parameter.
34	nslp=0.05 V	Effective doping bias-dependence parameter.
35	dnsub=0.0 V^-1	Effective doping bias-dependence parameter.
36	dphib=0.0 V	Offset parameter for PHIB.
37	delvtac=0.0 V	Offset parameter for PHIB in separate charge calculation.
38	np=1.0e+26 m^{-3}	Gate poly-silicon doping.
39	ct=0.0	Interface states factor.
40	toxov=2.0e-09 m	Overlap oxide thickness.
41	toxovd=2.0e-09 m	Overlap oxide thickness for drain side.
42	nov=5.0e+25 m^{-3}	Effective doping of overlap region.
43	novd=5.0e+25 m^{-3}	Effective doping of overlap region for drain side.
44	cf=0.0	DIBL parameter.
45	cfb=0.0 V^-1	Back bias dependence of CF.
46	betn=7e-2 m^2/V/s	Channel aspect ratio times zero-field mobility.
47	stbet=1.0	Temperature dependence of BETN.
48	mue=0.5 m/V	Mobility reduction coefficient at TR.
49	stmue=0.0	Temperature dependence of MUE.
50	themu=1.5	Mobility reduction exponent at TR.
51	stthemu=1.5	Temperature dependence of THEMU.
52	cs=0.0	Coulomb scattering parameter at TR.
53	stcs=0.0	Temperature dependence of CS.

© 2023 Cadence Design Systems, Inc.

54	`xcor=0.0 V^-1`	Non-universality factor.
55	`stxcor=0.0`	Temperature dependence of XCOR.
56	`feta=1.0`	Effective field parameter.
57	`rs=30 Ω`	Series resistance at TR.
58	`strs=1.0`	Temperature dependence of RS.
59	`rsb=0.0 V^-1`	Back-bias dependence of series resistance.
60	`rsg=0.0 V^-1`	Gate-bias dependence of series resistance.
61	`thesat=1.0 V^-1`	Velocity saturation parameter at TR.
62	`stthesat=1.0`	Temperature dependence of THESAT.
63	`thesatb=0.0 V^-1`	Back-bias dependence of velocity saturation.
64	`thesatg=0.0 V^-1`	Gate-bias dependence of velocity saturation.
65	`ax=3.0`	Linear/saturation transition factor.
66	`alp=0.01`	CLM pre-factor.
67	`alp1=0.00 V`	CLM enhancement factor above threshold.
68	`alp2=0.00 V^-1`	CLM enhancement factor below threshold.
69	`vp=0.05 V`	CLM logarithm dependence factor.
70	`a1=1.0`	Impact-ionization pre-factor.
71	`a2=10.0 V`	Impact-ionization exponent at TR.
72	`sta2=0.0 V`	Temperature dependence of A2.
73	`a3=1.0`	Saturation-voltage dependence of impact-ionization.
74	`a4=0.0 V^-0.5`	Back-bias dependence of impact-ionization.
75	`gco=0.0`	Gate tunneling energy adjustment.
76	`iginv=0.0 A`	Gate channel current pre-factor.
77	`igov=0.0 A`	Gate overlap current pre-factor.
78	`igovd=0.0 A`	Gate overlap current pre-factor for drain side.
79	`stig=2.0`	Temperature dependence of IGINV and IGOV.
80	`gc2=0.375`	Gate current slope factor.
81	`gc3=0.063`	Gate current curvature factor.
82	`chib=3.1 V`	Tunneling barrier height.

© 2023 Cadence Design Systems, Inc.

83	agidl=0.0 A/V^3	GIDL pre-factor.
84	agidld=0.0 A/V^3	GIDL pre-factor for drain side.
85	bgidl=41.0 V	GIDL probability factor at TR.
86	bgidld=41.0 V	GIDL probability factor at TR for drain side.
87	stbgidl=0.0 V/K	Temperature dependence of BGIDL.
88	stbgidld=0.0 V/K	Temperature dependence of BGIDL for drain side.
89	cgidl=0.0	Back-bias dependence of GIDL.
90	cgidld=0.0	Back-bias dependence of GIDL for drain side.
91	cox=1.0e-14 F	Oxide capacitance for intrinsic channel.
92	cgov=1.0e-15 F	Oxide capacitance for gate-drain/source overlap.
93	cgovd=1.0e-15 F	Oxide capacitance for gate-drain overlap.
94	cgbov=0.0 F	Oxide capacitance for gate-bulk overlap.
95	cfr=0.0 F	Outer fringe capacitance.
96	cfrd=0.0 F	Outer fringe capacitance for drain side.
97	fcgovacc=0.0	Factor for overlap capacitances in accumulation regime.
98	fcgovaccd=0.0	Factor for overlap capacitances in accumulation regime for drain side.
99	cgovaccg=1.0	Gate voltage dependence parameter of overlap capacitances in accumulation regime.
100	cinr=0.0 F	Inner fringe capacitance.
101	cinrd=0.0 F	Inner fringe capacitance for drain side.
102	dvfbinr=0.0 V	Flat-band voltage offset of inner fringe capacitances.
103	fcinrdep=0.3	Bias dependence parameter of inner fringe capacitances in depletion regime.
104	fcinracc=0.5	Bias dependence parameter of inner fringe capacitances in accumulation regime.
105	axinr=0.5	Accumulation/depletion transition factor of inner fringe capacitances.
106	fnt=1.0	Thermal noise coefficient.
107	FNTEXC=0.0	Excess noise coefficient.

© 2023 Cadence Design Systems, Inc.

108	`nfa=8.0e+22 V^-1/m`^{4}	First coefficient of flicker noise.
109	`nfb=3.0e+07 V^-1/m`^{2}	Second coefficient of flicker noise.
110	`nfc=0.0 V^-1`	Third coefficient of flicker noise.
111	`ef=1.0`	Flicker noise frequency exponent.
112	`munqs=1.0`	Relative mobility for NQS modelling.
113	`rg=0.0 Ω`	Gate resistance.
114	`rse=0.0 Ω`	External source resistance.
115	`rde=0.0 Ω`	External drain resistance.
116	`rbulk=0.0 Ω`	Bulk resistance between node BP and BI.
117	`rwell=0.0 Ω`	Well resistance between node BI and B.
118	`rjuns=0.0 Ω`	Source-side bulk resistance between node BI and BS.
119	`rjund=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
120	`rth=0.0 K/W`	Thermal resistance.
121	`cth=0.0 J/K`	Thermal capacitance.
122	`strth=0.0`	Temperature sensitivity of RTH.
123	`povfb=-1 V`	Coefficient for the geometry-independent part of VFB.
124	`plvfb=0.0 V`	Coefficient for the length dependence of VFB.
125	`pwvfb=0.0 V`	Coefficient for the width dependence of VFB.
126	`plwvfb=0.0 V`	Coefficient for the length times width dependence of VFB.
127	`postvfb=0.0005 V/K`	Coefficient for the geometry-independent part of STVFB.
128	`plstvfb=0.0 V/K`	Coefficient for the length dependence of STVFB.
129	`pwstvfb=0.0 V/K`	Coefficient for the width dependence of STVFB.
130	`plwstvfb=0.0 V/K`	Coefficient for the length times width dependence of STVFB.
131	`potox=2E-09 m`	Coefficient for the geometry-independent part of TOX.

© 2023 Cadence Design Systems, Inc.

132	`poepsrox=3.9`	Coefficient for the geometry-independent part of EPSOX.
133	`poneff=5E+23 m`$^{-3}$	Coefficient for the geometry-independent part of NEFF.
134	`plneff=0.0 m`$^{-3}$	Coefficient for the length dependence of NEFF.
135	`pwneff=0.0 m`$^{-3}$	Coefficient for the width dependence of NEFF.
136	`plwneff=0.0 m`$^{-3}$	Coefficient for the length times width dependence of NEFF.
137	`pofacneffac=1.0`	Coefficient for the geometry-independent part of FACNEFFAC.
138	`plfacneffac=0.0`	Coefficient for the length dependence of FACNEFFAC.
139	`pwfacneffac=0.0`	Coefficient for the width dependence of FACNEFFAC.
140	`plwfacneffac=0.0`	Coefficient for the length times width dependence of FACNEFFAC.
141	`pogfacnud=1.0`	Coefficient for the geometry-independent part of GFACNUD.
142	`plgfacnud=0.0`	Coefficient for the length dependence of GFACNUD.
143	`pwgfacnud=0.0`	Coefficient for the width dependence of GFACNUD.
144	`plwgfacnud=0.0`	Coefficient for the length times width dependence of GFACNUD.
145	`povsbnud=0.0 V`	Coefficient for the geometry-independent part of VSBNUD.
146	`podvsbnud=1.0 V`	Coefficient for the geometry-independent part of DVSBNUD.
147	`povnsub=0 V`	Coefficient for the geometry-independent part of VNSUB.
148	`ponslp=0.05 V`	Coefficient for the geometry-independent part of NSLP.
149	`podnsub=0 V^-1`	Coefficient for the geometry-independent part of DNSUB.
150	`podphib=0 V`	Coefficient for the geometry-independent part of DPHIB.
151	`pldphib=0.0 V`	Coefficient for the length dependence of DPHIB.
152	`pwdphib=0.0 V`	Coefficient for the width dependence of DPHIB.

© 2023 Cadence Design Systems, Inc.

153	plwdphib=0.0 V	Coefficient for the length times width dependence of DPHIB.
154	podelvtac=0 V	Coefficient for the geometry-independent part of DELVTAC.
155	pldelvtac=0.0 V	Coefficient for the length dependence of DELVTAC.
156	pwdelvtac=0.0 V	Coefficient for the width dependence of DELVTAC.
157	plwdelvtac=0.0 V	Coefficient for the length times width dependence of DELVTAC.
158	ponp=1E+26 m^{-3}	Coefficient for the geometry-independent part of NP.
159	plnp=0.0 m^{-3}	Coefficient for the length dependence of NP.
160	pwnp=0.0 m^{-3}	Coefficient for the width dependence of NP.
161	plwnp=0.0 m^{-3}	Coefficient for the length times width dependence of NP.
162	poct=0	Coefficient for the geometry-independent part of CT.
163	plct=0.0	Coefficient for the length dependence of CT.
164	pwct=0.0	Coefficient for the width dependence of CT.
165	plwct=0.0	Coefficient for the length times width dependence of CT.
166	potoxov=2E-09 m	Coefficient for the geometry-independent part of TOXOV.
167	potoxovd=2E-09 m	Coefficient for the geometry-independent part of TOXOV for drain side.
168	ponov=5E+25 m^{-3}	Coefficient for the geometry-independent part of NOV.
169	plnov=0.0 m^{-3}	Coefficient for the length dependence of NOV.
170	pwnov=0.0 m^{-3}	Coefficient for the width dependence of NOV.
171	plwnov=0.0 m^{-3}	Coefficient for the length times width dependence of NOV.
172	ponovd=5E+25 m^{-3}	Coefficient for the geometry-independent part of NOV for drain side.
173	plnovd=0.0 m^{-3}	Coefficient for the length dependence of NOV for drain side.

© 2023 Cadence Design Systems, Inc.

174	pwnovd=0.0 m^{-3}	Coefficient for the width dependence of NOV for drain side.
175	plwnovd=0.0 m^{-3}	Coefficient for the length times width dependence of NOV for drain side.
176	pocf=0	Coefficient for the geometry-independent part of CF.
177	plcf=0.0	Coefficient for the length dependence of CF.
178	pwcf=0.0	Coefficient for the width dependence of CF.
179	plwcf=0.0	Coefficient for the length times width dependence of CF.
180	plcfd=0.0 V^-1	Coefficient for the geometry-independent part of CFD.
181	pocfd=0 V^-1	Coefficient for the geometry-independent part of CFD.
182	pocfb=0 V^-1	Coefficient for the geometry-independent part of CFB.
183	pobetn=0.07 m^2/V/s	Coefficient for the geometry-independent part of BETN.
184	plbetn=0.0 m^2/V/s	Coefficient for the length dependence of BETN.
185	pwbetn=0.0 m^2/V/s	Coefficient for the width dependence of BETN.
186	plwbetn=0.0 m^2/V/s	Coefficient for the length times width dependence of BETN.
187	postbet=1	Coefficient for the geometry-independent part of STBET.
188	plstbet=0.0	Coefficient for the length dependence of STBET.
189	pwstbet=0.0	Coefficient for the width dependence of STBET.
190	plwstbet=0.0	Coefficient for the length times width dependence of STBET.
191	pomue=0.5 m/V	Coefficient for the geometry-independent part of MUE.
192	plmue=0.0 m/V	Coefficient for the length dependence of MUE.
193	pwmue=0.0 m/V	Coefficient for the width dependence of MUE.

© 2023 Cadence Design Systems, Inc.

194	`plwmue=0.0 m/V`	Coefficient for the length times width dependence of MUE.
195	`postmue=0`	Coefficient for the geometry-independent part of STMUE.
196	`pothemu=1.5`	Coefficient for the geometry-independent part of THEMU.
197	`postthemu=1.5`	Coefficient for the geometry-independent part of STTHEMU.
198	`pocs=0`	Coefficient for the geometry-independent part of CS.
199	`plcs=0.0`	Coefficient for the length dependence of CS.
200	`pwcs=0.0`	Coefficient for the width dependence of CS.
201	`plwcs=0.0`	Coefficient for the length times width dependence of CS.
202	`postcs=0`	Coefficient for the geometry-independent part of STCS.
203	`poxcor=0 V^-1`	Coefficient for the geometry-independent part of XCOR.
204	`plxcor=0.0 V^-1`	Coefficient for the length dependence of XCOR.
205	`pwxcor=0.0 V^-1`	Coefficient for the width dependence of XCOR.
206	`plwxcor=0.0 V^-1`	Coefficient for the length times width dependence of XCOR.
207	`postxcor=0`	Coefficient for the geometry-independent part of STXCOR.
208	`pofeta=1`	Coefficient for the geometry-independent part of FETA.
209	`pors=30 Ω`	Coefficient for the geometry-independent part of RS.
210	`plrs=0.0 Ω`	Coefficient for the length dependence of RS.
211	`pwrs=0.0 Ω`	Coefficient for the width dependence of RS.
212	`plwrs=0.0 Ω`	Coefficient for the length times width dependence of RS.
213	`postrs=1`	Coefficient for the geometry-independent part of STRS.
214	`porsb=0 V^-1`	Coefficient for the geometry-independent part of RSB.

© 2023 Cadence Design Systems, Inc.

215	`porsg=0 V^-1`	Coefficient for the geometry-independent part of RSG.
216	`pothesat=1 V^-1`	Coefficient for the geometry-independent part of THESAT.
217	`plthesat=0.0 V^-1`	Coefficient for the length dependence of THESAT.
218	`pwthesat=0.0 V^-1`	Coefficient for the width dependence of THESAT.
219	`plwthesat=0.0 V^-1`	Coefficient for the length times width dependence of THESAT.
220	`postthesat=1`	Coefficient for the geometry-independent part of STTHESAT.
221	`plstthesat=0.0`	Coefficient for the length dependence of STTHESAT.
222	`pwstthesat=0.0`	Coefficient for the width dependence of STTHESAT.
223	`plwstthesat=0.0`	Coefficient for the length times width dependence of STTHESAT.
224	`pothesatb=0 V^-1`	Coefficient for the geometry-independent part of THESATB.
225	`plthesatb=0.0 V^-1`	Coefficient for the length dependence of THESATB.
226	`pwthesatb=0.0 V^-1`	Coefficient for the width dependence of THESATB.
227	`plwthesatb=0.0 V^-1`	Coefficient for the length times width dependence of THESATB.
228	`pothesatg=0 V^-1`	Coefficient for the geometry-independent part of THESATG.
229	`plthesatg=0.0 V^-1`	Coefficient for the length dependence of THESATG.
230	`pwthesatg=0.0 V^-1`	Coefficient for the width dependence of THESATG.
231	`plwthesatg=0.0 V^-1`	

© 2023 Cadence Design Systems, Inc.

		Coefficient for the length times width dependence of THESATG.
232	`poax=3`	Coefficient for the geometry-independent part of AX.
233	`plax=0.0`	Coefficient for the length dependence of AX.
234	`pwax=0.0`	Coefficient for the width dependence of AX.
235	`plwax=0.0`	Coefficient for the length times width dependence of AX.
236	`poalp=0.01`	Coefficient for the geometry-independent part of ALP.
237	`plalp=0.0`	Coefficient for the length dependence of ALP.
238	`pwalp=0.0`	Coefficient for the width dependence of ALP.
239	`plwalp=0.0`	Coefficient for the length times width dependence of ALP.
240	`poalp1=0 V`	Coefficient for the geometry-independent part of ALP1.
241	`plalp1=0.0 V`	Coefficient for the length dependence of ALP1.
242	`pwalp1=0.0 V`	Coefficient for the width dependence of ALP1.
243	`plwalp1=0.0 V`	Coefficient for the length times width dependence of ALP1.
244	`poalp2=0 V^-1`	Coefficient for the geometry-independent part of ALP2.
245	`plalp2=0.0 V^-1`	Coefficient for the length dependence of ALP2.
246	`pwalp2=0.0 V^-1`	Coefficient for the width dependence of ALP2.
247	`plwalp2=0.0 V^-1`	Coefficient for the length times width dependence of ALP2.
248	`povp=0.05 V`	Coefficient for the geometry-independent part of VP.
249	`poa1=1`	Coefficient for the geometry-independent part of A1.
250	`pla1=0.0`	Coefficient for the length dependence of A1.
251	`pwa1=0.0`	Coefficient for the width dependence of A1.
252	`plwa1=0.0`	Coefficient for the length times width dependence of A1.
253	`poa2=10 V`	Coefficient for the geometry-independent part of A2.
254	`posta2=0 V`	Coefficient for the geometry-independent part of STA2.
255	`poa3=1`	Coefficient for the geometry-independent part of A3.

© 2023 Cadence Design Systems, Inc.

256	`pla3=0.0`	Coefficient for the length dependence of A3.
257	`pwa3=0.0`	Coefficient for the width dependence of A3.
258	`plwa3=0.0`	Coefficient for the length times width dependence of A3.
259	`poa4=0 V^-0.5`	Coefficient for the geometry-independent part of A4.
260	`pla4=0.0 V^-0.5`	Coefficient for the length dependence of A4.
261	`pwa4=0.0 V^-0.5`	Coefficient for the width dependence of A4.
262	`plwa4=0.0 V^-0.5`	Coefficient for the length times width dependence of A4.
263	`pogco=0`	Coefficient for the geometry-independent part of GCO.
264	`poiginv=0 A`	Coefficient for the geometry-independent part of IGINV.
265	`pliginv=0.0 A`	Coefficient for the length dependence of IGINV.
266	`pwiginv=0.0 A`	Coefficient for the width dependence of IGINV.
267	`plwiginv=0.0 A`	Coefficient for the length times width dependence of IGINV.
268	`poigov=0 A`	Coefficient for the geometry-independent part of IGOV.
269	`pligov=0.0 A`	Coefficient for the length dependence of IGOV.
270	`pwigov=0.0 A`	Coefficient for the width dependence of IGOV.
271	`plwigov=0.0 A`	Coefficient for the length times width dependence of IGOV.
272	`poigovd=0 A`	Coefficient for the geometry-independent part of IGOV for drain side.
273	`pligovd=0.0 A`	Coefficient for the length dependence of IGOV for drain side.
274	`pwigovd=0.0 A`	Coefficient for the width dependence of IGOV for drain side.
275	`plwigovd=0.0 A`	Coefficient for the length times width dependence of IGOV for drain side.
276	`postig=2`	Coefficient for the geometry-independent part of STIG.
277	`pogc2=0.375`	Coefficient for the geometry-independent part of GC2.
278	`pogc3=0.063`	Coefficient for the geometry-independent part of GC3.

© 2023 Cadence Design Systems, Inc.

279	`pochib=3.1 V`	Coefficient for the geometry-independent part of CHIB.
280	`poagidl=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL.
281	`plagidl=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL.
282	`pwagidl=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL.
283	`plwagidl=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL.
284	`poagidld=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL for drain side.
285	`plagidld=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL for drain side.
286	`pwagidld=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL for drain side.
287	`plwagidld=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL for drain side.
288	`pobgidl=41 V`	Coefficient for the geometry-independent part of BGIDL.
289	`pobgidld=41 V`	Coefficient for the geometry-independent part of BGIDL for drain side.
290	`postbgidl=0 V/K`	Coefficient for the geometry-independent part of STBGIDL.
291	`postbgidld=0 V/K`	Coefficient for the geometry-independent part of STBGIDL for drain side.
292	`pocgidl=0`	Coefficient for the geometry-independent part of CGIDL.
293	`pocgidld=0`	Coefficient for the geometry-independent part of CGIDL for drain side.
294	`pocox=1E-14 F`	Coefficient for the geometry-independent part of COX.
295	`plcox=0.0 F`	Coefficient for the length dependence of COX.

© 2023 Cadence Design Systems, Inc.

296	`pwcox=0.0 F`	Coefficient for the width dependence of COX.
297	`plwcox=0.0 F`	Coefficient for the length times width dependence of COX.
298	`pocgov=1E-15 F`	Coefficient for the geometry-independent part of CGOV.
299	`plcgov=0.0 F`	Coefficient for the length dependence of CGOV.
300	`pwcgov=0.0 F`	Coefficient for the width dependence of CGOV.
301	`plwcgov=0.0 F`	Coefficient for the length times width dependence of CGOV.
302	`pocgovd=1E-15 F`	Coefficient for the geometry-independent part of CGOV for drain side.
303	`plcgovd=0.0 F`	Coefficient for the length dependence of CGOV for drain side.
304	`pwcgovd=0.0 F`	Coefficient for the width dependence of CGOV for drain side.
305	`plwcgovd=0.0 F`	Coefficient for the length times width dependence of CGOV for drain side.
306	`pocgbov=0 F`	Coefficient for the geometry-independent part of CGBOV.
307	`plcgbov=0.0 F`	Coefficient for the length dependence of CGBOV.
308	`pwcgbov=0.0 F`	Coefficient for the width dependence of CGBOV.
309	`plwcgbov=0.0 F`	Coefficient for the length times width dependence of CGBOV.
310	`pocfr=0 F`	Coefficient for the geometry-independent part of CFR.
311	`plcfr=0.0 F`	Coefficient for the length dependence of CFR.
312	`pwcfr=0.0 F`	Coefficient for the width dependence of CFR.
313	`plwcfr=0.0 F`	Coefficient for the length times width dependence of CFR.
314	`pocfrd=0 F`	Coefficient for the geometry-independent part of CFR for drain side.
315	`plcfrd=0.0 F`	Coefficient for the length dependence of CFR for drain side.

© 2023 Cadence Design Systems, Inc.

316	`pwcfrd=0.0 F`	Coefficient for the width dependence of CFR for drain side.
317	`plwcfrd=0.0 F`	Coefficient for the length times width dependence of CFR for drain side.
318	`pofcgovacc=0.0`	Coefficient for the geometry-independent part of FCGOVACC.
319	`pofcgovaccd=0.0`	Coefficient for the geometry-independent part of FCGOVACC for drain side.
320	`pocgovaccg=1.0`	Coefficient for the geometry-independent part of CGOVACCG.
321	`pocinr=0.0 F`	Coefficient for the geometry-independent part of CINR.
322	`plcinr=0.0 F`	Coefficient for the length dependence of CINR.
323	`pwcinr=0.0 F`	Coefficient for the width dependence of CINR.
324	`plwcinr=0.0 F`	Coefficient for the length times width dependence of CINR.
325	`pocinrd=0.0 F`	Coefficient for the geometry-independent part of CINR for drain side.
326	`plcinrd=0.0 F`	Coefficient for the length dependence of CINR for drain side.
327	`pwcinrd=0.0 F`	Coefficient for the width dependence of CINR for drain side.
328	`plwcinrd=0.0 F`	Coefficient for the length times width dependence of CINR for drain side.
329	`podvfbinr=0.0 V`	Coefficient for the geometry-independent part of DVFBINR.
330	`pofcinrdep=0.3`	Coefficient for the geometry-independent part of FCINRDEP.
331	`pofcinracc=0.5`	Coefficient for the geometry-independent part of FCINRACC.
332	`poaxinr=0.5`	Coefficient for the geometry-independent part of AXINR.
333	`pofnt=1`	Coefficient for the geometry-independent part of FNT.
334	`pofntexc=0.0`	Coefficient for the geometry-independent part of FNTEXC.

© 2023 Cadence Design Systems, Inc.

335	`plfntexc=0.0`	Coefficient for the length dependence of FNTEXC.
336	`pwfntexc=0.0`	Coefficient for the width dependence of FNTEXC.
337	`plwfntexc=0.0`	Coefficient for the length times width dependence of FNTEXC.
338	`ponfa=8E+22 V^-1/m`^{4}	Coefficient for the geometry-independent part of NFA.
339	`plnfa=0.0 V^-1/m`^{4}	Coefficient for the length dependence of NFA.
340	`pwnfa=0.0 V^-1/m`^{4}	Coefficient for the width dependence of NFA.
341	`plwnfa=0.0 V^-1/m`^{4}	Coefficient for the length times width dependence of NFA.
342	`ponfb=3E+07 V^-1/m`^{2}	Coefficient for the geometry-independent part of NFB.
343	`plnfb=0.0 V^-1/m`^{2}	Coefficient for the length dependence of NFB.
344	`pwnfb=0.0 V^-1/m`^{2}	Coefficient for the width dependence of NFB.
345	`plwnfb=0.0 V^-1/m`^{2}	Coefficient for the length times width dependence of NFB.
346	`ponfc=0 V^-1`	Coefficient for the geometry-independent part of NFC.
347	`plnfc=0.0 V^-1`	Coefficient for the length dependence of NFC.
348	`pwnfc=0.0 V^-1`	Coefficient for the width dependence of NFC.
349	`plwnfc=0.0 V^-1`	Coefficient for the length times width dependence of NFC.
350	`poef=1.0`	Coefficient for the flicker noise frequency exponent.
351	`pokvthowe=0`	Coefficient for the geometry-independent part of KVTHOWE.

© 2023 Cadence Design Systems, Inc.

352	`plkvthowe=0`	Coefficient for the length dependence part of KVTHOWE.
353	`pwkvthowe=0`	Coefficient for the width dependence part of KVTHOWE.
354	`plwkvthowe=0`	Coefficient for the length times width dependence part of KVTHOWE.
355	`pokuowe=0`	Coefficient for the geometry-independent part of KUOWE.
356	`plkuowe=0`	Coefficient for the length dependence part of KUOWE.
357	`pwkuowe=0`	Coefficient for the width dependence part of KUOWE.
358	`plwkuowe=0`	Coefficient for the length times width dependence part of KUOWE.
359	`lmin=0 m`	Dummy parameter to label binning set.
360	`lmax=1.0 m`	Dummy parameter to label binning set.
361	`wmin=0 m`	Dummy parameter to label binning set.
362	`wmax=1.0 m`	Dummy parameter to label binning set.
363	`popsce=0.0`	Coefficient for the geometry-independent part of PSCE.
364	`plpsce=0.0`	Coefficient for the length dependence of PSCE.
365	`pwpsce=0.0`	Coefficient for the width dependence of PSCE.
366	`plwpsce=0.0`	Coefficient for the length times width dependence of PSCE.
367	`popsceb=0.0 V^-1`	Coefficient for the geometry-independent part of PSCEB.
368	`popsced=0.0 V^-1`	Coefficient for the geometry-independent part of PSCED.
369	`povfbedge=(-1.0) V`	Coefficient for the geometry-independent part of VFBEDGE.
370	`postvfbedge=0.0 V/K`	Coefficient for the geometry-independent part of STVFBEDGE.
371	`plstvfbedge=0.0 V/K`	Coefficient for the length dependence of STVFBEDGE
372	`pwstvfbedge=0.0 V/K`	Coefficient for the width dependence of STVFBEDGE.

© 2023 Cadence Design Systems, Inc.

373	`plwstvfbedge=0.0 V/K`	Coefficient for the length times width dependence of STVFBEDGE.
374	`podphibedge=0.0 V`	Coefficient for the geometry-independent part of DPHIBEDGE.
375	`pldphibedge=0.0 V`	Coefficient for the length dependence of DPHIBEDGE.
376	`pwdphibedge=0.0 V`	Coefficient for the width dependence of DPHIBEDGE.
377	`plwdphibedge=0.0 V`	Coefficient for the length times width dependence of DPHIBEDGE.
378	`poneffedge=5.0e23 m`$^{-3}$	Coefficient for the geometry-independent part of NEFFEDGE.
379	`plneffedge=0.0 m`$^{-3}$	Coefficient for the length dependence of NEFFEDGE.
380	`pwneffedge=0.0 m`$^{-3}$	Coefficient for the width dependence of NEFFEDGE.
381	`plwneffedge=0.0 m`$^{-3}$	Coefficient for the length times width dependence of NEFFEDGE.
382	`poctedge=0.0`	Coefficient for the geometry-independent part of CTEDGE.
383	`plctedge=0.0`	Coefficient for the length dependence of CTEDGE.
384	`pwctedge=0.0`	Coefficient for the width dependence of CTEDGE.
385	`plwctedge=0.0`	Coefficient for the length times width dependence of CTEDGE.
386	`pobetnedge=5.0e-4 m`^{2}`/V/s`	Coefficient for the geometry-independent part of BETNEDGE.
387	`plbetnedge=0.0 m`^{2}`/V/s`	Coefficient for the length dependence of BETNEDGE.
388	`pwbetnedge=0.0 m`^{2}`/V/s`	Coefficient for the width dependence of BETNEDGE.
389	`plwbetnedge=0.0 m`^{2}`/V/s`	Coefficient for the length times width dependence of BETNEDGE.
390	`postbetedge=1.0`	Coefficient for the geometry-independent part of STBETEDGE.

© 2023 Cadence Design Systems, Inc.

391	`plstbetedge=0.0`	Coefficient for the length dependence of STBETEDGE.
392	`pwstbetedge=0.0`	Coefficient for the width dependence of STBETEDGE.
393	`plwstbetedge=0.0`	Coefficient for the length times width dependence of STBETEDGE.
394	`popsceedge=0.0`	Coefficient for the geometry-independent part of PSCEEDGE.
395	`plpsceedge=0.0`	Coefficient for the length dependence of PSCEEDGE.
396	`pwpsceedge=0.0`	Coefficient for the width dependence of PSCEEDGE.
397	`plwpsceedge=0.0`	Coefficient for the length times width dependence of PSCEEDGE.
398	`popscebedge=0.0 V^-1`	Coefficient for the geometry-independent part of PSCEBEDGE.
399	`popscededge=0.0 V^-1`	Coefficient for the geometry-independent part of PSCEDEDGE.
400	`pocfedge=0.0`	Coefficient for the geometry-independent part of CFEDGE.
401	`plcfedge=0.0`	Coefficient for the length dependence of CFEDGE.
402	`pwcfedge=0.0`	Coefficient for the width dependence of CFEDGE.
403	`plwcfedge=0.0`	Coefficient for the length times width dependence of CFEDGE.
404	`pocfdedge=0.0 V^-1`	Coefficient for the geometry-independent part of CFDEDGE.
405	`pocfbedge=0.0 V^-1`	Coefficient for the geometry-independent part of CFBEDGE.
406	`pofntedge=1.0`	Coefficient for the geometry-independent part of FNTEDGE.
407	`ponfaedge=8.0e22 V^-1/m`^{4}	Coefficient for the geometry-independent part of NFAEDGE.

© 2023 Cadence Design Systems, Inc.

408	`plnfaedge=0.0 V^-1/m`^{4}	Coefficient for the length dependence of NFAEDGE.
409	`pwnfaedge=0.0 V^-1/m`^{4}	Coefficient for the width dependence of NFAEDGE.
410	`plwnfaedge=0.0 V^-1/m`^{4}	Coefficient for the length times width dependence of NFAEDGE.
411	`ponfbedge=3.0e7 V^-1/m`^{2}	Coefficient for the geometry-independent part of NFBEDGE.
412	`plnfbedge=0.0 V^-1/m`^{2}	Coefficient for the length dependence of NFBEDGE.
413	`pwnfbedge=0.0 V^-1/m`^{2}	Coefficient for the width dependence of NFBEDGE.
414	`plwnfbedge=0.0 V^-1/m`^{2}	Coefficient for the length times width dependence of NFBEDGE.
415	`ponfcedge=0.0 V^-1`	Coefficient for the geometry-independent part of NFCEDGE.
416	`plnfcedge=0.0 V^-1`	Coefficient for the length dependence of NFCEDGE.
417	`pwnfcedge=0.0 V^-1`	Coefficient for the width dependence of NFCEDGE.
418	`plwnfcedge=0.0 V^-1`	Coefficient for the length times width dependence of NFCEDGE.
419	`poefedge=1.0`	Coefficient for the geometry-independent part of EFEDGE.
420	`lvaro=0.0 m`	Geometry-independent difference between actual and programmed gate length.
421	`lvarl=0.0`	Length dependence of LVAR.
422	`lvarw=0.0`	Width dependence of LVAR.
423	`lap=0.0 m`	Effective channel length reduction per side.

© 2023 Cadence Design Systems, Inc.

424	`wvaro=0.0 m`	Geometry-independent difference between actual and programmed field-oxide opening.
425	`wvarl=0.0`	Length dependence of WVAR.
426	`wvarw=0.0`	Width dependence of WVAR.
427	`wot=0.0 m`	Effective channel width reduction per side.
428	`dlq=0.0 m`	Effective channel length reduction for CV.
429	`dwq=0.0 m`	Effective channel width reduction for CV.
430	`vfbo=-1.0 V`	Geometry-independent flat-band voltage at TR.
431	`vfbl=0.0 V`	Length dependence of flat-band voltage.
432	`vfbw=0.0 V`	Width dependence of flat-band voltage.
433	`vfblw=0.0 V`	Area dependence of flat-band voltage.
434	`stvfbo=5e-4 V/K`	Geometry-independent temperature dependence of VFB.
435	`stvfbl=0.0 V/K`	Length dependence of temperature dependence of VFB.
436	`stvfbw=0.0 V/K`	Width dependence of temperature dependence of VFB.
437	`stvfblw=0.0 V/K`	Area dependence of temperature dependence of VFB.
438	`toxo=2e-9 m`	Gate oxide thickness.
439	`epsroxo=3.9`	Relative permittivity of gate dielectric.
440	`nsubo=3e23` m^{-3}	Geometry-independent substrate doping.
441	`nsubw=0.0`	Width dependence of background doping NSUBO due to segregation.
442	`wseg=1e-8 m`	Character length of segregation of background doping NSUBO.
443	`npck=1e24` m^{-3}	Pocket doping level.
444	`npckw=0.0`	Width dependence of pocket doping NPCK due to segregation.
445	`wsegp=1e-8 m`	Character length of segregation of pocket doping NPCK.
446	`lpck=1e-8 m`	Character length of lateral doping profile.

© 2023 Cadence Design Systems, Inc.

447	`lpckw=0.0`	Width dependence of character length of lateral doping profile.
448	`fol1=0.0`	First length dependence coefficient for short channel body effect.
449	`fol2=0.0`	Second length dependence coefficient for short channel body effect.
450	`facneffaco=1.0`	Geometry-independent pre-factor for effective substrate doping in separate charge calculation.
451	`facneffacl=0.0`	Length dependence of FACNEFFAC.
452	`facneffacw=0.0`	Width dependence of FACNEFFAC.
453	`facneffaclw=0.0`	Area dependence of FACNEFFAC.
454	`gfacnudo=1.0`	Geometry-independent bodyfactor change due to NUD-effect.
455	`gfacnudl=0.0`	Length dependence of GFACNUD.
456	`gfacnudlexp=1.0`	Exponent for length dependence of GFACNUD.
457	`gfacnudw=0.0`	Width dependence of GFACNUD.
458	`gfacnudlw=0.0`	Area dependence of GFACNUD.
459	`vsbnudo=0.0 V`	Lower Vsb value for NUD-effect.
460	`dvsbnudo=1.0 V`	Vsb range for NUD-effect.
461	`vnsubo=0.0 V`	Effective doping bias-dependence parameter.
462	`nslpo=0.05 V`	Effective doping bias-dependence parameter.
463	`dnsubo=0.0 V^-1`	Effective doping bias-dependence parameter.
464	`dphibo=0.0 V`	Geometry-independent offset of PHIB.
465	`dphibl=0.0 V`	Length dependence offset of PHIB.
466	`dphiblexp=1.0`	Exponent for length dependence of offset of PHIB.
467	`dphibw=0.0 V`	Width dependence of offset of PHIB.
468	`dphiblw=0.0 V`	Area dependence of offset of PHIB.
469	`delvtaco=0.0 V`	Geometry-independent offset parameter for PHIB in separate charge calculation.
470	`delvtacl=0.0 V`	Length dependence of DELVTAC.
471	`delvtaclexp=1.0`	Exponent for length dependence of offset of DELVTAC.

© 2023 Cadence Design Systems, Inc.

472	`delvtacw=0.0 V`	Width dependence of DELVTAC.
473	`delvtaclw=0.0 V`	Area dependence of DELVTAC.
474	`npo=1e26 m^-3`	Geometry-independent gate poly-silicon doping.
475	`npl=0.0`	Length dependence of gate poly-silicon doping.
476	`cto=0.0`	Geometry-independent interface states factor.
477	`ctl=0.0`	Length dependence of interface states factor.
478	`ctlexp=1.0`	Exponent for length dependence of interface states factor.
479	`ctw=0.0`	Width dependence of interface states factor.
480	`ctlw=0.0`	Area dependence of interface states factor.
481	`toxovo=2e-9 m`	Overlap oxide thickness.
482	`toxovdo=2e-9 m`	Overlap oxide thickness for drain side.
483	`lov=0 m`	Overlap length for gate/drain and gate/source overlap capacitance.
484	`lovd=0 m`	Overlap length for gate/drain overlap capacitance.
485	`novo=5.0e25 m^-3`	Effective doping of overlap region.
486	`novdo=5.0e25 m^-3`	Effective doping of overlap region for drain side.
487	`cfl=0.0`	Length dependence of DIBL-parameter.
488	`cflexp=2.0`	Exponent for length dependence of CF.
489	`cfw=0.0`	Width dependence of CF.
490	`cfbo=0.0 V^-1`	Back-bias dependence of CF.
491	`uo=5e-2 m^2/V/s`	Zero-field mobility at TR.
492	`fbet1=0.0`	Relative mobility decrease due to first lateral profile.
493	`fbet1w=0.0`	Width dependence of relative mobility decrease due to first lateral profile.
494	`lp1=1e-8 m`	Mobility-related characteristic length of first lateral profile.
495	`lp1w=0.0`	Width dependence of mobility-related characteristic length of first lateral profile.
496	`fbet2=0.0`	Relative mobility decrease due to second lateral profile.

© 2023 Cadence Design Systems, Inc.

497	`lp2=1e-8 m`	Mobility-related characteristic length of second lateral profile.
498	`betw1=0.0`	First higher-order width scaling coefficient of BETN.
499	`betw2=0.0`	Second higher-order width scaling coefficient of BETN.
500	`wbet=1e-9 m`	Characteristic width for width scaling of BETN.
501	`stbeto=1.0`	Geometry-independent temperature dependence of BETN.
502	`stbetl=0.0`	Length dependence of temperature dependence of BETN.
503	`stbetw=0.0`	Width dependence of temperature dependence of BETN.
504	`stbetlw=0.0`	Area dependence of temperature dependence of BETN.
505	`mueo=0.5 m/V`	Geometry-independent mobility reduction coefficient at TR.
506	`muew=0.0`	Width dependence of mobility reduction coefficient at TR.
507	`stmueo=0.0`	Temperature dependence of MUE.
508	`themuo=1.5`	Mobility reduction exponent at TR.
509	`stthemuo=1.5`	Temperature dependence of THEMU.
510	`cso=0.0`	Geometry-independent coulomb scattering parameter at TR.
511	`csl=0.0`	Length dependence of CS.
512	`cslexp=1.0`	Exponent for length dependence of CS.
513	`csw=0.0`	Width dependence of CS.
514	`cslw=0.0`	Area dependence of CS.
515	`stcso=0.0`	Temperature dependence of CS.
516	`xcoro=0.0 V^-1`	Geometry-independent non-universality parameter.
517	`xcorl=0.0`	Length dependence of non-universality parameter.
518	`xcorw=0.0`	Width dependence of non-universality parameter.
519	`xcorlw=0.0`	Area dependence of non-universality parameter.

© 2023 Cadence Design Systems, Inc.

520	`stxcoro=0.0`	Temperature dependence of XCOR.
521	`fetao=1.0`	Effective field parameter.
522	`rsw1=50.0 Ω`	Source/drain series resistance for 1 um wide channel at TR.
523	`rsw2=0.0`	Higher-order width scaling of RS.
524	`strso=1.0`	Temperature dependence of RS.
525	`rsbo=0.0 V^-1`	Back-bias dependence of series resistance.
526	`rsgo=0.0 V^-1`	Gate-bias dependence of series resistance.
527	`thesato=0.0 V^-1`	Geometry-independent velocity saturation parameter at TR.
528	`thesatl=0.05 V^-1`	Length dependence of THESAT.
529	`thesatlexp=1.0`	Exponent for length dependence of THESAT.
530	`thesatw=0.0`	Width dependence of velocity saturation parameter.
531	`thesatlw=0.0`	Area dependence of velocity saturation parameter.
532	`stthesato=1.0`	Geometry-independent temperature dependence of THESAT.
533	`stthesatl=0.0`	Length dependence of temperature dependence of THESAT.
534	`stthesatw=0.0`	Width dependence of temperature dependence of THESAT.
535	`stthesatlw=0.0`	Area dependence of temperature dependence of THESAT.
536	`thesatbo=0.0 V^-1`	Back-bias dependence of velocity saturation.
537	`thesatgo=0.0 V^-1`	Gate-bias dependence of velocity saturation.
538	`axo=18`	Geometry-independent linear/saturation transition factor.
539	`axl=0.4`	Length dependence of AX.
540	`alpl=5e-4`	Length dependence of ALP.
541	`alplexp=1.0`	Exponent for length dependence of ALP.
542	`alpw=0.0`	Width dependence of ALP.

© 2023 Cadence Design Systems, Inc.

543	`alp1l1=0.0 V`	Length dependence of CLM enhancement factor above threshold.
544	`alp1lexp=0.5`	Exponent for length dependence of ALP1.
545	`alp1l2=0.0`	Second_order length dependence of ALP1.
546	`alp1w=0.0`	Width dependence of ALP1.
547	`alp2l1=0.0 V^-1`	Length dependence of CLM enhancement factor below threshold.
548	`alp2lexp=0.5`	Exponent for length dependence of ALP2.
549	`alp2l2=0.0`	Second_order length dependence of ALP2.
550	`alp2w=0.0`	Width dependence of ALP2.
551	`vpo=0.05 V`	CLM logarithmic dependence parameter.
552	`a1o=1.0`	Geometry-independent impact-ionization pre-factor.
553	`a1l=0.0`	Length dependence of A1.
554	`a1w=0.0`	Width dependence of A1.
555	`a2o=10 V`	Impact-ionization exponent at TR.
556	`sta2o=0.0 V`	Temperature dependence of A2.
557	`a3o=1.0`	Geometry-independent saturation-voltage dependence of II.
558	`a3l=0.0`	Length dependence of A3.
559	`a3w=0.0`	Width dependence of A3.
560	`a4o=0.0 V^-0.5`	Geometry-independent back-bias dependence of II.
561	`a4l=0.0`	Length dependence of A4.
562	`a4w=0.0`	Width dependence of A4.
563	`gcoo=0.0`	Gate tunneling energy adjustment.
564	`iginvlw=0.0 A`	Gate channel current pre-factor for 1 um^2 channel area.
565	`igovw=0.0 A`	Gate overlap current pre-factor for 1 um wide channel.
566	`igovdw=0.0 A`	Gate overlap current pre-factor for 1 um wide channel for drain side.
567	`stigo=2.0`	Temperature dependence of IGINV and IGOV.

© 2023 Cadence Design Systems, Inc.

568	`gc2o=0.375`	Gate current slope factor.
569	`gc3o=0.063`	Gate current curvature factor.
570	`chibo=3.1 V`	Tunneling barrier height.
571	`agidlw=0.0 A/V`^{3}	Width dependence of GIDL pre-factor.
572	`agidldw=0.0 A/V`^{3}	Width dependence of GIDL pre-factor for drain side.
573	`bgidlo=41 V`	GIDL probability factor at TR.
574	`bgidldo=41 V`	GIDL probability factor at TR for drain side.
575	`stbgidlo=0.0 V/K`	Temperature dependence of BGIDL.
576	`stbgidldo=0.0 V/K`	Temperature dependence of BGIDL for drain side.
577	`cgidlo=0.0`	Back-bias dependence of GIDL.
578	`cgidldo=0.0`	Back-bias dependence of GIDL for drain side.
579	`cgbovl=0.0 F`	Oxide capacitance for gate-bulk overlap for 1 um long channel.
580	`cfrw=0.0 F`	Outer fringe capacitance for 1 um wide channel.
581	`cfrdw=0.0 F`	Outer fringe capacitance for 1 um wide channel for drain side.
582	`fcgovacco=0.0`	Factor for overlap capacitances in accumulation regime.
583	`fcgovaccdo=0.0`	Factor for overlap capacitances in accumulation regime for drain side.
584	`cgovaccgo=1.0`	Gate voltage dependence parameter of overlap capacitances in accumulation regime.
585	`cinrw=0.0 F`	Inner fringe capacitance for 1 um wide channel.
586	`cinrdw=0.0 F`	Inner fringe capacitance for 1 um wide channel for drain side.
587	`dvfbinro=0.0 V`	Flat-band voltage offset of inner fringe capacitances.
588	`fcinrdepo=0.3`	Bias dependence parameter of inner fringe capacitances in depletion regime.
589	`fcinracco=0.5`	Bias dependence parameter of inner fringe capacitances in accumulation regime.
590	`axinro=0.5`	Accumulation/depletion transition factor of inner fringe capacitances.

© 2023 Cadence Design Systems, Inc.

591	`fnto=1.0`	Thermal noise coefficient.
592	`fntexcl=0.0`	Length dependence coefficient of excess noise.
593	`nfalw=8e22 V^-1/m`^{4}	First coefficient of flicker noise for 1 um^2 channel area.
594	`nfblw=3e7 V^-1/m`^{2}	Second coefficient of flicker noise for 1 um^2 channel area.
595	`nfclw=0.0 V^-1`	Third coefficient of flicker noise for 1 um^2 channel area.
596	`efo=1.0`	Flicker noise frequency exponent.
597	`lintnoi=0.0 m`	Length offset for flicker noise.
598	`alpnoi=2.0`	Exponent for length offset for flicker noise.
599	`kvthoweo=0`	Geometrical independent threshold shift parameter.
600	`kvthowel=0`	Length dependent threshold shift parameter.
601	`kvthowew=0`	Width dependent threshold shift parameter.
602	`kvthowelw=0`	Area dependent threshold shift parameter.
603	`kuoweo=0`	Geometrical independent mobility degradation factor.
604	`kuowel=0`	Length dependent mobility degradation factor.
605	`kuowew=0`	Width dependent mobility degradation factor.
606	`kuowelw=0`	Area dependent mobility degradation factor.
607	`munqso=1.0`	Relative mobility for NQS modelling.
608	`rgo=0.0 Ω`	Gate resistance.
609	`rint=0.0 Ω m`^{2}	Contact resistance between silicide and ploy.
610	`rvpoly=0.0 Ω m`^{2}	Vertical poly resistance.
611	`rshg=0.0 Ω/Sqr`	Gate electrode diffusion sheet resistance.
612	`dlsil=0.0 m`	Silicide extension over the physical gate length.
613	`rsh=0.0 Ω/sq`	Sheet resistance of source diffusion.
614	`rshd=0.0 Ω/sq`	Sheet resistance of drain diffusion.

© 2023 Cadence Design Systems, Inc.

615	`rbulko=0.0 Ω`	Bulk resistance between node BP and BI.
616	`rwello=0.0 Ω`	Well resistance between node BI and B.
617	`rjunso=0.0 Ω`	Source-side bulk resistance between node BI and BS.
618	`rjundo=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
619	`rtho=0.0 K/W`	Geometry-independent part of thermal resistance.
620	`rthw1=0.0 K/W`	Width dependence of thermal resistance.
621	`rthw2=0.0`	Offset in width dependence of thermal resistance.
622	`rthlw=0.0`	Length-correction to width dependence of thermal resistance.
623	`ctho=0.0 J/K`	Geometry-independent part of thermal capacitance.
624	`cthw1=0.0 J/K`	Width dependence of thermal capacitance.
625	`cthw2=0.0`	Offset in width dependence of thermal capacitance.
626	`cthlw=0.0`	Length-correction to width dependence of thermal capacitance.
627	`strtho=0.0`	Temperature sensitivity of RTH.
628	`saref=1.0e-6 m`	Reference distance between OD-edge and poly from one side.
629	`sbref=1.0e-6 m`	Reference distance between OD-edge and poly from other side.
630	`wlod=0 m`	Width parameter.
631	`kuo=0 m`	Mobility degradation/enhancement coefficient.
632	`kvsat=0 m`	Saturation velocity degradation/enhancement coefficient.
633	`tkuo=0`	Temperature dependence of KUO.
634	`lkuo=0 m^LLODKUO`	Length dependence of KUO.
635	`wkuo=0 m^WLODKUO`	Width dependence of KUO.
636	`pkuo=0 m^(LLODKUO+WLODKUO`	Cross-term dependence of KUO.
637	`llodkuo=0`	Length parameter for UO stress effect.
638	`wlodkuo=0`	Width parameter for UO stress effect.

© 2023 Cadence Design Systems, Inc.

639	`kvtho=0 Vm`	Threshold shift parameter.
640	`lkvtho=0 m^LLODVTH`	Length dependence of KVTHO.
641	`wkvtho=0 m^WLODVTH`	Width dependence of KVTHO.
642	`pkvtho=0 m^(LLODVTH+WLODVTH`	Cross-term dependence of KVTHO.
643	`llodvth=0`	Length parameter for VTH-stress effect.
644	`wlodvth=0`	Width parameter for VTH-stress effect.
645	`stetao=0 m`	eta0 shift factor related to VTHO change.
646	`lodetao=1.0`	eta0 shift modification factor for stress effect.
647	`scref=1.0e-6 m`	Distance between OD-edge and well edge of a reference device.
648	`web=0`	Coefficient for SCB.
649	`wec=0`	Coefficient for SCC.
650	`imax=1000 A`	Maximum current up to which forward current behaves exponentially.
651	`trj=21 C`	reference temperature.
652	`frev=1.0e3`	Coefficient for reverse breakdown current limitation.
653	`cjorbot=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.
654	`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.
655	`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
656	`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

657	`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
658	`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.
659	`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
660	`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
661	`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
662	`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
663	`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
664	`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
665	`idsatrbot=1E-12 Am^-2`	Saturation current density at the reference temperature of bottom component for source-bulk junction.
666	`idsatrsti=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
667	`idsatrgat=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
668	`csrhbot=1E2 Am^-3`	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
669	`csrhsti=1E-4 Am^-2`	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
670	`csrhgat=1E-4 Am^-2`	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

671	`xjunsti=100E-9 m`	Junction depth of STI-edge component for source-bulk junction.
672	`xjungat=100E-9 m`	Junction depth of gate-edge component for source-bulk junction.
673	`ctatbot=1E2 Am`$^{-3}$	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
674	`ctatsti=1E-4 Am`$^{-2}$	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
675	`ctatgat=1E-4 Am`$^{-2}$	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
676	`mefftatbot=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
677	`mefftatsti=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
678	`mefftatgat=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
679	`cbbtbot=1E-12 AV`$^{-3}$	Band-to-band tunneling prefactor of bottom component for source-bulk junction.
680	`cbbtsti=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
681	`cbbtgat=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
682	`fbbtrbot=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

683	`fbbtrsti=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
684	`fbbtrgat=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
685	`stfbbtbot=-1E-3 K^-1`	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
686	`stfbbtsti=-1E-3 K^-1`	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
687	`stfbbtgat=-1E-3 K^-1`	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
688	`vbrbot=10 V`	Breakdown voltage of bottom component for source-bulk junction.
689	`vbrsti=10 V`	Breakdown voltage of STI-edge component for source-bulk junction.
690	`vbrgat=10 V`	Breakdown voltage of gate-edge component for source-bulk junction.
681	`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component for source-bulk junction.
692	`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
693	`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
694	`cjorbotd=1E-3 Fm`$^{-2}$	

© 2023 Cadence Design Systems, Inc.

		Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.
695	`cjorstid=1E-9 Fm^-1`	
		Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.
696	`cjorgatd=1E-9 Fm^-1`	
		Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.
697	`vbirbotd=1 V`	Built-in voltage at the reference temperature of bottom component for drain-bulk junction.
698	`vbirstid=1 V`	Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.
699	`vbirgatd=1 V`	Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.
700	`pbotd=0.5`	Grading coefficient of bottom component for drain-bulk junction.
701	`pstid=0.5`	Grading coefficient of STI-edge component for drain-bulk junction.
702	`pgatd=0.5`	Grading coefficient of gate-edge component for drain-bulk junction.
703	`phigbotd=1.16 V`	Zero-temperature bandgap voltage of bottom component for drain-bulk junction.
704	`phigstid=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.
705	`phiggatd=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.
706	`idsatrbotd=1E-12 Am`$^{-2}$	
		Saturation current density at the reference temperature of bottom component for drain-bulk junction.
707	`idsatrstid=1E-18 Am^-1`	
		Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.
708	`idsatrgatd=1E-18 Am^-1`	

© 2023 Cadence Design Systems, Inc.

		Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.
709	csrhbotd=1E2 Am^{-3}	
		Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.
710	csrhstid=1E-4 Am^{-2}	
		Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
711	csrhgatd=1E-4 Am^{-2}	
		Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
712	xjunstid=100E-9 m	Junction depth of STI-edge component for drain-bulk junction.
713	xjungatd=100E-9 m	Junction depth of gate-edge component for drain-bulk junction.
714	ctatbotd=1E2 Am^{-3}	
		Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
715	ctatstid=1E-4 Am^{-2}	
		Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
716	ctatgatd=1E-4 Am^{-2}	
		Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.
717	mefftatbotd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
718	mefftatstid=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.
719	mefftatgatd=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
720	cbbtbotd=1E-12 AV^{-3}	

© 2023 Cadence Design Systems, Inc.

		Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
721	`cbbtstid=1E-18 AV-3m`	
		Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.
722	`cbbtgatd=1E-18 AV-3m`	
		Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.
723	`fbbtrbotd=1E9 Vm^-1`	
		Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.
724	`fbbtrstid=1E9 Vm^-1`	
		Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.
725	`fbbtrgatd=1E9 Vm^-1`	
		Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.
726	`stfbbtbotd=-1E-3 K^-1`	
		Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.
727	`stfbbtstid=-1E-3 K^-1`	
		Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.
728	`stfbbtgatd=-1E-3 K^-1`	
		Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.
729	`vbrbotd=10 V`	Breakdown voltage of bottom component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

730	`vbrstid=10 V`	Breakdown voltage of STI-edge component for drain-bulk junction.
731	`vbrgatd=10 V`	Breakdown voltage of gate-edge component for drain-bulk junction.
732	`pbrbotd=4 V`	Breakdown onset tuning parameter of bottom component for drain-bulk junction.
733	`pbrstid=4 V`	Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.
734	`pbrgatd=4 V`	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
735	`swjunexp=0`	Flag for JUNCAP-express; 0,full model, 1,express model.
736	`vjunref=2.5`	Typical maximum source-bulk junction voltage; usually about 2*VSUP.
737	`fjunq=0.03`	Fraction below which source-bulk junction capacitance components are considered negligible.
738	`vjunrefd=2.5`	Typical maximum drain-bulk junction voltage; usually about 2*VSUP.
739	`fjunqd=0.03`	Fraction below which drain-bulk junction capacitance components are considered negligible.
740	`dta=0.0 K`	Temperature offset w.r.t. ambient temperature.
741	`noisemethod=oldcmi`	Induced gate noise implementation. Possible values are `oldcmi` and `subckt`.
742	`swqsat=0`	Flag for separate capacitance calculation in saturation only: 0=off, 1=on.
743	`swqpart=0`	Flag for drain/source charge partitioning; 0=linear distribution, 1=source.Flag for drain/source charge partitioning; 0=linear distribution, 1=source.
744	`cfac=0.0`	DIBL-parameter of charge model when SWQSAT=1.
745	`thesatac=1.0 V^-1`	Velocity saturation parameter at TR of charge model when SWQSAT=1.
746	`axac=3.0`	Linear/saturation transition factor of charge model when SWQSAT=1.

© 2023 Cadence Design Systems, Inc.

747	`alpac=0.01`	CLM pre-factor of charge model when SWQSAT=1.
748	`gc2ov=0.375`	Gate overlap current slope factor, used only when SWIGATE=2.
749	`gc3ov=0.063`	Gate overlap current curvature factor, used only when SWIGATE=2.
750	`cfacl=0.0`	Length dependence of DIBL-parameter of charge model when SWQSAT=1.
751	`cfaclexp=2.0`	Exponent for length dependence of CF.
752	`cfacw=0.0`	Width dependence of CF.
753	`thesataco=0.0 V^-1`	Geometry-independent velocity saturation parameter at TR of charge model when SWQSAT=1.
754	`thesatacl=0.05 V^-1`	Length dependence of THESATAC.
755	`thesataclexp=1.0`	Exponent for length dependence of THESATAC.
756	`thesatacw=0.0`	Width dependence of THESATAC.
757	`thesataclw=0.0`	Area dependence of THESATAC.
758	`axaco=18.0`	Geometry-independent linear/saturation transition factor of charge model when SWQSAT=1.
759	`axacl=0.4`	Length dependence of AXAC.
760	`alpacl=5.0e-4`	Length dependence of ALPAC.
761	`alpaclexp=1.0`	Exponent for length dependence of ALPAC.
762	`alpacw=0.0`	Width dependence of ALPAC.
763	`gc2ovo=0.375`	Gate overlap current slope factor, used only when SWIGATE=2.
764	`gc3ovo=0.063`	Gate overlap current curvature factor, used only when SWIGATE=2.
765	`pocfac=0.0`	Coefficient for the geometry dependence of CFAC.
766	`plcfac=0.0`	Coefficient for the length dependence of CFAC.
767	`pwcfac=0.0`	Coefficient for the width dependence of CFAC.
768	`plwcfac=0.0`	Coefficient for the length times width dependence of CFAC.
769	`pothesatac=1.0 V^-1`	Coefficient for the geometry-independent part of THESATAC.

© 2023 Cadence Design Systems, Inc.

770	`plthesatac=0.0 V^-1`	Coefficient for the length dependence of THESATAC.
771	`pwthesatac=0.0 V^-1`	Coefficient for the width dependence of THESATAC.
772	`plwthesatac=0.0 V^-1`	Coefficient for the length times width dependence of THESATAC.
773	`poaxac=3.0`	Coefficient for the geometry-independent part of AXAC.
774	`plaxac=0.0`	Coefficient for the length dependence of AXAC.
775	`pwaxac=0.0`	Coefficient for the width dependence of AXAC.
776	`plwaxac=0.0`	Coefficient for the length times width dependence of AXAC.
777	`poalpac=1.0e-2`	Coefficient for the geometry-independent part of ALPAC.
778	`plalpac=0.0`	Coefficient for the length dependence of ALPAC
779	`pwalpac=0.0`	Coefficient for the width dependence of ALPAC.
780	`plwalpac=0.0`	Coefficient for the length times width dependence of ALPAC.
781	`pogc2ov=0.375`	Coefficient for the geometry-independent part of GC2OV, used only when SWIGATE=2.
782	`pogc3ov=0.063`	Coefficient for the geometry-independent part of GC3OV, used only when SWIGATE=2.
783	`kvsatac=0.0 m`	Saturation velocity degradation/enhancement coefficient of charge model when SWQSAT=1.
784	`betnedge=5.0e-4` $m^2/V/s$	Channel aspect ratio times zero-field mobility of edge transistor.
785	`stbetedge=1.0`	Temperature dependence of BETNEDGE.
786	`betedgew=0.0`	Width scaling coefficient of edge transistor mobility.
787	`cfbedge=0.0 V^-1`	Bulk voltage dependence parameter of DIBL-parameter of edge transistors.
788	`cfbedgeo=0.0 V^-1`	Bulk voltage dependence parameter of DIBL-parameter of edge transistors.
789	`cfd=0.0 V^-1`	Drain voltage dependence of CF.

© 2023 Cadence Design Systems, Inc.

790	`cfdedge=0.0 V^-1`	Drain voltage dependence parameter of DIBL-parameter of edge transistors.
791	`cfdedgeo=0.0 V^-1`	Drain voltage dependence parameter of DIBL-parameter of edge transistors.
792	`cfdo=0.0 V^-1`	Drain voltage dependence of CF.
793	`cfedge=0.0`	DIBL parameter of edge transistors.
794	`cfedgel=0.0`	Length dependence of DIBL-parameter of edge transistors.
795	`cfedgelexp=2.0`	Exponent for length dependence of DIBL-parameter of edge transistors.
796	`cfedgew=0.0`	Width dependence of DIBL-parameter of edge transistors.
797	`ctedge=0.0`	Interface states factor of edge transistors.
798	`ctedgeo=0.0`	Geometry-independent interface states factor of edge transistors.
799	`ctedgel=0.0`	Length dependence of interface states factor of edge transistors.
800	`ctedgelexp=1.0`	Exponent for length dependence of interface states factor of edge transistors.
801	`dphibedge=0.0 V`	Offset parameter for PHIB of edge transistors.
802	`dphibedgeo=0.0 V`	Geometry-independent of edge transistor PHIB offset.
803	`dphibedgel=0.0 V`	Length dependence of edge transistor PHIB offset.
804	`dphibedgelexp=1.0`	Exponent for length dependence of edge transistor PHIB offset.
805	`dphibedgew=0.0 V`	Width dependence of edge transistor PHIB offset.
806	`dphibedgelw=0.0 V`	Area dependence of edge transistor PHIB offset.
807	`efedge=1.0`	Flicker noise frequency exponent of edge transistors.
808	`efedgeo=1.0`	Flicker noise frequency exponent.
809	`fbetedge=0.0`	Length dependence of edge transistor mobility.
810	`fntedge=1.0`	Thermal noise coefficient of edge transistors.
811	`fntedgeo=1.0`	Thermal noise coefficient.

© 2023 Cadence Design Systems, Inc.

812	`lpedge=1.0e-8 m`	Exponent for length dependence of edge transistor mobility.
813	`neffedge=5.0e23 m`$^{-3}$	Effective substrate doping of edge transistors.
814	`nfaedge=8.0e22 V^-1/m`^{4}	First coefficient of flicker noise of edge transistors.
815	`nfaedgelw=8.0e22 V^-1/m`^{4}	First coefficient of flicker noise for 1 um^2 channel area.
816	`nfbedge=3.0e07 V^-1/m`^{2}	Second coefficient of flicker noise of edge transistors.
817	`nfbedgelw=3.0e7 V^-1/m`^{2}	Second coefficient of flicker noise for 1 um^2 channel area.
818	`nfcedge=0.0 V^-1`	Third coefficient of flicker noise of edge transistors.
819	`nfcedgelw=0.0 V^-1`	Third coefficient of flicker noise for 1 um^2 channel area.
820	`nsubedgel=0.0`	Length dependence of edge transistor substrate doping.
821	`nsubedgew=0.0`	Width dependence of edge transistor substrate doping.
822	`nsubedgelw=0.0`	Area dependence of edge transistor substrate doping.
823	`nsubedgeo=5.0e23 m`$^{-3}$	Geometry-independent substrate doping of edge transistors.
824	`psce=0.0`	Subthreshold slope coefficient for short channel transistor.
825	`psceb=0.0 V^-1`	Bulk voltage dependence parameter of subthreshold slope coefficient for short channel transistor.
826	`pscebedge=0.0 V^-1`	Bulk voltage dependence parameter of subthreshold slope coefficient for short channel edge transistors.
	`pscebedgeo=0.0 V^-1`	Bulk voltage dependence parameter of subthreshold slope coefficient for short channel edge transistors.
827	`pscebo=0.0 V^-1`	Bulk voltage dependence parameter of subthreshold slope coefficient for short channel transistor.
	`psced=0.0 V^-1`	Drain voltage dependence parameter of subthreshold slope coefficient for short channel transistor.
828	`pscededge=0.0 V^-1`	Drain voltage dependence parameter of subthreshold slope coefficient for short channel edge transistors.

© 2023 Cadence Design Systems, Inc.

829	`pscedo=0.0 V^-1`	Drain voltage dependence parameter of subthreshold slope coefficient for short channel transistor.
830	`pscededgeo=0.0 V^-1`	Drain voltage dependence parameter of subthreshold slope coefficient for short channel edge transistors.
831	`psceedge=0.0`	Subthreshold slope coefficient for short channel edge transistors.
832	`psceedgel=0.0`	Length dependence of subthreshold slope coefficient for short channel edge transistors.
833	`psceedgelexp=2.0`	Exponent for length dependence of subthreshold slope coefficient for short channel edge transistors.
834	`psceedgew=0.0`	Exponent for length dependence of subthreshold slope coefficient for short channel edge transistor.
835	`pscel=0.0`	Length dependence of subthreshold slope coefficient for short channel transistor.
836	`pscelexp=2.0`	Exponent for length dependence of subthreshold slope coefficient for short channel transistor.
837	`pscew=0.0`	Exponent for length dependence of subthreshold slope coefficient for short channel transistor.
838	`stbetedgeo=1.0`	Geometry-independent temperature dependence of BETNEDGE.
839	`stbetedgel=0.0`	Length dependence of temperature dependence of BETNEDGE.
840	`stbetedgew=0.0`	Width dependence of temperature dependence of BETNEDGE.
841	`stbetedgelw=0.0`	Area dependence of temperature dependence of BETNEDGE.
842	`stvfbedge=5.0e-4 V/K`	Temperature dependence of VFBEDGE.
843	`stvfbedgeo=5.0e-4 V/K`	Geometry-independent temperature dependence of VFBEDGE.
844	`stvfbedgel=0.0 V/K`	Length dependence of temperature dependence of VFBEDGE.
845	`stvfbedgew=0.0 V/K`	Width dependence of temperature dependence of VFBEDGE.

© 2023 Cadence Design Systems, Inc.

846	`stvfbedgelw=0.0 V/K`	Area dependence of temperature dependence of VFBEDGE.
847	`vfbedge=(-1.0) V`	Flat band voltage of edge transistors at TR.
848	`vfbedgeo=(-1.0) V`	Geometry-independent flat-band voltage of edge transistors at TR.
849	`wedge=1.0e-8 m`	Electrical width of edge transistor per side.
850	`wedgew=0.0`	Width dependence of edge WEDGE.
851	`w=10e-6 m`	Default width.
852	`l=10e-6 m`	Default length.
853	`nf=1`	Number of fingers, It served as the default value of instance nf.
854	`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
855	`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
856	`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
857	`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.
858	`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
859	`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
860	`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
861	`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.
862	`vgbr_max=vgb_max V`	Maximum allowed reverse voltage cross gate and bulk.

© 2023 Cadence Design Systems, Inc.

863	`vbsr_max=vbs_max V`	Maximum allowed reverse voltage cross source and bulk.
864	`vbdr_max=vbd_max V`	Maximum allowed reverse voltage cross source/drain and bulk.
865	`vbsr_max=vbs_max V`	Maximum allowed reverse voltage cross source and bulk.
866	`vbdr_max=vbd_max V`	Maximum allowed reverse voltage cross source/drain and bulk.
867	`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
868	`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
869	`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
870	`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
871	`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
872	`st2vfb=0.0` k^{-1}	Quadratic temperature dependence of VFB.
873	`thecs=2.0`	Coulomb scattering exponent at TR.
874	`stthecs=0.0`	Temperature dependence of THECS.
875	`post2vfb=0.0` k^{-1}	Coefficient for the geometry-independent part of ST2VFB.
876	`potthecs=2.0`	Coefficient for the geometry-independent part of THECS.
877	`postthecs=0.0`	Coefficient for the geometry-independent part of STTHECS.

© 2023 Cadence Design Systems, Inc.

878	`st2vfb0=0.0 k`$^{-1}$	Quadratic temperature dependence of VFB.
879	`thecso=2.0`	Coulomb scattering exponent at TR.
880	`stthecso=0.0`	Temperature dependence of THECS.
881	`ctg=0.0`	Gate voltage dependence of interface states factor.
882	`ctb=0.0`	Bulk voltage dependence of interface states factor.
883	`stct=1.0`	Geometry-independent temperature dependence of CT.
884	`poctg=0.0`	Coefficient for the geometry-independent part of CTG.
885	`poctb=0.0`	Coefficient for the geometry-independent part of CTB.
886	`postct=1.0`	Coefficient for the geometry-independent part of STCT.
887	`ctbo=0.0`	Bulk voltage dependence of interface states factor.
888	`stcto=1.0`	Geometry-independent temperature dependence of CT.
889	`ctgo=0.0`	Gate voltage dependence of interface states factor.
890	`nsubedgelexp=1.0`	Exponent for length dependence of edge transistor substrate doping.
891	`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, `tispice` and `pspice`.

Output Parameters

1	`weff (m)`	Effective channel width for geometrical models.
2	`leff (m)`	Effective channel length for geometrical models.
3	`lp_stvfb (V/K)`	Local parameter STVFB after clipping.
4	`lp_tox (m)`	Local parameter TOX after clipping.
5	`lp_epsrox`	Local parameter EPSROX after clipping.
6	`lp_neff (m`$^{-3}$`)`	Local parameter NEFF after clipping.

© 2023 Cadence Design Systems, Inc.

7	`lp_facneffac`	Local parameter FACNEFFAC after clipping.
8	`lp_gfacnud`	Local parameter GFACNUD after clipping.
9	`lp_vsbnud (V)`	Local parameter VSBNUD after clipping.
10	`lp_dvsbnud (V)`	Local parameter DVSBNUD after clipping.
11	`lp_vnsub (V)`	Local parameter VNSUB after clipping.
12	`lp_nslp (V)`	Local parameter NSLP after clipping.
13	`lp_dnsub (V^-1)`	Local parameter DNSUB after clipping.
14	`lp_dphib (V)`	Local parameter DPHIB after clipping.
15	`lp_delvtac (V)`	Local parameter DELVTAC after clipping.
16	`lp_np (m^-3)`	Local parameter NP after clipping.
17	`lp_toxov (m)`	Local parameter TOXOV after clipping.
18	`lp_toxovd (m)`	Local parameter TOXOVD after clipping.
19	`lp_nov (m^-3)`	Local parameter NOV after clipping.
20	`lp_novd (m^-3)`	Local parameter NOVD after clipping.
21	`lp_cf`	Local parameter CF after clipping.
22	`lp_cfd (V^-1)`	Local parameter CFD after clipping.
23	`lp_cfb (V^-1)`	Local parameter CFB after clipping.
24	`lp_psce`	Local parameter PSCE after clipping.
25	`lp_psceb (V^-1)`	Local parameter PSCEB after clipping.
26	`lp_psced (V^-1)`	Local parameter PSCED after clipping.
27	`lp_stbet`	Local parameter STBET after clipping.
28	`lp_stmue`	Local parameter STMUE after clipping.
29	`lp_stthemu`	Local parameter STTHEMU after clipping.
30	`lp_stcs`	Local parameter STCS after clipping.
31	`lp_stxcor`	Local parameter STXCOR after clipping.

© 2023 Cadence Design Systems, Inc.

32	`lp_feta`	Local parameter FETA after clipping.
33	`lp_strs`	Local parameter STRS after clipping.
34	`lp_rsb (V^-1)`	Local parameter RSB after clipping.
35	`lp_rsg (V^-1)`	Local parameter RSG after clipping.
36	`lp_stthesat`	Local parameter STTHESAT after clipping.
37	`lp_thesatb (V^-1)`	Local parameter THESATB after clipping.
38	`lp_thesatg (V^-1)`	Local parameter THESATG after clipping.
39	`lp_ax`	Local parameter AX after clipping.
40	`lp_alp`	Local parameter ALP after clipping.
41	`lp_alp1 (V)`	Local parameter ALP1 after clipping.
42	`lp_alp2 (V^-1)`	Local parameter ALP2 after clipping.
43	`lp_vp (V)`	Local parameter VP after clipping.
44	`lp_a1`	Local parameter A1 after clipping.
45	`lp_sta2`	Local parameter STA2 after clipping.
46	`lp_a3`	Local parameter A3 after clipping.
47	`lp_a4 (m`$^{-3}$`)`	Local parameter A4 after clipping.
48	`lp_gco`	Local parameter GCO after clipping.
49	`lp_iginv (A)`	Local parameter IGINV after T-scaling and clipping.
50	`lp_igov (A)`	Local parameter IGOV after T-scaling and clipping.
51	`lp_igovd (A)`	Local parameter IGOVD after T-scaling and clipping.
52	`lp_stig`	Local parameter STIG after clipping.
53	`lp_gc2`	Local parameter GC2 after clipping.
54	`lp_gc3`	Local parameter GC3 after clipping.
55	`lp_chib (V)`	Local parameter CHIB after clipping.
56	`lp_agidl (A/V`^{3}`)`	Local parameter AGIDL after clipping.

© 2023 Cadence Design Systems, Inc.

57	lp_agidld (A/V^3)	Local parameter AGIDLD after clipping.
58	lp_bgidl (V)	Local parameter BGIDL after T-scaling and clipping.
59	lp_bgidld (V)	Local parameter BGIDLD after T-scaling and clipping.
60	lp_stbgidl (V/K)	Local parameter STBGIDL after clipping.
61	lp_stbgidld (V/K)	Local parameter STBGIDLD after clipping.
62	lp_cgidl	Local parameter CGIDL after clipping.
63	lp_cgidld	Local parameter CGIDLD after clipping.
64	lp_cox (F)	Local parameter COX after clipping.
65	lp_cgov (F)	Local parameter CGOV after clipping.
66	lp_cgovd (F)	Local parameter CGOVD after clipping.
67	lp_cgbov (F)	Local parameter CGBOV after clipping.
68	lp_cfr (F)	Local parameter CFR after clipping.
69	lp_cfrd (F)	Local parameter CFRD after clipping.
70	lp_fnt	Local parameter FNT after clipping.
71	lp_fntexc	Local parameter FNTEXC after clipping.
72	lp_nfa (1/(V m^4))	Local parameter NFA after clipping.
73	lp_nfb (1/(V m^2))	Local parameter NFB after clipping.
74	lp_nfc (V^-1)	Local parameter NFC after clipping.
75	lp_ef	Local parameter EF after clipping.
76	lp_rg (Ω)	Local parameter RG after clipping.
77	lp_rse (Ω)	Local parameter RSE after clipping.
78	lp_rde (Ω)	Local parameter RDE after clipping.
79	lp_rbulk (Ω)	Local parameter RBULK after clipping.
80	lp_rwell (Ω)	Local parameter RWELL after clipping.

© 2023 Cadence Design Systems, Inc.

81	`lp_rjuns (Ω)`	Local parameter RJUNS after clipping.
82	`lp_rjund (Ω)`	Local parameter RJUND after clipping.
83	`lp_rth (K/W)`	Local parameter RTH after T-scaling and clipping.
84	`lp_cth (J/K)`	Local parameter CTH after clipping.
85	`lp_strth`	Local parameter STRTH after clipping.
86	`lp_vfbedge (V)`	Local parameter VFBEDGE after T-scaling and clipping.
87	`lp_stvfbedge (V/K)`	Local parameter STVFBEDGE after clipping.
88	`lp_dphibedge (V)`	Local parameter DPHIBEDGE after clipping.
89	`lp_neffedge (m`$^{-3}$`)`	Local parameter NEFFEDGE after clipping.
90	`lp_ctedge`	Local parameter CTEDGE after clipping.
91	`lp_betnedge (m`^{2}`/V/s)`	Local parameter BETNEDGE after T-scaling and clipping.
92	`lp_stbetedge`	Local parameter STBETEDGE after clipping.
93	`lp_psceedge`	Local parameter PSCEEDGE after clipping.
94	`lp_pscebedge (V^-1)`	Local parameter PSCEBEDGE after clipping.
95	`lp_pscededge (V^-1)`	Local parameter PSCEDEDGE after clipping.
96	`lp_cfedge (V)`	Local parameter CFEDGE after clipping.
97	`lp_cfdedge ( V^-1)`	Local parameter CFDEDGE after clipping.
98	`lp_cfbedge ( V^-1)`	Local parameter CFBEDGE after clipping.

© 2023 Cadence Design Systems, Inc.

99	`lp_fntedge ( )`	Local parameter FNTEDGE after clipping.
100	`lp_nfaedge ( 1/(V m^4))`	Local parameter NFAEDGE after clipping.
101	`lp_nfbedge ( 1/(V m^4))`	Local parameter NFBEDGE after clipping.
102	`lp_nfcedge ( V^-1)`	Local parameter NFCEDGE after clipping.
103	`lp_efedge`	Local parameter EFEDGE after clipping.
104	`cjosbot (F)`	Bottom component of total zero-bias source junction capacitance at device temperature.
105	`cjossti (F)`	STI-edge component of total zero-bias source junction capacitance at device temperature.
106	`cjosgat (F)`	Gate-edge component of total zero-bias source junction capacitance at device temperature.
107	`vbisbot (V)`	Built-in voltage of source-side bottom junction at device temperature.
108	`vbissti (V)`	Built-in voltage of source-side STI-edge junction at device temperature.
109	`vbisgat (V)`	Built-in voltage of source-side gate-edge junction at device temperature.
110	`idsatsbot (A)`	Total source-side bottom junction saturation current.
111	`idsatssti (A)`	Total source-side STI-edge junction saturation current.
112	`idsatsgat (A)`	Total source-side gate-edge junction saturation current.
113	`cjosbotd (F)`	Bottom component of total zero-bias drain junction capacitance at device temperature.
114	`cjosstid (F)`	STI-edge component of total zero-bias drain junction capacitance at device temperature.
115	`cjosgatd (F)`	Gate-edge component of total zero-bias drain junction capacitance at device temperature.
116	`vbisbotd (V)`	Built-in voltage of drain-side bottom junction at device temperature.

© 2023 Cadence Design Systems, Inc.

117	`vbisstid (V)`	Built-in voltage of drain-side STI-edge junction at device temperature.
118	`vbisgatd (V)`	Built-in voltage of drain-side gate-edge junction at device temperature.
119	`idsatsbotd (A)`	Total drain-side bottom junction saturation current.
120	`idsatsstid (A)`	Total drain-side STI-edge junction saturation current.
121	`idsatsgatd (A)`	Total drain-side gate-edge junction saturation current.
122	`lp_munqs`	Local parameter MUNQS after clipping.
123	`lv2 (m)`	Alias of w.
124	`lv1 (m)`	Alias of l.
125	`lv3 (m^2)`	Alias of ad.
126	`lv4 (m^2)`	Alias of as.
127	`lv11 (m)`	Alias of pd.
128	`lv12 (m)`	Alias of ps.
129	`tempeff (C)`	Effective temperature for a single device.
130	`meff`	Effective multiplicity factor (m-factor).
131	`lp_st2vfb (K^-1)`	Local parameter ST2VFB after clipping.
132	`lp_stthecs`	Local parameter STTHECS after clipping.
133	`lp_ctb`	Local parameter CTB after clipping.
134	`lp_stct`	Local parameter STCT after clipping.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

1	`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
2	`ctype`	Flag for channel type.
3	`sdint`	Flag for source-drain interchange.
4	`ise (A)`	Total source current.
5	`ige (A)`	Total gate current.
6	`ide (A)`	Total drain current.
7	`ibe (A)`	Total bulk current.
8	`is (A)`	Total source current.
9	`ig (A)`	Total gate current.
10	`id (A)`	Total drain current.
11	`ib (A)`	Total bulk current.
12	`ids (A)`	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
13	`idb (A)`	Drain to bulk current.
14	`isb (A)`	Source to bulk current.
15	`igs (A)`	Gate-source tunneling current.
16	`igd (A)`	Gate-drain tunneling current.
17	`igb (A)`	Gate-bulk tunneling current.
18	`idedge (A)`	Drain current of edge transistors.
19	`igcs (A)`	Gate-channel tunneling current (source component).
20	`igcd (A)`	Gate-channel tunneling current (drain component).
21	`iavl (A)`	Substrate current due to weak avalanche.
22	`igisl (A)`	Gate-induced source leakage current.
23	`igidl (A)`	Gate-induced drain leakage current.
24	`ijs (A)`	Total source junction current.
25	`ijsbot (A)`	Source junction current (bottom component).

© 2023 Cadence Design Systems, Inc.

26	`ijsgat (A)`	Source junction current (gate-edge component).
27	`ijssti (A)`	Source junction current (STI-edge component).
28	`ijd (A)`	Total drain junction current.
29	`ijdbot (A)`	Drain junction current (bottom component).
30	`ijdgat (A)`	Drain junction current (gate-edge component).
31	`ijdsti (A)`	Drain junction current (STI-edge component).
32	`qg (Coul)`	Intrinsic gate charge.
33	`qd (Coul)`	Intrinsic drain charge.
34	`qb (Coul)`	Intrinsic bulk charge.
35	`qs (Coul)`	Intrinsic source charge.
36	`qgs_ov (Coul)`	Overlap charge for gate-source.
37	`qgd_ov (Coul)`	Overlap charge for gate-drain.
38	`qfgs (Coul)`	Total outerFringe + overlap for gate-source.
39	`qfgd (Coul)`	Total outerFringe + overlap for gate-drain.
40	`qgb_ov (Coul)`	Gate-bulk overlap charge.
41	`qjun_s (Coul)`	Junction charge on source side.
42	`qjun_d (Coul)`	Junction charge on drain side.
43	`vds (V)`	Drain-source voltage.
44	`vgs (V)`	Gate-source voltage.
45	`vgd (V)`	Gate-drain voltage.
46	`vsb (V)`	Source-bulk voltage.
47	`vdb (V)`	Drain-bulk voltage.
48	`vth0 (V)`	Zero-bias threshold voltage.
49	`vto (V)`	Zero-bias threshold voltage.
50	`vts (V)`	Threshold voltage including back bias effects.
51	`vth (V)`	Threshold voltage including back bias and drain bias effects.
52	`vgt (V)`	Effective gate drive voltage including back bias and drain bias effects.

© 2023 Cadence Design Systems, Inc.

53	`vth_drive (V)`	Effective gate drive voltage including back bias and drain bias effects. Alias for Vgt..
54	`vdss (V)`	Drain saturation voltage at actual bias.
55	`vdsat (V)`	Drain saturation voltage at actual bias.
56	`vsat`	Saturation limit.
57	`vdsat_marg`	Saturation limit.
58	`pwr (W)`	Power at op point.
59	`gm (1/Ω)`	Transconductance.
60	`gmb (1/Ω)`	Substrate transconductance.
61	`go (1/Ω)`	Output conductance.
62	`gds (1/Ω)`	Output conductance.
63	`gjs (1/Ω)`	Source junction conductance.
64	`gjd (1/Ω)`	Drain junction conductance.
65	`cdd (F)`	Drain capacitance.
66	`cdg (F)`	Drain-gate capacitance.
67	`cds (F)`	Drain-source capacitance.
68	`cdb (F)`	Drain-bulk capacitance.
69	`cgd (F)`	Gate-drain capacitance.
70	`cgg (F)`	Gate capacitance.
71	`cgs (F)`	Gate-source capacitance.
72	`cgb (F)`	Gate-bulk capacitance.
73	`csd (F)`	Source-drain capacitance.
74	`csg (F)`	Source-gate capacitance.
75	`css (F)`	Source capacitance.
76	`csb (F)`	Source-bulk capacitance.
77	`cbd (F)`	Bulk-drain capacitance.
78	`cbg (F)`	Bulk-gate capacitance.
79	`cbs (F)`	Bulk-source capacitance.
80	`cbb (F)`	Bulk capacitance.

© 2023 Cadence Design Systems, Inc.

81	co (F)	Output Drain-Source capacitance.
82	cm (F)	Capacitance element 1 for QS model.
83	cmb (F)	Capacitance element 2 for QS model.
84	cmx (F)	Capacitance element 3 for QS model.
85	tau1 (s)	Time constant related to NQS first frequency pole.
86	fqslim (Hz)	QS model frequency limit.
87	cgsol (F)	Total gate-source overlap capacitance.
88	cgdol (F)	Total gate-drain overlap capacitance.
89	cgbol (F)	Total gate-bulk overlap capacitance.
90	cjs (F)	Total source junction capacitance.
91	cjsbot (F)	Source junction capacitance (bottom component).
92	cjsgat (F)	Source junction capacitance (gate-edge component).
93	cjssti (F)	Source junction capacitance (STI-edge component).
94	cjd (F)	Total drain junction capacitance.
95	cjdbot (F)	Drain junction capacitance (bottom component).
96	cjdgat (F)	Drain junction capacitance (gate-edge component).
97	cjdsti (F)	Drain junction capacitance (STI-edge component).
98	lpoly (m)	Length of poly.
99	u	Transistor gain.
100	self_gain	Transistor gain.
101	rout (Ω)	Small-signal output resistance.
102	vearly (V)	Equivalent early voltage.
103	beff (A/V^2)	Gain factor.
104	GmoverI (1/V)	Transconductance efficiency.
105	fug (Hz)	Unity gain frequency at actual bias.
106	ft (Hz)	Unity gain frequency at actual bias.
107	rg (Ω)	Gate resistance.
108	rgate (Ω)	Gate resistance.
109	sfl	Flicker noise current density at 1 Hz.

© 2023 Cadence Design Systems, Inc.

110	sqrtsff	Input-referred RMS white noise voltage density at 1 kHz.
111	sqrtsfw	Input-referred RMS white noise voltage density.
112	sid	White noise current density.
113	sig	Induced gate noise current density at 1 Hz.
114	cigid	Imaginary part of correlation coefficient between Sig and Sid.
115	noi_mid	
116	noi_mig	
117	noi_migid	
118	noi_cgeff	
119	noi_cigid	
120	fknee	Cross-over frequency above which white noise is dominant.
121	sigs	Gate-source current noise spectral density.
122	sigd	Gate-drain current noise spectral density.
123	siavl	Impact ionization current noise spectral density.
124	ssi	Total source junction current noise spectral density.
125	sdi	Total drain junction current noise spectral density.
126	sfledge (A^2/Hz)	Flicker noise current spectral density at 1 Hz of edge transistors.
127	sidedge (A^2/Hz)	White noise current spectral density of edge transistors.
128	lp_vfb (V)	Local parameter VFB after T-scaling and clipping.
129	lp_ct	Local parameter CT after clipping.
130	lp_betn (m^2/(V s)	Local parameter BETN after T-scaling and clipping.
131	lp_mue (m/V)	Local parameter MUE after T-scaling and clipping.

© 2023 Cadence Design Systems, Inc.

132	`lp_themu`	Local parameter THEMU after T-scaling and clipping.
133	`lp_cs`	Local parameter CS after T-scaling and clipping.
134	`lp_xcor (V^-1)`	Local parameter XCOR after T-scaling and clipping.
135	`lp_rs (Ω)`	Local parameter RS after T-scaling and clipping.
136	`lp_thesat (V^-1)`	Local parameter THESAT after T-scaling and clipping.
137	`lp_a2 (V)`	Local parameter A2 after T-scaling and clipping.
138	`pdiss (W)`	Power dissipation.
139	`dtsh (K)`	Temperature rise due to self heating.
140	`tk (K)`	Device Temperature.
141	`vbs (V)`	Bulk-source voltage.
142	`lv13`	Alias of nrd.
143	`lv14`	Alias of nrs.
144	`lv36 (F)`	Alias of cgsol.
145	`lv37 (F)`	Alias of cgdol.
146	`lv38 (F)`	Alias of cgbol.
147	`lv51 (m)`	Alias of tox.
148	`lp_thecs`	Local parameter THECS after T-scaling and clipping.
149	`lp_ctg`	Local parameter CTG after clipping.
150	`lp_cfac`	Local parameter CFAC after clipping.
151	`lp_thesatac (V^-1)`	Local parameter THESATAC after T-scaling and clipping.
152	`lp_axac`	Local parameter AXAC after clipping.
153	`lp_alpac`	Local parameter ALPAC after clipping.
154	`lp_gc2ov`	Local parameter GC2OV after clipping.
155	`lp_gc3ov`	Local parameter GC3OV after clipping.
156	`OPdef`	1: Device Physics notation. 2: Circuit Simulator notation.

© 2023 Cadence Design Systems, Inc.

157	SDop	Operation mode related to channel type and drain-source voltage sign. Possible values are Forward and Reverse.

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

GmoverI OP-104	idsatrstid M-705	phigstid M-702	pwgfacnud M-141
OPdef OP-165	idsatsbot O-110	pkuo M-634	pwiginv M-264
SDop OP-166	idsatsbotd O-119	pkvtho M-640	pwigov M-268
a1 M-68	idsatsgat O-112	pla1 M-248	pwigovd M-272
a1l M-551	idsatsgatd O-121	pla3 M-254	pwkuowe M-355
a1o M-550	idsatssti O-111	pla4 M-258	pwkvthowe M-351
a1w M-552	idsatsstid O-120	plagidl M-279	pwmue M-191
a2 M-69	ifactor I-35	plagidld M-283	pwneff M-133
a2o M-553	ig OP-9	plalp M-235	pwneffedge M-378
a3 M-71	igb OP-17	plalp1 M-239	pwnfa M-338
a3l M-556	igcd OP-20	plalp2 M-243	pwnfaedge M-407
a3o M-555	igcs OP-19	plalpac M-776	pwnfb M-342
a3w M-557	igd OP-16	plax M-231	pwnfbedge M-411
a4 M-72	ige OP-5	plaxac M-772	pwnfc M-346

© 2023 Cadence Design Systems, Inc.

a4l M-559
a4o M-558
a4w M-560
abdrain I-25
absource I-22
ad I-30
agidl M-81
agidld M-82
agidldw M-570
agidlw M-569
alp M-64
alp1 M-65
alp1l1 M-541
alp1l2 M-543
alp1lexp M-542
alp1w M-544
alp2 M-66
alp2l1 M-545
alp2l2 M-547
alp2lexp M-546
igidl OP-23
iginv M-74
iginvlw M-562
igisl OP-22
igov M-75
igovd M-76
igovdw M-564
igovw M-563
igs OP-15
ijd OP-28
ijdbot OP-29
ijdgat OP-30
ijdsti OP-31
ijs OP-24
ijsbot OP-25
ijsgat OP-26
ijssti OP-27
imax M-648
is OP-8
isb OP-14
plbetn M-182
plbetnedge M-385
plcf M-175
plcfac M-764
plcfd M-178
plcfedge M-399
plcfr M-309
plcfrd M-313
plcgbov M-305
plcgov M-297
plcgovd M-301
plcinr M-320
plcinrd M-324
plcox M-293
plcs M-197
plct M-161
plctedge M-381
pldelvtac M-153
pldphib M-149
pldphibedge M-373
pwnfcedge M-415
pwnov M-168
pwnovd M-172
pwnp M-158
pwpsce M-363
pwpsceedge M-394
pwr OP-58
pwrs M-209
pwstbet M-187
pwstbetedge M-390
pwstthesat M-220
pwstvfb M-127
pwstvfbedge M-370
pwthesat M-216
pwthesatac M-769
pwthesatb M-224
pwthesatg M-228
pwvfb M-123
pwxcor M-203
qb OP-34

© 2023 Cadence Design Systems, Inc.

alp2w M-548
alpac M-745
alpacl M-758
alpaclexp M-759
alpacw M-760
alpl M-538
alplexp M-539
alpnoi M-596
alpw M-540
as I-28
ax M-63
axac M-744
axacl M-757
axaco M-756
axinr M-103
axinro M-588
axl M-537
axo M-536
beff OP-103
betedgew M-784
ise OP-4
isnoisy I-37
ivth M-866
ivth_vdsmin M-869
ivthl M-868
ivthw M-867
jw I-17
kuo M-629
kuowel M-602
kuowelw M-604
kuoweo M-601
kuowew M-603
kvsat M-630
kvsatac M-781
kvtho M-637
kvthowel M-598
kvthowelw M-600
kvthoweo M-597
kvthowew M-599
l I-1
plfacneffac M-136
plfntexc M-333
plgfacnud M-140
pliginv M-263
pligov M-267
pligovd M-271
plkuowe M-354
plkvthowe M-350
plmue M-190
plneff M-132
plneffedge M-377
plnfa M-337
plnfaedge M-406
plnfb M-341
plnfbedge M-410
plnfc M-345
plnfcedge M-414
plnov M-167
plnovd M-171
plnp M-157
qd OP-33
qfgd OP-39
qfgs OP-38
qg OP-32
qgb_ov OP-40
qgd_ov OP-37
qgs_ov OP-36
qjun_d OP-42
qjun_s OP-41
qmc M-15
qs OP-35
rbulk M-114
rbulko M-613
rde M-113
region I-15
region OP-1
rg M-111
rg OP-107
rgate OP-108
rgo M-606

© 2023 Cadence Design Systems, Inc.

betn M-44
betnedge M-782
betw1 M-496
betw2 M-497
bgidl M-83
bgidld M-84
bgidldo M-572
bgidlo M-571
cbb OP-80
cbbtbot M-677
cbbtbotd M-718
cbbtgat M-679
cbbtgatd M-720
cbbtsti M-678
cbbtstid M-719
cbd OP-77
cbg OP-78
cbs OP-79
cdb OP-68
cdd OP-65
l M-852
lap M-421
leff O-2
level M-1
lgdrain I-27
lgsource I-24
lintnoi M-595
lkuo M-632
lkvtho M-638
llodkuo M-635
llodvth M-641
lmax M-358
lmin M-357
lodetao M-644
lov M-481
lovd M-482
lp1 M-492
lp1w M-493
lp2 M-495
lp_a1 O-44
plpsce M-362
plpsceedge M-393
plrs M-208
plstbet M-186
plstbetedge M-389
plstthesat M-219
plstvfb M-126
plstvfbedge M-369
plthesat M-215
plthesatac M-768
plthesatb M-223
plthesatg M-227
plvfb M-122
plwa1 M-250
plwa3 M-256
plwa4 M-260
plwagidl M-281
plwagidld M-285
plwalp M-237
plwalp1 M-241
rint M-607
rjund M-117
rjundo M-616
rjuns M-116
rjunso M-615
rout OP-101
rs M-55
rsb M-57
rsbo M-523
rse M-112
rsg M-58
rsgo M-524
rsh M-611
rshd M-612
rshg M-609
rsw1 M-520
rsw2 M-521
rth M-118
rthlw M-620
rtho M-617

© 2023 Cadence Design Systems, Inc.

cdg OP-66
cds OP-67
cf M-42
cfac M-742
cfacl M-748
cfaclexp M-749
cfactor I-36
cfacw M-750
cfb M-43
cfbedge M-785
cfbedgeo M-786
cfbo M-488
cfd M-787
cfdedge M-788
cfdedgeo M-789
cfdo M-790
cfedge M-791
cfedgel M-792
cfedgelexp M-793
cfedgew M-794
lp_a2 OP-137
lp_a3 O-46
lp_a4 O-47
lp_agidl O-56
lp_agidld O-57
lp_alp O-40
lp_alp1 O-41
lp_alp2 O-42
lp_alpac OP-162
lp_ax O-39
lp_axac OP-161
lp_axinr OP-146
lp_betn OP-130
lp_betnedge O-91
lp_bgidl O-58
lp_bgidld O-59
lp_cf O-21
lp_cfac OP-159
lp_cfb O-23
lp_cfbedge O-98
plwalp2 M-245
plwalpac M-778
plwax M-233
plwaxac M-774
plwbetn M-184
plwbetnedge M-387
plwcf M-177
plwcfac M-766
plwcfedge M-401
plwcfr M-311
plwcfrd M-315
plwcgbov M-307
plwcgov M-299
plwcgovd M-303
plwcinr M-322
plwcinrd M-326
plwcox M-295
plwcs M-199
plwct M-163
plwctedge M-383
rthw1 M-618
rthw2 M-619
rvpoly M-608
rwell M-115
rwello M-614
sa I-3
saref M-626
sb I-4
sbref M-627
sc I-9
sca I-6
scb I-7
scc I-8
scref M-645
sd I-5
sdi OP-125
sdint OP-3
self_gain OP-100
sfl OP-109
sfledge OP-126

© 2023 Cadence Design Systems, Inc.

cfl M-485
cflexp M-486
cfr M-93
cfrd M-94
cfrdw M-579
cfrw M-578
cfw M-487
cgb OP-72
cgbol OP-89
cgbov M-92
cgbovl M-577
cgd OP-69
cgdol OP-88
cgg OP-70
cgidl M-87
cgidld M-88
cgidldo M-576
cgidlo M-575
cgov M-90
lp_cfd O-22
lp_cfdedge O-97
lp_cfedge O-96
lp_cfr O-68
lp_cfrd O-69
lp_cgbov O-67
lp_cgidl O-62
lp_cgidld O-63
lp_cgov O-65
lp_cgovaccg OP-140
lp_cgovd O-66
lp_chib O-55
lp_cinr OP-141
lp_cinrd OP-142
lp_cox O-64
lp_cs OP-133
lp_ct OP-129
lp_ctb O-133
lp_ctedge O-90
plwdelvtac M-155
plwdphib M-151
plwdphibedge M-375
plwfacneffac M-138
plwfntexc M-335
plwgfacnud M-142
plwiginv M-265
plwigov M-269
plwigovd M-273
plwkuowe M-356
plwkvthowe M-352
plwmue M-192
plwneff M-134
plwneffedge M-379
plwnfa M-339
plwnfaedge M-408
plwnfb M-343
plwnfbedge M-412
plwnfc M-347
siavl OP-123
sid OP-112
sidedge OP-127
sig OP-113
sigd OP-122
sigs OP-121
sqrtsff OP-110
sqrtsfw OP-111
ssi OP-124
st2vfb M-870
st2vfbo M-876
sta2 M-70
sta2o M-554
stbet M-45
stbetedge M-783
stbetedgel M-839
stbetedgelw M-841
stbetedgeo M-838
stbetedgew M-840

© 2023 Cadence Design Systems, Inc.

cgovaccg M-97
cgovaccgo M-582
cgovd M-91
cgs OP-71
cgsol OP-87
chib M-80
chibo M-568
cigid OP-114
cinr M-98
cinrd M-99
cinrdw M-584
cinrw M-583
cjd OP-94
cjdbot OP-95
cjdgat OP-96
cjdsti OP-97
cjorbot M-651
cjorbotd M-692
lp_ctg OP-158
lp_cth O-84
lp_delvtac O-15
lp_dnsub O-13
lp_dphib O-14
lp_dphibedge O-88
lp_dvfbinr OP-143
lp_dvsbnud O-10
lp_ef O-75
lp_efedge O-103
lp_epsrox O-5
lp_facneffac O-7
lp_fcgovacc OP-138
lp_fcgovaccd OP-139
lp_fcinracc OP-145
lp_fcinrdep OP-144
lp_feta O-32
lp_fnt O-70
plwnfcedge M-416
plwnov M-169
plwnovd M-173
plwnp M-159
plwpsce M-364
plwpsceedge M-395
plwrs M-210
plwstbet M-188
plwstbetedge M-391
plwstthesat M-221
plwstvfb M-128
plwstvfbedge M-371
plwthesat M-217
plwthesatac M-770
plwthesatb M-225
plwthesatg M-229
plwvfb M-124
plwxcor M-204
stbetl M-500
stbetlw M-502
stbeto M-499
stbetw M-501
stbgidl M-85
stbgidld M-86
stbgidldo M-574
stbgidlo M-573
stcs M-51
stcso M-513
stct M-881
stcto M-886
stetao M-643
stfbbtbot M-683
stfbbtbotd M-724
stfbbtgat M-685
stfbbtgatd M-726
stfbbtsti M-684

© 2023 Cadence Design Systems, Inc.

cjorgat M-653
cjorgatd M-694
cjorsti M-652
cjorstid M-693
cjosbot O-104
cjosbotd O-113
cjosgat O-106
cjosgatd O-115
cjossti O-105
cjosstid O-114
cjs OP-90
cjsbot OP-91
cjsgat OP-92
cjssti OP-93
cm OP-82
cmb OP-83
cmx OP-84
co OP-81
compatible M-889
cox M-89
cs M-50
lp_fntedge O-99
lp_fntexc O-71
lp_gc2 O-53
lp_gc2ov OP-163
lp_gc3 O-54
lp_gc3ov OP-164
lp_gco O-48
lp_gfacnud O-8
lp_iginv O-49
lp_igov O-50
lp_igovd O-51
lp_mue OP-131
lp_munqs O-122
lp_neff O-6
lp_neffedge O-89
lp_nfa O-72
lp_nfaedge O-100
lp_nfb O-73
lp_nfbedge O-101
lp_nfc O-74
lp_nfcedge O-102
plxcor M-202
poa1 M-247
poa2 M-251
poa3 M-253
poa4 M-257
poagidl M-278
poagidld M-282
poalp M-234
poalp1 M-238
poalp2 M-242
poalpac M-775
poax M-230
poaxac M-771
poaxinr M-330
pobetn M-181
pobetnedge M-384
pobgidl M-286
pobgidld M-287
pocf M-174
pocfac M-763
pocfb M-180
stfbbtstid M-725
stig M-77
stigo M-565
stmue M-47
stmueo M-505
strs M-56
strso M-522
strth M-120
strtho M-625
stthecs M-872
stthecso M-878
stthemu M-49
stthemuo M-507
stthesat M-60
stthesatl M-531
stthesatlw M-533
stthesato M-530
stthesatw M-532
stvfb M-23
stvfbedge M-842
stvfbedgel M-844

© 2023 Cadence Design Systems, Inc.

csb OP-76
csd OP-73
csg OP-74
csl M-509
cslexp M-510
cslw M-512
cso M-508
csrhbot M-666
csrhbotd M-707
csrhgat M-668
csrhgatd M-709
csrhsti M-667
csrhstid M-708
css OP-75
csw M-511
ct M-37
ctatbot M-671
ctatbotd M-712
ctatgat M-673
ctatgatd M-714
lp_nov O-19
lp_novd O-20
lp_np O-16
lp_nslp O-12
lp_psce O-24
lp_psceb O-25
lp_pscebedge O-94
lp_psced O-26
lp_pscededge O-95
lp_psceedge O-93
lp_rbulk O-79
lp_rde O-78
lp_rg O-76
lp_rjund O-82
lp_rjuns O-81
lp_rs OP-135
lp_rsb O-34
lp_rse O-77
lp_rsg O-35
lp_rth O-83
pocfbedge M-403
pocfd M-179
pocfdedge M-402
pocfedge M-398
pocfr M-308
pocfrd M-312
pocgbov M-304
pocgidl M-290
pocgidld M-291
pocgov M-296
pocgovaccg M-318
pocgovd M-300
pochib M-277
pocinr M-319
pocinrd M-323
pocox M-292
pocs M-196
poct M-160
poctb M-883
poctedge M-380
stvfbedgelw M-846
stvfbedgeo M-843
stvfbedgew M-845
stvfbl M-433
stvfblw M-435
stvfbo M-432
stvfbw M-434
stxcor M-53
stxcoro M-518
swdelvtac M-13
swedge M-12
swgeo M-5
swgidl M-8
swigate M-6
swign M-14
swimpact M-7
swjunasym M-10
swjuncap M-9
swjunexp M-733
swnqs M-4

© 2023 Cadence Design Systems, Inc.

ctatsti M-672
ctatstid M-713
ctb M-880
ctbo M-885
ctedge M-795
ctedgel M-797
ctedgelexp M-798
ctedgeo M-796
ctg M-879
ctgo M-887
cth M-119
cthlw M-624
ctho M-621
cthw1 M-622
cthw2 M-623
ctl M-475
ctlexp M-476
ctlw M-478
cto M-474
lp_rwell O-80
lp_st2vfb O-131
lp_sta2 O-45
lp_stbet O-27
lp_stbetedge O-92
lp_stbgidl O-60
lp_stbgidld O-61
lp_stcs O-30
lp_stct O-134
lp_stig O-52
lp_stmue O-28
lp_strs O-33
lp_strth O-85
lp_stthecs O-132
lp_stthemu O-29
lp_stthesat O-36
lp_stvfb O-3
lp_stvfbedge O-87
lp_stxcor O-31
poctg M-882
podelvtac M-152
podnsub M-147
podphib M-148
podphibedge M-372
podvfbinr M-327
podvsbnud M-144
poef M-348
poefedge M-417
poepsrox M-130
pofacneffac M-135
pofcgovacc M-316
pofcgovaccd M-317
pofcinracc M-329
pofcinrdep M-328
pofeta M-206
pofnt M-331
pofntedge M-404
pofntexc M-332
swnud M-11
swqpart M-741
swqsat M-740
tau1 OP-85
tempeff O-129
thecs M-871
thecso M-877
themu M-48
themuo M-506
thesat M-59
thesatac M-743
thesatacl M-752
thesataclexp M-753
thesataclw M-755
thesataco M-751
thesatacw M-754
thesatb M-61
thesatbo M-534
thesatg M-62

© 2023 Cadence Design Systems, Inc.

ctw M-477
ctype OP-2
delvtac M-35
delvtacl M-468
delvtaclexp M-469
delvtaclw M-471
delvtaco M-467
delvtacw M-470
delvto I-18
delvtoedge I-20
dlq M-426
dlsil M-610
dnsub M-33
dnsubo M-461
dphib M-34
dphibedge M-799
dphibedgel M-801
dphibedgelexp M-802
dphibedgelw M-804
lp_thecs OP-157
lp_themu OP-132
lp_thesat OP-136
lp_thesatac OP-160
lp_thesatb O-37
lp_thesatg O-38
lp_tox O-4
lp_toxov O-17
lp_toxovd O-18
lp_vfb OP-128
lp_vfbedge O-86
lp_vnsub O-11
lp_vp O-43
lp_vsbnud O-9
lp_xcor OP-134
lpck M-444
lpckw M-445
lpedge M-810
lpoly OP-98
pogc2 M-275
pogc2ov M-779
pogc3 M-276
pogc3ov M-780
pogco M-261
pogfacnud M-139
poiginv M-262
poigov M-266
poigovd M-270
pokuowe M-353
pokvthowe M-349
pomue M-189
poneff M-131
poneffedge M-376
ponfa M-336
ponfaedge M-405
ponfb M-340
ponfbedge M-409
ponfc M-344
thesatgo M-535
thesatl M-526
thesatlexp M-527
thesatlw M-529
thesato M-525
thesatw M-528
tk OP-149
tkuo M-631
tox M-24
toxo M-436
toxov M-38
toxovd M-39
toxovdo M-480
toxovo M-479
tr M-3
trise I-16
trj M-649
type M-2
u OP-99

© 2023 Cadence Design Systems, Inc.

dphibedgeo M-800
dphibedgew M-803
dphibl M-463
dphiblexp M-464
dphiblw M-466
dphibo M-462
dphibw M-465
dta M-738
dtsh OP-148
dvfbinr M-100
dvfbinro M-585
dvsbnud M-30
dvsbnudo M-458
dwq M-427
ef M-109
efedge M-805
efedgeo M-806
efo M-594
epsrox M-25
epsroxo M-437
lsdrain I-26
lssource I-23
lv1 O-124
lv11 O-127
lv12 O-128
lv13 OP-151
lv14 OP-152
lv2 O-123
lv3 O-125
lv36 OP-153
lv37 OP-154
lv38 OP-155
lv4 O-126
lv51 OP-156
lvarl M-419
lvaro M-418
lvarw M-420
m I-34
mbe M-20
mbeo M-21
ponfcedge M-413
ponov M-166
ponovd M-170
ponp M-156
ponslp M-146
popsce M-361
popsceb M-365
popscebedge M-396
popsced M-366
popscededge M-397
popsceedge M-392
pors M-207
porsb M-212
porsg M-213
post2vfb M-873
posta2 M-252
postbet M-185
postbetedge M-388
postbgidl M-288
postbgidld M-289
uo M-489
vbd_max M-857
vbdr_max M-864
vbirbot M-654
vbirbotd M-695
vbirgat M-656
vbirgatd M-697
vbirsti M-655
vbirstid M-696
vbisbot O-107
vbisbotd O-116
vbisgat O-109
vbisgatd O-118
vbissti O-108
vbisstid O-117
vbrbot M-686
vbrbotd M-727
vbrgat M-688
vbrgatd M-729
vbrsti M-687

© 2023 Cadence Design Systems, Inc.

facneffac M-27
facneffacl M-449
facneffaclw M-451
facneffaco M-448
facneffacw M-450
factuo I-19
factuoedge I-21
fbbtrbot M-680
fbbtrbotd M-721
fbbtrgat M-682
fbbtrgatd M-723
fbbtrsti M-681
fbbtrstid M-722
fbet1 M-490
fbet1w M-491
fbet2 M-494
fbetedge M-807
fcgovacc M-95
fcgovaccd M-96
meff O-130
mefftatbot M-674
mefftatbotd M-715
mefftatgat M-676
mefftatgatd M-717
mefftatsti M-675
mefftatstid M-716
minr M-17
mue M-46
mueo M-503
muew M-504
mulid0 I-33
mult I-32
munqs M-110
munqso M-605
mvt M-18
mvto M-19
neff M-26
neffedge M-811
postcs M-200
postct M-884
postig M-274
postmue M-193
postrs M-211
postthecs M-875
postthemu M-195
postthesat M-218
postvfb M-125
postvfbedge M-368
postxcor M-205
pothecs M-874
pothemu M-194
pothesat M-214
pothesatac M-767
pothesatb M-222
pothesatg M-226
potox M-129
potoxov M-164
vbrstid M-728
vbs OP-150
vbs_max M-858
vbsr_max M-863
vdb OP-47
vds OP-43
vds_max M-854
vdsat OP-55
vdsat_marg OP-57
vdss OP-54
vearly OP-102
version M-16
vfb M-22
vfbedge M-847
vfbedgeo M-848
vfbl M-429
vfblw M-431
vfbo M-428
vfbw M-430

© 2023 Cadence Design Systems, Inc.

fcgovaccdo M-581
fcgovacco M-580
fcinracc M-102
fcinracco M-587
fcinrdep M-101
fcinrdepo M-586
feta M-54
fetao M-519
fjunq M-735
fjunqd M-737
fknee OP-120
fnt M-104
fntedge M-808
fntedgeo M-809
fntexc M-105
fntexcl M-590
fnto M-589
fol1 M-446
fol2 M-447
fqslim OP-86
nf I-10
nf M-853
nfa M-106
nfaedge M-812
nfaedgelw M-813
nfalw M-591
nfb M-107
nfbedge M-814
nfbedgelw M-815
nfblw M-592
nfc M-108
nfcedge M-816
nfcedgelw M-817
nfclw M-593
ngcon I-11
noi_cgeff OP-118
noi_cigid OP-119
noi_mid OP-115
noi_mig OP-116
noi_migid OP-117
potoxovd M-165
povfb M-121
povfbedge M-367
povnsub M-145
povp M-246
povsbnud M-143
poxcor M-201
ps I-29
psce M-822
psceb M-823
pscebedge M-824
pscebedgeo M-825
pscebo M-826
psced M-827
pscededge M-828
pscededgeo M-830
pscedo M-829
psceedge M-831
psceedgel M-832
psceedgelexp M-833
vgb_max M-859
vgbr_max M-862
vgd OP-45
vgd_max M-855
vgdr_max M-860
vgs OP-44
vgs_max M-856
vgsr_max M-861
vgt OP-52
vjunref M-734
vjunrefd M-736
vnsub M-31
vnsubo M-459
vp M-67
vpo M-549
vsat OP-56
vsb OP-46
vsbnud M-29
vsbnudo M-457
vth OP-51

© 2023 Cadence Design Systems, Inc.

frev M-650
ft OP-106
fug OP-105
gc2 M-78
gc2o M-566
gc2ov M-746
gc2ovo M-761
gc3 M-79
gc3o M-567
gc3ov M-747
gc3ovo M-762
gco M-73
gcoo M-561
gds OP-62
gfacnud M-28
gfacnudl M-453
gfacnudlexp M-454
gfacnudlw M-456
gfacnudo M-452
gfacnudw M-455
noisemethod M-739
nov M-40
novd M-41
novdo M-484
novo M-483
np M-36
npck M-441
npckw M-442
npl M-473
npo M-472
nrd I-14
nrs I-13
nslp M-32
nslpo M-460
nsubedgel M-818
nsubedgelexp M-888
nsubedgelw M-820
nsubedgeo M-821
nsubedgew M-819
nsubo M-438
psceedgew M-834
pscel M-835
pscelexp M-836
pscew M-837
psti M-658
pstid M-699
pwa1 M-249
pwa3 M-255
pwa4 M-259
pwagidl M-280
pwagidld M-284
pwalp M-236
pwalp1 M-240
pwalp2 M-244
pwalpac M-777
pwax M-232
pwaxac M-773
pwbetn M-183
pwbetnedge M-386
pwcf M-176
vth0 OP-48
vth_drive OP-53
vthmod M-865
vto OP-49
vts OP-50
w I-2
w M-851
wbet M-498
web M-646
wec M-647
wedge M-849
wedgew M-850
weff O-1
wkuo M-633
wkvtho M-639
wlod M-628
wlodkuo M-636
wlodvth M-642
wmax M-360
wmin M-359

© 2023 Cadence Design Systems, Inc.

gjd OP-64
gjs OP-63
gm OP-59
gmb OP-60
go OP-61
iavl OP-21
ib OP-11
ibe OP-7
id OP-10
idb OP-13
ide OP-6
idedge OP-18
ids OP-12
idsatrbot M-663
idsatrbotd M-704
idsatrgat M-665
idsatrgatd M-706
idsatrsti M-664
nsubw M-439
pbot M-657
pbotd M-698
pbrbot M-689
pbrbotd M-730
pbrgat M-691
pbrgatd M-732
pbrsti M-690
pbrstid M-731
pd I-31
pdiss OP-147
pgat M-659
pgatd M-700
phigbot M-660
phigbotd M-701
phiggat M-662
phiggatd M-703
phigsti M-661
pwcfac M-765
pwcfedge M-400
pwcfr M-310
pwcfrd M-314
pwcgbov M-306
pwcgov M-298
pwcgovd M-302
pwcinr M-321
pwcinrd M-325
pwcox M-294
pwcs M-198
pwct M-162
pwctedge M-382
pwdelvtac M-154
pwdphib M-150
pwdphibedge M-374
pwfacneffac M-137
pwfntexc M-334
wot M-425
wseg M-440
wsegp M-443
wvarl M-423
wvaro M-422
wvarw M-424
xcor M-52
xcorl M-515
xcorlw M-517
xcoro M-514
xcorw M-516
xgw I-12
xjungat M-670
xjungatd M-711
xjunsti M-669
xjunstid M-710

© 2023 Cadence Design Systems, Inc.

PSP NQS MOSFET Model (pspnqs103)

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
Component Sta
```

Instance Parameters

1	`l=10e-6 m`	Design length.
2	`w=10e-6 m`	Design width.
3	`sa=0.0 m`	Distance between OD-edge and poly from one side.
4	`sb=0.0 m`	Distance between OD-edge and poly from other side.
5	`sd=0.0 m`	Distance between neighboring fingers.
6	`sca=0.0`	Integral of the first distribution function for scattered well dopants.
7	`scb=0.0`	Integral of the second distribution function for scattered well dopants.
8	`scc=0.0`	Integral of the third distribution function for scattered well dopants.
9	`sc=0.0 m`	Distance between OD-edge and nearest well edge.
10	`nf=1`	Number of fingers.
11	`ngcon=1.0`	Number of gate contacts.
12	`xgw=1.0E-7 m`	Distance from the gate contact to the channel edge.
13	`nrs=0.0`	Number of squares of source diffusion.
14	`nrd=0.0`	Number of squares of drain diffusion.
15	`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
16	`trise=0.0 K`	Temperature rise from ambient.
17	`dtemp=0.0 K`	Temperature rise from ambient.
18	`jw=1E-6 m`	Gate-edge length of source/drain junction.

© 2023 Cadence Design Systems, Inc.

19	`delvto=0.0 V`	Threshold voltage shift parameter.
20	`factuo=1.0`	Zero-field mobility pre-factor.
21	`delvtoedge=0.0 V`	Threshold voltage shift parameter of edge transistor.
22	`factuoedge=1.0`	Zero-field mobility pre-factor of edge transistor.
23	`absource=1E-12` m^2	Bottom area of source junction.
24	`lssource=1E-6 m`	STI-edge length of source junction.
25	`lgsource=1E-6 m`	Gate-edge length of source junction.
26	`abdrain=1E-12` m^2	Bottom area of drain junction.
27	`lsdrain=1E-6 m`	STI-edge length of drain junction.
28	`lgdrain=1E-6 m`	Gate-edge length of drain junction.
29	`as=1E-12` m^2	Bottom area of source junction.
30	`ps=1E-6 m`	Perimeter of source junction.
31	`ad=1E-12` m^2	Bottom area of drain junction.
32	`pd=1E-6 m`	Perimeter of drain junction.
33	`mult=1.0`	Number of devices in parallel.
34	`mulid0=1`	Ids multiplier.
35	`m=1.0`	Multiplicity factor.
36	`ifactor=1.0`	Multiplier for current.
37	`cfactor=1.0`	Multiplier for depletion capacitance.
38	`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Definition

```
model modelName pspnqs103 parameter=value ...
```

Model Parameters

1	`level=103`	Model level.

© 2023 Cadence Design Systems, Inc.

2	`type=n`	Channel type parameter, n=NMOS p=PMOS. Possible values are `n` and `p`.
3	`tr=value of tnom C`	Nominal (reference) temperature.
4	`tref=value of tnom C`	Nominal (reference) temperature.
5	`swnqs=0`	Flag for NQS, 0, off, 1, 2, 3, 5, or 9, number of collocation points.
6	`swgeo=1`	Flag for geometrical model, 0: local, 1: global, 2: binning.
7	`swigate=0`	Flag for gate current, 0,turn off IG.
8	`swimpact=0`	Flag for impact ionization current, 0,turn off II.
9	`swgidl=0`	Flag for GIDL current, 0,turn off IGIDL.
10	`swjuncap=0`	Flag for juncap, 0,turn off juncap.
11	`swjunasym=0`	Flag for asymmetric junctions; 0,symmetric, 1,asymmetric.
12	`swnud=0`	Flag for NUD-effect. Possible values are: `0`: off `1`: on `2`: on+CV-correction.
13	`swedge=0.0`	Flag for drain current of edge transistors. Possible values are `0=off` and `1=on`.
14	`swdelvtac=0`	Flag for separate capacitance calculation. Possible values are `0`: off and `1`: on.
15	`swign=1.0`	Flag for induced gate noise. Possible values are `0`: off and `1`: on.
16	`swfix=0`	Flag for fixes introduced in PSP103.8.2.
17	`qmc=1.0`	Quantum-mechanical correction factor.
18	`version=103.0`	This parameter accepts only a real number values, for example, use 103.11 for the 103.1.1 version. The available versions are 103.0, 103.1, 103.11 (103.1.1), 103.2, 103.3, 103.4, 103.5, 103.6, and 103.7.

© 2023 Cadence Design Systems, Inc.

19	`minr=0.0`	Minimum resistance, in order to be compatible with the original model, set its default to 0.0.
20	`mvt=0.0`	DCmatch parameter.
21	`mvto=0.0`	DCmatch parameter.
22	`mbe=0.0`	DCmatch parameter.
23	`mbeo=0.0`	DCmatch parameter.
24	`vfb=-1.0 V`	Flat band voltage at TR.
25	`stvfb=5.0e-4 V/K`	Temperature dependence of VFB.
26	`tox=2.0e-09 m`	Gate oxide thickness.
27	`epsrox=3.9`	Relative permittivity of gate dielectric.
28	`neff=5.0e+23` m^{-3}	Effective substrate doping.
29	`facneffac=1.0`	Pre-factor for effective substrate doping in separate charge calculation.
30	`gfacnud=1.0`	Bodyfactor change due to NUD-effect.
31	`vsbnud=0.0 V`	Lower Vsb value for NUD-effect.
32	`dvsbnud=1.0 V`	Vsb-range for NUD-effect.
33	`vnsub=0.0 V`	Effective doping bias-dependence parameter.
34	`nslp=0.05 V`	Effective doping bias-dependence parameter.
35	`dnsub=0.0 V^-1`	Effective doping bias-dependence parameter.
36	`dphib=0.0 V`	Offset parameter for PHIB.
37	`delvtac=0.0 V`	Offset parameter for PHIB in separate charge calculation.
38	`np=1.0e+26` m^{-3}	Gate poly-silicon doping.
39	`ct=0.0`	Interface states factor.
40	`toxov=2.0e-09 m`	Overlap oxide thickness.
41	`toxovd=2.0e-09 m`	Overlap oxide thickness for drain side.
42	`nov=5.0e+25` m^{-3}	Effective doping of overlap region.
43	`novd=5.0e+25` m^{-3}	Effective doping of overlap region for drain side.
44	`cf=0.0`	DIBL parameter.
45	`cfb=0.0 V^-1`	Back bias dependence of CF.

© 2023 Cadence Design Systems, Inc.

46	betn=7e-2 m^2/V/s	Channel aspect ratio times zero-field mobility.
47	stbet=1.0	Temperature dependence of BETN.
48	mue=0.5 m/V	Mobility reduction coefficient at TR.
49	stmue=0.0	Temperature dependence of MUE.
50	themu=1.5	Mobility reduction exponent at TR.
51	stthemu=1.5	Temperature dependence of THEMU.
52	cs=0.0	Coulomb scattering parameter at TR.
53	stcs=0.0	Temperature dependence of CS.
54	xcor=0.0 V^-1	Non-universality factor.
55	stxcor=0.0	Temperature dependence of XCOR.
56	feta=1.0	Effective field parameter.
57	rs=30 Ω	Series resistance at TR.
58	strs=1.0	Temperature dependence of RS.
59	rsb=0.0 V^-1	Back-bias dependence of series resistance.
60	rsg=0.0 V^-1	Gate-bias dependence of series resistance.
61	thesat=1.0 V^-1	Velocity saturation parameter at TR.
62	stthesat=1.0	Temperature dependence of THESAT.
63	thesatb=0.0 V^-1	Back-bias dependence of velocity saturation.
64	thesatg=0.0 V^-1	Gate-bias dependence of velocity saturation.
65	ax=3.0	Linear/saturation transition factor.
66	alp=0.01	CLM pre-factor.
67	alp1=0.00 V	CLM enhancement factor above threshold.
68	alp2=0.00 V^-1	CLM enhancement factor below threshold.
69	vp=0.05 V	CLM logarithm dependence factor.
70	a1=1.0	Impact-ionization pre-factor.
71	a2=10.0 V	Impact-ionization exponent at TR.
72	sta2=0.0 V	Temperature dependence of A2.
73	a3=1.0	Saturation-voltage dependence of impact-ionization.
74	a4=0.0 V^-0.5	Back-bias dependence of impact-ionization.

© 2023 Cadence Design Systems, Inc.

75	`gco=0.0`	Gate tunneling energy adjustment.
76	`iginv=0.0 A`	Gate channel current pre-factor.
77	`igov=0.0 A`	Gate overlap current pre-factor.
78	`igovd=0.0 A`	Gate overlap current pre-factor for drain side.
79	`stig=2.0`	Temperature dependence of IGINV and IGOV.
80	`gc2=0.375`	Gate current slope factor.
81	`gc3=0.063`	Gate current curvature factor.
82	`chib=3.1 V`	Tunneling barrier height.
83	`agidl=0.0 A/V`^{3}	GIDL pre-factor.
84	`agidld=0.0 A/V`^{3}	GIDL pre-factor for drain side.
85	`bgidl=41.0 V`	GIDL probability factor at TR.
86	`bgidld=41.0 V`	GIDL probability factor at TR for drain side.
87	`stbgidl=0.0 V/K`	Temperature dependence of BGIDL.
88	`stbgidld=0.0 V/K`	Temperature dependence of BGIDL for drain side.
89	`cgidl=0.0`	Back-bias dependence of GIDL.
90	`cgidld=0.0`	Back-bias dependence of GIDL for drain side.
91	`cox=1.0e-14 F`	Oxide capacitance for intrinsic channel.
92	`cgov=1.0e-15 F`	Oxide capacitance for gate-drain/source overlap.
93	`cgovd=1.0e-15 F`	Oxide capacitance for gate-drain overlap.
94	`cgbov=0.0 F`	Oxide capacitance for gate-bulk overlap.
95	`cfr=0.0 F`	Outer fringe capacitance.
96	`cfrd=0.0 F`	Outer fringe capacitance for drain side.
97	`fcgovacc=0.0`	Factor for overlap capacitances in accumulation regime.
98	`fcgovaccd=0.0`	Factor for overlap capacitances in accumulation regime for drain side.
99	`cgovaccg=1.0`	Gate voltage dependence parameter of overlap capacitances in accumulation regime.
100	`cinr=0.0 F`	Inner fringe capacitance.
101	`cinrd=0.0 F`	Inner fringe capacitance for drain side.

© 2023 Cadence Design Systems, Inc.

102	`dvfbinr=0.0 V`	Flat-band voltage offset of inner fringe capacitances.
103	`fcinrdep=0.3`	Bias dependence parameter of inner fringe capacitances in depletion regime.
104	`fcinracc=0.5`	Bias dependence parameter of inner fringe capacitances in accumulation regime.
105	`axinr=0.5`	Accumulation/depletion transition factor of inner fringe capacitances.
106	`fnt=1.0`	Thermal noise coefficient.
107	`FNTEXC=0.0`	Excess noise coefficient.
108	`nfa=8.0e+22 V^-1/m`^{4}	First coefficient of flicker noise.
109	`nfb=3.0e+07 V^-1/m`^{2}	Second coefficient of flicker noise.
110	`nfc=0.0 V^-1`	Third coefficient of flicker noise.
111	`ef=1.0`	Flicker noise frequency exponent.
112	`munqs=1.0`	Relative mobility for NQS modelling.
113	`rg=0.0 Ω`	Gate resistance.
114	`rse=0.0 Ω`	External source resistance.
115	`rde=0.0 Ω`	External drain resistance.
116	`rbulk=0.0 Ω`	Bulk resistance between node BP and BI.
117	`rwell=0.0 Ω`	Well resistance between node BI and B.
118	`rjuns=0.0 Ω`	Source-side bulk resistance between node BI and BS.
119	`rjund=0.0 Ω`	Drain-side bulk resistance between node BI and BD.
120	`rth=0.0 K/W`	Thermal resistance.
121	`cth=0.0 J/K`	Thermal capacitance.
122	`strth=0.0`	Temperature sensitivity of RTH.
123	`povfb=-1 V`	Coefficient for the geometry-independent part of VFB.
124	`plvfb=0.0 V`	Coefficient for the length dependence of VFB.
125	`pwvfb=0.0 V`	Coefficient for the width dependence of VFB.

© 2023 Cadence Design Systems, Inc.

126	`plwvfb=0.0 V`	Coefficient for the length times width dependence of VFB.
127	`postvfb=0.0005 V/K`	Coefficient for the geometry-independent part of STVFB.
128	`plstvfb=0.0 V/K`	Coefficient for the length dependence of STVFB.
129	`pwstvfb=0.0 V/K`	Coefficient for the width dependence of STVFB.
130	`plwstvfb=0.0 V/K`	Coefficient for the length times width dependence of STVFB.
131	`potox=2E-09 m`	Coefficient for the geometry-independent part of TOX.
132	`poepsrox=3.9`	Coefficient for the geometry-independent part of EPSOX.
133	`poneff=5E+23` m^{-3}	Coefficient for the geometry-independent part of NEFF.
134	`plneff=0.0` m^{-3}	Coefficient for the length dependence of NEFF.
135	`pwneff=0.0` m^{-3}	Coefficient for the width dependence of NEFF.
136	`plwneff=0.0` m^{-3}	Coefficient for the length times width dependence of NEFF.
137	`pofacneffac=1.0`	Coefficient for the geometry-independent part of FACNEFFAC.
138	`plfacneffac=0.0`	Coefficient for the length dependence of FACNEFFAC.
139	`pwfacneffac=0.0`	Coefficient for the width dependence of FACNEFFAC.
140	`plwfacneffac=0.0`	Coefficient for the length times width dependence of FACNEFFAC.
141	`pogfacnud=1.0`	Coefficient for the geometry-independent part of GFACNUD.
142	`plgfacnud=0.0`	Coefficient for the length dependence of GFACNUD.
143	`pwgfacnud=0.0`	Coefficient for the width dependence of GFACNUD.
144	`plwgfacnud=0.0`	Coefficient for the length times width dependence of GFACNUD.
145	`povsbnud=0.0 V`	Coefficient for the geometry-independent part of VSBNUD.

© 2023 Cadence Design Systems, Inc.

146	`podvsbnud=1.0 V`	Coefficient for the geometry-independent part of DVSBNUD.
147	`povnsub=0 V`	Coefficient for the geometry-independent part of VNSUB.
148	`ponslp=0.05 V`	Coefficient for the geometry-independent part of NSLP.
149	`podnsub=0 V^-1`	Coefficient for the geometry-independent part of DNSUB.
150	`podphib=0 V`	Coefficient for the geometry-independent part of DPHIB.
151	`pldphib=0.0 V`	Coefficient for the length dependence of DPHIB.
152	`pwdphib=0.0 V`	Coefficient for the width dependence of DPHIB.
153	`plwdphib=0.0 V`	Coefficient for the length times width dependence of DPHIB.
154	`podelvtac=0 V`	Coefficient for the geometry-independent part of DELVTAC.
155	`pldelvtac=0.0 V`	Coefficient for the length dependence of DELVTAC.
156	`pwdelvtac=0.0 V`	Coefficient for the width dependence of DELVTAC.
157	`plwdelvtac=0.0 V`	Coefficient for the length times width dependence of DELVTAC.
158	`ponp=1E+26 m^-3`	Coefficient for the geometry-independent part of NP.
159	`plnp=0.0 m^-3`	Coefficient for the length dependence of NP.
160	`pwnp=0.0 m^-3`	Coefficient for the width dependence of NP.
161	`plwnp=0.0 m^-3`	Coefficient for the length times width dependence of NP.
162	`poct=0`	Coefficient for the geometry-independent part of CT.
163	`plct=0.0`	Coefficient for the length dependence of CT.
164	`pwct=0.0`	Coefficient for the width dependence of CT.
165	`plwct=0.0`	Coefficient for the length times width dependence of CT.
166	`potoxov=2E-09 m`	Coefficient for the geometry-independent part of TOXOV.

© 2023 Cadence Design Systems, Inc.

167	potoxovd=2E-09 m	Coefficient for the geometry-independent part of TOXOV for drain side.
168	ponov=5E+25 m^{-3}	Coefficient for the geometry-independent part of NOV.
169	plnov=0.0 m^{-3}	Coefficient for the length dependence of NOV.
170	pwnov=0.0 m^{-3}	Coefficient for the width dependence of NOV.
171	plwnov=0.0 m^{-3}	Coefficient for the length times width dependence of NOV.
172	ponovd=5E+25 m^{-3}	Coefficient for the geometry-independent part of NOV for drain side.
173	plnovd=0.0 m^{-3}	Coefficient for the length dependence of NOV for drain side.
174	pwnovd=0.0 m^{-3}	Coefficient for the width dependence of NOV for drain side.
175	plwnovd=0.0 m^{-3}	Coefficient for the length times width dependence of NOV for drain side.
176	pocf=0	Coefficient for the geometry-independent part of CF.
177	plcf=0.0	Coefficient for the length dependence of CF.
178	pwcf=0.0	Coefficient for the width dependence of CF.
179	plwcf=0.0	Coefficient for the length times width dependence of CF.
180	plcfd=0.0 V^-1	Coefficient for the geometry-independent part of CFD.
181	pocfd=0 V^-1	Coefficient for the geometry-independent part of CFD.
182	pocfb=0 V^-1	Coefficient for the geometry-independent part of CFB.
183	pobetn=0.07 m^2/V/s	Coefficient for the geometry-independent part of BETN.
184	plbetn=0.0 m^2/V/s	Coefficient for the length dependence of BETN.
185	pwbetn=0.0 m^2/V/s	Coefficient for the width dependence of BETN.
186	plwbetn=0.0 m^2/V/s	

© 2023 Cadence Design Systems, Inc.

		Coefficient for the length times width dependence of BETN.
187	`postbet=1`	Coefficient for the geometry-independent part of STBET.
188	`plstbet=0.0`	Coefficient for the length dependence of STBET.
189	`pwstbet=0.0`	Coefficient for the width dependence of STBET.
190	`plwstbet=0.0`	Coefficient for the length times width dependence of STBET.
191	`pomue=0.5 m/V`	Coefficient for the geometry-independent part of MUE.
192	`plmue=0.0 m/V`	Coefficient for the length dependence of MUE.
193	`pwmue=0.0 m/V`	Coefficient for the width dependence of MUE.
194	`plwmue=0.0 m/V`	Coefficient for the length times width dependence of MUE.
195	`postmue=0`	Coefficient for the geometry-independent part of STMUE.
196	`pothemu=1.5`	Coefficient for the geometry-independent part of THEMU.
197	`postthemu=1.5`	Coefficient for the geometry-independent part of STTHEMU.
198	`pocs=0`	Coefficient for the geometry-independent part of CS.
199	`plcs=0.0`	Coefficient for the length dependence of CS.
200	`pwcs=0.0`	Coefficient for the width dependence of CS.
201	`plwcs=0.0`	Coefficient for the length times width dependence of CS.
202	`postcs=0`	Coefficient for the geometry-independent part of STCS.
203	`poxcor=0 V^-1`	Coefficient for the geometry-independent part of XCOR.
204	`plxcor=0.0 V^-1`	Coefficient for the length dependence of XCOR.
205	`pwxcor=0.0 V^-1`	Coefficient for the width dependence of XCOR.
206	`plwxcor=0.0 V^-1`	Coefficient for the length times width dependence of XCOR.

© 2023 Cadence Design Systems, Inc.

207	`postxcor=0`	Coefficient for the geometry-independent part of STXCOR.
208	`pofeta=1`	Coefficient for the geometry-independent part of FETA.
209	`pors=30 Ω`	Coefficient for the geometry-independent part of RS.
210	`plrs=0.0 Ω`	Coefficient for the length dependence of RS.
211	`pwrs=0.0 Ω`	Coefficient for the width dependence of RS.
212	`plwrs=0.0 Ω`	Coefficient for the length times width dependence of RS.
213	`postrs=1`	Coefficient for the geometry-independent part of STRS.
214	`porsb=0 V^-1`	Coefficient for the geometry-independent part of RSB.
215	`porsg=0 V^-1`	Coefficient for the geometry-independent part of RSG.
216	`pothesat=1 V^-1`	Coefficient for the geometry-independent part of THESAT.
217	`plthesat=0.0 V^-1`	Coefficient for the length dependence of THESAT.
218	`pwthesat=0.0 V^-1`	Coefficient for the width dependence of THESAT.
219	`plwthesat=0.0 V^-1`	Coefficient for the length times width dependence of THESAT.
220	`postthesat=1`	Coefficient for the geometry-independent part of STTHESAT.
221	`plstthesat=0.0`	Coefficient for the length dependence of STTHESAT.
222	`pwstthesat=0.0`	Coefficient for the width dependence of STTHESAT.
223	`plwstthesat=0.0`	Coefficient for the length times width dependence of STTHESAT.
224	`pothesatb=0 V^-1`	Coefficient for the geometry-independent part of THESATB.
225	`plthesatb=0.0 V^-1`	Coefficient for the length dependence of THESATB.
226	`pwthesatb=0.0 V^-1`	Coefficient for the width dependence of THESATB.

© 2023 Cadence Design Systems, Inc.

227	`plwthesatb=0.0 V^-1`	Coefficient for the length times width dependence of THESATB.
228	`pothesatg=0 V^-1`	Coefficient for the geometry-independent part of THESATG.
229	`plthesatg=0.0 V^-1`	Coefficient for the length dependence of THESATG.
230	`pwthesatg=0.0 V^-1`	Coefficient for the width dependence of THESATG.
231	`plwthesatg=0.0 V^-1`	Coefficient for the length times width dependence of THESATG.
232	`poax=3`	Coefficient for the geometry-independent part of AX.
233	`plax=0.0`	Coefficient for the length dependence of AX.
234	`pwax=0.0`	Coefficient for the width dependence of AX.
235	`plwax=0.0`	Coefficient for the length times width dependence of AX.
236	`poalp=0.01`	Coefficient for the geometry-independent part of ALP.
237	`plalp=0.0`	Coefficient for the length dependence of ALP.
238	`pwalp=0.0`	Coefficient for the width dependence of ALP.
239	`plwalp=0.0`	Coefficient for the length times width dependence of ALP.
240	`poalp1=0 V`	Coefficient for the geometry-independent part of ALP1.
241	`plalp1=0.0 V`	Coefficient for the length dependence of ALP1.
242	7 `pwalp1=0.0 V`	Coefficient for the width dependence of ALP1.
243	`plwalp1=0.0 V`	Coefficient for the length times width dependence of ALP1.
244	`poalp2=0 V^-1`	Coefficient for the geometry-independent part of ALP2.
245	`plalp2=0.0 V^-1`	Coefficient for the length dependence of ALP2.
246	`pwalp2=0.0 V^-1`	Coefficient for the width dependence of ALP2.

© 2023 Cadence Design Systems, Inc.

247	`plwalp2=0.0 V^-1`	Coefficient for the length times width dependence of ALP2.
248	`povp=0.05 V`	Coefficient for the geometry-independent part of VP.
249	`poa1=1`	Coefficient for the geometry-independent part of A1.
250	`pla1=0.0`	Coefficient for the length dependence of A1.
251	`pwa1=0.0`	Coefficient for the width dependence of A1.
252	`plwa1=0.0`	Coefficient for the length times width dependence of A1.
253	`poa2=10 V`	Coefficient for the geometry-independent part of A2.
254	`posta2=0 V`	Coefficient for the geometry-independent part of STA2.
255	`poa3=1`	Coefficient for the geometry-independent part of A3.
256	`pla3=0.0`	Coefficient for the length dependence of A3.
257	`pwa3=0.0`	Coefficient for the width dependence of A3.
258	`plwa3=0.0`	Coefficient for the length times width dependence of A3.
259	`poa4=0 V^-0.5`	Coefficient for the geometry-independent part of A4.
260	`pla4=0.0 V^-0.5`	Coefficient for the length dependence of A4.
261	`pwa4=0.0 V^-0.5`	Coefficient for the width dependence of A4.
262	`plwa4=0.0 V^-0.5`	Coefficient for the length times width dependence of A4.
263	`pogco=0`	Coefficient for the geometry-independent part of GCO.
264	`poiginv=0 A`	Coefficient for the geometry-independent part of IGINV.
265	`pliginv=0.0 A`	Coefficient for the length dependence of IGINV.
266	`pwiginv=0.0 A`	Coefficient for the width dependence of IGINV.
267	`plwiginv=0.0 A`	Coefficient for the length times width dependence of IGINV.
268	`poigov=0 A`	Coefficient for the geometry-independent part of IGOV.
269	`pligov=0.0 A`	Coefficient for the length dependence of IGOV.
270	`pwigov=0.0 A`	Coefficient for the width dependence of IGOV.
271	`plwigov=0.0 A`	Coefficient for the length times width dependence of IGOV.

© 2023 Cadence Design Systems, Inc.

272	`poigovd=0 A`	Coefficient for the geometry-independent part of IGOV for drain side.
273	`pligovd=0.0 A`	Coefficient for the length dependence of IGOV for drain side.
274	`pwigovd=0.0 A`	Coefficient for the width dependence of IGOV for drain side.
275	`plwigovd=0.0 A`	Coefficient for the length times width dependence of IGOV for drain side.
276	`postig=2`	Coefficient for the geometry-independent part of STIG.
277	`pogc2=0.375`	Coefficient for the geometry-independent part of GC2.
278	`pogc3=0.063`	Coefficient for the geometry-independent part of GC3.
279	`pochib=3.1 V`	Coefficient for the geometry-independent part of CHIB.
280	`poagidl=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL.
281	`plagidl=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL.
282	`pwagidl=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL.
283	`plwagidl=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL.
284	`poagidld=0 A/V`^{3}	Coefficient for the geometry-independent part of AGIDL for drain side.
285	`plagidld=0.0 A/V`^{3}	Coefficient for the length dependence of AGIDL for drain side.
286	`pwagidld=0.0 A/V`^{3}	Coefficient for the width dependence of AGIDL for drain side.
287	`plwagidld=0.0 A/V`^{3}	Coefficient for the length times width dependence of AGIDL for drain side.
288	`pobgidl=41 V`	Coefficient for the geometry-independent part of BGIDL.

© 2023 Cadence Design Systems, Inc.

289	`pobgidld=41 V`	Coefficient for the geometry-independent part of BGIDL for drain side.
290	`postbgidl=0 V/K`	Coefficient for the geometry-independent part of STBGIDL.
291	`postbgidld=0 V/K`	Coefficient for the geometry-independent part of STBGIDL for drain side.
292	`pocgidl=0`	Coefficient for the geometry-independent part of CGIDL.
293	`pocgidld=0`	Coefficient for the geometry-independent part of CGIDL for drain side.
294	`pocox=1E-14 F`	Coefficient for the geometry-independent part of COX.
295	`plcox=0.0 F`	Coefficient for the length dependence of COX.
296	`pwcox=0.0 F`	Coefficient for the width dependence of COX.
297	`plwcox=0.0 F`	Coefficient for the length times width dependence of COX.
298	`pocgov=1E-15 F`	Coefficient for the geometry-independent part of CGOV.
299	`plcgov=0.0 F`	Coefficient for the length dependence of CGOV.
300	`pwcgov=0.0 F`	Coefficient for the width dependence of CGOV.
301	`plwcgov=0.0 F`	Coefficient for the length times width dependence of CGOV.
302	`pocgovd=1E-15 F`	Coefficient for the geometry-independent part of CGOV for drain side.
303	`plcgovd=0.0 F`	Coefficient for the length dependence of CGOV for drain side.
304	`pwcgovd=0.0 F`	Coefficient for the width dependence of CGOV for drain side.
305	`plwcgovd=0.0 F`	Coefficient for the length times width dependence of CGOV for drain side.
306	`pocgbov=0 F`	Coefficient for the geometry-independent part of CGBOV.
307	`plcgbov=0.0 F`	Coefficient for the length dependence of CGBOV.
308	`pwcgbov=0.0 F`	Coefficient for the width dependence of CGBOV.

© 2023 Cadence Design Systems, Inc.

309	`plwcgbov=0.0 F`	Coefficient for the length times width dependence of CGBOV.
310	`pocfr=0 F`	Coefficient for the geometry-independent part of CFR.
311	`plcfr=0.0 F`	Coefficient for the length dependence of CFR.
312	`pwcfr=0.0 F`	Coefficient for the width dependence of CFR.
313	`plwcfr=0.0 F`	Coefficient for the length times width dependence of CFR.
314	`pocfrd=0 F`	Coefficient for the geometry-independent part of CFR for drain side.
315	`plcfrd=0.0 F`	Coefficient for the length dependence of CFR for drain side.
316	`pwcfrd=0.0 F`	Coefficient for the width dependence of CFR for drain side.
317	`plwcfrd=0.0 F`	Coefficient for the length times width dependence of CFR for drain side.
318	`pofcgovacc=0.0`	Coefficient for the geometry-independent part of FCGOVACC.
319	`pofcgovaccd=0.0`	Coefficient for the geometry-independent part of FCGOVACC for drain side.
320	`pocgovaccg=1.0`	Coefficient for the geometry-independent part of CGOVACCG.
321	`pocinr=0.0 F`	Coefficient for the geometry-independent part of CINR.
322	`plcinr=0.0 F`	Coefficient for the length dependence of CINR.
323	`pwcinr=0.0 F`	Coefficient for the width dependence of CINR.
324	`plwcinr=0.0 F`	Coefficient for the length times width dependence of CINR.
325	`pocinrd=0.0 F`	Coefficient for the geometry-independent part of CINR for drain side.
326	`plcinrd=0.0 F`	Coefficient for the length dependence of CINR for drain side.
327	`pwcinrd=0.0 F`	Coefficient for the width dependence of CINR for drain side.

© 2023 Cadence Design Systems, Inc.

328	`plwcinrd=0.0 F`	Coefficient for the length times width dependence of CINR for drain side.
329	`podvfbinr=0.0 V`	Coefficient for the geometry-independent part of DVFBINR.
330	`pofcinrdep=0.3`	Coefficient for the geometry-independent part of FCINRDEP.
331	`pofcinracc=0.5`	Coefficient for the geometry-independent part of FCINRACC.
332	`poaxinr=0.5`	Coefficient for the geometry-independent part of AXINR.
333	`pofnt=1`	Coefficient for the geometry-independent part of FNT.
334	`pofntexc=0.0`	Coefficient for the geometry-independent part of FNTEXC.
335	`plfntexc=0.0`	Coefficient for the length dependence of FNTEXC.
336	`pwfntexc=0.0`	Coefficient for the width dependence of FNTEXC.
337	`plwfntexc=0.0`	Coefficient for the length times width dependence of FNTEXC.
338	`ponfa=8E+22 V^-1/m`^{4}	Coefficient for the geometry-independent part of NFA.
339	`plnfa=0.0 V^-1/m`^{4}	Coefficient for the length dependence of NFA.
340	`pwnfa=0.0 V^-1/m`^{4}	Coefficient for the width dependence of NFA.
341	`plwnfa=0.0 V^-1/m`^{4}	Coefficient for the length times width dependence of NFA.
342	`ponfb=3E+07 V^-1/m`^{2}	Coefficient for the geometry-independent part of NFB.
343	`plnfb=0.0 V^-1/m`^{2}	Coefficient for the length dependence of NFB.
344	`pwnfb=0.0 V^-1/m`^{2}	

© 2023 Cadence Design Systems, Inc.

		Coefficient for the width dependence of NFB.
345	plwnfb=0.0 V^-1/m^2	
		Coefficient for the length times width dependence of NFB.
346	ponfc=0 V^-1	Coefficient for the geometry-independent part of NFC.
347	plnfc=0.0 V^-1	Coefficient for the length dependence of NFC.
348	pwnfc=0.0 V^-1	Coefficient for the width dependence of NFC.
349	plwnfc=0.0 V^-1	Coefficient for the length times width dependence of NFC.
350	poef=1.0	Coefficient for the flicker noise frequency exponent.
351	pokvthowe=0	Coefficient for the geometry-independent part of KVTHOWE.
352	plkvthowe=0	Coefficient for the length dependence part of KVTHOWE.
353	pwkvthowe=0	Coefficient for the width dependence part of KVTHOWE.
354	plwkvthowe=0	Coefficient for the length times width dependence part of KVTHOWE.
355	pokuowe=0	Coefficient for the geometry-independent part of KUOWE.
356	plkuowe=0	Coefficient for the length dependence part of KUOWE.
357	pwkuowe=0	Coefficient for the width dependence part of KUOWE.
358	plwkuowe=0	Coefficient for the length times width dependence part of KUOWE.
359	lmin=0 m	Dummy parameter to label binning set.
360	lmax=1.0 m	Dummy parameter to label binning set.
361	wmin=0 m	Dummy parameter to label binning set.
362	wmax=1.0 m	Dummy parameter to label binning set.
363	popsce=0.0	Coefficient for the geometry-independent part of PSCE.
364	plpsce=0.0	Coefficient for the length dependence of PSCE.
365	pwpsce=0.0	Coefficient for the width dependence of PSCE.

© 2023 Cadence Design Systems, Inc.

366	`plwpsce=0.0`	Coefficient for the length times width dependence of PSCE.
367	`popsceb=0.0 V^-1`	Coefficient for the geometry-independent part of PSCEB.
368	`popsced=0.0 V^-1`	Coefficient for the geometry-independent part of PSCED.
369	`povfbedge=(-1.0) V`	Coefficient for the geometry-independent part of VFBEDGE.
370	`postvfbedge=0.0 V/K`	Coefficient for the geometry-independent part of STVFBEDGE.
371	`plstvfbedge=0.0 V/K`	Coefficient for the length dependence of STVFBEDGE
372	`pwstvfbedge=0.0 V/K`	Coefficient for the width dependence of STVFBEDGE.
373	`plwstvfbedge=0.0 V/K`	Coefficient for the length times width dependence of STVFBEDGE.
374	`podphibedge=0.0 V`	Coefficient for the geometry-independent part of DPHIBEDGE.
375	`pldphibedge=0.0 V`	Coefficient for the length dependence of DPHIBEDGE.
376	`pwdphibedge=0.0 V`	Coefficient for the width dependence of DPHIBEDGE.
377	`plwdphibedge=0.0 V`	Coefficient for the length times width dependence of DPHIBEDGE.
378	`poneffedge=5.0e23 m`$^{-3}$	Coefficient for the geometry-independent part of NEFFEDGE.
379	`plneffedge=0.0 m`$^{-3}$	Coefficient for the length dependence of NEFFEDGE.
380	`pwneffedge=0.0 m`$^{-3}$	Coefficient for the width dependence of NEFFEDGE.
381	`plwneffedge=0.0 m`$^{-3}$	Coefficient for the length times width dependence of NEFFEDGE.
382	`poctedge=0.0`	Coefficient for the geometry-independent part of CTEDGE.
383	`plctedge=0.0`	Coefficient for the length dependence of CTEDGE.
384	`pwctedge=0.0`	Coefficient for the width dependence of CTEDGE.
385	`plwctedge=0.0`	Coefficient for the length times width dependence of CTEDGE.
386	`pobetnedge=5.0e-4 m`^{2}`/V/s`	

© 2023 Cadence Design Systems, Inc.

		Coefficient for the geometry-independent part of BETNEDGE.
387	`plbetnedge=0.0` $m^2/V/s$	
		Coefficient for the length dependence of BETNEDGE.
388	`pwbetnedge=0.0` $m^2/V/s$	
		Coefficient for the width dependence of BETNEDGE.
389	`plwbetnedge=0.0` $m^2/V/s$	
		Coefficient for the length times width dependence of BETNEDGE.
390	`postbetedge=1.0`	Coefficient for the geometry-independent part of STBETEDGE.
391	`plstbetedge=0.0`	Coefficient for the length dependence of STBETEDGE.
392	`pwstbetedge=0.0`	Coefficient for the width dependence of STBETEDGE.
393	`plwstbetedge=0.0`	Coefficient for the length times width dependence of STBETEDGE.
394	`popsceedge=0.0`	Coefficient for the geometry-independent part of PSCEEDGE.
395	`plpsceedge=0.0`	Coefficient for the length dependence of PSCEEDGE.
396	`pwpsceedge=0.0`	Coefficient for the width dependence of PSCEEDGE.
397	`plwpsceedge=0.0`	Coefficient for the length times width dependence of PSCEEDGE.
398	`popscebedge=0.0 V^-1`	
		Coefficient for the geometry-independent part of PSCEBEDGE.
399	`popscededge=0.0 V^-1`	
		Coefficient for the geometry-independent part of PSCEDEDGE.
400	`pocfedge=0.0`	Coefficient for the geometry-independent part of CFEDGE.
401	`plcfedge=0.0`	Coefficient for the length dependence of CFEDGE.
402	`pwcfedge=0.0`	Coefficient for the width dependence of CFEDGE.

© 2023 Cadence Design Systems, Inc.

403	`plwcfedge=0.0`	Coefficient for the length times width dependence of CFEDGE.
404	`pocfdedge=0.0 V^-1`	Coefficient for the geometry-independent part of CFDEDGE.
405	`pocfbedge=0.0 V^-1`	Coefficient for the geometry-independent part of CFBEDGE.
406	`pofntedge=1.0`	Coefficient for the geometry-independent part of FNTEDGE.
407	`ponfaedge=8.0e22 V^-1/m`^{4}	Coefficient for the geometry-independent part of NFAEDGE.
408	`plnfaedge=0.0 V^-1/m`^{4}	Coefficient for the length dependence of NFAEDGE.
409	`pwnfaedge=0.0 V^-1/m`^{4}	Coefficient for the width dependence of NFAEDGE.
410	`plwnfaedge=0.0 V^-1/m`^{4}	Coefficient for the length times width dependence of NFAEDGE.
411	`ponfbedge=3.0e7 V^-1/m`^{2}	Coefficient for the geometry-independent part of NFBEDGE.
412	`plnfbedge=0.0 V^-1/m`^{2}	Coefficient for the length dependence of NFBEDGE.
413	`pwnfbedge=0.0 V^-1/m`^{2}	Coefficient for the width dependence of NFBEDGE.
414	`plwnfbedge=0.0 V^-1/m`^{2}	Coefficient for the length times width dependence of NFBEDGE.
415	`ponfcedge=0.0 V^-1`	Coefficient for the geometry-independent part of NFCEDGE.
416	`plnfcedge=0.0 V^-1`	Coefficient for the length dependence of NFCEDGE.
417	`pwnfcedge=0.0 V^-1`	Coefficient for the width dependence of NFCEDGE.

© 2023 Cadence Design Systems, Inc.

418	`plwnfcedge=0.0 V^-1`	Coefficient for the length times width dependence of NFCEDGE.
419	`poefedge=1.0`	Coefficient for the geometry-independent part of EFEDGE.
420	`lvaro=0.0 m`	Geometry-independent difference between actual and programmed gate length.
421	`lvarl=0.0`	Length dependence of LVAR.
422	`lvarw=0.0`	Width dependence of LVAR.
423	`lap=0.0 m`	Effective channel length reduction per side.
424	`wvaro=0.0 m`	Geometry-independent difference between actual and programmed field-oxide opening.
425	`wvarl=0.0`	Length dependence of WVAR.
426	`wvarw=0.0`	Width dependence of WVAR.
427	`wot=0.0 m`	Effective channel width reduction per side.
428	`dlq=0.0 m`	Effective channel length reduction for CV.
429	`dwq=0.0 m`	Effective channel width reduction for CV.
430	`vfbo=-1.0 V`	Geometry-independent flat-band voltage at TR.
431	`vfbl=0.0 V`	Length dependence of flat-band voltage.
432	`vfbw=0.0 V`	Width dependence of flat-band voltage.
433	`vfblw=0.0 V`	Area dependence of flat-band voltage.
434	`stvfbo=5e-4 V/K`	Geometry-independent temperature dependence of VFB.
435	`stvfbl=0.0 V/K`	Length dependence of temperature dependence of VFB.
436	`stvfbw=0.0 V/K`	Width dependence of temperature dependence of VFB.
437	`stvfblw=0.0 V/K`	Area dependence of temperature dependence of VFB.
438	`toxo=2e-9 m`	Gate oxide thickness.
439	`epsroxo=3.9`	Relative permittivity of gate dielectric.
440	`nsubo=3e23` m^{-3}	Geometry-independent substrate doping.

© 2023 Cadence Design Systems, Inc.

441	`nsubw=0.0`	Width dependence of background doping NSUBO due to segregation.
442	`wseg=1e-8 m`	Character length of segregation of background doping NSUBO.
443	`npck=1e24 m`$^{-3}$	Pocket doping level.
444	`npckw=0.0`	Width dependence of pocket doping NPCK due to segregation.
445	`wsegp=1e-8 m`	Character length of segregation of pocket doping NPCK.
446	`lpck=1e-8 m`	Character length of lateral doping profile.
447	`lpckw=0.0`	Width dependence of character length of lateral doping profile.
448	`fol1=0.0`	First length dependence coefficient for short channel body effect.
449	`fol2=0.0`	Second length dependence coefficient for short channel body effect.
450	`facneffaco=1.0`	Geometry-independent pre-factor for effective substrate doping in separate charge calculation.
451	`facneffacl=0.0`	Length dependence of FACNEFFAC.
452	`facneffacw=0.0`	Width dependence of FACNEFFAC.
453	`facneffaclw=0.0`	Area dependence of FACNEFFAC.
454	`gfacnudo=1.0`	Geometry-independent bodyfactor change due to NUD-effect.
455	`gfacnudl=0.0`	Length dependence of GFACNUD.
456	`gfacnudlexp=1.0`	Exponent for length dependence of GFACNUD.
457	`gfacnudw=0.0`	Width dependence of GFACNUD.
458	`gfacnudlw=0.0`	Area dependence of GFACNUD.
459	`vsbnudo=0.0 V`	Lower Vsb value for NUD-effect.
460	`dvsbnudo=1.0 V`	Vsb range for NUD-effect.
461	`vnsubo=0.0 V`	Effective doping bias-dependence parameter.
462	`nslpo=0.05 V`	Effective doping bias-dependence parameter.
463	`dnsubo=0.0 V^-1`	Effective doping bias-dependence parameter.

© 2023 Cadence Design Systems, Inc.

464	`dphibo=0.0 V`	Geometry-independent offset of PHIB.
465	`dphibl=0.0 V`	Length dependence offset of PHIB.
466	`dphiblexp=1.0`	Exponent for length dependence of offset of PHIB.
467	`dphibw=0.0 V`	Width dependence of offset of PHIB.
468	`dphiblw=0.0 V`	Area dependence of offset of PHIB.
469	`delvtaco=0.0 V`	Geometry-independent offset parameter for PHIB in separate charge calculation.
470	`delvtacl=0.0 V`	Length dependence of DELVTAC.
471	`delvtaclexp=1.0`	Exponent for length dependence of offset of DELVTAC.
472	`delvtacw=0.0 V`	Width dependence of DELVTAC.
473	`delvtaclw=0.0 V`	Area dependence of DELVTAC.
474	`npo=1e26` m^{-3}	Geometry-independent gate poly-silicon doping.
475	`npl=0.0`	Length dependence of gate poly-silicon doping.
476	`cto=0.0`	Geometry-independent interface states factor.
477	`ctl=0.0`	Length dependence of interface states factor.
478	`ctlexp=1.0`	Exponent for length dependence of interface states factor.
479	`ctw=0.0`	Width dependence of interface states factor.
480	`ctlw=0.0`	Area dependence of interface states factor.
481	`toxovo=2e-9 m`	Overlap oxide thickness.
482	`toxovdo=2e-9 m`	Overlap oxide thickness for drain side.
483	`lov=0 m`	Overlap length for gate/drain and gate/source overlap capacitance.
484	`lovd=0 m`	Overlap length for gate/drain overlap capacitance.
485	`novo=5.0e25` m^{-3}	Effective doping of overlap region.
486	`novdo=5.0e25` m^{-3}	Effective doping of overlap region for drain side.
487	`cfl=0.0`	Length dependence of DIBL-parameter.
488	`cflexp=2.0`	Exponent for length dependence of CF.
489	`cfw=0.0`	Width dependence of CF.
490	`cfbo=0.0 V^-1`	Back-bias dependence of CF.

© 2023 Cadence Design Systems, Inc.

491	`uo=5e-2 m^2/V/s`	Zero-field mobility at TR.
492	`fbet1=0.0`	Relative mobility decrease due to first lateral profile.
493	`fbet1w=0.0`	Width dependence of relative mobility decrease due to first lateral profile.
494	`lp1=1e-8 m`	Mobility-related characteristic length of first lateral profile.
495	`lp1w=0.0`	Width dependence of mobility-related characteristic length of first lateral profile.
496	`fbet2=0.0`	Relative mobility decrease due to second lateral profile.
497	`lp2=1e-8 m`	Mobility-related characteristic length of second lateral profile.
498	`betw1=0.0`	First higher-order width scaling coefficient of BETN.
499	`betw2=0.0`	Second higher-order width scaling coefficient of BETN.
500	`wbet=1e-9 m`	Characteristic width for width scaling of BETN.
501	`stbeto=1.0`	Geometry-independent temperature dependence of BETN.
502	`stbetl=0.0`	Length dependence of temperature dependence of BETN.
503	`stbetw=0.0`	Width dependence of temperature dependence of BETN.
504	`stbetlw=0.0`	Area dependence of temperature dependence of BETN.
505	`mueo=0.5 m/V`	Geometry-independent mobility reduction coefficient at TR.
506	`muew=0.0`	Width dependence of mobility reduction coefficient at TR.
507	`stmueo=0.0`	Temperature dependence of MUE.
508	`themuo=1.5`	Mobility reduction exponent at TR.
509	`stthemuo=1.5`	Temperature dependence of THEMU.
510	`cso=0.0`	Geometry-independent coulomb scattering parameter at TR.
511	`csl=0.0`	Length dependence of CS.

© 2023 Cadence Design Systems, Inc.

512	`cslexp=1.0`	Exponent for length dependence of CS.
513	`csw=0.0`	Width dependence of CS.
514	`cslw=0.0`	Area dependence of CS.
515	`stcso=0.0`	Temperature dependence of CS.
516	`xcoro=0.0 V^-1`	Geometry-independent non-universality parameter.
517	`xcorl=0.0`	Length dependence of non-universality parameter.
518	`xcorw=0.0`	Width dependence of non-universality parameter.
519	`xcorlw=0.0`	Area dependence of non-universality parameter.
520	`stxcoro=0.0`	Temperature dependence of XCOR.
521	`fetao=1.0`	Effective field parameter.
522	`rsw1=50.0 Ω`	Source/drain series resistance for 1 um wide channel at TR.
523	`rsw2=0.0`	Higher-order width scaling of RS.
524	`strso=1.0`	Temperature dependence of RS.
525	`rsbo=0.0 V^-1`	Back-bias dependence of series resistance.
526	`rsgo=0.0 V^-1`	Gate-bias dependence of series resistance.
527	`thesato=0.0 V^-1`	Geometry-independent velocity saturation parameter at TR.
528	`thesatl=0.05 V^-1`	Length dependence of THESAT.
529	`thesatlexp=1.0`	Exponent for length dependence of THESAT.
530	`thesatw=0.0`	Width dependence of velocity saturation parameter.
531	`thesatlw=0.0`	Area dependence of velocity saturation parameter.
532	`stthesato=1.0`	Geometry-independent temperature dependence of THESAT.
533	`stthesatl=0.0`	Length dependence of temperature dependence of THESAT.
534	`stthesatw=0.0`	Width dependence of temperature dependence of THESAT.
535	`stthesatlw=0.0`	Area dependence of temperature dependence of THESAT.
536	`thesatbo=0.0 V^-1`	Back-bias dependence of velocity saturation.

© 2023 Cadence Design Systems, Inc.

537	`thesatgo=0.0 V^-1`	Gate-bias dependence of velocity saturation.
538	`axo=18`	Geometry-independent linear/saturation transition factor.
539	`axl=0.4`	Length dependence of AX.
540	`alpl=5e-4`	Length dependence of ALP.
541	`alplexp=1.0`	Exponent for length dependence of ALP.
542	`alpw=0.0`	Width dependence of ALP.
543	`alp1l1=0.0 V`	Length dependence of CLM enhancement factor above threshold.
544	`alp1lexp=0.5`	Exponent for length dependence of ALP1.
545	`alp1l2=0.0`	Second_order length dependence of ALP1.
546	`alp1w=0.0`	Width dependence of ALP1.
547	`alp2l1=0.0 V^-1`	Length dependence of CLM enhancement factor below threshold.
548	`alp2lexp=0.5`	Exponent for length dependence of ALP2.
549	`alp2l2=0.0`	Second_order length dependence of ALP2.
550	`alp2w=0.0`	Width dependence of ALP2.
551	`vpo=0.05 V`	CLM logarithmic dependence parameter.
552	`a1o=1.0`	Geometry-independent impact-ionization pre-factor.
553	`a1l=0.0`	Length dependence of A1.
554	`a1w=0.0`	Width dependence of A1.
555	`a2o=10 V`	Impact-ionization exponent at TR.
556	`sta2o=0.0 V`	Temperature dependence of A2.
557	`a3o=1.0`	Geometry-independent saturation-voltage dependence of II.
558	`a3l=0.0`	Length dependence of A3.
559	`a3w=0.0`	Width dependence of A3.
560	`a4o=0.0 V^-0.5`	Geometry-independent back-bias dependence of II.
561	`a4l=0.0`	Length dependence of A4.
562	`a4w=0.0`	Width dependence of A4.

© 2023 Cadence Design Systems, Inc.

563	`gcoo=0.0`	Gate tunneling energy adjustment.
564	`iginvlw=0.0 A`	Gate channel current pre-factor for 1 um^2 channel area.
565	`igovw=0.0 A`	Gate overlap current pre-factor for 1 um wide channel.
566	`igovdw=0.0 A`	Gate overlap current pre-factor for 1 um wide channel for drain side.
567	`stigo=2.0`	Temperature dependence of IGINV and IGOV.
568	`gc2o=0.375`	Gate current slope factor.
569	`gc3o=0.063`	Gate current curvature factor.
570	`chibo=3.1 V`	Tunneling barrier height.
571	`agidlw=0.0 A/V`^{3}	Width dependence of GIDL pre-factor.
572	`agidldw=0.0 A/V`^{3}	Width dependence of GIDL pre-factor for drain side.
573	`bgidlo=41 V`	GIDL probability factor at TR.
574	`bgidldo=41 V`	GIDL probability factor at TR for drain side.
575	`stbgidlo=0.0 V/K`	Temperature dependence of BGIDL.
576	`stbgidldo=0.0 V/K`	Temperature dependence of BGIDL for drain side.
577	`cgidlo=0.0`	Back-bias dependence of GIDL.
578	`cgidldo=0.0`	Back-bias dependence of GIDL for drain side.
579	`cgbovl=0.0 F`	Oxide capacitance for gate-bulk overlap for 1 um long channel.
580	`cfrw=0.0 F`	Outer fringe capacitance for 1 um wide channel.
581	`cfrdw=0.0 F`	Outer fringe capacitance for 1 um wide channel for drain side.
582	`fcgovacco=0.0`	Factor for overlap capacitances in accumulation regime.
583	`fcgovaccdo=0.0`	Factor for overlap capacitances in accumulation regime for drain side.
584	`cgovaccgo=1.0`	Gate voltage dependence parameter of overlap capacitances in accumulation regime.
585	`cinrw=0.0 F`	Inner fringe capacitance for 1 um wide channel.

© 2023 Cadence Design Systems, Inc.

586	`cinrdw=0.0 F`	Inner fringe capacitance for 1 um wide channel for drain side.
587	`dvfbinro=0.0 V`	Flat-band voltage offset of inner fringe capacitances.
588	`fcinrdepo=0.3`	Bias dependence parameter of inner fringe capacitances in depletion regime.
589	`fcinracco=0.5`	Bias dependence parameter of inner fringe capacitances in accumulation regime.
590	`axinro=0.5`	Accumulation/depletion transition factor of inner fringe capacitances.
591	`fnto=1.0`	Thermal noise coefficient.
592	`fntexcl=0.0`	Length dependence coefficient of excess noise.
593	`nfalw=8e22 V^-1/m`^{4}	First coefficient of flicker noise for 1 um^2 channel area.
594	`nfblw=3e7 V^-1/m`^{2}	Second coefficient of flicker noise for 1 um^2 channel area.
595	`nfclw=0.0 V^-1`	Third coefficient of flicker noise for 1 um^2 channel area.
596	`efo=1.0`	Flicker noise frequency exponent.
597	`lintnoi=0.0 m`	Length offset for flicker noise.
598	`alpnoi=2.0`	Exponent for length offset for flicker noise.
599	`kvthoweo=0`	Geometrical independent threshold shift parameter.
600	`kvthowel=0`	Length dependent threshold shift parameter.
601	`kvthowew=0`	Width dependent threshold shift parameter.
602	`kvthowelw=0`	Area dependent threshold shift parameter.
603	`kuoweo=0`	Geometrical independent mobility degradation factor.
604	`kuowel=0`	Length dependent mobility degradation factor.
605	`kuowew=0`	Width dependent mobility degradation factor.
606	`kuowelw=0`	Area dependent mobility degradation factor.
607	`munqso=1.0`	Relative mobility for NQS modelling.

© 2023 Cadence Design Systems, Inc.

608	`rgo=0.0` Ω	Gate resistance.
609	`rint=0.0` Ω m^2	Contact resistance between silicide and ploy.
610	`rvpoly=0.0` Ω m^2	Vertical poly resistance.
611	`rshg=0.0` Ω/Sqr	Gate electrode diffusion sheet resistance.
612	`dlsil=0.0 m`	Silicide extension over the physical gate length.
613	`rsh=0.0` Ω/sq	Sheet resistance of source diffusion.
614	`rshd=0.0` Ω/sq	Sheet resistance of drain diffusion.
615	`rbulko=0.0` Ω	Bulk resistance between node BP and BI.
616	`rwello=0.0` Ω	Well resistance between node BI and B.
617	`rjunso=0.0` Ω	Source-side bulk resistance between node BI and BS.
618	`rjundo=0.0` Ω	Drain-side bulk resistance between node BI and BD.
619	`rtho=0.0 K/W`	Geometry-independent part of thermal resistance.
620	`rthw1=0.0 K/W`	Width dependence of thermal resistance.
621	`rthw2=0.0`	Offset in width dependence of thermal resistance.
622	`rthlw=0.0`	Length-correction to width dependence of thermal resistance.
623	`ctho=0.0 J/K`	Geometry-independent part of thermal capacitance.
624	`cthw1=0.0 J/K`	Width dependence of thermal capacitance.
625	`cthw2=0.0`	Offset in width dependence of thermal capacitance.
626	`cthlw=0.0`	Length-correction to width dependence of thermal capacitance.
627	`strtho=0.0`	Temperature sensitivity of RTH.
628	`saref=1.0e-6 m`	Reference distance between OD-edge and poly from one side.
629	`sbref=1.0e-6 m`	Reference distance between OD-edge and poly from other side.
630	`wlod=0 m`	Width parameter.
631	`kuo=0 m`	Mobility degradation/enhancement coefficient.

© 2023 Cadence Design Systems, Inc.

632	`kvsat=0 m`	Saturation velocity degradation/enhancement coefficient.
633	`tkuo=0`	Temperature dependence of KUO.
634	`lkuo=0 m^LLODKUO`	Length dependence of KUO.
635	`wkuo=0 m^WLODKUO`	Width dependence of KUO.
636	`pkuo=0 m^(LLODKUO+WLODKUO`	Cross-term dependence of KUO.
637	`llodkuo=0`	Length parameter for UO stress effect.
638	`wlodkuo=0`	Width parameter for UO stress effect.
639	`kvtho=0 Vm`	Threshold shift parameter.
640	`lkvtho=0 m^LLODVTH`	Length dependence of KVTHO.
641	`wkvtho=0 m^WLODVTH`	Width dependence of KVTHO.
642	`pkvtho=0 m^(LLODVTH+WLODVTH`	Cross-term dependence of KVTHO.
643	`llodvth=0`	Length parameter for VTH-stress effect.
644	`wlodvth=0`	Width parameter for VTH-stress effect.
645	`stetao=0 m`	eta0 shift factor related to VTHO change.
646	`lodetao=1.0`	eta0 shift modification factor for stress effect.
647	`scref=1.0e-6 m`	Distance between OD-edge and well edge of a reference device.
648	`web=0`	Coefficient for SCB.
649	`wec=0`	Coefficient for SCC.
650	`imax=1000 A`	Maximum current up to which forward current behaves exponentially.
651	`trj=21 C`	reference temperature.
652	`frev=1.0e3`	Coefficient for reverse breakdown current limitation.
653	`cjorbot=1E-3 Fm`$^{-2}$	

© 2023 Cadence Design Systems, Inc.

		Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction.
654	`cjorsti=1E-9 Fm^-1`	
		Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction.
655	`cjorgat=1E-9 Fm^-1`	
		Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction.
656	`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component for source-bulk junction.
657	`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component for source-bulk junction.
658	`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component for source-bulk junction.
659	`pbot=0.5`	Grading coefficient of bottom component for source-bulk junction.
660	`psti=0.5`	Grading coefficient of STI-edge component for source-bulk junction.
661	`pgat=0.5`	Grading coefficient of gate-edge component for source-bulk junction.
662	`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component for source-bulk junction.
663	`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for source-bulk junction.
664	`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for source-bulk junction.
665	`idsatrbot=1E-12` Am^{-2}	
		Saturation current density at the reference temperature of bottom component for source-bulk junction.
666	`idsatrsti=1E-18 Am^-1`	
		Saturation current density at the reference temperature of STI-edge component for source-bulk junction.
667	`idsatrgat=1E-18 Am^-1`	

© 2023 Cadence Design Systems, Inc.

		Saturation current density at the reference temperature of gate-edge component for source-bulk junction.
668	`csrhbot=1E2` Am^{-3}	Shockley-Read-Hall prefactor of bottom component for source-bulk junction.
669	`csrhsti=1E-4` Am^{-2}	Shockley-Read-Hall prefactor of STI-edge component for source-bulk junction.
670	`csrhgat=1E-4` Am^{-2}	Shockley-Read-Hall prefactor of gate-edge component for source-bulk junction.
671	`xjunsti=100E-9 m`	Junction depth of STI-edge component for source-bulk junction.
672	`xjungat=100E-9 m`	Junction depth of gate-edge component for source-bulk junction.
673	`ctatbot=1E2` Am^{-3}	Trap-assisted tunneling prefactor of bottom component for source-bulk junction.
674	`ctatsti=1E-4` Am^{-2}	Trap-assisted tunneling prefactor of STI-edge component for source-bulk junction.
675	`ctatgat=1E-4` Am^{-2}	Trap-assisted tunneling prefactor of gate-edge component for source-bulk junction.
676	`mefftatbot=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for source-bulk junction.
677	`mefftatsti=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for source-bulk junction.
678	`mefftatgat=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for source-bulk junction.
679	`cbbtbot=1E-12` AV^{-3}	Band-to-band tunneling prefactor of bottom component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

680	`cbbtsti=1E-18 AV-3m`	Band-to-band tunneling prefactor of STI-edge component for source-bulk junction.
681	`cbbtgat=1E-18 AV-3m`	Band-to-band tunneling prefactor of gate-edge component for source-bulk junction.
682	`fbbtrbot=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction.
683	`fbbtrsti=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction.
684	`fbbtrgat=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction.
685	`stfbbtbot=-1E-3 K^-1`	Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction.
686	`stfbbtsti=-1E-3 K^-1`	Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction.
687	`stfbbtgat=-1E-3 K^-1`	Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction.
688	`vbrbot=10 V`	Breakdown voltage of bottom component for source-bulk junction.
689	`vbrsti=10 V`	Breakdown voltage of STI-edge component for source-bulk junction.

© 2023 Cadence Design Systems, Inc.

690	`vbrgat=10 V`	Breakdown voltage of gate-edge component for source-bulk junction.
691	`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component for source-bulk junction.
692	`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component for source-bulk junction.
693	`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component for source-bulk junction.
694	`cjorbotd=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction.
695	`cjorstid=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction.
696	`cjorgatd=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction.
697	`vbirbotd=1 V`	Built-in voltage at the reference temperature of bottom component for drain-bulk junction.
698	`vbirstid=1 V`	Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction.
699	`vbirgatd=1 V`	Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction.
700	`pbotd=0.5`	Grading coefficient of bottom component for drain-bulk junction.
701	`pstid=0.5`	Grading coefficient of STI-edge component for drain-bulk junction.
702	`pgatd=0.5`	Grading coefficient of gate-edge component for drain-bulk junction.
703	`phigbotd=1.16 V`	Zero-temperature bandgap voltage of bottom component for drain-bulk junction.
704	`phigstid=1.16 V`	Zero-temperature bandgap voltage of STI-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

705	`phiggatd=1.16 V`	Zero-temperature bandgap voltage of gate-edge component for drain-bulk junction.
706	`idsatrbotd=1E-12 Am`$^{-2}$	Saturation current density at the reference temperature of bottom component for drain-bulk junction.
707	`idsatrstid=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component for drain-bulk junction.
708	`idsatrgatd=1E-18 Am^-1`	Saturation current density at the reference temperature of gate-edge component for drain-bulk junction.
709	`csrhbotd=1E2 Am`$^{-3}$	Shockley-Read-Hall prefactor of bottom component for drain-bulk junction.
710	`csrhstid=1E-4 Am`$^{-2}$	Shockley-Read-Hall prefactor of STI-edge component for drain-bulk junction.
711	`csrhgatd=1E-4 Am`$^{-2}$	Shockley-Read-Hall prefactor of gate-edge component for drain-bulk junction.
712	`xjunstid=100E-9 m`	Junction depth of STI-edge component for drain-bulk junction.
713	`xjungatd=100E-9 m`	Junction depth of gate-edge component for drain-bulk junction.
714	`ctatbotd=1E2 Am`$^{-3}$	Trap-assisted tunneling prefactor of bottom component for drain-bulk junction.
715	`ctatstid=1E-4 Am`$^{-2}$	Trap-assisted tunneling prefactor of STI-edge component for drain-bulk junction.
716	`ctatgatd=1E-4 Am`$^{-2}$	Trap-assisted tunneling prefactor of gate-edge component for drain-bulk junction.

© 2023 Cadence Design Systems, Inc.

717	`mefftatbotd=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of bottom component for drain-bulk junction.
718	`mefftatstid=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component for drain-bulk junction.
719	`mefftatgatd=0.25`	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component for drain-bulk junction.
720	`cbbtbotd=1E-12 AV`$^{-3}$	Band-to-band tunneling prefactor of bottom component for drain-bulk junction.
721	`cbbtstid=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction.
722	`cbbtgatd=1E-18 AV`$^{-3}$`m`	Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction.
723	`fbbtrbotd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction.
724	`fbbtrstid=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction.
725	`fbbtrgatd=1E9 Vm^-1`	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction.
726	`stfbbtbotd=-1E-3 K^-1`	Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction.
727	`stfbbtstid=-1E-3 K^-1`	

© 2023 Cadence Design Systems, Inc.

		Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction.
728	`stfbbtgatd=-1E-3 K^-1`	
		Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction.
729	`vbrbotd=10 V`	Breakdown voltage of bottom component for drain-bulk junction.
730	`vbrstid=10 V`	Breakdown voltage of STI-edge component for drain-bulk junction.
731	`vbrgatd=10 V`	Breakdown voltage of gate-edge component for drain-bulk junction.
732	`pbrbotd=4 V`	Breakdown onset tuning parameter of bottom component for drain-bulk junction.
733	`pbrstid=4 V`	Breakdown onset tuning parameter of STI-edge component for drain-bulk junction.
734	`pbrgatd=4 V`	Breakdown onset tuning parameter of gate-edge component for drain-bulk junction.
735	`swjunexp=0`	Flag for JUNCAP-express; 0,full model, 1,express model.
736	`vjunref=2.5`	Typical maximum source-bulk junction voltage; usually about 2*VSUP.
737	`fjunq=0.03`	Fraction below which source-bulk junction capacitance components are considered negligible.
738	`vjunrefd=2.5`	Typical maximum drain-bulk junction voltage; usually about 2*VSUP.
739	`fjunqd=0.03`	Fraction below which drain-bulk junction capacitance components are considered negligible.
740	`dta=0.0 K`	Temperature offset w.r.t. ambient temperature.
741	`noisemethod=oldcmi`	
		Induced gate noise implementation. Possible values are `oldcmi` and `subckt`.

© 2023 Cadence Design Systems, Inc.

742	`swqsat=0`	Flag for separate capacitance calculation in saturation only: 0=off, 1=on.
743	`swqpart=0`	Flag for drain/source charge partitioning; 0=linear distribution, 1=source.Flag for drain/source charge partitioning; 0=linear distribution, 1=source.
744	`cfac=0.0`	DIBL-parameter of charge model when SWQSAT=1.
745	`thesatac=1.0 V^-1`	Velocity saturation parameter at TR of charge model when SWQSAT=1.
746	`axac=3.0`	Linear/saturation transition factor of charge model when SWQSAT=1.
747	`alpac=0.01`	CLM pre-factor of charge model when SWQSAT=1.
748	`gc2ov=0.375`	Gate overlap current slope factor, used only when SWIGATE=2.
749	`gc3ov=0.063`	Gate overlap current curvature factor, used only when SWIGATE=2.
750	`cfacl=0.0`	Length dependence of DIBL-parameter of charge model when SWQSAT=1.
751	`cfaclexp=2.0`	Exponent for length dependence of CF.
752	`cfacw=0.0`	Width dependence of CF.
753	`thesataco=0.0 V^-1`	Geometry-independent velocity saturation parameter at TR of charge model when SWQSAT=1.
754	`thesatacl=0.05 V^-1`	Length dependence of THESATAC.
755	`thesataclexp=1.0`	Exponent for length dependence of THESATAC.
756	`thesatacw=0.0`	Width dependence of THESATAC.
757	`thesataclw=0.0`	Area dependence of THESATAC.
758	`axaco=18.0`	Geometry-independent linear/saturation transition factor of charge model when SWQSAT=1.
759	`axacl=0.4`	Length dependence of AXAC.
760	`alpacl=5.0e-4`	Length dependence of ALPAC.
761	`alpaclexp=1.0`	Exponent for length dependence of ALPAC.
762	`alpacw=0.0`	Width dependence of ALPAC.

© 2023 Cadence Design Systems, Inc.

763	`gc2ovo=0.375`	Gate overlap current slope factor, used only when SWIGATE=2.
764	`gc3ovo=0.063`	Gate overlap current curvature factor, used only when SWIGATE=2.
765	`pocfac=0.0`	Coefficient for the geometry dependence of CFAC.
766	`plcfac=0.0`	Coefficient for the length dependence of CFAC.
767	`pwcfac=0.0`	Coefficient for the width dependence of CFAC.
768	`plwcfac=0.0`	Coefficient for the length times width dependence of CFAC.
769	`pothesatac=1.0 V^-1`	Coefficient for the geometry-independent part of THESATAC.
770	`plthesatac=0.0 V^-1`	Coefficient for the length dependence of THESATAC.
771	`pwthesatac=0.0 V^-1`	Coefficient for the width dependence of THESATAC.
772	`plwthesatac=0.0 V^-1`	Coefficient for the length times width dependence of THESATAC.
773	`poaxac=3.0`	Coefficient for the geometry-independent part of AXAC.
774	`plaxac=0.0`	Coefficient for the length dependence of AXAC.
775	`pwaxac=0.0`	Coefficient for the width dependence of AXAC.
776	`plwaxac=0.0`	Coefficient for the length times width dependence of AXAC.
777	`poalpac=1.0e-2`	Coefficient for the geometry-independent part of ALPAC.
778	`plalpac=0.0`	Coefficient for the length dependence of ALPAC
779	`pwalpac=0.0`	Coefficient for the width dependence of ALPAC.
780	`plwalpac=0.0`	Coefficient for the length times width dependence of ALPAC.
781	`pogc2ov=0.375`	Coefficient for the geometry-independent part of GC2OV, used only when SWIGATE=2.
782	`pogc3ov=0.063`	Coefficient for the geometry-independent part of GC3OV, used only when SWIGATE=2.
783	`kvsatac=0.0 m`	Saturation velocity degradation/enhancement coefficient of charge model when SWQSAT=1.

© 2023 Cadence Design Systems, Inc.

784	betnedge=5.0e-4 $m^2/V/s$	Channel aspect ratio times zero-field mobility of edge transistor.
785	stbetedge=1.0	Temperature dependence of BETNEDGE.
786	betedgew=0.0	Width scaling coefficient of edge transistor mobility.
787	cfbedge=0.0 V^-1	Bulk voltage dependence parameter of DIBL-parameter of edge transistors.
788	cfbedgeo=0.0 V^-1	Bulk voltage dependence parameter of DIBL-parameter of edge transistors.
789	cfd=0.0 V^-1	Drain voltage dependence of CF.
790	cfdedge=0.0 V^-1	Drain voltage dependence parameter of DIBL-parameter of edge transistors.
791	cfdedgeo=0.0 V^-1	Drain voltage dependence parameter of DIBL-parameter of edge transistors.
792	cfdo=0.0 V^-1	Drain voltage dependence of CF.
793	cfedge=0.0	DIBL parameter of edge transistors.
794	cfedgel=0.0	Length dependence of DIBL-parameter of edge transistors.
795	cfedgelexp=2.0	Exponent for length dependence of DIBL-parameter of edge transistors.
796	cfedgew=0.0	Width dependence of DIBL-parameter of edge transistors.
797	ctedge=0.0	Interface states factor of edge transistors.
798	ctedgeo=0.0	Geometry-independent interface states factor of edge transistors.
799	ctedgel=0.0	Length dependence of interface states factor of edge transistors.
800	ctedgelexp=1.0	Exponent for length dependence of interface states factor of edge transistors.
801	dphibedge=0.0 V	Offset parameter for PHIB of edge transistors.
802	dphibedgeo=0.0 V	Geometry-independent of edge transistor PHIB offset.
803	dphibedgel=0.0 V	Length dependence of edge transistor PHIB offset.

© 2023 Cadence Design Systems, Inc.

804	dphibedgelexp=1.0	Exponent for length dependence of edge transistor PHIB offset.
805	dphibedgew=0.0 V	Width dependence of edge transistor PHIB offset.
806	dphibedgelw=0.0 V	Area dependence of edge transistor PHIB offset.
807	efedge=1.0	Flicker noise frequency exponent of edge transistors.
808	efedgeo=1.0	Flicker noise frequency exponent.
809	fbetedge=0.0	Length dependence of edge transistor mobility.
810	fntedge=1.0	Thermal noise coefficient of edge transistors.
811	fntedgeo=1.0	Thermal noise coefficient.
812	lpedge=1.0e-8 m	Exponent for length dependence of edge transistor mobility.
813	neffedge=5.0e23 m^{-3}	Effective substrate doping of edge transistors.
814	nfaedge=8.0e22 V^{-1}/m^4	First coefficient of flicker noise of edge transistors.
815	nfaedgelw=8.0e22 V^{-1}/m^4	First coefficient of flicker noise for 1 um^2 channel area.
816	nfbedge=3.0e07 V^{-1}/m^2	Second coefficient of flicker noise of edge transistors.
817	nfbedgelw=3.0e7 V^{-1}/m^2	Second coefficient of flicker noise for 1 um^2 channel area.
818	nfcedge=0.0 V^-1	Third coefficient of flicker noise of edge transistors.
819	nfcedgelw=0.0 V^-1	Third coefficient of flicker noise for 1 um^2 channel area.
820	nsubedgel=0.0	Length dependence of edge transistor substrate doping.
821	nsubedgew=0.0	Width dependence of edge transistor substrate doping.
822	nsubedgelw=0.0	Area dependence of edge transistor substrate doping.
823	nsubedgeo=5.0e23 m^{-3}	Geometry-independent substrate doping of edge transistors.
824	psce=0.0	Subthreshold slope coefficient for short channel transistor.

© 2023 Cadence Design Systems, Inc.

825	`psceb=0.0 V^-1`	Bulk voltage dependence parameter of subthreshold slope coefficient for short channel transistor.
826	`pscebedge=0.0 V^-1`	Bulk voltage dependence parameter of subthreshold slope coefficient for short channel edge transistors.
827	`pscebedgeo=0.0 V^-1`	Bulk voltage dependence parameter of subthreshold slope coefficient for short channel edge transistors.
828	`pscebo=0.0 V^-1`	Bulk voltage dependence parameter of subthreshold slope coefficient for short channel transistor.
829	`psced=0.0 V^-1`	Drain voltage dependence parameter of subthreshold slope coefficient for short channel transistor.
830	`pscededge=0.0 V^-1`	Drain voltage dependence parameter of subthreshold slope coefficient for short channel edge transistors.
831	`pscedo=0.0 V^-1`	Drain voltage dependence parameter of subthreshold slope coefficient for short channel transistor.
832	`pscededgeo=0.0 V^-1`	Drain voltage dependence parameter of subthreshold slope coefficient for short channel edge transistors.
833	`psceedge=0.0`	Subthreshold slope coefficient for short channel edge transistors.
834	`psceedgel=0.0`	Length dependence of subthreshold slope coefficient for short channel edge transistors.
835	`psceedgelexp=2.0`	Exponent for length dependence of subthreshold slope coefficient for short channel edge transistors.
836	`psceedgew=0.0`	Exponent for length dependence of subthreshold slope coefficient for short channel edge transistor.
837	`pscel=0.0`	Length dependence of subthreshold slope coefficient for short channel transistor.
838	`pscelexp=2.0`	Exponent for length dependence of subthreshold slope coefficient for short channel transistor.
839	`pscew=0.0`	Exponent for length dependence of subthreshold slope coefficient for short channel transistor.
840	`stbetedgeo=1.0`	Geometry-independent temperature dependence of BETNEDGE.
841	`stbetedgel=0.0`	Length dependence of temperature dependence of BETNEDGE.

© 2023 Cadence Design Systems, Inc.

842	`stbetedgew=0.0`	Width dependence of temperature dependence of BETNEDGE.
843	`stbetedgelw=0.0`	Area dependence of temperature dependence of BETNEDGE.
844	`stvfbedge=5.0e-4 V/K`	Temperature dependence of VFBEDGE.
845	`stvfbedgeo=5.0e-4 V/K`	Geometry-independent temperature dependence of VFBEDGE.
846	`stvfbedgel=0.0 V/K`	Length dependence of temperature dependence of VFBEDGE.
847	`stvfbedgew=0.0 V/K`	Width dependence of temperature dependence of VFBEDGE.
848	`stvfbedgelw=0.0 V/K`	Area dependence of temperature dependence of VFBEDGE.
849	`vfbedge=(-1.0) V`	Flat band voltage of edge transistors at TR.
850	`vfbedgeo=(-1.0) V`	Geometry-independent flat-band voltage of edge transistors at TR.
851	`wedge=1.0e-8 m`	Electrical width of edge transistor per side.
852	`wedgew=0.0`	Width dependence of edge WEDGE.
853	`w=10e-6 m`	Default width.
854	`l=10e-6 m`	Default length.
855	`nf=1`	Number of fingers, It served as the default value of instance nf.
856	`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
857	`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
858	`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
859	`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.
860	`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.

© 2023 Cadence Design Systems, Inc.

861	`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
862	`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
863	`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.
864	`vgbr_max=vgb_max V`	Maximum allowed reverse voltage cross gate and bulk.
865	`vbsr_max=vbs_max V`	Maximum allowed reverse voltage cross source and bulk.
866	`vbdr_max=vbd_max V`	Maximum allowed reverse voltage cross source/drain and bulk.
867	`vthmod`	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'. Possible values are `std` and `vthcc`.
868	`ivth (A)`	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
869	`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
870	`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
871	`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
872	`st2vfb=0.0` k^{-1}	Quadratic temperature dependence of VFB.
873	`thecs=2.0`	Coulomb scattering exponent at TR.

© 2023 Cadence Design Systems, Inc.

874	`stthecs=0.0`	Temperature dependence of THECS.
875	`post2vfb=0.0` k^{-1}	Coefficient for the geometry-independent part of ST2VFB.
876	`potthecs=2.0`	Coefficient for the geometry-independent part of THECS.
877	`postthecs=0.0`	Coefficient for the geometry-independent part of STTHECS.
878	`st2vfb0=0.0` k^{-1}	Quadratic temperature dependence of VFB.
879	`thecso=2.0`	Coulomb scattering exponent at TR.
880	`stthecso=0.0`	Temperature dependence of THECS.
881	`ctg=0.0`	Gate voltage dependence of interface states factor.
882	`ctb=0.0`	Bulk voltage dependence of interface states factor.
883	`stct=1.0`	Geometry-independent temperature dependence of CT.
884	`poctg=0.0`	Coefficient for the geometry-independent part of CTG.
885	`poctb=0.0`	Coefficient for the geometry-independent part of CTB.
886	`postct=1.0`	Coefficient for the geometry-independent part of STCT.
887	`ctbo=0.0`	Bulk voltage dependence of interface states factor.
888	`stcto=1.0`	Geometry-independent temperature dependence of CT.
889	`ctgo=0.0`	Gate voltage dependence of interface states factor.
890	`nsubedgelexp=1.0`	Exponent for length dependence of edge transistor substrate doping.
891	`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, `mica`, `tispice` and `pspice`.

© 2023 Cadence Design Systems, Inc.

Output Parameters

1	`weff (m)`	Effective channel width for geometrical models.
2	`leff (m)`	Effective channel length for geometrical models.
3	`lp_stvfb (V/K)`	Local parameter STVFB after clipping.
4	`lp_tox (m)`	Local parameter TOX after clipping.
5	`lp_epsrox`	Local parameter EPSROX after clipping.
6	`lp_neff (m`$^{-3}$`)`	Local parameter NEFF after clipping.
7	`lp_facneffac`	Local parameter FACNEFFAC after clipping.
8	`lp_gfacnud`	Local parameter GFACNUD after clipping.
9	`lp_vsbnud (V)`	Local parameter VSBNUD after clipping.
10	`lp_dvsbnud (V)`	Local parameter DVSBNUD after clipping.
11	`lp_vnsub (V)`	Local parameter VNSUB after clipping.
12	`lp_nslp (V)`	Local parameter NSLP after clipping.
13	`lp_dnsub (V^-1)`	Local parameter DNSUB after clipping.
14	`lp_dphib (V)`	Local parameter DPHIB after clipping.
15	`lp_delvtac (V)`	Local parameter DELVTAC after clipping.
16	`lp_np (m`$^{-3}$`)`	Local parameter NP after clipping.
17	`lp_toxov (m)`	Local parameter TOXOV after clipping.
18	`lp_toxovd (m)`	Local parameter TOXOVD after clipping.
19	`lp_nov (m`$^{-3}$`)`	Local parameter NOV after clipping.
20	`lp_novd (m`$^{-3}$`)`	Local parameter NOVD after clipping.
21	`lp_cf`	Local parameter CF after clipping.
22	`lp_cfd (V^-1)`	Local parameter CFD after clipping.
23	`lp_cfb (V^-1)`	Local parameter CFB after clipping.
24	`lp_psce`	Local parameter PSCE after clipping.
25	`lp_psceb (V^-1)`	

© 2023 Cadence Design Systems, Inc.

		Local parameter PSCEB after clipping.
26	`lp_psced (V^-1)`	
		Local parameter PSCED after clipping.
27	`lp_stbet`	Local parameter STBET after clipping.
28	`lp_stmue`	Local parameter STMUE after clipping.
29	`lp_stthemu`	Local parameter STTHEMU after clipping.
30	`lp_stcs`	Local parameter STCS after clipping.
31	`lp_stxcor`	Local parameter STXCOR after clipping.
32	`lp_feta`	Local parameter FETA after clipping.
33	`lp_strs`	Local parameter STRS after clipping.
34	`lp_rsb (V^-1)`	Local parameter RSB after clipping.
35	`lp_rsg (V^-1)`	Local parameter RSG after clipping.
36	`lp_stthesat`	Local parameter STTHESAT after clipping.
37	`lp_thesatb (V^-1)`	
		Local parameter THESATB after clipping.
38	`lp_thesatg (V^-1)`	
		Local parameter THESATG after clipping.
39	`lp_ax`	Local parameter AX after clipping.
40	`lp_alp`	Local parameter ALP after clipping.
41	`lp_alp1 (V)`	Local parameter ALP1 after clipping.
42	`lp_alp2 (V^-1)`	Local parameter ALP2 after clipping.
43	`lp_vp (V)`	Local parameter VP after clipping.
44	`lp_a1`	Local parameter A1 after clipping.
45	`lp_sta2`	Local parameter STA2 after clipping.
46	`lp_a3`	Local parameter A3 after clipping.
47	`lp_a4 (m`$^{-3}$`)`	
		Local parameter A4 after clipping.
48	`lp_gco`	Local parameter GCO after clipping.
49	`lp_iginv (A)`	Local parameter IGINV after T-scaling and clipping.

© 2023 Cadence Design Systems, Inc.

50	lp_igov (A)	Local parameter IGOV after T-scaling and clipping.
51	lp_igovd (A)	Local parameter IGOVD after T-scaling and clipping.
52	lp_stig	Local parameter STIG after clipping.
53	lp_gc2	Local parameter GC2 after clipping.
54	lp_gc3	Local parameter GC3 after clipping.
55	lp_chib (V)	Local parameter CHIB after clipping.
56	lp_agidl (A/V^3)	Local parameter AGIDL after clipping.
57	lp_agidld (A/V^3)	Local parameter AGIDLD after clipping.
58	lp_bgidl (V)	Local parameter BGIDL after T-scaling and clipping.
59	lp_bgidld (V)	Local parameter BGIDLD after T-scaling and clipping.
60	lp_stbgidl (V/K)	Local parameter STBGIDL after clipping.
61	lp_stbgidld (V/K)	Local parameter STBGIDLD after clipping.
62	lp_cgidl	Local parameter CGIDL after clipping.
63	lp_cgidld	Local parameter CGIDLD after clipping.
64	lp_cox (F)	Local parameter COX after clipping.
65	lp_cgov (F)	Local parameter CGOV after clipping.
66	lp_cgovd (F)	Local parameter CGOVD after clipping.
67	lp_cgbov (F)	Local parameter CGBOV after clipping.
68	lp_cfr (F)	Local parameter CFR after clipping.
69	lp_cfrd (F)	Local parameter CFRD after clipping.
70	lp_fnt	Local parameter FNT after clipping.
71	lp_fntexc	Local parameter FNTEXC after clipping.
72	lp_nfa ($1/(V\ m^4)$)	Local parameter NFA after clipping.
73	lp_nfb ($1/(V\ m^2)$)	

© 2023 Cadence Design Systems, Inc.

		Local parameter NFB after clipping.
74	lp_nfc (V^-1)	Local parameter NFC after clipping.
75	lp_ef	Local parameter EF after clipping.
76	lp_rg (Ω)	Local parameter RG after clipping.
77	lp_rse (Ω)	Local parameter RSE after clipping.
78	lp_rde (Ω)	Local parameter RDE after clipping.
79	lp_rbulk (Ω)	Local parameter RBULK after clipping.
80	lp_rwell (Ω)	Local parameter RWELL after clipping.
81	lp_rjuns (Ω)	Local parameter RJUNS after clipping.
82	lp_rjund (Ω)	Local parameter RJUND after clipping.
83	lp_rth (K/W)	Local parameter RTH after T-scaling and clipping.
84	lp_cth (J/K)	Local parameter CTH after clipping.
85	lp_strth	Local parameter STRTH after clipping.
86	lp_vfbedge (V)	Local parameter VFBEDGE after T-scaling and clipping.
87	lp_stvfbedge (V/K)	Local parameter STVFBEDGE after clipping.
88	lp_dphibedge (V)	Local parameter DPHIBEDGE after clipping.
89	lp_neffedge (m^{-3})	Local parameter NEFFEDGE after clipping.
90	lp_ctedge	Local parameter CTEDGE after clipping.
91	lp_betnedge (m^2/V/s)	Local parameter BETNEDGE after T-scaling and clipping.
92	lp_stbetedge	Local parameter STBETEDGE after clipping.
93	lp_psceedge	Local parameter PSCEEDGE after clipping.
94	lp_pscebedge (V^-1)	

© 2023 Cadence Design Systems, Inc.

		Local parameter PSCEBEDGE after clipping.
95	`lp_pscededge (V^-1)`	
		Local parameter PSCEDEDGE after clipping.
96	`lp_cfedge (V)`	Local parameter CFEDGE after clipping.
97	`lp_cfdedge ( V^-1)`	
		Local parameter CFDEDGE after clipping.
98	`lp_cfbedge ( V^-1)`	
		Local parameter CFBEDGE after clipping.
99	`lp_fntedge ( )`	Local parameter FNTEDGE after clipping.
100	`lp_nfaedge ( 1/(V m^4))`	
		Local parameter NFAEDGE after clipping.
101	`lp_nfbedge ( 1/(V m^4))`	
		Local parameter NFBEDGE after clipping.
102	`lp_nfcedge ( V^-1)`	
		Local parameter NFCEDGE after clipping.
103	`lp_efedge`	Local parameter EFEDGE after clipping.
104	`cjosbot (F)`	Bottom component of total zero-bias source junction capacitance at device temperature.
105	`cjossti (F)`	STI-edge component of total zero-bias source junction capacitance at device temperature.
106	`cjosgat (F)`	Gate-edge component of total zero-bias source junction capacitance at device temperature.
107	`vbisbot (V)`	Built-in voltage of source-side bottom junction at device temperature.
108	`vbissti (V)`	Built-in voltage of source-side STI-edge junction at device temperature.
109	`vbisgat (V)`	Built-in voltage of source-side gate-edge junction at device temperature.
110	`idsatsbot (A)`	Total source-side bottom junction saturation current.

© 2023 Cadence Design Systems, Inc.

111	idsatssti (A)	Total source-side STI-edge junction saturation current.
112	idsatsgat (A)	Total source-side gate-edge junction saturation current.
113	cjosbotd (F)	Bottom component of total zero-bias drain junction capacitance at device temperature.
114	cjosstid (F)	STI-edge component of total zero-bias drain junction capacitance at device temperature.
115	cjosgatd (F)	Gate-edge component of total zero-bias drain junction capacitance at device temperature.
116	vbisbotd (V)	Built-in voltage of drain-side bottom junction at device temperature.
117	vbisstid (V)	Built-in voltage of drain-side STI-edge junction at device temperature.
118	vbisgatd (V)	Built-in voltage of drain-side gate-edge junction at device temperature.
119	idsatsbotd (A)	Total drain-side bottom junction saturation current.
120	idsatsstid (A)	Total drain-side STI-edge junction saturation current.
121	idsatsgatd (A)	Total drain-side gate-edge junction saturation current.
122	lp_munqs	Local parameter MUNQS after clipping.
123	lv2 (m)	Alias of w.
124	lv1 (m)	Alias of l.
125	lv3 (m^2)	Alias of ad.
126	lv4 (m^2)	Alias of as.
127	lv11 (m)	Alias of pd.
128	lv12 (m)	Alias of ps.
129	tempeff (C)	Effective temperature for a single device.
130	meff	Effective multiplicity factor (m-factor).
131	lp_st2vfb (K^-1)	Local parameter ST2VFB after clipping.
132	lp_stthecs	Local parameter STTHECS after clipping.
133	lp_ctb	Local parameter CTB after clipping.
134	lp_stct	Local parameter STCT after clipping.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters
Parameters

1	`region=triode`	Estimated operating region. %Z outputs the number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
2	`ctype`	Flag for channel type.
3	`sdint`	Flag for source-drain interchange.
4	`ise (A)`	Total source current.
5	`ige (A)`	Total gate current.
6	`ide (A)`	Total drain current.
7	`ibe (A)`	Total bulk current.
8	`is (A)`	Total source current.
9	`ig (A)`	Total gate current.
10	`id (A)`	Total drain current.
11	`ib (A)`	Total bulk current.
12	`ids (A)`	Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents.
13	`idb (A)`	Drain to bulk current.
14	`isb (A)`	Source to bulk current.
15	`igs (A)`	Gate-source tunneling current.
16	`igd (A)`	Gate-drain tunneling current.
17	`igb (A)`	Gate-bulk tunneling current.
18	`idedge (A)`	Drain current of edge transistors.
19	`igcs (A)`	Gate-channel tunneling current (source component).
20	`igcd (A)`	Gate-channel tunneling current (drain component).
21	`iavl (A)`	Substrate current due to weak avalanche.
22	`igisl (A)`	Gate-induced source leakage current.
23	`igidl (A)`	Gate-induced drain leakage current.
24	`ijs (A)`	Total source junction current.

© 2023 Cadence Design Systems, Inc.

25	`ijsbot (A)`	Source junction current (bottom component).
26	`ijsgat (A)`	Source junction current (gate-edge component).
27	`ijssti (A)`	Source junction current (STI-edge component).
28	`ijd (A)`	Total drain junction current.
29	`ijdbot (A)`	Drain junction current (bottom component).
30	`ijdgat (A)`	Drain junction current (gate-edge component).
31	`ijdsti (A)`	Drain junction current (STI-edge component).
32	`qg (Coul)`	Intrinsic gate charge.
33	`qd (Coul)`	Intrinsic drain charge.
34	`qb (Coul)`	Intrinsic bulk charge.
35	`qs (Coul)`	Intrinsic source charge.
36	`qgs_ov (Coul)`	Overlap charge for gate-source.
37	`qgd_ov (Coul)`	Overlap charge for gate-drain.
38	`qfgs (Coul)`	Total outerFringe + overlap for gate-source.
39	`qfgd (Coul)`	Total outerFringe + overlap for gate-drain.
40	`qgb_ov (Coul)`	Gate-bulk overlap charge.
41	`qjun_s (Coul)`	Junction charge on source side.
42	`qjun_d (Coul)`	Junction charge on drain side.
43	`vds (V)`	Drain-source voltage.
44	`vgs (V)`	Gate-source voltage.
45	`vgd (V)`	Gate-drain voltage.
46	`vsb (V)`	Source-bulk voltage.
47	`vdb (V)`	Drain-bulk voltage.
48	`vth0 (V)`	Zero-bias threshold voltage.
49	`vto (V)`	Zero-bias threshold voltage.
50	`vts (V)`	Threshold voltage including back bias effects.
51	`vth (V)`	Threshold voltage including back bias and drain bias effects.

© 2023 Cadence Design Systems, Inc.

52	`vgt (V)`	Effective gate drive voltage including back bias and drain bias effects.
53	`vth_drive (V)`	Effective gate drive voltage including back bias and drain bias effects. Alias for Vgt..
54	`vdss (V)`	Drain saturation voltage at actual bias.
55	`vdsat (V)`	Drain saturation voltage at actual bias.
56	`vsat`	Saturation limit.
57	`vdsat_marg`	Saturation limit.
58	`pwr (W)`	Power at op point.
59	`gm (1/Ω)`	Transconductance.
60	`gmb (1/Ω)`	Substrate transconductance.
61	`go (1/Ω)`	Output conductance.
62	`gds (1/Ω)`	Output conductance.
63	`gjs (1/Ω)`	Source junction conductance.
64	`gjd (1/Ω)`	Drain junction conductance.
65	`cdd (F)`	Drain capacitance.
66	`cdg (F)`	Drain-gate capacitance.
67	`cds (F)`	Drain-source capacitance.
68	`cdb (F)`	Drain-bulk capacitance.
69	`cgd (F)`	Gate-drain capacitance.
70	`cgg (F)`	Gate capacitance.
71	`cgs (F)`	Gate-source capacitance.
72	`cgb (F)`	Gate-bulk capacitance.
73	`csd (F)`	Source-drain capacitance.
74	`csg (F)`	Source-gate capacitance.
75	`css (F)`	Source capacitance.
76	`csb (F)`	Source-bulk capacitance.
77	`cbd (F)`	Bulk-drain capacitance.
78	`cbg (F)`	Bulk-gate capacitance.

© 2023 Cadence Design Systems, Inc.

79	`cbs (F)`	Bulk-source capacitance.
80	`cbb (F)`	Bulk capacitance.
81	`co (F)`	Output Drain-Source capacitance.
82	`cm (F)`	Capacitance element 1 for QS model.
83	`cmb (F)`	Capacitance element 2 for QS model.
84	`cmx (F)`	Capacitance element 3 for QS model.
85	`tau1 (s)`	Time constant related to NQS first frequency pole.
86	`fqslim (Hz)`	QS model frequency limit.
87	`cgsol (F)`	Total gate-source overlap capacitance.
88	`cgdol (F)`	Total gate-drain overlap capacitance.
89	`cgbol (F)`	Total gate-bulk overlap capacitance.
90	`cjs (F)`	Total source junction capacitance.
91	`cjsbot (F)`	Source junction capacitance (bottom component).
92	`cjsgat (F)`	Source junction capacitance (gate-edge component).
93	`cjssti (F)`	Source junction capacitance (STI-edge component).
94	`cjd (F)`	Total drain junction capacitance.
95	`cjdbot (F)`	Drain junction capacitance (bottom component).
96	`cjdgat (F)`	Drain junction capacitance (gate-edge component).
97	`cjdsti (F)`	Drain junction capacitance (STI-edge component).
98	`lpoly (m)`	Length of poly.
99	`u`	Transistor gain.
100	`self_gain`	Transistor gain.
101	`rout (Ω)`	Small-signal output resistance.
102	`vearly (V)`	Equivalent early voltage.
103	`beff (A/V`^{2}`)`	Gain factor.
104	`GmoverI (1/V)`	Transconductance efficiency.
105	`fug (Hz)`	Unity gain frequency at actual bias.
106	`ft (Hz)`	Unity gain frequency at actual bias.
107	`rg (Ω)`	Gate resistance.

© 2023 Cadence Design Systems, Inc.

108	rgate (Ω)	Gate resistance.
109	sfl	Flicker noise current density at 1 Hz.
110	sqrtsff	Input-referred RMS white noise voltage density at 1 kHz.
111	sqrtsfw	Input-referred RMS white noise voltage density.
112	sid	White noise current density.
113	sig	Induced gate noise current density at 1 Hz.
114	cigid	Imaginary part of correlation coefficient between Sig and Sid.
115	noi_mid	
116	noi_mig	
117	noi_migid	
118	noi_cgeff	
119	noi_cigid	
120	fknee	Cross-over frequency above which white noise is dominant.
121	sigs	Gate-source current noise spectral density.
122	sigd	Gate-drain current noise spectral density.
123	siavl	Impact ionization current noise spectral density.
124	ssi	Total source junction current noise spectral density.
125	sdi	Total drain junction current noise spectral density.
126	sfledge (A^2/Hz)	Flicker noise current spectral density at 1 Hz of edge transistors.
127	sidedge (A^2/Hz)	White noise current spectral density of edge transistors.
128	lp_vfb (V)	Local parameter VFB after T-scaling and clipping.
129	lp_ct	Local parameter CT after clipping.
130	lp_betn (m^2/(V s)	

© 2023 Cadence Design Systems, Inc.

		Local parameter BETN after T-scaling and clipping.
131	lp_mue (m/V)	Local parameter MUE after T-scaling and clipping.
132	lp_themu	Local parameter THEMU after T-scaling and clipping.
133	lp_cs	Local parameter CS after T-scaling and clipping.
134	lp_xcor (V^-1)	Local parameter XCOR after T-scaling and clipping.
135	lp_rs (Ω)	Local parameter RS after T-scaling and clipping.
136	lp_thesat (V^-1)	Local parameter THESAT after T-scaling and clipping.
137	lp_a2 (V)	Local parameter A2 after T-scaling and clipping.
138	pdiss (W)	Power dissipation.
139	dtsh (K)	Temperature rise due to self heating.
140	tk (K)	Device Temperature.
141	vbs (V)	Bulk-source voltage.
142	lv13	Alias of nrd.
143	lv14	Alias of nrs.
144	lv36 (F)	Alias of cgsol.
145	lv37 (F)	Alias of cgdol.
146	lv38 (F)	Alias of cgbol.
147	lv51 (m)	Alias of tox.
148	lp_thecs	Local parameter THECS after T-scaling and clipping.
149	lp_ctg	Local parameter CTG after clipping.
150	lp_cfac	Local parameter CFAC after clipping.
151	lp_thesatac (V^-1)	Local parameter THESATAC after T-scaling and clipping.
152	lp_axac	Local parameter AXAC after clipping.
153	lp_alpac	Local parameter ALPAC after clipping.
154	lp_gc2ov	Local parameter GC2OV after clipping.
155	lp_gc3ov	Local parameter GC3OV after clipping.

© 2023 Cadence Design Systems, Inc.

156	`OPdef`	1: Device Physics notation. 2: Circuit Simulator notation.
157	`SDop`	Operation mode related to channel type and drain-source voltage sign. Possible values are `Forward` and `Reverse`.

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

GmoverI OP-104
idsatrstid M-705
phigstid M-702
pwgfacnud M-141
OPdef OP-165
idsatsbot O-110
pkuo M-634
pwiginv M-264
SDop OP-166
idsatsbotd O-119
pkvtho M-640
pwigov M-268
a1 M-68
idsatsgat O-112
pla1 M-248
pwigovd M-272
a1l M-551
idsatsgatd O-121
pla3 M-254
pwkuowe M-355
a1o M-550
idsatssti O-111
pla4 M-258
pwkvthowe M-351
a1w M-552
idsatsstid O-120
plagidl M-279
pwmue M-191
a2 M-69
ifactor I-35
plagidld M-283
pwneff M-133
a2o M-553
ig OP-9
plalp M-235
pwneffedge M-378
a3 M-71
igb OP-17
plalp1 M-239
pwnfa M-338
a3l M-556
igcd OP-20
plalp2 M-243
pwnfaedge M-407
a3o M-555
igcs OP-19
plalpac M-776
pwnfb M-342
a3w M-557
igd OP-16
plax M-231
pwnfbedge M-411

© 2023 Cadence Design Systems, Inc.

a4 M-72
a4l M-559
a4o M-558
a4w M-560
abdrain I-25
absource I-22
ad I-30
agidl M-81
agidld M-82
agidldw M-570
agidlw M-569
alp M-64
alp1 M-65
alp1l1 M-541
alp1l2 M-543
alp1lexp M-542
alp1w M-544
alp2 M-66
alp2l1 M-545
alp2l2 M-547
ige OP-5
igidl OP-23
iginv M-74
iginvlw M-562
igisl OP-22
igov M-75
igovd M-76
igovdw M-564
igovw M-563
igs OP-15
ijd OP-28
ijdbot OP-29
ijdgat OP-30
ijdsti OP-31
ijs OP-24
ijsbot OP-25
ijsgat OP-26
ijssti OP-27
imax M-648
is OP-8
plaxac M-772
plbetn M-182
plbetnedge M-385
plcf M-175
plcfac M-764
plcfd M-178
plcfedge M-399
plcfr M-309
plcfrd M-313
plcgbov M-305
plcgov M-297
plcgovd M-301
plcinr M-320
plcinrd M-324
plcox M-293
plcs M-197
plct M-161
plctedge M-381
pldelvtac M-153
pldphib M-149
pwnfc M-346
pwnfcedge M-415
pwnov M-168
pwnovd M-172
pwnp M-158
pwpsce M-363
pwpsceedge M-394
pwr OP-58
pwrs M-209
pwstbet M-187
pwstbetedge M-390
pwstthesat M-220
pwstvfb M-127
pwstvfbedge M-370
pwthesat M-216
pwthesatac M-769
pwthesatb M-224
pwthesatg M-228
pwvfb M-123
pwxcor M-203

© 2023 Cadence Design Systems, Inc.

alp2lexp M-546
alp2w M-548
alpac M-745
alpacl M-758
alpaclexp M-759
alpacw M-760
alpl M-538
alplexp M-539
alpnoi M-596
alpw M-540
as I-28
ax M-63
axac M-744
axacl M-757
axaco M-756
axinr M-103
axinro M-588
axl M-537
axo M-536
beff OP-103
isb OP-14
ise OP-4
isnoisy I-37
ivth M-866
ivth_vdsmin M-869
ivthl M-868
ivthw M-867
jw I-17
kuo M-629
kuowel M-602
kuowelw M-604
kuoweo M-601
kuowew M-603
kvsat M-630
kvsatac M-781
kvtho M-637
kvthowel M-598
kvthowelw M-600
kvthoweo M-597
kvthowew M-599
pldphibedge M-373
plfacneffac M-136
plfntexc M-333
plgfacnud M-140
pliginv M-263
pligov M-267
pligovd M-271
plkuowe M-354
plkvthowe M-350
plmue M-190
plneff M-132
plneffedge M-377
plnfa M-337
plnfaedge M-406
plnfb M-341
plnfbedge M-410
plnfc M-345
plnfcedge M-414
plnov M-167
plnovd M-171
qb OP-34
qd OP-33
qfgd OP-39
qfgs OP-38
qg OP-32
qgb_ov OP-40
qgd_ov OP-37
qgs_ov OP-36
qjun_d OP-42
qjun_s OP-41
qmc M-15
qs OP-35
rbulk M-114
rbulko M-613
rde M-113
region I-15
region OP-1
rg M-111
rg OP-107
rgate OP-108

© 2023 Cadence Design Systems, Inc.

betedgew M-784
betn M-44
betnedge M-782
betw1 M-496
betw2 M-497
bgidl M-83
bgidld M-84
bgidldo M-572
bgidlo M-571
cbb OP-80
cbbtbot M-677
cbbtbotd M-718
cbbtgat M-679
cbbtgatd M-720
cbbtsti M-678
cbbtstid M-719
cbd OP-77
cbg OP-78
cbs OP-79
cdb OP-68
l I-1
l M-852
lap M-421
leff O-2
level M-1
lgdrain I-27
lgsource I-24
lintnoi M-595
lkuo M-632
lkvtho M-638
llodkuo M-635
llodvth M-641
lmax M-358
lmin M-357
lodetao M-644
lov M-481
lovd M-482
lp1 M-492
lp1w M-493
lp2 M-495
plnp M-157
plpsce M-362
plpsceedge M-393
plrs M-208
plstbet M-186
plstbetedge M-389
plstthesat M-219
plstvfb M-126
plstvfbedge M-369
plthesat M-215
plthesatac M-768
plthesatb M-223
plthesatg M-227
plvfb M-122
plwa1 M-250
plwa3 M-256
plwa4 M-260
plwagidl M-281
plwagidld M-285
plwalp M-237
rgo M-606
rint M-607
rjund M-117
rjundo M-616
rjuns M-116
rjunso M-615
rout OP-101
rs M-55
rsb M-57
rsbo M-523
rse M-112
rsg M-58
rsgo M-524
rsh M-611
rshd M-612
rshg M-609
rsw1 M-520
rsw2 M-521
rth M-118
rthlw M-620

© 2023 Cadence Design Systems, Inc.

cdd OP-65
cdg OP-66
cds OP-67
cf M-42
cfac M-742
cfacl M-748
cfaclexp M-749
cfactor I-36
cfacw M-750
cfb M-43
cfbedge M-785
cfbedgeo M-786
cfbo M-488
cfd M-787
cfdedge M-788
cfdedgeo M-789
cfdo M-790
cfedge M-791
cfedgel M-792
cfedgelexp M-793
lp_a1 O-44
lp_a2 OP-137
lp_a3 O-46
lp_a4 O-47
lp_agidl O-56
lp_agidld O-57
lp_alp O-40
lp_alp1 O-41
lp_alp2 O-42
lp_alpac OP-162
lp_ax O-39
lp_axac OP-161
lp_axinr OP-146
lp_betn OP-130
lp_betnedge O-91
lp_bgidl O-58
lp_bgidld O-59
lp_cf O-21
lp_cfac OP-159
lp_cfb O-23
plwalp1 M-241
plwalp2 M-245
plwalpac M-778
plwax M-233
plwaxac M-774
plwbetn M-184
plwbetnedge M-387
plwcf M-177
plwcfac M-766
plwcfedge M-401
plwcfr M-311
plwcfrd M-315
plwcgbov M-307
plwcgov M-299
plwcgovd M-303
plwcinr M-322
plwcinrd M-326
plwcox M-295
plwcs M-199
plwct M-163
rtho M-617
rthw1 M-618
rthw2 M-619
rvpoly M-608
rwell M-115
rwello M-614
sa I-3
saref M-626
sb I-4
sbref M-627
sc I-9
sca I-6
scb I-7
scc I-8
scref M-645
sd I-5
sdi OP-125
sdint OP-3
self_gain OP-100
sfl OP-109

© 2023 Cadence Design Systems, Inc.

cfedgew M-794
cfl M-485
cflexp M-486
cfr M-93
cfrd M-94
cfrdw M-579
cfrw M-578
cfw M-487
cgb OP-72
cgbol OP-89
cgbov M-92
cgbovl M-577
cgd OP-69
cgdol OP-88
cgg OP-70
cgidl M-87
cgidld M-88
cgidldo M-576
cgidlo M-575
lp_cfbedge O-98
lp_cfd O-22
lp_cfdedge O-97
lp_cfedge O-96
lp_cfr O-68
lp_cfrd O-69
lp_cgbov O-67
lp_cgidl O-62
lp_cgidld O-63
lp_cgov O-65
lp_cgovaccg OP-140
lp_cgovd O-66
lp_chib O-55
lp_cinr OP-141
lp_cinrd OP-142
lp_cox O-64
lp_cs OP-133
lp_ct OP-129
lp_ctb O-133
plwctedge M-383
plwdelvtac M-155
plwdphib M-151
plwdphibedge M-375
plwfacneffac M-138
plwfntexc M-335
plwgfacnud M-142
plwiginv M-265
plwigov M-269
plwigovd M-273
plwkuowe M-356
plwkvthowe M-352
plwmue M-192
plwneff M-134
plwneffedge M-379
plwnfa M-339
plwnfaedge M-408
plwnfb M-343
plwnfbedge M-412
sfledge OP-126
siavl OP-123
sid OP-112
sidedge OP-127
sig OP-113
sigd OP-122
sigs OP-121
sqrtsff OP-110
sqrtsfw OP-111
ssi OP-124
st2vfb M-870
st2vfbo M-876
sta2 M-70
sta2o M-554
stbet M-45
stbetedge M-783
stbetedgel M-839
stbetedgelw M-841
stbetedgeo M-838

© 2023 Cadence Design Systems, Inc.

cgov M-90
cgovaccg M-97
cgovaccgo M-582
cgovd M-91
cgs OP-71
cgsol OP-87
chib M-80
chibo M-568
cigid OP-114
cinr M-98
cinrd M-99
cinrdw M-584
cinrw M-583
cjd OP-94
cjdbot OP-95
cjdgat OP-96
cjdsti OP-97
cjorbot M-651
lp_ctedge O-90
lp_ctg OP-158
lp_cth O-84
lp_delvtac O-15
lp_dnsub O-13
lp_dphib O-14
lp_dphibedge O-88
lp_dvfbinr OP-143
lp_dvsbnud O-10
lp_ef O-75
lp_efedge O-103
lp_epsrox O-5
lp_facneffac O-7
lp_fcgovacc OP-138
lp_fcgovaccd OP-139
lp_fcinracc OP-145
lp_fcinrdep OP-144
lp_feta O-32
plwnfc M-347
plwnfcedge M-416
plwnov M-169
plwnovd M-173
plwnp M-159
plwpsce M-364
plwpsceedge M-395
plwrs M-210
plwstbet M-188
plwstbetedge M-391
plwstthesat M-221
plwstvfb M-128
plwstvfbedge M-371
plwthesat M-217
plwthesatac M-770
plwthesatb M-225
plwthesatg M-229
plwvfb M-124
stbetedgew M-840
stbetl M-500
stbetlw M-502
stbeto M-499
stbetw M-501
stbgidl M-85
stbgidld M-86
stbgidldo M-574
stbgidlo M-573
stcs M-51
stcso M-513
stct M-881
stcto M-886
stetao M-643
stfbbtbot M-683
stfbbtbotd M-724
stfbbtgat M-685
stfbbtgatd M-726

© 2023 Cadence Design Systems, Inc.

cjorbotd M-692
cjorgat M-653
cjorgatd M-694
cjorsti M-652
cjorstid M-693
cjosbot O-104
cjosbotd O-113
cjosgat O-106
cjosgatd O-115
cjossti O-105
cjosstid O-114
cjs OP-90
cjsbot OP-91
cjsgat OP-92
cjssti OP-93
cm OP-82
cmb OP-83
cmx OP-84
co OP-81
compatible M-889
cox M-89
lp_fnt O-70
lp_fntedge O-99
lp_fntexc O-71
lp_gc2 O-53
lp_gc2ov OP-163
lp_gc3 O-54
lp_gc3ov OP-164
lp_gco O-48
lp_gfacnud O-8
lp_iginv O-49
lp_igov O-50
lp_igovd O-51
lp_mue OP-131
lp_munqs O-122
lp_neff O-6
lp_neffedge O-89
lp_nfa O-72
lp_nfaedge O-100
lp_nfb O-73
lp_nfbedge O-101
lp_nfc O-74
plwxcor M-204
plxcor M-202
poa1 M-247
poa2 M-251
poa3 M-253
poa4 M-257
poagidl M-278
poagidld M-282
poalp M-234
poalp1 M-238
poalp2 M-242
poalpac M-775
poax M-230
poaxac M-771
poaxinr M-330
pobetn M-181
pobetnedge M-384
pobgidl M-286
pobgidld M-287
pocf M-174
pocfac M-763
stfbbtsti M-684
stfbbtstid M-725
stig M-77
stigo M-565
stmue M-47
stmueo M-505
strs M-56
strso M-522
strth M-120
strtho M-625
stthecs M-872
stthecso M-878
stthemu M-49
stthemuo M-507
stthesat M-60
stthesatl M-531
stthesatlw M-533
stthesato M-530
stthesatw M-532
stvfb M-23
stvfbedge M-842

© 2023 Cadence Design Systems, Inc.

cs M-50
csb OP-76
csd OP-73
csg OP-74
csl M-509
cslexp M-510
cslw M-512
cso M-508
csrhbot M-666
csrhbotd M-707
csrhgat M-668
csrhgatd M-709
csrhsti M-667
csrhstid M-708
css OP-75
csw M-511
ct M-37
ctatbot M-671
ctatbotd M-712
ctatgat M-673
lp_nfcedge O-102
lp_nov O-19
lp_novd O-20
lp_np O-16
lp_nslp O-12
lp_psce O-24
lp_psceb O-25
lp_pscebedge O-94
lp_psced O-26
lp_pscededge O-95
lp_psceedge O-93
lp_rbulk O-79
lp_rde O-78
lp_rg O-76
lp_rjund O-82
lp_rjuns O-81
lp_rs OP-135
lp_rsb O-34
lp_rse O-77
lp_rsg O-35
pocfb M-180
pocfbedge M-403
pocfd M-179
pocfdedge M-402
pocfedge M-398
pocfr M-308
pocfrd M-312
pocgbov M-304
pocgidl M-290
pocgidld M-291
pocgov M-296
pocgovaccg M-318
pocgovd M-300
pochib M-277
pocinr M-319
pocinrd M-323
pocox M-292
pocs M-196
poct M-160
poctb M-883
stvfbedgel M-844
stvfbedgelw M-846
stvfbedgeo M-843
stvfbedgew M-845
stvfbl M-433
stvfblw M-435
stvfbo M-432
stvfbw M-434
stxcor M-53
stxcoro M-518
swdelvtac M-13
swedge M-12
swgeo M-5
swgidl M-8
swigate M-6
swign M-14
swimpact M-7
swjunasym M-10
swjuncap M-9
swjunexp M-733

© 2023 Cadence Design Systems, Inc.

ctatgatd M-714
ctatsti M-672
ctatstid M-713
ctb M-880
ctbo M-885
ctedge M-795
ctedgel M-797
ctedgelexp M-798
ctedgeo M-796
ctg M-879
ctgo M-887
cth M-119
cthlw M-624
ctho M-621
cthw1 M-622
cthw2 M-623
ctl M-475
ctlexp M-476
ctlw M-478
lp_rth O-83
lp_rwell O-80
lp_st2vfb O-131
lp_sta2 O-45
lp_stbet O-27
lp_stbetedge O-92
lp_stbgidl O-60
lp_stbgidld O-61
lp_stcs O-30
lp_stct O-134
lp_stig O-52
lp_stmue O-28
lp_strs O-33
lp_strth O-85
lp_stthecs O-132
lp_stthemu O-29
lp_stthesat O-36
lp_stvfb O-3
lp_stvfbedge O-87
poctedge M-380
poctg M-882
podelvtac M-152
podnsub M-147
podphib M-148
podphibedge M-372
podvfbinr M-327
podvsbnud M-144
poef M-348
poefedge M-417
poepsrox M-130
pofacneffac M-135
pofcgovacc M-316
pofcgovaccd M-317
pofcinracc M-329
pofcinrdep M-328
pofeta M-206
pofnt M-331
pofntedge M-404
swnqs M-4
swnud M-11
swqpart M-741
swqsat M-740
tau1 OP-85
tempeff O-129
thecs M-871
thecso M-877
themu M-48
themuo M-506
thesat M-59
thesatac M-743
thesatacl M-752
thesataclexp M-753
thesataclw M-755
thesataco M-751
thesatacw M-754
thesatb M-61
thesatbo M-534

© 2023 Cadence Design Systems, Inc.

cto M-474
ctw M-477
ctype OP-2
delvtac M-35
delvtacl M-468
delvtaclexp M-469
delvtaclw M-471
delvtaco M-467
delvtacw M-470
delvto I-18
delvtoedge I-20
dlq M-426
dlsil M-610
dnsub M-33
dnsubo M-461
dphib M-34
dphibedge M-799
dphibedgel M-801
dphibedgelexp M-802
lp_stxcor O-31
lp_thecs OP-157
lp_themu OP-132
lp_thesat OP-136
lp_thesatac OP-160
lp_thesatb O-37
lp_thesatg O-38
lp_tox O-4
lp_toxov O-17
lp_toxovd O-18
lp_vfb OP-128
lp_vfbedge O-86
lp_vnsub O-11
lp_vp O-43
lp_vsbnud O-9
lp_xcor OP-134
lpck M-444
lpckw M-445
lpedge M-810
pofntexc M-332
pogc2 M-275
pogc2ov M-779
pogc3 M-276
pogc3ov M-780
pogco M-261
pogfacnud M-139
poiginv M-262
poigov M-266
poigovd M-270
pokuowe M-353
pokvthowe M-349
pomue M-189
poneff M-131
poneffedge M-376
ponfa M-336
ponfaedge M-405
ponfb M-340
ponfbedge M-409
thesatg M-62
thesatgo M-535
thesatl M-526
thesatlexp M-527
thesatlw M-529
thesato M-525
thesatw M-528
tk OP-149
tkuo M-631
tox M-24
toxo M-436
toxov M-38
toxovd M-39
toxovdo M-480
toxovo M-479
tr M-3
trise I-16
trj M-649
type M-2

© 2023 Cadence Design Systems, Inc.

dphibedgelw M-804
dphibedgeo M-800
dphibedgew M-803
dphibl M-463
dphiblexp M-464
dphiblw M-466
dphibo M-462
dphibw M-465
dta M-738
dtsh OP-148
dvfbinr M-100
dvfbinro M-585
dvsbnud M-30
dvsbnudo M-458
dwq M-427
ef M-109
efedge M-805
efedgeo M-806
efo M-594
lpoly OP-98
lsdrain I-26
lssource I-23
lv1 O-124
lv11 O-127
lv12 O-128
lv13 OP-151
lv14 OP-152
lv2 O-123
lv3 O-125
lv36 OP-153
lv37 OP-154
lv38 OP-155
lv4 O-126
lv51 OP-156
lvarl M-419
lvaro M-418
lvarw M-420
m I-34
ponfc M-344
ponfcedge M-413
ponov M-166
ponovd M-170
ponp M-156
ponslp M-146
popsce M-361
popsceb M-365
popscebedge M-396
popsced M-366
popscededge M-397
popsceedge M-392
pors M-207
porsb M-212
porsg M-213
post2vfb M-873
posta2 M-252
postbet M-185
postbetedge M-388
u OP-99
uo M-489
vbd_max M-857
vbdr_max M-864
vbirbot M-654
vbirbotd M-695
vbirgat M-656
vbirgatd M-697
vbirsti M-655
vbirstid M-696
vbisbot O-107
vbisbotd O-116
vbisgat O-109
vbisgatd O-118
vbissti O-108
vbisstid O-117
vbrbot M-686
vbrbotd M-727
vbrgat M-688

© 2023 Cadence Design Systems, Inc.

epsrox M-25
epsroxo M-437
facneffac M-27
facneffacl M-449
facneffaclw M-451
facneffaco M-448
facneffacw M-450
factuo I-19
factuoedge I-21
fbbtrbot M-680
fbbtrbotd M-721
fbbtrgat M-682
fbbtrgatd M-723
fbbtrsti M-681
fbbtrstid M-722
fbet1 M-490
fbet1w M-491
fbet2 M-494
fbetedge M-807
mbe M-20
mbeo M-21
meff O-130
mefftatbot M-674
mefftatbotd M-715
mefftatgat M-676
mefftatgatd M-717
mefftatsti M-675
mefftatstid M-716
minr M-17
mue M-46
mueo M-503
muew M-504
mulid0 I-33
mult I-32
munqs M-110
munqso M-605
mvt M-18
mvto M-19
postbgidl M-288
postbgidld M-289
postcs M-200
postct M-884
postig M-274
postmue M-193
postrs M-211
postthecs M-875
postthemu M-195
postthesat M-218
postvfb M-125
postvfbedge M-368
postxcor M-205
pothecs M-874
pothemu M-194
pothesat M-214
pothesatac M-767
pothesatb M-222
pothesatg M-226
vbrgatd M-729
vbrsti M-687
vbrstid M-728
vbs OP-150
vbs_max M-858
vbsr_max M-863
vdb OP-47
vds OP-43
vds_max M-854
vdsat OP-55
vdsat_marg OP-57
vdss OP-54
vearly OP-102
version M-16
vfb M-22
vfbedge M-847
vfbedgeo M-848
vfbl M-429
vfblw M-431

© 2023 Cadence Design Systems, Inc.

fcgovacc M-95
fcgovaccd M-96
fcgovaccdo M-581
fcgovacco M-580
fcinracc M-102
fcinracco M-587
fcinrdep M-101
fcinrdepo M-586
feta M-54
fetao M-519
fjunq M-735
fjunqd M-737
fknee OP-120
fnt M-104
fntedge M-808
fntedgeo M-809
fntexc M-105
fntexcl M-590
fnto M-589
fol1 M-446
fol2 M-447
neff M-26
neffedge M-811
nf I-10
nf M-853
nfa M-106
nfaedge M-812
nfaedgelw M-813
nfalw M-591
nfb M-107
nfbedge M-814
nfbedgelw M-815
nfblw M-592
nfc M-108
nfcedge M-816
nfcedgelw M-817
nfclw M-593
ngcon I-11
noi_cgeff OP-118
noi_cigid OP-119
noi_mid OP-115
noi_mig OP-116
potox M-129
potoxov M-164
potoxovd M-165
povfb M-121
povfbedge M-367
povnsub M-145
povp M-246
povsbnud M-143
poxcor M-201
ps I-29
psce M-822
psceb M-823
pscebedge M-824
pscebedgeo M-825
pscebo M-826
psced M-827
pscededge M-828
pscededgeo M-830
pscedo M-829
psceedge M-831
psceedgel M-832
vfbo M-428
vfbw M-430
vgb_max M-859
vgbr_max M-862
vgd OP-45
vgd_max M-855
vgdr_max M-860
vgs OP-44
vgs_max M-856
vgsr_max M-861
vgt OP-52
vjunref M-734
vjunrefd M-736
vnsub M-31
vnsubo M-459
vp M-67
vpo M-549
vsat OP-56
vsb OP-46
vsbnud M-29
vsbnudo M-457

© 2023 Cadence Design Systems, Inc.

fqslim OP-86
noi_migid OP-117
psceedgelexp M-833
vth OP-51
frev M-650
noisemethod M-739
psceedgew M-834
vth0 OP-48
ft OP-106
nov M-40
pscel M-835
vth_drive OP-53
fug OP-105
novd M-41
pscelexp M-836
vthmod M-865
gc2 M-78
novdo M-484
pscew M-837
vto OP-49
gc2o M-566
novo M-483
psti M-658
vts OP-50
gc2ov M-746
np M-36
pstid M-699
w I-2
gc2ovo M-761
npck M-441
pwa1 M-249
w M-851
gc3 M-79
npckw M-442
pwa3 M-255
wbet M-498
gc3o M-567
npl M-473
pwa4 M-259
web M-646
gc3ov M-747
npo M-472
pwagidl M-280
wec M-647
gc3ovo M-762
nrd I-14
pwagidld M-284
wedge M-849
gco M-73
nrs I-13
pwalp M-236
wedgew M-850
gcoo M-561
nslp M-32
pwalp1 M-240
weff O-1
gds OP-62
nslpo M-460
pwalp2 M-244
wkuo M-633
gfacnud M-28
nsubedgel M-818
pwalpac M-777
wkvtho M-639
gfacnudl M-453
nsubedgelexp M-888
pwax M-232
wlod M-628
gfacnudlexp M-454
nsubedgelw M-820
pwaxac M-773
wlodkuo M-636
gfacnudlw M-456
nsubedgeo M-821
pwbetn M-183
wlodvth M-642

© 2023 Cadence Design Systems, Inc.

gfacnudo M-452
gfacnudw M-455
gjd OP-64
gjs OP-63
gm OP-59
gmb OP-60
go OP-61
iavl OP-21
ib OP-11
ibe OP-7
id OP-10
idb OP-13
ide OP-6
idedge OP-18
ids OP-12
idsatrbot M-663
idsatrbotd M-704
idsatrgat M-665
idsatrgatd M-706
idsatrsti M-664
nsubedgew M-819
nsubo M-438
nsubw M-439
pbot M-657
pbotd M-698
pbrbot M-689
pbrbotd M-730
pbrgat M-691
pbrgatd M-732
pbrsti M-690
pbrstid M-731
pd I-31
pdiss OP-147
pgat M-659
pgatd M-700
phigbot M-660
phigbotd M-701
phiggat M-662
phiggatd M-703
phigsti M-661
pwbetnedge M-386
pwcf M-176
pwcfac M-765
pwcfedge M-400
pwcfr M-310
pwcfrd M-314
pwcgbov M-306
pwcgov M-298
pwcgovd M-302
pwcinr M-321
pwcinrd M-325
pwcox M-294
pwcs M-198
pwct M-162
pwctedge M-382
pwdelvtac M-154
pwdphib M-150
pwdphibedge M-374
pwfacneffac M-137
pwfntexc M-334
wmax M-360
wmin M-359
wot M-425
wseg M-440
wsegp M-443
wvarl M-423
wvaro M-422
wvarw M-424
xcor M-52
xcorl M-515
xcorlw M-517
xcoro M-514
xcorw M-516
xgw I-12
xjungat M-670
xjungatd M-711
xjunsti M-669
xjunstid M-710

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

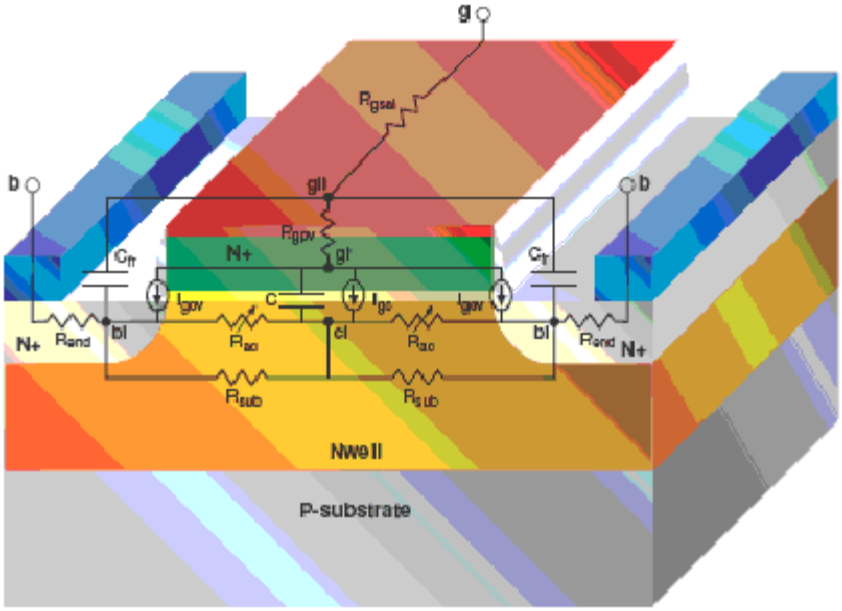
26

PSP-Based MOS Varactor Model (mosvar)

The PSP-based varactor model is intended for analog and radio-frequency circuit design. It includes dynamic inversion, finite poly doping, quantum mechanics, gate tunneling for different polarity combinations, and parasitics to model advanced MOS technologies.

Device Structure

The following figure shows a cross section of the standard MOS varactor offered in the current MOS technologies with its equivalent circuit model overlapped on it. g, bi and b are the external terminals while gii, gi and ci are the internal nodes.



© 2023 Cadence Design Systems, Inc.

The following table explains the meanings of the symbols in the above figure.

No.	Name	Description
1	C	Gate-channel capacitance
2	C_{fr}	Fringe and overlap capacitance
3	I_{gc}	Gate-channel current
4	I_{gov}	Gate-overlap current
5	R_{gsal}	Metal resistance
6	R_{gpv}	Poly gate resistance
7	R_{ac}	Accumulation resistance
8	R_{sub}	Substrate (in well region) resistance
9	R_{end}	End resistance

Related Topics

Model Equations

Model Version Updates

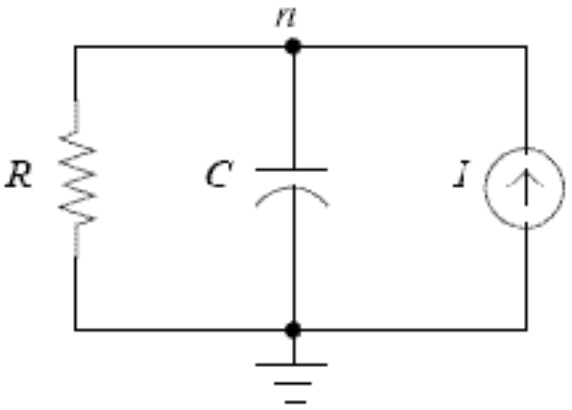
Model Usage

Component Statements

© 2023 Cadence Design Systems, Inc.

Model Equations

RC Circuit Model for Inversion Charge



(26-1)

$$q_i = q_i 0 - TAU \cdot \frac{dq_i}{dt}$$

Parameter Initializing

Capacitance of Oxide and Body Factors

(26-2)

$$C_{ox} = \varepsilon_{ox} \cdot (EPSROXO/3.9)/TOXO$$

© 2023 Cadence Design Systems, Inc.

(26-3)

$$\Upsilon s = \sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot NSUBO / C_{ox}}$$

$$\Upsilon p = \sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot NPO / C_{ox}}$$

$$\Upsilon ov,s = \sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot NOVO / C_{ox}}$$

If QMC>0,

(26-4)

$$q_q = \begin{cases} 0.4 \cdot QMN \cdot QMC \cdot (C_{ox})^{2/3} & if \text{ TYPE>0} \\ 0.4 \cdot QMP \cdot QMC \cdot (C_{ox})^{2/3} & otherwise \end{cases}$$

else

(26-5)

$q_q = 0.$

(26-6)

$$\eta_\mu = \begin{cases} 0.5 \cdot FETA & if \text{ TYPE} > 0 \\ \frac{1}{3} \cdot FETA & otherwise \end{cases}$$

$$norm_{tox} = TOXO / 10^{-9}$$

© 2023 Cadence Design Systems, Inc.

Initializing Parameters

Temperature-Related Parameters

(26-7)

$$\mathrm{TR1} = \begin{cases} \mathbf{TR}, & \text{if } \mathbf{TR} \geq -273 \\ -273, & \text{if } \mathbf{TR} < -273 \end{cases}$$

$$T_{\mathrm{KR}} = 273.15 + \mathrm{TR1}$$

$$T_{\mathrm{KD}} = \mathrm{T_A} + \mathbf{DTA}$$

$$\Delta T = T_{\mathrm{KD}} - T_{\mathrm{KR}}$$

$$\phi_{\mathrm{T}} = k_{\mathrm{B}} \cdot T_{\mathrm{KD}} / q$$

$$q_{\mathrm{lim2}} = 100 \cdot \phi_{\mathrm{T}}^2$$

$$V_{\mathrm{fb,\,T}} = \mathbf{VFBO} + \Delta T \cdot \mathbf{STVFB}$$

$$R_{\mathrm{shg,\,T}} = \mathbf{RSHG} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}} \right)^{\mathbf{STRSHG}}$$

$$R_{\mathrm{pv,\,T}} = \mathbf{RPV} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}} \right)^{\mathbf{STRPV}}$$

$$R_{\mathrm{end,\,T}} = \mathbf{REND} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}} \right)^{\mathbf{STREND}}$$

$$R_{\mathrm{shs,\,T}} = \mathbf{RSHS} \cdot \left(\frac{T_{\mathrm{KR}}}{T_{\mathrm{KD}}} \right)^{\mathbf{STRSHS}}$$

$$U_{\mathrm{ac,\,T}} = \mathbf{UAC} \cdot \left(\frac{T_{\mathrm{KD}}}{T_{\mathrm{KR}}} \right)^{\mathbf{STUAC}}$$

© 2023 Cadence Design Systems, Inc.

General Parameters

(26-8)

$$nt0 = 4 \cdot \text{`KBOL} \cdot T_{\text{KD}}$$

$$L_{\text{eff}} = L + \mathbf{DLQ}$$

$$W_{\text{eff}} = W + \mathbf{DWQ}$$

$$M_{\text{eff}} = \text{M_SEG} \cdot \text{` MFACTOR_USE}$$

$$\text{INV}_{\text{Meff}} = 1.0 \,/\, M_{\text{eff}}$$

$$E_{\text{g}} = 1.179 - T_{\text{KD}} \cdot \left(9.025 \cdot 10^{-5} + 3.05 \cdot 10^{-7} \cdot T_{\text{KD}}\right)$$

$$r_{\text{T}} = (1.045 + 4.5 \cdot 10^{-4} \cdot T_{\text{KD}}) \cdot (0.523 + 1.4 \cdot 10^{-3} \cdot T_{\text{KD}} - 1.48 \cdot 10^{-6} \cdot T_{\text{KD}}^2) \cdot \frac{T_{\text{KD}}^2}{90000}$$

$$\text{INV}_{\text{ni}} = 4 \cdot 10^{-26} \cdot r_{\text{T}}^{-0.75}$$

$$\phi_{\text{b}} = E_{\text{g}} + 2 \cdot \phi_{\text{T}} \cdot \ln\left(\mathbf{NSUBO} \cdot \text{INV}_{\text{ni}}\right)$$

$$k_{\text{se1}} = 230.26$$

$$k_{\text{se2}} = 460.52$$

© 2023 Cadence Design Systems, Inc.

Parameters Related to Polysilicon and Overlap Regions

(26-9)

$$G_{\mathrm{p}} = \gamma_{\mathrm{p}} / \sqrt{\phi_{\mathrm{T}}}$$

$$\xi_{\mathrm{p}} = 1 + G_{\mathrm{p}} / \sqrt{2}$$

$$w_{\mathrm{mrgp}} = 10^{-5} \cdot \xi_{\mathrm{p}}$$

$$\phi_{\mathrm{p}} = E_{\mathrm{g}} + 2 \cdot \phi_{\mathrm{T}} \cdot \ln\left(\mathbf{NPO} \cdot \mathrm{INV}_{\mathrm{ni}}\right)$$

$$w_{\mathrm{np}} = \phi_{\mathrm{p}} / \phi_{\mathrm{T}}$$

$$\Delta_{\mathrm{np}} = \begin{cases} \exp(-w_{\mathrm{np}}), & \text{if } w_{\mathrm{np}} < k_{\mathrm{se2}} \\ \dfrac{10^{-200}}{\mathrm{P3}\left(w_{\mathrm{np}} - k_{\mathrm{se2}}\right)}, & \text{otherwise} \end{cases}$$

$$G_{\mathrm{ov,\,s}} = \gamma_{\mathrm{ov,\,s}} / \sqrt{\phi_{\mathrm{T}}}$$

$$\xi_{\mathrm{ov,\,s}} = 1 + G_{\mathrm{ov,\,s}} / \sqrt{2}$$

$$w_{\mathrm{mrgov,\,s}} = 10^{-5} \cdot \xi_{\mathrm{ov,\,s}}$$

$$\phi_{\mathrm{b,\,ov}} = E_{\mathrm{g}} + 6 \cdot \phi_{\mathrm{T}}$$

$$w_1 = 1.25$$

$$w_{\mathrm{g1,\,ov}} = w_1 + G_{\mathrm{ov,\,s}} \cdot \sqrt{\exp(-w_1) + w_1 - 1}$$

© 2023 Cadence Design Systems, Inc.

Fringing Capacitance

(26-10)

$$C_{fr} = 2 \cdot (CFRW \cdot W + CFRL \cdot L)$$

© 2023 Cadence Design Systems, Inc.

Resistances

(26-11)

© 2023 Cadence Design Systems, Inc.

$$\text{If } \mathbf{SWRES} = \text{true} \begin{cases} R_{\text{gsal}} = \dfrac{R_{\text{shg, T}} \cdot W}{L \cdot [3 + 9 \cdot (\mathbf{NGCON} - 1)]} \\ R_{\text{gpv}} = \dfrac{R_{\text{pv, T}}}{W \cdot L} \\ R_{\text{end}} = \dfrac{R_{\text{end, T}}}{2 \cdot (W + \mathbf{DWR})} \\ R_{\text{sub}} = \dfrac{R_{\text{shs, T}} \cdot L}{12 \cdot (W + \mathbf{DWR})} \\ R_{\text{gsal}} = \text{`CLIP_BOTH}(R_{\text{gsal}},\ 1.0e-03,\ 1e01) \\ R_{\text{gpv}} = \text{`CLIP_BOTH}(R_{\text{gpv}},\ 1.0e-03,\ 1e02) \\ R_{\text{end}} = \text{`CLIP_BOTH}(R_{\text{end}},\ 1.0e-03,\ 1e01) \\ R_{\text{sub}} = \text{`CLIP_BOTH}(R_{\text{sub}},\ 1.0e-03,\ 1e03) \\ U_{\text{ac,T}} = \text{`CLIP_BOTH}(U_{\text{ac,T}},\ 1.0e-03,\ 2e01) \\ G_{\text{gsal}} = 1/R_{\text{gsal}} \\ G_{\text{gpv}} = 1/R_{\text{gpv}} \\ G_{\text{end}} = 1/R_{\text{end}} \\ G_{\text{sub}} = 1/R_{\text{sub}} \\ G_{\text{ac0}} = 12 \cdot U_{\text{ac, T}} \cdot W/L \end{cases}$$

$$\text{If } \mathbf{SWRES} = \text{false} \begin{cases} G_{\text{gsal}} = 0.0 \\ G_{\text{gpv}} = 0.0 \\ G_{\text{end}} = 0.0 \\ G_{\text{sub}} = 0.0 \\ G_{\text{ac0}} = 0.0 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Gate Tunneling Parameters

© 2023 Cadence Design Systems, Inc.

(26-12)

$$
\text{If } \mathbf{SWIGATE} = \text{true} \begin{cases}
I_{\text{ginv}} = \mathbf{IGINVLW} \cdot W_{\text{eff}} \cdot L_{\text{eff}} \cdot 10^{12} \cdot \left(\frac{T_{\text{KD}}}{T_{\text{KR}}}\right)^{\mathbf{STIG}} \\
I_{\text{gov}} = 2 \cdot \mathbf{IGOVW} \cdot \mathbf{LOV} \cdot W_{\text{eff}} \cdot 10^{12} \cdot \left(\frac{T_{\text{KD}}}{T_{\text{KR}}}\right)^{\mathbf{STIG}} \\
I_{\text{gcHVB}} = \mathbf{IGCHVLW} \cdot W_{\text{eff}} \cdot L_{\text{eff}} \cdot 10^{12} \cdot \left(\frac{T_{\text{KD}}}{T_{\text{KR}}}\right)^{\mathbf{STIG}} \\
I_{\text{govHVB}} = 2 \cdot \mathbf{IGOVHVW} \cdot \mathbf{LOV} \cdot W_{\text{eff}} \cdot 10^{12} \cdot \left(\frac{T_{\text{KD}}}{T_{\text{KR}}}\right)^{\mathbf{STIG}} \\
\text{INV}_{\text{CHIB}} = 1/\mathbf{CHIBO} \\
\text{INV}_{\text{CHIB, HVB}} = 1/\mathbf{CHIBPO} \\
B_{\text{CH}} = (4/3) \cdot \mathbf{TOXO} \cdot \sqrt{2 \cdot q \cdot m_0 \cdot \mathbf{CHIBO}}\,/\hbar \\
B_{\text{OV}} = B_{\text{CH}} \\
B_{\text{CH, HVB}} = (4/3) \cdot \mathbf{TOXO} \cdot \sqrt{2 \cdot q \cdot m_0 \cdot \mathbf{CHIBPO}}\,/\hbar \\
B_{\text{OV, HVB}} = B_{\text{CH, HVB}} \\
\text{If } \mathbf{GC3O} < 0,\ \ Q_{\text{CQ}} = -0.495 \cdot \mathbf{GC2O}/\mathbf{GC3O}, \\
\text{else } \ Q_{\text{CQ}} = 0.0 \text{ , endif} \\
\alpha_{\text{b, s}} = 0.5 \cdot (E_{\text{g}} + \mathbf{TYPE} \cdot \phi_{\text{b}}) \\
\alpha_{\text{b, ov}} = 0.5 \cdot (E_{\text{g}} + \mathbf{TYPE} \cdot \phi_{\text{b, ov}}) \\
D_{\text{ch}} = \mathbf{GCOO} \cdot \phi_{\text{T}} \\
D_{\text{ch, HVB}} = \mathbf{GCOO} \cdot \phi_{\text{T}}
\end{cases}
$$

$$
\text{If } \mathbf{SWIGATE} = \text{false} \begin{cases}
I_{\text{ginv}} = 0 \\
I_{\text{gov}} = 0 \\
I_{\text{gcHVB}} = 0 \\
I_{\text{govHVB}} = 0 \\
\text{INV}_{\text{CHIB}} = 0.1 \\
\text{INV}_{\text{CHIB, HVB}} = 0.1 \\
B_{\text{CH}} = 0 \\
B_{\text{OV}} = 0 \\
B_{\text{CH, HVB}} = 0 \\
B_{\text{OV, HVB}} = 0 \\
Q_{\text{CQ}} = 0 \\
\alpha_{\text{b, s}} = 0 \\
\alpha_{\text{b, ov}} = 0 \\
D_{\text{ch}} = 0 \\
D_{\text{ch. HVB}} = 0
\end{cases}
$$

© 2023 Cadence Design Systems, Inc.

Static Evaluations

(26-13)

$$N_{\mathrm{b,\,lim}} = \mathbf{NSUBO} \cdot \mathbf{MNSUBO}$$

$$N_{\mathrm{b1}} = \mathbf{NSUBO} \cdot \left[1 + \mathbf{DNSUBO} \cdot \mathrm{MAXA}(\mathbf{TYPE} \cdot (V_{\mathrm{C}} - \mathbf{VNSUBO}),\ 0,\ \mathbf{NSLPO})\right],$$

where `Vc` is the voltage across the capacitor `C`.

© 2023 Cadence Design Systems, Inc.

(26-14)

$$N_{\mathrm{b,v}} = \mathbf{NSUBO} \cdot \mathrm{MINA}(N_{\mathrm{b1}}/\mathbf{NSUBO},\ \mathbf{MNSUBO},\ 10^{-6})$$

$$norm_{\mathrm{nsub}} = N_{\mathrm{b,v}}/10^{23}$$

$$\phi_{\mathrm{b1}} = E_{\mathrm{g}} + 2 \cdot \boldsymbol{\phi}_{\mathbf{T}} \cdot \ln\left(N_{\mathrm{b,v}} \cdot \mathrm{INV}_{\mathrm{ni}}\right)$$

$$\gamma_{\mathrm{s1}} = \sqrt{2 \cdot q \cdot \epsilon_{\mathrm{si}} \cdot N_{\mathrm{b,v}}}/C_{\mathrm{ox}}$$

$$\text{If } \mathbf{QMC} > 0 \begin{cases} q_{\mathrm{b0}} = \sqrt{\gamma_s^2 \cdot \phi_b} \\ d_{\phi\mathrm{bq}} = 0.75 \cdot q_q \cdot (q_{\mathrm{b0}})^{2/3} \\ \phi_{\mathrm{b}} = \phi_{\mathrm{b1}} + d_{\phi\mathrm{bq}} \\ \gamma_{\mathrm{s}} = \gamma_{\mathrm{s1}} \cdot \left(1 + \dfrac{4}{3}\dfrac{d_{\phi\mathrm{bq}}}{q_{\mathrm{b0}}}\right) \end{cases}$$

$$G_{\mathrm{s}} = \gamma_{\mathrm{s}}/\sqrt{\boldsymbol{\phi}_{\mathbf{T}}}$$

$$\xi_{\mathrm{s}} = 1 + G_{\mathrm{s}}/\sqrt{2}$$

$$x_{\mathrm{mrgs}} = 10^{-5} \cdot \xi_{\mathrm{s}}$$

$$x_{\mathrm{ns}} = \phi_{\mathrm{b}}/\boldsymbol{\phi}_{\mathbf{T}}$$

$$\Delta_{\mathrm{ns}} = \begin{cases} \exp(-x_{\mathrm{ns}}), & \text{if } x_{\mathrm{ns}} < k_{\mathrm{se2}} \\ \dfrac{10^{-200}}{\mathrm{P3}\,(x_{\mathrm{ns}} - k_{\mathrm{se2}})}, & \text{otherwise} \end{cases}$$

$$x_{\mathrm{g1}} = x_1 + G_{\mathrm{s}} \cdot \sqrt{\exp(-x_1) + x_1 - 1}$$

$$x_{\mathrm{g1,\,ov}} = x_1 + G_{\mathrm{ov,\,s}} \cdot \sqrt{\exp(-x_1) + x_1 - 1}$$

Calculation of Surface Potential at the Channel Side

A macro Φ_s is defined to calculate the surface potential at the channel side with output `xs`, and inputs: `xns`, Δ`ns`, `G`, `G`^{2}, `G`$^{-2}$, ζ , ξ^{-1}, `xmrg`.

© 2023 Cadence Design Systems, Inc.

(26-15)

$$\text{if } x_g < -x_{mrg} \begin{cases} y_g = -x_g \\ z = 1.25 \cdot y_g / \xi \\ \eta = \left[z + 10 - \sqrt{(z-6)^2 + 64} \right] / 2 \\ a = (y_g - \eta)^2 + G^2 \cdot (\eta + 1) \\ c = 2 \cdot (y_g - \eta) - G^2 \\ \tau = -\eta + \ln\left(a / G^2\right) \\ y_0 = \sigma_1(a,\, c,\, \tau,\, \eta) \\ \Delta_0 = \mathrm{expl}_{\mathrm{high}}(y_0) \\ p = 2 \cdot (y_g - y_0) + G^2 \cdot [\Delta_0 - 1 + \Delta_{ns} \cdot (1 - 1/\Delta_0)] \\ q = (y_g - y_0)^2 + G^2 \cdot [y_0 - \Delta_0 + 1 + \Delta_{ns} \cdot (1 - 1/\Delta_0 - 2 \cdot y_0)] \\ x_s = -y_0 - \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot [2 - G^2 \cdot (\Delta_0 + \Delta_{ns}/\Delta_0)]}} \end{cases}$$

$$\text{if } |x_g| \le x_{mrg} \begin{cases} x_s = \dfrac{x_g}{\xi} \cdot \left[1 + G \cdot x_g \cdot \dfrac{1 - \Delta_{ns}}{\xi^2 \cdot 6 \cdot \sqrt{2}} \right] \end{cases}$$

© 2023 Cadence Design Systems, Inc.

(26-16)

$$
\text{if } x_g > x_{mrg} \quad \begin{cases}
\hat{x}_{g1} = x_1 + G \cdot \sqrt{\exp(-x_1) + x_1 - 1} \\
\bar{x} = \dfrac{x_g}{\xi} \cdot \left[1 + x_g \cdot (\xi \cdot x_1 - \hat{x}_{g1})/\hat{x}_{g1}^2\right] \\
x_0 = x_g + G^2/2 - G \cdot \sqrt{x_g + G^2/4 - 1 + \text{expl}_{\text{low}}(-\bar{x})} \\
b_x = x_{ns} + 3 \\
\eta = \text{MINA}(x_0,\, b_x,\, 5) - \left(b_x - \sqrt{b_x^2 + 5}\right)/2 \\
a = (x_g - \eta)^2 - G^2 \cdot [\exp(-\eta) + \eta - 1 - \Delta_{ns} \cdot (\eta + 1)] \\
b = 1 - G^2/2 \cdot \exp(-\eta) \\
c = 2 \cdot (x_g - \eta) + G^2 \cdot [1 - \exp(-\eta) - \Delta_{ns}] \\
\tau = x_{ns} - \eta + \ln\left(a/G^2\right) \\
y_0 = \sigma_2(a,\, b,\, c,\, \tau,\, \eta) \\
\Delta_0 = \begin{cases}
\exp\left(y_0\right), & \text{if } y_0 < k_{se1} \\
\exp\left(y_0 - x_{ns}\right), & \text{if } y_0 > x_{ns} - k_{se1} \\
\dfrac{10^{-100}}{\text{P3}(x_{ns} - y_0 - k_{se1})}, & \text{otherwise}
\end{cases} \\
p = 2 \cdot (x_g - y_0) + G^2 \cdot [1 - 1/\Delta_0 + \Delta_{ns} \cdot (\Delta_0 - 1)] \\
q = (x_g - y_0)^2 - G^2 \cdot [y_0 + 1/\Delta_0 - 1 + \Delta_{ns} \cdot (\Delta_0 - y_0 - 1)] \\
x_s = y_0 + \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot [2 - G^2 \cdot (1/\Delta_0 + \Delta_{ns} \cdot \Delta_0)]}}
\end{cases}
$$

© 2023 Cadence Design Systems, Inc.

Calculation of Surface Potential at the Overlap Regions

A macro Φ_{ov} is defined to calculate the surface potential at the channel side with output xov, and inputs: xg, Gov, G_{ov}^2, x_{mrgov}, , ξ_{ov}, x_{g1}.

© 2023 Cadence Design Systems, Inc.

(26-17)

$$
x_{\mathrm{ov}}(x_{\mathrm{g}}) = \begin{cases}
\text{if } x_{\mathrm{g}} < -x_{\mathrm{mrgov}} \begin{cases}
y_{\mathrm{g}} = -x_{\mathrm{g}} \\
z = x_1 \cdot y_{\mathrm{g}} / \xi_{\mathrm{ov}} \\
\eta = \left[z + 10 - \sqrt{(z-6)^2 + 64} \right] \Big/ 2 \\
a = (y_{\mathrm{g}} - \eta)^2 + G_{\mathrm{ov}}^2 \cdot (\eta + 1) \\
c = 2 \cdot (y_{\mathrm{g}} - \eta) - G_{\mathrm{ov}}^2 \\
\tau = -\eta + \ln\left(a / G_{\mathrm{ov}}^2\right) \\
y_0 = \sigma_1(a,\, c,\, \tau,\, \eta) \\
\Delta_0 = \exp\left(y_0\right) \\
p = 2 \cdot (y_{\mathrm{g}} - y_0) + G_{\mathrm{ov}}^2 \cdot (\Delta_0 - 1) \\
q = (y_{\mathrm{g}} - y_0)^2 + G_{\mathrm{ov}}^2 \cdot (y_0 - \Delta_0 + 1) \\
x_{\mathrm{ov}} = -y_0 - \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot (2 - G_{\mathrm{ov}}^2 \cdot \Delta_0)}}
\end{cases} \\
\text{if } |x_{\mathrm{g}}| < x_{\mathrm{mrgov}} \begin{cases} x_{\mathrm{ov}} = x_{\mathrm{g}} / \xi_{\mathrm{ov}} \end{cases} \\
\text{if } x_{\mathrm{g}} > x_{\mathrm{mrgov}} \begin{cases}
\bar{x} = x_{\mathrm{g}} / \xi_{\mathrm{ov}} \cdot \left[1 + x_{\mathrm{g}} \cdot (\xi_{\mathrm{ov}} \cdot x_1 - x_{\mathrm{g1}}) / x_{\mathrm{g1}}^2 \right] \\
\omega = \begin{cases} 1 - \exp\left(-\bar{x}\right), & \text{if } \bar{x} < k_{\mathrm{se2}} \\ 1 - \dfrac{10^{-200}}{\mathrm{P3}(\bar{x} - k_{\mathrm{se2}})}, & \text{otherwise} \end{cases} \\
x_0 = x_{\mathrm{g}} + G_{\mathrm{ov}}^2 / 2 - G_{\mathrm{ov}} \cdot \sqrt{x_{\mathrm{g}} + G_{\mathrm{ov}}^2 / 4 - \omega} \\
\Delta_0 = \begin{cases} \exp\left(-x_0\right), & \text{if } x_0 < k_{\mathrm{se2}} \\ \dfrac{10^{-200}}{\mathrm{P3}(x_0 - k_{\mathrm{se2}})}, & \text{otherwise} \end{cases} \\
p = 2 \cdot (x_{\mathrm{g}} - x_0) + G_{\mathrm{ov}}^2 \cdot (1 - \Delta_0) \\
q = (x_{\mathrm{g}} - x_0)^2 - G_{\mathrm{ov}}^2 \cdot (x_0 + \Delta_0 - 1) \\
x_{\mathrm{ov}} = x_0 + \dfrac{2 \cdot q}{p + \sqrt{p^2 - 2 \cdot q \cdot (2 - G_{\mathrm{ov}}^2 \cdot \Delta_0)}}
\end{cases}
\end{cases}
$$

© 2023 Cadence Design Systems, Inc.

Surface Potential Without Poly Effect

(26-18)

$$V_{\mathrm{gb1}} = \mathbf{TYPE} \cdot (V_{\mathrm{C}} - V_{\mathrm{fb,\,T}})$$

$$x_{\mathrm{g}} = V_{\mathrm{gb1}}/\phi_{\mathbf{T}}$$

$$x_{\mathrm{s0}} = \Phi_{\mathrm{s}}(x_{\mathrm{g}},\ x_{\mathrm{ns}},\ \Delta_{\mathrm{ns}},\ G_{\mathrm{s}},\ G_{\mathrm{s}}^{2},\ G_{\mathrm{s}}^{-2},\ \xi_{\mathrm{s}},\ \xi_{\mathrm{s}}^{-1},\ x_{\mathrm{mrgs}})$$

$$\psi_{\mathrm{s0}} = x_{\mathrm{s0}} \cdot \phi_{\mathbf{T}}.$$

Surface Potential With Poly Effect

The following calculates the poly surface potential when NPO < 10^{27}.

(26-19)

$$x_{\mathrm{gp}} = -\mathbf{TYPE} \cdot \mathbf{TYPEP} \cdot (V_{\mathrm{gb1}} - \psi_{\mathrm{s0}})/\phi_{\mathbf{T}}$$

$$x_{\mathrm{p0}} = \Phi_{\mathrm{s}}(x_{\mathrm{gp}},\ x_{\mathrm{np}},\ \Delta_{\mathrm{np}},\ G_{\mathrm{p}},\ G_{\mathrm{p}}^{2},\ G_{\mathrm{p}}^{-2},\ \xi_{\mathrm{p}},\ \xi_{\mathrm{p}}^{-1},\ x_{\mathrm{mrgp}})$$

$$\psi_{\mathrm{p0}} = -\mathbf{TYPE} \cdot \mathbf{TYPEP} \cdot x_{\mathrm{p0}} \cdot \phi_{\mathbf{T}}$$

$$x_{\mathrm{g}} = (V_{\mathrm{gb1}} - \psi_{\mathrm{p0}})/\phi_{\mathbf{T}}$$

$$x_{\mathrm{s0}} = \Phi_{\mathrm{s}}(x_{\mathrm{g}},\ x_{\mathrm{ns}},\ \Delta_{\mathrm{ns}},\ G_{\mathrm{s}},\ G_{\mathrm{s}}^{2},\ G_{\mathrm{s}}^{-2},\ \xi_{\mathrm{s}},\ \xi_{\mathrm{s}}^{-1},\ x_{\mathrm{mrgs}})$$

$$\psi_{\mathrm{s0}} = x_{\mathrm{s0}} \cdot \phi_{\mathbf{T}}.$$

Static Inversion Charge Calculations

The following calculates the surface potential-related variables and inversion charge:

(26-20)

If `xg <=0`, `qis=0`

© 2023 Cadence Design Systems, Inc.

When xg >0, (namely the depletion and inversion regions) following is performed to find `qis` and `qeff`:

(26-21)

$$\Delta_{1s} = 0$$

© 2023 Cadence Design Systems, Inc.

(26-22)

$$
\begin{cases}
\text{If } x_{s0} < k_{se1} & \begin{cases} \Delta_{ls1} = \exp(x_{s0}) \\ E_s = \Delta_{ls1}^{-1} \\ \Delta_{ls} = \Delta_{ns} \cdot \Delta_{ls1} \\ D_s = \Delta_{ns} \cdot (E_s^{-1} - x_{s0} - 1) \end{cases} \\
\text{elseif } x_{s0} > x_{ns} - k_{se1} & \begin{cases} \Delta_{ls} = \exp(x_{s0} - x_{ns}) \\ E_s = \Delta_{ns}/\Delta_{ls} \\ D_s = \Delta_{ls} - \Delta_{ns} \cdot (x_{s0} + 1) \end{cases} \\
\text{else} & \begin{cases} \Delta_{ls} = \dfrac{10^{-100}}{\mathrm{P3}(x_{ns} - x_{s0} - k_{se1})} \\ E_s = \dfrac{10^{-100}}{\mathrm{P3}(x_{s0} - k_{se1})} \\ D_s = \Delta_{ls} - \Delta_{ns} \cdot (x_{s0} + 1) \end{cases}
\end{cases}
$$

$$
\begin{cases}
\text{If } x_{s0} < 10^{-5} & \begin{cases} P_s = 0.5 \cdot x_{s0}^2 \cdot \left[1 - \dfrac{1}{3} x_{s0} \cdot (1 - 0.25 \cdot x_{s0})\right] \\ D_s = \dfrac{1}{6} \Delta_{ns} \cdot x_{s0}^3 \cdot (1 + 1.75 \cdot x_{s0}) \\ S_{qs} = x_{s0} \cdot \sqrt{0.5 - \dfrac{1}{6} x_{s0} \cdot (1 - 0.25 \cdot x_{s0})} \end{cases} \\
\text{else} & \begin{cases} P_s = x_{s0} + E_s - 1 \\ S_{qs} = \sqrt{P_s} \end{cases}
\end{cases}
$$

$$x_{gs} = G_s \cdot \sqrt{P_s + D_s}$$

$$q_{is} = \phi_T \cdot G_s^2 \cdot D_s / (x_{gs} + G_s \cdot S_{qs})$$

The normalized static inversion charge is:

(26-23)

```
Qi0 = -qis
```


© 2023 Cadence Design Systems, Inc.

Time-Dependent Silicon Surface Potential Without Poly Effect

(26-24)

$$x_{\mathrm{g,t}} = (V_{\mathrm{gb1}} + V_{\mathrm{n}})/\phi_{\mathbf{T}},$$

where `Vn` is the voltage at the internal time constant node n.

(26-25)

$$x_{\mathrm{s}} = \Phi_{\mathrm{ov}}(x_{\mathrm{g,t}},\ G_{\mathrm{s}},\ G_{\mathrm{s}}^2,\ x_{\mathrm{mrgs}},\ \xi_{\mathrm{s}},\ x_{\mathrm{g1}}),$$

where Φ_{ov} calculates the normalized surface potential as defined in Calculation of Surface Potential at the Overlap Regions on page 2069.

(26-26)

$$\psi_{\mathrm{s}} = x_{\mathrm{s}} \cdot \phi_{\mathbf{T}}$$

Time-Dependent Poly Surface Potential Calculation Correction

If NPO >= 10^{27}, Ψ_p=0, otherwise, the following procedure is used:

(26-27)

$$x_{\mathrm{gp,t}} = -\mathbf{TYPE} \cdot \mathbf{TYPEP} \cdot (V_{\mathrm{gb1}} - \psi_{\mathrm{s}})/\phi_{\mathbf{T}}$$

$$x_{\mathrm{p}} = \Phi_{\mathrm{s}}(x_{\mathrm{gp,t}},\ x_{\mathrm{np}},\ \Delta_{\mathrm{np}},\ G_{\mathrm{p}},\ G_{\mathrm{p}}^2,\ G_{\mathrm{p}}^{-2},\ \xi_{\mathrm{p}},\ \xi_{\mathrm{p}}^{-1},\ x_{\mathrm{mrgp}})$$

$$\psi_{\mathrm{p}} = -\mathbf{TYPE} \cdot \mathbf{TYPEP} \cdot x_{\mathrm{p}} \cdot \phi_{\mathbf{T}}$$

$$x_{\mathrm{g,t}} = (V_{\mathrm{gb1}} + V_{\mathrm{n}} - \psi_{\mathrm{p}})/\phi_{\mathbf{T}}$$

$$x_{\mathrm{s}} = \Phi_{\mathrm{ov}}(x_{\mathrm{g,t}},\ G_{\mathrm{s}},\ G_{\mathrm{s}}^2,\ x_{\mathrm{mrgs}},\ \xi_{\mathrm{s}},\ x_{\mathrm{g1}})$$

$$\psi_{\mathrm{s}} = x_{\mathrm{s}} \cdot \phi_{\mathbf{T}}$$

© 2023 Cadence Design Systems, Inc.

Quantum Mechanical Corrections

(26-28)

$$\Delta_{ls} = 0$$

$$\begin{cases} \text{If } x_s < k_{se1} & \begin{cases} \Delta_{ls} = \exp(x_s) \\ E_s = \Delta_{ls}^{-1} \end{cases} \\ \text{elseif } x_s > x_{ns} - k_{se1} & \begin{cases} \Delta_{ls} = \exp(x_{ns} - x_s) \\ E_s = \Delta_{ns} \cdot \Delta_{ls} \end{cases} \\ \text{else} & E_s = \dfrac{10^{-100}}{\mathrm{P3}(x_s - k_{se1})} \end{cases}$$

$$\begin{cases} \text{If } x_s < -x_{mrgs} & \begin{cases} P_s = E_s + x_s - 1.0 \\ S_{qs} = -\sqrt{P_s} \end{cases} \\ \text{else if } abs(x_s) <= x_{mrgs} & \begin{cases} P_s = 0.5 \cdot x_s^2 \cdot \left[1 - \dfrac{1}{3} x_s \cdot (1 - 0.25 \cdot x_s)\right] \\ S_{qs} = x_s \cdot \sqrt{0.5 - \dfrac{1}{6} x_s \cdot (1 - 0.25 \cdot x_s)} \end{cases} \\ \text{else} & \begin{cases} P_s = x_s + E_s - 1 \\ S_{qs} = \sqrt{P_s} \end{cases} \end{cases}$$

$$q_{bs} = \phi_T \cdot S_{qs} \cdot G_s$$

$$\epsilon = 1.62 \cdot [(1 + norm_{nsub}) \cdot (1 + 0.37 \cdot norm_{tox})]^2 \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{1.5} \cdot \phi_T^2;$$

$$q_{eff} = \mathrm{MAXA}(q_{bs}, -q_{bs}, \epsilon) + \eta_\mu \cdot \mathrm{MAXA}(-V(b_cn), V(b_cn), \epsilon)$$

The following $C_{ox,qm}$ calculation is for all regions (x_g <=0 and x_g >0)

© 2023 Cadence Design Systems, Inc.

(26-29)

$$C_{\text{ox, qm}} = \begin{cases} C_{\text{ox}}, & q_{\text{q}} = 0 \\ \dfrac{C_{\text{ox}}}{1 + q_{\text{q}} \cdot \left(q_{\text{eff}}^2 + q_{\text{lim2}}\right)^{-1/6}}, & q_{\text{q}} > 0 \end{cases}$$

Accumulation Resistance Bias Dependence

(26-30)

$$f_{\text{rac}} = \begin{cases} \phi_{\mathbf{T}} \cdot \exp(-10), & \text{if } x_{\text{s0}} > 10 \\ \phi_{\mathbf{T}} \cdot \exp(-x_{\text{s0}}), & \text{otherwise} \end{cases}$$

$$q_{\text{ac}} = \gamma_s \cdot C_{\text{ox, qm}} \cdot \sqrt{f_{\text{rac}}}$$

$$m_{\text{axs}} = 0.5 \cdot \left(-V_{\text{gb1}} + \sqrt{V_{\text{gb1}}^2 + 0.04}\right)$$

$$G_{\text{ac}} = G_{\text{ac0}} \cdot q_{\text{ac}} / (1 + \mathbf{UACRED} \cdot m_{\text{axs}})$$

Calculation of Gate Tunneling Current

A macro $\texttt{I}_{\texttt{gate}}$ is defined as a function of $\texttt{I}_{\texttt{gin}}$, $\texttt{I}_{\texttt{ginHVB}}$, $\texttt{E}_{\texttt{g}}$, $\texttt{V}_{\texttt{ov}}$, $\texttt{D}_{\texttt{ch}}$, $\texttt{D}_{\texttt{ch, HVB}}$, $\texttt{INV}_{\texttt{CHIB}}$, $\texttt{INV}_{\texttt{CHIB, HVB}}$, GC2O, GC3O, GC2HVO, GC3HVO, $\texttt{Q}_{\texttt{CQ}}$, $\texttt{Q}_{\texttt{CQ, HVB}}$, $\texttt{I}_{\texttt{g, type}}$, $\texttt{x}_{\texttt{s}}$, $\alpha_{\texttt{b, s}}$, $\alpha_{\texttt{b, ov}}$, Φ_T^{-1}, TYPEP, TYPE, $\texttt{V}_{\texttt{b,ig}}$, $\texttt{B}_{\texttt{OV}}$, and $\texttt{B}_{\texttt{OV}}$, $\texttt{H}_{\texttt{VB}}$ as shown in the following with $\texttt{I}_{\texttt{gout}}$ as output. It is used for the calculation of gate tunneling current.

© 2023 Cadence Design Systems, Inc.

(26-31)

$$
\text{If } \mathbf{TYPEP} = 1 \begin{cases}
\psi_t = \text{MAXA}(0,\ \mathbf{TYPE} \cdot V_{ov} + D_{ch,\,HVB},\ 0.01) \\
z_g = \sqrt{V_{ov}^2 + 10^{-6}} \cdot \text{INV}_{CHIB,\,HVB} \\
\text{If } \mathbf{GC3HVO} < 0 \\
\quad z_g = \text{MINA}(z_g,\ Q_{CQ,HVB},\ 10^{-6}) \\
\text{endif} \\
\Delta_{si} = \begin{cases}
\exp\left[-\mathbf{TYPE} \cdot x_s - (E_g - \alpha_{b,ov} + \psi_t) \cdot \phi_T^{-1}\right], & \text{if } I_{g,\,type} = 0 \\
\exp\left[-\mathbf{TYPE} \cdot x_s - (E_g - \alpha_{b,s} + \psi_t) \cdot \phi_T^{-1}\right], & \text{if } I_{g,\,type} = 1
\end{cases} \\
\Delta_{gate} = \Delta_{si} \cdot \exp\left(\mathbf{TYPE} \cdot V_{b,ig} \cdot \phi_T^{-1}\right) \\
D = \exp\{B_{OV} \cdot [-1.5 + z_g \cdot (\mathbf{GC2HVO} + \mathbf{GC3HVO} \cdot z_g)]\} \\
I_{gout,\,HVB} = I_{ginHVB} \cdot D \cdot \mathbf{TYPE} \cdot \ln\left(\dfrac{1.0 + \Delta_{gate}}{1.0 + \Delta_{si}}\right)
\end{cases}
$$

$$\psi_t = \text{MINA}(0,\ \mathbf{TYPE} \cdot V_{ov} + D_{ch},\ 0.01)$$

$$z_g = \sqrt{V_{ov}^2 + 10^{-6}} \cdot \text{INV}_{CHIB}$$

(26-32)

$$
\begin{cases}
\text{If } \mathbf{GC3O} < 0 \\
\quad z_g = \text{MINA}(z_g,\ Q_{CQ},\ 10^{-6}) \\
\text{endif} \\
\Delta_{si} = \begin{cases}
\exp\left(\mathbf{TYPE} \cdot x_s + (-\alpha_{b,ov} + \psi_t) \cdot \phi_T^{-1}\right), & \text{if } I_{g,\,type} = 0 \\
\exp\left(\mathbf{TYPE} \cdot x_s + (-\alpha_{b,s} + \psi_t) \cdot \phi_T^{-1}\right), & \text{if } I_{g,\,type} = 1
\end{cases} \\
\Delta_{gate} = \Delta_{si} \cdot \exp\left(-\mathbf{TYPE} \cdot V_{b,ig} \cdot \phi_T^{-1}\right) \\
D = \exp\{B_{OV} \cdot [-1.5 + z_g \cdot (\mathbf{GC2O} + \mathbf{GC3O} \cdot z_g)]\} \\
I_{gout,\,ECB} = I_{gin} \cdot D \cdot \mathbf{TYPE} \cdot \ln\left(\dfrac{1.0 + \Delta_{si}}{1.0 + \Delta_{gate}}\right) \\
I_{gout} = I_{gout,\,HVB} + I_{gout,\,ECB}
\end{cases}
$$

© 2023 Cadence Design Systems, Inc.

Gate Tunneling Current

(26-33)

$$V_{\mathrm{fb,\,ov}} = \begin{cases} \mathbf{TYPEP} \cdot E_{\mathrm{g}}, & \text{if } \mathbf{TYPE} \cdot \mathbf{TYPEP} = -1 \\ 0, & \text{otherwise} \end{cases}$$

$$x_{\mathrm{g,\,ov}} = \mathbf{TYPE} \cdot \left(V_{\mathrm{b,\,ov}} - V_{\mathrm{fb,\,ov}}\right) / \phi_{\mathbf{T}},$$

where $V_{\mathrm{b,\,ov}}$ is the voltage across the overlap, from bi to gi.

If $\mathbf{SWIGATE} \neq 0$ and $I_{\mathrm{gov}} + I_{\mathrm{govHVB}} > 0$

$$x_{\mathrm{ov,\,s0}} = \Phi_{\mathrm{ov}}(x_{\mathrm{g,\,ov}},\ G_{\mathrm{ov,\,s}},\ G^2_{\mathrm{ov,\,s}},\ x_{\mathrm{mrgov,\,s}},\ \xi_{\mathrm{ov,\,s}},\ x_{\mathrm{g1,\,ov}})$$

$$V_{\mathrm{ov}} = \phi_{\mathbf{T}} \cdot (x_{\mathrm{g,\,ov}} - x_{\mathrm{ov,\,s0}})$$

else

$$V_{\mathrm{ov}} = 0.0$$

$$x_{\mathrm{ov,\,s0}} = 0.0$$

end

Initially, `I`$_{GC}$`=0.0` and `I`$_{GOV}$`=0.0`.

If `SWIGATE=true`

© 2023 Cadence Design Systems, Inc.

(26-34)

$$\begin{aligned}
&\text{If } I_{\text{gov}} + I_{\text{govHVB}} > 0 \\
&\quad V_{\text{bov,ig}} = V_{\text{b, ov}} \cdot \mathbf{TYPE} \\
&\quad I_{\text{GOV}} = I_{\text{gate}}(I_{\text{gov}},\ I_{\text{govHVB}},\ E_{\text{g}},\ V_{\text{ov}},\ D_{\text{ch}},\ D_{\text{ch, HVB}},\ \mathbf{INV_{CHIB}},\ \mathbf{INV_{CHIB, HVB}},\ \mathbf{GC2O}, \\
&\qquad \mathbf{GC3O},\ \mathbf{GC2HVO},\ \mathbf{GC3HVO},\ Q_{\text{CQ}},\ 0,\ x_{\text{ov, s0}},\ \alpha_{\text{b, s}},\ \alpha_{\text{b, ov}},\ \phi_{\mathbf{T}}^{-1},\ \mathbf{TYPEP},\ \mathbf{TYPE}, \\
&\qquad V_{\text{bov,ig}},\ B_{\text{OV}},\ B_{\text{OV, HVB}}) \\
&\text{end}
\end{aligned}$$

$$\begin{aligned}
&\text{If } I_{\text{ginv}} + I_{\text{gcHVB}} > 0 \\
&\quad V_{\text{bci, ig}} = V_{\text{C}} \cdot \mathbf{TYPE} \\
&\quad V_{\text{ox}} = (x_{\text{g}} - x_{\text{s}}) \cdot \phi_{\mathbf{T}} \\
&\quad I_{\text{GC}} = I_{\text{gate}}(I_{\text{ginv}},\ I_{\text{gcHVB}},\ E_{\text{g}},\ V_{\text{ox}},\ D_{\text{ch}},\ D_{\text{ch, HVB}},\ \mathbf{INV_{CHIB}},\ \mathbf{INV_{CHIB, HVB}},\ \mathbf{GC2O}, \\
&\qquad \mathbf{GC3O},\ \mathbf{GC2HVO},\ \mathbf{GC3HVO},\ Q_{\text{CQ}},\ 1,\ x_{\text{s}},\ \alpha_{\text{b, s}},\ \alpha_{\text{bci, ig}},\ \phi_{\mathbf{T}}^{-1},\ \mathbf{TYPEP},\ \mathbf{TYPE}, \\
&\qquad V_{\text{bci,ig}},\ B_{\text{CH}},\ B_{\text{CH, HVB}}) \\
&\text{end}
\end{aligned}$$

Terminal Currents

DC Currents

(26-35)

Current through the gate $\mathtt{I_{g,DC}} = \mathbf{m} \cdot (I_{\text{GC}} + I_{\text{GOV}})$,

(26-36)

Current through the gate $\mathtt{I_{b,DC}} = -\mathbf{m} \cdot (I_{\text{GC}} + I_{\text{GOV}})$.

Terminal Charges

Total charges at the gate

© 2023 Cadence Design Systems, Inc.

(26-37)

$$Q_{\text{g, total}} = (V_{\text{gb1}} - \phi_{\text{s}} - \phi_{\text{p}}) \cdot L_{\text{eff}} \cdot W_{\text{eff}} \cdot C_{\text{ox, qm}} \cdot \mathbf{TYPE} + C_{\text{fr}} \cdot V_{\text{C, fr}}$$

Total charges at the bulk

(26-38)

$$Q_{\text{b, total}} = -(V_{\text{gb1}} - \phi_{\text{s}} - \phi_{\text{p}}) \cdot L_{\text{eff}} \cdot W_{\text{eff}} \cdot C_{\text{ox, qm}} \cdot \mathbf{TYPE} - C_{\text{fr}} \cdot V_{\text{C, fr}}$$

Noise

Thermal Noise

Thermal noise contributions from `rgsal`, `rgpv`, `rend`, `rsub` and `rac0` are calculated when `SWRES = 1`.

When `SWRES = 0`, the noise contribution is 0. This is realized in the code by setting $G_{\texttt{gsal}}$, $G_{\texttt{gpv}}$, $G_{\texttt{end}}$, $G_{\texttt{sub}}$, and $G_{\texttt{ac0}}$ to 0.

Following are the equations for thermal noise calculation:

(26-39)

$$rgsalnoise = \mathrm{m} \cdot nt0 \cdot G_{gsal}$$

$$rgpvnoise = \mathrm{m} \cdot nt0 \cdot G_{gpv}$$

$$rendnoise = \mathrm{m} \cdot nt0 \cdot G_{end}$$

$$rsubnoise = \mathrm{m} \cdot nt0 \cdot G_{sub}$$

© 2023 Cadence Design Systems, Inc.

(26-40)

If (**RACNOISE** $==0$)

$racnoise = 0$

else if (**RACNOISE** $==1$)

$racnoise = \mathrm{m} \cdot nt0 \cdot G_{ac0}$

else if (**RACNOISE** $==2$)

$racnoise = \mathrm{m} \cdot nt0 \cdot G_{ac}$

end

Shot Noise

Shot noise contributions from the gate tunneling current are calculated when when `SWIGATE=1`. Following are the equations for shot noise calculation:

(26-41)

$$igcnoise = \mathrm{m} \cdot 2 \cdot q \cdot |I_{GC}|$$

$$igovnoise = \mathrm{m} \cdot 2 \cdot q \cdot |I_{GOV}|$$

Parameter Extraction

Capacitance-Related Model Parameter Extraction

(26-42)

$$C(V) = C_o(V) \cdot L \cdot W \cdot m + C_{fr} \cdot m$$

where C_0 is the bias-dependent capacitance of an intrinsic device,

© 2023 Cadence Design Systems, Inc.

(26-43)

$$L = L_g + DLQ, \mathrm{W} = W_g + DWQ$$

and m is the multiplicity factor. Parameters DWQ and DLQ describe the deviations of the effective channel length (L) and Width (W) from their drawn values L_g and W_g.

The total fringe capacitance is given by

$$C_{fr} = 2 \cdot (CFRW \cdot W + CFRL \cdot L)$$

© 2023 Cadence Design Systems, Inc.

Auxiliary Equations

(26-44)

$$\mathrm{MINA}\,(x,\,y,\,a) = \frac{1}{2}\cdot\left[x+y-\sqrt{(x-y)^2+a}\right]$$

$$\mathrm{MAXA}\,(x,\,y,\,a) = \frac{1}{2}\cdot\left[x+y+\sqrt{(x-y)^2+a}\right]$$

$$\nu = a + c$$

$$\mu_1 = \frac{v^2}{\tau} + \frac{c^2}{2} - a$$

$$\sigma_1\,(a,\,c,\,\tau,\,\eta) = \frac{a\cdot\nu}{\mu_1 + (c^2/3 - a)\cdot c\cdot\nu/\mu_1} + \eta$$

$$\mu_2 = \frac{v^2}{\tau} + \frac{c^2}{2} - a\cdot b$$

$$\sigma_2\,(a,\,b,\,c,\,\tau,\,\eta) = \frac{a\cdot\nu}{\mu_2 + (c^2/3 - a\cdot b)\cdot c\cdot\nu/\mu_2} + \eta$$

$$\mathrm{P3}(u) = 1 + u\cdot[1 + 0.5\cdot u\cdot(1 + u/3)]$$

$$\mathrm{expl}(x) = \begin{cases} \exp(x), & \text{if } |x| < k_{\mathrm{sel}} \\ \dfrac{10^{-100}}{\mathrm{P3}(-k_{\mathrm{sel}} - x)}, & \text{if } x < -k_{\mathrm{sel}} \\ 10^{100}\cdot\mathrm{P3}(x - k_{\mathrm{sel}}), & \text{otherwise} \end{cases}$$

$$\mathrm{expl}_{\mathrm{low}}(x) = \begin{cases} \exp(x), & \text{if } x > -k_{\mathrm{sel}} \\ \dfrac{10^{-100}}{\mathrm{P3}(-k_{\mathrm{sel}} - x)}, & \text{otherwise} \end{cases}$$

$$\mathrm{expl}_{\mathrm{high}}(x) = \begin{cases} \exp(x), & \text{if } x < k_{\mathrm{sel}} \\ 10^{100}\cdot\mathrm{P3}(x - k_{\mathrm{sel}}), & \text{otherwise} \end{cases}$$

Related Topics

© 2023 Cadence Design Systems, Inc.

PSP-Based MOS Varactor Model (mosvar)

Model Version Updates

Model Usage

Component Statements

Model Version Updates

Version 1.2.0

- Parameter `EPSROXO` has been added for relative dielectric permittivity
- Gate current computations has been revised to avoid numerical problems and to use `GC3HVO` for HVB current
- Parameter `RACNOISE` has been added to select noise equations for `Rac`.
- Noise names have been made more descriptive.
- Shot noise for gate currents has been added.

Version 1.3.0

- Range of parameters TOXO and NSUB0 extended.
- `V(b_cf)` has been replaced with `V(b_ov)` for `Igov` calculation.
- `V(b_cf)` has been replaced with `V(b_ci)` for I`gc` calculation.

Related Topics

PSP-Based MOS Varactor Model (mosvar)

Model Equations

Model Usage

Component Statements

© 2023 Cadence Design Systems, Inc.

Model Usage

Instance Syntax

```
Name g bi b ModelName <parameter=value> ...
```

Model Syntax

```
model modelName mosvar parameter=value ...
```

Related Topics

PSP-Based MOS Varactor Model (mosvar)

Model Version Updates

Model Usage

Component Statements

Component Statements

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1.0`	Multiplicity factor.
`w=1.0e-06 m`	Design width of varactor.
`l=1.0e-06 m`	Design length of varactor.
`ngcon=1`	Number of gate contacts.
`dta=0.0 degC`	Alias of DTA.
`trise=0.0 degC`	Alias of DTA.
`dta=0.0 degC`	Local temperature delta to ambient.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Parameters

`version=1.1`	The available versions are 1.1, 1.2, and 1.3.
`subversion=0.0`	Model subversion.
`revision=0.0`	Model revision.
`level=1000`	Model level.
`tmin=(-100.0) degC`	Minimum reference/ambient temperature.
`tmax=500.0 degC`	Maximum reference/ambient temperature.
`vmax=10000.0 V`	Maximum voltage applied between nodes g and b.
`tr=21.0 degC`	Nominal (reference) temperature.
`lmin=1.0e-08 m`	Minimum allowed drawn length.
`lmax=9.9e+09 m`	Maximum allowed drawn length.
`wmin=1.0e-08 m`	Minimum allowed drawn width.
`wmax=9.9e+09 m`	Maximum allowed drawn width.
`swres=1`	Switch to control series resistance: 0=exclude and 1=include.
`type=(-1)`	Substrate doping TYPE: -1=n-TYPE and +1=p-TYPE.

© 2023 Cadence Design Systems, Inc.

typep=(-1)	Polysilicon doping TYPE: -1=n-TYPE and +1=p-TYPE.
toxo=20.0e-10 m	Oxide thickness.
epsroxo=3.9	Relative permittivity.
tau=0.1 s	Time constant for inversion charge recombination/ generation.
vfbo=0.0 V	Flatband voltage (for p-TYPE substrate).
nsubo=3.0e+23 /m^3	Substrate doping level.
mnsubo=1.0	Maximum change in absolute doping, limited to 1 order of mag up.
dnsubo=0.0	Doping profile slope parameter.
vnsubo=0.0	Doping profile corner voltage parameter.
nslpo=0.1	Doping profile smoothing parameter.
npo=1.0e+27 /m^3	Polysilicon doping level.
qmc=1.0	Quantum mechanical correction factor.
dlq=0.0 m	Length delta for capacitor size.
dwq=0.0 m	Width delta for capacitor size.
dwr=0.0 m	Width delta for substrate resistance calculation.
cfrl=0.0 F/m	Fringing capacitance in length direction.
cfrw=0.0 F/m	Fringing capacitance in width direction.
rshg=1.0 Ω/sq	Gate sheet resistance.
rpv=0.0 Ω m^2	Vertical resistance down through gate in units of ohm*m^2.
rend=1.0e-04 Ω m	End resistance (extrinsic well res. plus vertical contact res. to well) per width.
rshs=1000.0 Ω/sq	Substrate sheet resistance.
uac=5.0e-02 m^2/V/s	Accumulation layer zero bias mobility.
uacred=0.0 /V	Accumulation layer mobility degradation factor.
stvfb=0.0 V/K	Temperature dependence of VFB.
strshg=0.0	Temperature dependence of RSHG.

© 2023 Cadence Design Systems, Inc.

`strpv=0.0`	Temperature dependence of RPV.
`strend=0.0`	Temperature dependence of REND.
`strshs=0.0`	Temperature dependence of RSHS.
`stuac=0.0`	Temperature dependence of UAC.
`feta=1.0`	Effective field parameter.
`swigate=0`	Flag for gate current: 0=turn off and 1=turn on.
`chibo=3.1 V`	Tunneling barrier height for electrons.
`chibpo=4.5 V`	Tunneling barrier height for holes.
`stig=2.0`	Common temperature coefficient for gate currents (ECB, HVB and HVB).
`lov=0.0 m`	Overlap length.
`novo=5.0e+25 /m`^{3}	Effective doping level of overlap regions.
`iginvlw=0.0 A`	ECB gate channel current pre-factor for 1 um^2 channel area.
`igovw=0.0 A`	ECB gate overlap current pre-factor for 1 um wide gate overlap region.
`gcoo=0.0`	ECB gate tunneling energy adjustment.
`gc2o=0.375`	ECB gate current slope factor.
`gc3o=0.063`	ECB gate current curvature factor.
`igchvlw=0.0 A`	HVB gate channel current pre-factor for 1 um^2 channel area.
`igovhvw=0.0 A`	HVB gate overlap current pre-factor for 1 um wide gate overlap region.
`gcohvo=0.0`	HVB gate tunneling energy adjustment.
`gc2hvo=0.375`	HVB gate current slope factor.
`gc3hvo=0.063`	HVB gate current curvature factor.
`minr=0.001`	Minimum resistor between bi and b.
`igmax=1.0e-05 A`	Maximum gate tunneling current.
`compatible=spectre`	Compatible parameters. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.

© 2023 Cadence Design Systems, Inc.

racnoise=1	Rac noise selector.
noscale=0	Enables or disables scale support.
dta=0.0 C	Temperature rise from ambient. It served as the default value of instance DTA.
trise=0.0 C	Alias of DTA.

Output Parameters

tempeff (C)	Effective temperature for a single device.
meff	Effective multiplicity factor (m-factor).

Operating-Point Parameters

v	voltage across capacitor.
i	Current through capacitor.
cap	LOw frequency capacitance.
qg	Intrinsic charge.
igc	Gate tunneling current.
igover	Gate overlap tunneling current.

Related Topics

PSP-Based MOS Varactor Model (mosvar)

Model Equations

Model Version Updates

Model Usage

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

27

EKV MOSFET Model (ekv)

The EPFL-EKV MOSFET model was developed by the Electronics Laboratories, Swiss Federal Institute of Technology (EPFL), Switzerland.

This description concentrates on the intrinsic part of the MOSFET. The extrinsic part of the MOSFET is handled as it is commonly made for other MOSFET models.

The EPFL-EKV MOSFET model is formulated as a *single expression*, which preserves the continuity of first- and higher-order derivatives with respect to any terminal voltage, in the entire range of validity of the model.

The EPFL-EKV MOSFET model version 2.6 includes modeling of the following physical effects:

- Basic geometrical and process-related aspects, such as oxide thickness, junction depth, and effective channel length and width
- Effects of doping profile and substrate effects
- Modeling of weak, moderate, and strong inversion behavior
- Modeling of mobility effects due to vertical and lateral fields and velocity saturation
- Short-channel effects, such as channel-length modulation (CLM), source and drain charge-sharing (including for narrow channel widths), and reverse short-channel effect (RSCE)
- Quasi-static charge-based dynamic model
- Thermal and flicker noise modeling
- First-order nonquasi-static model for the transadmittances

Coherence of Static and Dynamic Models

All aspects regarding the static, the quasi-static, and nonquasi-static dynamic and noise models are all derived in a coherent way from a single characteristic, the normalized

© 2023 Cadence Design Systems, Inc.

transconductance-to-current ratio. Symmetric normalized forward and reverse currents are used throughout these expressions. The Spectre® circuit simulator supports only one dynamic model, a charge-based model for the node charges and transcapacitances. The dynamic model, including the time constant for the nonquasi-static model, is described in symmetrical terms of the forward and reverse normalized currents. The charge formulation is further used to express the effective mobility dependence of the local field.

Bulk Reference and Symmetry

Voltages are all referred to the local substrate:

$V_G = V_{GB}$ Intrinsic gate-to-bulk voltage

$V_S = V_{\mathrm{SB}}$Intrinsic source-to-bulk voltage

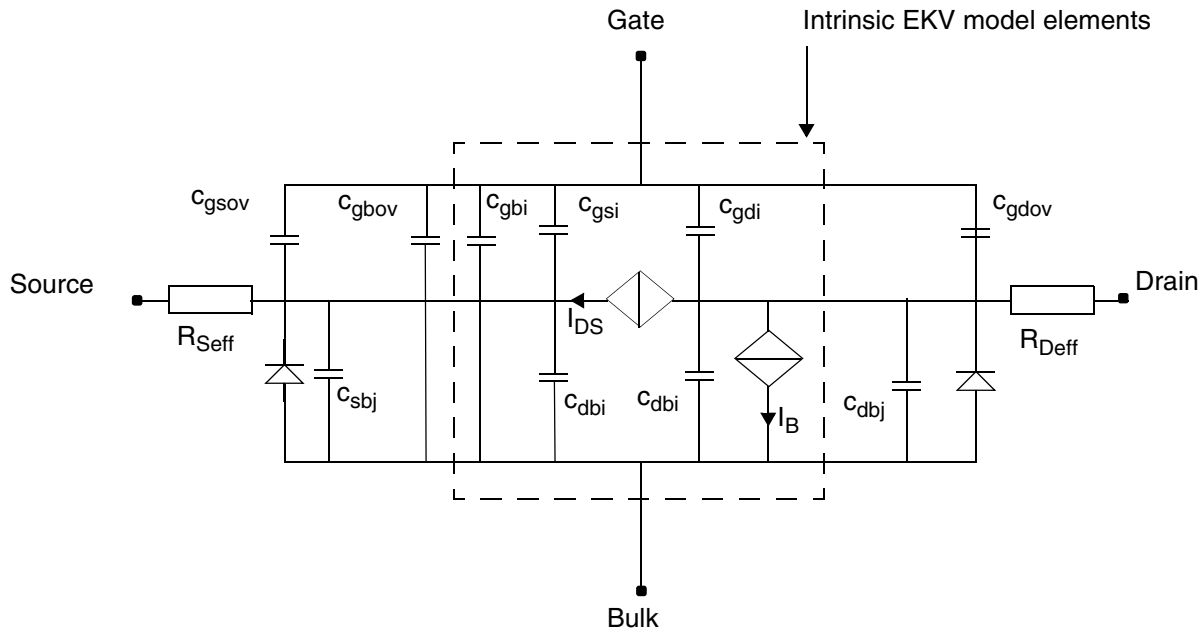
$V_D = V_{DB}$Intrinsic drain-to-bulk voltage

V_S and V_D are the intrinsic voltages, which means that the voltage drop over extrinsic resistive elements is supposed to already be accounted for externally. V_D is the electrical drain voltage such that $V_D \geq V_S$. Bulk reference allows the model to be handled symmetrically with respect to source and drain, a symmetry that is inherent in common MOS technologies (excluding asymmetric source-drain layouts).

Note: Intrinsic model equations are present for an N-channel MOSFET. P-channel MOSFETs are dealt with as pseudo-N-channels; that is, the polarity of the voltages (V_G, V_S, V_D, as well as VTO) is inverted before computing the current for PMOS, which is given a negative sign. No other distinctions are made between NMOS and PMOS, with the exception of the η factor for effective mobility calculation.

© 2023 Cadence Design Systems, Inc.

Equivalent Circuit



This figure represents the intrinsic and extrinsic elements of the MOS transistor. For quasi-static dynamic operation, only the intrinsic capacitances from the simpler capacitances model are shown in the figure. However, a charge-based transcapacitances model is also available for computer simulation.

Related Topics

Model Equations

Model Usage

Component Statements

© 2023 Cadence Design Systems, Inc.

Model Equations

Static Intrinsic Model

Basic Relations

(27-1)

$$\varepsilon_0\varepsilon_{si} = SCALE \cdot 104.5 \times 10^{-12}[F/m]$$

Thermal voltage

(27-2)

$$V_t = \frac{k \cdot T}{q}$$

Energy Gap

(27-3)

$$E_g(T) = 1.16 - 0.000702 \cdot \frac{T^2}{T + 1108}$$

Intrinsic Parameters Initialization

The basic intrinsic model parameters COX, $GAMMA$, PHI, VTO, KP, and $UCRIT$ are related to the fundamental process parameters TOX, $NSUB$, VFB, UO, $VMAX$, respectively, similarly as in early SPICE models.

If $UCRIT$ is not specified, it is initialized as

(27-4)

© 2023 Cadence Design Systems, Inc.

$$UCRIT = \begin{cases} VMAX/(UO \cdot 10^{-4}) & \text{for } VMAX > 0, UO > 0 \\ default & otherwise \end{cases}$$

If $E0$ is not specified, a simplified mobility model is used with the parameter $THETA$:

(27-5)

$$E0 = \begin{cases} 0 & if\ THETA\ specified \\ default & otherwise \end{cases}$$

Note: The value zero is given to $E0$ here, indicating that the simplified mobility model is used in conjunction with $THETA$ instead of the standard mobility model.

Intrinsic Parameters Temperature Dependence

(27-6)

$$VTO(T) = VTO - TCV \cdot (T - Tnom)$$

(27-7)

$$KP(T) = KP \cdot \left(\frac{T}{Tnom}\right)^{BEX}$$

(27-8)

$$UCRIT(T) = UCRIT \cdot \left(\frac{T}{Tnom}\right)^{UCEX}$$

(27-9)

$$PHI(T) = PHI \cdot \frac{T}{Tnom} - 3 \cdot V_t \cdot \ln\left(\frac{T}{Tnom}\right) - E_g Tnom \cdot \frac{T}{Tnom} + E_g(T)$$

(27-10)

© 2023 Cadence Design Systems, Inc.

$$IBB(T) = IBB \cdot [1.0 + IBBT \cdot (T - Tnom)]$$

Effective Channel Length and Width

(27-11)

$$W_{eff} = W + DW$$

(27-12)

$$L_{eff} = L + DL$$

Note: Contrary to the convention adopted in other MOSFET models, DL and DW usually have a negative value because of the preceding definition.

Short Distance Matching

Random mismatch between two transistors with identical layout and close to each other is in most cases suitably described by a law following the inverse of the square root of the transistors' area. The following relationships have been adopted:

(27-13)

$$VTO_a = VTO + \frac{AVTO}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

(27-14)

$$KP_a = KP \cdot \left(1 + \frac{AKP}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}\right)$$

(27-15)

© 2023 Cadence Design Systems, Inc.

$$GAMMA_a = GAMMA + \frac{AGAMMA}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

Note: Because negative values for both KP_a and $GAMMA_a$ are not physically meaningful, these are clipped at zero.

Reverse Short-Channel Effect (RSCE)

(27-16)

$$C_\varepsilon = 4 \cdot (22 \times 10^{-3})^2$$

(27-17)

$$C_A = 0.028$$

(27-18)

$$\xi = C_A \cdot \left(10 \cdot \frac{L_{eff}}{LK} - 1\right)$$

(27-19)

$$\Delta V_{RSCE} = \frac{2 \cdot Q0}{COX} \cdot \frac{1}{\left[1 + \frac{1}{2} \cdot \left(\xi + \sqrt{\xi^2 + C_\xi}\right)\right]^2}$$

Effective Gate Voltage Including RSCE

(27-20)

© 2023 Cadence Design Systems, Inc.

$$V_G' = V_G - VTO_a - \Delta V_{RSCE} + PHI + GAMMA_a\sqrt{PHI}$$

Effective Substrate Factor Including Charge-Sharing for Short and Narrow Channels

Pinchoff Voltage for Narrow-Channel Effect

(27-21)

$$V_{P0} = \begin{cases} V_G' - PHI - GAMMA_a\left(\sqrt{V_G' + \left(\frac{GAMMA_a}{2}\right)^2} - \frac{GAMMA_a}{2}\right) & \text{for } V_G' > 0 \\ -PHI & \text{for } V_G' \le 0 \end{cases}$$

Effective Substrate Factor Accounting for Charge Sharing

(27-22)

$$V'_{S(D)} = \frac{1}{2}\cdot\left[V_{S(D)} + PHI + \sqrt{(V_{S(D)} + PHI)^2 + (4V_t)^2}\right]$$

Note: The preceding equation prevents the argument of the square roots in the subsequent code from becoming negative.

(27-23)

$$\gamma^o = GAMMA_a - \frac{\varepsilon_0 \cdot \varepsilon_{Si}}{COX}\cdot\left[\frac{LETA}{L_{eff}}\cdot\left(\sqrt{V'_S} + \sqrt{V'_D}\right) - \frac{3\cdot WETA}{W_{eff}}\left(\sqrt{V_{P0} + PHI + 0.1\cdot V_t}\right)\right]$$

(27-24)

© 2023 Cadence Design Systems, Inc.

$$\gamma' = \frac{1}{2} \cdot \left(\gamma^{o} + \sqrt{\gamma^{o2} + 0.1 \cdot V_t} \right)$$

Note: The purpose of the preceding equation is to prevent the effective substrate factor from becoming negative.

Pinchoff Voltage Including Short- and Narrow-Channel Effects

(27-25)

$$V_P = \begin{cases} V_G' - PHI - \gamma' \left(\sqrt{V_G' + \left(\frac{\gamma'}{2} \right)^2} - \frac{\gamma'}{2} \right) & \text{for } V_G' > 0 \\ -PHI & \text{for } V_G' \le 0 \end{cases}$$

Slope Factor

(27-26)

$$n = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 4V_t}}$$

Large-Signal Interpolation Function

$F(v)$ is the large-scale interpolation function relating the normalized currents to the normalized voltages. A simple and accurate expression for the transconductance interpolation allows a consistent formulation of the static large-signal interpolation function, the dynamic model for the intrinsic charges (and capacitances), and the intrinsic time constant and the thermal noise model.

(27-27)

© 2023 Cadence Design Systems, Inc.

$$gms \cdot V_t / I_D = \frac{\sqrt{0.25 + i} - 0.5}{i}$$

Large-signal interpolation function:

(27-28)

$$y = \sqrt{0.25 + i} - 0.5$$

(27-29)

$$v = 2y + \ln(y)$$

Unfortunately, the preceding equation cannot be inverted analytically. However, it can be inverted using a Newton-Raphson iterative scheme. Currently, a simplification of this algorithm that avoids iteration is used, leading to a continuous expression for the large-signal interpolation function.

Large-Signal Interpolation Function for Hand Calculation

For hand calculations, an analytically simple interpolation function, presenting the same asymptotic behavior with slightly reduced accuracy in moderate inversion, can be used:

(27-30)

$$F(v) = [\ln(1 + \exp(v/2))]^2$$

Forward Normalized Current

(27-31)

© 2023 Cadence Design Systems, Inc.

$$i_f = F\left[\frac{V_P - V_S}{V_t}\right]$$

Velocity Saturation Voltage

(27-32)

$$V_C = UCRIT \cdot L_{eff}$$

(27-33)

$$V_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \sqrt{i_f}} - \frac{1}{2}\right]$$

Note: The variable V_{DSS} in this formulation for computer simulation is half the value of the actual saturation voltage.

Drain-to-Source Saturation Voltage for Reverse Normalized Current

(27-34)

$$V_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \left(\sqrt{i_f} - \frac{3}{4} \cdot \ln(i_f)\right)} - \frac{1}{2}\right] + V_t \cdot \left[\ln\left(\frac{V_C}{2V_t}\right) - 0.6\right]$$

Channel-Length Modulation

(27-35)

$$\Delta V = 4 \cdot V_t \cdot \sqrt{LAMBDA \cdot \left(\sqrt{i_f} - \frac{V_{DSS}}{V_t}\right) + \frac{1}{64}}$$

(27-36)

© 2023 Cadence Design Systems, Inc.

$$\Delta L = LAMBDA \cdot L_C \cdot \ln\left(1 + \frac{V_{ds} - V_{ip}}{L_C \cdot UCRIT}\right)$$

(27-37)

$$V_{ds} = \frac{V_D - V_S}{2}$$

(27-38)

$$L_C = \sqrt{\frac{\varepsilon_0 \varepsilon_{si}}{COX} \cdot XJ}$$

(27-39)

$$V_{ip} = \sqrt{V_{DSS}^2 + \Delta V^2} - \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2}$$

Equivalent Channel Length Including Channel-Length Modulation and Velocity Saturation

(27-40)

$$L' = L_{eff} - \Delta L + \frac{V_{ds} + V_{ip}}{UCRIT}$$

(27-41)

$$L_{min} = L_{eff} / 10$$

(27-42)

© 2023 Cadence Design Systems, Inc.

$$L_{eq} = \frac{1}{2} \cdot \left(L' + \sqrt{L'^2 + L_{min}^2} \right)$$

Note: The preceding equation prevents the equivalent channel length from becoming zero or negative.

Reverse Normalized Current

Reverse Normalized Current

(27-43)

$$i_r' = F\left[\frac{V_P - V_{ds} - V_S - \sqrt{V_{DSS}^2 + \Delta V^2} + \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2}}{V_t} \right]$$

Reverse Normalized Current for Mobility Model, Intrinsic Charges/Capacitances, and NQS Time Constant

(27-44)

$$i_r = F\left[\frac{V_P - V_D}{V_t} \right]$$

Transconductance Factor and Mobility Reduction Due to Vertical Field

(27-45)

$$\beta_0 = KP_a \cdot \frac{NP \cdot W_{eff}}{NS \cdot L_{eq}}$$

Note: The use of the device parameter NP (or M) gives accurate results for the simulation of parallel devices, whereas the use of NS for series devices is only approximate.

© 2023 Cadence Design Systems, Inc.

(27-46)

$$\eta = \begin{cases} 1/2 & \text{for NMOS} \\ 1/3 & \text{for PMOS} \end{cases}$$

(27-47)

$$q_{B0} = GAMMA_a \cdot \sqrt{PHI}$$

(27-48)

$$\beta_0' = \beta_0 \cdot \left(1 + \frac{COX}{E0 \cdot \varepsilon_0 \varepsilon_{si}} \cdot q_{B0}\right)$$

(27-49)

$$\beta = \frac{\beta_0'}{1 + \frac{COX}{E0 \cdot \varepsilon_0 \varepsilon_{si}} \cdot V_t \cdot \left|q_B + \eta \cdot q_I\right|}$$

For the definition of the normalized bulk and inversion charges q_B and q_I, refer to Normalized Intrinsic Node Charges.

Note: This formulation arises from the exact integration of the local effective field as a function of depletion and inversion charge densities along the channel. The bias dependence, in particular with the substrate bias, is accounted for due to the dependency on the channel charges.

Mobility Reduction Model Used in Former EKV Model Versions

For reasons of compatibility with EKV model versions before 2.6, a simpler mobility reduction model that uses the parameter $THETA$ can be used. The choice among model versions is made using the model version selector $UPDATE$. Check with the documentation in your simulator. If a model version $UPDATE$<2.6 is specified, the former mobility reduction model is chosen:

(27-50)

© 2023 Cadence Design Systems, Inc.

$$V_P' = \frac{1}{2} \cdot \left(V_P + \sqrt{V_P^2 + 2V_t} \right)^2$$

(27-51)

$$\beta = \frac{\beta_0}{1 + THETA \cdot V_P'}$$

Specific Current

(27-52)

$$I_S = 2 \cdot n \cdot \beta \cdot V_t^2$$

Drain-to-Source Current

(27-53)

$$I_{DS} = I_S \cdot (i_f - i'_r)$$

Note: This drain current expression is a single equation, valid in all operating regions: weak, moderate, and strong inversion; conduction; and saturation. It is therefore not only continuous among all these regions, it is also continuously derivable.

Impact Ionization Current

(27-54)

$$V_{ib} = V_D - V_S - IBN \cdot 2 \cdot V_{DSS}$$

(27-55)

© 2023 Cadence Design Systems, Inc.

$$I_B = \begin{cases} I_{DS} \cdot \frac{IBA}{IBB} \cdot V_{ib} \cdot \exp\left(\frac{-IBB \cdot L_C}{V_{ib}}\right) & \text{for } V_{ib} > 0 \\ 0 & \text{for } V_{ib} \le 0 \end{cases}$$

Note: The factor 2 in the expression for V_{ib} accounts for the fact that the numerical value of V_{DSS} is half the actual saturation voltage. The substrate current is intended to be treated as a component of the total extrinsic drain current, flowing from the drain to the bulk. It therefore also affects the total extrinsic conductances, in particular the drain conductance.

Quasi-static Model

Both a charge-based model for transcapacitances, allowing charge conservation during transient analysis, and a simpler capacitances-based model are available.

Note: The charges model is in principle formulated in symmetric terms of the forward and reverse normalized currents, that is, symmetrical for both drain and source sides. Further, short-channel effects, such as charge sharing and reverse short-channel effects, are included in the dynamic model through the pinchoff voltage.

Dynamic Model for the Intrinsic Node Charges

(27-56)

$$n_q = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 10^{-6}}}$$

Normalized Intrinsic Node Charges

(27-57)

$$x_f = \sqrt{\frac{1}{4} + i_f}$$

(27-58)

© 2023 Cadence Design Systems, Inc.

$$x_r = \sqrt{\frac{1}{4} + i_r}$$

(27-59)

$$qQ_d = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_r^3 + 6x_r^2 x_f + 4x_r x_f^2 + 2x_f^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

(27-60)

$$q_S = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_f^3 + 6x_f^2 x_r + 4x_f x_r^2 + 2x_r^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

(27-61)

$$q_I = q_S + q_D = -n_q \cdot \left(\frac{4}{3} \cdot \frac{x_f^2 + x_f x_r + x_r^2}{x_f + x_r} - 1 \right)$$

(27-62)

$$q_B = \begin{cases} \left(-GAMMA_a \cdot \sqrt{V_P + PHI + 10^{-6}} \right) \cdot \frac{1}{V_t} - \left(\frac{n_q - 1}{n_q} \right) \cdot q_I & \text{for } V'_G > 0 \\ -V'_G \cdot \frac{1}{V_t} & \text{for } V'_G \le 0 \end{cases}$$

(27-63)

© 2023 Cadence Design Systems, Inc.

$$q_G = -q_I - q_{OX} - q_B$$

q_{OX} is a fixed-oxide charge assumed to be zero. The preceding equation expresses the charge conservation among the four nodes of the transistor.

Total Node Charges

(27-64)

$$C_{OX} = COX \cdot NP \cdot W_{eff} \cdot NS \cdot L_{eff}$$

(27-65)

$$Q_{(I,B,D,S,G)} = C_{ox} \cdot V_t \cdot q_{(I,B,D,S,G)}$$

Intrinsic Capacitances

Transcapacitances

The intrinsic capacitances are obtained through derivation of the node charges with respect to the terminal voltages. This results in simple analytical functions for all the trancapacitances in terms of x_f, x_r, the pinchoff voltage, the slope factor, and derivatives thereof.

Normalized Intrinsic Capacitances

A simpler model using the five intrinsic capacitances corresponding to the equivalent circuit shown in Equivalent Circuit can be obtained when neglecting the slight dependence on the slope factor n, resulting in the following simple functions:

(27-66)

$$c_{gs} = \frac{2}{3} \cdot \left(1 - \frac{x_r^2 - x_r + \frac{1}{2} x_f}{(x_f + x_r)^2} \right)$$

(27-67)

© 2023 Cadence Design Systems, Inc.

$$c_{gd} = \frac{2}{3} \cdot \left(1 - \frac{x_f^2 - x_f + \frac{1}{2} x_r}{(x_f + x_r)^2} \right)$$

(27-68)

$$c_{gb} = \left(\frac{n_q - 1}{n_q} \right) \cdot (1 - c_{gs} - c_{gd})$$

(27-69)

$$c_{sb} = (n_q - 1) \cdot c_{gs}$$

(27-70)

$$c_{db} = (n_q - 1) \cdot c_{gd}$$

Total Intrinsic Capacitances

(27-71)

$$C_{(gs,gd,gb,sb,db)} = C_{ox} \cdot c_{(gs,gd,gb,sb,db)}$$

Nonquasi-static (NQS) Model

The EKV model includes a first-order NQS model for small-signal (`.AC`) simulations. The expression of the NQS drain current is obtained from the quasi-static value of the drain current, which is then first-order low-pass filtered. NQS is a flag (model parameter) allowing you to disable the NQS model, and τ is the bias-dependent characteristic time constant.

© 2023 Cadence Design Systems, Inc.

Intrinsic Time Constant

τ_0 is the intrinsic time constant defined as

(27-72)

$$\tau_0 = \frac{COX}{2 \cdot \beta \cdot V_t} = \frac{(NS \cdot L_{eff})^2}{2 \cdot \mu_{eff} \cdot V_t}$$

(27-73)

$$\tau = \tau_0 \cdot \frac{4}{15} \cdot \frac{(x_f^2 + 3x_f x_r + x_r^2)}{(x_f + x_r)^3}$$

(27-74)

$$I_{DS}(s) = \frac{I_{DSq}(s)}{1 + NQS \cdot s \cdot \tau}$$

The corresponding small-signal (`.AC`) transadmittances are then given by

(27-75)

$$Y_m(s) = \frac{g_m}{1 + NQS \cdot s \cdot \tau}$$

(27-76)

$$Y_{ms}(s) = \frac{g_{ms}}{1 + NQS \cdot s \cdot \tau}$$

(27-77)

© 2023 Cadence Design Systems, Inc.

$$Y_{ds}(s) = \frac{g_{ds}}{1 + NQS \cdot s \cdot \tau}$$

(27-78)

$$Y_{mbs}(s) = Y_{ms}(s) - Y_{m}(s) - Y_{ds}(s)$$

where g_m, g_{ms}, and g_{ds} are the transconductances and output conductance evaluated at the operating point.

Intrinsic Noise Model

The noise is modeled by a current source I_{NDS} betwe en intrinsic source and drain. It is composed of a thermal noise component and a flicker noise component and has the following power spectral density (PSD):

(27-79)

$$S_{INDS} = S_{thermal} + S_{flicker}$$

Thermal Noise

If model parameter `nlevel=1`,

(27-80)

$$S_{thermal} = \frac{8 \times kT \times |gm|}{3}$$

else

(27-81)

© 2023 Cadence Design Systems, Inc.

$$S_{thermal} = 4kT \cdot \frac{\mu_{eff}}{(NS \cdot L_{eff})^2} \cdot |Q_I| = 4kT \cdot \beta \cdot |q_I|$$

Note: The thermal noise expression is *valid in all regions of operation*, including for small V_{DS}.

Flicker Noise

When model parameter `noisemod=1`,

(27-82)

$$S_{flicker} = \frac{KF \times |Ids|^{AF}}{NP \cdot W_{eff} \cdot NS \cdot L_{eff} \cdot COX \cdot f^{EF}}$$

When model parameter `noisemod=2`,

(27-83)

$$S_{flicker} = \frac{KF \cdot |Ids|^{AF}}{NP \cdot L_{eff} \cdot NS \cdot L_{eff} \cdot COX \cdot f^{EF}}$$

When model parameter `noisemod=3`,

(27-84)

$$S_{flicker} = \frac{KF \cdot gm^2}{NP \cdot W_{eff} \cdot NS \cdot L_{eff} \cdot COX \cdot f^{AF}}$$

Related Topics

EKV MOSFET Model (ekv)

Model Usage

© 2023 Cadence Design Systems, Inc.

Component Statements

Model Usage

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Sample Instance Statement

```
mn1 (dn gn sn 0) ekvnmos w=1.5u l=1u ad=2.6p as=2.6p pd=6.6p ps=6.6p nrd=1.54
nrs=1.54
```

Model Syntax

```
model modelName ekv parameter=value ...
```

Sample Model Statement

```
model ekvnmos ekv type=n update=2.6 xqc=0.4 cox=3.4e-3 xj=0.145e-6 vto=0.6
gamma=0.71 phi=0.967 kp=155e-6 e0=88e6 iba=200e6 ibb=350e6 tnom=25 tcv=1.55e-3
bex=-1.45 kf=1e-27 af=1 hdif=0.94e-6 rsh=512 jsw=1.5e-10
```

Related Topics

EKV MOSFET Model (ekv)

Model Equations

Component Statements

Component Statements

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

w (m)	Channel width.
l (m)	Channel length.
as (m^2)	Area of source diffusion.
ad (m^2)	Area of drain diffusion.
ps (m)	Perimeter of source diffusion.
pd (m)	Perimeter of drain diffusion.
nrd (m/m)	Number of squares of drain diffusion.
nrs (m/m)	Number of squares of source diffusion.
rdc (Ohm)	Drain contact resistance.
rsc (Ohm)	Source contact resistance.
m=1	Multiplicity factor (number of MOSFETs in parallel).
ns=1	Series Multiplicity factor (number of MOSFETs in series).
region=triode	Estimated operating region. Spectre outputs a number (0-3) in rawfile. Possible values are off, triode, sat, or subth.
trise	Temperature rise from ambient.
isnoisy=yes	Should device generate noise. Possible values are no or yes.

Model Parameters

Device type parameters:

type=n	Transistor type. Possible values are n or p.
vnds=-1.0 m	Reverse diode current transition point.
nds=1.0 m	Reverse bias slope coefficient.

© 2023 Cadence Design Systems, Inc.

`compatible=spectre`	Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax. Possible values are spectre, spice2, spice3, cdsspice, spiceplus, eldo, or sspice.

Process parameters:

`tox=2e-8 m`	Gate oxide thickness.
`cox=7e-4 F/m^2`	Gate oxide capacitance. (Overrides Tox).
`xj=1.0e-7 m`	Metallurgical junction depth.
`dw=0 m`	Channel Width Correction.
`dl=0 m`	Channel Length Correction.
`nfs=0 cm^-2`	Fast surface state density.
`nsub=1.13e16 cm^-3`	Channel doping concentration.

Drain current model parameters:

`vto=0.5 V`	Threshold voltage at zero body bias.
`gamma=1.0 sqrt(V)`	Body-effect parameter.
`phi=0.7 V`	Surface potential at strong inversion.
`kp=5.0e-5 A/V^2`	Transconductance parameter.
`e0=1.0e12 V/m`	Vertical Critical Field.
`ucrit=2.0e6 V/cm`	Longitudinal Critical field for mobility degradation.
`theta=0.0 1/V`	Mobility reduction coefficient.
`uo=710 cm^2/V*s`	Carrier surface mobility.
`vmax (m/s)`	Carrier saturation velocity.
`vfb (V)`	Flat-band voltage.
`lambda=0.5`	Channel length modulation parameter.
`weta=0.25`	Narrow Channel Effect Coefficient.
`leta=0.1`	Short Channel Effect Coefficient.

© 2023 Cadence Design Systems, Inc.

`xw=0 m`	Width variation due to masking and etching.
`xl=0 m`	Length variation due to masking and etching.
`meto=0 m`	Metal overlap in fringing field.

Impact ionization parameters
:

`iba=0 1/m`	First Impact Ionization Coefficient.
`ibb=3.0e8 V/m`	Second Impact Ionization Coefficient.
`ibc=0`	Third Impact Ionization Coefficient.
`ibn=1.0`	Saturation velocity factor for impact ionization.

Reverse Short Channel parameters
:

`q0=0 A*s/m^2`	Reverse short channel peak charge density.
`lk=2.9e-7 m`	Reverse short channel characteristic length.

Charge model selection parameters:

`xqc=0.0`	Drain/source channel charge partition in saturation for charge models, e.g. use 0.4 for 40/60, 0.5 for 50/50, 0 for 0/100.

Junction diode model parameters:

`is=1e-14 A`	Bulk junction reverse saturation current.
`js (A/m^2)`	Bulk junction reverse saturation current density.
`jsw=0 A/m`	Bulk junction reverse saturation sidewall current density.
`n=1`	Junction emission coefficient.
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol'. Possible values are no or yes.

© 2023 Cadence Design Systems, Inc.

`imelt=`imax' A`	Explosion current, diode is linearized beyond this current to aid convergence.

Junction capacitance model parameters:

`cbd=0 F`	Bulk-drain zero-bias p-n capacitance.
`cbs=0 F`	Bulk-source zero-bias p-n capacitance.
`cj=0 F/m^2`	Zero-bias junction bottom capacitance density.
`cjsw=0 F/m`	Zero-bias junction sidewall capacitance density.
`mj=0.5`	Bulk junction bottom grading coefficient.
`mjsw=0.33`	Bulk junction sidewall grading coefficient.
`cjswg=0 F/m`	Gate-side zero-bias junction sidewall capacitance density.
`mjswg=0.33`	Gate-side bulk junction sidewall grading coefficient.
`pbswg=0.8 V`	Gate-side junction built-in potential.
`fc=0.5`	Forward-bias capacitance coefficient.
`pb=0.8 V`	ulk p-n bottom contact potential.
`pbsw=0.8 V`	Side-wall contact potential.
`tt=0.0 V`	Bulk p-n transit time.
`fcsw=0.5`	Side-wall forward-bias depletion capacitance threshold.

Overlap capacitance parameters:

`cgso=0 F/m`	Gate-source overlap capacitance.
`cgdo=0 F/m`	Gate-drain overlap capacitance.
`cgbo=0 F/m`	ate-bulk overlap capacitance.

© 2023 Cadence Design Systems, Inc.

Parasitic resistance parameters:

`rs=0 Ohm`	Source resistance.
`rd=0 Ohm`	Drain resistance.
`rsh=0 Ohm/sqr`	Source/drain diffusion sheet resistance.
`rss=0 Ohm*m`	Scalable source resistance.
`rdd=0 Ohm*m`	Scalable drain resistance.
`rsc=0 Ohm`	Source contact resistance.
`rdc=0 Ohm`	Drain contact resistance.
`minr=0.1 Ohm`	Minimum source/drain resistance.
`ldif=0 m`	Lateral diffusion beyond the gate.
`hdif=0 m`	Length of heavily doped diffusion.

Short distance matching parameters:

`avto=0 V*m`	Area related threshold voltage mismatch parameter.
`akp=0 m`	Area related gain mismatch parameter.
`agamma=0 sqrt(V)*m`	Area related body effect mismatch parameter.

Operating region warning control parameters:

`alarm=none`	Forbidden operating region. Possible values are none, off, triode, sat, subth, or rev.
`imax=1 A`	Maximum current, currents above this limit generate a warning.
`jmax=1e8 A/m^2`	Maximum current density, currents above this limit generate a warning.
`vbox=1e9*tox V`	Oxide breakdown voltage.
`bvj=infinity V`	Junction reverse breakdown voltage.

© 2023 Cadence Design Systems, Inc.

Temperature effects parameters:

`tnom (C)`	Parameters measurement temperature. Default set by `options'.
`trise=0 C`	Temperature rise from ambient.
`tcv=1.0e-3 V/C`	Threshold voltage temperature coefficient.
`bex=-1.5`	Mobility temperature exponent.
`ucex=0.8`	Longitudinal critical field temp. exponent.
`ibbt=9.0e-4 1/C`	Temperature coefficient for IBB.
`xti=3`	Saturation current temperature exponent.
`tlev=0`	DC temperature selector.
`tlevc=0`	C temperature selector.
`phitmod=0`	hi(T) selector for sanyo.
`eg=1.12452 V`	Energy band gap.
`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.
`tr1=0.6`	First source-drain resistance temperature coefficient.
`tr2=0.6`	Second source-drain resistance temperature coefficient.
`ptc=0 V/C`	Surface potential temperature coefficient.
`pta=0 V/C`	Junction potential temperature coefficient.
`ptp=0 V/C`	Sidewall junction potential temperature coefficient.
`cta=0 1/C`	Junction capacitance temperature coefficient.
`ctp=0 1/C`	Sidewall junction capacitance temperature coefficient.

Default instance parameters:

`w=3e-6 m`	Default channel width.
`l=3e-6 m`	Default channel length.
`as=0 m^2`	Default area of source diffusion.

© 2023 Cadence Design Systems, Inc.

`ad=0 m^2`	Default area of drain diffusion.
`ps=0 m`	Default perimeter of source diffusion.
`pd=0 m`	Default perimeter of drain diffusion.
`nrd=0 m/m`	Default number of squares of drain diffusion.
`nrs=0 m/m`	Default number of squares of source diffusion.

Noise model parameters:

`noisemod=1`	Noise model selector.
`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`ef=1`	Flicker (1/f) noise frequency exponent.
`nlevel=1`	Noise level selector just for spice3 compatible.

Model selection parameters:

`nqs=0`	Nonquasi-static flag.
`satlim=exp(4)`	Ratio defining saturation limit.
`ekvint=0.0`	Interpolation function selector.
`scalem=1.0`	Model scaling factor.
`update=2.6`	Model version selector.

Auto Model Selector parameters:

`wmax=1.0 m`	Maximum channel width for which the model is valid.
`wmin=0.0 m`	Minimum channel width for which the model is valid.
`lmax=1.0 m`	Maximum channel length for which the model is valid.
`lmin=0.0 m`	Minimum channel length for which the model is valid.

© 2023 Cadence Design Systems, Inc.

msgskip=off	Skip some warning message customer requested. Possible values are off or on.

DC-mismatch model parameters:

mvtwl=0.0 V*m	Threshold mismatch area dependence.
mvtwl2=0.0 v*m^1.5	Threshold mismatch area square dependence.
mvt0=0.0 V	Threshold mismatch intercept.
mbe0=0.0	Beta mismatch intercept.
mbewl=0.0 m	Beta mismatch area dependence.

Imax and Imelt

The imax parameter aids convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for current up toimax. If imax is exceeded during iterations, the linear model is substituted until the current drops below imax or until convergence is achieved. If convergence is achieved with the current exceeding imax, the results are inaccurate, and a warning is printed out.

A separate model parameter, imelt, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds imelt, the base and collector currents are composed of many exponential terms, a warning will be issued and the results become inaccurate. The junction current is linearized above the value of `imelt' to prevent arithmetic exception, with the exponential term replaced by a linear equation at imelt.

Both of these parameters have current density counterparts, jmax and jmelt, that you can specify if you want the absolute current values to depend on the device area.

Auto Model Selection

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group

© 2023 Cadence Design Systems, Inc.

is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax', `lmin', `wmax', and `wmin' should be given. The selection criteria to choose a model is as follows:

```
lmin <= inst_length < lmax  and   wmin <= inst_width  < wmax
```

Example:

```
model ModelName ModelType {
   1:     <model parameters> lmin=2 lmax=4 wmin=1 wmax=2
   2:     <model parameters> lmin=1 lmax=2 wmin=2 wmax=4
   3:     <model parameters> lmin=2 lmax=4 wmin=4 wmax=6
}
```

Then for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

Output Parameters

`weff (m)`	Effective channel width (alias lv2).
`leff (m)`	Effective channel length (alias lv1).
`rseff (Ohm)`	Effective source resistance (alias lv16).
`rdeff (Ohm)`	Effective drain resistance (alias lv17).
`aseff (m^2)`	Effective source area (alias=lv4).
`adeff (m^2)`	Effective drain area (alias=lv3).
`pseff (m)`	Effective source perimeter (alias=lv12).
`pdeff (m)`	Effective drain perimeter (alias=lv11).

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are n or p.
`region=triode`	Estimated operating region. Spectre generates output number (0-3) in a rawfile. Possible values are off, triode, sat, or subth.
`reversed`	Reverse mode indicator. Possible values are no or yes.
`ids (A)`	Resistive drain-to-source current.
`vgs (V)`	Gate-source voltage (alias lx2).
`vds (V)`	Drain-source voltage (alias lx3).
`vbs (V)`	Bulk-source voltage (alias lx1).
`vp (V)`	Pinchoff voltage.
`vth (V)`	Threshold voltage.
`vdss (V)`	Drain-source saturation voltage.
`gm (S)`	Common-source transconductance (alias lx7).
`gds (S)`	Common-source output conductance (alias lx8).
`gmbs (S)`	Body-transconductance (alias lx9).
`nfac`	Slope factor.
`if (A)`	Forward current.
`ir (A)`	Reverse current.
`irprime (A)`	Reverse current.
`isub (A)`	Substrate Current.
`ibd (A)`	Bulk-drain junction current.
`ibs (A)`	Bulk-source junction current.
`pwr (W)`	Power at op point.
`gmoverid (1/V)`	`Gm'/`Ids'.
`gamma (sqrt(V))`	Body-effect parameter.
`cjd (F)`	Drain-bulk junction capacitance (alias lx29).
`cjs (F)`	Source-bulk junction capacitance (alias lx28).
`cgg (F)`	Gate-gate capacitance.

© 2023 Cadence Design Systems, Inc.

`cgd (F)`	Gate-drain capacitance (alias lx19).
`cgs (F)`	Gate-source capacitance (alias lx20).
`cgb (F)`	Gate-bulk capacitance.
`cdg (F)`	Drain-gate capacitance (alias lx32).
`cdd (F)`	Drain-drain capacitance (alias lx33).
`cds (F)`	Drain-source capacitance (alias lx34).
`cdb (F)`	Drain-bulk capacitance.
`csg (F)`	Source-gate capacitance.
`csd (F)`	Source-drain capacitance.
`css (F)`	Source-source capacitance.
`csb (F)`	Source-bulk capacitance.
`cbg (F)`	Bulk-gate capacitance (alias lx21).
`cbd (F)`	Bulk-drain capacitance (alias lx22).
`cbs (F)`	Bulk-source capacitance (alias lx23).
`cbb (F)`	Bulk-bulk capacitance.
`vm (V)`	Early voltage.
`vovrdr (V)`	Overdrive voltage.
`tau (s)`	NQS time constant.
`tau0 (s)`	Intrinsic time constant.
`ron (Ohm)`	On-resistance.

Related Topics

EKV MOSFET Model (ekv)

Model Equations

Model Usage

© 2023 Cadence Design Systems, Inc.

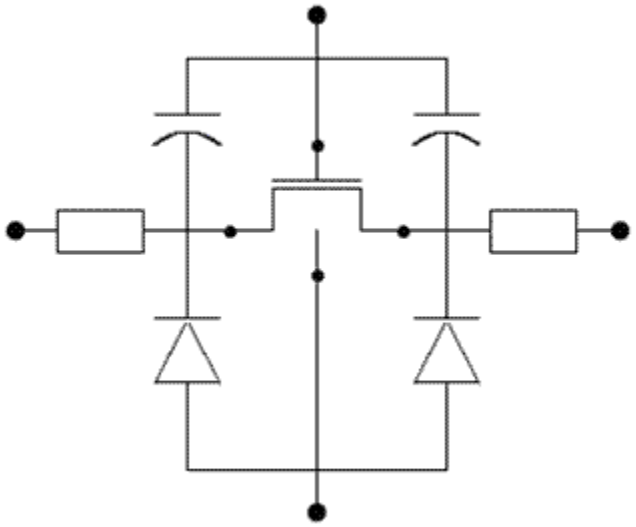
28

EKV3 MOSFET Model (ekv3)

© 2023 Cadence Design Systems, Inc.

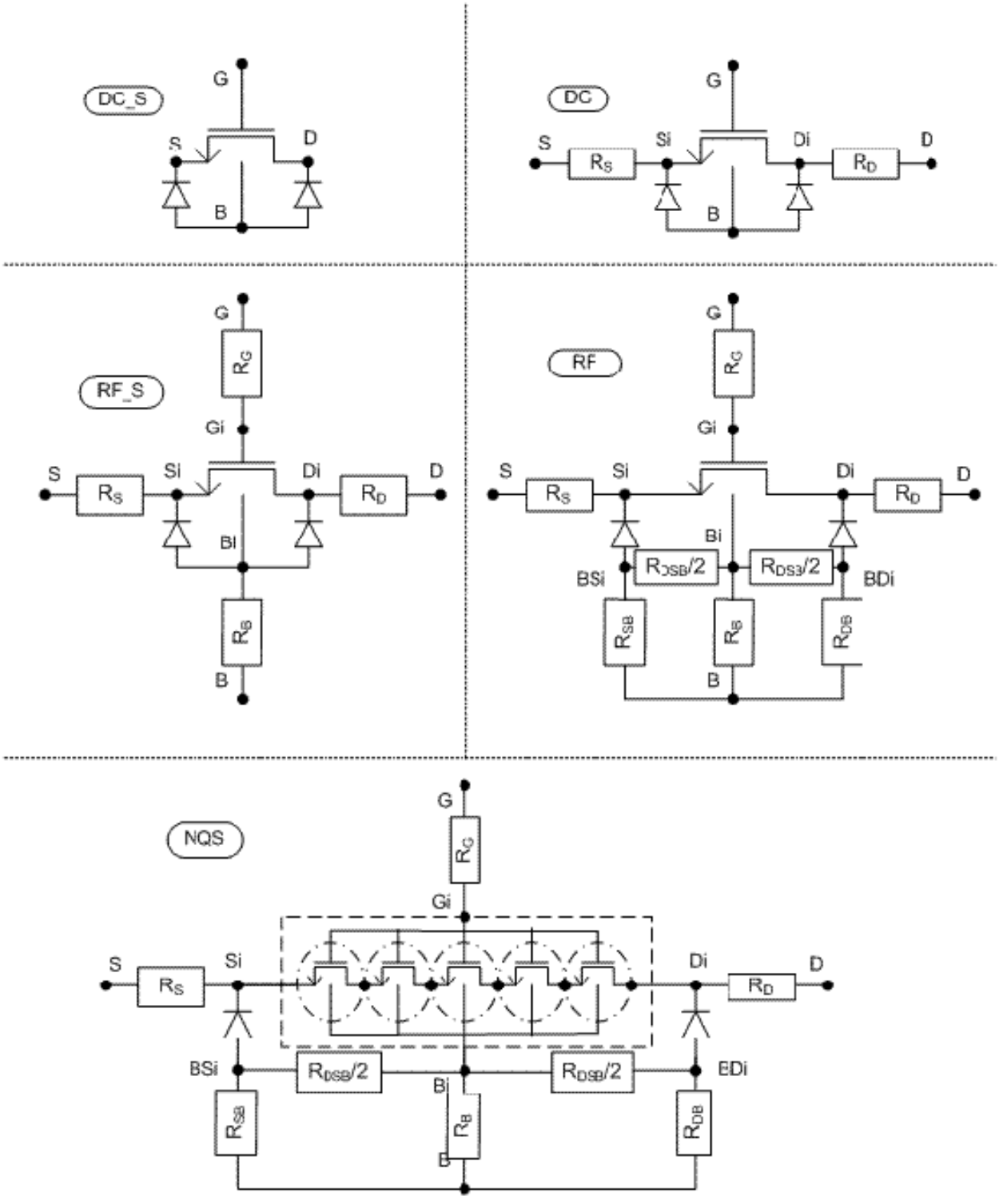
Modes

The low-frequency macro model of the EKV3 model is shown in Figure 26.1. The EKV3 model supports five versions of internal circuitry. Each version covers the needs of certain areas.l



Mode Name	Description	Internal Nodes
DC_S	No external resistors	0
DC	External series resistors	2
RF_S	External series resistors, gate resistor and 4 single substrate resistor	4
RF	External series resistors, gate resistor and 6 full substrate resistor network	6
NQS	External series resistors, gate resistor and 10 full substrate resistor network; minimal channel segmentation	10

© 2023 Cadence Design Systems, Inc.



© 2023 Cadence Design Systems, Inc.

Related Topics

Model Equations

Model Usage

Component Statements

Device ekv3_nqs (ekv3_nqs)

Device ekv3_r4 (ekv3_r4)

Device ekv3_rf (ekv3_rf)

Device ekv3_s (ekv3_s)

© 2023 Cadence Design Systems, Inc.

Model Equations

(28-1)

$$t_{si} = \frac{\epsilon_{si}}{COX}$$

$$t_{ox} = \frac{\epsilon_{ox}}{COX}$$

$$LC = \sqrt{t_{si} \cdot XJ}$$

Instance Level

Effective Geometry

(28-2)

$$L_{scaled} = L \cdot SCALE + XL$$

$$W_{scaled} = W \cdot SCALE + WL$$

$$L_{eff} = L_{scaled} + DL + \frac{WDL}{W_{scaled}} + \frac{LL}{L_{scaled}^{LLN}}$$

$$W_{eff} = W_{scaled} + DW + \frac{LDW}{L_{scaled}}$$

$$L_{eff,C} = L_{eff} + DLC$$

$$W_{eff,C} = W_{eff} + DWC$$

Matching

(28-3)

$$VTO_a = VTO + \frac{AVTO \cdot 10^6}{\sqrt{W_{eff} \cdot L_{eff}}}$$

$$GAMMA_a = GAMMA + \frac{AGAMMA \cdot 10^6}{\sqrt{W_{ef} \cdot L_{eff}}}$$

$$KP_a = KP \left(1 + \frac{AKP \cdot 10^6}{\sqrt{W_{ef} \cdot L_{eff}}}\right)$$

© 2023 Cadence Design Systems, Inc.

Long and wide channel correction of VTO and GAMMA

(28-4)

$$\Delta VT_L = -AVT \cdot MX_S(\ln \frac{L_{eff}}{LVT}, 0, 10^{-2})$$

$$\Delta VT_W = -AVT \cdot MX_S(\ln \frac{W_{eff}}{WVT}, 0, 10^{-2})$$

$$\Delta GAMMA_L = -AGAM \cdot MX_S(\ln \frac{L_{eff}}{LGAM}, 0, 10^{-2})$$

$$\Delta GAMMA_W = -AGAM \cdot MX_S(\ln \frac{W_{eff}}{WGAM}, 0, 10^{-2})$$

Parameter width and length scaling

(28-5)

$$LR_g = LR + \frac{WLR}{W_{eff}}$$

$$QLR_g = QLR \cdot \left(1 + \frac{WQLR}{W_{eff}}\right)$$

$$NLR_g = NLR \cdot \left(1 + \frac{WNLR}{W_{eff}}\right)$$

$$E0_g = E0 \cdot \left(1 + \frac{WE0}{W_{eff}}\right)$$

$$E1_g = E1 \cdot \left(1 + \frac{WE1}{W_{eff}}\right)$$

$$UCRIT_g = UCRIT \cdot \left(1 + \frac{WUCRIT}{W_{eff}}\right)$$

$$LAMBDA_g = LAMBDA \cdot \left(1 + \frac{WLAMBDA}{W_{eff}}\right)$$

$$ETAD_g = ETAD \cdot \left(1 + \frac{WETAD}{W_{eff}}\right)$$

$$UCEX_g = UCEX \cdot \left(1 + \frac{WUCEX}{W_{eff}}\right)$$

$$WR_g = WR + \frac{LWR}{L_{eff}}$$

$$QWR_g = QWR \cdot \left(1 + \frac{LQWR}{L_{eff}}\right)$$

$$NWR_g = NWR \cdot \left(1 + \frac{LNWR}{L_{eff}}\right)$$

$$TCV_g = TCV + \frac{TCVL}{L_{eff}} + \frac{TCVW}{W_{eff}} + \frac{TCVWL}{W_{eff} \cdot L_{eff}}$$

© 2023 Cadence Design Systems, Inc.

Reverse short channel effect (RSCE)

(28-6)

$$\Delta VT_{RSCE} = \frac{2 \cdot QLR_g \cdot \left(1 - \exp\left(-\left(\frac{L_{eff}}{LR_g}\right)^2\right)\right)}{COX \cdot \frac{L_{eff}}{LR_g}}$$

$$GAMMA_{RSCE} = \sqrt{1.0 + \frac{2 \cdot NLR_g \cdot \left(1 - \exp\left(-\left(\frac{L_{eff}}{LR_g}\right)^2\right)\right)}{COX \cdot \frac{L_{eff}}{LR_g}}}$$

$$\Delta\Phi_{f,RSCE} = U_T \cdot FLR \cdot \ln\left(1 + \frac{2 \cdot NLR_g \cdot \left(1 - \exp\left(-\left(\frac{L_{eff}}{LR_g}\right)^2\right)\right)}{COX \cdot \frac{L_{eff}}{LR_g}}\right)$$

Inverse narrow width effect (INWE)

(28-7)

$$\Delta VT_{INWE} = -\frac{2 \cdot QWR_g \cdot \left(1 - \exp\left(-\left(\frac{W_{eff}}{WR_g}\right)^2\right)\right)}{COX \cdot \frac{W_{eff}}{WR_g}}$$

$$GAMMA_{INWE} = \frac{1}{\sqrt{1.0 + \frac{2 \cdot NWR_g \cdot \left(1 - \exp\left(-\left(\frac{W_{eff}}{WR_g}\right)^2\right)\right)}{COX \cdot \frac{W_{eff}}{WR_g}}}}$$

© 2023 Cadence Design Systems, Inc.

Mobility Scaling

(28-8)

$$KP_l = \frac{1}{\left(1+\frac{KA \cdot LA}{L_{eff}}\right)\cdot\left(1-\exp\left(-\frac{L_{eff}}{LA}\right)\right)+\left(1+\frac{KB \cdot LB}{L_{eff}}\right)\cdot\left(1-\exp\left(-\frac{L_{eff}}{LB}\right)\right)}$$

$$KP_w = 1 + WKP2 \cdot \exp\left(-\left(\frac{\ln\left(\frac{W_{eff}}{WKP1}\right)}{WKP3}\right)^2\right)$$

Instance level parameters

(28-9)

$$VTO_g = VTO_a + \Delta VT_L + \Delta VT_W + \Delta VT_{RSCE} + \Delta VT_{NWE}$$

$$GAMMA_g = (GAMMA_a + \Delta GAMMA_L + \Delta GAMMA_W) \cdot GAMMA_{RSCE} \cdot GAMMA_{NWE}$$

$$\Phi_{fg} = PHIF + \Delta\Phi_{f,RSCE}$$

$$KP_g = KP \cdot KP_l \cdot KP_w$$

Temperature scaling

(28-10)

$$\Delta T = T - TNOM$$

$$rT = \frac{T}{TNOM}$$

$$VTO_{gt} = VTO_g - TCV_g \cdot \Delta T$$

$$KP_{gt} = KP_g \cdot rT^{BEX}$$

$$ETA_t = ETA - TETA \cdot \Delta T$$

$$E0_{gt} = E0_g \cdot rT^{TE0EX}$$

$$E1_{gt} = E1_g \cdot rT^{TE1EX}$$

$$\Phi_{f,gt} = \Phi_{f,g} \cdot rT - \frac{E_g(T) - E_g(TNOM) \cdot rT - 3 \cdot U_T \cdot \ln rT}{2}$$

© 2023 Cadence Design Systems, Inc.

Normalizing

(28-11)

$$\phi_f = \frac{\Phi_{fgt}}{U_T}$$
$$vto = \frac{VTO_{gt}}{U_T}$$
$$\gamma = \frac{GAMMA_g}{\sqrt{U_T}}$$
$$\gamma_b = \frac{GAMMAG}{\sqrt{U_T}}$$
$$\gamma_{ov} = \frac{GAMMAOV}{\sqrt{U_T}}$$
$$vfb_{ov} = \frac{VFBOV}{U_T}$$
$$ucrit = \frac{UCRIT}{U_T}$$
$$xb = \frac{XB}{U_T}$$
$$ub = \frac{EB \cdot t_{ox}}{XB}$$

Slope factor nQ0

(28-12)

$$nq0 = \begin{cases} 1 + \frac{\gamma}{2 \cdot \sqrt{2 \cdot \phi_f}}, & \text{if } TG = 0 \text{ or } 1 \\ dfrac11 + \frac{\gamma^2}{\gamma_g^2} \cdot \frac{2 \cdot \sqrt{2 \cdot \phi_f}}{\gamma} + \frac{\gamma}{2 \cdot \sqrt{2 \cdot \phi_f}}, & \text{if } TG = -1 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Quantum mechanic effect

(28-13)

$$\alpha_{qma} = AQMA \cdot \frac{COX^{2/3}}{U_T^{1/3}} \cdot ETAQM^{2/3}$$

$$\delta_{qmi} = \frac{1}{3} \cdot AQMI \cdot \frac{\gamma \cdot COX}{2 \cdot \phi_f \cdot \sqrt{U_T}} \left(\frac{2 \cdot ETAQM \cdot n_{Q0} \cdot \sqrt{2 \cdot \phi_f}}{\gamma} - 1 \right)$$

$$\Delta\Psi_0 = AQMI \cdot \frac{2}{3} \cdot \left(\gamma \cdot COX \cdot \sqrt{2 \cdot \phi_f} \right)^{2/3}$$

$$\Delta\psi_0 = \frac{\Delta\Psi_0}{U_T}$$

$$\phi = 2 \cdot \phi_f + \ln\left(4 \cdot n_{Q0} \cdot \frac{\sqrt{2 \cdot \phi_f}}{\gamma} \right) + \Delta\psi_0$$

Normalization factor for charges

(28-14)

$$Q_0 = -W_{eff,C} \cdot NF \cdot L_{eff,C} \cdot U_T \cdot \frac{COX}{1 + \delta_{qmi}} \frac{W_{eff} - WEDGE}{W_{eff}}$$

$$Q_{0OV} = -W_{eff} \cdot NF \cdot LOV \cdot U_T \cdot \frac{COX}{1 + \delta_{qmi}}$$

Normalization of potentials

(28-15)

$$v_g = \frac{V_{GB}}{U_T}$$

$$v_d = \begin{cases} \frac{V_{DB}}{U_T}, & \text{if } V_D \geq V_S \\ \frac{V_{SB}}{U_T}, & \text{if } V_D < V_S \end{cases}$$

$$v_s = \begin{cases} \frac{V_{SB}}{U_T}, & \text{if } V_D \geq V_S \\ \frac{V_{DB}}{U_T}, & \text{if } V_D < V_S \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Charge sharing effect

(28-16)

$$\mathrm{CHSH_L} = \mathrm{LETA0} + \frac{\mathrm{LETA}}{\mathrm{L_{eff}}} + \frac{\mathrm{LETA2}}{\mathrm{L_{eff}^2}}$$

$$\mathrm{CHSH_W} = \frac{\mathrm{WETA}}{\mathrm{W_{eff}}}$$

$$\mathrm{NUV} = \mathrm{N0} + 3 \cdot \mathrm{NCS} \cdot \mathrm{t_{ox}} \cdot \mathrm{CHSH_L}$$

$$\mathrm{A_1} = 1 \quad \frac{\mathrm{CHSH_L} \cdot \mathrm{t_{si}}}{\gamma} \left(\sqrt{\mathrm{MX_S}\left(\mathrm{v_{Li}} \mid \mathrm{v_s}, 0, \mathrm{U_I^2}\right)} \quad \sqrt{\mathrm{MX_S}\left(\mathrm{v_{Li}} \mid \mathrm{v_d}, 0, \mathrm{U_I^2}\right)} \right)$$

$$\mathrm{A_2} = 2 \cdot \mathrm{A_1} \quad 1 \mid 2 \cdot \mathrm{CHSH_W} \cdot \frac{\sqrt{\phi}}{\gamma}$$

$$\mathrm{A_3} = 1 + \mathrm{CHSH_W} \cdot \mathrm{t_{si}} \cdot \frac{\gamma}{\gamma_g} \cdot \mathrm{A_2}$$

$$\gamma_{\mathrm{chsh}} = \gamma \cdot \frac{\mathrm{A_1}}{1 + \mathrm{CHSH_W}}$$

$$\gamma_{\mathrm{eff}} = \gamma \cdot \frac{\mathrm{A_1}}{\mathrm{A_3}}$$

$$\mathrm{A_{1,0}} = 1 - 2 \cdot \frac{\mathrm{CHSH_L} \cdot \mathrm{t_{si}}}{\gamma} \cdot \sqrt{\mathrm{v_{bi}}}$$

$$\mathrm{A_{2,0}} = 2 \cdot \mathrm{A_{1,0}} - 1 + 2 \cdot \mathrm{CHSH_W} \cdot \frac{\sqrt{\phi}}{\gamma}$$

$$\mathrm{A_{3,0}} = 1 + \mathrm{CHSH_W} \cdot \mathrm{t_{si}} \cdot \frac{\gamma^2}{\gamma_g^2} \cdot \mathrm{A_{2,0}}$$

$$\gamma_{\mathrm{chsh,0}} = \gamma \cdot \frac{\mathrm{A_{1,0}}}{1 + \mathrm{CHSH_W}}$$

Flat-band voltage

(28-17)

$$\mathrm{v_{fb}} - \mathrm{v_{fo}} - \phi \cdot \left(1 + \mathrm{CHSH_W} \cdot \mathrm{t_{si}} + \frac{\gamma^2}{\gamma_g^2} \cdot \left(1 - 2 \cdot \mathrm{CHSH_L} \cdot \mathrm{t_{si}} \cdot \frac{\sqrt{\mathrm{v_{bi}}}}{\gamma} \right)^2 \right) -$$
$$- \gamma \cdot \left(1 - 2 \cdot \mathrm{CHSH_L} \cdot \frac{\sqrt{\mathrm{v_{bi}}}}{\gamma} \cdot \sqrt{\phi} \right)$$

© 2023 Cadence Design Systems, Inc.

Effective gate-voltage

(28-18)

$$v'_g = v_g - v_{fb}$$
$$v'_{g,chsh} = \frac{v'_g}{1 + CHSH_W \cdot t_{si}}$$
$$v'_{g,chsh,pd} = \frac{v'_g}{A_3}$$
$$v'_{g,chsh,pd,0} = \frac{v'_g}{A_{3,0}}$$

Pinch-off surface potential

Approximation around zero

(28-19)

$$\psi_{po} = MX_S\left(v'_{g,chsh} - 6 \cdot \left(1 + \frac{\gamma_{chsh}}{\sqrt{2}}\right), 0.6 \cdot v'_{g,chsh}\right)$$
$$\psi_{po,0} = MX_S\left(v'_{g,chsh} - 6 \cdot \left(1 + \frac{\gamma_{chsh,0}}{\sqrt{2}}\right), 0.6 \cdot v'_{g,chsh}\right)$$

Exact solution

(28-20)

$$\psi_p = \begin{cases} -\ln\left(1 - \psi_{po} + \left(\frac{\psi_{po} - v'_{g,chsh}}{\gamma_{chsh}}\right)^2\right), & \text{if } v'_g < 0 \\ \left(\sqrt{v_{g,chsh,pd} - 1 + \exp(-\psi_{po}) + \frac{\gamma_{eff}^2}{4}} - \frac{\gamma_{eff}}{2}\right)^2 + 1 - \exp(-\psi_{po}), & \text{if } v'_g \geq 0 \end{cases} \quad (2.90)$$

$$\psi_{p0} = \begin{cases} -\ln\left(1 - \psi_{po,0} + \left(\frac{\psi_{po,0} - v'_{g,chsh}}{\gamma_{chsh,0}}\right)^2\right), & \text{if } v'_g < 0 \\ \left(\sqrt{v_{g,chsh,pd,0} - 1 + \exp(-\psi_{po,0}) + \frac{\gamma_{chsh,0}^2}{4}} - \frac{\gamma_{chsh,0}}{2}\right)^2 + 1 - \exp(-\psi_{po,0}), & \text{if } v'_g \geq 0 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Pinch-off voltage

(28-21)

$$v_p = \psi_p - \phi$$

Velocity saturation

(28-22)

$$e_{clm} = \frac{2}{u_{crit} \cdot L_{eff}}$$

$$q_{sat} = \frac{2 \cdot e_{clm} \cdot i_f}{e_{clm} + 2 + 2 \cdot e_{clm} \cdot q_s + \sqrt{(e_{clm}+2)^2 + 8 \cdot e_{clm} \cdot q_s}}$$

$$v_{d,sat} = v_p - \frac{(2 \cdot q_{sat} + \ln q_{sat})(1 + e_{clm} \cdot (q_s - q_{sat}))}{\sqrt{1 + \frac{2 \cdot (e_{clm} \cdot (2 - \mathbf{DELTA}) \cdot (q_s - q_{sat}))^2}{0.1 + e_{clm} \cdot (2 - \mathbf{DELTA}) \cdot (q_s - q_{sat})}} + e_{clm} \cdot (q_s - q_{sat})}$$

$$v_{ds,sat} = MX_S(v_{d,sat} - v_s, 3, 4)$$

$$dv = \frac{\mathbf{ACLM}}{\mathbf{DELTA}} \cdot \frac{4 \cdot q_{sat} + \mathbf{DELTA}}{q_s + 1}$$

$$v'_d = \frac{1}{2} \cdot \sqrt{\left((v_d - v_s) \cdot \sqrt{1 + \frac{4 \cdot dv}{v_{ds,sat}}} + v_{ds,sat}\right)^2 + 4 \cdot dv \cdot v_{ds,sat}} - \frac{1}{2} \cdot \sqrt{\left((v_d - v_s) \cdot \sqrt{1 + \frac{4 \cdot dv}{v_{ds,sat}}} - v_{ds,sat}\right)^2 + 4 \cdot dv \cdot v_{ds,sat}} + v_s$$

© 2023 Cadence Design Systems, Inc.

Channel length modulation

(28-23)

$$u_{clm} = \frac{e_{clm} \cdot L_{eff}}{L_C \cdot (v_d - v'_d)}$$

$$\alpha_{clm} = \frac{L_C}{L_{eff} - 2 \cdot L_C}$$

$$\delta L = LAMBDA_{g,t} \cdot L_C \cdot \ln \frac{\alpha_{clm} + u_{clm} + \sqrt{u_{clm}^2 + 2 \cdot \alpha_{clm} \cdot u_{clm} + 1}}{\alpha_{clm} + 1}$$

Normalized drain inversion charge

(28-24)

$$q_d = q(v_p + \delta\psi_s - v'_d)$$

Normalized forward current

(28-25)

$$i_f = q_d + q_d^2$$

Slope factor n_v

(28-26)

$$n_v = A_3 + \gamma \cdot \frac{A_1}{2 \cdot \sqrt{\psi_p}}$$

© 2023 Cadence Design Systems, Inc.

Drain induced barrier lowering effect

(28-27)

$$l_0 = \mathrm{ETA_g} \cdot t_{si} \cdot \sqrt{\frac{2 \cdot \sqrt{\phi}}{\gamma}}$$

$$v_c = 4 + 40 \cdot \frac{l_0}{L_{eff}}$$

$$dv = \mathrm{MNS}(v_p, \mathrm{MNS}(v_s, v_d, v_o^2), v_o^2)$$

$$\delta\psi_s = \exp\left(-\frac{L_{eff}}{2 \cdot l_0}\right) \cdot \left(2 + \mathrm{SIGMAD} \cdot \frac{L_{eff}}{2 \cdot l_0} \cdot \frac{dv}{2 \cdot \phi}\right) \cdot \sqrt{(nul - v_s - dv) \cdot (nul + v_d - dv)} \quad (2.97)$$

Normalized source inversion charge

(28-28)

$$q(v) = \begin{cases} \text{if } \dfrac{v}{NUV} < -0.8 \\ \quad z_1 = \dfrac{1}{4} \cdot \left(\dfrac{v}{NUV} - 1.4 + \sqrt{\dfrac{v}{NUV} \cdot \left(\dfrac{v}{NUV} - 0.384936\right) + 9.662671}\right) \\ \quad z_2 = \dfrac{\dfrac{v}{NUV} - (2 \cdot z_1 + \ln z_1)}{2 \cdot z_1 + 1} \\ \quad z_1 (1 + z_2 \cdot (1 + 0.07 \cdot z_2)) \cdot NUV \\ \text{if } \dfrac{v}{NUV} \geq -0.8 \\ \quad z_{1,lu} - 0.5 \cdot \left(\dfrac{v}{NUV} - 0.201491 - \sqrt{\dfrac{v}{NUV} \cdot \left(\dfrac{v}{NUV} - 0.402982\right) + 2.446562}\right) \\ \quad z_1 = \dfrac{1}{4} \cdot \left(\dfrac{v}{NUV} - 1.4 + \sqrt{\dfrac{v}{NUV} \cdot \left(\dfrac{v}{NUV} - 0.384936\right) + 9.662671}\right) \\ \quad z_2 = \dfrac{\dfrac{v}{NUV} - (2 \cdot \exp(z_{1,lu}) + z_{1,lu})}{2z_1 + 1} \\ \quad z_1 (1 + z_2 \cdot (1 + 0.483 \cdot z_2)) \cdot NUV \end{cases}$$

$$q_s = q(v_p - \delta\psi_s - v_s)$$

Normalized forward current

(28-29)

$$i_f = q_s + q_s^2$$

© 2023 Cadence Design Systems, Inc.

Slope factor n_Q

(28-30)

$$\psi_{sa} = \psi_p \quad q_s \quad q_d \tag{2.112}$$

$$n_Q = \begin{cases} \text{if TG} < 0 \\ \dfrac{1 + \dfrac{\gamma^2}{\gamma_g^2} + \dfrac{\text{GAMMA}}{\sqrt{U_T}(\sqrt{\psi_p} + \sqrt{\psi_{sa}})}}{\dfrac{1}{2} + \dfrac{\gamma^2}{\gamma_g^2}\dfrac{\sqrt{U_T}\sqrt{\psi_{ss}}}{\text{GAMMA}} + \sqrt{\left(\dfrac{1}{2} + \dfrac{\gamma^2}{\gamma_g^2}\dfrac{\sqrt{U_T}\sqrt{\psi_{ss}}}{\text{GAMMA}}\right)^2 + \left(1 + \dfrac{\gamma^2}{\gamma_g^2} + \dfrac{\text{GAMMA}}{\sqrt{U_T}(\sqrt{\psi_p} + \sqrt{\psi_{sa}})}\right)\dfrac{q_s + q_d}{\gamma_g^2}}} \\ \text{if TG} \geq 0 \\ 1 + \dfrac{\text{GAMMA}}{\sqrt{U_T} \cdot (\sqrt{\psi_p} + \sqrt{\psi_{sa}})} \end{cases}$$

Charge model

(28-31)

$$v_o = v'_{g,chsh} - \psi_{p,0}$$

Quantum mechanic effect

(28-32)

$$q_{bo} = v'_{g,chsh} - \psi_{po}, \quad \text{if } v'_g < 0$$

$$q_{bo} = \frac{v'_{g,chsh}}{1 + \dfrac{\gamma^2}{\gamma_g^2}} \quad \psi_{po}, \quad \text{if } v'_g < 0$$

$$\delta\psi_v = \alpha_{qma} \cdot \left(\left(\sqrt{\frac{q_{bo}^2}{4} + 4 \cdot \alpha_{qma} \cdot \gamma'_{chsh}} - \frac{q_{bo}}{2} \right)^{2/3} - \left(\sqrt{\frac{9 \cdot \gamma'^2_{chsh}}{2} + 4 \cdot \alpha_{qma} \cdot \gamma'^2_{chsh}} - \frac{3 \cdot \gamma_{chsh}}{\sqrt{2}} \right)^{2/3} \right)$$

$$v_{o,qm} = v_o + \delta\psi_v$$

© 2023 Cadence Design Systems, Inc.

Q_S, Q_D, Q_G, Q_B

(28-33)

$$q_S = \frac{n_Q}{3\cdot(1+\delta q_{mi})}\cdot\left(2\cdot q_s + q_d + \frac{(1+\frac{4}{5}\cdot q_s+\frac{6}{5}\cdot q_d)\cdot(q_s-q_c)^2}{2\cdot(q_s+q_d+1)^2}\right)$$

$$q_D = \frac{n_Q}{3\cdot(1+\delta q_{mi})}\cdot\left(q_s - 2\cdot q_d + \frac{(1+\frac{6}{5}\cdot q_s+\frac{4}{5}\cdot q_d)\cdot(q_s-q_d)^2}{2\cdot(q_s+q_d+1)^2}\right)$$

$$q_G = \begin{cases} \text{if } TG < 0 \\ \quad \dfrac{v_{o,qm}+\frac{2\cdot q_s}{1+\delta_{qmi}}}{1+2\cdot\sqrt{\frac{1}{4}+\frac{v_{o,qm}+\frac{2\cdot q_s}{1+\delta_{cmi}}}{\gamma_g^2}}} + \dfrac{v_{o,qm}+\frac{2\cdot q_d}{1+\delta_{qmi}}}{1+2\cdot\sqrt{\frac{1}{4}+\frac{v_{o,qm}-\frac{2\cdot q_d}{1+\delta_{qmi}}}{\gamma_g^2}}} + \\ \quad -\dfrac{1}{3\cdot(1+\delta_{qmi})}\cdot\dfrac{(q_s-q_d)^2}{\left(\sqrt{\frac{1}{4}+\frac{v_{o,qm}+\frac{2\cdot q_s}{1+\delta_{qmi}}}{\gamma_g^2}}+\sqrt{\frac{1}{4}+\frac{v_{o,qm}+\frac{2\cdot q_d}{1+\delta_{qmi}}}{\gamma_g^2}}\right)^3} \\ \quad \cdot\frac{4}{5}\cdot\left(\sqrt{\frac{1}{4}+\frac{v_{o,qm}+\frac{2\cdot q_s}{1+\delta_{qmi}}}{\gamma_g^2}}+\sqrt{\frac{1}{4}+\frac{v_{o,qm}+\frac{2\cdot q_d}{1+\delta_{cmi}}}{\gamma_g^2}}\right)^2 + \\ \quad -\frac{4}{5}\cdot\sqrt{\frac{1}{4}+\frac{v_{o,qm}+\frac{2\cdot q_s}{1+\delta_{qmi}}}{\gamma_g^2}}\cdot\sqrt{\frac{1}{4}+\frac{v_{o,qm}+\frac{2\cdot q_d}{1+\delta_{qmi}}}{\gamma_g^2}}+\frac{2}{\gamma_g^2} \\ \text{if } TG \geq 0 \\ \quad v_{o,qm}+q_s+q_s+\dfrac{1}{3\cdot(1+\delta_{qmi})}\cdot\dfrac{(q_s-q_d)^2}{q_s+q_d+1} \end{cases}$$

$$q_I = q_S + q_D$$

$$q_B = q_G - q_S - q_D$$

© 2023 Cadence Design Systems, Inc.

Mobility effects

Coulomb scattering

(28-34)

$$\beta_{coul} = \frac{THC}{(1 + n_v \cdot ZC \cdot q_s) \cdot (1 + n_v \cdot ZC \cdot q_d)}$$

Vertical field effect

(28-35)

$$e_{q0} = q_B + ETA_t \cdot n_v \cdot q_I$$

$$e_{q1} = \left(\gamma_{eff} \cdot \sqrt{\psi_p} + n_v \cdot (1 - ETA_t) - 1\right)^2 + (n_v \cdot (1 - ETA_t) - 1)^2 \cdot (1 + 2 \cdot i_f + 2 \cdot i_r) - \\ -\frac{8}{3} \cdot (n_v \cdot (1 - ETA_t) - 1) \cdot (\gamma_{eff} \cdot \sqrt{\psi_p} + n_v \cdot (1 - ETA_t) - 1) \cdot \\ \cdot \frac{i_f + i_r + 0.5 + \sqrt{(i_f + 0.25) \cdot (i_r + 0.25)}}{\sqrt{i_f + 0.25} + \sqrt{i_r + 0.25}}$$

$$\beta_{rvf,coul} = \frac{1 + \frac{U_T}{E0_{g,t} \cdot t_{si}} \cdot \gamma_{eff} \cdot \sqrt{\phi} + \left(\frac{U_T}{E1_{g,t} \cdot t_{si}} \cdot \gamma_{eff} \cdot \sqrt{\phi}\right)^2}{1 + \frac{U_T}{E0_{g,t} \cdot t_{si}} \cdot e_{q0} + \left(\frac{U_T}{E1_{g,t} \cdot t_{si}}\right)^2 \cdot e_{q1} + \beta_{coul}}$$

Channel length modulation

(28-36)

$$\beta_{clm} = \left(\sqrt{1 + \frac{2 \cdot (e_{clm} \cdot (2 - DELTA) \cdot (q_s - q_H))^2}{0.1 + e_{clm} \cdot (2 - DELTA) \cdot (q_s - q_d)} + (e_{clm} \cdot (q_s - q_d))^2}\right)^{-1}$$

Overall effect

(28-37)

$$\beta = KP_{g,t} \cdot \beta_{rvf,coul} \cdot \beta_{clm}$$

© 2023 Cadence Design Systems, Inc.

Specific current

(28-38)

$$I_{SPEC} = \frac{2 \cdot n_Q \cdot U_T^2 \cdot \beta}{1 + \delta_{qmi}} \cdot \frac{(W_{eff} - WEDGE) \cdot NF}{L_{eff} - \delta L}$$

Drain induced threshold shift

(28-39)

$$v_{a_{dits}} = \frac{\frac{1}{1 + FPROUT \cdot \frac{T_{eff}}{q_I + 2}}}{PDITS} \cdot (1 + (1 + PDITSL \cdot L_{eff}) \cdot \exp(PDITSD \cdot (v_d - v_s) \cdot U_T))$$

$$v_{ds,dits} = v_{ds,sat} - MXs(v_{ds,sat} - (v_d - v_s) - DDITS, 0.4 \cdot DDITS \cdot v_{ds,sat})$$

$$f_{dits} = 1 + \frac{v_d - v_s - v_{ds,dits}}{v_{a_{dits}}}$$

Denormalizing

(28-40)

$$Q_S = q_S \cdot Q_0$$

$$Q_D = q_D \cdot Q_0$$

$$Q_G = -q_G \cdot Q_0$$

$$Q_B = q_B \cdot Q_0$$

$$I_{ds} = I_{SPEC} \cdot (i_f - i_r) \cdot f_{dits}$$

© 2023 Cadence Design Systems, Inc.

Edge Conductance

Normalization Factors (Edge Device)

(28-41)

$$I_{SPEC,edge} = \frac{2 \cdot n_Q \cdot U_T^2 \cdot \beta}{1+\delta_{qmi}} \frac{W_{eff} \cdot NF}{L_{eff} - \ell L} \cdot \frac{W_{eff} - WEDGE}{W_{eff}}$$

$$Q_{0,edge} = -W_{eff,C} \cdot NF \cdot L_{eff,C} \cdot U_T \cdot \frac{COX}{1+\delta_{qmi}} \cdot \frac{WEDGE}{W_{eff}}$$

Scaling - Normalizing

(28-42)

$$\delta\gamma_{edge} = \frac{DGAMMAEDGE}{\sqrt{U_T}} \cdot \left(1.0 + \frac{WLDGAMMAEDGE}{W_{eff} \cdot L_{eff}}\right)$$

$$\delta\phi_{edge} = \frac{DPHIEDGE}{U_T} \cdot \left(1.0 + \frac{LDPHIEDGE}{L_{eff}}\right) \cdot \left(1.0 + \frac{WDPHIEDGE}{W_{eff}}\right) \cdot \left(1.0 + \frac{WLDPHIEDGE}{W_{eff} \cdot L_{eff}}\right)$$

$$\delta v_{p,edge} = -\delta\gamma_{edge} \cdot \frac{\psi_p}{\sqrt{\psi_p} + \frac{\gamma}{2}} - \delta\phi_{edge}$$

Normalized Inversion Charges (Edge Device)

(43)

$$q_{s,edge} = q\left(v_p + \delta v_{p,edge} + \delta\psi_s - v_s\right)$$

$$q_{d,edge} = q\left(v_p + \delta v_{p,edge} + \delta\psi_s - v'_d\right)$$

© 2023 Cadence Design Systems, Inc.

Normalized Currents (Edge Device)

(28-44)

$$i_{f,edge} = q_{s,edge}^2 + q_{s,edge}$$
$$i_{r,edge} = q_{d,edge}^2 + q_{d,edge}$$

Drain Current (Edge Device)

(28-45)

$$I_{DS,edge} = I_{SPEC,edge} \cdot (i_{f,edge} - i_{r,edge}) \cdot f_{dits}$$

Edge Device: Charge Model

(28-46)

$$\psi_{p,edge} = \psi_p - \delta\gamma_{edge} \cdot \frac{\psi_p}{\sqrt{\psi_p} + \frac{\gamma}{2}}$$

$$\gamma_{edge} = \gamma + \delta\gamma_{edge}$$

$n_{q,edge}$

$Q_{S,edge}, Q_{Dedge}, Q_{G,edge}, Q_{B,edge}$

© 2023 Cadence Design Systems, Inc.

Overlap Capacitances

(28-47)

$$v'_{gs,ov} = v_g - VOV \cdot v_s - vfb_{ov}$$

if $TG < 0$

$$\gamma_{dep,sov} = \begin{cases} \gamma_{g,ov} & \text{if } v'_{gs,ov} \geq 0 \\ \gamma_{ov} & \text{if } v'_{gs,ov} < 0 \end{cases}$$

$$\gamma_{acc,sov} = \begin{cases} \gamma_{ov} & \text{if } v'_{gs,ov} \geq 0 \\ \gamma_{g,ov} & \text{if } v'_{gs,ov} < 0 \end{cases}$$

$$v_{0,sov} = \begin{cases} v'_{gs,ov} & \text{if } v'_{gs,ov} \geq 0 \\ -v'_{gs,ov} & \text{if } v'_{gs,ov} < 0 \end{cases}$$

$$a_{0,sov} = 1.0 + \frac{\gamma_{acc,sov}}{\sqrt{2}}$$

$$a_{1,sov} = \frac{\gamma_{dep,sov}}{\gamma_{acc,sov}}$$

$$a_{2,sov} = \frac{a_{0,sov}}{a_{0,sov} + a_{1,sov}}$$

$$a_{3,sov} = 1 + \frac{\gamma_{dep,sov}}{\sqrt{2}} + a_{1,sov}$$

$$v_{1,sov} = \frac{v_{0,sov}}{2} - 3 \cdot a_{2,sov} \cdot a_{3,sov}$$

$$\delta\psi_{gs0} = v_{1,sov} + \sqrt{v_{1,sov}^2 + 6 \cdot a_{0,sov} \cdot a_{3,sov}}$$

$$\gamma_{dep2,sov} = \gamma_{dep,sov} \cdot \left(\frac{1}{2} + \frac{3}{3 \cdot \sqrt{2} \cdot \gamma_{acc,sov} + v_{0,sov} - \delta\psi_{gs0}} \right)$$

$$a_{4,sov} = 1 - \exp\left(-\delta\psi_{gs0}\right)$$

$$v_{2,sov} = v_{0,sov} - a_{4,sov}$$

© 2023 Cadence Design Systems, Inc.

(28-48)

$$\delta\psi_{gs} = \left(\frac{v_{2,sov}}{\gamma_{dep2,sov} + \sqrt{\gamma_{dep2,sov}^2 + v_{2,sov}}} \right)^2 - a_{4,sov}$$

$$v_{2b,sov} = v_{0,sov} - \delta\psi_{gs}$$

$$v_{3,sov} = \frac{v_{2b,sov}}{2}$$

$$\delta\psi_{ox,s} = \begin{cases} v_{3,sov} - 3 \cdot a_{0,sov} + \sqrt{\left(\frac{v_{3,sov}}{3 \cdot a_{0,sov}}\right)^2 - 6 \cdot v_{2b,sov}} & \text{if } v'_{gs,ov} > 0 \\ \left(v_{3,sov} \quad 3 \cdot a_{0,sov} + \sqrt{\left(\frac{v_{3,sov}}{3 \cdot a_{0,sov}}\right)^2 \quad 6 \cdot v_{2b,sov}}\right) & \text{if } v'_{gs,ov} < 0 \end{cases}$$

if $\mathbf{TG} \geq 0$

if $v'_{gs,ov} \geq 0$

$$\gamma_{acc,sov} = \gamma_{ov}$$

$$v_{0,sov} = v_{gs,ov}$$

$$a_{0,sov} = 1 + \frac{\gamma_{acc,sov}}{\sqrt{2}}$$

$$v_{1,sov} = \frac{v_{c,sov}}{2} - 3 \cdot a_{0,sov}^2$$

$$\delta\psi_{gs0} = v_{1,sov} + \sqrt{v_{1,sov}^2}$$

$$\delta\psi_{gs} - 1 - \exp\left(-\delta\psi_{gs0}\right)$$

$$v_{2b,sov} = v_{0,sov} - \delta\psi_{gs}$$

$$v_{3,sov} = \frac{v_{2b,sov}}{2}$$

$$\delta\psi_{ox,s} = v_{3,sov} - 2 \cdot a_{0,sov} + \sqrt{(v_{3,sov} + 3 \cdot a_{0,sov})^2 - 6 \cdot v_{2b,sov}}$$

© 2023 Cadence Design Systems, Inc.

(28-49)

$$\text{if } v'_{gs,ov} < 0$$

$$\gamma_{dep,sov} = \gamma_{ov}$$

$$v_{0,sov} = -v_{gs,ov}$$

$$a_{3,sov} = 1 + \frac{\gamma_{dep,sov}}{\sqrt{2}}$$

$$v_{1,sov} = \frac{v_{0,sov}}{2} - 3 \cdot a_{3,sov}^2$$

$$\delta\psi_{gs0} = v_{1,sov} + \sqrt{v_{1,sov}^2 + 6 \cdot v_{0,sov}}$$

$$\gamma_{dep2,sov} = \gamma_{dep,sov} 2$$

$$a_{4,sov} = 1 - \exp\left(-\delta\psi_{gs0}\right)$$

$$v_{2,sov} = v_{0,sov} - a_{4,sov}$$

$$\delta\psi_{gs} = \left(\frac{v_{2,sov}}{\gamma_{dep2,sov} + \sqrt{\gamma_{dep2,sov}^2 + v_{2,sov}}} \right)^2 + a_{4,sov}$$

$$v_{2b,sov} = v_{0,sov} \quad \delta\psi_{gs}$$

$$\delta\psi_{ox,s} = -v_{2b,sov}$$

Denormalizing (Overlap)

(28-50)

$$Q_{G,OV} = -Q_{0,OV} \cdot \delta\psi_{ox,s}$$

$$Q_{D,OV} = -Q_{0,OV} \cdot \delta\psi_{ox,d}$$

© 2023 Cadence Design Systems, Inc.

Fringing Capacitance

(28-51)

$$Q_{S,FR} = W_{eff,c} \cdot \mathbf{NF} \cdot \mathbf{KJF}(1 + \mathbf{CJF} \cdot U_T \cdot v_s) \cdot \sqrt{MX_S\left(v_{bi} + \frac{\mathbf{VFR}}{U_T} + v_s - (\psi_P - 2 \cdot q_s), 0, \mathbf{DFR}\right)} \tag{2.192}$$

$$Q_{D,FR} = W_{eff,c} \cdot \mathbf{NF} \cdot \mathbf{KJF}\left(1 + \mathbf{CJF} \cdot U_T \cdot v'_d\right) \cdot \sqrt{MX_S\left(v_{bi} + \frac{\mathbf{VFR}}{U_T} + v'_d - (\psi_P - 2 \cdot q'_d), 0, \mathbf{DFR}\right)}$$

Bias-Independent Overlap Capacitances

(28-52)

$$C_{GSO} = \mathbf{CGSO} \cdot W_{eff}$$

$$C_{GDO} = \mathbf{CGDO} \cdot W_{eff}$$

$$C_{GBO} = \mathbf{CGBO} \cdot 2 \cdot L_{eff}$$

Gate Induced Drain and Source Current

(28-53)

$$v_{gs,e} = v_{fb} + \psi_P - 2 \cdot q_s$$

$$I_{GIDL} = \mathbf{AGIDL} \cdot W_{eff} \cdot \mathbf{NF}^{\frac{(v'_d - v_s - v_{gs,e}) \cdot U_T - \mathbf{EGIDL}}{3 \cdot T_{OX}}} \cdot \exp\left(-\frac{3 \cdot T_{OX} \cdot \mathbf{BGIDL}}{(v'_d - v_s - v_{gs,e}) \cdot U_T - \mathbf{EGIDL}}\right) \cdot \frac{(v_d \cdot U_T)^3}{\mathbf{CGIDL} + (v_d \cdot U_T)^3}$$

$$v_{gd,e} = v_{fb} + \psi_P - 2 \cdot q'_d$$

$$I_{CISL} = \mathbf{AGIDL} \cdot W_{eff} \cdot \mathbf{NF}^{\frac{(v_d - v'_d - v_{gd,e}) \cdot U_T - \mathbf{EGIDL}}{3 \cdot T_{OX}}} \cdot \exp\left(-\frac{3 \cdot T_{OX} \cdot \mathbf{BGIDL}}{(v_s \quad v'_d \quad v_{gd,e}) \cdot U_T \quad \mathbf{EGIDL}}\right) \cdot \frac{(v_s \cdot U_T)^3}{\mathbf{CGIDL} \; + \; (v_s \cdot U_T)^3}$$

© 2023 Cadence Design Systems, Inc.

Gate Current

(28-54)

$$\text{if } ((\psi_p \geq 0) \text{ and } (\mathbf{TG} < 0)) \text{ or } ((\psi_p < 0) \text{ and } (\mathbf{TG} \geq 0))$$

$$v_1 = \sqrt{\frac{1}{4} + \frac{v_o + 2 \cdot q_s}{\gamma_g^2}}$$

$$v_2 = v_1 + \frac{1}{2}$$

$$\psi_{ox} = \frac{v_o + 2 \cdot q_s}{v_2}$$

$$\delta\psi_{dq} = \frac{2}{v_2} \cdot \left(1 - \frac{v_o + 2 \cdot q_s}{2 \cdot v_1 \cdot v_2 \gamma_g^2}\right)$$

$$\text{if } ((\psi_p \leq 0) \text{ and } (\mathbf{TG} \leq 0)) \text{ or } ((\psi_p > 0) \text{ and } (\mathbf{TG} > 0))$$

$$\psi_{ox} = \frac{v_o + 2 \cdot q_s}{v_2}$$

$$\delta\psi_{dq} = 2$$

$$\psi_x = \frac{\psi_{ox}}{x_b}$$

$$p_{tun} = \begin{cases} \exp\left(-y_i \left(\frac{1}{1+\sqrt{1-\psi_x}} + \sqrt{1-\psi_r}\right)\right) & \text{if } \psi_x < 1 \\ \exp\left(-\frac{u_b}{\psi_x}\right) & \text{if } \psi_x > 1 \end{cases}$$

$$i_{go} = q_s \cdot \psi_{ox} \cdot p_{tun}$$

(28-55)

© 2023 Cadence Design Systems, Inc.

if $(v_s = v_d)$ or $(\psi_{ox} = 0)$

$$n_{gc} = i_{go} \cdot n_Q$$

$$n_{gs} = \frac{n_{igc}}{2}$$

$$n_{gd} = n_{igs}$$

if $(v_s \neq v_d)$ and $(\psi_{ox} \neq 0)$

$$\delta q_{\delta\xi} = \frac{i_r' - i_f}{1 + 2 \cdot q_s}$$

$$a_{gc} = \delta q_{\delta\xi} \cdot \left(\frac{1}{q_s} + \frac{\delta\psi_{dq}}{\psi_{ox}} \right)$$

if $\psi_x < 1$

$$b_{gc} = \begin{cases} \delta q_{\delta\xi} \cdot \delta\psi_{dq} \cdot \dfrac{u_b}{x_b} \cdot \dfrac{3 + \psi_x}{4 + 2\sqrt{1 - \psi_x} \cdot (2 + \psi_x)} & \text{if } \psi_{ox} > 0 \\ -\delta q_{\delta\xi} \cdot \delta\psi_{dq} \cdot \dfrac{u_b}{x_b} \cdot \dfrac{3 + \psi_x}{4 + 2\sqrt{1 - \psi_x} \cdot (2 + \psi_x)} & \text{if } \psi_{ox} < 0 \end{cases}$$

if $\psi_x \geq 1$

$$b_{gc} = \delta q_{\delta\xi} \cdot \delta\psi_{dq} \cdot \frac{u_b}{\psi_x + \psi_{ox}}$$

$$n_{gc} = i_{go} \cdot n_Q \cdot \frac{2 + a_{gc}}{2 - b_{gc}}$$

$$n_{gs} = \frac{1}{2} \cdot i_{go} \cdot n_Q \cdot \frac{3 + a_{gc}}{3 - b_{gc}}$$

$$n_{gd} = n_{igc} - n_{igs}$$

(28-56)

© 2023 Cadence Design Systems, Inc.

if $v_g \geq v_{fb}$

$$I_{GB} = 0$$

$$I_G - 2 \cdot \mathbf{KG} \cdot W_{eff} \cdot \mathbf{NF} \cdot L_{eff} \cdot U_T^2 \cdot n_{igv} \cdot p_{tun} \cdot T_{OX}^{-2}$$

$$I_{GD} = 2 \cdot \mathbf{KG} \cdot W_{eff} \cdot \mathbf{NF} \cdot L_{eff} \cdot U_T^2 \cdot n_{igd} \cdot p_{tun} \cdot T_{OX}^{-2}$$

$$I_{GS} = I_G - I_{GD}$$

if $v_g < v_{fb}$

$$I_{GB} = \mathbf{KG} \cdot W_{eff} \cdot \mathbf{NF} \cdot L_{eff} \cdot U_T^2 \cdot \psi_{ox} \cdot |\psi_{ox}| \cdot p_{tun} \cdot T_{OX}^{-2}$$

$$I_G = 0$$

$$I_{GD} = 0$$

$$I_{GS} = 0$$

Overlap Gate Current

Gate - Source (Overlap Current)

(28-57)

$$\psi_{oxr,sov} = \begin{cases} v_g - v_s - \left(\sqrt{v_g - v_s - v_{fb,ov} + \frac{\gamma_g^2}{4}} - \frac{\gamma_g}{2} \right)^2 & \text{if } v_g - v_s > v_{fb,ov} \\ v_g - v_s + \left(\sqrt{-v_g + v_s + v_{fb,ov} + \frac{\gamma_{ov}^2}{4}} - \frac{\gamma_{ov}}{2} \right)^2 & \text{if } v_g - v_s < v_{fb,ov} \end{cases}$$

$$\psi_{xr,sov} = \frac{|\psi_{oxr,sov}|}{x_b}$$

$$p_{tun,sov} = \begin{cases} \exp\left(-y_b \left(\frac{1}{1 + \sqrt{1 - \psi_{xr,sov}}} + \sqrt{1 - \psi_{xr,sov}} \right) \right) & \text{if } \psi_{xr,sov} < 1 \\ \exp\left(-\frac{y_b}{\psi_{xr,sov}} \right) & \text{if } \psi_{xr,sov} > 1 \end{cases}$$

$$I_{GSOV} = \mathbf{KG} \cdot W_{eff} \cdot \mathbf{NF} \cdot \mathbf{LOVIG} \cdot \psi_{oxr,sov} \cdot |\psi_{oxr,sov}| \cdot U_T^2 \cdot p_{tun} \cdot T_{OX}^{-2}$$

© 2023 Cadence Design Systems, Inc.

Gate - Drain (Overlap Current)

Equations similar to Gate - Source (Overlap Current)

Impact Ionization Current

(28-58)

$$\mathrm{v_{ib}} = \mathrm{v_d} - \mathrm{v_s} - 2 \cdot \mathbf{IBN} \cdot \mathrm{v_{dsatt}}$$

$$\mathrm{I_{DB}} = \begin{cases} I_{DS} \cdot v_{ib} \cdot U_T \cdot \exp\left(\dfrac{IBB_t \cdot L_C}{v_{ib} \cdot U_T}\right) \cdot \dfrac{\mathbf{IBA}}{IBB_t} & \text{if } v_{ib} > 0 \\ 0 & \text{if } v_{ib} < 0 \end{cases}$$

Noise

Thermal Noise

(28-59)

$$\mathrm{g_n} = \frac{2}{(1 + \mathrm{e_{clm}} \cdot (\mathrm{q_s} - \mathrm{q'_d}))^2 \cdot (\mathrm{q_s} + \mathrm{q'_d} + 1)} \cdot \frac{1}{3} \cdot (\mathrm{q_s^2} + \mathrm{q_s} + \mathrm{q'^2_d} + \mathrm{q'_d}) + \mathrm{e_{clm}^2} \cdot \frac{(\mathrm{i_f} - \mathrm{i'_r})^2}{4} + \\ + \frac{(\mathrm{e_{clm}} \cdot (\mathrm{i_f} - \mathrm{i'_r}) + 1) \cdot (\mathrm{q_s} + \mathrm{q'_d})}{4} + \\ + \frac{\mathrm{e_{clm}} \cdot (\mathrm{i_f} - \mathrm{i'_r}) - 1}{8} \cdot \mathrm{e_{clm}^2} \cdot (\mathrm{i_f} - \mathrm{i'_r}) \cdot (\mathrm{q_s} + \mathrm{q'_d} + 1) \cdot \ln \frac{\mathrm{q_s} + \frac{1}{2} + \frac{\mathrm{e_{clm}} \cdot (\mathrm{i_f} - \mathrm{i'_r})}{2}}{\mathrm{q'_d} + \frac{1}{2} + \frac{\mathrm{e_{clm}} \cdot (\mathrm{i_f} - \mathrm{i'_r})}{2}}$$

$$\mathrm{thermal} = 4 \cdot \mathrm{K} \cdot \mathrm{T} \frac{\mathrm{I_{SPEC}}}{\mathrm{U_T}} \cdot \mathrm{g_n} \cdot \mathbf{TH_NOI}$$

© 2023 Cadence Design Systems, Inc.

Flicker Noise

(28-60)

$$g_{ng} = \frac{I_{SPEC}}{U_T} \cdot \frac{q_s - q_d'}{n_v}$$

$$\text{flicker} - \frac{\mathbf{KF} \cdot g_{ng}^{\mathbf{EF}} \cdot (\delta q_{mi} + 1)}{W_{eff} \cdot \mathbf{NF} \cdot L_{eff} \cdot \mathbf{COX}}$$

$$s_{id,flicker}(f) = \frac{\text{flicker}}{f^{AF}}$$

Induced Gate Noise

(28-61)

$$\omega_{spec} - \frac{\beta \cdot U_T}{\mathbf{COX} \cdot L_{eff}^2}$$

$$x_f = q_s + \frac{1}{2}$$

$$x_r = q_d' + \frac{1}{2}$$

$$s_{n,idid} = \frac{4 \cdot x_f^2 - 3 \cdot x_f + 4 \cdot x_f \cdot x_r - 3 \cdot x_r + 4 \cdot x_r^2}{6 \cdot (x_f + x_r)}$$

$$s_{n,igig} = \frac{\omega^2 \;\; 16x_f^4 + 16x_r^4 + 80x_f x_r^3 + 80x_f^3 x_r + 168x_f^2 x_r^2 - 15x_r^3 - 15x_f^3 - 75x_f^2 x_r - 75x_r^2 x_f}{\omega_{spec}^2 \qquad 540 n_{q0}^3 (x_f + x_r)^5}$$

$$s_{n,ibib} = \frac{s_{n,igig}}{(n_{q0} - 1)^2}$$

$$s_{n,igid} = \frac{J \cdot \frac{\omega}{\omega_{spec}}}{18 \cdot n_{q0}} \cdot \frac{(x_f - x_r) \cdot (x_f^2 + 4 \cdot x_f \cdot x_r + x_r^2)}{(x_f + x_r)^3}$$

$$c_{igid} = J \frac{s_{n,igid}}{\sqrt{s_{n,idd} \cdot s_{n,igig}}}$$

© 2023 Cadence Design Systems, Inc.

Shot and Flicker Gate Noise

(28-62)

$$s_{ig,shot} = 2 \cdot q_e \cdot I_G$$

$$s_{ig,flicker}(f) = \frac{KGFN \cdot I_G^2}{f}$$

Here is a table that lists the parameter names and their meaning in the Spectre Noise Summary table for the EKV3.0 model.

Parameter	Meaning
`fn_id`	Channel current flicker noise
`fn_ig`	Channel current gate noise
`rs`	Source parasitic resistor thermal noise
`rd`	Drain parasitic resistor thermal noise
`rg`	Gate parasitic resistor thermal noise
`rsb`	Thermal noise for the substrate resistor connected between BSi and B (see Figure on page 2126).
`rdb`	Thermal noise for the substrate resistor connected between BDi and B (see Figure on page 2126).
`rbbs`	Thermal noise for the substrate resistor connected between BSi and Bi (see Figure on page 2126 where it is labeled $R_{DSB}/2$
`rbbd`	Thermal noise for the substrate resistor connected between BDi and Bi (see Figure on page 2126 where it is labeled $R_{DSB}/2$
`id`	Thermal noise of the channel resistor
`cor`	Induced gate noise
`shot_ig`	Gate current shot noise

© 2023 Cadence Design Systems, Inc.

Diodes

Temperature Dependence

(28-63)

$$JS_t = \mathbf{JS} \cdot \exp\left(\frac{U_{T,nom} \quad U_T \quad T_{NOM}}{\mathbf{ND}}\right)$$

$$JSW_t = \mathbf{JSW} \cdot \exp\left(\frac{\frac{E_{g,nom}}{U_{T,nom}} - \frac{E_g}{U_T} + \mathbf{XTI} \cdot \frac{T}{T_{NOM}}}{\mathbf{ND}}\right)$$

$$JSWG_t = \mathbf{JSWG} \cdot \exp\left(\frac{\frac{E_{g,nom}}{U_{T,nom}} - \frac{E_g}{U_T} + \mathbf{XTI} \cdot \frac{T}{T_{NOM}}}{\mathbf{ND}}\right)$$

$$PB_t = \mathbf{PB} - \mathbf{TPB} \cdot (T - T_{NOM})$$

$$PBSW_t = \mathbf{PBSW} - \mathbf{TPBSW} \cdot (T - T_{NOM})$$

$$PBSWG_t = \mathbf{PBSWG} - \mathbf{TPBSWG} \cdot (T - T_{NOM})$$

$$CJ_t = \mathbf{CJ} \cdot (1 + \mathbf{TCJ} \cdot (T - T_{NOM}))$$

$$CJSW_t = \mathbf{CJSW} \cdot (1 + \mathbf{TCJSW} \cdot (T - T_{NOM}))$$

$$CJSWG_t = \mathbf{CJSWG} \cdot (1 + \mathbf{TCJSWG} \cdot (T - T_{NOM}))$$

(28-64)

© 2023 Cadence Design Systems, Inc.

$$\mathrm{JTS_t} = \mathbf{JTS} \cdot \exp\left(\frac{\mathrm{E_{g,nom}}}{\mathrm{U_T}} \cdot \mathbf{XTS} \cdot \left(1 - \frac{\mathrm{T}}{\mathrm{T_{NOM}}}\right)\right)$$

$$\mathrm{JTSW_t} = \mathbf{JTSW} \cdot \exp\left(\frac{\mathrm{E_{g,nom}}}{\mathrm{U_T}} \cdot \mathbf{XTSW} \cdot \left(1 - \frac{\mathrm{T}}{\mathrm{T_{NOM}}}\right)\right)$$

$$\mathrm{JTSWG_t} = \mathbf{JTSWG} \cdot \exp\left(\frac{\mathrm{E_{g,nom}}}{\mathrm{U_T}} \cdot \mathbf{XTSWG} \cdot \left(1 - \frac{\mathrm{T}}{\mathrm{T_{NOM}}}\right)\right)$$

$$\mathrm{NJTS_t} = \mathbf{NJTS} \cdot \left(1 + \left(\frac{\mathrm{T}}{\mathrm{T_{NOM}}} - 1\right) \cdot \mathbf{TNJTS}\right)$$

$$\mathrm{NJTSSW_t} = \mathbf{NJTSSW} \cdot \left(1 + \left(\frac{\mathrm{T}}{\mathrm{T_{NOM}}} - 1\right) \cdot \mathbf{TNJTSSW}\right)$$

$$\mathrm{NJTSSWG_t} = \mathbf{NJTSSWG} \cdot \left(1 + \left(\frac{\mathrm{T}}{\mathrm{T_{NOM}}} - 1\right) \cdot \mathbf{TNJTSSWG}\right)$$

Area and Perimeter

(28-65)

$$\mathrm{AS} = 2 \cdot \mathbf{HDIF} \cdot \mathrm{W_{eff}} \cdot \mathbf{NF}$$

$$\mathrm{AD} = 2 \cdot \mathbf{HDIF} \cdot \mathrm{W_{eff}} \cdot \mathbf{NF}$$

$$\mathrm{PS} - (4 \cdot \mathbf{HDIF} + \mathrm{W_{eff}}) \cdot \mathbf{NF}$$

$$\mathrm{PD} = (4 \cdot \mathbf{HDIF} + \mathrm{W_{eff}}) \cdot \mathbf{NF}$$

© 2023 Cadence Design Systems, Inc.

Junction Current

(28-66)

$$I_{S,D} = JS_t \cdot AD + JSW_t \cdot PD + JSWG_t \cdot W_{sff} \cdot \mathbf{NF}$$

$$f_{breakdown,d} = 1 + \mathbf{XJBV} \cdot \exp\left(-\frac{-V(di,b) + \mathbf{BV}}{U_T \cdot \mathbf{ND} \cdot T_{NOM}}\right)$$

$$\begin{aligned} I_{DE,tun} =& W_{eff} \cdot \mathbf{NF} \cdot JTSWG_t \cdot \left(\exp\left(\frac{V(di,b) \cdot T}{T_{NOM} \cdot U_T \cdot NJTSSWG_t} \frac{\mathbf{VTSSWG}}{\mathbf{VTSSWG} + V(ci,b)}\right) - 1\right) \\ &+ PD \cdot JTSW_t \cdot \left(\exp\left(\frac{V(di,b) \cdot T}{T_{NOM} \cdot U_T \cdot NJTSSW_t} \frac{\mathbf{VTSSW}}{\mathbf{VTSSW} + V(di,b)}\right) - 1\right) \\ &+ AD \cdot JT_t \cdot \left(\exp\left(\frac{V(di,b) \cdot T}{T_{NOM} \cdot U_T \cdot NJTS_t} \frac{\mathbf{VTS}}{\mathbf{VTS} + V(di,b)}\right) - 1\right) \end{aligned}$$

$$I_{DBJ} = I_{S,D} \cdot \left(1 - \exp\left(-\frac{V(di,b) \cdot T}{T_{NOM} \cdot U_T \cdot \mathbf{ND}}\right)\right) \cdot f_{breakdown,d} + V(di,b) \cdot \mathbf{GMIN}$$

Junction Capacitance

(28-67)

if $V(di,b) \geq 0$

$$\begin{aligned} C_{DBJ} =& CJ_t \cdot AD \cdot \exp\left(\mathbf{MJ} \cdot \ln\left(1 + \frac{V(di,b)}{PB_t}\right)\right) + \\ &+ CJSW_t \cdot PD \cdot \exp\left(\mathbf{MJSW} \cdot \ln\left(1 + \frac{V(di,b)}{PBSW_t}\right)\right) + \\ &+ CJSWG_t \cdot W_{eff} \cdot \mathbf{NF} \cdot \exp\left(\mathbf{MJSWG} \cdot \ln\left(1 - \frac{V(di,b)}{PBSWG_t}\right)\right) \end{aligned}$$

if $V(di,b) < 0$

$$\begin{aligned} C_{DBJ} =& CJ_t \cdot AD \cdot \left(1 - \mathbf{MJ} \cdot \frac{V(di,b)}{PB_t}\right) + \\ &+ CJSW_t \cdot PD \cdot \left(1 - \mathbf{MJSW} \cdot \frac{V(di,b)}{PBSW_t}\right) + \\ &+ CJSWG_t \cdot W_{eff} \cdot \mathbf{NF} \cdot \left(1 - \mathbf{MJSWG} \cdot \frac{V(di,b)}{PBSWG_t}\right) \end{aligned}$$

© 2023 Cadence Design Systems, Inc.

External Resistors (Gate, Series, Bulk)

(28-68)

$$RS = \frac{\mathbf{HDIF} \cdot \mathbf{RSH} + \left(\mathbf{LDIF} - \frac{\mathbf{DL}}{2}\right) \cdot \mathbf{RS}}{W_{eff}\mathbf{NF}}$$

$$RD - \frac{\mathbf{HDIF} \cdot \mathbf{RSH} + \left(\mathbf{LDIF} - \frac{\mathbf{DL}}{2}\right) \cdot \mathbf{RD}}{W_{eff}\mathbf{NF}}$$

$$RS_g = ES \cdot \left(1 + \frac{\mathbf{WRLX}}{W_{eff}}\right)$$

$$RD_g = RD \cdot \left(1 + \frac{\mathbf{WRLX}}{W_{eff}}\right)$$

$$RG = \mathbf{RGSH} \cdot \frac{W_{eff}}{3 \cdot \mathbf{GC}^2 \cdot \mathbf{NF} \cdot L_{eff}}$$

$$RDSB = \mathbf{RDSBSH} \cdot \frac{L_{eff}}{L_{eff} \cdot \mathbf{NF}}$$

(28-69)

© 2023 Cadence Design Systems, Inc.

if $\mathbf{RINGTYPE} = 1(\mathrm{HORSE-SHOE})$

$$\mathrm{RB} = \begin{cases} \dfrac{\mathbf{RBWSH}}{2 \cdot W_{eff}} & \text{if } \mathrm{RBN} = 0 \\ \dfrac{1}{\dfrac{2 \cdot W_{eff}}{\mathbf{RBWSH}} + \dfrac{\mathbf{NF}}{\mathbf{RBN}}} & \text{if } \mathrm{RBN} \neq 0 \end{cases}$$

if **NF** is even

$$\mathrm{RSB} = \begin{cases} \dfrac{\mathbf{RSBWSH}}{2 \cdot W_{eff}} & \text{if } \mathbf{RSBN} = 0 \\ \dfrac{1}{\dfrac{2 \cdot W_{eff}}{\mathbf{RSBWSH}} + \dfrac{\mathbf{NF}}{\mathbf{RSBN}}} & \text{if } \mathbf{RSBN} \neq 0 \end{cases}$$

$$\mathrm{RDB} = \begin{cases} \dfrac{\mathbf{RDBWSH}}{2 \cdot W_{eff}} & \text{if } \mathbf{RDBN} = 0 \\ \dfrac{1}{\dfrac{2 \cdot W_{eff}}{\mathbf{RDBWSH}} + \dfrac{\mathbf{NF}}{\mathbf{RDBN}}} & \text{if } \mathbf{RDBN} \neq 0 \end{cases}$$

if **NF** is odd

$$\mathrm{RSB} = \begin{cases} \dfrac{\mathbf{RSBWSH}}{W_{eff}} & \text{if } \mathbf{RSBN} = 0 \\ \dfrac{1}{\dfrac{W_{eff}}{\mathbf{RSBWSH}} + \dfrac{\mathbf{NF}}{\mathbf{RSBN}}} & \text{if } \mathbf{RSBN} \neq 0 \end{cases}$$

$$\mathrm{RDB} = \mathrm{RSB}$$

(28-70)

© 2023 Cadence Design Systems, Inc.

if $\mathbf{RINGTYPE} = 2(\mathrm{SYMMETRIC})$

$$\mathrm{RB} = \frac{\mathbf{RBWSH}}{2 \cdot \mathrm{W_{eff}}}$$

if **NF** is even

$$\mathrm{RSB} = \frac{\mathbf{RSBWSH}}{2 \cdot \mathrm{W_{eff}}}$$

$$\mathrm{RDB} = \frac{\mathbf{RDBWSH}}{2 \cdot \mathrm{W_{eff}}}$$

---

if **NF** is odd

$$\mathrm{RSB} = \frac{\mathbf{RSBWSH}}{\mathrm{W_{eff}}}$$

$$\mathrm{RDB} = \mathrm{RSB}$$

Temperature Dependence

(28-71)

$$\mathrm{RS_{gt}} = \mathrm{RS_g} \cdot (1 + \mathbf{TR} \cdot (\mathrm{T} - \mathrm{T_{NOM}}) + \mathbf{TR2} \cdot (\mathrm{T} - \mathrm{T_{NOM}})^2)$$

$$\mathrm{RD_{gt}} = \mathrm{RD_g} \cdot (1 + \mathbf{TR} \cdot (\mathrm{T} - \mathrm{T_{NOM}}) + \mathbf{TR2} \cdot (\mathrm{T} - \mathrm{T_{NOM}})^2)$$

$$\mathrm{RG_t} = \mathrm{RG} \cdot (1 + \mathbf{TR} \cdot (\mathrm{T} - \mathrm{T_{NOM}}) + \mathbf{TR2} \cdot (\mathrm{T} - \mathrm{T_{NOM}})^2)$$

$$\mathrm{RB_t} = \mathrm{RB} \cdot (1 + \mathbf{TR} \cdot (\mathrm{T} - \mathrm{T_{NOM}}) + \mathbf{TR2} \cdot (\mathrm{T} - \mathrm{T_{NOM}})^2)$$

$$\mathrm{RSB_t} = \mathrm{RSB} \cdot (1 + \mathbf{TR} \cdot (\mathrm{T} - \mathrm{T_{NOM}}) + \mathbf{TR2} \cdot (\mathrm{T} - \mathrm{T_{NOM}})^2)$$

$$\mathrm{RDB_t} = \mathrm{RDB} \cdot (1 + \mathbf{TR} \cdot (\mathrm{T} - \mathrm{T_{NOM}}) + \mathbf{TR2} \cdot (\mathrm{T} - \mathrm{T_{NOM}})^2)$$

$$\mathrm{RDSB_t} = \mathrm{RDSB} \cdot (1 + \mathbf{TR} \cdot (\mathrm{T} - \mathrm{T_{NOM}}) + \mathbf{TR2} \cdot (\mathrm{T} - \mathrm{T_{NOM}})^2)$$

Related Topics

EKV3 MOSFET Model (ekv3)

Model Usage

© 2023 Cadence Design Systems, Inc.

Component Statements

Device ekv3_nqs (ekv3_nqs)

Device ekv3_r4 (ekv3_r4)

Device ekv3_rf (ekv3_rf)

Device ekv3_s (ekv3_s)

Model Usage

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Model Syntax

```
model modelName ekv3 parameter=value ...
```

Related Topics

EKV3 MOSFET Model (ekv3)

Model Equations

Component Statements

Device ekv3_nqs (ekv3_nqs)

Device ekv3_r4 (ekv3_r4)

Device ekv3_rf (ekv3_rf)

Device ekv3_s (ekv3_s)

© 2023 Cadence Design Systems, Inc.

Component Statements

Instance Parameters

`l=10.0E-06`	Gate's length.
`w=10.0E-06`	Gate's width.
`nf=1`	Number of fingers.
`m=1`	Number of devices in parallel.
`ad=0.0`	Drain's area.
`as=0.0`	Source's area.
`pd=0.0`	Drain's perimeter.
`ps=0.0`	Source's perimeter.
`sa=0.0`	Sti parameter; distance from sti (side a).
`sb=0.0`	Sti parameter; distance from sti (side b).
`sd=0.0`	Sti parameter; distance between gates.
`trise=0.0`	Temperature change for particular transistor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Parameters

`version=301.02`	Parameter for version control. Supported versions are 301.02 and 302.00. The default version is 301.02.
`sign=1`	Sign = 1 for nmos; sign = -1 for pmos.
`tg=(-1)`	Type of gate: -1 enhancement type; 1 depletion type.
`tnom=27.0`	Nominal temperature for model parameters.
`scale=1.0`	Scaling size factor.
`xl=0.0`	Optical offset for channel length.
`xw=0.0`	Optical offset for channel width.

© 2023 Cadence Design Systems, Inc.

nqs_noi=1.0	Flag for turning on nqs thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1.
th_noi=0.0	Flag for turning on short channel effects thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1.
info_level=0.0	Flag for information printout. currently only value of 1 is supported.
qoff=0.0	Flag for turning off the dynamic behavior of the model (for debugging purposes).
avto=0.0	Matching parameter for threshold voltage (vto).
agamma=0.0	Matching parameter for body factor (gamma).
akp=0.0	Matching parameter for mobility (kp).
cox=0.012	Oxide capacitance per unit area.
xj=20.0E-09	Depth of junction (source and drain).
vto=0.3	Threshold voltage.
phif=0.45	Fermi bulk potential.
gamma=0.3	Body effect coefficient.
gammag=4.1	Gate doping coefficient for polysilicon depletion effect.
n0=1.0	Weak inversion fine tuning parameter.
vbi=0.0	Built-in voltage drop-off. If left to default zero value, it is set to the nominal value of 3ut higher than phi.
aqma=0.5	Quantum mechanical effect accumulation region coefficient.
aqmi=0.4	Quantum mechanical effect inversion region coefficient.
etaqm=0.75	Quantum mechanical effect accumulation eta parameter.
kp=500.0E-06	Mobility (multiplied by cox) parameter.
e0=1.0E+10	First order parameter for mobility reduction due to vertical field effect.
e1=3.1E+08	Second order parameter for mobility reduction due to vertical field effect.
eta=0.5	Inversion charge coefficient for vertical field calculation.
thc=0.0	Coulomb scattering parameter.

© 2023 Cadence Design Systems, Inc.

zc=1.0E-6	Coulomb scattering inversion charge coefficient.
la=1.0	Critical length a of mobility length scaling.
lb=1.0	Critical length b of mobility length scaling.
ka=0.0	Parameter for critical length a of mobility length scaling.
kb=0.0	Parameter for critical length b of mobility length scaling.
wkp1=1.0E-6	Critical width of mobility width scaling.
wkp2=0.0	Amplitude parameter for mobility width scaling.
wkp3=1.0	Span parameter for mobility width scaling.
dl=(-10.0E-9)	Effective length parameter.
dlc=0.0	Effective length parameter for dynamic behavior.
dw=(-10.0E-9)	Effective width parameter.
dwc=0.0	Effective width parameter for dynamic behavior.
wdl=0.0	Effective length parameter for narrow channel devices.
ldw=0.0	Effective width parameter for short channel devices.
ll=0.0	Base of exponential model for effective length.
lln=1.0	Exponent of exponential model for effective length.
avt=0.0	Parameter for long and wide channel vto correction.
lvt=1.0	Length for long and wide channel vto correction.
wvt=1.0	Width for long and wide channel vto correction.
agam=0.0	Parameter for long and wide channel gamma correction.
lgam=1.0	Length for long and wide channel gamma correction.
wgam=1.0	Width for long and wide channel gamma correction.
nfvta=0.0	Number of fingers for vto correction for multifinger devices (obsolete model by sti stress effect).
nfvtb=10000.0	Parameter for vto correction for multifinger devices (obsolete model by sti stress effect).
ucrit=5.0E+06	Critical velocity of velocity saturation effect.
delta=2.0	Variable order (from 1.0 to 2.0) of velocity saturation effect.
lambda=0.5	Length parameter for channel length modulation.

© 2023 Cadence Design Systems, Inc.

aclm=0.83	Fine tuning parameter for channel length modulation.
lr=50.0E-09	Length parameter for reverse short channel effect.
qlr=0.5E-3	Charge parameter for reverse short channel effect (vto).
nlr=10.0E-3	Doping parameter for reverse short channel effect (gamma).
flr=1.0	Fermi potential fine tuning parameter for reverse short channel effect (phif).
leta0=0.0	Length independent parameter for charge sharing (long channel).
leta=500.0E-3	Length scaling parameter for charge sharing.
leta2=0.0	Second order length scaling parameter for charge sharing (shortest channel).
weta=200.0E-3	Width scaling parameter for charge sharing.
ncs=1.0	Weak inversion slope parameter for charge sharing.
etad=1.0	Eta parameter for drain induced barrier lowering.
sigmad=1.0	Sigma parameter for drain induced barrier lowering.
wr=90.0E-09	Width parameter for inverse narrow channel effect.
qwr=0.3E-3	Charge parameter for inverse narrow channel effect (vto).
nwr=5.0E-3	Doping parameter for inverse narrow channel effect (gamma).
fprout=1.0E6	Output resistance parameter for drain induced threshold shift.
pdits=0.0	Parameter for drain induced threshold shift (if set to zero the dits effect is disabled).
pditsl=0.0	Length scaling parameter for drain induced threshold shift.
pditsd=1.0	Bias parameter for drain induced threshold shift.
ddits=0.3	Smooth factor of output conductance for drain induced threshold shift.
iba=000.0E+06	Parameter a of impact ionization current.
ibb=300.0E+06	Parameter b of impact ionization current.
ibn=1.0	Parameter n of impact ionization current.

© 2023 Cadence Design Systems, Inc.

xb=3.1	Silicon to silicon oxide tunneling barrier height.
eb=29.0E+09	Characteristic electrical field.
kg=00.0E-6	Mobility for gate current.
lovig=20.0E-9	Overlap gate length for overlap gate current.
agidl=0.0	Parameter a of gate induced drain leakage.
bgidl=2.3E+09	Parameter b of gate induced drain leakage.
cgidl=0.5	Parameter c of gate induced drain leakage.
egidl=0.8	Parameter e of gate induced drain leakage.
lfnoi=0	Flicker noise model selection.
kf=0.0	Flicker noise parameter.
af=1.0	Flicker noise frequency exponent.
ef=2.0	Flicker noise transconductance exponent.
nt=1.0E+14	Number of trapped carriers.
alphac=10.0E+4	Coulomb scattering coefficient.
alphah=1.0E-20	Hooge parameter for mobility fluctuation noise model.
kgfn=0.0	Gate flicker noise parameter.
ecn=1.0E+4	Critical field value.
sdr=1.0E-6	Series resistance noise parameter.
lwr=0.0	Length scaling parameter for wr.
lqwr=0.0	Length scaling parameter for qwr.
lnwr=0.0	Length scaling parameter for nwr.
ldphiedge=0.0	Length scaling parameter for dphiedge.
wlr=0.0	Width scaling parameter for lr.
wqlr=0.0	Width scaling parameter for qlr.
wnlr=0.0	Width scaling parameter for nlr.
wucrit=0.0	Width scaling parameter for ucrit.
wlambda=0.0	Width scaling parameter for lambda.
wetad=0.0	Width scaling parameter for etad.
we0=0.0	Width scaling parameter for e0.

© 2023 Cadence Design Systems, Inc.

`we1=0.0`	Width scaling parameter for e1.
`wrlx=0.0`	Width scaling parameter for rlx.
`wucex=0.0`	Width scaling parameter for ucex.
`wdphiedge=0.0`	Width scaling parameter for dphiedge.
`wldphiedge=0.0`	Fine tuning scaling for combined short and narrow devices for dphiedge.
`wldgammaedge=0.0`	Fine tuning scaling for combined short and narrow devices for dgammaedge.
`wedge=0.0`	Total effective width of edge device for edge conductance effect.
`dgammaedge=0.0`	Differential gamma parameter of edge device with respect to the main device.
`dphiedge=0.0`	Differential phi parameter of edge device with respect to the main device.
`saref=0.0`	Reference sa parameter for sti stress effect parameter extraction.
`sbref=0.0`	Reference sb parameter for sti stress effect parameter extraction.
`wlod=0.0`	Width effective parameter for sti stress effect.
`kkp=0.0`	Mobility parameter for sti stress effect.
`lkkp=0.0`	Length scaling of mobility for sti stress effect.
`wkkp=0.0`	Width scaling of mobility for sti stress effect.
`pkkp=0.0`	Area scaling of mobility for sti stress effect.
`tkkp=0.0`	Temperature scaling of mobility for sti stress effect.
`llodkkp=1.0`	Exponential length scaling parameter of mobility for sti stress effect.
`wlodkkp=1.0`	Exponential width scaling parameter of mobility for sti stress effect.
`kvto=0.0`	Threshold voltage parameter for sti stress effect.
`lkvto=0.0`	Length scaling of threshold voltage for sti stress effect.
`wkvto=0.0`	Width scaling of threshold voltage for sti stress effect.
`pkvto=0.0`	Area scaling of threshold voltage for sti stress effect.

© 2023 Cadence Design Systems, Inc.

`llodkvto=1.0`	Exponential length scaling parameter of threshold voltage for sti stress effect.
`wlodkvto=1.0`	Exponential width scaling parameter of threshold voltage for sti stress effect.
`kgamma=0.0`	Body effect coefficient parameter for sti stress effect.
`lodkgamma=1.0`	Fine tuning parameter for body effect coefficient scaling of sti stress effect.
`ketad=0.0`	Dibl effect parameter for sti stress effect.
`lodketad=1.0`	Fine tuning parameter for dibl effect parameter scaling of sti stress effect.
`kucrit=0.0`	Critical velocity of velocity saturation effect parameter for sti stress effect.
`tcv=600.0E-6`	Temperature scaling of threshold voltage.
`bex=(-1.5)`	Temperature scaling of mobility.
`te0ex=0.5`	Temperature scaling of e0.
`te1ex=0.5`	Temperature scaling of e1.
`teta=(-0.9E-3)`	Temperature scaling of eta parameter.
`ucex=1.5`	Temperature scaling of critical velocity of velocity saturation effect.
`tlambda=0.0`	Temperature scaling of lambda parameter.
`ibbt=800.0E-6`	Temperature scaling of ibb.
`tcvl=0.0`	Length scaling of tcv.
`tcvw=0.0`	Width scaling of tcv.
`tcvwl=0.0`	Area scaling of tcv.
`gammaov=1.6`	Body effect coefficient of the gate overlap region.
`gammagov=10.0`	Gate doping coefficient for polysilicon depletion effect of the gate overlap region.
`vfbov=0.0`	Flat-band voltage of the gate overlap region.
`lov=20.0E-9`	Effective length of the gate overlap region.
`vov=1.0`	Bias parameter of the overlap capacitances.

© 2023 Cadence Design Systems, Inc.

`cgso=0.0`	Bias-independent overlap capacitance per gate width unit between gate and source.
`cgdo=0.0`	Bias-independent overlap capacitance per gate width unit between gate and drain.
`cgbo=0.0`	Bias-independent overlap capacitance per gate length unit between gate and bulk.
`kjf=0.0`	Fringing capacitance parameter.
`cjf=0.0`	Bias scaling of fringing capacitance.
`vfr=0.0`	Built-in voltage fine tuning for fringing capacitance model.
`dfr=1.0E-3`	Smooth parameter of fringing capacitance model.
`hdif=0.0e-6`	Half length of the active area.
`rsh=0.0`	Square resistance of active area.
`ldif=0.0`	Distance between the middle of the active area and the start of the channel.
`rs=0.0`	Ldd source series resistance.
`rd=0.0`	Ldd drain series resistance.
`rlx=(-1.0)`	External series resistance per width unit.
`rsx=(-1.0)`	External series resistance per width unit, source side (asymmetric model).
`rdx=(-1.0)`	External series resistance per width unit, drain side (asymmetric model).
`tr=0.0`	First order resistance temperature scaling parameter.
`tr2=0.0`	Second order resistance temperature scaling parameter.
`gmin=0.0`	Minimum conductance of junction diodes.
`njs=1.0`	Slope factor for junction diode, source side (asymmetrical model).
`xjbvs=0.0`	Break-down effect coefficient for junction diode, source side (asymmetrical model).
`bvs=10.0`	Break-down voltage for junction diode, source side (asymmetrical model).
`jss=0.0E-09`	Area component of current for junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`jssws=0.0E-12`	Sideways component of current for junction diode, source side (asymmetrical model).
`jsswgs=0.0E-12`	Gate-side component of current for junction diode, source side (asymmetrical model).
`jtss=0.0E-09`	Area component of trap-assisted current for junction diode, source side (asymmetrical model).
`jtssws=0.0E-12`	Sideways component of trap-assisted current for junction diode, source side (asymmetrical model).
`jtsswgs=0.0E-12`	Gateside component of trap-assisted current for junction diode, source side (asymmetrical model).
`njtss=1.0`	Area slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`njtssws=1.0`	Sideways slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`njtsswgs=1.0`	Gateside slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`vtss=0.0`	Area voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
`vtssws=0.0`	Sideways voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
`vtsswgs=0.0`	Gateside voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
`cjs=0.0E-06`	Area component of capacitance for junction diode, source side (asymmetrical model).
`cjsws=0.0E-09`	Sideways component of capacitance for junction diode, source side (asymmetrical model).
`cjswgs=0.0E-09`	Gateside component of capacitance for junction diode, source side (asymmetrical model).
`pbs=0.800`	Area parameter of capacitance for junction diode, source side (asymmetrical model).
`pbsws=0.600`	Sideways parameter of capacitance for junction diode, source side (asymmetrical model).
`pbswgs=0.600`	Gateside parameter of capacitance for junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`mjs=0.900`	Area exponent of capacitance for junction diode, source side (asymmetrical model).
`mjsws=0.700`	Sideways exponent of capacitance for junction diode, source side (asymmetrical model).
`mjswgs=0.700`	Gateside exponent of capacitance for junction diode, source side (asymmetrical model).
`xtis=3.0`	Temperature dependence for junction diode, source side (asymmetrical model).
`xtss=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtssws=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtsswgs=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`tnjtss=0.0`	Temperature dependence of njtss (area), junction diode, source side (asymmetrical model).
`tnjtssws=0.0`	Temperature dependence of njtssws (sideways), junction diode, source side (asymmetrical model).
`tnjtsswgs=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, source side (asymmetrical model).
`tcj=0.0`	Temperature dependence of area component of capacitance for junction diodes (cjs and cjd), both (source and drain) sides (asymmetrical model).
`tcjsw=0.0`	Temperature dependence of sideways component of capacitance for junction diodes (cjsws and cjswd), both (source and drain) sides (asymmetrical model).
`tcjswg=0.0`	Temperature dependence of gateside component of capacitance for junction diodes (cjswgs and cjswgd), both (source and drain) sides (asymmetrical model).
`tpb=0.0`	Temperature dependence of area parameter of capacitance for junction diodes (pbs and pbd), both (source and drain) sides (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`tpbsw=0.0`	Temperature dependence of sideways parameter of capacitance for junction diodes (pbsws and pbswd), both (source and drain) sides (asymmetrical model).
`tpbswg=0.0`	Temperature dependence of gateside parameter of capacitance for junction diodes (pbswgs and pbswgd), both (source and drain) sides (asymmetrical model).
`njd=1.0`	Slope factor for junction diode, drain side (asymmetrical model).
`xjbvd=0.0`	Break-down effect coefficient for junction diode, drain side (asymmetrical model).
`bvd=10.0`	Break-down voltage for junction diode, drain side (asymmetrical model).
`jsd=0.0E-09`	Area component of current for junction diode, drain side (asymmetrical model).
`jsswd=0.0E-12`	Sideways component of current for junction diode, drain side (asymmetrical model).
`jsswgd=0.0E-12`	Gate-side component of current for junction diode, drain side (asymmetrical model).
`jtsd=0.0E-09`	Area component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswd=0.0E-12`	Sideways component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswgd=0.0E-12`	Gateside component of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsd=1.0`	Area slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswd=1.0`	Sideways slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswgd=1.0`	Gateside slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsd=0.0`	Area voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsswd=0.0`	Sideways voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`vtsswgd=0.0`	Gateside voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`cjd=0.0E-06`	Area component of capacitance for junction diode, drain side (asymmetrical model).
`cjswd=0.0E-09`	Sideways component of capacitance for junction diode, drain side (asymmetrical model).
`cjswgd=0.0E-09`	Gateside component of capacitance for junction diode, drain side (asymmetrical model).
`pbd=0.800`	Area parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswd=0.600`	Sideways parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswgd=0.600`	Gateside parameter of capacitance for junction diode, drain side (asymmetrical model).
`mjd=0.900`	Area exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswd=0.700`	Sideways exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswgd=0.700`	Gateside exponent of capacitance for junction diode, drain side (asymmetrical model).
`xtid=3.0`	Temperature dependence for junction diode, drain side (asymmetrical model).
`xtsd=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`xtsswd=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`xtsswgd=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`tnjtsd=0.0`	Temperature dependence of njtss (area), junction diode, drain side (asymmetrical model).
`tnjtsswd=0.0`	Temperature dependence of njtssws (sideways), junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`tnjtsswgd=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, drain side (asymmetrical model).
`rgsh=3.0`	Gate sheet resistance.
`gc=1`	Type of gate contacts (gc = 1: single sided, gc = 2: both sides).
`krgl1=0.0`	Gate resistance length scaling parameter.
`rdsbsh=1.0E+3`	Substrate network sheet resistance between internal drain and source nodes (used at rf and nqs modes).
`rbwsh=3.0E-3`	Substrate network bulk resistance per width unit between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rbn=0.0`	Substrate network bulk resistance per finger between internal bulk and external bulk nodes (used at rf4, rf, and nqs modes).
`rsbwsh=1.0E-3`	Substrate network resistance per width unit between internal source and external bulk nodes (used at rf and nqs modes).
`rsbn=0.0`	Substrate network resistance per finger between internal source and external bulk nodes (used at rf and nqs modes).
`rdbwsh=1.0E-3`	Substrate network resistance per width unit between internal drain and external bulk nodes (used at rf and, nqs modes).
`rdbn=0.0`	Substrate network resistance per finger between internal drain and external bulk nodes (used at rf and nqs, modes).
`ringtype=1.0`	Ringtype, shape of bulk connector (ringtype = 1 for horse-shoe, three sides contact, ringtype = 2 for symmetric, two sides contact), (used at rf4, rf and nqs modes).

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`vs (V)`	Vs.
`vd (V)`	Vd.
`vg (V)`	Vg.
`vb (V)`	Vb.
`vds (V)`	Vds.
`vgs (V)`	Vgs.
`vbs (V)`	Vbs.
`vdb (V)`	Vdb.
`vgb (V)`	Vgb.
`beta (A/V`^{2}`)`	Beta.
`idsi (A)`	Intrinsic current.
`idsedge (A)`	Edge effect current.
`idex (A)`	Extrinsic current drain side.
`isex (A)`	Extrinsic current source side.
`igex (A)`	Extrinsic current gate side.
`ibex (A)`	Extrinsic current bulk side.
`n`	Slope factor n.
`vp`	Pinch-off voltage.
`vod (V)`	Overdrive voltage n*(vp-vs).
`vdsat (V)`	Saturation voltage.
`sat (s)`	Saturation flag.
`vth (V)`	Effective threshold voltage vth.
`vtb (V)`	Effective threshold voltage vtb.
`weffnf (m)`	Effective total width.
`weff (m)`	Effective finger width.
`leff (m)`	Effective length.
`op_nf`	Number of fingers.

© 2023 Cadence Design Systems, Inc.

ic	Inversion coefficient.
ispec (A)	Specific current.
gmgi (S)	Intrinsic gate tranconductance.
gmsi (S)	Intrinsic source tranconductance.
gmdi (S)	Intrinsic drain tranconductance.
gmbi (S)	Intrinsic bulk tranconductance.
gmgex (S)	Extrinsic gate tranconductance.
gmsex (S)	Extrinsic source tranconductance.
gmdex (S)	Extrinsic drain tranconductance.
gds (S)	Extrinsic drain tranconductance, alias to Gmdex.
gmbex (S)	Extrinsic bulk tranconductance.
gmgutid	Gmg*ut/ids.
gmsutid	Gms*ut/ids.
gmdutid	Gmd*ut/ids.
gmbutid	Gmb*ut/ids.
avi	Intrinsic gain.
gmgid (1/V)	Gm/ids.
vm (V)	Early voltage ids/gds.
ft (Hz)	Transit frequency.
tau0 (s)	Tau0.
tau (s)	Nqs time constant.
cggi (F)	Cggi.
cgsi (F)	Cgsi.
cgdi (F)	Cgdi.
cgbi (F)	Cgbi.
csgi (F)	Csgi.
csdi (F)	Csdi.
csbi (F)	Csbi.
cssi (F)	Cssi.

© 2023 Cadence Design Systems, Inc.

`cdgi (F)`	Cdgi.
`cddi (F)`	Cddi.
`cdbi (F)`	Cdbi.
`cdsi (F)`	Cdsi.
`cbgi (F)`	Cbgi.
`cbdi (F)`	Cbdi.
`cbbi (F)`	Cbbi.
`cbsi (F)`	Cbsi.
`cgsex (F)`	Extrinsic gate-source capacitance.
`cgdex (F)`	Extrinsic gate-drain capacitance.
`cgbex (F)`	Extrinsic gate-bulk capacitance.
`ctotex (F)`	Total extrinsic capacitance.
`cgsov (F)`	Cgsov.
`cgdov (F)`	Cgdov.
`sid_flicker (`A^2`/Hz)`	Flicker noise psd sdid @ 1hz.
`sid_thermal (`A^2`/Hz)`	Thermal noise psd sdid.
`svg_flicker (`V^2`/Hz)`	Flicker noise psd sdvg @ 1hz.
`svg_thermal (`V^2`/Hz)`	Thermal noise psd sdvg.
`sigmadidoid`	Relative current mismatch.
`sigmavg (V)`	Gate voltage offset.
`i0 (V)`	Technology current.
`qs (C)`	Source charge.
`qd (C)`	Drain charge.
`qg (C)`	Gate charge.
`qb (C)`	Bulk charge.

© 2023 Cadence Design Systems, Inc.

`ids (A)`	Resistive drain-to-source current.
`idb (A)`	Impact ionization current.
`qsedge (C)`	Edge charge.
`qdedge (C)`	Edge charge.
`qgedge (C)`	Edge charge.
`qbedge (C)`	Edge charge.
`qsov (C)`	Source side overlap charge.
`qdov (C)`	Drain sie overlap charge.
`qsfr (C)`	Source side fringing charge.
`qdfr (C)`	Drain side fringing charge.
`igidl (A)`	Gate induced drain current.
`igisl (A)`	Gate induced source current.
`igb (A)`	Gate current (bulk).
`igd (A)`	Gate current (drain).
`igs (A)`	Gate current (source).
`igdov (A)`	Overlap gate current (drain).
`igsov (A)`	Overlap gate current (source).
`region`	Estimated operating region. Spectre outputs a number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`pwr (W)`	Power dissipation.

Related Topics

EKV3 MOSFET Model (ekv3)

Model Equations

Component Statements

Device ekv3_nqs (ekv3_nqs)

Device ekv3_r4 (ekv3_r4)

© 2023 Cadence Design Systems, Inc.

Device ekv3_rf (ekv3_rf)

Device ekv3_s (ekv3_s)

Device ekv3_nqs (ekv3_nqs)

This device is supported within altergroups.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Model Syntax

```
model modelName ekv3_nqs parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`l=10.0E-06`	Gate's length.
`w=10.0E-06`	Gate's width.
`nf=1`	Number of fingers.
`m=1`	Number of devices in parallel.
`ad=0.0`	Drain's area.
`as=0.0`	Source's area.
`pd=0.0`	Drain's perimeter.
`ps=0.0`	Source's perimeter.
`sa=0.0`	Sti parameter; distance from sti (side a).
`sb=0.0`	Sti parameter; distance from sti (side b).
`sd=0.0`	Sti parameter; distance between gates.
`trise=0.0`	Temperature change for particular transistor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Parameters

`version=301.02`	Parameter for version control. Valid values are 301.02 and 302.00. The default version is 301.02.
`sign=1`	Sign = 1 for nmos; sign = -1 for pmos.
`tg=(-1)`	Type of gate: -1 enhancement type; 1 depletion type.
`tnom=27.0`	Nominal temperature for model parameters.
`scale=1.0`	Scaling size factor.
`xl=0.0`	Optical offset for channel length.
`xw=0.0`	Optical offset for channel width.
`nqs_noi=1.0`	Flag turning on nqs thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1.

© 2023 Cadence Design Systems, Inc.

th_noi=0.0	Flag turning on short channel effects thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1.
info_level=0.0	Flag for information printout. currently only value of 1 is supported.
qoff=0.0	Flag for turning off the dynamic behavior of the model (for debugging purposes).
avto=0.0	Matching parameter for threshold voltage (vto).
agamma=0.0	Matching parameter for body factor (gamma).
akp=0.0	Matching parameter for mobility (kp).
cox=0.012	Oxide capacitance per unit area.
xj=20.0E-09	Depth of junction (source and drain).
vto=0.3	Threshold voltage.
phif=0.45	Fermi bulk potential.
gamma=0.3	Body effect coefficient.
gammag=4.1	Gate doping coefficient for polysilicon depletion effect.
n0=1.0	Weak inversion fine tuning parameter.
vbi=0.0	Built-in voltage drop-off. if left to default zero value, it is set to the nominal value of 3ut higher than phi..
aqma=0.5	Quantum mechanical effect accumulation region coefficient.
aqmi=0.4	Quantum mechanical effect inversion region coefficient.
etaqm=0.75	Quantum mechanical effect accumulation eta parameter.
kp=500.0E-06	Mobility (multiplied by cox) parameter.
e0=1.0E+10	First order parameter for mobility reduction due to vertical field effect.
e1=3.1E+08	Second order parameter for mobility reduction due to vertical field effect.
eta=0.5	Inversion charge coefficient for vertical field calculation.
thc=0.0	Coulomb scattering parameter.
zc=1.0E-6	Coulomb scattering inversion charge coefficient.

© 2023 Cadence Design Systems, Inc.

`la=1.0`	Critical length a of mobility length scaling.
`lb=1.0`	Critical length b of mobility length scaling.
`ka=0.0`	Parameter for critical length a of mobility length scaling.
`kb=0.0`	Parameter for critical length b of mobility length scaling.
`wkp1=1.0E-6`	Critical width of mobility width scaling.
`wkp2=0.0`	Amplitude parameter for mobility width scaling.
`wkp3=1.0`	Span parameter for mobility width scaling.
`dl=(-10.0E-9)`	Effective length parameter.
`dlc=0.0`	Effective length parameter for dynamic behavior.
`dw=(-10.0E-9)`	Effective width parameter.
`dwc=0.0`	Effective width parameter for dynamic behavior.
`wdl=0.0`	Effective length parameter for narrow channel devices.
`ldw=0.0`	Effective width parameter for short channel devices.
`ll=0.0`	Base of exponential model for effective length.
`lln=1.0`	Exponent of exponential model for effective length.
`avt=0.0`	Parameter for long and wide channel vto correction.
`lvt=1.0`	Length for long and wide channel vto correction.
`wvt=1.0`	Width for long and wide channel vto correction.
`agam=0.0`	Parameter for long and wide channel gamma correction.
`lgam=1.0`	Length for long and wide channel gamma correction.
`wgam=1.0`	Width for long and wide channel gamma correction.
`nfvta=0.0`	Number of fingers for vto correction for multifinger devices (obsolete model by sti stress effect).
`nfvtb=10000.0`	Parameter for vto correction for multifinger devices (obsolete model by sti stress effect).
`ucrit=5.0E+06`	Critical velocity of velocity saturation effect.
`delta=2.0`	Variable order (from 1.0 to 2.0) of velocity saturation effect.
`lambda=0.5`	Length parameter for channel length modulation.
`aclm=0.83`	Fine tuning parameter for channel length modulation.

© 2023 Cadence Design Systems, Inc.

`lr=50.0E-09`	Length parameter for reverse short channel effect.
`qlr=0.5E-3`	Charge parameter for reverse short channel effect (vto).
`nlr=10.0E-3`	Doping parameter for reverse short channel effect (gamma).
`flr=1.0`	Fermi potential fine tuning parameter for reverse short channel effect (phif).
`leta0=0.0`	Length independent parameter for charge sharing (long channel).
`leta=500.0E-3`	Length scaling parameter for charge sharing.
`leta2=0.0`	Second order length scaling parameter for charge sharing (shortest channel).
`weta=200.0E-3`	Width scaling parameter for charge sharing.
`ncs=1.0`	Weak inversion slope parameter for charge sharing.
`etad=1.0`	Eta parameter for drain induced barrier lowering.
`sigmad=1.0`	Sigma parameter for drain induced barrier lowering.
`wr=90.0E-09`	Width parameter for inverse narrow channel effect.
`qwr=0.3E-3`	Charge parameter for inverse narrow channel effect (vto).
`nwr=5.0E-3`	Doping parameter for inverse narrow channel effect (gamma).
`fprout=1.0E6`	Output resistance parameter for drain induced threshold shift.
`pdits=0.0`	Parameter for drain induced threshold shift (if set to zero the dits effect is disabled).
`pditsl=0.0`	Length scaling parameter for drain induced threshold shift.
`pditsd=1.0`	Bias parameter for drain induced threshold shift.
`ddits=0.3`	Smooth factor of output conductance for drain induced threshold shift.
`iba=000.0E+06`	Parameter a of impact ionization current.
`ibb=300.0E+06`	Parameter b of impact ionization current.
`ibn=1.0`	Parameter n of impact ionization current.
`xb=3.1`	Silicon to silicon oxide tunneling barrier height.

© 2023 Cadence Design Systems, Inc.

`eb=29.0E+09`	Characteristic electrical field.
`kg=00.0E-6`	Mobility for gate current.
`lovig=20.0E-9`	Overlap gate length for overlap gate current.
`agidl=0.0`	Parameter a of gate induced drain leakage.
`bgidl=2.3E+09`	Parameter b of gate induced drain leakage.
`cgidl=0.5`	Parameter c of gate induced drain leakage.
`egidl=0.8`	Parameter e of gate induced drain leakage.
`lfnoi=0`	Flicker noise model selection.
`kf=0.0`	Flicker noise parameter.
`af=1.0`	Flicker noise frequency exponent.
`ef=2.0`	Flicker noise transconductance exponent.
`nt=1.0E+14`	Number of trapped carriers.
`alphac=10.0E+4`	Coulomb scattering coefficient.
`alphah=1.0E-20`	Hooge parameter for mobility fluctuation noise model.
`kgfn=0.0`	Gate flicker noise parameter.
`ecn=1.0E+4`	Critical field value.
`sdr=1.0E-6`	Series resistance noise parameter.
`lwr=0.0`	Length scaling parameter for wr.
`lqwr=0.0`	Length scaling parameter for qwr.
`lnwr=0.0`	Length scaling parameter for nwr.
`ldphiedge=0.0`	Length scaling parameter for dphiedge.
`wlr=0.0`	Width scaling parameter for lr.
`wqlr=0.0`	Width scaling parameter for qlr.
`wnlr=0.0`	Width scaling parameter for nlr.
`wucrit=0.0`	Width scaling parameter for ucrit.
`wlambda=0.0`	Width scaling parameter for lambda.
`wetad=0.0`	Width scaling parameter for etad.
`we0=0.0`	Width scaling parameter for e0.
`we1=0.0`	Width scaling parameter for e1.

© 2023 Cadence Design Systems, Inc.

`wrlx=0.0`	Width scaling parameter for rlx.
`wucex=0.0`	Width scaling parameter for ucex.
`wdphiedge=0.0`	Width scaling parameter for dphiedge.
`wldphiedge=0.0`	Fine tuning scaling for combined short and narrow devices for dphiedge.
`wldgammaedge=0.0`	Fine tuning scaling for combined short and narrow devices for dgammaedge.
`wedge=0.0`	Total effective width of edge device for edge conductance effect.
`dgammaedge=0.0`	Differential gamma parameter of edge device with respect to the main device.
`dphiedge=0.0`	Differential phi parameter of edge device with respect to the main device.
`saref=0.0`	Reference sa parameter for sti stress effect parameter extraction.
`sbref=0.0`	Reference sb parameter for sti stress effect parameter extraction.
`wlod=0.0`	Width effective parameter for sti stress effect.
`kkp=0.0`	Mobility parameter for sti stress effect.
`lkkp=0.0`	Length scaling of mobility for sti stress effect.
`wkkp=0.0`	Width scaling of mobility for sti stress effect.
`pkkp=0.0`	Area scaling of mobility for sti stress effect.
`tkkp=0.0`	Temperature scaling of mobility for sti stress effect.
`llodkkp=1.0`	Exponential length scaling parameter of mobility for sti stress effect.
`wlodkkp=1.0`	Exponential width scaling parameter of mobility for sti stress effect.
`kvto=0.0`	Threshold voltage parameter for sti stress effect.
`lkvto=0.0`	Length scaling of threshold voltage for sti stress effect.
`wkvto=0.0`	Width scaling of threshold voltage for sti stress effect.
`pkvto=0.0`	Area scaling of threshold voltage for sti stress effect.

© 2023 Cadence Design Systems, Inc.

`llodkvto=1.0`	Exponential length scaling parameter of threshold voltage for sti stress effect.
`wlodkvto=1.0`	Exponential width scaling parameter of threshold voltage for sti stress effect.
`kgamma=0.0`	Body effect coefficient parameter for sti stress effect.
`lodkgamma=1.0`	Fine tuning parameter for body effect coefficient scaling of sti stress effect.
`ketad=0.0`	Dibl effect parameter for sti stress effect.
`lodketad=1.0`	Fine tuning parameter for dibl effect parameter scaling of sti stress effect.
`kucrit=0.0`	Critical velocity of velocity saturation effect parameter for sti stress effect.
`tcv=600.0E-6`	Temperature scaling of threshold voltage.
`bex=(-1.5)`	Temperature scaling of mobility.
`te0ex=0.5`	Temperature scaling of e0.
`te1ex=0.5`	Temperature scaling of e1.
`teta=(-0.9E-3)`	Temperature scaling of eta parameter.
`ucex=1.5`	Temperature scaling of critical velocity of velocity saturation effect.
`tlambda=0.0`	Temperature scaling of lambda parameter.
`ibbt=800.0E-6`	Temperature scaling of ibb.
`tcvl=0.0`	Length scaling of tcv.
`tcvw=0.0`	Width scaling of tcv.
`tcvwl=0.0`	Area scaling of tcv.
`gammaov=1.6`	Body effect coefficient of the gate overlap region.
`gammagov=10.0`	Gate doping coefficient for polysilicon depletion effect of the gate overlap region.
`vfbov=0.0`	Flat-band voltage of the gate overlap region.
`lov=20.0E-9`	Effective length of the gate overlap region.
`vov=1.0`	Bias parameter of the overlap capacitances.

© 2023 Cadence Design Systems, Inc.

`cgso=0.0`	Bias-independent overlap capacitance per gate width unit between gate and source.
`cgdo=0.0`	Bias-independent overlap capacitance per gate width unit between gate and drain.
`cgbo=0.0`	Bias-independent overlap capacitance per gate length unit between gate and bulk.
`kjf=0.0`	Fringing capacitance parameter.
`cjf=0.0`	Bias scaling of fringing capacitance.
`vfr=0.0`	Built-in voltage fine tuning for fringing capacitance model.
`dfr=1.0E-3`	Smooth parameter of fringing capacitance model.
`hdif=0.0e-6`	Half length of the active area.
`rsh=0.0`	Square resistance of active area.
`ldif=0.0`	Distance between the middle of the active area and the start of the channel.
`rs=0.0`	Ldd source series resistance.
`rd=0.0`	Ldd drain series resistance.
`rlx=(-1.0)`	External series resistance per width unit.
`rsx=(-1.0)`	External series resistance per width unit, source side (asymmetric model).
`rdx=(-1.0)`	External series resistance per width unit, drain side (asymmetric model).
`tr=0.0`	First order resistance temperature scaling parameter.
`tr2=0.0`	Second order resistance temperature scaling parameter.
`gmin=0.0`	Minimum conductance of junction diodes.
`njs=1.0`	Slope factor for junction diode, source side (asymmetrical model).
`xjbvs=0.0`	Break-down effect coefficient for junction diode, source side (asymmetrical model).
`bvs=10.0`	Break-down voltage for junction diode, source side (asymmetrical model).
`jss=0.0E-09`	Area component of current for junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`jssws=0.0E-12`	Sideways component of current for junction diode, source side (asymmetrical model).
`jsswgs=0.0E-12`	Gate-side component of current for junction diode, source side (asymmetrical model).
`jtss=0.0E-09`	Area component of trap-assisted current for junction diode, source side (asymmetrical model).
`jtssws=0.0E-12`	Sideways component of trap-assisted current for junction diode, source side (asymmetrical model).
`jtsswgs=0.0E-12`	Gateside component of trap-assisted current for junction diode, source side (asymmetrical model).
`njtss=1.0`	Area slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`njtssws=1.0`	Sideways slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`njtsswgs=1.0`	Gateside slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`vtss=0.0`	Area voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
`vtssws=0.0`	Sideways voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
`vtsswgs=0.0`	Gateside voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
`cjs=0.0E-06`	Area component of capacitance for junction diode, source side (asymmetrical model).
`cjsws=0.0E-09`	Sideways component of capacitance for junction diode, source side (asymmetrical model).
`cjswgs=0.0E-09`	Gateside component of capacitance for junction diode, source side (asymmetrical model).
`pbs=0.800`	Area parameter of capacitance for junction diode, source side (asymmetrical model).
`pbsws=0.600`	Sideways parameter of capacitance for junction diode, source side (asymmetrical model).
`pbswgs=0.600`	Gateside parameter of capacitance for junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`mjs=0.900`	Area exponent of capacitance for junction diode, source side (asymmetrical model).
`mjsws=0.700`	Sideways exponent of capacitance for junction diode, source side (asymmetrical model).
`mjswgs=0.700`	Gateside exponent of capacitance for junction diode, source side (asymmetrical model).
`xtis=3.0`	Temperature dependence for junction diode, source side (asymmetrical model).
`xtss=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtssws=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtsswgs=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`tnjtss=0.0`	Temperature dependence of njtss (area), junction diode, source side (asymmetrical model).
`tnjtssws=0.0`	Temperature dependence of njtssws (sideways), junction diode, source side (asymmetrical model).
`tnjtsswgs=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, source side (asymmetrical model).
`tcj=0.0`	Temperature dependence of area component of capacitance for junction diodes (cjs and cjd), both (source and drain) sides (asymmetrical model).
`tcjsw=0.0`	Temperature dependence of sideways component of capacitance for junction diodes (cjsws and cjswd), both (source and drain) sides (asymmetrical model).
`tcjswg=0.0`	Temperature dependence of gateside component of capacitance for junction diodes (cjswgs and cjswgd), both (source and drain) sides (asymmetrical model).
`tpb=0.0`	Temperature dependence of area parameter of capacitance for junction diodes (pbs and pbd), both (source and drain) sides (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`tpbsw=0.0`	Temperature dependence of sideways parameter of capacitance for junction diodes (pbsws and pbswd), both (source and drain) sides (asymmetrical model).
`tpbswg=0.0`	Temperature dependence of gateside parameter of capacitance for junction diodes (pbswgs and pbswgd), both (source and drain) sides (asymmetrical model).
`njd=1.0`	Slope factor for junction diode, drain side (asymmetrical model).
`xjbvd=0.0`	Break-down effect coefficient for junction diode, drain side (asymmetrical model).
`bvd=10.0`	Break-down voltage for junction diode, drain side (asymmetrical model).
`jsd=0.0E-09`	Area component of current for junction diode, drain side (asymmetrical model).
`jsswd=0.0E-12`	Sideways component of current for junction diode, drain side (asymmetrical model).
`jsswgd=0.0E-12`	Gate-side component of current for junction diode, drain side (asymmetrical model).
`jtsd=0.0E-09`	Area component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswd=0.0E-12`	Sideways component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswgd=0.0E-12`	Gateside component of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsd=1.0`	Area slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswd=1.0`	Sideways slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswgd=1.0`	Gateside slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsd=0.0`	Area voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsswd=0.0`	Sideways voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`vtsswgd=0.0`	Gateside voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`cjd=0.0E-06`	Area component of capacitance for junction diode, drain side (asymmetrical model).
`cjswd=0.0E-09`	Sideways component of capacitance for junction diode, drain side (asymmetrical model).
`cjswgd=0.0E-09`	Gateside component of capacitance for junction diode, drain side (asymmetrical model).
`pbd=0.800`	Area parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswd=0.600`	Sideways parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswgd=0.600`	Gateside parameter of capacitance for junction diode, drain side (asymmetrical model).
`mjd=0.900`	Area exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswd=0.700`	Sideways exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswgd=0.700`	Gateside exponent of capacitance for junction diode, drain side (asymmetrical model).
`xtid=3.0`	Temperature dependence for junction diode, drain side (asymmetrical model).
`xtsd=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`xtsswd=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`xtsswgd=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`tnjtsd=0.0`	Temperature dependence of njtss (area), junction diode, drain side (asymmetrical model).
`tnjtsswd=0.0`	Temperature dependence of njtssws (sideways), junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`tnjtsswgd=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, drain side (asymmetrical model).
`rgsh=3.0`	Gate sheet resistance.
`gc=1`	Type of gate contacts (gc = 1: single sided, gc = 2: both sides).
`krgl1=0.0`	Gate resistance length scaling parameter.
`rdsbsh=1.0E+3`	Substrate network sheet resistance between internal drain and source nodes (used at rf and nqs modes).
`rbwsh=3.0E-3`	Substrate network bulk resistance per width unit between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rbn=0.0`	Substrate network bulk resistance per finger between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rsbwsh=1.0E-3`	Substrate network resistance per width unit between internal source and external bulk nodes (used at rf and nqs modes).
`rsbn=0.0`	Substrate network resistance per finger between internal source and external bulk nodes (used at rf and nqs modes).
`rdbwsh=1.0E-3`	Substrate network resistance per width unit between internal drain and external bulk nodes (used at rf and nqs modes).
`rdbn=0.0`	Substrate network resistance per finger between internal drain and external bulk nodes (used at rf and nqs modes).
`ringtype=1.0`	Ringtype, shape of bulk connector (ringtype = 1 for horse-shoe, three sides contact, ringtype = 2 for symmetric, two sides contact), (used at rf4, rf and nqs modes).

Operating-Point Parameters

`meff`	Effective multiplicity factor (m-factor).

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`vs (V)`	Vs.
`vd (V)`	Vd.
`vg (V)`	Vg.
`vb (V)`	Vb.
`vds (V)`	Vds.
`vgs (V)`	Vgs.
`vbs (V)`	Vbs.
`vdb (V)`	Vdb.
`vgb (V)`	Vgb.
`beta (A/V`^{2}`)`	Beta.
`idsi (A)`	Intrinsic current.
`idsedge (A)`	Edge effect current.
`idex (A)`	Extrinsic current drain side.
`isex (A)`	Extrinsic current source side.
`igex (A)`	Extrinsic current gate side.
`ibex (A)`	Extrinsic current bulk side.
`n`	Slope factor n.
`vp`	Pinch-off voltage.
`vod (V)`	Overdrive voltage n*(vp-vs).
`vdsat (V)`	Saturation voltage.
`sat (s)`	Saturation flag.
`vth (V)`	Effective threshold voltage vth.
`vtb (V)`	Effective threshold voltage vtb.
`weffnf (m)`	Effective total width.
`weff (m)`	Effective finger width.
`leff (m)`	Effective length.
`op_nf`	Number of fingers.

© 2023 Cadence Design Systems, Inc.

ic	Inversion coefficient.
ispec (A)	Specific current.
gmgi (S)	Intrinsic gate tranconductance.
gmsi (S)	Intrinsic source tranconductance.
gmdi (S)	Intrinsic drain tranconductance.
gmbi (S)	Intrinsic bulk tranconductance.
gmgex (S)	Extrinsic gate tranconductance.
gmsex (S)	Extrinsic source tranconductance.
gmdex (S)	Extrinsic drain tranconductance.
gds (S)	Extrinsic drain tranconductance, alias to Gmdex.
gmbex (S)	Extrinsic bulk tranconductance.
gmgutid	Gmg*ut/ids.
gmsutid	Gms*ut/ids.
gmdutid	Gmd*ut/ids.
gmbutid	Gmb*ut/ids.
avi	Intrinsic gain.
gmgid (1/V)	Gm/ids.
vm (V)	Early voltage ids/gds.
ft (Hz)	Transit frequency.
tau0 (s)	Tau0.
tau (s)	Nqs time constant.
cggi (F)	Cggi.
cgsi (F)	Cgsi.
cgdi (F)	Cgdi.
cgbi (F)	Cgbi.
csgi (F)	Csgi.
csdi (F)	Csdi.
csbi (F)	Csbi.
cssi (F)	Cssi.

© 2023 Cadence Design Systems, Inc.

`cdgi (F)`	Cdgi.
`cddi (F)`	Cddi.
`cdbi (F)`	Cdbi.
`cdsi (F)`	Cdsi.
`cbgi (F)`	Cbgi.
`cbdi (F)`	Cbdi.
`cbbi (F)`	Cbbi.
`cbsi (F)`	Cbsi.
`cgsex (F)`	Extrinsic gate-source capacitance.
`cgdex (F)`	Extrinsic gate-drain capacitance.
`cgbex (F)`	Extrinsic gate-bulk capacitance.
`ctotex (F)`	Total extrinsic capacitance.
`cgsov (F)`	Cgsov.
`cgdov (F)`	Cgdov.
`sid_flicker (`A^2`/Hz)`	Flicker noise psd sdid @ 1hz.
`sid_thermal (`A^2`/Hz)`	Thermal noise psd sdid.
`svg_flicker (`V^2`/Hz)`	Flicker noise psd sdvg @ 1hz.
`svg_thermal (`V^2`/Hz)`	Thermal noise psd sdvg.
`sigmadidoid`	Relative current mismatch.
`sigmavg (V)`	Gate voltage offset.
`i0 (V)`	Technology current.
`qs (C)`	Source charge.
`qd (C)`	Drain charge.
`qg (C)`	Gate charge.
`qb (C)`	Bulk charge.

© 2023 Cadence Design Systems, Inc.

`ids (A)`	Resistive drain-to-source current.
`idb (A)`	Impact ionization current.
`qsedge (C)`	Edge charge.
`qdedge (C)`	Edge charge.
`qgedge (C)`	Edge charge.
`qbedge (C)`	Edge charge.
`qsov (C)`	Source side overlap charge.
`qdov (C)`	Drain sie overlap charge.
`qsfr (C)`	Source side fringing charge.
`qdfr (C)`	Drain side fringing charge.
`igidl (A)`	Gate induced drain current.
`igisl (A)`	Gate induced source current.
`igb (A)`	Gate current (bulk).
`igd (A)`	Gate current (drain).
`igs (A)`	Gate current (source).
`igdov (A)`	Overlap gate current (drain).
`igsov (A)`	Overlap gate current (source).
`region`	Estimated operating region. Spectre a outputs number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`pwr (W)`	Power dissipation.

Related Topics

EKV3 MOSFET Model (ekv3)

Device ekv3_r4 (ekv3_r4)

Device ekv3_rf (ekv3_rf)

Device ekv3_s (ekv3_s)

© 2023 Cadence Design Systems, Inc.

Device ekv3_r4 (ekv3_r4)

This device is supported within altergroups.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Model Syntax

```
model modelName ekv3_r4 parameter=value ...
```

Instance Parameters

`l=10.0E-06`	Gate's length.
`w=10.0E-06`	Gate's width.
`nf=1`	Number of fingers.
`m=1`	Number of devices in parallel.
`ad=0.0`	Drain's area.
`as=0.0`	Source's area.
`pd=0.0`	Drain's perimeter.
`ps=0.0`	Source's perimeter.
`sa=0.0`	Sti parameter; distance from sti (side a).
`sb=0.0`	Sti parameter; distance from sti (side b).
`sd=0.0`	Sti parameter; distance between gates.
`trise=0.0`	Temperature change for particular transistor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Parameters

`version=301.02`	Parameter for version control. Valid values are 301.02 and 302.00. The default version is 301.02.

© 2023 Cadence Design Systems, Inc.

sign=1	Sign = 1 for nmos; sign = -1 for pmos.
tg=(-1)	Type of gate: -1 enhancement type; 1 depletion type.
tnom=27.0	Nominal temperature for model parameters.
scale=1.0	Scaling size factor.
xl=0.0	Optical offset for channel length.
xw=0.0	Optical offset for channel width.
nqs_noi=1.0	Flag turning on nqs thermal noise model. (At a time, only one of nqs_noi and th_noi should be set to 1.
th_noi=0.0	Flag turning on short channel effects thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1..
info_level=0.0	Flag for information printout. currently only value of 1 is supported.
qoff=0.0	Flag for turning off the dynamic behavior of the model (for debugging purposes).
avto=0.0	Matching parameter for threshold voltage (vto).
agamma=0.0	Matching parameter for body factor (gamma).
akp=0.0	Matching parameter for mobility (kp).
cox=0.012	Oxide capacitance per unit area.
xj=20.0E-09	Depth of junction (source and drain).
vto=0.3	Threshold voltage.
phif=0.45	Fermi bulk potential.
gamma=0.3	Body effect coefficient.
gammag=4.1	Gate doping coefficient for polysilicon depletion effect.
n0=1.0	Weak inversion fine tuning parameter.
vbi=0.0	Built-in voltage drop-off. if left to default zero value, it is set to the nominal value of 3ut higher than phi..
aqma=0.5	Quantum mechanical effect accumulation region coefficient.
aqmi=0.4	Quantum mechanical effect inversion region coefficient.

© 2023 Cadence Design Systems, Inc.

`etaqm=0.75`	Quantum mechanical effect accumulation eta parameter.
`kp=500.0E-06`	Mobility (multiplied by cox) parameter.
`e0=1.0E+10`	First order parameter for mobility reduction due to vertical field effect.
`e1=3.1E+08`	Second order parameter for mobility reduction due to vertical field effect.
`eta=0.5`	Inversion charge coefficient for vertical field calculation.
`thc=0.0`	Coulomb scattering parameter.
`zc=1.0E-6`	Coulomb scattering inversion charge coefficient.
`la=1.0`	Critical length a of mobility length scaling.
`lb=1.0`	Critical length b of mobility length scaling.
`ka=0.0`	Parameter for critical length a of mobility length scaling.
`kb=0.0`	Parameter for critical length b of mobility length scaling.
`wkp1=1.0E-6`	Critical width of mobility width scaling.
`wkp2=0.0`	Amplitude parameter for mobility width scaling.
`wkp3=1.0`	Span parameter for mobility width scaling.
`dl=(-10.0E-9)`	Effective length parameter.
`dlc=0.0`	Effective length parameter for dynamic behavior.
`dw=(-10.0E-9)`	Effective width parameter.
`dwc=0.0`	Effective width parameter for dynamic behavior.
`wdl=0.0`	Effective length parameter for narrow channel devices.
`ldw=0.0`	Effective width parameter for short channel devices.
`ll=0.0`	Base of exponential model for effective length.
`lln=1.0`	Exponent of exponential model for effective length.
`avt=0.0`	Parameter for long and wide channel vto correction.
`lvt=1.0`	Length for long and wide channel vto correction.
`wvt=1.0`	Width for long and wide channel vto correction.

© 2023 Cadence Design Systems, Inc.

agam=0.0	Parameter for long and wide channel gamma correction.
lgam=1.0	Length for long and wide channel gamma correction.
wgam=1.0	Width for long and wide channel gamma correction.
nfvta=0.0	Number of fingers for vto correction for multifinger devices (obsolete model by sti stress effect).
nfvtb=10000.0	Parameter for vto correction for multifinger devices (obsolete model by sti stress effect).
ucrit=5.0E+06	Critical velocity of velocity saturation effect.
delta=2.0	Variable order (from 1.0 to 2.0) of velocity saturation effect.
lambda=0.5	Length parameter for channel length modulation.
aclm=0.83	Fine tuning parameter for channel length modulation.
lr=50.0E-09	Length parameter for reverse short channel effect.
qlr=0.5E-3	Charge parameter for reverse short channel effect (vto).
nlr=10.0E-3	Doping parameter for reverse short channel effect (gamma).
flr=1.0	Fermi potential fine tuning parameter for reverse short channel effect (phif).
leta0=0.0	Length independent parameter for charge sharing (long channel).
leta=500.0E-3	Length scaling parameter for charge sharing.
leta2=0.0	Second order length scaling parameter for charge sharing (shortest channel).
weta=200.0E-3	Width scaling parameter for charge sharing.
ncs=1.0	Weak inversion slope parameter for charge sharing.
etad=1.0	Eta parameter for drain induced barrier lowering.
sigmad=1.0	Sigma parameter for drain induced barrier lowering.
wr=90.0E-09	Width parameter for inverse narrow channel effect.
qwr=0.3E-3	Charge parameter for inverse narrow channel effect (vto).

© 2023 Cadence Design Systems, Inc.

`nwr=5.0E-3`	Doping parameter for inverse narrow channel effect (gamma).
`fprout=1.0E6`	Output resistance parameter for drain induced threshold shift.
`pdits=0.0`	Parameter for drain induced threshold shift (if set to zero the dits effect is disabled).
`pditsl=0.0`	Length scaling parameter for drain induced threshold shift.
`pditsd=1.0`	Bias parameter for drain induced threshold shift.
`ddits=0.3`	Smooth factor of output conductance for drain induced threshold shift.
`iba=000.0E+06`	Parameter a of impact ionization current.
`ibb=300.0E+06`	Parameter b of impact ionization current.
`ibn=1.0`	Parameter n of impact ionization current.
`xb=3.1`	Silicon to silicon oxide tunneling barrier height.
`eb=29.0E+09`	Characteristic electrical field.
`kg=00.0E-6`	Mobility for gate current.
`lovig=20.0E-9`	Overlap gate length for overlap gate current.
`agidl=0.0`	Parameter a of gate induced drain leakage.
`bgidl=2.3E+09`	Parameter b of gate induced drain leakage.
`cgidl=0.5`	Parameter c of gate induced drain leakage.
`egidl=0.8`	Parameter e of gate induced drain leakage.
`lfnoi=0`	Flicker noise model selection.
`kf=0.0`	Flicker noise parameter.
`af=1.0`	Flicker noise frequency exponent.
`ef=2.0`	Flicker noise transconductance exponent.
`nt=1.0E+14`	Number of trapped carriers.
`alphac=10.0E+4`	Coulomb scattering coefficient.
`alphah=1.0E-20`	Hooge parameter for mobility fluctuation noise model.
`kgfn=0.0`	Gate flicker noise parameter.

© 2023 Cadence Design Systems, Inc.

`ecn=1.0E+4`	Critical field value.
`sdr=1.0E-6`	Series resistance noise parameter.
`lwr=0.0`	Length scaling parameter for wr.
`lqwr=0.0`	Length scaling parameter for qwr.
`lnwr=0.0`	Length scaling parameter for nwr.
`ldphiedge=0.0`	Length scaling parameter for dphiedge.
`wlr=0.0`	Width scaling parameter for lr.
`wqlr=0.0`	Width scaling parameter for qlr.
`wnlr=0.0`	Width scaling parameter for nlr.
`wucrit=0.0`	Width scaling parameter for ucrit.
`wlambda=0.0`	Width scaling parameter for lambda.
`wetad=0.0`	Width scaling parameter for etad.
`we0=0.0`	Width scaling parameter for e0.
`we1=0.0`	Width scaling parameter for e1.
`wrlx=0.0`	Width scaling parameter for rlx.
`wucex=0.0`	Width scaling parameter for ucex.
`wdphiedge=0.0`	Width scaling parameter for dphiedge.
`wldphiedge=0.0`	Fine tuning scaling for combined short and narrow devices for dphiedge.
`wldgammaedge=0.0`	Fine tuning scaling for combined short and narrow devices for dgammaedge.
`wedge=0.0`	Total effective width of edge device for edge conductance effect.
`dgammaedge=0.0`	Differential gamma parameter of edge device with respect to the main device.
`dphiedge=0.0`	Differential phi parameter of edge device with respect to the main device.
`saref=0.0`	Reference sa parameter for sti stress effect parameter extraction.
`sbref=0.0`	Reference sb parameter for sti stress effect parameter extraction.

© 2023 Cadence Design Systems, Inc.

`wlod=0.0`	Width effective parameter for sti stress effect.
`kkp=0.0`	Mobility parameter for sti stress effect.
`lkkp=0.0`	Length scaling of mobility for sti stress effect.
`wkkp=0.0`	Width scaling of mobility for sti stress effect.
`pkkp=0.0`	Area scaling of mobility for sti stress effect.
`tkkp=0.0`	Temperature scaling of mobility for sti stress effect.
`llodkkp=1.0`	Exponential length scaling parameter of mobility for sti stress effect.
`wlodkkp=1.0`	Exponential width scaling parameter of mobility for sti stress effect.
`kvto=0.0`	Threshold voltage parameter for sti stress effect.
`lkvto=0.0`	Length scaling of threshold voltage for sti stress effect.
`wkvto=0.0`	Width scaling of threshold voltage for sti stress effect.
`pkvto=0.0`	Area scaling of threshold voltage for sti stress effect.
`llodkvto=1.0`	Exponential length scaling parameter of threshold voltage for sti stress effect.
`wlodkvto=1.0`	Exponential width scaling parameter of threshold voltage for sti stress effect.
`kgamma=0.0`	Body effect coefficient parameter for sti stress effect.
`lodkgamma=1.0`	Fine tuning parameter for body effect coefficient scaling of sti stress effect.
`ketad=0.0`	Dibl effect parameter for sti stress effect.
`lodketad=1.0`	Fine tuning parameter for dibl effect parameter scaling of sti stress effect.
`kucrit=0.0`	Critical velocity of velocity saturation effect parameter for sti stress effect.
`tcv=600.0E-6`	Temperature scaling of threshold voltage.
`bex=(-1.5)`	Temperature scaling of mobility.
`te0ex=0.5`	Temperature scaling of e0.
`te1ex=0.5`	Temperature scaling of e1.
`teta=(-0.9E-3)`	Temperature scaling of eta parameter.

© 2023 Cadence Design Systems, Inc.

`ucex=1.5`	Temperature scaling of critical velocity of velocity saturation effect.
`tlambda=0.0`	Temperature scaling of lambda parameter.
`ibbt=800.0E-6`	Temperature scaling of ibb.
`tcvl=0.0`	Length scaling of tcv.
`tcvw=0.0`	Width scaling of tcv.
`tcvwl=0.0`	Area scaling of tcv.
`gammaov=1.6`	Body effect coefficient of the gate overlap region.
`gammagov=10.0`	Gate doping coefficient for polysilicon depletion effect of the gate overlap region.
`vfbov=0.0`	Flat-band voltage of the gate overlap region.
`lov=20.0E-9`	Effective length of the gate overlap region.
`vov=1.0`	Bias parameter of the overlap capacitances.
`cgso=0.0`	Bias-independent overlap capacitance per gate width unit between gate and source.
`cgdo=0.0`	Bias-independent overlap capacitance per gate width unit between gate and drain.
`cgbo=0.0`	Bias-independent overlap capacitance per gate length unit between gate and bulk.
`kjf=0.0`	Fringing capacitance parameter.
`cjf=0.0`	Bias scaling of fringing capacitance.
`vfr=0.0`	Built-in voltage fine tuning for fringing capacitance model.
`dfr=1.0E-3`	Smooth parameter of fringing capacitance model.
`hdif=0.0e-6`	Half length of the active area.
`rsh=0.0`	Square resistance of active area.
`ldif=0.0`	Distance between the middle of the active area and the start of the channel.
`rs=0.0`	Ldd source series resistance.
`rd=0.0`	Ldd drain series resistance.
`rlx=(-1.0)`	External series resistance per width unit.

© 2023 Cadence Design Systems, Inc.

`rsx=(-1.0)`	External series resistance per width unit, source side (asymmetric model).
`rdx=(-1.0)`	External series resistance per width unit, drain side (asymmetric model).
`tr=0.0`	First order resistance temperature scaling parameter.
`tr2=0.0`	Second order resistance temperature scaling parameter.
`gmin=0.0`	Minimum conductance of junction diodes.
`njs=1.0`	Slope factor for junction diode, source side (asymmetrical model).
`xjbvs=0.0`	Break-down effect coefficient for junction diode, source side (asymmetrical model).
`bvs=10.0`	Break-down voltage for junction diode, source side (asymmetrical model).
`jss=0.0E-09`	Area component of current for junction diode, source side (asymmetrical model).
`jsswswgs=0.0E-12`	Sideways component of current for junction diode, source side (asymmetrical model).
`jsswgs=0.0E-12`	Gate-side component of current for junction diode, source side (asymmetrical model).
`jtss=0.0E-09`	Area component of trap-assisted current for junction diode, source side (asymmetrical model).
`jtsswswgs=0.0E-12`	Sideways component of trap-assisted current for junction diode, source side (asymmetrical model).
`jtsswgs=0.0E-12`	Gateside component of trap-assisted current for junction diode, source side (asymmetrical model).
`njtss=1.0`	Area slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`njtsswswgs=1.0`	Sideways slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`njtsswgs=1.0`	Gateside slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
`vtss=0.0`	Area voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`vtssws=0.0`	Sideways voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
`vtsswgs=0.0`	Gateside voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
`cjs=0.0E-06`	Area component of capacitance for junction diode, source side (asymmetrical model).
`cjsws=0.0E-09`	Sideways component of capacitance for junction diode, source side (asymmetrical model).
`cjswgs=0.0E-09`	Gateside component of capacitance for junction diode, source side (asymmetrical model).
`pbs=0.800`	Area parameter of capacitance for junction diode, source side (asymmetrical model).
`pbsws=0.600`	Sideways parameter of capacitance for junction diode, source side (asymmetrical model).
`pbswgs=0.600`	Gateside parameter of capacitance for junction diode, source side (asymmetrical model).
`mjs=0.900`	Area exponent of capacitance for junction diode, source side (asymmetrical model).
`mjsws=0.700`	Sideways exponent of capacitance for junction diode, source side (asymmetrical model).
`mjswgs=0.700`	Gateside exponent of capacitance for junction diode, source side (asymmetrical model).
`xtis=3.0`	Temperature dependence for junction diode, source side (asymmetrical model).
`xtss=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtssws=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtsswgs=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`tnjtss=0.0`	Temperature dependence of njtss (area), junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`tnjtsswsw=0.0`	Temperature dependence of njtsswsw (sideways), junction diode, source side (asymmetrical model).
`tnjtsswgs=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, source side (asymmetrical model).
`tcj=0.0`	Temperature dependence of area component of capacitance for junction diodes (cjs and cjd), both (source and drain) sides (asymmetrical model).
`tcjsw=0.0`	Temperature dependence of sideways component of capacitance for junction diodes (cjsws and cjswd), both (source and drain) sides (asymmetrical model).
`tcjswg=0.0`	Temperature dependence of gateside component of capacitance for junction diodes (cjswgs and cjswgd), both (source and drain) sides (asymmetrical model).
`tpb=0.0`	Temperature dependence of area parameter of capacitance for junction diodes (pbs and pbd), both (source and drain) sides (asymmetrical model).
`tpbsw=0.0`	Temperature dependence of sideways parameter of capacitance for junction diodes (pbsws and pbswd), both (source and drain) sides (asymmetrical model).
`tpbswg=0.0`	Temperature dependence of gateside parameter of capacitance for junction diodes (pbswgs and pbswgd), both (source and drain) sides (asymmetrical model).
`njd=1.0`	Slope factor for junction diode, drain side (asymmetrical model).
`xjbvd=0.0`	Break-down effect coefficient for junction diode, drain side (asymmetrical model).
`bvd=10.0`	Break-down voltage for junction diode, drain side (asymmetrical model).
`jsd=0.0E-09`	Area component of current for junction diode, drain side (asymmetrical model).
`jsswd=0.0E-12`	Sideways component of current for junction diode, drain side (asymmetrical model).
`jsswgd=0.0E-12`	Gate-side component of current for junction diode, drain side (asymmetrical model).
`jtsd=0.0E-09`	Area component of trap-assisted current for junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`jtsswd=0.0E-12`	Sideways component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswgd=0.0E-12`	Gateside component of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsd=1.0`	Area slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswd=1.0`	Sideways slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswgd=1.0`	Gateside slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsd=0.0`	Area voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsswd=0.0`	Sideways voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsswgd=0.0`	Gateside voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`cjd=0.0E-06`	Area component of capacitance for junction diode, drain side (asymmetrical model).
`cjswd=0.0E-09`	Sideways component of capacitance for junction diode, drain side (asymmetrical model).
`cjswgd=0.0E-09`	Gateside component of capacitance for junction diode, drain side (asymmetrical model).
`pbd=0.800`	Area parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswd=0.600`	Sideways parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswgd=0.600`	Gateside parameter of capacitance for junction diode, drain side (asymmetrical model).
`mjd=0.900`	Area exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswd=0.700`	Sideways exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswgd=0.700`	Gateside exponent of capacitance for junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`xtid=3.0`	Temperature dependence for junction diode, drain side (asymmetrical model).
`xtsd=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`xtsswd=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`xtsswgd=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`tnjtsd=0.0`	Temperature dependence of njtss (area), junction diode, drain side (asymmetrical model).
`tnjtsswd=0.0`	Temperature dependence of njtssws (sideways), junction diode, drain side (asymmetrical model).
`tnjtsswgd=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, drain side (asymmetrical model).
`rgsh=3.0`	Gate sheet resistance.
`gc=1`	Type of gate contacts (gc = 1: single sided, gc = 2: both sides).
`krgl1=0.0`	Gate resistance length scaling parameter.
`rdsbsh=1.0E+3`	Substrate network sheet resistance between internal drain and source nodes (used at rf and nqs modes).
`rbwsh=3.0E-3`	Substrate network bulk resistance per width unit between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rbn=0.0`	Substrate network bulk resistance per finger between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rsbwsh=1.0E-3`	Substrate network resistance per width unit between internal source and external bulk nodes (used at rf and nqs modes).
`rsbn=0.0`	Substrate network resistance per finger between internal source and external bulk nodes (used at rf and nqs modes).

© 2023 Cadence Design Systems, Inc.

`rdbwsh=1.0E-3`	Substrate network resistance per width unit between internal drain and external bulk nodes (used at rf and nqs modes).
`rdbn=0.0`	Substrate network resistance per finger between internal drain and external bulk nodes (used at rf and nqs modes).
`ringtype=1.0`	Ringtype, shape of bulk connector (ringtype = 1 for horse-shoe, three sides contact, ringtype = 2 for symmetric, two sides contact), (used at rf4, rf and nqs modes).

Output Parameters

`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`vs (V)`	Vs.
`vd (V)`	Vd.
`vg (V)`	Vg.
`vb (V)`	Vb.
`vds (V)`	Vds.
`vgs (V)`	Vgs.
`vbs (V)`	Vbs.
`vdb (V)`	Vdb.
`vgb (V)`	Vgb.
`beta (A/V`^{2}`)`	Beta.
`idsi (A)`	Intrinsic current.
`idsedge (A)`	Edge effect current.
`idex (A)`	Extrinsic current drain side.
`isex (A)`	Extrinsic current source side.
`igex (A)`	Extrinsic current gate side.

© 2023 Cadence Design Systems, Inc.

ibex (A)	Extrinsic current bulk side.
n	Slope factor n.
vp	Pinch-off voltage.
vod (V)	Overdrive voltage n*(vp-vs).
vdsat (V)	Saturation voltage.
sat (s)	Saturation flag.
vth (V)	Effective threshold voltage vth.
vtb (V)	Effective threshold voltage vtb.
weffnf (m)	Effective total width.
weff (m)	Effective finger width.
leff (m)	Effective length.
op_nf	Number of fingers.
ic	Inversion coefficient.
ispec (A)	Specific current.
gmgi (S)	Intrinsic gate tranconductance.
gmsi (S)	Intrinsic source tranconductance.
gmdi (S)	Intrinsic drain tranconductance.
gmbi (S)	Intrinsic bulk tranconductance.
gmgex (S)	Extrinsic gate tranconductance.
gmsex (S)	Extrinsic source tranconductance.
gmdex (S)	Extrinsic drain tranconductance.
gds (S)	Extrinsic drain tranconductance, alias to Gmdex.
gmbex (S)	Extrinsic bulk tranconductance.
gmgutid	Gmg*ut/ids.
gmsutid	Gms*ut/ids.
gmdutid	Gmd*ut/ids.
gmbutid	Gmb*ut/ids.
avi	Intrinsic gain.
gmgid (1/V)	Gm/ids.

© 2023 Cadence Design Systems, Inc.

`vm (V)`	Early voltage ids/gds.
`ft (Hz)`	Transit frequency.
`tau0 (s)`	Tau0.
`tau (s)`	Nqs time constant.
`cggi (F)`	Cggi.
`cgsi (F)`	Cgsi.
`cgdi (F)`	Cgdi.
`cgbi (F)`	Cgbi.
`csgi (F)`	Csgi.
`csdi (F)`	Csdi.
`csbi (F)`	Csbi.
`cssi (F)`	Cssi.
`cdgi (F)`	Cdgi.
`cddi (F)`	Cddi.
`cdbi (F)`	Cdbi.
`cdsi (F)`	Cdsi.
`cbgi (F)`	Cbgi.
`cbdi (F)`	Cbdi.
`cbbi (F)`	Cbbi.
`cbsi (F)`	Cbsi.
`cgsex (F)`	Extrinsic gate-source capacitance.
`cgdex (F)`	Extrinsic gate-drain capacitance.
`cgbex (F)`	Extrinsic gate-bulk capacitance.
`ctotex (F)`	Total extrinsic capacitance.
`cgsov (F)`	Cgsov.
`cgdov (F)`	Cgdov.
`sid_flicker (A`^{2}`/Hz)`	Flicker noise psd sdid @ 1hz.
`sid_thermal (A`^{2}`/Hz)`	

© 2023 Cadence Design Systems, Inc.

	Thermal noise psd sdid.
svg_flicker (V^2/Hz)	
	Flicker noise psd sdvg @ 1hz.
svg_thermal (V^2/Hz)	
	Thermal noise psd sdvg.
sigmadidoid	Relative current mismatch.
sigmavg (V)	Gate voltage offset.
i0 (V)	Technology current.
qs (C)	Source charge.
qd (C)	Drain charge.
qg (C)	Gate charge.
qb (C)	Bulk charge.
ids (A)	Resistive drain-to-source current.
idb (A)	Impact ionization current.
qsedge (C)	Edge charge.
qdedge (C)	Edge charge.
qgedge (C)	Edge charge.
qbedge (C)	Edge charge.
qsov (C)	Source side overlap charge.
qdov (C)	Drain sie overlap charge.
qsfr (C)	Source side fringing charge.
qdfr (C)	Drain side fringing charge.
igidl (A)	Gate induced drain current.
igisl (A)	Gate induced source current.
igb (A)	Gate current (bulk).
igd (A)	Gate current (drain).
igs (A)	Gate current (source).
igdov (A)	Overlap gate current (drain).
igsov (A)	Overlap gate current (source).

© 2023 Cadence Design Systems, Inc.

`region`	Estimated operating region. Spectre outputs a number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`pwr (W)`	Power dissipation

Related Topics

EKV3 MOSFET Model (ekv3)

Device ekv3_nqs (ekv3_nqs)

Device ekv3_rf (ekv3_rf)

Device ekv3_s (ekv3_s)

Device ekv3_rf (ekv3_rf)

Description

ekv3_rf model (compiled=Jun 2 2008 cmi=4.0 developer=admsXml-2.2.7, interface=spectre500 2.1.1, version=unknown)

This device is supported within altergroups.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Model Syntax

```
model modelName ekv3_rf parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`l=10.0E-06`	Gate's length.
`w=10.0E-06`	Gate's width.
`nf=1`	Number of fingers.
`m=1`	Number of devices in parallel.
`ad=0.0`	Drain's area.
`as=0.0`	Source's area.
`pd=0.0`	Drain's perimeter.
`ps=0.0`	Source's perimeter.
`sa=0.0`	Sti parameter; distance from sti (side a).
`sb=0.0`	Sti parameter; distance from sti (side b).
`sd=0.0`	Sti parameter; distance between gates.
`trise=0.0`	Temperature change for particular transistor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Parameters

`version=301.02`	Parameter for version control. Valid values are 301.02 and 302.00. The default version is 301.02.
`sign=1`	Sign = 1 for nmos; sign = -1 for pmos.
`tg=(-1)`	Type of gate: -1 enhancement type; 1 depletion type.
`tnom=27.0`	Nominal temperature for model parameters.
`scale=1.0`	Scaling size factor.
`xl=0.0`	Optical offset for channel length.
`xw=0.0`	Optical offset for channel width.
`nqs_noi=1.0`	Flag turning on nqs thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1.

© 2023 Cadence Design Systems, Inc.

th_noi=0.0	Flag turning on short channel effects thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1.
info_level=0.0	Flag for information printout. currently only value of 1 is supported.
qoff=0.0	Flag for turning off the dynamic behavior of the model (for debugging purposes).
avto=0.0	Matching parameter for threshold voltage (vto).
agamma=0.0	Matching parameter for body factor (gamma).
akp=0.0	Matching parameter for mobility (kp).
cox=0.012	Oxide capacitance per unit area.
xj=20.0E-09	Depth of junction (source and drain).
vto=0.3	Threshold voltage.
phif=0.45	Fermi bulk potential.
gamma=0.3	Body effect coefficient.
gammag=4.1	Gate doping coefficient for polysilicon depletion effect.
n0=1.0	Weak inversion fine tuning parameter.
vbi=0.0	Built-in voltage drop-off. if left to default zero value, it is set to the nominal value of 3ut higher than phi..
aqma=0.5	Quantum mechanical effect accumulation region coefficient.
aqmi=0.4	Quantum mechanical effect inversion region coefficient.
etaqm=0.75	Quantum mechanical effect accumulation eta parameter.
kp=500.0E-06	Mobility (multiplied by cox) parameter.
e0=1.0E+10	First order parameter for mobility reduction due to vertical field effect.
e1=3.1E+08	Second order parameter for mobility reduction due to vertical field effect.
eta=0.5	Inversion charge coefficient for vertical field calculation.

© 2023 Cadence Design Systems, Inc.

`thc=0.0`	Coulomb scattering parameter.
`zc=1.0E-6`	Coulomb scattering inversion charge coefficient.
`la=1.0`	Critical length a of mobility length scaling.
`lb=1.0`	Critical length b of mobility length scaling.
`ka=0.0`	Parameter for critical length a of mobility length scaling.
`kb=0.0`	Parameter for critical length b of mobility length scaling.
`wkp1=1.0E-6`	Critical width of mobility width scaling.
`wkp2=0.0`	Amplitude parameter for mobility width scaling.
`wkp3=1.0`	Span parameter for mobility width scaling.
`dl=(-10.0E-9)`	Effective length parameter.
`dlc=0.0`	Effective length parameter for dynamic behavior.
`dw=(-10.0E-9)`	Effective width parameter.
`dwc=0.0`	Effective width parameter for dynamic behavior.
`wdl=0.0`	Effective length parameter for narrow channel devices.
`ldw=0.0`	Effective width parameter for short channel devices.
`ll=0.0`	Base of exponential model for effective length.
`lln=1.0`	Exponent of exponential model for effective length.
`avt=0.0`	Parameter for long and wide channel vto correction.
`lvt=1.0`	Length for long and wide channel vto correction.
`wvt=1.0`	Width for long and wide channel vto correction.
`agam=0.0`	Parameter for long and wide channel gamma correction.
`lgam=1.0`	Length for long and wide channel gamma correction.
`wgam=1.0`	Width for long and wide channel gamma correction.
`nfvta=0.0`	Number of fingers for vto correction for multifinger devices (obsolete model by sti stress effect).
`nfvtb=10000.0`	Parameter for vto correction for multifinger devices (obsolete model by sti stress effect).

© 2023 Cadence Design Systems, Inc.

`ucrit=5.0E+06`	Critical velocity of velocity saturation effect.
`delta=2.0`	Variable order (from 1.0 to 2.0) of velocity saturation effect.
`lambda=0.5`	Length parameter for channel length modulation.
`aclm=0.83`	Fine tuning parameter for channel length modulation.
`lr=50.0E-09`	Length parameter for reverse short channel effect.
`qlr=0.5E-3`	Charge parameter for reverse short channel effect (vto).
`nlr=10.0E-3`	Doping parameter for reverse short channel effect (gamma).
`flr=1.0`	Fermi potential fine tuning parameter for reverse short channel effect (phif).
`leta0=0.0`	Length independent parameter for charge sharing (long channel).
`leta=500.0E-3`	Length scaling parameter for charge sharing.
`leta2=0.0`	Second order length scaling parameter for charge sharing (shortest channel).
`weta=200.0E-3`	Width scaling parameter for charge sharing.
`ncs=1.0`	Weak inversion slope parameter for charge sharing.
`etad=1.0`	Eta parameter for drain induced barrier lowering.
`sigmad=1.0`	Sigma parameter for drain induced barrier lowering.
`wr=90.0E-09`	Width parameter for inverse narrow channel effect.
`qwr=0.3E-3`	Charge parameter for inverse narrow channel effect (vto).
`nwr=5.0E-3`	Doping parameter for inverse narrow channel effect (gamma).
`fprout=1.0E6`	Output resistance parameter for drain induced threshold shift.
`pdits=0.0`	Parameter for drain induced threshold shift (if set to zero the dits effect is disabled).
`pditsl=0.0`	Length scaling parameter for drain induced threshold shift.

© 2023 Cadence Design Systems, Inc.

pditsd=1.0	Bias parameter for drain induced threshold shift.
ddits=0.3	Smooth factor of output conductance for drain induced threshold shift.
iba=000.0E+06	Parameter a of impact ionization current.
ibb=300.0E+06	Parameter b of impact ionization current.
ibn=1.0	Parameter n of impact ionization current.
xb=3.1	Silicon to silicon oxide tunneling barrier height.
eb=29.0E+09	Characteristic electrical field.
kg=00.0E-6	Mobility for gate current.
lovig=20.0E-9	Overlap gate length for overlap gate current.
agidl=0.0	Parameter a of gate induced drain leakage.
bgidl=2.3E+09	Parameter b of gate induced drain leakage.
cgidl=0.5	Parameter c of gate induced drain leakage.
egidl=0.8	Parameter e of gate induced drain leakage.
lfnoi=0	Flicker noise model selection.
kf=0.0	Flicker noise parameter.
af=1.0	Flicker noise frequency exponent.
ef=2.0	Flicker noise transconductance exponent.
nt=1.0E+14	Number of trapped carriers.
alphac=10.0E+4	Coulomb scattering coefficient.
alphah=1.0E-20	Hooge parameter for mobility fluctuation noise model.
kgfn=0.0	Gate flicker noise parameter.
ecn=1.0E+4	Critical field value.
sdr=1.0E-6	Series resistance noise parameter.
lwr=0.0	Length scaling parameter for wr.
lqwr=0.0	Length scaling parameter for qwr.
lnwr=0.0	Length scaling parameter for nwr.
ldphiedge=0.0	Length scaling parameter for dphiedge.
wlr=0.0	Width scaling parameter for lr.

© 2023 Cadence Design Systems, Inc.

wqlr=0.0	Width scaling parameter for qlr.
wnlr=0.0	Width scaling parameter for nlr.
wucrit=0.0	Width scaling parameter for ucrit.
wlambda=0.0	Width scaling parameter for lambda.
wetad=0.0	Width scaling parameter for etad.
we0=0.0	Width scaling parameter for e0.
we1=0.0	Width scaling parameter for e1.
wrlx=0.0	Width scaling parameter for rlx.
wucex=0.0	Width scaling parameter for ucex.
wdphiedge=0.0	Width scaling parameter for dphiedge.
wldphiedge=0.0	Fine tuning scaling for combined short and narrow devices for dphiedge.
wldgammaedge=0.0	Fine tuning scaling for combined short and narrow devices for dgammaedge.
wedge=0.0	Total effective width of edge device for edge conductance effect.
dgammaedge=0.0	Differential gamma parameter of edge device with respect to the main device.
dphiedge=0.0	Differential phi parameter of edge device with respect to the main device.
saref=0.0	Reference sa parameter for sti stress effect parameter extraction.
sbref=0.0	Reference sb parameter for sti stress effect parameter extraction.
wlod=0.0	Width effective parameter for sti stress effect.
kkp=0.0	Mobility parameter for sti stress effect.
lkkp=0.0	Length scaling of mobility for sti stress effect.
wkkp=0.0	Width scaling of mobility for sti stress effect.
pkkp=0.0	Area scaling of mobility for sti stress effect.
tkkp=0.0	Temperature scaling of mobility for sti stress effect.

© 2023 Cadence Design Systems, Inc.

`llodkkp=1.0`	Exponential length scaling parameter of mobility for sti stress effect.
`wlodkkp=1.0`	Exponential width scaling parameter of mobility for sti stress effect.
`kvto=0.0`	Threshold voltage parameter for sti stress effect.
`lkvto=0.0`	Length scaling of threshold voltage for sti stress effect.
`wkvto=0.0`	Width scaling of threshold voltage for sti stress effect.
`pkvto=0.0`	Area scaling of threshold voltage for sti stress effect.
`llodkvto=1.0`	Exponential length scaling parameter of threshold voltage for sti stress effect.
`wlodkvto=1.0`	Exponential width scaling parameter of threshold voltage for sti stress effect.
`kgamma=0.0`	Body effect coefficient parameter for sti stress effect.
`lodkgamma=1.0`	Fine tuning parameter for body effect coefficient scaling of sti stress effect.
`ketad=0.0`	Dibl effect parameter for sti stress effect.
`lodketad=1.0`	Fine tuning parameter for dibl effect parameter scaling of sti stress effect.
`kucrit=0.0`	Critical velocity of velocity saturation effect parameter for sti stress effect.
`tcv=600.0E-6`	Temperature scaling of threshold voltage.
`bex=(-1.5)`	Temperature scaling of mobility.
`te0ex=0.5`	Temperature scaling of e0.
`te1ex=0.5`	Temperature scaling of e1.
`teta=(-0.9E-3)`	Temperature scaling of eta parameter.
`ucex=1.5`	Temperature scaling of critical velocity of velocity saturation effect.
`tlambda=0.0`	Temperature scaling of lambda parameter.
`ibbt=800.0E-6`	Temperature scaling of ibb.
`tcvl=0.0`	Length scaling of tcv.
`tcvw=0.0`	Width scaling of tcv.

© 2023 Cadence Design Systems, Inc.

`tcvwl=0.0`	Area scaling of tcv.
`gammaov=1.6`	Body effect coefficient of the gate overlap region.
`gammagov=10.0`	Gate doping coefficient for polysilicon depletion effect of the gate overlap region.
`vfbov=0.0`	Flat-band voltage of the gate overlap region.
`lov=20.0E-9`	Effective length of the gate overlap region.
`vov=1.0`	Bias parameter of the overlap capacitances.
`cgso=0.0`	Bias-independent overlap capacitance per gate width unit between gate and source.
`cgdo=0.0`	Bias-independent overlap capacitance per gate width unit between gate and drain.
`cgbo=0.0`	Bias-independent overlap capacitance per gate length unit between gate and bulk.
`kjf=0.0`	Fringing capacitance parameter.
`cjf=0.0`	Bias scaling of fringing capacitance.
`vfr=0.0`	Built-in voltage fine tuning for fringing capacitance model.
`dfr=1.0E-3`	Smooth parameter of fringing capacitance model.
`hdif=0.0e-6`	Half length of the active area.
`rsh=0.0`	Square resistance of active area.
`ldif=0.0`	Distance between the middle of the active area and the start of the channel.
`rs=0.0`	Ldd source series resistance.
`rd=0.0`	Ldd drain series resistance.
`rlx=(-1.0)`	External series resistance per width unit.
`rsx=(-1.0)`	External series resistance per width unit, source side (asymmetric model).
`rdx=(-1.0)`	External series resistance per width unit, drain side (asymmetric model).
`tr=0.0`	First order resistance temperature scaling parameter.
`tr2=0.0`	Second order resistance temperature scaling parameter.

© 2023 Cadence Design Systems, Inc.

gmin=0.0	Minimum conductance of junction diodes.
njs=1.0	Slope factor for junction diode, source side (asymmetrical model).
xjbvs=0.0	Break-down effect coefficient for junction diode, source side (asymmetrical model).
bvs=10.0	Break-down voltage for junction diode, source side (asymmetrical model).
jss=0.0E-09	Area component of current for junction diode, source side (asymmetrical model).
jssws=0.0E-12	Sideways component of current for junction diode, source side (asymmetrical model).
jsswgs=0.0E-12	Gate-side component of current for junction diode, source side (asymmetrical model).
jtss=0.0E-09	Area component of trap-assisted current for junction diode, source side (asymmetrical model).
jtssws=0.0E-12	Sideways component of trap-assisted current for junction diode, source side (asymmetrical model).
jtsswgs=0.0E-12	Gateside component of trap-assisted current for junction diode, source side (asymmetrical model).
njtss=1.0	Area slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
njtssws=1.0	Sideways slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
njtsswgs=1.0	Gateside slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
vtss=0.0	Area voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
vtssws=0.0	Sideways voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
vtsswgs=0.0	Gateside voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
cjs=0.0E-06	Area component of capacitance for junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`cjsws=0.0E-09`	Sideways component of capacitance for junction diode, source side (asymmetrical model).
`cjswgs=0.0E-09`	Gateside component of capacitance for junction diode, source side (asymmetrical model).
`pbs=0.800`	Area parameter of capacitance for junction diode, source side (asymmetrical model).
`pbsws=0.600`	Sideways parameter of capacitance for junction diode, source side (asymmetrical model).
`pbswgs=0.600`	Gateside parameter of capacitance for junction diode, source side (asymmetrical model).
`mjs=0.900`	Area exponent of capacitance for junction diode, source side (asymmetrical model).
`mjsws=0.700`	Sideways exponent of capacitance for junction diode, source side (asymmetrical model).
`mjswgs=0.700`	Gateside exponent of capacitance for junction diode, source side (asymmetrical model).
`xtis=3.0`	Temperature dependence for junction diode, source side (asymmetrical model).
`xtss=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtssws=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtsswgs=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`tnjtss=0.0`	Temperature dependence of njtss (area), junction diode, source side (asymmetrical model).
`tnjtssws=0.0`	Temperature dependence of njtssws (sideways), junction diode, source side (asymmetrical model).
`tnjtsswgs=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`tcj=0.0`	Temperature dependence of area component of capacitance for junction diodes (cjs and cjd), both (source and drain) sides (asymmetrical model).
`tcjsw=0.0`	Temperature dependence of sideways component of capacitance for junction diodes (cjsws and cjswd), both (source and drain) sides (asymmetrical model).
`tcjswg=0.0`	Temperature dependence of gateside component of capacitance for junction diodes (cjswgs and cjswgd), both (source and drain) sides (asymmetrical model).
`tpb=0.0`	Temperature dependence of area parameter of capacitance for junction diodes (pbs and pbd), both (source and drain) sides (asymmetrical model).
`tpbsw=0.0`	Temperature dependence of sideways parameter of capacitance for junction diodes (pbsws and pbswd), both (source and drain) sides (asymmetrical model).
`tpbswg=0.0`	Temperature dependence of gateside parameter of capacitance for junction diodes (pbswgs and pbswgd), both (source and drain) sides (asymmetrical model).
`njd=1.0`	Slope factor for junction diode, drain side (asymmetrical model).
`xjbvd=0.0`	Break-down effect coefficient for junction diode, drain side (asymmetrical model).
`bvd=10.0`	Break-down voltage for junction diode, drain side (asymmetrical model).
`jsd=0.0E-09`	Area component of current for junction diode, drain side (asymmetrical model).
`jsswd=0.0E-12`	Sideways component of current for junction diode, drain side (asymmetrical model).
`jsswgd=0.0E-12`	Gate-side component of current for junction diode, drain side (asymmetrical model).
`jtsd=0.0E-09`	Area component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswd=0.0E-12`	Sideways component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswgd=0.0E-12`	Gateside component of trap-assisted current for junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`njtsd=1.0`	Area slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswd=1.0`	Sideways slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswgd=1.0`	Gateside slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsd=0.0`	Area voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsswd=0.0`	Sideways voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsswgd=0.0`	Gateside voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`cjd=0.0E-06`	Area component of capacitance for junction diode, drain side (asymmetrical model).
`cjswd=0.0E-09`	Sideways component of capacitance for junction diode, drain side (asymmetrical model).
`cjswgd=0.0E-09`	Gateside component of capacitance for junction diode, drain side (asymmetrical model).
`pbd=0.800`	Area parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswd=0.600`	Sideways parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswgd=0.600`	Gateside parameter of capacitance for junction diode, drain side (asymmetrical model).
`mjd=0.900`	Area exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswd=0.700`	Sideways exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswgd=0.700`	Gateside exponent of capacitance for junction diode, drain side (asymmetrical model).
`xtid=3.0`	Temperature dependence for junction diode, drain side (asymmetrical model).
`xtsd=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`xtsswd=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`xtsswgd=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`tnjtsd=0.0`	Temperature dependence of njtss (area), junction diode, drain side (asymmetrical model).
`tnjtsswd=0.0`	Temperature dependence of njtssws (sideways), junction diode, drain side (asymmetrical model).
`tnjtsswgd=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, drain side (asymmetrical model).
`rgsh=3.0`	Gate sheet resistance.
`gc=1`	Type of gate contacts (gc = 1: single sided, gc = 2: both sides).
`krgl1=0.0`	Gate resistance length scaling parameter.
`rdsbsh=1.0E+3`	Substrate network sheet resistance between internal drain and source nodes (used at rf and nqs modes).
`rbwsh=3.0E-3`	Substrate network bulk resistance per width unit between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rbn=0.0`	Substrate network bulk resistance per finger between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rsbwsh=1.0E-3`	Substrate network resistance per width unit between internal source and external bulk nodes (used at rf and nqs modes).
`rsbn=0.0`	Substrate network resistance per finger between internal source and external bulk nodes (used at rf and nqs modes).
`rdbwsh=1.0E-3`	Substrate network resistance per width unit between internal drain and external bulk nodes (used at rf and nqs modes).
`rdbn=0.0`	Substrate network resistance per finger between internal drain and external bulk nodes (used at rf and nqs modes).

© 2023 Cadence Design Systems, Inc.

`ringtype=1.0`	Ringtype, shape of bulk connector (ringtype = 1 for horse-shoe, three sides contact, ringtype = 2 for symmetric, two sides contact), (used at rf4, rf and nqs modes).

Output Parameters

`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`vs (V)`	Vs.
`vd (V)`	Vd.
`vg (V)`	Vg.
`vb (V)`	Vb.
`vds (V)`	Vds.
`vgs (V)`	Vgs.
`vbs (V)`	Vbs.
`vdb (V)`	Vdb.
`vgb (V)`	Vgb.
`beta (A/V`^{2}`)`	Beta.
`idsi (A)`	Intrinsic current.
`idsedge (A)`	Edge effect current.
`idex (A)`	Extrinsic current drain side.
`isex (A)`	Extrinsic current source side.
`igex (A)`	Extrinsic current gate side.
`ibex (A)`	Extrinsic current bulk side.
`n`	Slope factor n.
`vp`	Pinch-off voltage.
`vod (V)`	Overdrive voltage n*(vp-vs).

© 2023 Cadence Design Systems, Inc.

vdsat (V)	Saturation voltage.
sat (s)	Saturation flag.
vth (V)	Effective threshold voltage vth.
vtb (V)	Effective threshold voltage vtb.
weffnf (m)	Effective total width.
weff (m)	Effective finger width.
leff (m)	Effective length.
op_nf	Number of fingers.
ic	Inversion coefficient.
ispec (A)	Specific current.
gmgi (S)	Intrinsic gate tranconductance.
gmsi (S)	Intrinsic source tranconductance.
gmdi (S)	Intrinsic drain tranconductance.
gmbi (S)	Intrinsic bulk tranconductance.
gmgex (S)	Extrinsic gate tranconductance.
gmsex (S)	Extrinsic source tranconductance.
gmdex (S)	Extrinsic drain tranconductance.
gds (S)	Extrinsic drain tranconductance, alias to Gmdex.
gmbex (S)	Extrinsic bulk tranconductance.
gmgutid	Gmg*ut/ids.
gmsutid	Gms*ut/ids.
gmdutid	Gmd*ut/ids.
gmbutid	Gmb*ut/ids.
avi	Intrinsic gain.
gmgid (1/V)	Gm/ids.
vm (V)	Early voltage ids/gds.
ft (Hz)	Transit frequency.
tau0 (s)	Tau0.
tau (s)	Nqs time constant.

© 2023 Cadence Design Systems, Inc.

`cggi (F)`	Cggi.
`cgsi (F)`	Cgsi.
`cgdi (F)`	Cgdi.
`cgbi (F)`	Cgbi.
`csgi (F)`	Csgi.
`csdi (F)`	Csdi.
`csbi (F)`	Csbi.
`cssi (F)`	Cssi.
`cdgi (F)`	Cdgi.
`cddi (F)`	Cddi.
`cdbi (F)`	Cdbi.
`cdsi (F)`	Cdsi.
`cbgi (F)`	Cbgi.
`cbdi (F)`	Cbdi.
`cbbi (F)`	Cbbi.
`cbsi (F)`	Cbsi.
`cgsex (F)`	Extrinsic gate-source capacitance.
`cgdex (F)`	Extrinsic gate-drain capacitance.
`cgbex (F)`	Extrinsic gate-bulk capacitance.
`ctotex (F)`	Total extrinsic capacitance.
`cgsov (F)`	Cgsov.
`cgdov (F)`	Cgdov.
`sid_flicker (`A^2`/Hz)`	Flicker noise psd sdid @ 1hz.
`sid_thermal (`A^2`/Hz)`	Thermal noise psd sdid.
`svg_flicker (`V^2`/Hz)`	Flicker noise psd sdvg @ 1hz.
`svg_thermal (`V^2`/Hz)`	

© 2023 Cadence Design Systems, Inc.

	Thermal noise psd sdvg.
`sigmadidoid`	Relative current mismatch.
`sigmavg (V)`	Gate voltage offset.
`i0 (V)`	Technology current.
`qs (C)`	Source charge.
`qd (C)`	Drain charge.
`qg (C)`	Gate charge.
`qb (C)`	Bulk charge.
`ids (A)`	Resistive drain-to-source current.
`idb (A)`	Impact ionization current.
`qsedge (C)`	Edge charge.
`qdedge (C)`	Edge charge.
`qgedge (C)`	Edge charge.
`qbedge (C)`	Edge charge.
`qsov (C)`	Source side overlap charge.
`qdov (C)`	Drain sie overlap charge.
`qsfr (C)`	Source side fringing charge.
`qdfr (C)`	Drain side fringing charge.
`igidl (A)`	Gate induced drain current.
`igisl (A)`	Gate induced source current.
`igb (A)`	Gate current(bulk).
`igd (A)`	Gate current(drain).
`igs (A)`	Gate current(source).
`igdov (A)`	Overlap gate current (drain).
`igsov (A)`	Overlap gate current (source).
`region`	Estimated operating region. Spectre outputs a number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`pwr (W)`	Power dissipation.

© 2023 Cadence Design Systems, Inc.

Related Topics

EKV3 MOSFET Model (ekv3)

Device ekv3_nqs (ekv3_nqs)

Device ekv3_r4 (ekv3_r4)

Device ekv3_s (ekv3_s)

Device ekv3_s (ekv3_s)

This device is supported within altergroups.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Model Syntax

```
model modelName ekv3_s parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

`l=10.0E-06`	Gate's length.
`w=10.0E-06`	Gate's width.
`nf=1`	Number of fingers.
`m=1`	Number of devices in parallel.
`ad=0.0`	Drain's area.
`as=0.0`	Source's area.
`pd=0.0`	Drain's perimeter.
`ps=0.0`	Source's perimeter.
`sa=0.0`	Sti parameter; distance from sti (side a).
`sb=0.0`	Sti parameter; distance from sti (side b).
`sd=0.0`	Sti parameter; distance between gates.
`trise=0.0`	Temperature change for particular transistor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Parameters

`version=301.02`	Parameter for version control Valid values are 301.02 and 302.00. The default version is 301.02.
`sign=1`	Sign = 1 for nmos; sign = -1 for pmos.
`tg=(-1)`	Type of gate: -1 enhancement type; 1 depletion type.
`tnom=27.0`	Nominal temperature for model parameters.
`scale=1.0`	Scaling size factor.
`xl=0.0`	Optical offset for channel length.
`xw=0.0`	Optical offset for channel width.
`nqs_noi=1.0`	Flag turning on nqs thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1.

© 2023 Cadence Design Systems, Inc.

th_noi=0.0	Flag turning on short channel effects thermal noise model. At a time, only one of nqs_noi and th_noi should be set to 1.
info_level=0.0	Flag for information printout. currently only value of 1 is supported..
qoff=0.0	Flag for turning off the dynamic behavior of the model (for debugging purposes).
avto=0.0	Matching parameter for threshold voltage (vto).
agamma=0.0	Matching parameter for body factor (gamma).
akp=0.0	Matching parameter for mobility (kp).
cox=0.012	Oxide capacitance per unit area.
xj=20.0E-09	Depth of junction (source and drain).
vto=0.3	Threshold voltage.
phif=0.45	Fermi bulk potential.
gamma=0.3	Body effect coefficient.
gammag=4.1	Gate doping coefficient for polysilicon depletion effect.
n0=1.0	Weak inversion fine tuning parameter.
vbi=0.0	Built-in voltage drop-off. if left to default zero value, it is set to the nominal value of 3ut higher than phi..
aqma=0.5	Quantum mechanical effect accumulation region coefficient.
aqmi=0.4	Quantum mechanical effect inversion region coefficient.
etaqm=0.75	Quantum mechanical effect accumulation eta parameter.
kp=500.0E-06	Mobility (multiplied by cox) parameter.
e0=1.0E+10	First order parameter for mobility reduction due to vertical field effect.
e1=3.1E+08	Second order parameter for mobility reduction due to vertical field effect.
eta=0.5	Inversion charge coefficient for vertical field calculation.

© 2023 Cadence Design Systems, Inc.

`thc=0.0`	Coulomb scattering parameter.
`zc=1.0E-6`	Coulomb scattering inversion charge coefficient.
`la=1.0`	Critical length a of mobility length scaling.
`lb=1.0`	Critical length b of mobility length scaling.
`ka=0.0`	Parameter for critical length a of mobility length scaling.
`kb=0.0`	Parameter for critical length b of mobility length scaling.
`wkp1=1.0E-6`	Critical width of mobility width scaling.
`wkp2=0.0`	Amplitude parameter for mobility width scaling.
`wkp3=1.0`	Span parameter for mobility width scaling.
`dl=(-10.0E-9)`	Effective length parameter.
`dlc=0.0`	Effective length parameter for dynamic behavior.
`dw=(-10.0E-9)`	Effective width parameter.
`dwc=0.0`	Effective width parameter for dynamic behavior.
`wdl=0.0`	Effective length parameter for narrow channel devices.
`ldw=0.0`	Effective width parameter for short channel devices.
`ll=0.0`	Base of exponential model for effective length.
`lln=1.0`	Exponent of exponential model for effective length.
`avt=0.0`	Parameter for long and wide channel vto correction.
`lvt=1.0`	Length for long and wide channel vto correction.
`wvt=1.0`	Width for long and wide channel vto correction.
`agam=0.0`	Parameter for long and wide channel gamma correction.
`lgam=1.0`	Length for long and wide channel gamma correction.
`wgam=1.0`	Width for long and wide channel gamma correction.
`nfvta=0.0`	Number of fingers for vto correction for multifinger devices (obsolete model by sti stress effect).
`nfvtb=10000.0`	Parameter for vto correction for multifinger devices (obsolete model by sti stress effect).

© 2023 Cadence Design Systems, Inc.

`ucrit=5.0E+06`	Critical velocity of velocity saturation effect.
`delta=2.0`	Variable order (from 1.0 to 2.0) of velocity saturation effect.
`lambda=0.5`	Length parameter for channel length modulation.
`aclm=0.83`	Fine tuning parameter for channel length modulation.
`lr=50.0E-09`	Length parameter for reverse short channel effect.
`qlr=0.5E-3`	Charge parameter for reverse short channel effect (vto).
`nlr=10.0E-3`	Doping parameter for reverse short channel effect (gamma).
`flr=1.0`	Fermi potential fine tuning parameter for reverse short channel effect (phif).
`leta0=0.0`	Length independent parameter for charge sharing (long channel).
`leta=500.0E-3`	Length scaling parameter for charge sharing.
`leta2=0.0`	Second order length scaling parameter for charge sharing (shortest channel).
`weta=200.0E-3`	Width scaling parameter for charge sharing.
`ncs=1.0`	Weak inversion slope parameter for charge sharing.
`etad=1.0`	Eta parameter for drain induced barrier lowering.
`sigmad=1.0`	Sigma parameter for drain induced barrier lowering.
`wr=90.0E-09`	Width parameter for inverse narrow channel effect.
`qwr=0.3E-3`	Charge parameter for inverse narrow channel effect (vto).
`nwr=5.0E-3`	Doping parameter for inverse narrow channel effect (gamma).
`fprout=1.0E6`	Output resistance parameter for drain induced threshold shift.
`pdits=0.0`	Parameter for drain induced threshold shift (if set to zero the dits effect is disabled).
`pditsl=0.0`	Length scaling parameter for drain induced threshold shift.

© 2023 Cadence Design Systems, Inc.

pditsd=1.0	Bias parameter for drain induced threshold shift.
ddits=0.3	Smooth factor of output conductance for drain induced threshold shift.
iba=000.0E+06	Parameter a of impact ionization current.
ibb=300.0E+06	Parameter b of impact ionization current.
ibn=1.0	Parameter n of impact ionization current.
xb=3.1	Silicon to silicon oxide tunneling barrier height.
eb=29.0E+09	Characteristic electrical field.
kg=00.0E-6	Mobility for gate current.
lovig=20.0E-9	Overlap gate length for overlap gate current.
agidl=0.0	Parameter a of gate induced drain leakage.
bgidl=2.3E+09	Parameter b of gate induced drain leakage.
cgidl=0.5	Parameter c of gate induced drain leakage.
egidl=0.8	Parameter e of gate induced drain leakage.
lfnoi=0	Flicker noise model selection.
kf=0.0	Flicker noise parameter.
af=1.0	Flicker noise frequency exponent.
ef=2.0	Flicker noise transconductance exponent.
nt=1.0E+14	Number of trapped carriers.
alphac=10.0E+4	Coulomb scattering coefficient.
alphah=1.0E-20	Hooge parameter for mobility fluctuation noise model.
kgfn=0.0	Gate flicker noise parameter.
ecn=1.0E+4	Critical field value.
sdr=1.0E-6	Series resistance noise parameter.
lwr=0.0	Length scaling parameter for wr.
lqwr=0.0	Length scaling parameter for qwr.
lnwr=0.0	Length scaling parameter for nwr.
ldphiedge=0.0	Length scaling parameter for dphiedge.
wlr=0.0	Width scaling parameter for lr.

© 2023 Cadence Design Systems, Inc.

wqlr=0.0	Width scaling parameter for qlr.
wnlr=0.0	Width scaling parameter for nlr.
wucrit=0.0	Width scaling parameter for ucrit.
wlambda=0.0	Width scaling parameter for lambda.
wetad=0.0	Width scaling parameter for etad.
we0=0.0	Width scaling parameter for e0.
we1=0.0	Width scaling parameter for e1.
wrlx=0.0	Width scaling parameter for rlx.
wucex=0.0	Width scaling parameter for ucex.
wdphiedge=0.0	Width scaling parameter for dphiedge.
wldphiedge=0.0	Fine tuning scaling for combined short and narrow devices for dphiedge.
wldgammaedge=0.0	Fine tuning scaling for combined short and narrow devices for dgammaedge.
wedge=0.0	Total effective width of edge device for edge conductance effect.
dgammaedge=0.0	Differential gamma parameter of edge device with respect to the main device.
dphiedge=0.0	Differential phi parameter of edge device with respect to the main device.
saref=0.0	Reference sa parameter for sti stress effect parameter extraction.
sbref=0.0	Reference sb parameter for sti stress effect parameter extraction.
wlod=0.0	Width effective parameter for sti stress effect.
kkp=0.0	Mobility parameter for sti stress effect.
lkkp=0.0	Length scaling of mobility for sti stress effect.
wkkp=0.0	Width scaling of mobility for sti stress effect.
pkkp=0.0	Area scaling of mobility for sti stress effect.
tkkp=0.0	Temperature scaling of mobility for sti stress effect.

© 2023 Cadence Design Systems, Inc.

`llodkkp=1.0`	Exponential length scaling parameter of mobility for sti stress effect.
`wlodkkp=1.0`	Exponential width scaling parameter of mobility for sti stress effect.
`kvto=0.0`	Threshold voltage parameter for sti stress effect.
`lkvto=0.0`	Length scaling of threshold voltage for sti stress effect.
`wkvto=0.0`	Width scaling of threshold voltage for sti stress effect.
`pkvto=0.0`	Area scaling of threshold voltage for sti stress effect.
`llodkvto=1.0`	Exponential length scaling parameter of threshold voltage for sti stress effect.
`wlodkvto=1.0`	Exponential width scaling parameter of threshold voltage for sti stress effect.
`kgamma=0.0`	Body effect coefficient parameter for sti stress effect.
`lodkgamma=1.0`	Fine tuning parameter for body effect coefficient scaling of sti stress effect.
`ketad=0.0`	Dibl effect parameter for sti stress effect.
`lodketad=1.0`	Fine tuning parameter for dibl effect parameter scaling of sti stress effect.
`kucrit=0.0`	Critical velocity of velocity saturation effect parameter for sti stress effect.
`tcv=600.0E-6`	Temperature scaling of threshold voltage.
`bex=(-1.5)`	Temperature scaling of mobility.
`te0ex=0.5`	Temperature scaling of e0.
`te1ex=0.5`	Temperature scaling of e1.
`teta=(-0.9E-3)`	Temperature scaling of eta parameter.
`ucex=1.5`	Temperature scaling of critical velocity of velocity saturation effect.
`tlambda=0.0`	Temperature scaling of lambda parameter.
`ibbt=800.0E-6`	Temperature scaling of ibb.
`tcvl=0.0`	Length scaling of tcv.
`tcvw=0.0`	Width scaling of tcv.

© 2023 Cadence Design Systems, Inc.

`tcvwl=0.0`	Area scaling of tcv.
`gammaov=1.6`	Body effect coefficient of the gate overlap region.
`gammagov=10.0`	Gate doping coefficient for polysilicon depletion effect of the gate overlap region.
`vfbov=0.0`	Flat-band voltage of the gate overlap region.
`lov=20.0E-9`	Effective length of the gate overlap region.
`vov=1.0`	Bias parameter of the overlap capacitances.
`cgso=0.0`	Bias-independent overlap capacitance per gate width unit between gate and source.
`cgdo=0.0`	Bias-independent overlap capacitance per gate width unit between gate and drain.
`cgbo=0.0`	Bias-independent overlap capacitance per gate length unit between gate and bulk.
`kjf=0.0`	Fringing capacitance parameter.
`cjf=0.0`	Bias scaling of fringing capacitance.
`vfr=0.0`	Built-in voltage fine tuning for fringing capacitance model.
`dfr=1.0E-3`	Smooth parameter of fringing capacitance model.
`hdif=0.0e-6`	Half length of the active area.
`rsh=0.0`	Square resistance of active area.
`ldif=0.0`	Distance between the middle of the active area and the start of the channel.
`rs=0.0`	Ldd source series resistance.
`rd=0.0`	Ldd drain series resistance.
`rlx=(-1.0)`	External series resistance per width unit.
`rsx=(-1.0)`	External series resistance per width unit, source side (asymmetric model).
`rdx=(-1.0)`	External series resistance per width unit, drain side (asymmetric model).
`tr=0.0`	First order resistance temperature scaling parameter.
`tr2=0.0`	Second order resistance temperature scaling parameter.

© 2023 Cadence Design Systems, Inc.

gmin=0.0	Minimum conductance of junction diodes.
njs=1.0	Slope factor for junction diode, source side (asymmetrical model).
xjbvs=0.0	Break-down effect coefficient for junction diode, source side (asymmetrical model).
bvs=10.0	Break-down voltage for junction diode, source side (asymmetrical model).
jss=0.0E-09	Area component of current for junction diode, source side (asymmetrical model).
jssws=0.0E-12	Sideways component of current for junction diode, source side (asymmetrical model).
jsswgs=0.0E-12	Gate-side component of current for junction diode, source side (asymmetrical model).
jtss=0.0E-09	Area component of trap-assisted current for junction diode, source side (asymmetrical model).
jtssws=0.0E-12	Sideways component of trap-assisted current for junction diode, source side (asymmetrical model).
jtsswgs=0.0E-12	Gateside component of trap-assisted current for junction diode, source side (asymmetrical model).
njtss=1.0	Area slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
njtssws=1.0	Sideways slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
njtsswgs=1.0	Gateside slope factor of trap-assisted current for junction diode, source side (asymmetrical model).
vtss=0.0	Area voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
vtssws=0.0	Sideways voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
vtsswgs=0.0	Gateside voltage factor of trap-assisted current for junction diode, source side (asymmetrical model).
cjs=0.0E-06	Area component of capacitance for junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`cjsws=0.0E-09`	Sideways component of capacitance for junction diode, source side (asymmetrical model).
`cjswgs=0.0E-09`	Gateside component of capacitance for junction diode, source side (asymmetrical model).
`pbs=0.800`	Area parameter of capacitance for junction diode, source side (asymmetrical model).
`pbsws=0.600`	Sideways parameter of capacitance for junction diode, source side (asymmetrical model).
`pbswgs=0.600`	Gateside parameter of capacitance for junction diode, source side (asymmetrical model).
`mjs=0.900`	Area exponent of capacitance for junction diode, source side (asymmetrical model).
`mjsws=0.700`	Sideways exponent of capacitance for junction diode, source side (asymmetrical model).
`mjswgs=0.700`	Gateside exponent of capacitance for junction diode, source side (asymmetrical model).
`xtis=3.0`	Temperature dependence for junction diode, source side (asymmetrical model).
`xtss=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtssws=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`xtsswgs=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, source side (asymmetrical model).
`tnjtss=0.0`	Temperature dependence of njtss (area), junction diode, source side (asymmetrical model).
`tnjtssws=0.0`	Temperature dependence of njtssws (sideways), junction diode, source side (asymmetrical model).
`tnjtsswgs=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, source side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`tcj=0.0`	Temperature dependence of area component of capacitance for junction diodes (cjs and cjd), both (source and drain) sides (asymmetrical model).
`tcjsw=0.0`	Temperature dependence of sideways component of capacitance for junction diodes (cjsws and cjswd), both (source and drain) sides (asymmetrical model).
`tcjswg=0.0`	Temperature dependence of gateside component of capacitance for junction diodes (cjswgs and cjswgd), both (source and drain) sides (asymmetrical model).
`tpb=0.0`	Temperature dependence of area parameter of capacitance for junction diodes (pbs and pbd), both (source and drain) sides (asymmetrical model).
`tpbsw=0.0`	Temperature dependence of sideways parameter of capacitance for junction diodes (pbsws and pbswd), both (source and drain) sides (asymmetrical model).
`tpbswg=0.0`	Temperature dependence of gateside parameter of capacitance for junction diodes (pbswgs and pbswgd), both (source and drain) sides (asymmetrical model).
`njd=1.0`	Slope factor for junction diode, drain side (asymmetrical model).
`xjbvd=0.0`	Break-down effect coefficient for junction diode, drain side (asymmetrical model).
`bvd=10.0`	Break-down voltage for junction diode, drain side (asymmetrical model).
`jsd=0.0E-09`	Area component of current for junction diode, drain side (asymmetrical model).
`jsswd=0.0E-12`	Sideways component of current for junction diode, drain side (asymmetrical model).
`jsswgd=0.0E-12`	Gate-side component of current for junction diode, drain side (asymmetrical model).
`jtsd=0.0E-09`	Area component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswd=0.0E-12`	Sideways component of trap-assisted current for junction diode, drain side (asymmetrical model).
`jtsswgd=0.0E-12`	Gateside component of trap-assisted current for junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`njtsd=1.0`	Area slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswd=1.0`	Sideways slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`njtsswgd=1.0`	Gateside slope factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsd=0.0`	Area voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsswd=0.0`	Sideways voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`vtsswgd=0.0`	Gateside voltage factor of trap-assisted current for junction diode, drain side (asymmetrical model).
`cjd=0.0E-06`	Area component of capacitance for junction diode, drain side (asymmetrical model).
`cjswd=0.0E-09`	Sideways component of capacitance for junction diode, drain side (asymmetrical model).
`cjswgd=0.0E-09`	Gateside component of capacitance for junction diode, drain side (asymmetrical model).
`pbd=0.800`	Area parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswd=0.600`	Sideways parameter of capacitance for junction diode, drain side (asymmetrical model).
`pbswgd=0.600`	Gateside parameter of capacitance for junction diode, drain side (asymmetrical model).
`mjd=0.900`	Area exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswd=0.700`	Sideways exponent of capacitance for junction diode, drain side (asymmetrical model).
`mjswgd=0.700`	Gateside exponent of capacitance for junction diode, drain side (asymmetrical model).
`xtid=3.0`	Temperature dependence for junction diode, drain side (asymmetrical model).
`xtsd=0.0`	Area component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).

© 2023 Cadence Design Systems, Inc.

`xtsswd=0.0`	Sideways component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`xtsswgd=0.0`	Gateside component of temperature dependence of trap-assisted current for junction diode, drain side (asymmetrical model).
`tnjtsd=0.0`	Temperature dependence of njtss (area), junction diode, drain side (asymmetrical model).
`tnjtsswd=0.0`	Temperature dependence of njtssws (sideways), junction diode, drain side (asymmetrical model).
`tnjtsswgd=0.0`	Temperature dependence of njtsswgs (gateside), junction diode, drain side (asymmetrical model).
`rgsh=3.0`	Gate sheet resistance.
`gc=1`	Type of gate contacts (gc = 1: single sided, gc = 2: both sides).
`krgl1=0.0`	Gate resistance length scaling parameter.
`rdsbsh=1.0E+3`	Substrate network sheet resistance between internal drain and source nodes (used at rf and nqs modes).
`rbwsh=3.0E-3`	Substrate network bulk resistance per width unit between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rbn=0.0`	Substrate network bulk resistance per finger between internal bulk and external bulk nodes (used at rf4, rf and nqs modes).
`rsbwsh=1.0E-3`	Substrate network resistance per width unit between internal source and external bulk nodes (used at rf and nqs modes).
`rsbn=0.0`	Substrate network resistance per finger between internal source and external bulk nodes (used at rf and nqs modes).
`rdbwsh=1.0E-3`	Substrate network resistance per width unit between internal drain and external bulk nodes (used at rf and nqs modes).
`rdbn=0.0`	Substrate network resistance per finger between internal drain and external bulk nodes (used at rf and nqs modes).

© 2023 Cadence Design Systems, Inc.

`ringtype=1.0`	Ringtype, shape of bulk connector (ringtype = 1 for horse-shoe, three sides contact, ringtype = 2 for symmetric, two sides contact), (used at rf4, rf and nqs modes).

Output Parameters

`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`vs (V)`	Vs.
`vd (V)`	Vd.
`vg (V)`	Vg.
`vb (V)`	Vb.
`vds (V)`	Vds.
`vgs (V)`	Vgs.
`vbs (V)`	Vbs.
`vdb (V)`	Vdb.
`vgb (V)`	Vgb.
`beta (A/V`^{2}`)`	Beta.
`idsi (A)`	Intrinsic current.
`idsedge (A)`	Edge effect current.
`idex (A)`	Extrinsic current drain side.
`isex (A)`	Extrinsic current source side.
`igex (A)`	Extrinsic current gate side.
`ibex (A)`	Extrinsic current bulk side.
`n`	Slope factor n.
`vp`	Pinch-off voltage.
`vod (V)`	Overdrive voltage n*(vp-vs).

© 2023 Cadence Design Systems, Inc.

vdsat (V)	Saturation voltage.
sat (s)	Saturation flag.
vth (V)	Effective threshold voltage vth.
vtb (V)	Effective threshold voltage vtb.
weffnf (m)	Effective total width.
weff (m)	Effective finger width.
leff (m)	Effective length.
op_nf	Number of fingers.
ic	Inversion coefficient.
ispec (A)	Specific current.
gmgi (S)	Intrinsic gate tranconductance.
gmsi (S)	Intrinsic source tranconductance.
gmdi (S)	Intrinsic drain tranconductance.
gmbi (S)	Intrinsic bulk tranconductance.
gmgex (S)	Extrinsic gate tranconductance.
gmsex (S)	Extrinsic source tranconductance.
gmdex (S)	Extrinsic drain tranconductance.
gds (S)	Extrinsic drain tranconductance, alias to Gmdex.
gmbex (S)	Extrinsic bulk tranconductance.
gmgutid	Gmg*ut/ids.
gmsutid	Gms*ut/ids.
gmdutid	Gmd*ut/ids.
gmbutid	Gmb*ut/ids.
avi	Intrinsic gain.
gmgid (1/V)	Gm/ids.
vm (V)	Early voltage ids/gds.
ft (Hz)	Transit frequency.
tau0 (s)	Tau0.
tau (s)	Nqs time constant.

© 2023 Cadence Design Systems, Inc.

`cggi (F)`	Cggi.
`cgsi (F)`	Cgsi.
`cgdi (F)`	Cgdi.
`cgbi (F)`	Cgbi.
`csgi (F)`	Csgi.
`csdi (F)`	Csdi.
`csbi (F)`	Csbi.
`cssi (F)`	Cssi.
`cdgi (F)`	Cdgi.
`cddi (F)`	Cddi.
`cdbi (F)`	Cdbi.
`cdsi (F)`	Cdsi.
`cbgi (F)`	Cbgi.
`cbdi (F)`	Cbdi.
`cbbi (F)`	Cbbi.
`cbsi (F)`	Cbsi.
`cgsex (F)`	Extrinsic gate-source capacitance.
`cgdex (F)`	Extrinsic gate-drain capacitance.
`cgbex (F)`	Extrinsic gate-bulk capacitance.
`ctotex (F)`	Total extrinsic capacitance.
`cgsov (F)`	Cgsov.
`cgdov (F)`	Cgdov.
`sid_flicker (`A^2`/Hz)`	Flicker noise psd sdid @ 1hz.
`sid_thermal (`A^2`/Hz)`	Thermal noise psd sdid.
`svg_flicker (`V^2`/Hz)`	Flicker noise psd sdvg @ 1hz.
`svg_thermal (`V^2`/Hz)`	

© 2023 Cadence Design Systems, Inc.

	Thermal noise psd sdvg.
`sigmadidoid`	Relative current mismatch.
`sigmavg (V)`	Gate voltage offset.
`i0 (V)`	Technology current.
`qs (C)`	Source charge.
`qd (C)`	Drain charge.
`qg (C)`	Gate charge.
`qb (C)`	Bulk charge.
`ids (A)`	Resistive drain-to-source current.
`idb (A)`	Impact ionization current.
`qsedge (C)`	Edge charge.
`qdedge (C)`	Edge charge.
`qgedge (C)`	Edge charge.
`qbedge (C)`	Edge charge.
`qsov (C)`	Source side overlap charge.
`qdov (C)`	Drain sie overlap charge.
`qsfr (C)`	Source side fringing charge.
`qdfr (C)`	Drain side fringing charge.
`igidl (A)`	Gate induced drain current.
`igisl (A)`	Gate induced source current.
`igb (A)`	Gate current (bulk).
`igd (A)`	Gate current (drain).
`igs (A)`	Gate current (source).
`igdov (A)`	Overlap gate current (drain).
`igsov (A)`	Overlap gate current (source).
`region`	Estimated operating region. Spectre a outputs number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`pwr (W)`	Power dissipation.

© 2023 Cadence Design Systems, Inc.

Related Topics

EKV3 MOSFET Model (ekv3)

Device ekv3_nqs (ekv3_nqs)

Device ekv3_r4 (ekv3_r4)

Device ekv3_rf (ekv3_rf)

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

29

BSIMSOI MOSFET Model (bsimsoi)

The BSIMSOI model is a Silicon-on-Insulator (SOI) MOSFET model. It was developed by the BSIM/SOI modeling group at the University of California, Berkeley.

There are two modes in BSIMSOI depending on the value of *soiMod*:

- PD mode (`soiMod=0`), where the body potential is independent of ΔV_{bi} (V_{BS}>ΔV_{bi}). Hence the calculation of ΔV_{bi} is skipped in this mode.
- DD (Unified) mode (`soiMod=1`), where both ΔV_{bi} and body current/charge are calculated to capture the floating-body behavior exhibited in FD devices.
- FD mode (`soiMod=2`), where the body potential is equal to ΔV_{bi}. Hence the calculation of body current/charge, which is essential to the PD model, is skipped.

Related Topics

Device Structure

Equivalent Circuit

Device Regions

Global Control Options

Model Equations

Model Version Updates

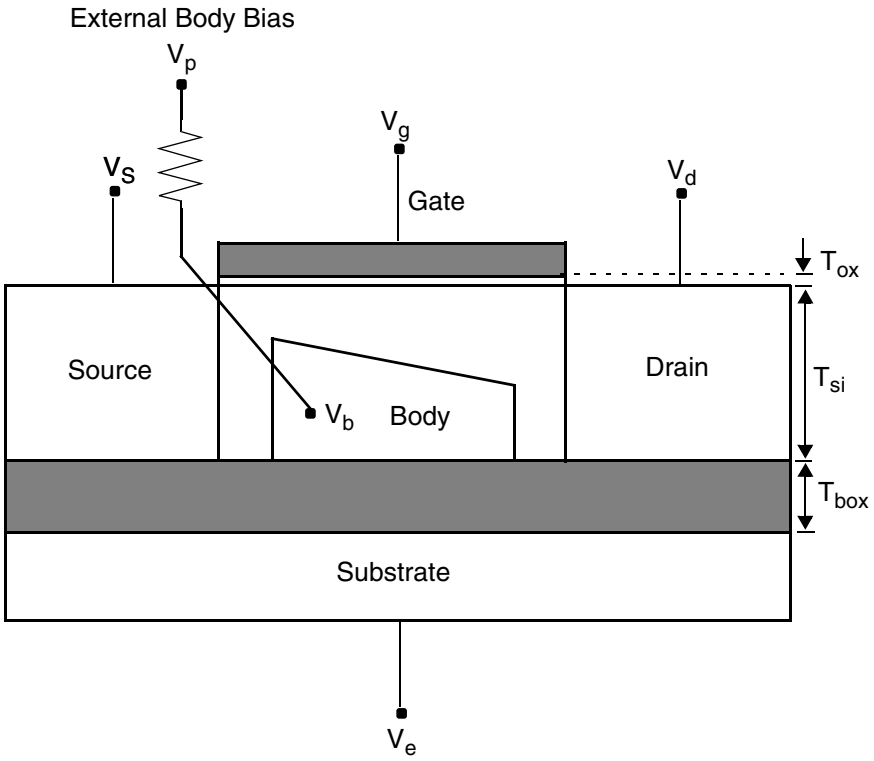
Model Usage

Component Statements

© 2023 Cadence Design Systems, Inc.

Device Structure

BSIMSOI device's typical structure is shown in the following figure.



In the floating body configuration, there are four external biases: drain voltage (Vd), gate voltage (Vg), source voltage (Vs) and backgate voltage (Ve). The voltage of floating body is solved by iterating in circuit simulation. If body contact is applied, there is one mode external bias: bulk voltage (Vp).

Since the backgate is decoupled by the isolated layer, there are three models to describe the behaviors of the floating body (selected by model parameter 'soimod'):

- PD mode (soimod=0): the body potential is independent for ?Vbi;
- DD mode (soimod=1): both ?Vbi and body current/charge are concerned to capture the floating body behavior;
- FD mode (soimod=2): the body potential is equal to ?vbi

© 2023 Cadence Design Systems, Inc.

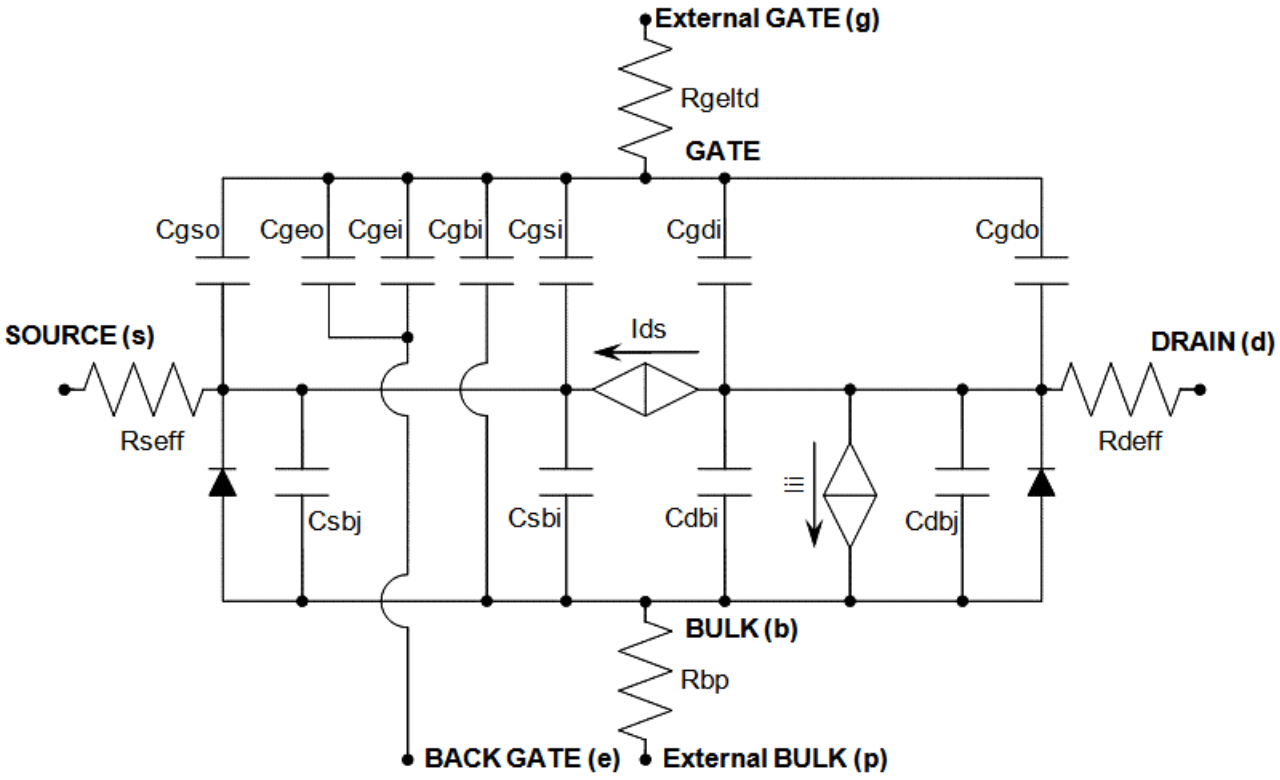
Auto mode (soimod=3): determine the floating body model by with model parameters automatically.

Related Topics

BSIMSOI MOSFET Model (bsimsoi)

Equivalent Circuit

Because the BSIMSOI model is developed based on the BSIM3v3 model, it shares the similar basic equivalent circuit with the BSIM3v3 model except the part of floating body. The followings show the equivalent circuits for BSIMSOI devices:



Related Topics

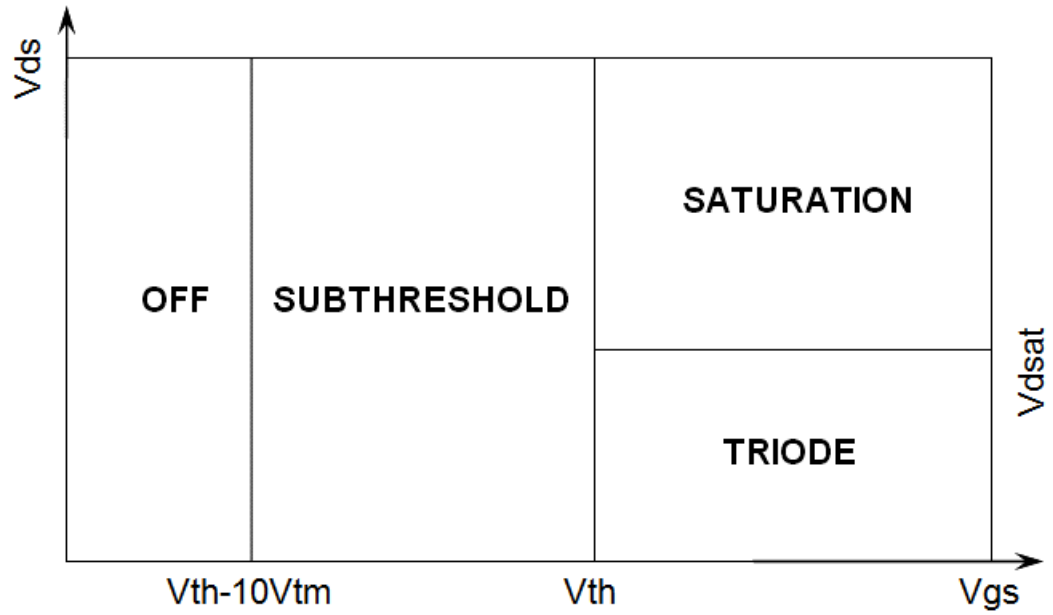
BSIMSOI MOSFET Model (bsimsoi)

© 2023 Cadence Design Systems, Inc.

Device Regions

This section describes devices region for the BSIMSOI model. Device region is determined by both Vds and Vgs. The following figure shows the region of N-type BSIMSOI device. For P-type device, all the voltage in figure is negative.

V_{tm} is the thermal voltage which is about 0.026V for 300°K temperature.



Related Topics

BSIMSOI MOSFET Model (bsimsoi)

Global Control Options

The following global options affect BSIMSOI model.

1. GMIN: GMIN helps solver convergence. It places a conductance in parallel with both the channel and source junction. The default GMIN is 1.0e-12.
2. MINR: Source, drain and gate parasitic resistors inside devices less than minr will be removed. The order of checking inside devices is:
   - Check if resistors are smaller than local minr, if so then remove the parasitic resistors, give warning message.

© 2023 Cadence Design Systems, Inc.

- Check global minr, parasitic resistors less than global minr will be removed and warning message will be issued.

In Spectre, both model parameter minr and global minr take effect at same time. So, for global minr to be activated, the value for minr has to be set both globally and locally.

Note: Local minr is specified by model parameter minr. The default value is 0.1

COMPATIBLE: Encourage device equations to be compatible with a foreign simulator. This option does not affect input syntax. Possible values are spectre, spice2, or, spice3.

Related Topics

BSIMSOI MOSFET Model (bsimsoi)

© 2023 Cadence Design Systems, Inc.

Model Equations

DC current

(29-1)

$$I_{ds,MOSFET} = \frac{I_{ds0}}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A} \right)$$

$$I_{ds0} = \frac{\beta V_{gsteff} \left(1 - A_{bulk} \frac{V_{dseff}}{2\left(V_{gsteff} + 2V_t\right)} \right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}}$$

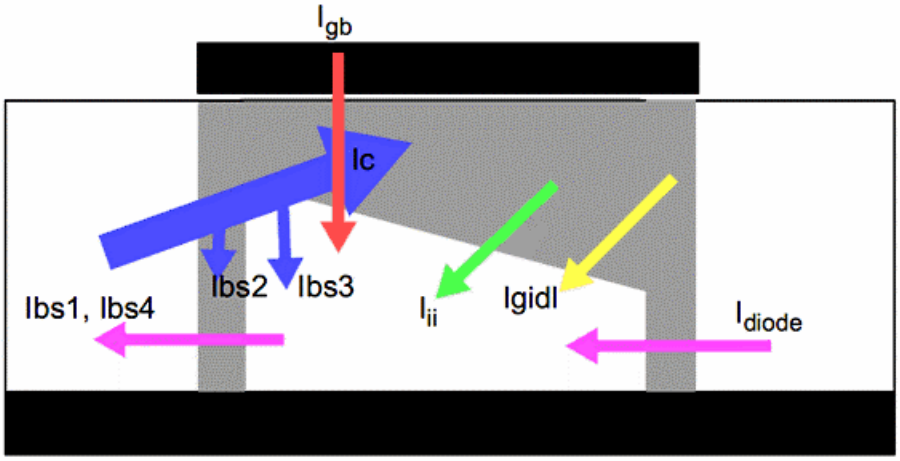
$$\beta = \mu_{eff} f C_{ox} \frac{W_{eff}}{L_{eff}}$$

Where Abulk is the bulk charge factor:

$$A_{bulk} = 1 + \left(\frac{K_{1ox} \cdot \sqrt{1 + \frac{LPEB}{L_{eff}}}}{2\sqrt{\left(\phi_s + Keta\right) - \frac{V_{bsh}}{1 + Keta \cdot V_{bsh}}}} \left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{T_{si} X_{dep}}} \left(1 - A_{gs} V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{T_{si} X_{dep}}} \right)^2 \right) + \frac{B_0}{W_{eff} + B_1} \right) \right)$$

© 2023 Cadence Design Systems, Inc.

Body current



The backward injection current in the B-S/D diode can be expressed as

(29-2)

$$I_{bs1} = W_{dios} T_{si} j_{sdif} \left(e^{\frac{V_{bs}}{n_{diode} V_t}} - 1 \right)$$

$$I_{bd1} = W_{diod} T_{si} j_{ddif} \left(e^{\frac{V_{bd}}{n_{diode} V_t}} - 1 \right)$$

The carrier recombination and trap-assisted tunneling current in the space-charge region is modeled by

(29-3)

$$I_{bs2} = W_{dios} T_{si} j_{srec} \left(e^{\frac{V_{bs}}{0.026\, n_{recf}}} - e^{\frac{V_{sb}}{0.026\, n_{recr}} \frac{V_{rec0}}{V_{rec0}+V_{sb}}} \right)$$

$$I_{bd2} = W_{diod} T_{si} j_{drec} \left(e^{\frac{V_{bd}}{0.026\, n_{recfd}}} - e^{\frac{V_{db}}{0.026\, n_{recrd}} \frac{V_{rec0d}}{V_{rec0d}+V_{db}}} \right)$$

© 2023 Cadence Design Systems, Inc.

The reverse bias tunneling current, which may be significant in junctions with high doping concentration, can be expressed as

(29-4)

$$I_{bs4} = W_{dios} T_{si} j_{stun} \left(1 - e^{\frac{V_{sb}}{0.026\, n_{tun}} \frac{V_{tun0}}{V_{tun0}+V_{sb}}} \right)$$

$$I_{bd4} = W_{diod} T_{si} j_{dtun} \left(1 - e^{\frac{V_{db}}{0.026\, n_{tund}} \frac{V_{tun0d}}{V_{tun0d}+V_{db}}} \right)$$

The recombination current in the neutral body can be described by

(29-5)

$$I_{bs3} = \left(1 - \alpha_{bjt}\right) I_{en} \left(e^{\frac{V_{bs}}{n_{diode} V_t}} - 1 \right) \frac{1}{\sqrt{E_{hlis}+1}}$$

$$I_{bd3} = \left(1 - \alpha_{bjt}\right) I_{en} \left(e^{\frac{V_{bd}}{n_{dioded} V_t}} - 1 \right) \frac{1}{\sqrt{E_{hlid}+1}}$$

$$I_{en} = W'_{eff} T_{si} j_{sbjt} \left(L_{bjt0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right) \right)^N$$

$$E_{hlis} = A_{hli_eff} \left(e^{\frac{V_{bs}}{n_{dio} V_t}} - 1 \right)$$

$$E_{hlid} = A_{hli_eff} \left(e^{\frac{V_{bd}}{n_{dio} V_t}} - 1 \right)$$

$$\alpha_{bjt} = e^{-0.5 \left(\frac{L_{eff}}{L_n} \right)^2}$$

The BJT collector current is modeled as

© 2023 Cadence Design Systems, Inc.

(29-6)

$$I_c = \alpha_{bjt} I_{en} \left(e^{\frac{V_{bs}}{n_{diodes} V_t}} - e^{\frac{V_{bd}}{n_{dioded} V_t}} \right) \frac{1}{E_{2nd}}$$

$$E_{2nd} = \frac{E_{ely} + \sqrt{E_{ely}^{\ 2} + 4E_{hli}}}{2}$$

$$E_{ely} = 1 + \frac{V_{bs} + V_{bd}}{V_{Abjt} + A_{ely} L_{eff}}$$

$$E_{hli} = E_{hlis} + E_{hlid}$$

Impact Ionization Current Equation is modeled as

(29-7)

$$I_{ii} = \alpha_0 \left(I_{ds,MOSFET} + I_{ii_BJT} \right) e^{\frac{V_{diff}}{\beta_2 + \beta_1 V_{diff} + \beta_0 V_{diff}^{\ 2}}}$$

In this expression, the parasitic BJT effect current is modeled as

(29-8)

- IiiMod = 0

$$I_{ii_BJT} = F_{bjtii} I_c$$

$$V_{diff} = V_{ds} - V_{dsatii}$$

$$V_{dsatii} = V_{gsStep} + \left(V_{dsatii0} \left(1 + T_{ii} \left(\frac{T}{T_{nom}} - 1 \right) \right) - \frac{L_{ii}}{L_{eff}} \right)$$

$$V_{gsStep} = \left(\frac{E_{satii} L_{eff}}{1 + E_{satii} L_{eff}} \right) \left(\frac{1}{1 + S_{ii1} V_{gsteff}} + S_{ii2} \right) \left(\frac{S_{ii0} V_{gst}}{1 + S_{iid} V_{ds}} \right)$$

© 2023 Cadence Design Systems, Inc.

(29-9)

- IiiMod = 1

$$I_{ii_BJT} = \frac{CBJTII + EBJTII \cdot L_{eff}}{L_{eff}} I_c \left(V_{bci} - V_{bd}\right) e^{-ABJTii \cdot \left(V_{bci} - V_{bd}\right)^{(MBJTII-1)}}$$

$$V_{bci} = VBCI\left(1 + TVBCI\left(\frac{T}{T_{nom}} - 1\right)\right)$$

If body contact is applied, there is one more bulk contact current flow into bulk. It is modeled as:

(29-10)

$$I_{bp} = \frac{V_{bp}}{R_{bp} + R_{bodyext}}$$

$$R_{bp} = \left(R_{body}\frac{W'_{eff}}{L_{eff}}\right) \| \left(R_{halo}\frac{W'_{eff}}{2}\right)$$

$$R_{bodyext} = R_{bsh} N_{rb}$$

Leakage current

Gate Induced Source/Drain Leakage Current is modeled as:

(29-11)

gidlMod = 0

$$I_{GIDL} = A_{GIDL} \cdot W_{diod} \cdot Nf \frac{V_{ds} - V_{gse} - E_{GIDL} + V_{fbsd}}{3T_{oxe}} e^{-\frac{3T_{oxe}B_{GIDL}}{V_{ds} - V_{gse} - E_{GIDL}}} \frac{V_{db}^{\ 3}}{C_{GIDL} + V_{db}^{\ 3}}$$

$$I_{GISL} = A_{GISL} \cdot W_{dios} \cdot Nf \frac{-V_{ds} - V_{gde} - E_{GISL} + V_{fbsd}}{3T_{oxe}} e^{-\frac{3T_{oxe}B_{GISL}}{-V_{ds} - V_{gde} - E_{GISL}}} \frac{V_{sb}^{\ 3}}{C_{GISL} + V_{sb}^{\ 3}}$$

© 2023 Cadence Design Systems, Inc.

(29-12)

gidlMod = 1

$$I_{GIDL} = A_{GIDL} \cdot W_{diod} \cdot Nf \frac{V_{ds} - R_{GIDL} V_{gse} - E_{GIDL} + V_{fbsd}}{3T_{oxe}} e^{-\frac{3T_{oxe} B_{GIDL}}{V_{ds} - V_{gse} - E_{GIDL}}} e^{\frac{K_{GIDL}}{V_{bd} - F_{GIDL}}}$$

$$I_{GISL} = A_{GISL} \cdot W_{dios} \cdot Nf \frac{-V_{ds} - R_{GISL} V_{gde} - E_{GISL} + V_{fbsd}}{3T_{oxe}} e^{-\frac{3T_{oxe} B_{GISL}}{-V_{ds} - V_{gde} - E_{GISL}}} e^{\frac{K_{GISL}}{V_{bs} - F_{GISL}}}$$

For thin oxide (below 2nm), oxide tunneling is important in the determination of floating-body potential. In inversion, the tunneling current is:

(29-13)

$$J_{gb} = A \frac{V_{gb} V_{aux}}{T_{ox}^{\ 2}} \left(\frac{T_{oxref}}{T_{oxqm}} \right)^{N_{tox}} e^{\frac{-B\left(\alpha_{gb1} - \beta_{gb1} |V_{ox}|\right) T_{ox}}{1 - \frac{|V_{ox}|}{V_{gb1}}}}$$

$$V_{aux} = V_{EVB} \ln\left(1 + e^{\frac{|V_{ox}| - \varphi_g}{V_{EVB}}} \right)$$

$$A = \frac{q^3}{8\pi h \phi_b}$$

$$B = \frac{8\pi \sqrt{2 m_{ox}} \phi_b^{\ 3/2}}{3hq}$$

$$\phi_b = 4.2eV$$

$$m_{ox} = 0.3 m_0$$

In accumulation, the tunneling current is:

© 2023 Cadence Design Systems, Inc.

(29-14)

$$J_{gb} = A\frac{V_{gb}V_{aux}}{T_{ox}^{\ 2}}\left(\frac{T_{oxref}}{T_{oxqm}}\right)^{N_{tox}} e^{\frac{-B\left(\alpha_{gb2}-\beta_{gb2}|V_{ox}|\right)T_{ox}}{1-\frac{|V_{ox}|}{V_{gb2}}}}$$

$$V_{aux} = V_{ECB}\ln\left(1+e^{-\frac{V_{gb}-V_{fb}}{V_{ECB}}}\right)$$

$$A = \frac{q^3}{8\pi h\phi_b}$$

$$B = \frac{8\pi\sqrt{2m_{ox}}\phi_b^{\ 3/2}}{3hq}$$

$$\phi_b = 3.2eV$$

$$m_{ox} = 0.4m_0$$

In BSIMSOI4.1, the instance parameter Agbcp2 represents the parasitic gate to body overlap area due to the body contact. This parameter applies for the opposite-type gate. The tunneling current in this region is modeled as:

(29-15)

$$I_{g_agbcp2} = A\cdot A_{agbcp2}\min\left(V_{gp}-V_{fb2},0\right)\cdot V_{gp_eff}T_{oxRatio}e^{-B\cdot T_{oxqm}\left(A_{IGBCP2}-B_{IGBCP2}V_{gp_eff}\right)\left(1+C_{IGBCP2}V_{gp_eff}\right)}$$

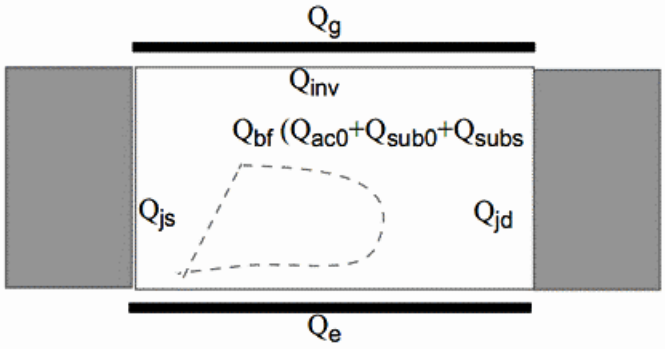
$$V_{gp_eff} = 0.5\left(\sqrt{\left(V_{gp}-V_{fb2}\right)^2+\delta^2}-\left(V_{gp}-V_{fb2}\right)-\delta\right)$$

$$\delta = 0.01$$

© 2023 Cadence Design Systems, Inc.

Charge and Capacitance

The following is the schematic of Charge model in BSIMSOI model.



For intrinsic charge, BSIMSOI PD model uses similar expressions to $BSIM_{3v3}$ for inversion charge (Q_{inv}) and front gate body charge (Q_{Bf}). The bulk charge constant A_{bulkCV} is defined as:

(29-16)

$$A_{bulkCV} = A_{bulk0}\left(1+\left(\frac{CLC}{L_{active}}\right)^{CLE}\right)$$

$$A_{bulk0} = A_{bulk}\left(V_{gsteff} = 0\right)$$

The effective CV V_{gst} has two equations selected by model parameter `vgstcvmod`:

(29-17)

vg4stcvmod = 0 and 1

$$V_{gsteffCV} = nV_t \ln\left(1+e^{\frac{V_{gs}-V_{th}}{nV_t}}\cdot e^{-\frac{delvt}{nV_t}}\right)$$

The difference between `vgstcvmod` = 0 and 1 is that `vgstcvmod` = 1 fixed the bug of vgstcvmod = 0. The default value for `vgstcvmod` has been changed to 1 from 0 after BSIMSOI model version 4.2.

(29-18)

© 2023 Cadence Design Systems, Inc.

vgstcvmod = 2

$$V_{gsteffCV} = \frac{nV_t \ln\left(1+e^{\frac{m^{*CV}\left(V_{gs_eff}-V_{th}-delvt\right)}{nV_t}}\right)}{m^{*CV}+nC_{ox}\sqrt{\frac{2\phi_s}{q\varepsilon_{si}N_{dep}}}e^{-\frac{\left(1-m^{*CV}\right)\left(V_{gs_eff}-V_{th}-delvt\right)-V_{offCV}}{nV_t}}}$$

$$m^{*CV} = 0.5+\frac{\arctan\left(MINCV\right)}{\pi}$$

Then the inversion charge can be expressed as:

(29-19)

$$Q_{inv} = -W_{active}L_{active}C_{ox}\left(\left(V_{gsteffCV}-\frac{A_{bulkCV}}{2}V_{dsCV}\right)+\frac{A_{bulkCV}{}^2V_{dsCV}{}^2}{12\left(V_{gsteffCV}-\frac{A_{bulkCV}{}^2}{2}V_{dsCV}\right)}\right)$$

$$V_{dsCV} = V_{dsatCV}-\frac{1}{2}\left(V_{dsatCV}-V_{ds}-\delta+\sqrt{\left(V_{dsatCV}-V_{ds}-\delta\right)^2+4\delta V_{dsatCV}}\right)$$

$$V_{dsatCV} = V_{gsteffCV}/A_{bulkCV}$$

The accumulation charge can be calculated as:

(29-20)

$$Q_{ac0} = -F_{body}W_{active}L_{activeB}C_{ox}\left(V_{FBeff}-V_{fb}\right)$$

$$V_{FBeff} = V_{fb}-0.5\left(\left(V_{fb}-V_{gb}-\delta\right)+\sqrt{\left(V_{fb}-V_{gb}-\delta\right)^2+\delta^2}\right)$$

$$V_{gb} = V_{gs}-V_{bseff}$$

$$V_{fb} = V_{th}-\phi_s-K_{1eff}\sqrt{\phi_s-V_{bseff}}$$

© 2023 Cadence Design Systems, Inc.

The gate-induced depletion charge and drain-induced depletion charge can be expressed as:

(29-21)

$$Q_{sub0} = -F_{body} W_{active} L_{activeB} C_{ox} \frac{K_{1eff}^{\ 2}}{2} \left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffCV} - V_{bseff})}{K_{1eff}^{\ 2}}} \right)$$

$$Q_{subs} = F_{body} W_{active} L_{activeB} K_{1eff} C_{ox} (1 - A_{bulkCV}) \left(\frac{V_{dsCV}}{2} - \frac{A_{bulkCV} V_{dsCV}^{\ 2}}{12(V_{gsteffCV} - A_{bulkCV} V_{dsCV}/2)} \right)$$

The back gate body charge can be modeled by

(29-22)

$$Q_e = F_{body} W_{active} L_{activeBG} C_{box} (V_{es} - V_{fbb} - V_{bseff})$$

For `capmod`=3, the flat band voltage is calculated from the bias-independent threshold voltage, which is different from `capMod`=2.

In BSIMSOI PD model, both the depletion and diffusion capacitance of the junction are considered. The diffusion charges Qbddif/Qbsdif are modeled as:

(29-23)

$$Q_{bsdif} = \tau \frac{W_{eff}^{'}}{N_{seg}} T_{si} J_{sbjt} \left(1 + L_{dif0} \left(L_{bj0} \left(\frac{1}{L_{eff}} - \frac{1}{L_n} \right) \right)^{N_{dif}} \right) \left(e^{\frac{V_{bs}}{n_{dios} V_t}} - 1 \right) \frac{1}{\sqrt{E_{hlis} + 1}}$$

$$Q_{bddif} = \tau \frac{W_{eff}^{'}}{N_{seg}} T_{si} J_{dbjt} \left(1 + L_{dif0} \left(L_{bj0} \left(\frac{1}{L_{eff}} - \frac{1}{L_n} \right) \right)^{N_{dif}} \right) \left(e^{\frac{V_{bd}}{n_{diod} V_t}} - 1 \right) \frac{1}{\sqrt{E_{hlid} + 1}}$$

The depletion charges Q_{bddep}/Q_{bsdep} are modeled as:

© 2023 Cadence Design Systems, Inc.

(29-24)

$$Q_{bsdep} = W_{dioCV} C_{jswgs} \frac{T_{si}}{10^{-7}} \frac{P_{bswgs}}{1 - M_{jswgs}} \left(1 - \left(1 - \frac{V_{bs}}{P_{bswgs}} \right)^{1 - M_{jswgs}} \right)$$

$$Q_{bddep} = W_{dioCV} C_{jswgd} \frac{T_{si}}{10^{-7}} \frac{P_{bswgd}}{1 - M_{jswgd}} \left(1 - \left(1 - \frac{V_{bd}}{P_{bswgd}} \right)^{1 - M_{jswgd}} \right)$$

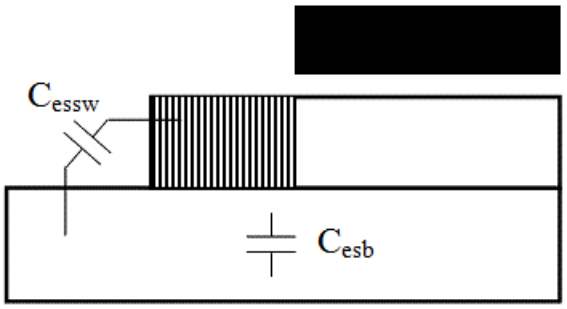
For `capmod=3`, the inversion charge layer thickness is given by:

(29-25)

$$X_{dc} = \frac{ADOS \times 1.9 \times 10^{-9} m}{1 + \left(\frac{V_{gsteff} + 4(VTH0 - VFB - \Phi_s)}{2TOXP} \right)^{0.7 \times BDOS}}$$

Expressions for source/drain-to-gate overlap capacitance and source/drain-to-gate fringing capacitance are taken from BSIM3v3. New SOI-specific parameters added are substrate-to-source sidewall capacitance (C_{esw}), substrate-to-drain sidewall capacitance (C_{edw}), substrate-to-source bottom capacitance (C_{esb}), and substrate-to-drain bottom capacitance (C_{edb}). The following figure shows the BSIMSOI extrinsic charge components.

(29-26)



The substrate-to-source bottom capacitance (per unit source/drain area) C_{esb} is:

© 2023 Cadence Design Systems, Inc.

(29-27)

$$C_{esb} = \begin{cases} C_{box} & if \quad V_{se} < V_{sdfb} \\ C_{box} - \dfrac{1}{A_{sd}}\left(C_{box} - C_{\min}\right)\left(\dfrac{V_{se} - V_{sdfb}}{V_{sdth} - V_{sdfb}}\right)^2 & elseif \quad V_{se} < V_{sdfb} + A_{sd}\left(V_{sdth} - V_{sdfb}\right) \\ C_{\min} - \dfrac{1}{1 - A_{sd}}\left(C_{box} - C_{\min}\right)\left(\dfrac{V_{se} - V_{sdth}}{V_{sdth} - V_{sdfb}}\right)^2 & elseif \quad V_{se} < V_{sdth} \\ C_{\min} & else \end{cases}$$

The sidewall source/drain to substrate capacitance (per unit source/drain perimeter length) $C_{s/d,esw}$ is:

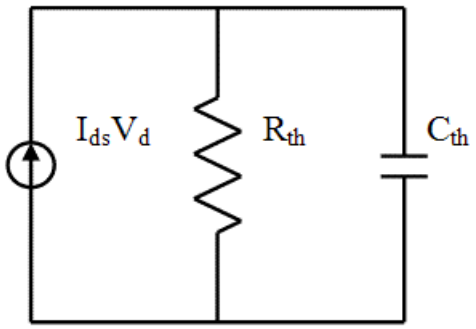
(29-28)

$$C_{s/d,esw} = C_{sdesw} \log\left(1 + \frac{T_{si}}{T_{box}}\right)$$

Selfheating

An equivalent circuit for self-heating simulation is shown below:

(29-29)



BSIMPD models the self-heating by an auxiliary $R_{th}C_{th}$ circuit shown in the figure above. The temperature node (T node) is created in SPICE simulation if the self-heating selector shMod is on and the thermal resistance is non-zero. The T node is treated as a voltage node and is connected to ground through a thermal resistance Rth and a thermal capacitance Cth.

© 2023 Cadence Design Systems, Inc.

(29-30)

$$R_{th} = \frac{R_{th0}}{W_{eff}^{'} + W_{th0}}$$

$$C_{th} = C_{th0}\left(W_{eff}^{'} + W_{th0}\right)$$

where Rth0 and Cth0 are normalized thermal resistance and capacitance respectively. Wth0 is the minimum width for thermal resistance calculation. The current source is driving a current equal to the power dissipated in the device.

(29-31)

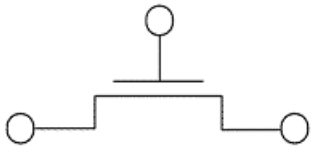
$$P = \left| I_{ds} V_{ds} \right|$$

RF model

BSIMSOI provides the gate resistance model used in RF application. You have the following options for modeling gate electrode resistance (bias independent) and intrinsic-input resistance (R_{ii}, bias-dependent):

(29-32)

RgateMod=0 (zero-resistance)

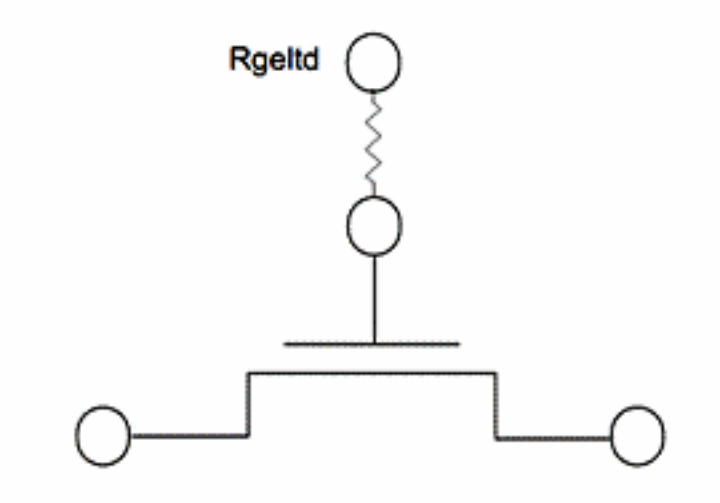


In this case, no gate resistance is generated.

(29-33)

© 2023 Cadence Design Systems, Inc.

RgateMod=1 (constant-resistance)



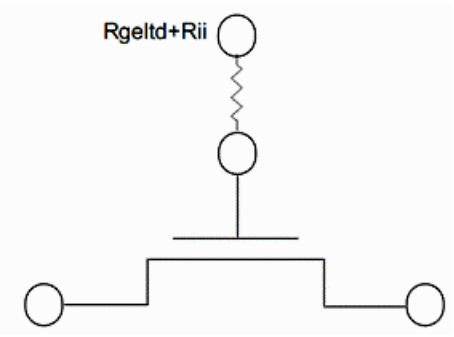
In this case, only electrode gate resistance (bias-independent) is generated by adding an internal gate node. The electrode gate resistance is given by

(29-34)

$$R_{geltd} = \frac{R_{SHG}\left(X_{GW} + \dfrac{W_{eff}}{3N_{GCON} \cdot N_{seg}}\right)}{N_{GCON}\left(L_{drawn} - X_{GL}\right)}$$

(29-35)

RgateMod=2 (R_{ll} model with variable resistance)



The gate resistance here is the sum of the electrode resistance and the intrinsic-input resistance R_{ii}, as given by:

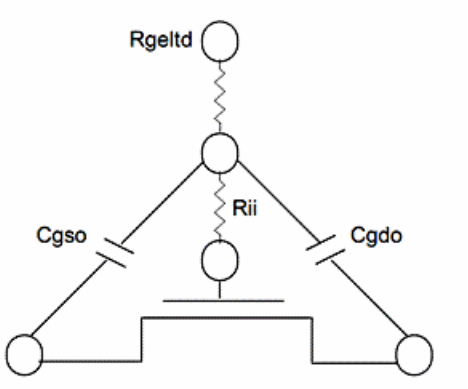
© 2023 Cadence Design Systems, Inc.

(29-36)

$$\frac{1}{R_{ii}} = X_{RGRFG1}\left(\frac{I_{ds}}{V_{dseff}} + X_{RCRG2}\frac{W_{eff}\mu_{eff}C_{oxeff}k_BT}{qL_{eff}}\right)$$

(29-37)

RgateMod=3 (R_{II} model with two nodes)



The gate electrode resistance here is in series with the intrinsic-input resistance R_{ii} through the two internal gate nodes so the overlap capacitance current does not pass through the intrinsic-input resistance.

Noise

In BSIMSOI model, flicker noise and thermal noise models are compatible with BSIM4. Gate tunneling induced shot noise and thermal noise due to gate electrode resistance are also included.

Two flicker noise models are provided in BSIMSOI model:

(29-38)

fnoiMod=0

$$S_{id}(f) = \left(\frac{W_{eff}}{W_{0FLK}}\right)^{1-af}\frac{K_f I_{ds}^{af}}{C_{oxe}L_{eff}^{2}f^{ef}}$$

© 2023 Cadence Design Systems, Inc.

(29-39)

fnoiMod=1

The noise density in inversion region is given by:

$$S_{id,inv}(f)=\frac{k_B T q^2 \mu_{eff} I_{ds}}{C_{oxe} {L_{eff}}^2 A_{bulk} f^{ef} \cdot 10^{10}}\left(Noia\left(\frac{N_0+N^*}{N_l+N^*}\right)+Noib(N_0-N_l)+\frac{Noic}{2}\left({N_0}^2-{N_l}^2\right)\right)$$
$$+\frac{k_B T \cdot {I_{ds}}^2 \Delta L_{clm}}{W_{eff} {L_{eff}}^2 f^{ef} \cdot 10^{10}}\frac{Noia+Noib \cdot N_l+Noic \cdot {N_l}^2}{\left(N_l+N^*\right)^2}$$

The noise density in subthreshold region is given by:

(29-40)

$$S_{id,subV_t}(f)=\frac{Noia \cdot k_B T \cdot {I_{ds}}^2}{W_{eff} L_{eff} f^{ef} \left(N^*\right)^2 \cdot 10^{10}}$$

The total flicker noise density is:

(29-41)

$$S_{id}(f)=\frac{S_{id,inv}(f) \times S_{id,subV_t}(f)}{S_{id,inv}(f)+S_{id,subV_t}(f)}$$

Following thermal noise models are provided in BSIMSOI model:

(29-42)

tnoiMod=0

$$\overline{{i_d}^2}=\frac{4k_B T \Delta f}{R_{ds}+\frac{{L_{eff}}^2}{\mu_{eff}\left|Q_{inv}\right|}}N_{tnoi}$$

(29-43)

© 2023 Cadence Design Systems, Inc.

tnoiMod=1

The noise voltage source partitioned to the source side is given by:

$$\overline{v_d^{\,2}} = 4k_B T \cdot \theta_{tnoi}^{\,2} \frac{V_{dseff}\,\Delta f}{I_{ds}}$$

The noise current source put in the channel region with gate and body amplification is given by:

(29-44)

$$\overline{i_d^{\,2}} = 4k_B T \frac{V_{dseff}\,\Delta f}{I_{ds}} \left(G_{ds} + \beta_{tnoi}\left(G_m + G_{mbs}\right)\right)^2 - \overline{v_d^{\,2}}\left(G_{ds} + G_m + G_{mbs}\right)^2$$

The junction currents (I_{bs}, I_{bd}) for shot noise(`fb_ibs`, `fb_ibd`) are given by:

(29-45)

$$\overrightarrow{I_{bs}^{2}} = 2qI_{bs} = 2q(I_{bs1} + I_{bs2} + I_{bs3} + I_{bs4})$$
$$\overrightarrow{I_{bd}^{2}} = 2qI_{bd} = 2q(I_{bd1} + I_{bd2} + I_{bd3} + I_{bd4})$$

(29-46)

tnoimod=2 (SPICE2 model)

$$\overline{i_d^{\,2}} = \frac{8k_B T\Delta f}{3} \cdot NTNOI \cdot (G_m + G_{mbs} + G_{ds})$$

The `NTNOI` parameter provides the flexibility to tune the magnitude of noise density.

tnoimod=3

In this noise model, noise for both gate and drain is implemented as current noise sources. The drain current noise flows from drain to source, whereas the induced gate current noise flows from gate to source and drain. The correlatoin between the two noise sources can be tuned with the parameter RNOIC.

© 2023 Cadence Design Systems, Inc.

(29-47)

$$V_b = \frac{V_{gsteff} + 2v_t}{A_{bulk}}$$

$$\eta = 1 - \frac{V_{dseff}}{V_b}$$

$$L_{vsat} = L_{eff} \cdot \left[1 + \frac{V_{dseff}}{E_{sat} L_{eff}}\right]$$

$$\alpha = A_{bulk}$$

$$\gamma = \frac{L}{L_{vsat}} \left[\frac{1+\eta}{2} + \frac{(1-\eta)^2}{6\left[(1+\eta) + \frac{2V_t\alpha}{V_{gsteff}}\right]}\right]$$

$$\delta = \frac{1}{6}\left(\frac{L_{vsat}}{L}\right)^3 \left[\frac{1+\eta}{\left[(1+\eta) + \frac{2\alpha V_t}{V_{gsteff}}\right]^2} - \frac{\left[6(1+\eta) + \frac{2\alpha V_t}{V_{gsteff}}\right](1-\eta)^2}{15\left[(1+\eta) + \frac{2\alpha V_t}{V_{gsteff}}\right]^4} + \frac{(1-\eta)^4}{9\left[(1+\eta) + \frac{2\alpha V_t}{V_{gsteff}}\right]^5}\right]$$

$$\epsilon = \frac{1}{6} \cdot \frac{L_{vsat}}{L} \left[\frac{1-\eta}{\left[(1+\eta) + \frac{2\alpha V_t}{V_{gsteff}}\right]} + \frac{(1-\eta)^3}{3\left[(1+\eta) + \frac{2\alpha V_t}{V_{gsteff}}\right]^3}\right]$$

$$n_c = RNOIC.\left[1 + TNOIC.\ L_{eff}.\left(\frac{V_{gsteff}}{E_{sat} L_{eff}}\right)^2\right]$$

$$c_{tnoi} = \frac{\epsilon}{\sqrt{\gamma.\delta}}.\left(\frac{n_c}{0.395}\right)$$

$$n_\beta = RNOIA.\left[1 + TNOIA.\ L_{eff}.\left(\frac{V_{gsteff}}{E_{sat} L_{eff}}\right)^2\right]$$

© 2023 Cadence Design Systems, Inc.

$$n_\theta = RNOIB.\left[1 + TNOIB.\ L_{eff}.\left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right]$$

$$g_{d0} = NF \times \frac{\mu_{eff}C_{oxeff}\frac{W_{eff}}{L_{eff}}V_{gsteff}}{1 + gche \cdot R_{ds}}$$

$$S_{id} = 4kT.\gamma.(3n_\beta{}^2)\,g_{d0}$$

$$C_0 = NF \times C_{oxeff}W_{eff,CV}L_{eff,CV}$$

$$sf = \frac{g_{d0}}{\sqrt{\delta \times 3.75 \times n_\theta{}^2 / \gamma}}$$

$$I(di,si) <+\ white_noise\left(S_{id} \times |1 - c_{tnoi}{}^2|\right)$$

$$I(N) <+\ V(N) \times sf \times SCALEN$$

$$I(N) <+ white_noise\left(\frac{S_{id}}{sf^2 \times SCALEN^2}\right)$$

$$I(di,si) <+\ c_{tnoi} \times V(N) \times sf \times SCALEN$$

$$I(gi,si) <+\ ddt\left(0.5 \times C_0 \times SCALEN \times V(N)\right)$$

$$I(gi,di) <+\ ddt\left(0.5 \times C_0 \times SCALEN \times V(N)\right)$$

Related Topics

BSIMSOI MOSFET Model (bsimsoi)

Device Structure

Equivalent Circuit

Device Regions

© 2023 Cadence Design Systems, Inc.

Global Control Options

Model Version Updates

Model Usage

Component Statements

Model Version Updates

Version 3.2

1. Add model selector “soimod”. “soimod” will determine the operation of BSIMSOI: If soimod=0 (default), the model equation is identical to the BSIMPD equation; if soimod=1 the model equation is an unified model for PD FD; if soimod=2, the model equation is identical to the BSIMFD equation
2. Implements a flicker noise and thermal noise model compatible with BSIM4 has been. In addition, the new noise model includes gate tunneling-induced shot noise and thermal noise due to gate electrode resistance.

Version 4.0

1. A scalable stress effect model for process induced stress effect, device performance becoming thus a function of the active area geometry and the location of the device in the active area;
2. Asymmetric current/capacitance model S/D diode and asymmetric S/D resistance;
3. Improved GIDL model with BSIM4 GIDL compatibility;
4. Noise model Improvements;
   - Improved width/length dependence on flicker noise
   - SPICE2 thermal noise model is introduced as TNOIMOD=2 with parameter NTNOI that adjusts the magnitude of the noise density
   - Body contact resistance induced thermal noise
   - Thermal noise induced by the body resistance network
   - Shot noises induced by Ibs and Ibd separated
5. A two resistance body resistance network introduced for RF simulation;

© 2023 Cadence Design Systems, Inc.

6. Threshold voltage model enhancement;
   - Long channel DIBL effect model added
   - Channel-length dependence of body effect improved
7. Drain induced threshold shift (DITS) model introduced in output conductance;
8. Improved model accuracy in moderate inversion region with BSIM4 compatible Vgsteff;
9. Multi-finger device with instance parameter NF;
10. A new instance parameter AGBCPD to improve gate current for body contact;
11. A new instance parameter DELVTO representing threshold voltage variation;
12. FRBODY is both instance/model parameters.

Version 4.1

1. New Material Model
2. New Mobility Model for High k Material
3. New GIDL/GISL Model
4. New Impact Ionization Current Model
5. New Body Contact Model
6. New DITS Model
7. Improved VgsteffCV model
8. Improved Built Improved Built-in Potential Lowering (?Vbi) Model

Version 4.2

1. No new features are added in this version.
2. Bug-fix for charge and capacitance
3. Bug-fix for gate to bulk tunneling current “Igb” calculation
4. Bug-fix for vgsteff derivative calculation.

© 2023 Cadence Design Systems, Inc.

Version 4.3

1. No new features are added in this version.
2. Bug-fix for temperature derivative calculation with selfheating.
3. Bug-fix for dc swapping issue.
4. Bug-fix for Abulk discontinuity issue.
5. Bug-fix for vgst, vfbeff, vfbeff2, vgsteff, vgsteff 2, Qs2 and I_{ii} derivative calculation.
6. Bug-fix for missing number of finger in some calculation.
7. Add source and drain edge components of Gate-source, Gate-drain diffusion tunneling currents.
8. I_{gisl} and I_{gidl} current formulations revised for continuity and consistency.

Version 4.31

1. No new features are added in this version.
2. Bug-fix for new material model
3. Bug-fix for missing number of finger in Ig_agbcp2 current.
4. Bug-fix for Igcs/Igcd derivative calculation.

Version 4.4

1. Extensive derivative fixes for SOIMOD=1 and 2 are provided
2. A new sidewall fringe capacitance model parameter `cfrcoeff` is added.
3. Limiting for peak channel doping concentration parameter `nch` when soimod=2.

Version 4.5

1. Support added for correlated thermal noise at `tnoimod=3`.
2. `dc` and `ac` DIBL parameters have been decoupled
3. New model parameters `EGGBCP2`, `EGGDEP`, `AGB1`, `BGB1`, `AGB2`, `BGB2`, `AGBC2N`, `AGBC2P`, `BGBC2N`, `BGBC2P`, and `VTM00` have been added.

© 2023 Cadence Design Systems, Inc.

4. The source/drain conductance is now set to `1.0e3` instead of 0 when the value of `NRS` and `NRD` is 0.
5. Inconsistency in drain current when selfheating is on has been addressed.
6. `GISL/GIDL` model for `gidlMod=0` and `gidlMod=1`has been modified.
7. In `capmod=3`, XDC calculation has been modified.
8. `pwr` is now positive in `white_noise(pwr,name)` in the thermal noise model implementation.
9. `NTNOI` and `NOIF` parameters are now limited to positive values only.
10. Thermal noise contribution due to `rbody` has been included.
11. Calculation of A_{bulk} has been updated to avoid non-monotonic behavior at high body bias.
12. Some bugs have been fixed.

Version 4.6.0

1. Added identifying names to all noise sources.
2. Support added for node collapsing difference between C code and Verilog-A code for SOIMOD=2 4.
3. Binning parameter for Npeak.
4. Improved implementation of source/drain resistance when `RSH=0` to speed up simulation.
5. Introduced parameters for better fitting accuracy when using `MTRLMOD=0` (body contacted device).
6. Use of Clamped log function.
7. Proper units and ranges are set for parameters.
8. Improved the clamped log function efficiency.
9. Modified gate charge and capacitance calculations to include overlap charge.
10. Binning of Built-In Potential Lowering (ÄVbi) Model Parameters.
11. Output variables added for self-heating mode.
12. Some bugs have been fixed.

© 2023 Cadence Design Systems, Inc.

Version 4.6.1

1. Support added for SHMOD as both model/instance parameter for backward compatibility.

Special Bugfixes

Rth thermal resistance

R_{th} is the thermal resistance of one device and should be the total resistance of the shunt connected fingers.

UC Berkeley

```
Rth = Rth0 / (Weff + Wth0) * Nseg;
```

Cadence

```
Rth = Rth0 / (NF* (Weff + Wth0)) * Nseg;
```

It is fixed in MMSIM611_ISR16

Cth thermal capacity

C_{th} is the thermal capacity of one device and should be the total resistance of the shunt connected fingers.

UC Berkeley

```
    Cth = Cth0 * (Weff + Wth0) / Nseg;
```

Cadence

```
Cth = Cth0 * (NF* (Weff + Wth0)) / Nseg;
```

It is fixed in MMSIM611_ISR16

ExpVgst bug handling

In the original BSIMSOI model, ExpVgst was multiplied by itself by a mistake when calculate the effective Vgst for charge model. To fix this issue UC Berkeley added Vgstcvmod flag in BSIMSOI 4.1

`Vgstcvmod=0`: keep the bug (Cadence fixed it for version > 4.0)

`Vgstcvmod=1`: the bug fixed in UC Berkeley code

© 2023 Cadence Design Systems, Inc.

Vgstcvmod=2: New charge model (introduced in 4.1)

It is released in MMSIM711 with BSIMSOI version 4.1. The default value of Vgstcvmod is 0.

In BSIMSOI version 4.2 released in MMSIM72, the default value of $V_{gstcvmod}$ is changed to 1.

Temperature node tolerance and quantity

Spectre supports handling different node behavior and temperature node property should be different from electric node. BSIMSOI temperature node is not properly implemented in Spectre which may cause convergence issue.

It is fixed in MMSIM711_ISR6 (April, 2009)

I_{ii} (substrate current)

I_{ii} is the impact ionization current from channel to bulk body for one finger and should multiply with number of ginger to get the total impact ionization current. Cadence fixed it as I_{ii} * NF

It is fixed in MMSIM72 base release with BSIMSOI version 4.2.

Bugfix control methodology

Spectre BSIMSOI model introduced a new methodology to control all bugfix Cadence did. A new model flag parameter "bugfix_selector" was add to BSIMSOI model to control the special bugfix cadence did in BSIMSOI model. It is an unsigned int. Every bit of its binary format controls one bugfix. With this methodology, every bugfix can be turned on or off independently.

Currently, there are three bugfixes are controlled:

1. Bit0 for bugfix of double ExpVgst when VgstcvMod = 0. (Version != 4.01)
2. Bit1 for bugfix of Vgsteff derivative when VgstcvMod = 0. (Version >= 3.2)

Bit2 for bugfix of channel thermal noise when nf > 1. (Version < 4.31)

© 2023 Cadence Design Systems, Inc.

That means:

bugfix_selecor		Bugfix list		
Value in base 10	Value in base 2	a	b	c
0	0000-0000-0000-0000	×	×	×
1	0000-0000-0000-0001	●	×	×
2	0000-0000-0000-0010	×	●	×
3	0000-0000-0000-0011	●	●	×
4	0000-0000-0000-0100	×	×	●
5	0000-0000-0000-0101	●	×	●
6	0000-0000-0000-0110	×	●	●
7	0000-0000-0000-0111	●	●	●
8	0000-0000-0000-1000	×	×	×
…	…	…	…	…

TMI Support

Starting with the SPECTRE 17.1 release, support for the TMI model has been added in the BSIMSOI model. TMI is a modeling application programming interface (API) that supports extensions of standard compact models.

TMI provides an alternative approach to support model equations for advanced technologies in addition to adding more macro models. It provides good flexibility as macro model and good simulation efficiency as built-in standard model at the same time.

To use the TMI for the BSIMSOI model, you need to correctly set the TMI options and parameters. For more information on TMI options and parameters, refer to the TMI documentation.

Related Topics

BSIMSOI MOSFET Model (bsimsoi)

Device Structure

Equivalent Circuit

© 2023 Cadence Design Systems, Inc.

Device Regions

Global Control Options

Model Equations

Model Usage

Component Statements

Model Usage

Instance Syntax

BSIMSOI instances can have 4 to 7 terminals: drain (d), gate (g) source (s), back-gate (e), external-bulk (p), bulk (b), and temperature node (t). When more than 4 terminals are given, instance parameter “tnodeout” is specified, the last terminal is interpreted as temperature terminal. All the possible terminal connects are follows:

- `InstanceName d g s eModelName parameter=value`
- `InstanceName d g s e [p]ModelName parameter=value`
- `InstanceName d g s e [p b]ModelName parameter=value`
- `InstanceName d g s e [p b t]ModelName parameter=value`
- `InstanceName d g s e [t]ModelName tnodeout=1 parameter=value`
- `InstanceName d g s e [p t]ModelName tnodeout=1 parameter=value`
- `InstanceName d g s e [p b t]ModelName tnodeout=1 parameter=value`

To specify BSIMSOI instance element, the ModelName has to be associated with a BSIMSOI model card.

Sample Instance Statement

```
MN1 (Vd Vg Vs Ve ) nmos_soi1  l=1e-6 w=5e-6
```

Model Syntax

The following syntax specified BSIMSOI model:

© 2023 Cadence Design Systems, Inc.

```
model ModelName bsimsoi parameter=value ...
```

The third parameter, `bsimsoi`, is the master to indicate this model is a BSIMSOI model card.

Sample Model Statement

```
model bsimsoi_nmos1 bsimsoi type=n version=4.0 tnom=25 tox=3.0e-9 tsi=41e-9
tbox=100e-9 toxm=3.0e-9 vth0=0.29 nch=4e17 nsub=1e16 rbody=0 rbsh=0
```

Related Topics

BSIMSOI MOSFET Model (bsimsoi)

Device Structure

Equivalent Circuit

Device Regions

Global Control Options

Model Equations

Model Version Updates

Component Statements

Component Statements

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

w	(m)	Channel width(alias=lv2).
l	(m)	Channel length(alias=lv1).
nf	1.0	Number of fingers.
as	(m^2)	Area of source diffusion(alias=lv4).
ad	(m^2)	Area of drain diffusion(alias=lv3).
ps	(m)	Perimeter of source diffusion(alias=lv12).
pd	(m)	Perimeter of drain diffusion(alias=lv11).
nrd	(m/m)	Number of squares of drain diffusion.
nrs	(m/m)	Number of squares of source diffusion.
nrb	(m/m)	Number of body squares.
nbc	0 m/m	Number of body contact isolation edge.
nseg	1 m/m	Number of segments for channel width partitioning.
pdbcp	0 m	Perimeter length for body contact parasitic at drain.
psbcp	0 m	Perimeter length for body contact parasitic at source.
agbcp	0 m^2	Gate to body overlap area for body contact parasitic.
aebcp	0 m^2	Substrate to body overlap area for body contact parasitic.
m	1	Multiplicity factor (number of MOSFETs in parallel).

© 2023 Cadence Design Systems, Inc.

soimod	0	SOI model selector. SoiMod=0:PD module. SoiMod=1: DD module. SoiMod=2: FD module.
rgatemod		Rgate flag (available from Version 3.1).
rbodymod		Body R model selector.
tnodeout		Temperature node flag associated with T node(Given or NOT Given).
isnoisy	yes	Should device generate noise.Possible values are no and yes.
region	triode	Estimated operating region.Possible values are off, triode, sat and subth.
rth0	((m C)/w)	Thermal resistance.
cth0	(w s/(m C))	Thermal capacitance.
bjtoff	0	BJT off flag.
vbsusr	0 V	Optional initial value of Vbs for transient.
frbody	1	Layout dependent body-resistance coefficient.
sa	0 m	Distance between OD edge and poly from one side.
sb	0 m	Distance between OD edge and poly from the other side.
sd	0 m	Distance between neighbor fingers.
rbdb	(Ω)	Body resistance.
rbsb	(Ω)	Body resistance.

© 2023 Cadence Design Systems, Inc.

agbcpd	agbcp m^2	Gate to body overlap area for bc parasitics in DC.
agbcp2	0 m^2	Parasitic gate to body overlap area for bc parasitics.
delvto	0 V	Zero bias threshold voltage variation.
trise	(C)	Temperature rise from ambient.
shmod	0	Self heating mode selector.

Note:

1. tnodeout is a flag parameter of instance. If it is specified and the instance has more than 4 terminals, then the last terminal is interpreted as temperature node. tnodeout=1 indicates that tnodeout is specified in instance statement and it will treat the last terminal as temperature terminal.
2. region can set the initial device work state for simulator, a correct region value can help simulator converge faster but will not effect the final result.

© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type *parameters*

type	n	Transistor type.Possible values are n and p.
version	3.0	Model parameter "version" only accepts a real number value, like 2.23 for version=2.2.3. The available versions are 2.23(2.2.3), 3.0, 3.11(3.1.1), 3.2, 4.0, 4.1, 4.2, 4.3, 4.31(4.3.1), 4.4, 4.5, 4.6 and 4.6.1..
binunit	1	Bin parameter unit selector. 1 for microns and 2 for meters.
cdnver	1	Cadence version selector.
soimod	0	SOI model selector. SoiMod=0: PD module. SoiMod=1: DD module. SoiMod=2: FD module.
mtrlmod	0	Parameter for non-silicon substrate or metal gate selector.
mobmod	1	Mobility model selector.
fdmod	0	Improved dVbi model selector.
gidlmod	0	Parameter for GIDL selector.
gatetype	h	Gate structure type selector.Possible values are h and non_h.
capmod	2	Intrinsic charge model.
vgstcvmod	0	Improved VgsteffCV selector.
igmod	0	Gate tunneling current model selector.
igbmod	0	Gate-body tunneling current model selector.

© 2023 Cadence Design Systems, Inc.

igcmod	0	Gate-channel tunneling current model selector.
iiimod	0	Parameter for Iii selector.
rbodymod	0	Body R model selector.
rdsmod	0	Bias-dependent S/D resistance model selector.
rgatemod	0	Rgate flag.
shmod	0	Self-heating selector.
tlev	0	DC temperature selector.
tlevc	0	AC temperature selector.
noimod	1	Noise model selector.
fnoimod	1	Flicker Noise model selector.
tnoimod	0	Thermal Noise model selector.

© 2023 Cadence Design Systems, Inc.

Process *parameters*

nsub	6e16 cm^{-3}	Substrate doping concentration.
nch	1.7e17 cm^{-3}	Peak channel doping concentration.
ngate	0 cm^{-3}	Poly-gate doping concentration.
nsd	1.0e20 cm^{-3}	S/D doping concentration.
xj	0.15e-6 m	Source/drain junction depth.
tsi	1e-7 m	Silicon film thickness.
etsi	1e-7 m	Effective Silicon-on-insulator thickness in meters.
tbox	3e-7 m	Buried oxide thickness.
tox	1e-8 m	Gate oxide thickness.
toxm	(m)	Gate oxide thickness used in extraction.
toxp	tox	Physical gate oxide thickness.
xt	1.55e-7 m	Doping depth.
rdsw	100 Ω µm^wr	Width dependence of drain-source resistance.
prwb	0 1/V	Body-effect coefficient for Rds.
prwg	0 1/V	Gate-effect coefficient for Rds.
wr	1	Width offset for parasitic resistance.

© 2023 Cadence Design Systems, Inc.

dwg	0 m/V	Gate-bias dependence of channel width.
dwb	0 m/V	Body-bias dependence of channel width.
dwbc	0 m	Width offset for body contact isolation edge.
lint	0 m	Lateral diffusion for one side.
wint	0 m	Width reduction for one side.
ll	0 m^lln	Length dependence of delta L.
lln	1	Length exponent of delta L.
llc	0 m^lln	Length dependence of delta LC.
lwc	0 m^wln	Width dependence of delta LC.
lwlc	0 m^(lln+lwn)	Area dependence of delta LC.
lw	0 m^lwn	Width dependence of delta L.
lwn	1	Width exponent of delta L.
lwl	0 m^(lln+lwn)	Area dependence of delta L.
wl	0 m^wln	Length dependence of delta W.
wlc	0 m^wln	Length dependence of delta WC.
wwc	0 m^wwn	Width dependence of delta WC.
wwlc	0 m^(wwn+wln)	Area dependence of delta WC.

© 2023 Cadence Design Systems, Inc.

wln	1	Length exponent of delta W.
ww	0 m^wwn	Width dependence of delta W.
wwn	1	Width exponent of delta W.
wwl	0 m^(wwn+wln)	Area dependence of delta W.
xl	0 m	Length variation due to masking and etching.
xw	0 m	Width variation due to masking and etching.

© 2023 Cadence Design Systems, Inc.

Material model *parameters*

eot	100.0e-10 m	Effective SiO2 thickness.
epsrox	3.9	Dielectric constant of the gate oxide relative to vacuum.
epsrsub	11.7	Dielectric constant of substrate relative to vacuum.
ni0sub	1.45e10 cm^{-3}	Intrinsic carrier concentration of substrate at Tnom.
bg0sub	1.16 eV	Band-gap of substrate at T=0K.
tbgasub	7.02e-4 V/K	First parameter of band-gap change due to temperature.
tbgbsub	1108.0 K	Second parameter of band-gap change due to temperature.
phig	4.05 eV	Work function of gate.
easub	4.05 eV	Electron affinity of substrate.
leffeot	1.0 µm	Effective length for extraction of EOT.
weffeot	10.0 µm	Effective width for extraction of EOT.
vddeot	1.5 V	Voltage for extraction of EOT.
tempeot	300.15 K	Temperature for extraction of EOT.
ados	1.0	Charge centroid parameter.
bdos	1.0	Charge centroid parameter.
epsrgate	11.7	Dielectric constant of gate relative to vacuum.

© 2023 Cadence Design Systems, Inc.

Threshold voltage *parameters*

vtho	(V)	Threshold voltage at zero body bias for long-channel devices. For enhancement-mode devices, vtho > 0 for n-channel and vth < 0 for p-channel. Default value is calculated from other model parameters.
k1	0.53 V	Body-effect coefficient.
k1w1	0 m	First body effect width dependent parameter.
k1w2	0 m	Second body effect width dependent parameter.
k2	-0.0186	Charge-sharing parameter.
k3	0	Narrow width coefficient.
k3b	0 1/V	Narrow width coefficient.
w0	2.5e-6 m	Narrow width coefficient.
lpe0	1.74e-7 m	Lateral non-uniform doping coefficient.
nlx	1.74e-7 m	Lateral non-uniform doping coefficient.
lpeb	0 m	Lateral non-uniform doping effect for body bias.
dvt0	2.2	First coefficient of short-channel effects.
dvt1	0.53	Second coefficient of short-channel effects.
dvt2	-0.032 1/V	Body-bias coefficient of short-channel effects.
dvt0w	0	First coefficient of narrow-width effects.
dvt1w	5.3e6	Second coefficient of narrow-width effects.

© 2023 Cadence Design Systems, Inc.

dvt2w	-0.032 1/V	Body-bias coefficient of narrow-width effects.
vbx	0 V	Threshold voltage transition body voltage.
vbm	-3 V	Maximum applied body voltage.
vfb	-1.0 V	Flat Band Voltage.
a0	1	Non-uniform depletion width effect coefficient.
b0	0 m	Bulk charge coefficient due to narrow width effect.
b1	0 m	Bulk charge coefficient due to narrow width effect.
a1	0	Non-saturation coefficient.
a2	1	Non-saturation coefficient.
ags	0 1/V	Gate-bias dependence of abulk.
keta	-0.6 1/V	Body-bias coefficient for non-uniform depletion width effect.
ketas	0 V	Surface potential adjustment for bulk charge effect.
dvtp0	0 m	First parameter for Vth shift due to pocket.
dvtp1	0 1/V	Second parameter for Vth shift due to pocket.
dvtp2	0	Third parameter for Vth shift due to pocket.
dvtp3	0	Fourth parameter for Vth shift due to pocket.
dvtp4	0	Fifth parameter for Vth shift due to pocket.
minv	0	Parameter for moderate inversion in Vgsteff.

© 2023 Cadence Design Systems, Inc.

pdits	1e-20 1/V	Coefficient for drain-induced Vth shifts.
pditsl	0 1/m	Length dependence of drain-induced Vth shifts.
pditsd	0 1/V	Vds dependence of drain-induced Vth shifts.
gamma1	0 $\sqrt{V}$	Body-effect coefficient near the surface.
gamma2	0 $\sqrt{V}$	Body-effect coefficient in the bulk.

© 2023 Cadence Design Systems, Inc.

Mobility *parameters*

u0	670 $cm^2/V\ s$	Low-field surface mobility at tnom. Default is 250 for PMOS.
vsat	8e4 m/s	Carrier saturation velocity at tnom.
ua	2.25e-9 m/V	First-order mobility reduction coefficient.
ub	5.87e-19 m^2/V^2	Second-order mobility reduction coefficient.
uc	-4.65e-11 m/V^2	Body-bias dependence of mobility. Default is -0.046 and unit is 1/V for mobmod=3.
ud	0 $/m^2$	Coulomb scattering factor of mobility.
eu	1.67	Mobility exponent.
ucs	1.67	Mobility exponent.

Subthreshold *parameters*

cdsc	2.4e-4 F/m^2	Source/drain and channel coupling capacitance.
cdscb	0 F/m^2 V	Body-bias dependence of cdsc.
cdscd	0 F/m^2 V	Drain-bias dependence of cdsc.
nfactor	1	Subthreshold swing coefficient.
cit	0 F/m^2	Interface trap parameter for subthreshold swing.
voff	-0.08 V	Threshold voltage offset.

© 2023 Cadence Design Systems, Inc.

`noff`	`1.0 1/V`	C-V turn-on/off parameter.
`dsub`	`drout`	DIBL effect in subthreshold region.
`eta0`	`0.08`	DIBL coefficient subthreshold region.
`etab`	`-0.07 1/V`	Body-bias dependence of `et0`.

© 2023 Cadence Design Systems, Inc.

Output resistance *parameters*

drout	0.56	DIBL effect on output resistance coefficient.
fprout	0 V/m	Rout degradation coefficient for pocket devices.
pclm	1.3	Channel length modulation coefficient.
pdiblc1	0.39	First coefficient of drain-induced barrier lowering.
pdiblc2	8.6e-3	Second coefficient of drain-induced barrier lowering.
pdiblcb	0 1/V	Body-effect coefficient for DIBL.
pvag	0	Gate dependence of early voltage.
delta	0.01 V	Effective drain voltage smoothing parameter.

Substrate current *parameters*

alpha0	0 m/V	Substrate current impact ionization coefficient.
beta0	0 1/V	First Vds dependent parameter of impact ionization current.
fbjtii	0	Fraction of bipolar current affecting the impact ionization.
beta1	0	Second Vds dependent parameter of impact ionization current.
beta2	0.1 V	Third Vds dependent parameter of impact ionization current.
vdsatii0	0.9 V	Nominal drain saturation voltage at threshold for impact ionization current.

© 2023 Cadence Design Systems, Inc.

vbci	0 V	Internal B-C built-in potential.
tii	0	Temperature dependent parameter for impact ionization current.
lii	0	Channel length dependent parameter at threshold for impact ionization current.
esatii	1e7 V/m	Saturation channel electric field for impact ionization current.
sii0	0.5 1/V	First Vgs dependent parameter for impact ionization current.
sii1	0.1 1/V	Second Vgs dependent parameter for impact ionization current.
sii2	0 1/V	Third Vgs dependent parameter for impact ionization current.
siid	0 1/V	Vds dependent parameter of drain saturation voltage for impact ionization current.
ebjtii	0 1/V	Impact ionization parameter for BJT part.
cbjtii	0 1/m/V	Length scaling parameter for II BJT part.
abjtii	0	Exponent factor for avalanche current.
mbjtii	0.4	Internal B-C grading coefficient.

© 2023 Cadence Design Systems, Inc.

SOI specific *parameters*

ngidl	1.2 V	GIDL Vds enhancement coefficient.
egidl	1.2 V	GIDL first parameter.
agidl	0 S	GIDL constant.
bgidl	0 V/m	GIDL exponential coefficient.
cgidl	0 V^3	GIDL vb parameter.
rgidl	1.0 1/V	GIDL vg parameter.
kgidl	0 1/V	GIDL vb parameter.
fgidl	0 V	GIDL vb parameter.
egisl	egidl	GISL first parameter.
agisl	agidl	GISL constant.
bgisl	bgidl	GISL exponential coefficient.
cgisl	cgidl	GISL vb parameter.
rgisl	Rgidl	GISL vg parameter.
kgisl	kgidl	GISL vb parameter.
fgisl	fgidl	GISL vb parameter.
ntun	10	Reverse tunneling non-ideality factor.
ntund	ntun	Reverse tunneling non-ideality factor.
ndioded	ndiode	Diode non-ideality factor.
nrecf0	2.0	Recombination non-ideality factor at forward bias.

© 2023 Cadence Design Systems, Inc.

nrecr0	10	Recombination non-ideality factor at reverse bias.
nrecf0d	nrecf0	Recombination non-ideality factor at forward bias.
nrecr0d	nrecr0	Recombination non-ideality factor at reverse bias.
isbjt	1e-6 A/m^2	BJT saturation current.
isdif	0 A/m^2	Diffusion saturation current.
isrec	1e-5 A/m^2	Recombination saturation current.
istun	0 A/m^2	Tunneling saturation current.
idbjt	isbjt A/m^2	BJT injection saturation current.
iddif	isdif A/m^2	Body to source/drain injection saturation current.
idrec	isrec A/m^2	Recombination saturation current.
idtun	idtun A/m^2	Tunneling saturation current.
ln	2e-6 m	Electron diffusion length.
vrec0	0 V	Voltage dependent parameter for recombination current.
vtun0	0 V	Voltage dependent parameter for tunneling current.
vrec0d	vrec0 V	Voltage dependent parameter for recombination current.
vtun0d	vtun0 V	Voltage dependent parameter for tunneling current.

© 2023 Cadence Design Systems, Inc.

nbjt	1	Power coefficient of channel length dependency for bipolar current.
lbjt0	0.20e-6 m	Reference channel length for bipolar current.
vabjt	10 V	Early voltage for bipolar current.
aely	0 V/m	Channel length dependency of early voltage for bipolar current.
ahli	0	High level injection parameter for bipolar current.
ahlid	ahli	High level injection parameter for bipolar current.
ndiode	1	Diode non-ideality factor.
vbsa	0 V	Non-ideal offset voltage.
nofffd	1.0	Smooth parameter in FD module.
vofffd	0	Smooth parameter in FD module.
k1b	1.0	First backgate body effect parameter.
k2b	0	Second backgate body effect parameter for short channel effect.
dk2b	0	Third backgate body effect parameter for short channel effect.
dvbd0	0	First short-channel effect parameter in FD module.
dvbd1	0	Second short-channel effect parameter in FD module.
moinfd	1.0e3	Gate bias dependence coefficient of surface potential.

© 2023 Cadence Design Systems, Inc.

vbs0pd	0 V	Upper bound of built-in potential lowering for PD operation.
vbs0fd	0.5 V	Lower bound of built-in potential lowering for FD operation.

© 2023 Cadence Design Systems, Inc.

Parasitic resistance *parameters*

rbody	0 Ω	Body resistance.
rbsh	0 Ω	Extrinsic body contact sheet resistance.
rsh	0 Ω/sqr	Source/drain diffusion sheet resistance.
rs	0 Ω	Source resistance.
rd	0 Ω	Drain resistance.
rsc	0 Ω	Source contact resistance.
rdc	0 Ω	Drain contact resistance.
rsw	50 Ω	Source resistance per width.
rdw	50 Ω	Drain resistance per width.
rswmin	0 Ω	Source resistance per width at high Vg.
rdwmin	0 Ω	Drain resistance per width at high Vg.
rss	0 Ω m	Scalable source resistance.
rdd	0 Ω m	Scalable drain resistance.
rhalo	1.0e15 Ω/sqr	Body halo sheet resistance.
frbody	1	Layout dependent body-resistance coefficient.
minr	0.1 Ω	Minimum source/drain resistance.
hdif	0 m	Length of heavily doped diffusion.
ldif	0 m	Lateral diffusion beyond the gate.

© 2023 Cadence Design Systems, Inc.

Gate tunneling *parameters*

ntox	1.0	Power term of gate current.
toxqm	Tox m	Effective oxide thickness considering quantum effects.
toxref	2.5e-9 m	Target oxide thickness.
ebg	1.2 V	Effective bandgap in gate current calculation.
alphagb1	0.35	First Vox dependent parameter for gate current in inversion.
betagb1	0.03	Second Vox dependent parameter for gate current in inversion.
vgb1	300	Third Vox dependent parameter for gate current in inversion.
vevb	0.075	Vaux parameter for valence-band electron tunneling.
nevb	3.0	Valence-band electron non-ideality factor.
alphagb2	0.43	First Vox dependent parameter for gate current in accumulation.
betagb2	0.05	Second Vox dependent parameter for gate current in accumulation.
vgb2	17	Third Vox dependent parameter for gate current in accumulation.
vecb	0.026	Vaux parameters for conduction-band electron tunneling.
necb	1.0	Conduction-band electron non-ideality factor.
aigc	0.43	Parameter for Igc.

© 2023 Cadence Design Systems, Inc.

bigc	0.054	Parameter for Igc.
cigc	0.075 1/V	Parameter for Igc.
aigsd	0.43	Parameter for Igs/Igd.
bigsd	0.054	Parameter for Igs/Igd.
cigsd	0.075 1/V	parameter for Igs/Igd.
nigc	1.0	Parameter for Igc slope.
pigcd	1.0	Parameter for Igc partition.
poxedge	1.0	Factor for the gate edge Tox.
dlcig	lint m	Delta Length for Ig model.
voxh	5.0 V	Limit of Vox in gate current calculation.
deltavox	0.005 V	Smoothing parameter in the Vox smoothing function.
aigbcp2	0.043	First Vgp dependent parameter for gate current in accumulation in AGBCP2 region.
bigbcp2	0.0054	Second Vgp dependent parameter for gate current in accumulation in AGBCP2 region.
cigbcp2	0.0075	Third Vgp dependent parameter for gate current in accumulation in AGBCP2 region.

© 2023 Cadence Design Systems, Inc.

Overlap capacitance parameters

`cgso`	`0 F/m`	Gate-source overlap capacitance.
`cgdo`	`0 F/m`	Gate-drain overlap capacitance.
`cgeo`	`0 F/m`	Gate-substrate overlap capacitance.
`cgbo`	`0 F/m`	Gate-bulk overlap capacitance.
`cgsl`	`0 F/m`	Gate-source overlap capacitance in LDD region.
`cgdl`	`0 F/m`	Gate-drain overlap capacitance in LDD region.
`ckappa`	`0.6`	Overlap capacitance fitting parameter.

Junction capacitance model parameters

`cjswg`	`1e-10 F/m`^{2}	Zero-bias gate-side junction capacitance density.
`mjswg`	`0.5`	Gate-side junction grading coefficient.
`pbswg`	`0.7 V`	Gate-side junction built-in potential.
`cjswgd`	`cjswg F/m`^{2}	Drain(gate side) sidewall junction capacitance per unit width.
`mjswgd`	`mjswg V`	Drain (gate side) sidewall junction capacitance grading coefficient.
`pbswgd`	`pbswg V`	Drain(gate side) sidewall junction capacitance built in potential.
`tt`	`1e-12 s`	Transit time.

© 2023 Cadence Design Systems, Inc.

ndif	-1	Power coefficient of channel length dependency for diffusion capacitance.
ldif0	1	Power coefficient of channel length dependency for diffusion capacitance.
asd	0.3	Source/Drain diffusion smoothing parameter.
vsdfb	(F/m)	Source/Drain diffusion flatband voltage.
vsdth		Source/Drain diffusion threshold voltage.
csdmin	(F)	Source/Drain diffusion bottom minimum capacitance.
csdesw	0 F/m	Source/drain sidewall fringing constant.

© 2023 Cadence Design Systems, Inc.

Charge model selection parameters

cf	0 F/m	Fringe capacitance parameter.
cfrcoeff	1.0	Sidewall fringe capacitance parameter.
clc	1e-8 m	Intrinsic capacitance fitting parameter.
cle	0	Intrinsic capacitance fitting parameter.
dlc	lint m	Delta L for capacitance model.
dlcb	0 m	Length offset fitting parameter for body charge.
dlbg	0 m	Length offset fitting parameter for backgate charge.
dwc	wint m	Delta W for capacitance model.
delvt	0 V	Threshold voltage adjustment for C-V.
fbody	1.0	Scaling factor for body charge.
voffcv	-0.08 V	CV Threshold voltage offset.
minvcv	0	Parameter for moderate inversion in VgsteffCV.
dtoxcv	0 m	Delta oxide thickness in Capmod3.
kb1	1	Scaling factor for backgate charge.
kb3	1	Backgate coupling coefficient at subthreshold.
xpart	0	Drain/source channel charge partition in saturation for BSIM charge model. Use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
vsce	0 V	SCE parameter for improved dVbi model.
cdsbs	0 F/m^2	Coupling from Vd to Vbs for improved dVbi model.

© 2023 Cadence Design Systems, Inc.

RF model parameters

rshg	0.1	Gate sheet resistance.
xrcrg1		First fitting parameter for the bias-dependent Rg.
xrcrg2		Second fitting parameter for the bias-dependent Rg.
ngcon		Number of gate contacts.
xgw		Distance from gate contact center to device edge.
xgl		Variation in Ldrawn.
rbdb	50 Ω	Resistance between bNode and dbNode.
rbsb	50 Ω	Resistance between bNode and sbNode.
gbmin	1e-12 S	Minimum body conductance.

Temperature effects parameters

tnom	27.0 C	Parameters measurement temperature. The default value is set by the options statement.
trise	0 C	Temperature rise from ambient.
ids0mult	1	Variability in Drain current for misc. reasons.
ids0multmod	0	The flag for rd/rs scaling.
tmax	500 C	Maximum device temperature above ambient.
kt1	-0.11 V	Temperature coefficient for threshold voltage.
kt11	0 V m	Temperature coefficient for threshold voltage.

© 2023 Cadence Design Systems, Inc.

kt2	0.022	Temperature coefficient for threshold voltage.
at	3.3e4 m/s	Temperature coefficient for vsat.
tcjswg	0 1/K	Temperature coefficient of Cjswg.
tpbswg	0 V/K	Temperature coefficient of Pbswg.
tcjswgd	tcjswg 1/K	Temperature coefficient of Cjswgd.
tpbswgd	tpbswg V/K	Temperature coefficient of Pbswgd.
ua1	4.31e-9 m/V	Temperature coefficient for ua.
ub1	-7.61e-18 m^2/V^2	Temperature coefficient for ub.
uc1	-5.5e-11 m/V^2	Temperature coefficient for uc. Default is -0.056 for mobmod=3.
ucste	-4.775e-3 1/K	Temperature coefficient of UCS.
ud1	0 $/m^2/K$	Temperature coefficient of ud.
prt	0 Ω	Temperature coefficient for Rds.
ute	-1.5	Mobility temperature exponent.
cth0	1e-5 w s/(m C)	Self-heating thermal capacitance.
rth0	0 (m C)/w	Self-heating thermal resistance.

© 2023 Cadence Design Systems, Inc.

ntrecf	0	Temperature coefficient of Nrecf.
ntrecr	0	Temperature coefficient of Nrecr.
xbjt	1	BJT current temperature exponent.
xdif	2	Diffusion current temperature exponent.
xrec	1	Recombination current temperature exponent.
xtun	0	Tunneling current temperature exponent.
xdifd	xdif	Temperature coefficient for Iddif.
xrecd	xrec	Temperature coefficient for Idrec.
xtund	xtun	Temperature coefficient for Idtun.
wth0	0 μm	Minimum width for thermal resistance calculation.
tvbci	0 V/K	Temperature coefficient for vbci.
trs	0 1/C	Temperature parameter for source resistance.
trd	0 1/C	Temperature parameter for drain resistance.

© 2023 Cadence Design Systems, Inc.

Noise model parameters

tnoia	1.5	Thermal noise parameter.
tnoib	3.5	Thermal noise parameter.
rnoia	0.577	Thermal noise coefficient.
rnoib	0.37	Thermal noise coefficient.
ntnoi	1.0	Thermal noise coefficient.
noif	1	Floating body excess noise ideality factor.
w0flk	0 m	Width constant for flicker noise equation.
bf	2.0	Flicker noise length dependence exponent.
kf	0	Flicker (1/f) noise coefficient.
af	1	Flicker (1/f) noise exponent.
ef	1	Flicker (1/f) noise frequency exponent.
noia	1e20	Oxide trap density coefficient. Default is 9.9e18 for pmos.
noib	5e4	Oxide trap density coefficient. Default is 2.4e3 for pmos.
noic	-1.4e-12	Oxide trap density coefficient. Default is 1.4e-8 for pmos.
em	4.1e7 V/m	Maximum electric field.

© 2023 Cadence Design Systems, Inc.

Stress model parameters

saref	1e-6 m	Reference distance between OD edge and poly from one side.
sbref	1e-6 m	Reference distance between OD edge and poly from the other side.
wlod	0 m	Width parameter for stress effect.
ku0	0 m	Mobility degradation/enhancement coefficient for LOD.
tku0	0	Temperature coefficient of KU0.
llodku0	0	Length parameter for u0 LOD effect.
wlodku0	0	Width parameter for u0 LOD effect.
kvth0	0 V m	Threshold degradation/enhancement parameter for LOD.
llodvth	0	Length parameter for vth LOD effect.
wlodvth	0	Width parameter for vth LOD effect.
kvsat	0 m	Saturation velocity degradation/enhancement parameter for LOD.
stk2	0 m	K2 shift factor related to stress effect on vth.
lodk2	1.0	K2 shift modification factor for stress effect.
steta0	0 m	eta0 shift factor related to stress effect on vth.
lodeta0	1.0	eta0 shift modification factor for stress effect.

© 2023 Cadence Design Systems, Inc.

Default instance parameters

w	5e-6 m	Default channel width.
l	5e-6 m	Default channel length.
as	0 m^2	Default area of source diffusion.
ad	0 m^2	Default area of drain diffusion.
ps	0 m	Default perimeter of source diffusion.
pd	0 m	Default perimeter of drain diffusion.
nrd	1 m/m	Default number of squares of drain diffusion.
nrs	1 m/m	Default number of squares of source diffusion.
nrb	1 m/m	Default body squares.
paramchk	1	Model parameter checking selector.

Auto Model Selector parameters

wmax	1 m	Maximum channel width for which the model is valid.
wmin	0 m	Minimum channel width for which the model is valid.
lmax	1 m	Maximum channel length for which the model is valid.
lmin	0 m	Minimum channel length for which the model is valid.

© 2023 Cadence Design Systems, Inc.

Compatibility model parameters

`compatible`	`spectre`	Causes device equations to be compatible with a foreign simulator. This option does not affect input syntax.Possible values are spectre, spice2, spice3, cdsspice, hspice, spiceplus, eldo, sspice and mica.

Junction diode model parameters

`dskip`	`yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`.Possible values are no and yes.

Operating region warning control parameters

`alarm`	`none`	Forbidden operating region.Possible values are none, off, triode, sat, subth and rev.
`imax`	`1 A`	Maximum allowable current.
`bvj`	`infinity V`	Junction reverse breakdown voltage.
`vbox`	`1e9*tox V`	Oxide breakdown voltage.
`warn`	`on`	Parameter to turn warnings on and off.Possible values are off and on.

DC-mismatch dependent parameters

`mismatchmod`	`0`	Select mismatch mode.

© 2023 Cadence Design Systems, Inc.

`mismatchdist`	`0 m`	Mismatch distance.
`mvtwl`	`0 V m`	Threshold mismatch area dependence.
`mvtwl2`	`0 V m^1.5`	Threshold mismatch area square dependence.
`mvt0`	`0 V`	Threshold mismatch intercept.
`mbewl`	`0 m`	Beta mismatch area dependence.
`mbe0`	`0`	Beta mismatch intercept.

© 2023 Cadence Design Systems, Inc.

Length dependent parameters

`lnch`	0	Length dependence of nch.
`lnsub`	0	Length dependence of nsub.
`lngate`	0	Length dependence of ngate.
`lvtho`	0	Length dependence of vtho.
`lk1`	0	Length dependence of k1.
`lk1w1`	0	Length dependence of k1w1.
`lk1w2`	0	Length dependence of k1w2.
`lk2`	0	Length dependence of k2.
`lk3`	0	Length dependence of k3.
`lk3b`	0	Length dependence of k3b.
`lkb1`	0	Length dependence of kb1.
`lw0`	0	Length dependence of w0.
`lnlx`	0	Length dependence of nlx.
`ldvt0`	0	Length dependence of dvt0.
`ldvt1`	0	Length dependence of dvt1.
`ldvt2`	0	Length dependence of dvt2.
`ldvt0w`	0	Length dependence of dvt0w.
`ldvt1w`	0	Length dependence of dvt1w.
`ldvt2w`	0	Length dependence of dvt2w.

© 2023 Cadence Design Systems, Inc.

lu0	0	Length dependence of u0.
lua	0	Length dependence of ua.
lub	0	Length dependence of ub.
luc	0	Length dependence of uc.
lvsat	0	Length dependence of vsat.
la0	0	Length dependence of a0.
lags	0	Length dependence of ags.
lb0	0	Length dependence of b0.
lb1	0	Length dependence of b1.
lketa	0	Length dependence of keta.
lketas	0	Length dependence of ketas.
la1	0	Length dependence of a1.
la2	0	Length dependence of a2.
lrdsw	0	Length dependence of rdsw.
lprwb	0	Length dependence of prwb.
lprwg	0	Length dependence of prwg.
lwr	0	Length dependence of wr.
lnfactor	0	Length dependence of nfactor.
ldwg	0	Length dependence of dwg.

© 2023 Cadence Design Systems, Inc.

ldwb	0	Length dependence of dwb.
lvoff	0	Length dependence of voff.
leta0	0	Length dependence of eta0.
letab	0	Length dependence of etab.
ldsub	0	Length dependence of dsub.
lcit	0	Length dependence of cit.
lcdsc	0	Length dependence of cdsc.
lcdscb	0	Length dependence of cdscb.
lcdscd	0	Length dependence of cdscd.
lpclm	0	Length dependence of pclm.
lpdiblc1	0	Length dependence of pdiblc1.
lpdiblc2	0	Length dependence of pdiblc2.
lpdiblcb	0	Length dependence of pdiblcb.
ldrout	0	Length dependence of drout.
lpvag	0	Length dependence of pvag.
ldelta	0	Length dependence of delta.
lalpha0	0	Length dependence of alpha0.
lfbjtii	0	Length dependence of fbjtii.
lbeta0	0	Length dependence of beta0.

© 2023 Cadence Design Systems, Inc.

lbeta1	0	Length dependence of beta1.
lbeta2	0	Length dependence of beta2.
lvdsatii0	0	Length dependence of vdstaii0.
llii	0	Length dependence of lii.
lesatii	0	Length dependence of esatii.
lsii0	0	Length dependence of sii0.
lsii1	0	Length dependence of sii1.
lsii2	0	Length dependence of sii2.
lsiid	0	Length dependence of siid.
lagidl	0	Length dependence of agidl.
lbgidl	0	Length dependence of bgidl.
lngidl	0	Length dependence of ngidl.
lntun	0	Length dependence of ntun.
lndiode	0	Length dependence of ndoide.
lnrecf0	0	Length dependence of nrecf0.
lnrecr0	0	Length dependence of nrecr0.
lisbjt	0	Length dependence of isbjt.
lisdif	0	Length dependence of isdif.
lisrec	0	Length dependence of isrec.

© 2023 Cadence Design Systems, Inc.

`listun`	0	Length dependence of istun.
`lvrec0`	0	Length dependence of vrec0.
`lvtun0`	0	Length dependence of vtun0.
`lnbjt`	0	Length dependence of nbjt.
`llbjt0`	0	Length dependence of lbjt0.
`lvabjt`	0	Length dependence of vabjt.
`laely`	0	Length dependence of aely.
`lahli`	0	Length dependence of ahli.
`lxrcrg1`	0	Length dependence of xrcrg1.
`lxrcrg2`	0	Length dependence of xrcrg2.
`lvsdfb`	0	Length dependence of vsdfb.
`lvsdth`	0	Length dependence of vsdth.
`ldelvt`	0	Length dependence of delvt.
`lacde`	0	Length dependence of acde.
`lmoin`	0	Length dependence of moin.
`laigc`	0	Length dependence of aigc.
`lbigc`	0	Length dependence of bigc.
`lcigc`	0	Length dependence of cigc.
`laigsd`	0	Length dependence of aigsd.

© 2023 Cadence Design Systems, Inc.

lbigsd	0	Length dependence of bigsd.
lcigsd	0	Length dependence of cigsd.
lnigc	0	Length dependence of nigc.
lpigcd	0	Length dependence of pigcd.
lpoxedge	0	Length dependence of poxedge.
lxj	0	Length dependence of xj.
lalphagb1	0	Length dependence of alphagb1.
lalphagb2	0	Length dependence of alphagb2.
lbetagb1	0	Length dependence of betagb1.
lbetagb2	0	Length dependence of betagb2.
lcgsl	0	Length dependence of cgsl.
lcgdl	0	Length dependence of cgdl.
lckappa	0	Length dependence of ckappa.
lndif	0	Length dependence of ndif.
lute	0	Length dependence of ute.
lkt1	0	Length dependence of kt1.
lkt1l	0	Length dependence of kt1l.
lkt2	0	Length dependence of kt2.
lua1	0	Length dependence of ua1.

© 2023 Cadence Design Systems, Inc.

lub1	0	Length dependence of ub1.
luc1	0	Length dependence of uc1.
lat	0	Length dependence of at.
lprt	0	Length dependence of prt.
lntrecf	0	Length dependence of ntrecf.
lntrecr	0	Length dependence of ntrecr.
lxbjt	0	Length dependence of xbjt.
lxdif	0	Length dependence of xdif.
lxrec	0	Length dependence of xrec.
lxtun	0	Length dependence of xtun.
lxdifd	0	Length dependence of xdifd.
lxrecd	0	Length dependence of xrecd.
lxtund	0	Length dependence of xtund.
llpe0	0	Length dependence of lpe0.
llpeb	0	Length dependence of lpeb.
lrsw	0	Length dependence of Rsw.
lrdw	0	Length dependence of Rdw.
lcgidl	0	Length dependence of cgidl.
legidl	0	Length dependence of egidl.

© 2023 Cadence Design Systems, Inc.

lntund	0	Length dependence of ntund.
lndioded	0	Length dependence of ndioded.
lnrecf0d	0	Length dependence of nrecf0d.
lnrecr0d	0	Length dependence of nrecr0d.
lidbjt	0	Length dependence of idbjt.
liddif	0	Length dependence of iddif.
lidrec	0	Length dependence of idrec.
lidtun	0	Length dependence of idtun.
lvrec0d	0	Length dependence of vrec0d.
lvtun0d	0	Length dependence of vtun0d.
lahlid	0	Length dependence of lahlid.
lnoff	0	Length dependence of noff.
ldvtp0	0	Length dependence of dvtp0.
ldvtp1	0	Length dependence of dvtp1.
lminv	0	Length dependence of minv.
lfprout	0	Length dependence of pdiblcb.
lpdits	0	Length dependence of pdits.
lpditsd	0	Length dependence of pditsd.
lku0	0	Length dependence of ku0.

© 2023 Cadence Design Systems, Inc.

lkvth0	0	Length dependence of kvth0.
lvoffcv	0	Length dependence of voffcv.
lminvcv	0	Length dependence of minvcv.
lud	0	Length dependence of ud.
lud1	0	Length dependence of ud1.
lebjtii	0	Length dependence of ebjtii.
lcbjtii	0	Length dependence of cbjtii.
labjtii	0	Length dependence of abjtii.
lmbjtii	0	Length dependence of mbjtii.
lvbci	0	Length dependence of vbci.
ldvtp2	0	Length dependence of dvtp2.
ldvtp3	0	Length dependence of dvtp3.
ldvtp4	0	Length dependence of dvtp4.
laigbcp2	0	Length dependence of aigbcp2.
lbigbcp2	0	Length dependence of bigbcp2.
lcigbcp2	0	Length dependence of cigbcp2.
lnsd	0	Length dependence of nsd.
lvfb	0	Length dependence of vfb.
leu	0	Length dependence of eu.

© 2023 Cadence Design Systems, Inc.

`lucs`	0	Length dependence of ucs.
`lucste`	0	Length dependence of ucste.
`legisl`	0	Length dependence of egisl.
`lagisl`	0	Length dependence of agisl.
`lbgisl`	0	Length dependence of bgisl.
`lcgisl`	0	Length dependence of cgisl.
`lrgidl`	0	Length dependence of rgidl.
`lkgidl`	0	Length dependence of kgidl.
`lfgidl`	0	Length dependence of fgidl.
`lrgisl`	0	Length dependence of rgisl.
`lkgisl`	0	Length dependence of kgisl.
`lfgisl`	0	Length dependence of fgisl.

© 2023 Cadence Design Systems, Inc.

Width dependent parameters

wnch	0	Width dependence of nch.
wnsub	0	Width dependence of nsub.
wngate	0	Width dependence of ngate.
wvtho	0	Width dependence of vto.
wk1	0	Width dependence of k1.
wk1w1	0	Width dependence of k1w1.
wk1w2	0	Width dependence of k1w2.
wk2	0	Width dependence of k2.
wk3	0	Width dependence of k3.
wk3b	0	Width dependence of k3b.
wkb1	0	Width dependence of kb1.
ww0	0	Width dependence of w0.
wnlx	0	Width dependence of nlx.
wdvt0	0	Width dependence of dvt0.
wdvt1	0	Width dependence of dvt1.
wdvt2	0	Width dependence of dvt2.
wdvt0w	0	Width dependence of dvt0w.
wdvt1w	0	Width dependence of dvt1w.
wdvt2w	0	Width dependence of dvt2w.

© 2023 Cadence Design Systems, Inc.

wu0	0	Width dependence of u0.
wua	0	Width dependence of ua.
wub	0	Width dependence of ub.
wuc	0	Width dependence of uc.
wvsat	0	Width dependence of vsat.
wa0	0	Width dependence of a0.
wags	0	Width dependence of ags.
wb0	0	Width dependence of b0.
wb1	0	Width dependence of b1.
wketa	0	Width dependence of keta.
wketas	0	Width dependence of ketas.
wa1	0	Width dependence of a1.
wa2	0	Width dependence of a2.
wrdsw	0	Width dependence of rdsw.
wprwb	0	Width dependence of prwb.
wprwg	0	Width dependence of prwg.
wwr	0	Width dependence of wr.
wnfactor	0	Width dependence of nfactor.
wdwg	0	Width dependence of dwg.

© 2023 Cadence Design Systems, Inc.

wdwb	0	Width dependence of dwb.
wvoff	0	Width dependence of voff.
weta0	0	Width dependence of eta0.
wetab	0	Width dependence of etab.
wdsub	0	Width dependence of dsub.
wcit	0	Width dependence of cit.
wcdsc	0	Width dependence of cdsc.
wcdscb	0	Width dependence of cdscb.
wcdscd	0	Width dependence of cdscd.
wpclm	0	Width dependence of pclm.
wpdiblc1	0	Width dependence of pdiblc1.
wpdiblc2	0	Width dependence of pdiblc2.
wpdiblcb	0	Width dependence of pdiblcb.
wdrout	0	Width dependence of drout.
wpvag	0	Width dependence of pvag.
wdelta	0	Width dependence of delta.
walpha0	0	Width dependence of alpha0.
wfbjtii	0	Width dependence of fbjtii.
wbeta0	0	Width dependence of beta0.

© 2023 Cadence Design Systems, Inc.

wbeta1	0	Width dependence of beta1.
wbeta2	0	Width dependence of beta2.
wvdsatii0	0	Width dependence of vdsatii0.
wlii	0	Width dependence of lii.
wesatii	0	Width dependence of esatii.
wsii0	0	Width dependence of sii0.
wsii1	0	Width dependence of sii1.
wsii2	0	Width dependence of sii2.
wsiid	0	Width dependence of siid.
wagidl	0	Width dependence of agidl.
wbgidl	0	Width dependence of bgidl.
wngidl	0	Width dependence of ngidl.
wntun	0	Width dependence of wntun.
wndiode	0	Width dependence of ndiode.
wnrecf0	0	Width dependence of nrecf0.
wnrecr0	0	Width dependence of nrecr0.
wisbjt	0	Width dependence of isbjt.
wisdif	0	Width dependence of isdif.
wisrec	0	Width dependence of isrec.

© 2023 Cadence Design Systems, Inc.

wistun	0	Width dependence of istun.
wvrec0	0	Width dependence of vrec0.
wvtun0	0	Width dependence of vtun0.
wnbjt	0	Width dependence of nbjt.
wlbjt0	0	Width dependence of lbjt0.
wvabjt	0	Width dependence of vabjt.
waely	0	Width dependence of aely.
wahli	0	Width dependence of ahli.
wxrcrg1	0	Width dependence of xrcrg1.
wxrcrg2	0	Width dependence of xrcrg2.
wvsdfb	0	Width dependence of vsdfb.
wvsdth	0	Width dependence of vsdth.
wdelvt	0	Width dependence of delvt.
wacde	0	Width dependence of acde.
wmoin	0	Width dependence of moin.
waigc	0	Width dependence of aigc.
wbigc	0	Width dependence of bigc.
wcigc	0	Width dependence of cigc.
waigsd	0	Width dependence of aigsd.

© 2023 Cadence Design Systems, Inc.

wbigsd	0	Width dependence of bigsd.
wcigsd	0	Width dependence of cigsd.
wnigc	0	Width dependence of nigc.
wpigcd	0	Width dependence of pigcd.
wpoxedge	0	Width dependence of poxedge.
wxj	0	Width dependence of xj.
walphagb1	0	Width dependence of alphagb1.
walphagb2	0	Width dependence of alpagb2.
wbetagb1	0	Width dependence of betagb1.
wbetagb2	0	Width dependence of betabg2.
wcgsl	0	Width dependence of cgsl.
wcgdl	0	Width dependence of cgdl.
wckappa	0	Width dependence of ckappa.
wndif	0	Width dependence of ndif.
wute	0	Width dependence of ute.
wkt1	0	Width dependence of kt1.
wkt1l	0	Width dependence of kt1l.
wkt2	0	Width dependence of kt2.
wua1	0	Width dependence of ua1.

© 2023 Cadence Design Systems, Inc.

wub1	0	Width dependence of ub1.
wuc1	0	Width dependence of uc1.
wat	0	Width dependence of at.
wprt	0	Width dependence of prt.
wntrecf	0	Width dependence of ntrecf.
wntrecr	0	Width dependence of ntrecr.
wxbjt	0	Width dependence of xbjt.
wxdif	0	Width dependence of xdif.
wxrec	0	Width dependence of xrec.
wxdifd	0	Width dependence of xdifd.
wxrecd	0	Width dependence of xrecd.
wxtund	0	Width dependence of xtund.
wlpe0	0	Width dependence of lpe0.
wlpeb	0	Width dependence of lpeb.
wrsw	0	Width dependence of rsw.
wrdw	0	Width dependence of rdw.
wcgidl	0	Width dependence of Cgidl.
wegidl	0	Width dependence of Egidl.
wntund	0	Width dependence of ntund.

© 2023 Cadence Design Systems, Inc.

wndioded	0	Width dependence of ndioded.
wnrecf0d	0	Width dependence of nrecf0d.
wnrecr0d	0	Width dependence of nrecr0d.
widbjt	0	Width dependence of Idbjt.
widdif	0	Width dependence of iddif.
widrec	0	Width dependence of idrec.
widtun	0	Width dependence of idtun.
wvrec0d	0	Width dependence of Vrec0d.
wvtun0d	0	Width dependence of Vtun0d.
wahlid	0	Width dependence of Ahlid.
wxtun	0	Width dependence of xtun.
wnoff	0	Width dependence of noff.
wdvtp0	0	Width dependence of dvtp0.
wdvtp1	0	Width dependence of dvtp1.
wminv	0	width dependence of minv.
wfprout	0	Width dependence of pdiblcb.
wpdits	0	Width dependence of pdits.
wpditsd	0	Width dependence of pditsd.
wku0	0	Width dependence of ku0.

© 2023 Cadence Design Systems, Inc.

wkvth0	0	Width dependence of kvth0.
wvoffcv	0	Width dependence of voffcv.
wminvcv	0	Width dependence of minvcv.
wud	0	Width dependence of ud.
wud1	0	Width dependence of ud1.
webjtii	0	Width dependence of ebjtii.
wcbjtii	0	Width dependence of cbjtii.
wabjtii	0	Width dependence of abjtii.
wmbjtii	0	Width dependence of mbjtii.
wvbci	0	Width dependence of vbci.
wdvtp2	0	Width dependence of dvtp2.
wdvtp3	0	Width dependence of dvtp3.
wdvtp4	0	Width dependence of dvtp4.
waigbcp2	0	Width dependence of aigbcp2.
wbigbcp2	0	Width dependence of bigbcp2.
wcigbcp2	0	Width dependence of cigbcp2.
wnsd	0	Width dependence of nsd.
wvfb	0	Width dependence of vfb.
weu	0	Width dependence of eu.

© 2023 Cadence Design Systems, Inc.

wucs	0	Width dependence of ucs.
wucste	0	Width dependence of ucste.
wegisl	0	Width dependence of egisl.
wagisl	0	Width dependence of agisl.
wbgisl	0	Width dependence of bgisl.
wcgisl	0	Width dependence of cgisl.
wrgidl	0	Width dependence of rgidl.
wkgidl	0	Width dependence of kgidl.
wfgidl	0	Width dependence of fgidl.
wrgisl	0	Width dependence of rgisl.
wkgisl	0	Width dependence of kgisl.
wfgisl	0	Width dependence of fgisl.

© 2023 Cadence Design Systems, Inc.

Cross-term dependent parameters

pnch	0	Cross-term dependence of nch.
pnsub	0	Cross-term dependence of nsub.
pngate	0	Cross-term dependence of ngate.
pvtho	0	Cross-term dependence of vto.
pk1	0	Cross-term dependence of k1.
pk1w1	0	Cross-term dependence of k1w1.
pk1w2	0	Cross-term dependence of k1w2.
pk2	0	Cross-term dependence of k2.
pk3	0	Cross-term dependence of k3.
pk3b	0	Cross-term dependence of k3b.
pkb1	0	Cross-term dependence of kb1.
pw0	0	Cross-term dependence of w0.
pnlx	0	Cross-term dependence of nlx.
pdvt0	0	Cross-term dependence of dvt0.
pdvt1	0	Cross-term dependence of dvt1.
pdvt2	0	Cross-term dependence of dvt2.
pdvt0w	0	Cross-term dependence of dvt0w.
pdvt1w	0	Cross-term dependence of dvt1w.
pdvt2w	0	Cross-term dependence of dvt2w.

© 2023 Cadence Design Systems, Inc.

pu0	0	Cross-term dependence of u0.
pua	0	Cross-term dependence of ua.
pub	0	Cross-term dependence of ub.
puc	0	Cross-term dependence of uc.
pvsat	0	Cross-term dependence of vsat.
pa0	0	Cross-term dependence of a0.
pags	0	Cross-term dependence of ags.
pb0	0	Cross-term dependence of b0.
pb1	0	Cross-term dependence of b1.
pketa	0	Cross-term dependence of keta.
pketas	0	Cross-term dependence of ketas.
pa1	0	Cross-term dependence of a1.
pa2	0	Cross-term dependence of a2.
prdsw	0	Cross-term dependence of rdsw.
pprwb	0	Cross-term dependence of prwb.
pprwg	0	Cross-term dependence of prwg.
pwr	0	Cross-term dependence of wr.
pnfactor	0	Cross-term dependence of nfactor.
pdwg	0	Cross-term dependence of dwg.

© 2023 Cadence Design Systems, Inc.

pdwb	0	Cross-term dependence of dwb.
pvoff	0	Cross-term dependence of voff.
peta0	0	Cross-term dependence of eta0.
petab	0	Cross-term dependence of etab.
pdsub	0	Cross-term dependence of dsub.
pcit	0	Cross-term dependence of cit.
pcdsc	0	Cross-term dependence of cdsc.
pcdscb	0	Cross-term dependence of cdscb.
pcdscd	0	Cross-term dependence of cdscd.
ppclm	0	Cross-term dependence of pclm.
ppdiblc1	0	Cross-term dependence of pdiblc1.
ppdiblc2	0	Cross-term dependence of pdiblc2.
ppdiblcb	0	Cross-term dependence of pdiblcb.
pdrout	0	Cross-term dependence of drout.
ppvag	0	Cross-term dependence of pvag.
pdelta	0	Cross-term dependence of delta.
palpha0	0	Cross-term dependence of alpha0.
pfbjtii	0	Cross-term dependence of fbjtii.
pbeta0	0	Cross-term dependence of beta0.

© 2023 Cadence Design Systems, Inc.

pbeta1	0	Cross-term dependence of beta1.
pbeta2	0	Cross-term dependence of beta2.
pvdsatii0	0	Cross-term dependence of vdsatii0.
plii	0	Cross-term dependence of lii.
pesatii	0	Cross-term dependence of esatii.
psii0	0	Cross-term dependence of sii0.
psii1	0	Cross-term dependence of sii1.
psii2	0	Cross-term dependence of sii2.
psiid	0	Cross-term dependence of siid.
pagidl	0	Cross-term dependence of agidl.
pbgidl	0	Cross-term dependence of bgidl.
pngidl	0	Cross-term dependence of ngidl.
pntun	0	Cross-term dependence of ntun.
pndiode	0	Cross-term dependence of ndiode.
pnrecf0	0	Cross-term dependence of nrecf0.
pnrecr0	0	Cross-term dependence of nrecr0.
pisbjt	0	Cross-term dependence of isbjt.
pisdif	0	Cross-term dependence of isdif.
pisrec	0	Cross-term dependence of isrec.

© 2023 Cadence Design Systems, Inc.

pistun	0	Cross-term dependence of istun.
pvrec0	0	Cross-term dependence of vrec0.
pvtun0	0	Cross-term dependence of vtun0.
pnbjt	0	Cross-term dependence of nbjt.
plbjt0	0	Cross-term dependence of lbjt0.
pvabjt	0	Cross-term dependence of vabjt.
paely	0	Cross-term dependence of aely.
pahli	0	Cross-term dependence of ahli.
pxrcrg1	0	Cross-term dependence of xrcrg1.
pxrcrg2	0	Cross-term dependence of xrcrg2.
pvsdfb	0	Cross-term dependence of vsdfb.
pvsdth	0	Cross-term dependence of vsdth.
pdelvt	0	Cross-term dependence of delvt.
pacde	0	Cross-term dependence of acde.
pmoin	0	Cross-term dependence of moin.
paigc	0	Cross-term dependence of aigc.
pbigc	0	Cross-term dependence of bigc.
pcigc	0	Cross-term dependence of cigc.
paigsd	0	Cross-term dependence of aigsd.

© 2023 Cadence Design Systems, Inc.

pbigsd	0	Cross-term dependence of bigsd.
pcigsd	0	Cross-term dependence of cigsd.
pnigc	0	Cross-term dependence of nigc.
ppigcd	0	Cross-term dependence of pigcd.
ppoxedge	0	Cross-term dependence of poxedge.
pxj	0	Cross-term dependence of xj.
palphagb1	0	Cross-term dependence of alphagb1.
palphagb2	0	Cross-term dependence of alphagb2.
pbetagb1	0	Cross-term dependence of betagb1.
pbetagb2	0	Cross-term dependence of betagb2.
pcgsl	0	Cross-term dependence of cgsl.
pcgdl	0	Cross-term dependence of cgdl.
pckappa	0	Cross-term dependence of ckappa.
pndif	0	Cross-term dependence of ndif.
pute	0	Cross-term dependence of ute.
pkt1	0	Cross-term dependence of kt1.
pkt1l	0	Cross-term dependence of kt1l.
pkt2	0	Cross-term dependence of kt2.
pua1	0	Cross-term dependence of ua1.

© 2023 Cadence Design Systems, Inc.

pub1	0	Cross-term dependence of ub1.
puc1	0	Cross-term dependence of uc1.
pat	0	Cross-term dependence of at.
pprt	0	Cross-term dependence of prt.
pntrecf	0	Cross-term dependence of ntrecf.
pntrecr	0	Cross-term dependence of ntrecr.
pxbjt	0	Cross-term dependence of xbjt.
pxdif	0	Cross-term dependence of xdif.
pxrec	0	Cross-term dependence of xrec.
pxtun	0	Cross-term dependence of xtun.
pxdifd	0	Cross-term dependence of xdifd.
pxrecd	0	Cross-term dependence of xrecd.
pxtund	0	Cross-term dependence of xtund.
plpe0	0	Cross-term dependence of lpe0.
plpeb	0	Cross-term dependence of lpeb.
prsw	0	Cross-term dependence of rsw.
prdw	0	Cross-term dependence of rdw.
pcgidl	0	Cross-term dependence of cgidl.
pegidl	0	Cross-term dependence of egidl.

© 2023 Cadence Design Systems, Inc.

pntund	0	Cross-term dependence of ntund.
pndioded	0	Cross-term dependence of ndioded.
pnrecf0d	0	Cross-term dependence of nrecf0d.
pnrecr0d	0	Cross-term dependence of nrecr0d.
pidbjt	0	Cross-term dependence of ldbjt.
piddif	0	Cross-term dependence of lddif.
pidrec	0	Cross-term dependence of ldrec.
pidtun	0	Cross-term dependence of idtun.
pvrec0d	0	Cross-term dependence of vrec0d.
pvtun0d	0	Cross-term dependence of vtun0d.
pahlid	0	Cross-term dependence of ahlid.
pnoff	0	Cross-term dependence of noff.
pdvtp0	0	Cross-term dependence of dvtp0.
pdvtp1	0	Cross-term dependence of dvtp1.
pminv	0	Cross-term dependence of minv.
pfprout	0	Cross-term dependence of pdiblcb.
ppdits	0	Cross-term dependence of pdits.
ppditsd	0	Cross-term dependence of pditsd.
pku0	0	Cross-term dependence of ku0.

© 2023 Cadence Design Systems, Inc.

pkvth0	0	Cross-term dependence of kvth0.
pvoffcv	0	Cross-term dependence of voffcv.
pminvcv	0	Cross-term dependence of minvcv.
pud	0	Cross-term dependence of ud.
pud1	0	Cross-term dependence of ud1.
pebjtii	0	Cross-term dependence of ebjtii.
pcbjtii	0	Cross-term dependence of cbjtii.
pabjtii	0	Cross-term dependence of abjtii.
pmbjtii	0	Cross-term dependence of mbjtii.
pvbci	0	Cross-term dependence of vbci.
pdvtp2	0	Cross-term dependence of dvtp2.
pdvtp3	0	Cross-term dependence of dvtp3.
pdvtp4	0	Cross-term dependence of dvtp4.
paigbcp2	0	Cross-term dependence of aigbcp2.
pbigbcp2	0	Cross-term dependence of bigbcp2.
pcigbcp2	0	Cross-term dependence of cigbcp2.
pnsd	0	Cross-term dependence of nsd.
pvfb	0	Cross-term dependence of vfb.
peu	0	Cross-term dependence of eu.

© 2023 Cadence Design Systems, Inc.

pucs	0	Cross-term dependence of ucs.
pucste	0	Cross-term dependence of ucste.
pegisl	0	Cross-term dependence of egisl.
pagisl	0	Cross-term dependence of agisl.
pbgisl	0	Cross-term dependence of bgisl.
pcgisl	0	Cross-term dependence of cgisl.
prgidl	0	Cross-term dependence of rgidl.
pkgidl	0	Cross-term dependence of kgidl.
pfgidl	0	Cross-term dependence of fgidl.
prgisl	0	Cross-term dependence of rgisl.
pkgisl	0	Cross-term dependence of kgisl.
pfgisl	0	Cross-term dependence of fgisl.
vthmod		Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'.Possible values are std and vthcc.
ivth	(A)	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
ivthw	(m)	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
ivthl	(m)	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.

© 2023 Cadence Design Systems, Inc.

ivth_vdsmin	(V)	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
gmin_compatible	spectre	Choose gmin compatibility of model, possible values are 'spectre'(default) and 'cmc'.Possible values are spectre and cmc.
eta0cv	0.08	Subthreshold region DIBL coefficient for C-V.
etabcv	(-0.07)	Subthreshold region DIBL coefficient for C-V.
steta0cv	0.0	eta0cv shift factor related to stress effect on vth.
lodeta0cv	1.0	eta0cv shift modification factor for stress effect.
leta0cv	0.0	Length dependence of eta0cv.
letabcv	0.0	Length dependence of etabcv.
weta0cv	0.0	Width dependence of eta0cv.
wetabcv	0.0	Width dependence of etabcv.
peta0cv	0.0	Cross-term dependence of eta0cv.
petabcv	0.0	Cross-term dependence of etabcv.
tnoic	3.5	Length dependent parameter for Correlation Coefficient.
rnoic	0.395	Correlation coefficient parameter.
scalen	1e5	Scale factor for correlated noise.
eggbcp2	1.12	Bandgap in Agbcp2 region.
eggdep	1.12	Bandgap for gate depletion effect.

© 2023 Cadence Design Systems, Inc.

agb1	3.7622e-7	'A' for Igb1 Tunneling current model.
bgb1	(-3.1051e10)	'B' for Igb1 tunneling current model.
agb2	4.9758e-7	'A' for Igb2 tunneling current model.
bgb2	(-2.357e10)	'B' for Igb2 tunneling current model.
agbc2n	3.4254e-7	NMOS 'A' for tunneling current model.
agbc2p	4.9723e-7	PMOS 'A' for tunneling current model.
bgbc2n	1.1665e12	NMOS 'B' for tunneling current model.
bgbc2p	7.4567e11	PMOS 'B' for tunneling current model.
vtm00	0.026	Thermal voltage at 25 degC.
nodechk	1	NODE checking flag.
noff2	1.0	C-V turn-on/off parameter /* v4.6.
lnoff2	0.0	Length dependence of noff2 /* v4.6.
wnoff2	0.0	Width dependence of noff2 /* v4.6.
pnoff2	0.0	Cross-term dependence of noff2 /* v4.6.
lvbsa	0.0	Length dependence of vbsa.

© 2023 Cadence Design Systems, Inc.

lvsce	0.0	Length dependence of vsce.
lcdsbs	0.0	Length dependence of cdsbs.
lnofffd	0.0	Length dependence of nofffd.
lvofffd	0.0	Length dependence of vofffd.
lk1b	0.0	Length dependence of k1b.
lk2b	0.0	Length dependence of k2b.
ldk2b	0.0	Length dependence of dk2b.
ldvbd0	0.0	Length dependence of dvbd0.
ldvbd1	0.0	Length dependence of dvbd1.
lmoinfd	0.0	Length dependence of moinfd.
lvbs0pd	0.0	Length dependence of vbs0pd.
lvbs0fd	0.0	Length dependence of vbs0fd.
wvbsa	0.0	Width dependence of vbsa.
wvsce	0.0	Width dependence of vsce.
wcdsbs	0.0	Width dependence of cdsbs.
wnofffd	0.0	Width dependence of nofffd.
wvofffd	0.0	Width dependence of vofffd.
wk1b	0.0	Width dependence of k1b.
wk2b	0.0	Width dependence of k2b.

© 2023 Cadence Design Systems, Inc.

wdk2b	0.0	Width dependence of dk2b.
wdvbd0	0.0	Width dependence of dvbd0.
wdvbd1	0.0	Width dependence of dvbd1.
wmoinfd	0.0	Width dependence of moinfd.
wvbs0pd	0.0	Width dependence of vbs0pd.
wvbs0fd	0.0	Width dependence of vbs0fd.
pvbsa	0.0	Cross-term dependence of vbsa.
pvsce	0.0	Cross-term dependence of vsce.
pcdsbs	0.0	Cross-term dependence of cdsbs.
pnofffd	0.0	Cross-term dependence of nofffd.
pvofffd	0.0	Cross-term dependence of vofffd.
pk1b	0.0	Cross-term dependence of k1b.
pk2b	0.0	Cross-term dependence of k2b.
pdk2b	0.0	Cross-term dependence of dk2b.
pdvbd0	0.0	Cross-term dependence of dvbd0.
pdvbd1	0.0	Cross-term dependence of dvbd1.
pmoinfd	0.0	Cross-term dependence of moinfd.
pvbs0pd	0.0	Cross-term dependence of vbs0pd.
pvbs0fd	0.0	Cross-term dependence of vbs0fd.

© 2023 Cadence Design Systems, Inc.

vgs_max	infinity	Maximum allowed voltage across gate and source.
vgd_max	infinity	Maximum allowed voltage across gate and drain.
vds_max	infinity	Maximum allowed voltage across drain and source.
vpd_max	infinity	Maximum allowed voltage across external body and drain.
vps_max	vpd_max	Maximum allowed voltage across external body and source.
vgp_max	vgs_max	Maximum allowed voltage across gate and external body.
vge_max	infinity	Maximum allowed voltage across gate and substrate.
ved_max	infinity	Maximum allowed voltage across substrate and drain.
ves_max	infinity	Maximum allowed voltage across substrate and source.
vpe_max	infinity	Maximum allowed voltage across external body and substrate.
vgb_max	vgs_max	Maximum allowed voltage across gate and body.
vbs_max	vbd_max	Maximum allowed voltage across body and source.
vbd_max	infinity	Maximum allowed voltage across body and drain.
vbe_max	infinity	Maximum allowed voltage across body and substrate.
vgsr_max	vgd_max	Maximum allowed reverse voltage across gate and source.

© 2023 Cadence Design Systems, Inc.

vgdr_max	vgd_max	Maximum allowed reverse voltage across gate and drain.
vgpr_max	vgp_max	Maximum allowed reverse voltage across gate and external body.
vpsr_max	vps_max	Maximum allowed reverse voltage across external body and source.
vpdr_max	vpd_max	Maximum allowed reverse voltage across external body and drain.
vger_max	infinity	Maximum allowed reverse voltage across gate and substrate.
vedr_max	infinity	Maximum allowed reverse voltage across substrate and drain.
vesr_max	infinity	Maximum allowed reverse voltage across substrate and source.
vper_max	infinity	Maximum allowed reverse voltage across external body and substrate.
vgbr_max	vgb_max	Maximum allowed reverse voltage across gate and body.
vbsr_max	vbs_max	Maximum allowed reverse voltage across body and source.
vbdr_max	vbd_max	Maximum allowed reverse voltage across body and drain.
vber_max	infinity	Maximum allowed reverse voltage across body and substrate.

© 2023 Cadence Design Systems, Inc.

Auto Model Selection

Many models need to be characterized for different geometries in order to obtain accurate results for model development. The model selector program automatically searches for a model with the length and width range specified in the instance statement and uses this model in the simulations.

For the auto model selector program to find a specific model, the models to be searched should be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin` should be given. The selection criteria to choose a model is as follows:

```
lmin <= inst_length < lmax  and   wmin <= inst_width  < wmax
```

Example:

model ModelName ModelType {

```
  1:  <model parameters> lmin=2 lmax=4 wmin=1 wmax=2

  2:  <model parameters> lmin=1 lmax=2 wmin=2 wmax=4

  3:  <model parameters> lmin=2 lmax=4 wmin=4 wmax=6
```

}

Then, for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program would search all the models in the model group with the name `ModelName` and then pick the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program would choose ModelName.2.

You must specify both length (l) and width (w) on the device instance line to enable automatic model selection.

© 2023 Cadence Design Systems, Inc.

Output Parameters

tempeff	(C)	Effective temperature for a single device.
meff		Effective multiplicity factor (m-factor).
weff	(m)	Effective channel width(alias=lx62).
leff	(m)	Effective channel length(alias=lx63).
lpoly	(m)	Effective poly length.
leffcv	(m)	Effective channel length for CV(alias=lx65).
weffcv	(m)	Effective channel width for CV(alias=lx64).
rtheff	(Ω)	Effective thermal resistance.
ctheff	(F)	Effective thermal capacitance.
rseff	(Ω)	Effective source resistance.
rdeff	(Ω)	Effective drain resistance.
phi	(V)	Surface potential (phi alias=lv50).
tox	(m)	Oxide thickness (tox alias=lv51).
gseff	(S)	Effective source parasitic conductance(alias=lv16).
gdeff	(S)	Effective drain parasitic conductance(alias=lv17).
rds	(Ω)	Drain resistance (squares) (alias=lv13).
rss	(Ω)	Source resistance (squares)(alias=lv14).

Note:

© 2023 Cadence Design Systems, Inc.

1. The output of charge “qb”, “qd”, and “qs” are the sum of intrinsic charge and junction charge. The output of capacitors “cdd”, “cdb”, “csb”, “cbd”, “cbb”, and “cbs” are the sum of intrinsic capacitors and junction capacitors.
2. “reversed” means that vds is negative for NMOS or non-negative for PMOS devices. It is not the same with SPICE3.

Related Topics

BSIMSOI MOSFET Model (bsimsoi)

Device Structure

Equivalent Circuit

Device Regions

Global Control Options

Model Equations

Model Version Updates

Model Usage

© 2023 Cadence Design Systems, Inc.

30

HiSIM2 Model (hisim2)

The HiSIM2 (Hiroshima-university STARC IGFET Model) model was developed at Hiroshima University in collaboration with the STARC research center. This is the first complete surface-potential-based MOSFET model for circuit simulation based on the drift-diffusion approximation, which was originally developed by Pao and Sah. The most important advantage of the surface-potential-based modeling is the unified description of device characteristics for all bias conditions. The physical reliability of the drift-diffusion approximation has been proved by 2D device simulations with channel lengths even down to below 0.1μm.

This chapter contains the following information about the HiSIM2 model:

- Model Concepts on page 2361
- Model Usage on page 2362
  - Instance Syntax on page 2362
  - Model Syntax on page 2362
- Model Version and Development on page 2362
- Version Update and Enhancement on page 2363
  - Version 3.2.1 Enhancement on page 2363
  - Version 3.1.1 Enhancement on page 2364
  - Version 3.1.1 Enhancement on page 2364
  - Version 3.1.0 Enhancement on page 2364
  - Version 3.0.0 Enhancement on page 2365
  - Version 2.91 Enhancement on page 2365
  - Version 2.90 Enhancement on page 2365
  - Version 2.80 Enhancement on page 2366

© 2023 Cadence Design Systems, Inc.

- Version 2.70 Enhancement on page 2366
- Version 2.70 Enhancement on page 2366
- Version 2.61 Enhancement on page 2367
- Version 2.60 Enhancement on page 2367

■ Reference on page 2368

- Model Equations on page 2368
- Component Statements on page 2406

© 2023 Cadence Design Systems, Inc.

Model Concepts

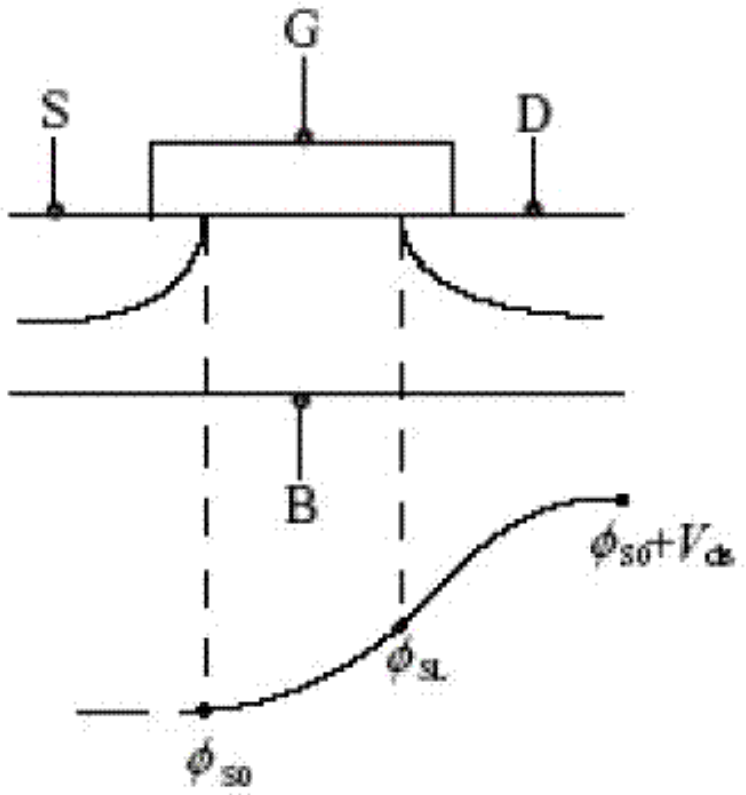


Figure 30-1 Schematic of the surface potential distribution in the channel

The figure shows the schematic of the surface potential distribution in the channel. To obtain analytical solutions for describing device performances, the charge sheet approximation of the inversion layer with zero thickness has been introduced. Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side (ϕ_{S0}) and at the drain side (ϕ_{SL}). These surface potentials are functions of applied voltages on the four MOSFET terminals; the gate voltage Vg, the drain voltage Vd, the bulk voltage Vb and the reference potential of the source Vs. This is the long-channel basis of the HiSIM model, and extensions of the model approximations are done for advanced technologies. All newly appearing phenomena such as short-channel and reverse-short-channel effects are included in the surface potential calculations causing modifications resulting from the features of these advanced technologies.

© 2023 Cadence Design Systems, Inc.

Model Usage

HiSIM2 model definition is used to describe the behavior of devices which has same model characteristic and the instance parameters can be used to describe the characteristics that belong to the specific device.

Instance Syntax

HiSIM2 instance need specify 4 terminals. To specify HiSIM2 instance element, the ModelName has to be associated with a HiSIM2 model card.

```
InstanceName d g s b [th] HiSIM2ModelName parameter=value ...
```

Sample Instance Statement

```
m1 (vdd vgg vss vbb) n_ch w=10u l=2u m=1 nf=10
```

For more instance parameters, refer to Reference on page 2368.

Model Syntax

The following syntax specifies HiSIM2 model:

```
model ModelName hisim2 parameter=value ...
```

The third parameter, `hisim2`, is the master to indicate this model card is a HiSIM2 model card.

Sample Model Statement

```
model n_ch hisim2 type=n version=2.60 tox=3e-8 corsrd=-1 rs=1e-3 rd=5e-2
```

For more model parameters, refer to Reference on page 2368.

Model Version and Development

Spectre/APS asupports the following versions of HiSIM2 model: 2.50, 2.51, 2.60, 2.61, 2.70, 2.80, 2.90, 2.91, 3.10(3.1.0), 3.11(3.1.1), and 3.20(3.2.0). Different model versions can be obtained by setting different model parameter VERSION = 2.50/2.51/2.60/2.61/2.70/2.80/2.90/2.91/3.0.0/3.1.0/3.1.1/3.2.0. 2.50 is set as the default version. The parameter cannot be parameterized, its value must be constant.

© 2023 Cadence Design Systems, Inc.

The following lists the recent model versions and their corresponding simulator version for your reference:

HiSIM2 Version 2.51	MMSIM101_ISR10
HiSIM2 Version 2.60	MMSIM111_ISR6
HiSIM2 Version 2.61	MMSIM111_ISR11
HiSIM2 Version 2.70	MMSIM131
HiSIM2 Version 2.80	MMSIM141
HiSIM2 Version 2.90	SPECTRE17.1
HiSIM2 Version 2.91	SPECTRE17.1
HiSIM2 Version 3.0.0	SPECTRE18.1
HiSIM2 Version 3.1.0	MMSIM18.1 ISR8
HiSIM2 Version 3.1.1	MMSIM18.1 ISR8
HiSIM2 Version 3.2.0	SPECTRE21.1

If you still have any questions, contact Cadence Customer Support team.

Version Update and Enhancement

Version 3.2.1 Enhancement

- Implemented clamp of forward back bias for vertically non-uniform doping (VNUD)effects model. This bug fix ensures protection against a negative input to sqrt().
- Added a new model parameter "`VBSRFAR`", allowing users to set the maximum reverse back bias value (that is, the farthest from zero).
- Extended the implementation of the VNUD model to include retrograde cases where `NSUBD` > `NSUBC`.
- The temperature dependence of $^{2\Phi_B}$ is now implemented in submodels, such as `Vth` shift associated with short-channel effects, reverse-short-channel effects, and GID(S)L. In these submodels, $^{2\Phi_B}$ now takes into account the temperature other than `300K`.
- The model flag `COPB20COMPAT` switches $^{2\Phi_B}$:
  - The recommended setting is `COPB20COMPAT=0`, which uses the temperature-dependent $^{2\Phi_B}$.

© 2023 Cadence Design Systems, Inc.

- However, for backward compatibility, the user can set `COPB20COMPAT=1` to use $^{2\Phi_B}$ at a temperature `T=300K`.

Version 3.1.1 Enhancement

Bug fix for backward compatibility in `* Qbd_swg` and `Qbs_swg` when `CODIO=0`.

Version 3.1.0 Enhancement

- Improvements in the depletion mode model
  - Added model flag for selection of `Vds,sat` treatment:

    ```
    + COVDSRES = 3 : ln(1+ exp) function(default)
                = -1 : Vds
    ```

  - New model parameters are added
  - Value of the following model parameter are updated:
    - `+ DEPQF = 4 -> 0.01`
    - `+ DEPPS = 0.05 -> 0.01`
- Added model parameters for Vertical-Doping-Inhomogeneity model. This model accounts for vertical-doping inhomogeneity as a shift of threshold voltage from the uniform doping case.
- Added model flag for selection model in deep punchthrough model. This model gives better capability of subthreshold slope.
- Updated oxide thickness in the overlap region:

  ```
  + TOXOV = 3.0e-9
  + OVINVDLT = 75.0
  ```

- Improvement in lateral diffusion of the S/D under the gate for better capacitance fitting:

  ```
  + XLDC = 0
  + XWDC = 0
  ```

- Added selector to include improved diode model:

  ```
  + CODIO = 0 (default)
  ```


© 2023 Cadence Design Systems, Inc.

`= 1 (improved)`

- Bug fixed on the induced gate noise for `Flip_N` and `Flip_P` tests.

Version 3.0.0 Enhancement

- Depletion mode model (`CODEP=3`) is implemented with improvements on the capacitance characteristics.

Version 2.91 Enhancement

Following bugs were fixed:

- RD/RS calculations in reverse mode.
- Negative Cdd/Css issue in `CODEP=2`. This fix causes non-backward compatibility, therefore, a flag COFIXCSS has been introduced to fix the issue.
  - `COFIXCSS=1` fixes the negative capacitance. Code is non-backward compatible.
  - `COFIXCSS=0` has negative capacitance. Code is backward compatible. (Default)

Note: The flag is only for HiSIM2 version 2.9.1. For HiSIM2 version 3.0.0 and future releases, the fix for negative capacitance will be implemented.

Version 2.90 Enhancement

- Improvement of the depletion mode model with `CODEP=2`, where `CODEP=1` refers to the version 2.8.0 model.
- Addition of a model parameter for the junction leakage current at the gate-edge sidewall.
- Improvement in the temperature dependence of Isub.
- Improvement in the ranges in parameter declaration.
- Addition of range checking for model parameter values and binning after calculation of `Lgate` and `Wgate`.
- Cleaning of source code.
- Bugs fixes:
  - Discontinuity in the derivative of Isub in `CODEP=1`.
  - Non-convergence when `CODEP=1` and `COIIGS=1`.

© 2023 Cadence Design Systems, Inc.

- Removal of uninitialized variable problem.
- Removal of hidden state problem.

Version 2.80 Enhancement

- New depletion mode MOSFET model introduced. It is activated with the flag CODEP=1.

  Note: Currently, STI leakage, channel length modulation, thermal noise and induced gate noise are not supported in this depletion mode model.
- Improved $V_{ds,eff}$ calculation with new model flag CODDLT=1.
- Range changed for parameters RSH, QME2, QME3, and VFBC.
- Default values of parameters QME2, DDLTICT and DDLTSLP VFBC , NSUBC , LP , NSUBP and MUESR1 changed when CODEP=1
- Bugs fixes:
  - Thermal noise when CORSRD>0 is fixed
  - Model for substrate current Isub
  - Floating point exception in the Fn_Pow function
  - Vbs dependence of the printed output for Vth

Version 2.70 Enhancement

- Unit conversion from CGS to MKS
- Change in model descriptions
  - Suppression of error messages from the range check when new the model flag `COERRREP` is set to 0
  - Improvement of GIDL current model with new model parameters `GIDL6` and `GIDL7`
  - Improvement of STI effect model with new model parameters `NSUBCSTI1`, `NSUBCSTI2`, and `NSUBCSTI3`
  - Introduction of gate length dependence for `VFBC` with new model parameters `VFBCL` and `VFBCLP`
  - Improvement of smoothness of the NSUBPFAC model with the new model parameter `NSUBPDLT`

© 2023 Cadence Design Systems, Inc.

- Invalidation of the NSUBPFAC model when NSUBPFAC = 1
- Range check of model parameters NSUBPFAC and NSUBPDLT

- Bug fixes:
  - Calculation of MUEPH1 when CODFM=1
  - Resetting of SC4 value when CORECIP=1
  - Calculation of some derivatives
  - Floating point exception in the smoothing functions
  - High-field effect model with model parameter GDLD
  - Code improvements of Fn_POW and Fn_SZ functions for higher exception robustness

Version 2.61 Enhancement

- Missing initialization of NSUBC, NSUBP, and MUEPH1 in the Initialize for repeating simulation
- Unit converting in the Initialize
- Derivative calculations in the Q_{over} model code
- Floating point exception in the QME model code
- Floating point exception in the smoothing functions

Version 2.60 Enhancement

- Introduction of the Well Proximity Effect model with new parameters:
  - Instance parameters: SCA , SCB, and SCC
  - Model parameters: WEB , WEC , NSUBCWPE , NSUBPWPE, and NPEXTWPE
- Improvement of the overlap capacitance model
- Activation of Induced Gate Noise model
- Change the default value of the instance parameters NRD and NRS.

© 2023 Cadence Design Systems, Inc.

Reference

Model Equations

Effective Length and Width

L_{gate} and W_{gate} are the gate length and gate width. They are calculated from the gate drawn length and width.

$$L_{gate} = L_{drawn} + XL$$

$$W_{gate} = \frac{W_{drawn}}{NF} + XW$$

$$L_{poly} = L_{gate} - 2\ \mathrm{X} \frac{LL}{(L_{gate} + LLD)^{LLN}}$$

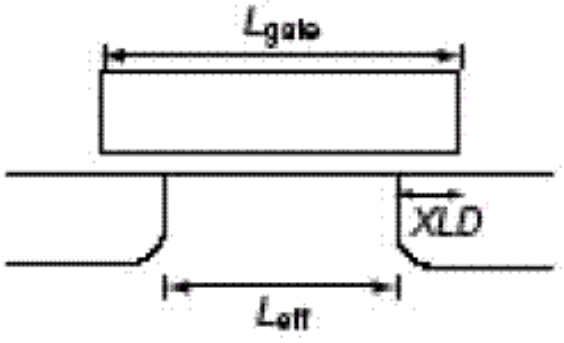
$$W_{poly} = W_{gate} - 2\ \mathrm{X} \frac{WL}{(W_{gate} + WLD)^{WLN}}$$

$$L_{eff} = L_{poly} - 2\ \mathrm{X}\ XLD$$

$$W_{eff} = W_{poly} - 2\ \mathrm{X}\ XWD$$

where XLD and XWD account for the overlaps of source/drain contact and gate oxide. LL, LLD, LLN, WL, WLD, and WLN are further model parameters for including L_{gate} or W_{gate} dependencies on L_{eff} and W_{eff}.

Figure 30-2 Cross section of the device



© 2023 Cadence Design Systems, Inc.

Charge

All device characteristics are determined on the basis of the charge control by applied voltages and by expressing the MOSFET charges as functions of the surface potentials. Under the charge-sheet approximation the charges on the four MOSFET terminals Q_G(gate), Q_B (bulk), Q_D (drain), and Q_S (source), are described as:

$$Q_G = -(Q_B + Q_I) = -Q_{SP}$$

$$Q_B = W_{eff} * NF * \int_0^{L_{eff}} Q_b(y)dy$$

$$Q_I = W_{eff} \int_0^{L_{eff}} Q_i(y)dy$$

$$Q_D = W_{eff} \int_0^{L_{eff}} \frac{y}{L_{eff}} Q_i(y)dy$$

$$Q_S = Q_I - Q_D$$

where Q_I is the inversion charge, Q_{SP} is the space charge, and y is the position along the channel. L_{eff} and 0 are the channel-end positions at the drain side and the source side, respectively.

By applying the Gauss law, the space charge density Q_{SP} is derived from the Poisson equation.

$$-Q_{SP} = C_{ox}(V_G' - \varphi_s(y))$$

$$C_{ox} = \frac{\varepsilon_{ox}}{TOX}$$

$$V_G' = V_{gs} - VFBC + \Delta Vth$$

$$\beta = \frac{q}{kT}$$

where VFBC is the at-band voltage, TOX is the physical gate-oxide thickness, and ΔVth is the threshold voltage shift in comparison to the threshold voltage of a long-channel transistor. The

© 2023 Cadence Design Systems, Inc.

electron charge is denoted by q, and ε_{si} and N_{sub} are the silicon permittivity and the substrate impurity concentration, respectively. The Boltzmann constant and the lattice temperature in Kelvin are k and T, respectively.

The quasi-Fermi potential ϕ_f (f) preserves the following relationship:

$$\varphi_f(L_{eff}) - \varphi_f(0) = V_{ds,eff}$$

$$V_{ds,\,eff} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_{ds,\,sat}}\right)^{\Delta}\right]^{\frac{1}{\Delta}}}$$

for CODDLT=1 (default):

$$\Delta = \frac{DDLTMAX \cdot T1}{DDLTMAX + T1} + DDLTICT$$

$$T1 = DDLTSLP \cdot L_{gate} \cdot 10^{6}$$

for CODDLT=0 (previous model):

$$\Delta = \frac{DDLTMAX \cdot T1}{DDLTMAX + T1} + 1$$

$$T1 = DDLTSLP \cdot L_{gate} \cdot 10^{6} + DDLTICT$$

The electron concentration at equilibrium condition n_{p0} is

$$n_{p0} = \frac{n_i^2}{P_{p0}}$$

© 2023 Cadence Design Systems, Inc.

where the intrinsic carrier concentration n_i is

$$n_i = n_{i0} T^{\frac{1}{2}} \exp\left(-\frac{E_g}{2q}\beta\right)$$

p_{p0} is approximated to be N_{sub}, and E_g describes the temperature dependence of the bandgap.

The Poisson equation and the Gauss law are used to derive the inversion charge and bulk charge related charge-density equations under the assumption of a homogeneous substrate impurity distribution as

$$Q_b(y) = -\sqrt{\frac{2\varepsilon_{si} q N_{sub}}{\beta}} [\exp\{-\beta(\varphi_s(y) - V_{bs})\} + \beta(\varphi_s(y) - V_{bs})]^{1/2}$$

$$Q_i(y) = -C_{ox}(V_G{}' - \varphi_s(y)) + \sqrt{\frac{2\varepsilon_{si} q N_{sub}}{\beta}} [\exp\{-\beta(\varphi_s(y) - V_{bs})\} + \beta(\varphi_s(y) - V_{bs}) - 1]^{1/2}$$

Drain Current

Under gradual-channel approximation with further approximations of an idealized gate structure and uniform channel doping, the drift-diffusion approximation describes the drain current I_{ds} as:

$$I_{ds} = \frac{W_{eff}{}^{*}NF}{L_{eff}} * \mu * \frac{I_{dd}}{\beta}$$

$$I_{dd} = C_{ox}(\beta V_G{}' + 1)(\varphi_{SL} - \varphi_{S0}) - \frac{\beta}{2} C_{ox}(\varphi_{SL}^2 - \varphi_{S0}^2)$$

$$-\frac{2}{3} const0[\{\beta(\varphi_{SL} - V_{bs}) - 1\}^{3/2} - \{\beta(\varphi_{S0} - V_{bs}) - 1\}^{3/2}]$$

$$+ const0[\{\beta(\varphi_{SL} - V_{bs}) - 1\}^{1/2} - \{\beta(\varphi_{S0} - V_{bs}) - 1\}^{1/2}]$$

$$\varphi_{S0} = 2\varphi_B, \varphi_B = \frac{2}{\beta} ln\left(\frac{N_{sub}}{n_i}\right)$$

$$\varphi_{SL} = 2\varphi_B + V_{ds}$$

© 2023 Cadence Design Systems, Inc.

The description for the long-channel case is obtained as:

$$I_{ds} = \frac{W_{eff}{}^{*}NF}{L_{eff}}\mu^{*}C_{ox}\left[(V_G{}' - V_{th})V_{ds} - \left(\frac{1}{2} + \frac{\sqrt{2\varepsilon_{si}\cdot qN_{sub}}}{4C_{ox}\sqrt{2\varphi_B}}\right)V_{ds}^2\right]$$

$$V_{th} = VFBC + 2\varphi_B + \frac{\sqrt{2\varepsilon_{si}\cdot qN_{sub}}}{C_{ox}}\sqrt{2\varphi_B}$$

Threshold Voltage Shift

Different from the drift approximation, the drift-diffusion approximation does not require a threshold voltage parameter Vth for describing device performances. The MOSFET device parameters, such as the oxide thickness T_{OX} and the substrate doping concentration NSUBC determine the complete MOSFET behavior including the subthreshold characteristics automatically and consistently. The measured V_{th} is influenced by various phenomena, such as the short-channel effects, which cause a reduction of Vth for short-channel transistors in comparison to long-channel transistors as shown in Fig. 5. This so-called ΔV_{th} roll-off is dependent on the technology applied for MOSFET fabrication. Therefore, HiSIM can derive many detailed information on the MOSFET fabrication technology, which is relevant for modeling device characteristics, from the V_{th} changes (ΔV_{th}) as a function of gate length (L_{gate}). The modeled ΔV_{th} is incorporated in the ϕ_S iteration, and can be viewed as consisting of two main effects or components:

1. The short-channel effect: $\Delta V_{th,SC}$
2. The reverse-short-channel effect: $\Delta V_{th,R}$ and $\Delta V_{th,P}$

The separation into these components is shown below:

Short-Channel Effect

Four important phenomena are observed:

1. Reduction of Vth for reduced Lgate
2. Vth dependence on Vds
3. Reduction of the body effect

© 2023 Cadence Design Systems, Inc.

4. Increase of the subthreshold swing, which is often not obvious for the normal case of fabrication technologies. Recent advanced technologies utilize aggressive scaling, which induces observable subthreshold degradation.

$$\Delta V_{th,SC} = \frac{\varepsilon_{si}}{C_{ox}} W_d \frac{dE_y}{dy}$$

where W_d is the depletion-layer thickness written as

$$W_d = \sqrt{\frac{2\varepsilon_{si}(2\varphi_B - V_{bs})}{qN_{sub}}}$$

$$2\varphi_B = \frac{2}{\beta} 1n\left(\frac{N_{sub}}{n_i}\right)$$

dE_y/dy is derived with model parameters in the form

$$\frac{dE_y}{dy} = \frac{2\{VBI - 2\varphi_B\}}{(L_{gate} - PARL2)^2}\left(SC1 + SC2*V_{ds} + SC3*\frac{2\varphi_B - V_{bs}}{L_{gate}} + SC4 \cdot V_{ds}(2\varphi_B - V_{bs})\right)$$

Reverse-Short-Channel Effects

Impurity concentration inhomogeneity in the direction vertical to the channel (Retrograded Implantation)

$$\Delta V_{th,R} = \frac{Q_{dep}}{C_{ox}} - \frac{Q_{dep}(long)}{C_{ox}}$$

$$Q_{dep} = q\int_0^{Wd} N_{sub}(\chi)d\chi$$

$$Q_{dep} = QDEPCC + \frac{QDEPCL}{L_{gate}^{QDEPCS}} + \left(QDEPBC + \frac{QDEPBL}{L_{gate}^{QDEPBS}}\right)\sqrt{2\varphi_B - V_{bs}}$$

$$Q_{Bmod} = \sqrt{2q \cdot N_{sub} \cdot \varepsilon_{si} \cdot \left(2\varphi_B - V_{bs} - \frac{BS1}{BS2 - V_{bs}}\right)}$$

© 2023 Cadence Design Systems, Inc.

where BS1 represents the strength of the deviation and BS2 is the starting value of Vbs where the deviation becomes visible.

© 2023 Cadence Design Systems, Inc.

Impurity concentration inhomogeneity in the lateral direction parallel to the channel (Pocket Implantation)

$$\Delta V_{th,P} = (\Delta V_{th,R} - V_{th0})\frac{\varepsilon_{si}}{C_{ox}} W_d \frac{dE_{y,P}}{dy} + dqb$$

$$V_{th,R} = VFBC + 2\varphi_B + \frac{Q_{B0}}{C_{ox}} + \frac{1}{\beta}\log\left(\frac{N_{subb}}{NSUBC}\right)$$

$$Q_{B0} = \sqrt{2q \cdot N_{sub} \cdot \varepsilon_{si} \cdot (2\varphi_B - V_{bs})}$$

$$V_{th0} = VFBC + 2\varphi_{BC} + \frac{\sqrt{2q \cdot NSUBC \cdot \varepsilon_{si} \cdot (2\varphi_{BC} - V_{bs})}}{C_{ox}}$$

$$N_{subb} = 2 \cdot NSUBP - \frac{(NSUBP - NSUBC) \cdot L_{gate}}{LP} - NSUBC$$

$$dqp = \frac{Q_{B0} - Q_{Bmod}}{C_{ox}}$$

$$\varphi_{BC} = \frac{2}{\beta} ln\left(\frac{NSUBC}{n_i}\right)$$

$$\varphi_B = \frac{2}{\beta} ln\left(\frac{N_{sub}}{n_i}\right)$$

$$N_{sub} = \frac{NSUBC(L_{gate} - LP) + NSUBP \cdot LP}{L_{gate}}$$

$$\Delta V_{th,P} = \Delta V_{th,P} - \frac{SCP22}{(SCP21 + V_{ds})^2}$$

$$N_{sub} = N_{sub} + \frac{NPEXT - N_{subc}}{\left(\frac{1}{\chi\chi} + \frac{1}{LPEXT}\right) L_{gate}}$$

© 2023 Cadence Design Systems, Inc.

where

$$\chi\chi = 0.5 \cdot L_{gate} - LP$$

CORECIP = 1 for Accurate Reciprocity Calculation of Capacitances

The model CORECIP enables accurate calculation of the capacitance reciprocity. If CORECIP = 1 is selected, the V_{ds} dependence is moved to the puchthrough model described in the next section. Accordingly, model parameters SC2,SC4,SCP2 and SCP4 must be set to zero, and PT2 and PT4 activated.

Short Channel Effects

Punchthrough Effect

The origin of the punchthrough effect is the bipolar effect through source, substrate, and drain.The effect is described by a power function of the potential difference instead of the exponential function as

$$POTENTIAL = (VBI - \varphi_{s0})^{PTP}$$

The final drain current I_{ds} is written

$$I_{ds} = I_{ds} + PUNCH$$

$$PUNCH = \frac{W_{eff} \cdot NF}{L_{eff}} \frac{\mu}{\beta} \cdot (\varphi_{SL} - \varphi_{S0})$$

$$\cdot \left\{ C_{ox} \cdot \beta \frac{PTL}{(L_{gate} \cdot 10^6)^{PTLP}} \cdot POTENTIAL \cdot \left(1 + PT2 \cdot V_{ds} + \frac{PT4 \cdot (\varphi_{s0} - V_{bs})}{(L_{gate} \cdot 10^6)^{PT4P}} \right) \right\}$$

© 2023 Cadence Design Systems, Inc.

Channel Conductance

The high field under the saturation condition causes the pinch-off region and the current flows away from the surface. This effect is considered as the lateral-field-induced charge for the capacitance. The simplified formulation is applied to consider the effect as

$$I_{ds} = I_{ds} + \frac{W_{eff} \cdot NF}{L_{eff}} \frac{\mu}{\beta} \cdot (\varphi_{SL} - \varphi_{S0}) \cdot CONDUCTANCE$$

$$CONDUCTANCE = C_{ox} \cdot \beta \frac{GDL}{(L_{gate} \cdot 10^{6} + GDLD \cdot 10^{6})^{GDLP}} \cdot V_{ds}$$

Pocket Impurity Concentration Reduction

If the gate length becomes shorter, the pocket-impurity concentration may become lower than for long channels. This effect is modeled as:

$$N_{subp} = NSUBP \cdot \left(\frac{2 \cdot (1 - NSUBPFAC)}{NSUBPL} \cdot L_{gate} \cdot 10^{6} + 2 \cdot NSUBPFAC - 1 \right)$$

Depletion Effect of the Gate Poly-Si

Carrier depletion in the gate poly-Si occurs due to the relatively low impurity concentration of the poly-Si in the region above the gate-oxide. Nevertheless, this concentration is usually much higher than the impurity concentration in the substrate. Therefore, carrier depletion in the poly-Si near the gate-oxide interface starts after the formation of the inversion layer in the

© 2023 Cadence Design Systems, Inc.

substrate. For modeling the gate poly-Si depletion a physical model parameter, namely the impurity concentration in the gate poly-Si (N_{pg}), is introduced.

$$V_G' - \varphi_S - \varphi_{Spg} = -\frac{Q_{SP}}{C_{ox}} = \frac{\varepsilon_{si} E_{Si}}{C_{ox}}$$

$$E_{pg} = qN_{pg}L_{D,pg}\sqrt{2}\left[\{\exp(-\beta\varphi_{Spg}) + \beta\varphi_{Spg} - 1\} + \frac{n_{p0,pg}}{p_{p0,pg}}\{\exp(-\beta\varphi_{Spg}) - \beta\varphi_{Spg} - 1\}\right]^{\frac{1}{2}}$$

$$E_{pg} = qN_{pg}L_{D,pg}\sqrt{2}(\beta\varphi_{Spg} - 1)^{\frac{1}{2}}$$

$$\varphi_{Spg} = PGD1\left(1 + \frac{1}{L_{gate}\cdot 10^6}\right)^{PGD4}\exp\left(\frac{V_{gs} - PGD2}{V}\right)$$

Quantum-Mechanical Effects

The main quantum-mechanical phenomenon, which has to be included into a MOSFET model for circuit simulation, is the repulsion of the channel's carrier-density peak into the substrate away from the surface. This can be described phenomenologically by an increased effective oxide thickness T_{ox}. Two major approximations are introduced to derive a simple set of equations for T_{ox}: First, a triangular potential perpendicular to the channel is approximated and second, carriers are assumed to occupy only the lowest quantized energy level. The resulting effective oxide thickness T_{ox} can be written as:

$$T_{ox} = TOX + \Delta T_{ox}$$

For HiSIM2.5

$$\Delta T_{ox} = \frac{QME1}{QME2^2}(V_{gs} - V_{th}(T_{ox} = TOX) - QME2)^2 + QME3$$

© 2023 Cadence Design Systems, Inc.

For HiSIM2.5.1

$$\Delta T_{ox} = \frac{QME1}{V_{gb} - V_{th}(T_{ox} = TOX) + QME2} + QME3$$

Mobility Model

Here E_{eff} is the effective field normal to the surface and is written as:

$$\frac{1}{\mu_0} = \frac{1}{\mu_{CB}} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}$$

$$\mu_{CB}(Coulomb) = M_{Coulomb0} + M_{Coulomb1}\frac{Q_i}{q \cdot 10^{11}}$$

$$\mu_{PH}(phonon) = \frac{Muephonon}{E_{eff}^{MUEPH0}}$$

$$\mu_{SR}(roughness) = \frac{MUESR1}{E_{eff}^{M_{uesurface}}}$$

Here E_{eff} is the effective field normal to the surface and is written as

$$E_{eff} = \frac{1}{\varepsilon_{Si}}(N_{dep} \cdot Q_b + NINV \cdot Q_i) \cdot f(\varphi_s)$$

$$f(\varphi_s) = \frac{1}{1 + (\varphi_{S0} - \varphi_{SL}) \cdot NINVD}$$

where N_{dep} considers the gate length dependence with two model parameters NDEPL and NDEPLP as:

$$N_{dep} = NDEP\frac{(L_{gate} \cdot 10^6)^{NDEPLP}}{NDEPL + (L_{gate} \cdot 10^6)^{NDEPLP}}$$

© 2023 Cadence Design Systems, Inc.

The mobility preserves the following conditions:

$$MUEPH0 \approx 0.3$$
$$M_{uesurface} = 2.0$$
$$NDEP = 1.0$$
$$NINV = 0.5$$

Due to the carrier ow at increasing distance from the surface with reducing Lgate, the electric field experienced by the carriers is different from the field in the long Lgate case. This results in a modification of $M_{uephonon}$, which is modeled as:

$$M_{uephonon} = MUEPH1 \cdot \left(1 + \frac{MUEPHL}{(L_{gate} \cdot 10^6 + MUEPLD \cdot 10^6)^{MUEPLP}}\right) \cdot \left(1 + \frac{MUEPHL2}{(L_{gate} \cdot 10^6)^{MUEPLP2}}\right)$$

The surface roughness co-efficient $M_{uesurface}$ is modelled to have a similar channel length dependence written as:

$$M_{uesurface} = MUESR0 \cdot \left(1 + \frac{MUESRL}{(L_{gate} \cdot 10^6)^{MUESLP}}\right)$$

The high field mobility is modeled as:

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_y}{V_{max}}\right)^{BB}\right)^{\frac{1}{BB}}}$$

© 2023 Cadence Design Systems, Inc.

where the maximum velocity V_{max} is temperature dependent. V_{max} should be the maximum electron-saturation velocity (' 1_107cm=s), which is exceeded at reduced L_{gate}. This is called velocity overshoot, and is included in the mobility model in the following manner:

$$V_{max} = VMAX \cdot \left(1 + \frac{VOVER}{(L_{gate} \cdot 10^6)^{VOVERP}} \right)$$

Channel-Length Modulation

The gradual-channel approximation is applied to derive analytical equations for describing device characteristics. However, this approximation is not valid for large Vds causing the pinch-off phenomenon in the channel. Without taking into account the pinch-off phenomenon, the calculated channel conductance gds enters abruptly into the saturation condition. To include the pinch-off phenomenon in HiSIM, we apply the conventional method of modeling the pinch-off region (ΔL) separately from the rest of the channel.

$$\Delta L = \varepsilon_{Si} \frac{E_D - E_C}{qN_{sub} + Q_i / W_d}$$

where

$$E^2_D = E^2_C + \frac{2qN_{sub}}{\varepsilon_{Si}} (\varphi_S(\Delta L) - \varphi_{SL})$$

and E_c is the electric field at y=0'.

$$E_C = \frac{Idd}{\beta (L_{eff} - \Delta L) Q_i}$$

The above equation can be simplified as follows:

$$E_C = \frac{Idd}{\beta L_{eff} Q_i}$$

$$\varphi_S(\Delta L) = (1 - CLM1) \cdot \varphi_{SL} + CLM1 \cdot (\varphi_{S0} + V_{ds})$$

© 2023 Cadence Design Systems, Inc.

Narrow Channel Effects

Threshold Voltage Modification

$$\Delta V_{th,W} = \left(\frac{1}{C_{ox}} - \frac{1}{C_{ox} + 2C_{ef}/(L_{eff}W_{eff})}\right) qN_{sub}W_d + \frac{WVTH0}{W_{gate} \cdot 10^6}$$

where WVTH0 is the parameter for including the basic width dependence and

$$C_{ef} = \frac{2\varepsilon_{ox}}{\pi} L_{eff} ln\left(\frac{2T_{fox}}{T_{ox}}\right) = \frac{WFC}{2} L_{eff}$$

Here, T_{fox} is the thickness of the oxide at the trench edge, and WFC is the model parameter for including the edge-fringing-capacitance effects.

$$\Delta V_{th} = \Delta V_{th,SC} + \Delta V_{th,R} + \Delta V_{th,P} + \Delta V_{th,W} - \varphi_{Spg}$$

Mobility Change

$$M_{uephonon} = M_{uephonon} \cdot \left(1 + \frac{MUEPHW}{(W_{gate} \cdot 10^6 + MUEPWP \cdot 10^6)^{MUEPWP}}\right) \cdot \left(1 + \frac{MUEPHW2}{(W_{gate} \cdot 10^6)^{MUEPWP2}}\right)$$

$$M_{uesurface} = M_{uesurface} \cdot \left(1 + \frac{MUESRW}{(W_{gate} \cdot 10^6)^{MUESWP}}\right)$$

© 2023 Cadence Design Systems, Inc.

Transistor Leakage due to Shallow Trench Isolation (STI): Hump in Ids

The shallow trench isolation induces also an undesired hump in the subthreshold region of the Ids-Vgs characteristics. This is due to an increased electric field at the edge of the trench. At this trench edge, the impurity concentration as well as the oxide thickness are different from the MOSFET middle position along the width direction. Therefore, the surface potential values are expected to be different at the trench edge and are found to cause a Vth reduction there. Thus a MOSFET leakage current occurs at these edges, which is smaller than the main MOSFET. The leakage current equation is written as:

$$I_{ds,STI} = 2\frac{W_{STI}}{L_{eff}-\Delta L}\mu\frac{Q_{i,STI}}{\beta}[1-\exp(-\beta V_{ds})]$$

where W_{STI} determines the width of the high-field region.

$$W_{STI} = WSTI\left(1+\frac{WSTIL}{(L_{gate,sm}\cdot 10^{6})^{WSTILP}}\right)\left(1+\frac{WSTIW}{(W_{gate}\cdot 10^{6})^{WSTIWP}}\right)$$

Small Geometry

Small size devices do not show the same scaling characteristic as long-channel or wide-channel devices, but deviate significantly. The reason is mainly due to the resolution inaccuracy of the lithography. The small geometry effects are modeled first as the threshold voltage shift

$$\Delta V_{th} = \Delta V_{th,SC}+\Delta V_{th,R}+\Delta V_{th,P}+\Delta V_{th,W}+\Delta V_{th,sm}-\varphi_{Spg}$$

$$\Delta V_{th,sm} = \frac{WL2}{wl^{WL2P}}$$

© 2023 Cadence Design Systems, Inc.

The mobility modification due to the small device geometry is also modeled in the phonon scattering as

$$M_{uephonon} = M_{uephonon} \cdot \left(1 + \frac{MUEPHS}{wl^{MUEPSP}}\right)$$

$$V_{max} = V_{max} \cdot \left(1 + \frac{VOVERS}{wl^{VOVERSP}}\right)$$

Effects of the Source/Drain Diffusion Length for Shallow Trench Isolation (STI) Technologies

The diffusion length, LOD between MOSFET gate and STI edge affects the MOSFET characteristics.

$$N_{substi} = \frac{1 + T1 \cdot T2}{1 + T1 \cdot T3}$$

where

$$T1 = \frac{1}{1 + NSUBPSTI2}$$

$$T2 = \left(\frac{NSUBPSTI1}{L_{od_\mathrm{half}}}\right)^{NSUBPSTI3}$$

$$T3 = \left(\frac{NSUBPSTI1}{L_{od_\mathrm{half_ref}}}\right)^{NSUBPSTI3}$$

$$N_{subp} = N_{subp} \cdot N_{substi}$$

$$M_{uesti} = \frac{1 + T1 \cdot T2}{1 + T1 \cdot T3}$$

© 2023 Cadence Design Systems, Inc.

where

$$T1 = \frac{1}{1 + MUESTI2}$$

$$T2 = \left(\frac{MUESTI1}{L_{od_half}}\right)^{MUESTI3}$$

$$T3 = \left(\frac{MUESTI1}{L_{od_half_ref}}\right)^{MUESTI3}$$

$$M_{uephonon} = M_{uephonon} \cdot M_{uesti}$$

Temperature Dependences

The temperature dependence is included automatically in the surface potentials through β, which is the inverse of the thermal voltage. Additionally the bandgap, the intrinsic carrier concentration, the carrier mobility, and the carrier saturation velocity are also temperature dependent. The temperature dependence of the bandgap determines the temperature dependence of V_{th} and is modeled as:

$$E_g = E_{g,TNOM} - BGTMP1 \cdot (T - TNOM) - BGTMP2 \cdot (T^2 - TNOM^2)$$

where T is the given temperature, and

$$E_{g,TNOM} = EG0 - 90.25 \times 10^{-6} \cdot TNOM - 1.0 \times 10^{-7} \cdot TNOM^2$$

© 2023 Cadence Design Systems, Inc.

where T is the given temperature. The temperature dependence of the intrinsic carrier concentration is given by

$$n_i = n_{i0} \cdot T^{\frac{3}{2}} \cdot \exp\left(-\frac{E_g}{2q}\beta\right)$$

$$\mu_{PH}(phonon) = \frac{M_{uephonon}}{(T/TNOM)^{MUETMP} \times E_{eff}^{MUEPH0}}$$

$$V_{max} = \frac{VMAX}{1.8 + 0.4(T/TNOM) + 0.1(T/TNOM)^2 - VTMP \times (1 - T/TNOM)}$$

The temperature dependence of the gate current is given by modifying the bandgap specific for the gate current as:

$$E_{gp} = E_{g,TNOM} + EGIG + IGTEMP2\left(\frac{1}{T} - \frac{1}{TNOM}\right) + IGTEMP3\left(\frac{1}{T^2} - \frac{1}{TNOM^2}\right)$$

Resistances

The source and the drain resistances R_s and R_d are considered by voltage drops on each terminal as:

$$V_{gs,eff} = V_{gs} - I_{ds} \cdot R_s$$
$$V_{ds,eff} = V_{ds} - I_{ds} \cdot (R_s + R_d)$$
$$V_{bs,eff} = V_{bs} - I_{ds} \cdot R_s$$

where

$$R_s = \frac{RS}{W_{eff} \cdot NF} + NRS \cdot RSH$$
$$R_d = \frac{RD}{W_{eff} \cdot NF} + NRD \cdot RSH$$

© 2023 Cadence Design Systems, Inc.

The flag CORSRD is provided for the selection of one of the possible approaches. `CORSRD = 0` refers to no contact resistance. `CORSRD =1, 2, -1` means "internal", "analytical", and "external" source/drain resistances, respectively. `CORSRD = 0` is the default. `CORSRD=2` is introduced to avoid simulation time penalty with an analytical description of the resistance effect as:

$$I_{ds} = \frac{I_{ds0}}{1 + I_{ds0}\frac{R_d}{V_{ds}}}$$

where I_{ds0} is the drain current without the resistance effect.

$$R_g = \frac{RSHG \cdot \left(XGW + \frac{W_{eff}}{3 \cdot NGCON}\right)}{NGCON \cdot (L_{drawn} - XGL) \cdot NF}$$

Capacitances

Intrinsic Capacitances

$$Q_y = \varepsilon_{Si} W_{eff} \cdot NF \cdot W_d \left(\frac{\varphi_{S0} + V_{ds} - \varphi_S(\Delta L)}{XQY}\right) + \frac{XQY1 \cdot W_{eff} \times 10^6 \cdot NF}{(L_{gate} \times 10^6)^{XQY2}} V_{bs}$$

Overlap Capacitances

Surface Potential-Based Model

under the depletion and the accumulation conditions

$$Q_{over} = W_{eff} \cdot NF \cdot LOVER \left(\sqrt{\frac{2\varepsilon_{Si} qNOVER}{\beta}} \sqrt{\beta(\varphi_S + V_{ds}) - 1}\right)$$

© 2023 Cadence Design Systems, Inc.

under inverse condition

$$Q_{over} = W_{eff} \cdot NF \cdot LOVER \cdot C_{ox}(V_{gs} - VFBOVER - \varphi_S)$$

Simplified Bias Dependent Model

$$Q_{god} = W_{eff} NF\, C_{ox}[(V_{gs} - V_{ds})LOVER - OVSLP \cdot (1.2 - (\varphi_{SL} - V_{ds})) \cdot (OVMAG + (V_{gs} - V_{ds}))]$$

Extrinsic Capacitances

$$C_f = \frac{\varepsilon_{ox}}{\pi/2} W_{gate} \cdot NF \cdot 1n\left(1 + \frac{TPOLY}{T_{ox}}\right)$$

© 2023 Cadence Design Systems, Inc.

Leakage Currents

Substrate Current

$$I_{sub} = X_{sub1} \cdot P_{sisubsat} \cdot I_{ds} \cdot \exp\left(-\frac{X_{sub2}}{P_{sisubsat}}\right)$$

$$X_{sub1} = SUB1 \cdot \left(1 + \frac{SUB1L}{L_{gate}^{SUB1LP}}\right)$$

$$X_{sub2} = SUB2 \cdot \left(1 + \frac{SUB2L}{L_{gate}}\right)$$

$$P_{sisubsat} = SVDS \cdot V_{ds} + \varphi_{S0} - \frac{L_{gate} \cdot P_{sislsat}}{X_{gate} + L_{gate}}$$

$$X_{gate} = SLG \cdot \left(1 + \frac{SIGL}{L_{gate}^{SLGLP}}\right)$$

$$P_{sislsat} = V_{g2} + \frac{q \cdot \varepsilon_{Si} \cdot N_{sub}}{C_{ox}^{2}} \cdot \left\{1 - \sqrt{1 + \frac{2C_{ox}^{2}}{q \cdot \varepsilon_{Si} \cdot N_{sub}}\left(V_{g2} - \frac{1}{\beta} - X_{vbs} \cdot V_{bs}\right)}\right\}$$

$$X_{vbs} = SVBS \cdot \left(1 + \frac{SVBSL}{L_{gate}^{SVBSLP}}\right)$$

$$V_{g2} = SVGS \cdot \left(1 + \frac{SVGSL}{L_{gate}^{SVGSLP}}\right) \cdot \frac{W_{gate}^{SVGSWP}}{W_{gate}^{SVGSWP} + SVGSW} \cdot V_{gp}$$

© 2023 Cadence Design Systems, Inc.

Impact-Ionization Induced Bulk Potential Change

$$\Delta I_{ds} = \frac{2}{3}\sqrt{\frac{2\varepsilon_{Si}qN_{sub}}{\beta}}[\{\beta(\phi_{SL}-V_{bs})-1\}^{\frac{3}{2}}\frac{3}{2}\frac{\beta\Delta V_{bulk}}{\beta(\phi_{SL}-V_{bs})-1}$$
$$-\{\beta(\phi_{S0}-V_{bs})-1\}^{\frac{3}{2}}\frac{3}{2}\frac{\beta\Delta V_{bulk}}{\beta(\phi_{S0}-V_{bs})-1}]$$
$$-\sqrt{\frac{2\varepsilon_{Si}qN_{sub}}{\beta}}[\{\beta(\phi_{SL}-V_{bs})-1\}^{\frac{1}{2}}\frac{1}{2}\frac{\beta\Delta V_{bulk}}{\beta(\phi_{SL}-V_{bs})-1}$$
$$-\{\beta(\phi_{S0}-V_{bs})-1\}^{\frac{1}{2}}\frac{1}{2}\frac{\beta\Delta V_{bulk}}{\beta(\phi_{S0}-V_{bs})-1}]$$

where

$$\Delta V_{bulk} = IBPC1(1+IBPC2\cdot\Delta V_{th})\cdot I_{sub}$$

IBPC1 and IBPC2 are model parameters.

Gate Current

Between Gate and Channel, Igate

$$I_{gate} = q\cdot GLEAK1\cdot\frac{E^2}{E_{gp}^{\frac{1}{2}}}\cdot\exp\left(-\frac{E_{gp}^{\frac{3}{2}}\times GLEAK2}{E}\right)\cdot\sqrt{\frac{Q_i}{const0}}\cdot W_{eff}\cdot NF\cdot L_{eff}$$
$$\cdot\frac{GLEAK6}{GLEAK6+V_{ds}}\cdot\frac{GLEAK7}{GLEAK7+W_{eff}+L_{eff}}$$

© 2023 Cadence Design Systems, Inc.

where

$$E = \frac{V_G - GLEAK3 \times \varphi_S(\Delta L)}{T_{ox}} \cdot \left(1 + \frac{E_y}{GLEAK5}\right)$$

$$V_G = V_{gs} - VFBC + GLEAK4 \cdot \Delta V_{th} \cdot L_{eff}$$
$$\Delta V_{th} = \Delta V_{th,SC} + \Delta V_{th,P} + \Delta V_{th,W} + \varphi_{Spg}$$
$$I_{gate} = I_{gate,s} + I_{gate,d}$$
$$I_{gate,s} = (1 - P_{artition}) \cdot I_{gate}$$
$$I_{gate,d} = P_{artition} \cdot I_{gate}$$

$$I_{gate,d} = \int_0^{L_{eff}} \frac{y}{L_{eff}} I_{gate}(y)dy = P_{artition} \cdot I_{gate}$$

Between Gate and Bulk, Igb

$$E_{gb} = -\frac{V_{gb} - VFBC + GLKB3}{T_{ox}}$$
$$I_{gb} = GLKB1 \cdot {E_{gb}}^2 \cdot \exp\left(-\frac{GLKB2}{E_{gb}}\right) W_{eff} \cdot NF \cdot L_{eff}$$

Between Gate and Source/Drain. Igs/Igd

$$I_{gs} = sign \cdot GLKSD1 \cdot {E_{gs}}^2 \exp(T_{ox}(-GLKSD2 \cdot V_{gs} + GLKSD3)) W_{eff} \cdot NF$$
$$E_{gs} = \frac{V_{gs}}{T_{ox}}$$
$$I_{gd} = sign \cdot GLKSD1 \cdot {E_{gd}}^2 \exp(T_{ox}(-GLKSD2 \cdot V_{gd} + GLKSD3)) W_{eff} \cdot NF$$
$$E_{gd} = \frac{V_{gs} - Vlds}{T_{ox}}$$

© 2023 Cadence Design Systems, Inc.

Gate-Induced Drain Leakage (GIDL)

HiSIM 2.5

$$I_{GIDL} = q \cdot GIDL1 \cdot \frac{E^2}{E_g^{\frac{1}{2}}} \cdot \exp\left(-GIDL2 \cdot \frac{E_g^{\frac{3}{2}}}{E}\right) \cdot W_{eff} \cdot NF$$

HiSIM 2.5.1

$$I_{GIDL} = q \cdot GIDL1 \cdot \frac{E^2}{E_g^{\frac{1}{2}}} \cdot \exp\left(-GIDL2 \cdot \frac{E_g^{\frac{3}{2}}}{E}\right) \cdot W_{eff} \cdot NF \cdot \frac{V_{db}^{\ 3}}{V_{db}^{\ 3} + small}$$

$$E = \frac{GIDL3 \cdot (V_{ds} + GIDL4) - V_G'}{T_{ox}}$$

$$V_G' = V_{gs} + \Delta V_{th} \cdot GIDL5$$

$$\Delta V_{th} = \Delta V_{th,SC} + \Delta V_{th,P}$$

$$V_{db} = V_{ds} - V_{bs}$$

$$small = 0.5$$

Conservation of Symmetry at Vds=0

HiSIM preserves the symmetry at Vds = 0 automatically due to the drift-diffusion approximation. However, modeling of the short-channel effects induces a small asymmetry. To eliminate the asymmetry caused by the artifacts of the modeling, the V_{th} modeling has to include a damping of the short-channel effects as V_{ds} approaches zero. This corresponds to a vanishing of shortchannel effects as V_{ds} gets near to zero, which is also observed in 2D simulations. In HiSIM, the damping is done by a mathematical function with two parameters: VZADD0 and PZADD0.

The values of these parameters are fixed, and it is recommended not to change them. Other modeled phenomena, which include a Vds dependence, cause a similar symmetry problem as the short-channel effects. They are therefore also damped.

© 2023 Cadence Design Systems, Inc.

Source/Bulk and Drain/Bulk Diode Model

Diode Current

The model equations for the source/bulk and drain/bulk diode currents are based on the concepts of BSIM3v3, but include a number of modifications.

These regions are distinguished in the modeling and are treated separately according to their origins.

$$T_{tnom} = \frac{T}{TNOM}$$

$$j_s = JS0 \cdot \exp\left\{\frac{E_g(T = TNOM) \cdot \beta(T = TNOM) - E_g\beta + XTI \cdot \log(T_{tnom})}{NJ}\right\}$$

$$j_{ssw} = JS0SW \cdot \exp\left\{\frac{E_g(T = TNOM) \cdot \beta(T = TNOM) - E_g\beta + XTI \cdot \log(T_{tnom})}{NJSW}\right\}$$

$$j_{s2} = JS0 \cdot \exp\left\{\frac{E_g(T = TNOM) \cdot \beta(T = TNOM) - E_g\beta + XTI2 \cdot \log(T_{tnom})}{NJ}\right\}$$

$$j_{ssw2} = JS0SW \cdot \exp\left\{\frac{E_g(T = TNOM) \cdot \beta(T = TNOM) - E_g\beta + XTI2 \cdot \log(T_{tnom})}{NJSW}\right\}$$

$$N_{vtm} = \frac{NJ}{\beta}$$

Between Drain and Bulk

With these current densities and the area parameter AD and the perimeter parameter PD of the drain region, the forward and backward currents between drain and bulk are calculated as

$$I_{sbd} = AD \cdot j_s + PD \cdot J_{ssw}$$

$$I_{sbd2} = AD \cdot j_{s2} + PD \cdot J_{ssw2}$$

© 2023 Cadence Design Systems, Inc.

a) Vbd ≥T1

$$I_{bd} = I_{sbd}\left\{\exp\left(\frac{T_1}{N_{vtm}}\right) - 1\right\} + \frac{I_{sbd}}{N_{vtm}}\exp\left(\frac{T_1}{N_{vtm}}\right)(V_{bd} - T1)$$

$$+I_{sbd2}\cdot CISB\left\{\exp\left(\frac{-V_{bd}CVBK}{N_{vtm}}\right) - 1\right\}\exp\{(T_{nom} - 1)CTEMP\}$$

$$+CISBK\left\{\exp\left(\frac{-V_{bd}CVBK}{N_{vtm}}\right) - 1\right\}$$

b) T1≥Vbd

$$I_{bd} = I_{sbd}\left\{\exp\left(\frac{V_{bd}}{N_{vtm}}\right) - 1\right\}$$

$$+I_{sbd2}\cdot CISB\left\{\exp\left(\frac{-V_{bd}CVB}{N_{vtm}}\right) - 1\right\}\exp\{(T_{nom} - 1)CTEMP\}$$

$$+CISBK\left\{\exp\left(\frac{-V_{bd}CVBK}{N_{vtm}}\right) - 1\right\}$$

$$T_1 = N_{vtm}\cdot\log\left\{\frac{VDIFFJ}{I_{sbd}}\cdot(T_{tnom})^2 + 1\right\}$$

$$I_{bd} = I_{bd} + DIVX\cdot I_{sbd2}\cdot V_{bd}$$

Between Source and Bulk

The area parameter AS and the perimeter parameter PS of the source region are used to calculate the forward and backward currents between source and bulk.

$$I_{sbs} = AS\cdot j_s + PS + j_{ssw}$$

$$I_{sbs2} = AS\cdot j_{s2} + PS\cdot J_{ssw2}$$

© 2023 Cadence Design Systems, Inc.

a) Vbs ≥T2

$$I_{bs} = I_{sbs}\left\{\exp\left(\frac{T_2}{N_{vtm}}\right)-1\right\}+\frac{I_{sbs}}{N_{vtm}}\exp\left(\frac{T_2}{N_{vtm}}\right)(V_{bs}-T2)$$

$$+I_{sbs2}\cdot CISB\left\{\exp\left(\frac{-V_{bs}CVBK}{N_{vtm}}\right)-1\right\}\exp\{(T_{nom}-1)CTEMP\}$$

$$+CISBK\left\{\exp\left(\frac{-V_{bs}CVBK}{N_{vtm}}\right)-1\right\}$$

b) T2≥Vbs

$$I_{bs} = I_{sbs}\left\{\exp\left(\frac{V_{bs}}{N_{vtm}}\right)-1\right\}$$

$$+I_{sbs2}\cdot CISB\left\{\exp\left(\frac{-V_{bs}CVB}{N_{vtm}}\right)-1\right\}\exp\{(T_{nom}-1)CTEMP\}$$

$$+CISBK\left\{\exp\left(\frac{-V_{bs}CVBK}{N_{vtm}}\right)-1\right\}$$

$$T_2 = N_{vtm}\cdot\log\left\{\frac{VDIFFJ}{I_{sbs}}\cdot(T_{tnom})^2+1\right\}$$

$$I_{bs} = I_{bs}+DIVX\cdot I_{sbs2}\cdot V_{bs}$$

Diode Capacitance

The notations

Θ= S; θ= s (for source/bulk junction) and

Θ = D;θ = d (for drain/bulk junction) apply.

$$c_{zb\theta} = CJ\cdot A\Theta$$

© 2023 Cadence Design Systems, Inc.

$P_\Theta > W_{eff}$

$$c_{zb\theta sw} = CJSW(P\Theta - W_{eff} \cdot NF)$$
$$C_{zb\theta swg} = CJSWG \cdot W_{eff} \cdot NF$$

(i) $V_{b\theta} = 0$

$$Q_{b\theta} = 0$$

$$C_{apb\theta} = c_{zb\theta} + c_{zb\theta sw} + c_{zb\theta swg}$$

(ii) $V_{b\theta} < 0$

1-1 $C_{zb\theta} > 0$

$$\arg = 1 - \frac{V_{b\theta}}{PB}$$

α) MJ = 0.5

$$s\arg = \frac{1}{\sqrt{\arg}}$$

β) MJ ≠ 0.5

$$s\arg = \exp(-MJ \cdot \log(\arg))$$

$$Q_{b\theta} = \frac{PB \cdot C_{zb\theta}(1 - \arg \cdot s\arg)}{1 - MJ}$$

$$C_{apb\theta} = c_{zb\theta} \cdot s\arg$$

1-2 $c_{zb\theta} \leq 0$

$$Q_{b\theta} = 0$$

© 2023 Cadence Design Systems, Inc.

$$C_{apb\theta} = 0$$

2) $c_{zb\theta sw} > 0$

$$\arg = 1 - \frac{V_{b\theta}}{PBSW}$$

α) MJSW = 0.5

$$\mathrm{sarg} = \frac{1}{\sqrt{\arg}}$$

β) MJSW ≠ 0.5

$$s\arg = \exp(-MJSW \cdot \log(\arg))$$

$$Q_{b\theta}+ = \frac{PBSW \cdot c_{zb\theta sw}(1 - \arg \cdot s\arg)}{1 - MJSW}$$

$$C_{apb\theta} = C_{zb\theta sw} \cdot s\arg$$

3) $c_{zb\theta swg} > 0$

$$\arg = 1 - \frac{V_{b\theta}}{PBSWG}$$

α) MJSWG = 0.5

$$\mathrm{sarg} = \frac{1}{\sqrt{\arg}}$$

β) MJSWG ≠ 0.5

$$s\arg = \exp(-MJSWG \cdot \log(\arg))$$

© 2023 Cadence Design Systems, Inc.

$$Q_{b\theta^+} = \frac{PBSWG \cdot c_{zb\theta swg}(1 - \arg \cdot s\arg)}{1 - MJSWG}$$

$$C_{apb\theta} = c_{zb\theta swg} \cdot s\arg$$

© 2023 Cadence Design Systems, Inc.

$P\Theta \leq W_{eff}$

$$c_{zb\theta swg} = CJSWG \cdot P\Theta$$

(i) $V_{b\theta} = 0$

$$Q_{b\theta} = 0$$

$$C_{apb\theta} = c_{zb\theta} + c_{zb\theta swg}$$

(ii) $V_{b\theta} < 0$

1-1 $C_{zb\theta} > 0$

$$\arg = 1 - \frac{V_{b\theta}}{PB}$$

α) MJ = 0.5

$$\mathrm{sarg} = \frac{1}{\sqrt{\arg}}$$

β) MJ $\neq$ 0.5

$$s\arg = \exp(-MJ \cdot \log(\arg))$$

$$Q_{b\theta} = \frac{PB \cdot c_{zb\theta}(1 - \arg \cdot s\arg)}{1 - MJ}$$

$$C_{apb\theta} = c_{zb\theta} \cdot s\arg$$

1-2 $C_{zb\theta} \leq 0$

$$Q_{b\theta} = 0$$

© 2023 Cadence Design Systems, Inc.

$$C_{apb\theta} = 0$$

$$c_{zb\theta swg} > 0$$

$$\arg = 1 - \frac{V_{b\theta}}{PBSWG}$$

α) MJSWG = 0.5

$$\mathrm{sarg} = \frac{1}{\sqrt{\arg}}$$

β) MJSWG $\neq$ 0.5

$$s\arg = \exp(-MJSWG \cdot \log(\arg))$$

$$Q_{b\theta}+ = \frac{PBSWG \cdot c_{zb\theta swg}(1 - \arg \cdot s\arg)}{1 - MJSWG}$$

$$C_{apb\theta}+ = c_{zb\theta swg} \cdot s\arg$$

(iii) $V_{b\theta} > 0$

$$Q_{b\theta} = V_{b\theta}(c_{zb\theta} + c_{zb\theta swg}) + V^2_{b\theta}\left(\frac{1}{2}\frac{c_{zb\theta} \cdot MJ}{PB} + \frac{1}{2}\frac{c_{zb\theta swg} \cdot MJSWG}{PBSWG}\right)$$

$$Q_{apb\theta} = c_{zb\theta} + c_{zb\theta swg} + V_{b\theta}\left(\frac{c_{zb\theta} \cdot MJ}{PB} + \frac{c_{zb\theta swg} \cdot MJSWG}{PBSWG}\right)$$

© 2023 Cadence Design Systems, Inc.

Noise Models

1/f Noise Model

$$fn = \frac{{I_{ds}}^2 NFTRP}{\beta f^{FALPH}(L_{eff} - \Delta L) W_{eff} \cdot NF}$$

$$\cdot \left[\frac{1}{(N_0 + N^*)(N_L + N^*)} + \frac{2\mu E_y NFALP}{N_L - N_0} 1n\left(\frac{N_L + N^*}{N_0 + N^*}\right) + (\mu E_y NFALP)^2 \right]$$

$$N^* = \frac{C_{ox} - C_{dep} + CIT}{q\beta}$$

$$N_{flick} = fn \cdot f^{FALPH}$$

Thermal Noise Model

$$id = 4kT \frac{W_{eff} \cdot NF \cdot C_{ox} V_g V_t \mu}{(L_{eff} - \Delta L)} \cdot \frac{(1 + 3\eta + 6\eta^2)\mu d^2 + (3 + 4\eta + 3\eta^2)\mu_d \mu_s + (6 + 3\eta + \eta^2)\mu_s}{15(1 + \eta){\mu_{av}}^2}$$

where μs, μd and μav are mobility at the source side, the drain side, and averaged, respectively.

$$\eta = 1 - \frac{(\varphi_{SL} - \varphi_0) + \chi(\varphi_{SL} - \varphi_0)}{V_g V_t}$$

$$\chi = 2\frac{cnst0}{C_{ox}} \left[\left[\frac{2}{3}\frac{1}{\beta} \frac{\{\beta(\varphi_{SL} - V_{bs}) - 1\}^{\frac{3}{2}} - \{\beta(\varphi_{S0} - V_{bs}) - 1\}^{\frac{3}{2}}}{\varphi_{SL} - V_{bs}} \right] - \sqrt{\beta(\varphi_{S0} - V_{bs}) - 1} \right]$$

$$N_{thrml} = id/(4kT)$$

© 2023 Cadence Design Systems, Inc.

Shot Noise

HiSIM 2.5

$$shot = 2q \cdot I_{ds}$$

HiSIM 2.5.1

shot noise due to Igs

$$i_{gs} = 2q \cdot I_{gs}$$

shot noise due to Igd

$$i_{gd} = 2q \cdot I_{gd}$$

shot noise due to Igb

$$i_{gb} = 2q \cdot I_{gb}$$

Induced Gate Noise Model

$$N_{igate} = S_{igate}/f^2$$

Non-Quasi-Static (NQS) Model

Carrier Formation

$$q(t_i) = \frac{q(t_{i-1}) + \frac{\Delta t}{\tau} Q(t_i)}{1 + \frac{\Delta t}{\tau}}$$

© 2023 Cadence Design Systems, Inc.

Delay Mechanism

$$\tau_{diff} = DLY1$$

$$\tau_{cond} = DLY2 \cdot \frac{Q_i}{I_{ds}}$$

$$\frac{1}{\tau} = \frac{1}{\tau_{diff}} + \frac{1}{\tau_{cond}}$$

$$\tau_B = DLY3 \cdot C_{ox}$$

Time-Domain Analysis

The total drain/source/bulk terminal currents are derived from the superposition of the transport current and the charging current. The transport current is a function of the instantaneous terminal voltages and is approximated by the steady-state solution. The source/drain/bulk charging currents are the time derivatives of the associated non-quasi-static charges, q_S, q_D, and q_B, respectively.

AC Analysis

$$\left(i\omega\frac{\partial q_I}{\partial v} + \frac{1}{\tau}\left(\frac{\partial q_I}{\partial v} - \frac{\partial Q_I}{\partial v}\right)\right)\Bigg|_{v = v0} \cdot V_e^{ist} = 0$$

$$\left(i\omega\frac{\partial q_B}{\partial v} + \frac{1}{\tau}\left(\frac{\partial q_B}{\partial v} - \frac{\partial Q_B}{\partial v}\right)\right)\Bigg|_{v = v0} \cdot V_e^{ist} = 0$$

where

$$\frac{\partial q_I}{\partial v} = \frac{1}{1 + i\omega\tau}\frac{\partial Q_I}{\partial v}$$

$$\frac{\partial q_B}{\partial v} = \frac{1}{1 + i\omega\tau_B}\frac{\partial Q_B}{\partial v}$$

© 2023 Cadence Design Systems, Inc.

DFM Model

To support design for manufacturability (DFM) HiSIM2 introduces an option for considering the variation of device parameters.

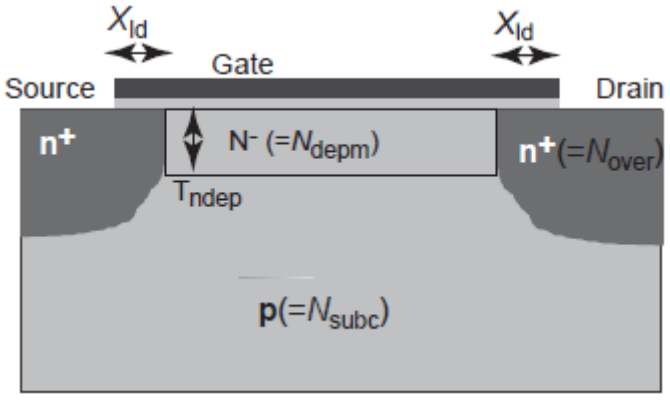
Accurate prediction of device performance for a wide range of the substrate-impurity-concentration variations is secured by introducing an impurity concentration dependent mobility due to the phonon scattering as

$$M_{uephonon} = MUEPH1[MPHDFM\{1n(NSUBCDFM) - 1n(NSUBC)\} + 1]$$
$$NSUBP = NSUBP + (NSUBCDFM - NSUBC)$$
$$NPEXT = NPEXT + (NSUBCDFM - NSUBC)$$

where NSUBCDFM is an instance parameter and MPHDFM is a model parameter describing the mobility reduction as the substrate impurity concentration is increased. This model parameter MPHDFM is required, if the model flag CODFM is switched to one. The default value is sufficient for the most applications. The DFM model is activated, if the instance parameter NSUBCDFM is also given.

Depletion Mode Model Option

In the depletion model MOSFET, an N- layer is constructed at the channel surface of the conventional MOSFET devices, as shown below.



This model is activated when the parameter `CODEP` is set to `1`.

© 2023 Cadence Design Systems, Inc.

Binning Model

Binning option is introduced in HiSIM2.4 to secure enough accuracy of model calculation results, even though the effects observed are not modeled yet. The binning method is the same as that used in BSIM3/4

$$Bin_HiSIM_model_parameter = HiSSIM_model_parameter + \frac{P1}{L_{bin}} + \frac{P2}{W_{bin}} + \frac{P3}{L_{bin}W_{bin}}$$

where P1, P2, and P3 are model parameters for L HiSIM model parameter, W HiSIM model parameter, and L* HiSIM model parameter, respectively and

$$L_{bin} = (L_{gate} \cdot 10^6)^{LBINN}$$

$$W_{bin} = (W_{gate} \cdot 10^6)^{WBINN}$$

© 2023 Cadence Design Systems, Inc.

Component Statements

This device is supported within altergroups.

Sample Instance Statement

```
m4 (0 2 1 1) nch w=2u l=0.8u as=250p ad=250p pd=168p ps=168p m=2
```

Sample Model Statement

```
model nch hisim2 type=n version=2.50 corsrd=0 conqs=0 cgso=7.43e-10 cgdo=7.43e-10
cgbo=2.56e-11
```

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

w (m)	Gate width.
l (m)	Gate length.
as (m^2)	Area of source junction.
ad (m^2)	Area of drain junction.
ps (m)	Perimeter of source junction.
pd (m)	Perimeter of drain junction.
temp (C)	Device temperature.
dtemp (C)	Device temperature rise from ambient.
nrs=0	Number of squares of source diffusion. Default value is 1.0 for the 2.50 and 2.51 versions.
nrd=0	Number of squares of drain diffusion. Default value is 1.0 for the 2.50 and 2.51 versions.
corbnet	Substrate resistance network selector.
rbpb (Ω)	Substrate resistance network.
rbpd (Ω)	Substrate resistance network.
rbps (Ω)	Substrate resistance network.

© 2023 Cadence Design Systems, Inc.

`rbdb (Ω)`	Substrate resistance network.
`rbsb (Ω)`	Substrate resistance network.
`corg`	Gate-contact resistance selector.
`ngcon=1.0`	Number of gate contacts.
`xgw=0.0 m`	Distance from gate contact to channel edge.
`xgl=0.0 m`	Offset of gate length due to variation in patterning.
`nf=1.0`	Number of gate fingers.
`lod=1.0E-5 m`	Length of diffusion between gate and STI.
`m=1`	Multiplicity factor (number of MOSFETs in parallel).
`sa=0.0 m`	Distance from STI edge to Gate edge, existed from 2.40.
`sb=0.0 m`	Distance from STI edge to Gate edge, existed from 2.40.
`sd=0.0 m`	Distance from Gate edge to Gate edge, existed from 2.40.
`nsubcdfm (cm`$^{-3}$`)`	Constant part of Nsub for DFM, existed from 2.40.
`mphdfm`	NSUBCDFM dependence of phonon scattering for DFM.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.
`sca=0.0`	WPE sca.
`scb=0.0`	WPE scb.
`scc=0.0`	WPE scc.
`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`trise=0 C`	Default device temperature rise from ambient.

Model Definition

```
model modelName hisim2 parameter=value ...
```

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` and `p`.

© 2023 Cadence Design Systems, Inc.

`version=2.50`	Model parameter "version" accepts only real number values, like 2.50 for version=2.5.0. The available versions are 2.50(2.5.0), 2.51(2.5.1), 2.60(2.6.0), 2.61(2.6.1), 2.70(2.7.0), 2.80(2.8.0), 2.90(2.9.0), 2.91(2.9.1), 3.0(3.0.0), 3.10(3.1.0), 3.11(3.1.1) and 3.20(3.2.0). The parameter cannot be parameterized, its value must be constant.
`corsrd=0`	Contact resistances Rs and Rd selector. Possible values are: `0` : no (default). `1` : yes, as internal resistances. `-1` : yes, as external resistances.
`coiprv=1`	Previous Ids is used for calculating source/drain resistance effect. Possible values are `0` : no and `1` : yes.
`copprv=1`	Previous surface potential is used for the initial guess. Possible values are `0` : no and `1` : yes.
`coadov=1`	Selector for lateral field induced and overlap charges/capacitances being added to intrinsic ones. Possible values are `0` : no and `1` : yes(default).
`coisub=0`	Substrate current selector. Possible values are `0` : no(default) and `1` : yes.
`cogidl=0`	GIDL current calculation selector. Possible values are `0` : no(default) and `1` : yes.
`coiigs=0`	Gate current calculation selector. Possible values are `0` : no(default) and `1` : yes.
`coovlp=1`	Overlap capacitance calculation selector. Possible values are `0` : constant overlap capacitance(default) and `1` : yes.
`coflick=0`	1/f noise calculation selector.
`coisti=0`	STI leakage current calculation selector. Possible values are `0` : no(default) and `1` : yes.
`conqs=0`	Non-quasi-static mode selector. Possible values are `0` : no(default) and `1` : yes.
`cothrml=0`	Thermal noise calculation selector. Possible values are `0` : no(default) and `1` : yes.
`tnom (C)`	Parameters measurement temperature. Default set by `options`.

© 2023 Cadence Design Systems, Inc.

corg=0	Gate-contact resistance calculation selector. Possible values are 0 : no(default) and 1 : yes.
corbnet=0	Substrate resistance network selector.
coign=0	Induced gate and cross correlation noise calculation selector.
compatible	Compatibility with spice3. Default value is spectre. Possible values are spectre, spice2, spice3, cdsspice, spiceplus, eldo, and sspice.
alarm=none	Forbidden operating region. Possible values are none, off, triode, sat, subth, and rev.
codfm=0	Calculation of model for DFM selector, existed from 2.40.
corecip=1	Capacitance reciprocity takes first priority.
coqy=0	Calculate lateral field-induced charge/capacitance.

Safe Operating Areas Parameters

vds_max=∞ V	Maximum allowed voltage cross source and drain.
vgd_max=∞ V	Maximum allowed voltage cross drain and gate.
vgs_max=∞ V	Maximum allowed voltage cross source/bulk and gate.
vbd_max=∞ V	Maximum allowed voltage cross drain/source and bulk.
vbs_max=∞ V	Maximum allowed voltage cross source and bulk.
vgb_max=∞ V	Maximum allowed voltage cross gate and bulk.
vgdr_max=vgd_max V	Maximum allowed reverse voltage across gate and drain.
vgsr_max=vgs_max V	Maximum allowed reverse voltage across gate and source.
vgsr_max=vgb_max V	Maximum allowed reverse voltage across gate and bulk.
vgsr_max=vbs_max V	Maximum allowed reverse voltage across bulk and source.
vgsr_max=vbd_max V	Maximum allowed reverse voltage across bulk and drain.

Default for instance parameters

w=5e-6 m	Default gate width.

© 2023 Cadence Design Systems, Inc.

`l=5e-6 m`	Default gate length.
`as=0` m^2	Default area of source junction.
`ad=0` m^2	Default area of drain junction.
`ps=0 m`	Default perimeter of source junction.
`pd=0 m`	Default perimeter of drain junction.
`temp=27 C`	Default device temperature.
`dtemp=0 C`	Default device temperature rise from ambient.

Basic Device Parameters

`tox=3.0e-9 m`	Physical oxide thickness.
`xld=0 m`	Gate-overlap length.
`xwd=0 m`	Gate-overlap width.
`tpoly=2.0E-7 m`	Height of the gate poly-si for fringing capacitance.
`nsubc=5.0e+17` cm^{-3}	Substrate-impurity concentration.
`nsubp=1.0e+18` cm^{-3}	Maximum pocket concentration.
`rs=0.0` Ω `m`	Source contact resistance in LDD region.
`rd=0.0` Ω `m`	Drain contact resistance in LDD region.
`vfbc=-1.0 V`	Constant part of flat-band voltage.
`lp=1.5e-8 m`	Length of the pocket penetration into the channel.
`xqy=10e-9 m`	Distance from channel/drain junction to maximum electric field point.
`lover=5.0E-8 m`	Overlap length.
`ll=0.0`	Gate length parameter.
`lld=0.0 m`	Gate length parameter.
`lln=0.0`	Gate length parameter.
`wl=0.0`	Gate width parameter.
`wld=0.0 m`	Gate width parameter.
`wln=0.0`	Gate width parameter.

© 2023 Cadence Design Systems, Inc.

`vbi=1.0 V`	Built-in potential.
`nsubpw=0.0 cm^-3`	Pocket implant parameter.
`nsubpwp=1.0`	Pocket implant parameter.
`lpext=1.0E-50 m`	Pocket extension.
`npext=5.0E17 cm^-3`	Pocket extension.
`rsh=0.0 V/A m`	Source/drain diffusion sheet resistance.
`rshg=0.0 V/A m`	Gate-electrode sheet resistance.
`rbpb=50.0 Ω`	Substrate resistance network.
`rbpd=50.0 Ω`	Substrate resistance network.
`rbps=50.0 Ω`	Substrate resistance network.
`rbdb=50.0 Ω`	Substrate resistance network.
`rbsb=50.0 Ω`	Substrate resistance network.
`gbmin=1.0E-12`	Minimum conductance for substrate resistance network.
`xl=0 m`	Gate length offset due to mask/etch effect, existed from 2.40.
`xw=0 m`	Gate width offset due to mask/etch effect, existed from 2.40.
`xqy1=0.0 F m^{XQY2}`	Vbs dependence of Qy, existed from 2.40.
`xqy2=2.0`	Lgate dependence of Qy, existed from 2.40.
`nsubpl=0.001 µm`	Gate-length dependence of NSUBP.
`nsubpfac=1.0`	Gate-length dependence of NSUBP.

Temperature dependence effects

`eg0=1.1785 eV`	Constant bandgap.
`bgtmp1=9.025e-5 eV/K`	First order temperature coefficient for band gap.
`bgtmp2=1.0e-7 eV/K^2`	Second order temperature coefficient for band gap.
`copb20compat=1`	Pb20(compat) or Pb2.
`ctempd=0.0`	Temperature coefficient for drain junction.
`ctemps=0.0`	Temperature coefficient for source junction.

© 2023 Cadence Design Systems, Inc.

Quantum Mechanical Effects

`qme1=0.0 m/V`^{2}	Coefficient for quantum mechanical effect.
`qme2=0.0 V`	Coefficient for quantum mechanical effect.
`qme3=0.0 m`	Coefficient for quantum mechanical effect.
`kappa=3.9`	Dielectric constant for high-k stacked gate.

Poly Depletion Effects

`pgd1=1.0E-4 V`	Strength of poly depletion.
`pgd2=0.3 V`	Threshold voltage of poly depletion.
`pgd4=0.0`	Parameter for gate-poly depletion.

Short Channel Effects

`parl2=1.0e-8 m`	Depletion width of channel/contact junction.
`sc1=1.0 1/V`	Short-channel coefficient 1.
`sc2=0.0 1/V`^{2}	Short-channel coefficient 2.
`sc2d=0.0`	Vds-dependent SCE associated with NSUBD (vertDop).
`sc3=0.0 m/V`^{2}	Short-channel coefficient 3.
`scp1=1.0 1/V`	Short-channel coefficient 1 for pocket.
`scp2=0.0 1/V`^{2}	Short-channel coefficient 2 for pocket.
`scp3=0.0 m/V`^{2}	Short-channel coefficient 3 for pocket.
`scp22=0.0 V`^{4}	Short-channel-effect modification for small Vds.
`scp21=0.0 V`	Short-channel-effect modification for small Vds.
`bs1=0.0 V`^{2}	Body-coefficient modification by impurity profile.
`bs2=0.9 V`	Body-coefficient modification by impurity profile.
`sc4=0.0`	Short-channel coefficient 4.
`copspt=0`	Flag Ps0 method for deep punchthrough.

© 2023 Cadence Design Systems, Inc.

`copt=0`	Flag punchthrough.

Narrow channel effects

`wfc=0.0 m F/cm`^{2}	Threshold voltage reduction.
`nsti=1.0e17 cm`$^{-3}$	Substrate-impurity concentration at the SIT edge.
`wsti=0.0 m`	Width of the high-field region at STI.
`muephw=0.0`	Phonon scattering parameter.
`muepwp=1.0`	Phonon scattering parameter.
`wvth0=0.0`	Threshold voltage shift.
`mueswp=1.0`	Change of surface roughness related mobility.
`vthsti=0.0`	Parameter for STI.
`muesti1=0.0`	STI Stress mobility parameter.
`muesti2=0.0`	STI Stress mobility parameter.
`muesti3=1.0`	STI Stress mobility parameter.
`nsubpsti1=0.0 m`	STI Stress pocket implant parameter.
`nsubpsti2=0.0 m`	STI Stress pocket implant parameter.
`nsubpsti3=1.0 m`	STI Stress pocket implant parameter.
`wstil=0.0`	Parameter for STI.
`wstilp=1.0`	Parameter for STI.
`scsti1=0.0`	Parameter for STI.
`scsti2=0.0 1/V`	Parameter for STI.
`saref=1e-6 m`	Reference distance from STI edge to Gate edge, existed from 2.40.
`sbref=1e-6 m`	Reference distance from STI edge to Gate edge, existed from 2.40.
`wstiw=0.0`	Parameter for STI, existed from 2.40.
`wstiwp=1.0`	Parameter for STI, existed from 2.40.
`vdsti=0.0`	parameter for STI, existed from 2.40.

© 2023 Cadence Design Systems, Inc.

`nsubcw=0.0`	Parameter for narrow channel effect.
`nsubcwp=1.0`	Parameter for narrow channel effect.
`nsubcmax=5e18`	Parameter for narrow channel effect.

Mobility Effects

`vds0=0.05 V`	Drain voltage for extracting the low-field mobility.
`muecb0=1000.0 cm^2/(V s)`	Coulomb scattering.
`muecb1=100.0 cm^2/(V s)`	Coulomb scattering.
`mueph0=0.3 cm^2 (V/cm)^(muesr1)/(V s)`	Phonon scattering.
`mueph1=2.5e4`	Phonon scattering.
`muetmp=1.5`	Temperature dependence of phonon scattering.
`muesr0=2.0 cm^2 (V/cm)^(muesr1)/(V s)`	Surface-roughness scattering.
`muesr1=1.0e15`	Surface-roughness scattering.
`ndep=1.0`	Coefficient of effective electric field.
`ninv=0.5`	Coefficient of effective electric field.
`bb=2.0`	High-field mobility degradation.
`vmax=1.0e7 cm/s`	Maximum of electron saturation velocity.
`vover=0.3 cm^(voverp)`	Parameter for velocity overshoot.
`voverp=0.3`	Lgate dependence of velocity overshoot.
`vovers=0.0`	Parameter for overshoot.
`voversp=0.0`	Parameter for overshoot.
`vtmp=0.0 cm/s`	Temperature dependence of the saturation velocity.
`muephl=0.0`	Phonon scattering parameter.
`mueplp=1.0`	Phonon scattering parameter.
`muesrl=0.0`	Surface roughness parameter.
`muesrw=0.0`	Change of surface roughness related mobility.

© 2023 Cadence Design Systems, Inc.

`mueslp=1.0`	Surface roughness parameter.
`ndepl=0.0`	Modification of Qb contribution for short-channel case, existed from 2.40.
`ndeplp=1.0`	Modification of Qb contribution for short-channel case, existed from 2.40.
`ninvd=0.0 1/V`	Modification of Vdse dependence on Eeff.
`muephl2=0.0`	Length dependence of phonon mobility reduction.
`mueplp2=1.0`	Length dependence of phonon mobility reduction.

Small size parameters

`wl1=0.0`	Threshold voltage shift of STI leakage due to small size effect.
`wl1p=1.0`	Threshold voltage shift of STI leakage due to small size effect.
`wl2=0.0`	Threshold voltage shift due to small size effect.
`wl2p=1.0`	Threshold voltage shift due to small size effect.
`muephs=0.0`	Mobility modification due to small size.
`muepsp=1.0`	Mobility modification due to small size.
`muepwd=0.0`	Phonon scattering parameter.
`muepld=0.0`	Phonon scattering parameter.

Channel Length Modulation Effects

`clm1=0.7`	First parameter for CLM.
`clm2=2.0 1/m`	Second parameter for CLM.
`clm3=1.0`	Third parameter for CLM.
`clm5=1.0`	Effect of pocket implantation.
`clm6=0.0`	Effect of pocket implantation.

© 2023 Cadence Design Systems, Inc.

Substrate Current Effects (URC)

`sub1=10.0 1/V`	First parameter for Isub.
`sub2=25.0 V`	Second parameter for Isub.
`svgs=0.8`	Substrate current dependence on Vgs.
`svbs=0.5`	Substrate current dependence on Vbs.
`svbsl=0.0`	Lgate dependence of SVBS.
`svds=0.8`	Substrate current dependence on Vds.
`slg=3.0E-8`	Substrate current dependence on Lgate.
`sub1l=2.5E-3`	Lgate dependence of SUB1.
`sub2l=2.0E-6`	Lgate dependence of SUB2.
`svgsl=0.0`	Lgate dependence of SVGS.
`svgslp=1.0`	Lgate dependence of SVGS.
`svgswp=1.0`	Wgate dependence of SVGS.
`svgsw=0.0`	Wgate dependence of SVGS.
`svbslp=1.0`	Lgate dependence of SVBS.
`slgl=0.0`	Substrate current dependence on Lgate.
`slglp=1.0`	Substrate current dependence on Lgate.
`sub1lp=1.0`	Lgate dependence of SUB1.
`ibpc1=0.0`	Impact-ionization induced bulk potential change.
`ibpc2=0.0`	Impact-ionization induced bulk potential change.
`subtmp=0.0`	Temperature dependence of Isub.

Gate Current Effects

`glpart1=0.5`	Partitioning of gate current.
`gleak1=50.0 A/(V^(3/2) c^(1/2))`	First gate current coefficient.
`gleak2=1.0E7 1/(V^(1/2) c^(3/2) m)`	

© 2023 Cadence Design Systems, Inc.

	Second gate current coefficient.
`gleak3=6.0E-2`	Third gate current coefficient.
`gleak4=4.0`	Parameter for gate current.
`gleak5=7.5E3`	Parameter for gate current.
`glksd1=1.0E-15`	Parameter for gate current.
`glksd2=5e-6`	Parameter for gate current.
`glksd3=-5e-6`	Parameter for gate current.
`glkb1=5.0E-16`	Parameter for gate current.
`glkb2=1.0`	Parameter for gate current.
`igtemp2=0.0`	Parameter for gate current.
`igtemp3=0.0`	Parameter for gate current.
`gleak6=0.25 V`	Parameter for gate current.
`gleak7=1.0E-6` m^2	Parameter for gate current.
`glkb3=0e0 V`	Parameter for gate current, existed from 2.40.
`egig=1.1 V`	Parameter for gate current, existed from 2.40.

GIDL Current Effects (URC)

`gidl1=2.0 A m/(V^(3/2) c^(1/2))`	
	First parameter for GIDL.
`gidl2=3.0E7 1/(V^(1/2) c^(3/2) m)`	
	Second parameter for GIDL.
`gidl3=0.9`	Third parameter for GIDL.
`gidl4=0.9`	Parameter for GIDL.
`gidl5=0.2`	Parameter for GIDL.

Noise 1/f Effects

`nfalp=1.0e-19`	Flicker (1/f) noise contribution of the mobility fluctuation.

© 2023 Cadence Design Systems, Inc.

`nfalp1=1.0E-19`	Contribution of the mobility fluctuation.
`nfalp2=1.0E-19`	Contribution of the mobility fluctuation.
`sidp=2.0`	Parameter for 1/f noise.
`dlnoise=0.0`	Parameter for 1/f noise.
`nftrp=1.0e10`	Flicker (1/f) noise ratio of trap density to attenuation coefficient.
`cit=0.0`	Flicker (1/f) noise interface trapped carriers capacitance.
`falph=1.0`	Parameter for 1/f noise.

NQS parameters

`dly1=1.0E-10`	Parameter for transit time.
`dly2=0.7`	Parameter for transit time.
`dly3=8.0E-7 Ω`	Parameter for transforming bulk charge.

Symmetry for Short-Channel MOSFET

`vzadd0=20.0e-3 V`	Symmetry conservation coefficient Vzadd at Vds=0.
`pzadd0=20.0e-3 V`	Symmetry conservation coefficient Pzadd at Vds=0.

P-N junctions parameters

`js0=5.0e-7 A/m`^{2}	Junction saturation current density.
`js0sw=0.0 A/m`	Side-wall saturation current density.
`nj=1.0`	Junction emission coefficient.
`njsw=1.0`	Junction emission coefficient (sidewall).
`xti=2.0`	Junction saturation current temperature exponent coefficient.
`cj=5.0e-4 F/m`^{2}	Bottom junction capacitance per unit area at zero bias.

© 2023 Cadence Design Systems, Inc.

`cjsw=5e-10 F/m`	Source/drain sidewall junction capacitance per unit length at zero bias.
`cjswg=5e-10 F/m`	Source/drain sidewall junction capacitance grading coefficient per unit length at zero bias.
`mj=0.5`	Bulk junction bottom grading coefficient.
`mjsw=0.33`	Source/drain sidewall junction capacitance grading coefficient.
`mjswg=0.33`	Bottom junction capacitance grading coefficient.
`pb=1.0 V`	Bottom junction build-in potential.
`pbsw=1.0 V`	Source/drain sidewall junction build-in potential.
`pbswg=1.0 V`	Source/drain gate sidewall junction build-in potential.
`vdiffj=6.0E-4 V`	Threshold voltage for S/D junction diode.
`xti2=0.0`	Temperature coefficient.
`cisb=0.0`	Reverse bias saturation current.
`cvb=0.0`	Bias dependence coefficient of cisb.
`ctemp=0.0`	Temperature coefficient.
`cisbk=0.0 A`	Reverse bias saturation current.
`cvbk=0.0`	Bias dependence coefficient of cisb.
`divx=0.0 1/V`	Parameter for junction.
`tcjbs=0.0`	Temperature dependence of czbs.
`tcjbd=0.0`	Temperature dependence of czbd.
`tcjbssw=0.0`	Temperature dependence of czbssw.
`tcjbdsw=0.0`	Temperature dependence of czbdsw.
`tcjbsswg=0.0`	Temperature dependence of czbsswg.
`tcjbdswg=0.0`	Temperature dependence of czbdswg.
`cisbd=0.0`	Reverse bias saturation current for drain junction.
`cisbkd=0.0`	Reverse bias saturation current for drain junction.
`cisbks=0.0`	Reverse bias saturation current for source junction.
`cisbs=0.0`	Reverse bias saturation current for source junction.

© 2023 Cadence Design Systems, Inc.

`cjd=5.0e-4`	Bottom junction capacitance per unit area at zero bias for drain junction.
`cjs=5.0e-4`	Bottom junction capacitance per unit area at zero bias for source junction.
`cjswd=5.0e-10`	Sidewall junction capacitance grading coefficient per unit length at zero bias for drain junction.
`cjswgd=5.0e-10`	Gate sidewall junction capacitance per unit length at zero bias for drain junction.
`cjswgs=5.0e-10`	Gate sidewall junction capacitance per unit length at zero bias for source junction.
`cjsws=5.0e-10`	Sidewall junction capacitance grading coefficient per unit length at zero bias for source junction.
`codio=0`	Selector for updated diode model
`cvbd=0.0`	Bias dependence coefficient of cisb for drain junction.
`cvbs=0.0`	Bias dependence coefficient of cisb for source junction.
`divxd=0.0`	Reverse coefficient for drain junction.
`divxs=0.0`	Reverse coefficient for source junction.
`js0d=0.5e-6`	Saturation current density for drain junction.
`js0s=0.5e-6`	Saturation current density for source junction.
`js0swd=0.0`	Side wall saturation current density for drain junction.
`js0swg=0.0`	Gate sidewall saturation current density.
`js0swgd=0.0`	Gate side wall saturation current density for drain junction.
`js0swgs=0.0`	Gate side wall saturation current density for source junction.
`js0sws=0.0`	Side wall saturation current density for source junction.
`mjd=0.5`	Bottom junction capacitance grading coefficient for drain junction.
`mjs=0.5`	Bottom junction capacitance grading coefficient for source junction.
`mjswd=0.33`	Sidewall junction capacitance grading coefficient for drain junction.
`mjswgd=0.33`	Gate sidewall junction capacitance grading coefficient for drain junction.

© 2023 Cadence Design Systems, Inc.

`mjswgs=0.33`	Gate sidewall junction capacitance grading coefficient for source junction.
`mjsws=0.33`	Sidewall junction capacitance grading coefficient for source junction.
`njs=1.0`	Emission coefficient for source junction.
`njswd=1.0`	Sidewall emission coefficient for drain junction.
`njswg=1.0`	Gate sidewall emission coefficient.
`njswgd=1.0`	Gate sidewall emission coefficient for drain junction.
`njswgs=1.0`	Gate sidewall emission coefficient for source junction.
`njsws=1.0`	Sidewall emission coefficient for source junction.
`pbd=1.0`	Bottom junction build-in potential for drain junction.
`pbs=1.0`	Bottom junction build-in potential for source junction.
`pbswd=1.0`	Sidewall junction build-in potential for drain junction.
`pbswgd=1.0`	Gate sidewall junction build-in potential for drain.
`pbswgs=1.0`	Gate sidewall junction build-in potential for source junction.
`pbsws=1.0`	Sidewall junction build-in potential for source junction.
`vdiffjd=0.6e-3`	Threshold voltage for junction diode for drain junction.
`vdiffjs=0.6e-3`	Threshold voltage for junction diode for source junction.
`xti2d=0.0`	Temperature coefficient for drain junction.
`xti2s=0.0`	Temperature coefficient for source junction.
`xtid=2.0`	Junction current temperature exponent coefficient for drain junction.
`xtis=2.0`	Junction current temperature exponent coefficient for source junction.

Overlap capacitance parameters

`cgso=0.0 F/m`	Gate-source overlap capacitance.
`cgdo=0.0 F/m`	Gate-drain overlap capacitance.
`cgbo=0.0 F/m`	Gate-bulk overlap capacitance.

© 2023 Cadence Design Systems, Inc.

`ovslp=2.1E-7`	Parameter for overlap capacitance.
`ovmag=0.6`	Parameter for overlap capacitance.
`vfbover=0.0 V`	Flat-band voltage in overlap region, existed from 2.40.
`nover=1e19 cm`$^{-3}$	Impurity concentration in overlap region, existed from 2.40.

Smoothing coefficient between linear and saturation

`ddltmax=10.0`	Coefficient of effective electric field, existed from 2.40.
`ddltslp=0.0`	Lgate dependence of smoothing coefficient, existed from 2.40.
`ddltict=10.0`	Lgate dependence of smoothing coefficient, existed from 2.40.

DFM parameters

`mphdfm=-0.3`	NSUBCDFM dependence of phonon scattering for DFM, existed from 2.40.

Depletion Mode Model Paramrters

`covdsres=3`	Vdssatres,Vdsres model switch: (-1) Vdsres=Vds; (3) Vdssatres ln(1+exp) depmos3.
`depcar=0.0`	Coefficient for Ndrift,res CODEP=3.
`depdvfbc=0.1`	Delta of Flat-band voltage of the resistor part (CODEP=3).
`depfdpd=0.2`	Smoothing param for FD/PD transition depmos3.
`deppb0=0.5`	Flooring for Eeff for Mu_res depmos3.
`depqf=4.0`	Smoothing param for Vdseff depmos3.
`deprdrdl1=0.0`	RDRDL1 for resistor layer CODEP=3.
`deprdrdl2=0.0`	Pinch-off length in resistor layer CODEP=3.
`depmue0=1e3`	Depletion model parameter.

© 2023 Cadence Design Systems, Inc.

depmue0l=0.0	Depletion model parameter.
depmue0lp=1.0	Depletion model parameter.
depmue1=0.0	Depletion model parameter.
depmue1l=0.0	Depletion model parameter.
depmue1lp=1.0	Depletion model parameter.
depmueback0=1e2	Depletion model parameter.
depmueback0l=0.0	Depletion model parameter.
depmueback0lp=1.0	Depletion model parameter.
depmueback1=0.0	Depletion model parameter.
depmueback1l=0.0	Depletion model parameter.
depmueback1lp=1.0	Depletion model parameter.
depmueph0=0.3	Depletion model parameter.
depmueph1=5e3	Depletion model parameter.
depvmax=3e7	Depletion model parameter.
depvmaxl=0.0	Depletion model parameter.
depvmaxlp=1.0	Depletion model parameter.
depvdsef1=2.0	Depletion model parameter.
depvdsef1l=0.0	Depletion model parameter.
depvdsef1lp=1.0	Depletion model parameter.
depvdsef2=0.5	Depletion model parameter.
depvdsef2l=0.0	Depletion model parameter.
depvdsef2lp=1.0	Depletion model parameter.
depbb=1.0	Depletion model parameter.

© 2023 Cadence Design Systems, Inc.

depmuetmp=1.5	Depletion model parameter.

WPE: Well Proximity Effects parameters

web=0.0	Modification of layout characterization factor.
wec=0.0	Modification of layout characterization factor.
nsubcwpe=0.0 cm^{-3}	Channel concentration change due to WPE.
npextwpe=0.0 cm^{-3}	Pocket-tail concentration change due to WPE.
nsubpwpe=0.0 cm^{-3}	Pocket concentration change due to WPE.

Binning model parameters which are existed from 2.40

lbinn=1.0	L modulation coefficient for binning.
wbinn=1.0	W modulation coefficient for binning.
lvmax=0.0 cm/s	Length dependence of vmax.
lbgtmp1=0.0 eV/K	Length dependence of bgtmp1.
lbgtmp2=0.0 eV/K^2	Length dependence of bgtmp2.
leg0=0.0 eV	Length dependence of eg0.
llover=0.0 m	Length dependence of lover.
lvfbover=0.0 V	Length dependence of vfbover.
lnover=0.0 cm^{-3}	Length dependence of nover.
lwl2=0.0	Length dependence of wl2.
lvfbc=0.0 V	Length dependence of vfbc.
lnsubc=0.0 cm^{-3}	Length dependence of nsubc.
lnsubp=0.0 cm^{-3}	Length dependence of nsubp.
lscp1=0.0 1/V	Length dependence of scp1.
lscp2=0.0 $1/V^2$	Length dependence of scp2.

© 2023 Cadence Design Systems, Inc.

`lscp3=0.0 m/V`^{2}	Length dependence of scp3.
`lsc1=0.0 1/V`	Length dependence of sc1.
`lsc2=0.0 1/V`^{2}	Length dependence of sc2.
`lsc3=0.0 m/V`^{2}	Length dependence of sc3.
`lpgd1=0.0 V`	Length dependence of pgd1.
`lndep=0.0`	Length dependence of ndep.
`lninv=0.0`	Length dependence of ninv.
`lmuecb0=0.0 cm`^{2}`/(V s)`	Length dependence of muecb0.
`lmuecb1=0.0 cm`^{2}`/(V s)`	Length dependence of muecb1.
`lmueph1=0.0`	Length dependence of mueph1.
`lvtmp=0.0 cm/s`	Length dependence of vtmp.
`lwvth0=0.0`	Length dependence of wvth0.
`lmuesr1=0.0`	Length dependence of muesr1.
`lmuetmp=0.0`	Length dependence of muetmp.
`lsub1=0.0 1/V`	Length dependence of sub1.
`lsub2=0.0 V`	Length dependence of sub2.
`lsvds=0.0`	Length dependence of svds.
`lsvbs=0.0`	Length dependence of svbs.
`lsvgs=0.0`	Length dependence of svgs.
`lnsti=0.0 cm`$^{-3}$	Length dependence of nsti.
`lwsti=0.0 m`	Length dependence of wsti.
`lscsti1=0.0`	Length dependence of scsti1.
`lscsti2=0.0 1/V`	Length dependence of scsti2.
`lvthsti=0.0`	Length dependence of vthsti.
`lmuesti1=0.0`	Length dependence of muesti1.
`lmuesti2=0.0`	Length dependence of muesti2.
`lmuesti3=0.0`	Length dependence of muesti3.
`lnsubpsti1=0.0 m`	Length dependence of nsubpsti1.
`lnsubpsti2=0.0 m`	Length dependence of nsubpsti2.

© 2023 Cadence Design Systems, Inc.

`lnsubpsti3=0.0 m`	Length dependence of nsubpsti3.
`lcgso=0.0 F/m`	Length dependence of cgso.
`lcgdo=0.0 F/m`	Length dependence of cgdo.
`ljs0=0.0 A/m`^{2}	Length dependence of js0.
`ljs0sw=0.0 A/m`	Length dependence of js0sw.
`lnj=0.0`	Length dependence of nj.
`lcisbk=0.0 A`	Length dependence of cisbk.
`lclm1=0.0`	Length dependence of clm1.
`lclm2=0.0 1/m`	Length dependence of clm2.
`lclm3=0.0`	Length dependence of clm3.
`lwfc=0.0 m F/cm`^{2}	Length dependence of wfc.
`lgidl1=0.0 A m/(V^(3/2) c^(1/2))`	Length dependence of gidl1.
`lgidl2=0.0 1/(V^(1/2) c^(3/2) m)`	Length dependence of gidl2.
`lgleak1=0.0 A/(V^(3/2) c^(1/2))`	Length dependence of gleak1.
`lgleak2=0.0 1/(V^(1/2) c^(3/2) m)`	Length dependence of gleak2.
`lgleak3=0.0`	Length dependence of gleak3.
`lgleak6=0.0 V`	Length dependence of gleak6.
`lglksd1=0.0`	Length dependence of glksd1.
`lglksd2=0.0`	Length dependence of glksd2.
`lglkb1=0.0`	Length dependence of glkb1.
`lglkb2=0.0`	Length dependence of glkb2.
`lnftrp=0.0`	Length dependence of nftrp.
`lnfalp=0.0`	Length dependence of nfalp.
`lvdiffj=0.0 V`	Length dependence of vdiffj.
`libpc1=0.0`	Length dependence of ibpc1.

© 2023 Cadence Design Systems, Inc.

`libpc2=0.0`	Length dependence of ibpc2.
`lsc4=0.0`	Length dependence of sc4.
`wvmax=0.0 cm/s`	Width dependence of vmax.
`wbgtmp1=0.0 eV/K`	Width dependence of bgtmp1.
`wbgtmp2=0.0 eV/K`^{2}	Width dependence of bgtmp2.
`weg0=0.0 eV`	Width dependence of eg0.
`wlover=0.0 m`	Width dependence of lover.
`wvfbover=0.0 V`	Width dependence of vfbover.
`wnover=0.0 am`$^{-3}$	Width dependence of over.
`wwl2=0.0`	Width dependence of wl2.
`wvfbc=0.0 V`	Width dependence of FPC.
`wnsubc=0.0 cm`$^{-3}$	Width dependence of nsubc.
`wnsubp=0.0 cm`$^{-3}$	Width dependence of nsubp.
`wscp1=0.0 1/V`	Width dependence of scp1.
`wscp2=0.0 1/V`^{2}	Width dependence of scp2.
`wscp3=0.0 m/V`^{2}	Width dependence of scp3.
`wsc1=0.0 1/V`	Width dependence of sc1.
`wsc2=0.0 1/V`^{2}	Width dependence of sc2.
`wsc3=0.0 m/V`^{2}	Width dependence of sc3.
`wpgd1=0.0 V`	Width dependence of pgd1.
`wndep=0.0`	Width dependence of ndep.
`wninv=0.0`	Width dependence of ninv.
`wmuecb0=0.0 cm`^{2}`/(V s)`	Width dependence of muecb0.
`wmuecb1=0.0 cm`^{2}`/(V s)`	Width dependence of muecb1.
`wmueph1=0.0`	Width dependence of mueph1.
`wvtmp=0.0 cm/s`	Width dependence of vtmp.
`wwvth0=0.0`	Width dependence of wvth0.
`wmuesr1=0.0`	Width dependence of muesr1.
`wmuetmp=0.0`	Width dependence of muetmp.

© 2023 Cadence Design Systems, Inc.

`wsub1=0.0 1/V`	Width dependence of sub1.
`wsub2=0.0 V`	Width dependence of sub2.
`wsvds=0.0`	Width dependence of svds.
`wsvbs=0.0`	Width dependence of svbs.
`wsvgs=0.0`	Width dependence of svgs.
`wnsti=0.0` cm^{-3}	Width dependence of nsti.
`wwsti=0.0 m`	Width dependence of wsti.
`wscsti1=0.0`	Width dependence of scsti1.
`wscsti2=0.0 1/V`	Width dependence of scsti2.
`wvthsti=0.0`	Width dependence of vthsti.
`wmuesti1=0.0`	Width dependence of muesti1.
`wmuesti2=0.0`	Width dependence of muesti2.
`wmuesti3=0.0`	Width dependence of muesti3.
`wnsubpsti1=0.0 m`	Width dependence of nsubpsti1.
`wnsubpsti2=0.0 m`	Width dependence of nsubpsti2.
`wnsubpsti3=0.0 m`	Width dependence of nsubpsti3.
`wcgso=0.0 F/m`	Width dependence of cgso.
`wcgdo=0.0 F/m`	Width dependence of cgdo.
`wjs0=0.0 A/m`^{2}	Width dependence of js0.
`wjs0sw=0.0 A/m`	Width dependence of js0sw.
`wnj=0.0`	Width dependence of nj.
`wcisbk=0.0 A`	Width dependence of cisbk.
`wclm1=0.0`	Width dependence of clm1.
`wclm2=0.0 1/m`	Width dependence of clm2.
`wclm3=0.0`	Width dependence of clm3.
`wwfc=0.0 m F/cm`^{2}	Width dependence of wfc.
`wgidl1=0.0 A m/(V^(3/2) c^(1/2))`	Width dependence of gidl1.
`wgidl2=0.0 1/(V^(1/2) c^(3/2) m)`	

© 2023 Cadence Design Systems, Inc.

	Width dependence of gidl2.
`wgleak1=0.0 A/(V^(3/2) c^(1/2))`	
	Width dependence of gleak1.
`wgleak2=0.0 1/(V^(1/2) c^(3/2) m)`	
	Width dependence of gleak2.
`wgleak3=0.0`	Width dependence of gleak3.
`wgleak6=0.0 V`	Width dependence of gleak6.
`wglksd1=0.0`	Width dependence of glksd1.
`wglksd2=0.0`	Width dependence of glksd2.
`wglkb1=0.0`	Width dependence of glkb1.
`wglkb2=0.0`	Width dependence of glkb2.
`wnftrp=0.0`	Width dependence of nftrp.
`wnfalp=0.0`	Width dependence of nfalp.
`wvdiffj=0.0 V`	Width dependence of vdiffj.
`wibpc1=0.0`	Width dependence of ibpc1.
`wibpc2=0.0`	Width dependence of ibpc2.
`wsc4=0.0`	Width dependence of sc4.
`pvmax=0.0 cm/s`	Cross-term dependence of vmax.
`pbgtmp1=0.0 eV/K`	Cross-term dependence of bgtmp1.
`pbgtmp2=0.0 eV/K`^{2}	Cross-term dependence of bgtmp2.
`peg0=0.0 eV`	Cross-term dependence of eg0.
`plover=0.0 m`	Cross-term dependence of lover.
`pvfbover=0.0 V`	Cross-term dependence of vfbover.
`pnover=0.0 cm`$^{-3}$	Cross-term dependence of nover.
`pwl2=0.0`	Cross-term dependence of wl2.
`pvfbc=0.0 V`	Cross-term dependence of vfbc.
`pnsubc=0.0 cm`$^{-3}$	Cross-term dependence of nsubc.
`pnsubp=0.0 cm`$^{-3}$	Cross-term dependence of nsubp.
`pscp1=0.0 1/V`	Cross-term dependence of scp1.

© 2023 Cadence Design Systems, Inc.

pscp2=0.0 1/V^2	Cross-term dependence of scp2.
pscp3=0.0 m/V^2	Cross-term dependence of scp3.
psc1=0.0 1/V	Cross-term dependence of sc1.
psc2=0.0 1/V^2	Cross-term dependence of sc2.
psc3=0.0 m/V^2	Cross-term dependence of sc3.
ppgd1=0.0 V	Cross-term dependence of pgd1.
pndep=0.0	Cross-term dependence of ndep.
pninv=0.0	Cross-term dependence of ninv.
pmuecb0=0.0 cm^2/(V s)	Cross-term dependence of muecb0.
pmuecb1=0.0 cm^2/(V s)	Cross-term dependence of muecb1.
pmueph1=0.0	Cross-term dependence of mueph1.
pvtmp=0.0 cm/s	Cross-term dependence of vtmp.
pwvth0=0.0	Cross-term dependence of wvth0.
pmuesr1=0.0	Cross-term dependence of muesr1.
pmuetmp=0.0	Cross-term dependence of muetmp.
psub1=0.0 1/V	Cross-term dependence of sub1.
psub2=0.0 V	Cross-term dependence of sub2.
psvds=0.0	Cross-term dependence of svds.
psvbs=0.0	Cross-term dependence of svbs.
psvgs=0.0	Cross-term dependence of svgs.
pnsti=0.0 cm^{-3}	Cross-term dependence of nsti.
pwsti=0.0 m	Cross-term dependence of wsti.
pscsti1=0.0	Cross-term dependence of scsti1.
pscsti2=0.0 1/V	Cross-term dependence of scsti2.
pvthsti=0.0	Cross-term dependence of vthsti.
pmuesti1=0.0	Cross-term dependence of muesti1.
pmuesti2=0.0	Cross-term dependence of muesti2.
pmuesti3=0.0	Cross-term dependence of muesti3.
pnsubpsti1=0.0 m	Cross-term dependence of nsubpsti1.

© 2023 Cadence Design Systems, Inc.

`pnsubpsti2=0.0 m`	Cross-term dependence of nsubpsti2.
`pnsubpsti3=0.0 m`	Cross-term dependence of nsubpsti3.
`pcgso=0.0 F/m`	Cross-term dependence of cgso.
`pcgdo=0.0 F/m`	Cross-term dependence of cgdo.
`pjs0=0.0 A/m`^{2}	Cross-term dependence of js0.
`pjs0sw=0.0 A/m`	Cross-term dependence of js0sw.
`pnj=0.0`	Cross-term dependence of nj.
`pcisbk=0.0 A`	Cross-term dependence of cisbk.
`pclm1=0.0`	Cross-term dependence of clm1.
`pclm2=0.0 1/m`	Cross-term dependence of clm2.
`pclm3=0.0`	Cross-term dependence of clm3.
`pwfc=0.0 m F/cm`^{2}	Cross-term dependence of wfc.
`pgidl1=0.0 A m/(V^(3/2) c^(1/2))`	Cross-term dependence of gidl1.
`pgidl2=0.0 1/(V^(1/2) c^(3/2) m)`	Cross-term dependence of gidl2.
`pgleak1=0.0 A/(V^(3/2) c^(1/2))`	Cross-term dependence of gleak1.
`pgleak2=0.0 1/(V^(1/2) c^(3/2) m)`	Cross-term dependence of gleak2.
`pgleak3=0.0`	Cross-term dependence of gleak3.
`pgleak6=0.0 V`	Cross-term dependence of gleak6.
`pglksd1=0.0`	Cross-term dependence of glksd1.
`pglksd2=0.0`	Cross-term dependence of glksd2.
`pglkb1=0.0`	Cross-term dependence of glkb1.
`pglkb2=0.0`	Cross-term dependence of glkb2.
`pnftrp=0.0`	Cross-term dependence of nftrp.
`pnfalp=0.0`	Cross-term dependence of nfalp.
`pvdiffj=0.0 V`	Cross-term dependence of vdiffj.

© 2023 Cadence Design Systems, Inc.

`pibpc1=0.0`	Cross-term dependence of ibpc1.
`pibpc2=0.0`	Cross-term dependence of ibpc2.
`psc4=0.0`	Cross-term dependence of sc4.
`vgsmin=-5  type V`	Minimal/maximal expected Vgs (NMOS/PMOS).
`sc3vbs=0.0 V`	Vbs value for clamping sc3.
`muecb0lp=0.0`	L dependence of MUECB0.
`muecb1lp=0.0`	L dependence of MUECB1.
`coqovsm=1`	Select smoothing method of Qover.
`codep=0`	Selector for depletion device.
`ndepm=1e17`	N- layer concentration of the depletion MOS model.
`tndep=0.2e-6`	N- layer depth of the depletion MOS model.
`depleak=0.5`	Leakage current modification parameter for the depletion MOS model.
`depeta=0.0`	Vds dependence of threshold voltage for the depletion MOS model.
`coddlt=0`	Flag used to evaluate DDLT, thus Vdseff. Since version 2.8.0.
`ninvdl=0.0`	LG dependence of NINVD.
`ninvdlp=1.0`	LG dependence of NINVD.
`depleakl=0.0`	L dependence of DEPLEAK.
`depleaklp=1.0`	L dependence of DEPLEAK.
`ndepml=0.0`	L dependence of NDEPM.
`ndepmlp=1.0`	L dependence of NDEPM.
`ndepw=0.0`	Coefficient of Qbm for Eeff.
`ndepwp=1.0`	Coefficient of Qbm for Eeff.
`npextw=0.0`	Modification of extension concentration for narrow width
`npextwp=0.0`	Modification of extension concentration for narrow width
`lnsubcsti1=0.0 m`	Length dependence of nsubcsti1.
`lnsubcsti2=0.0 m`	Length dependence of nsubcsti2.
`lnsubcsti3=0.0 m`	Length dependence of nsubcsti3.

© 2023 Cadence Design Systems, Inc.

wnsubcsti1=0.0 m	Wength dependence of nsubcsti1.
wnsubcsti2=0.0 m	Wength dependence of nsubcsti2.
wnsubcsti3=0.0 m	Wength dependence of nsubcsti3.
pnsubcsti1=0.0 m	Cross-term dependence of nsubcsti1.
pnsubcsti2=0.0 m	Cross-term dependence of nsubcsti2.
pnsubcsti3=0.0 m	Cross-term dependence of nsubcsti3.
lcisbkd=0.0	Length dependence of cisbkd.
lcisbks=0.0	Length dependence of cisbks.
ljs0d=0.0	Length dependence of js0d.
ljs0s=0.0	Length dependence of js0s.
ljs0swd=0.0	Length dependence of js0swd.
ljs0swg=0.0	Length dependence of js0swg.
ljs0sws=0.0	Length dependence of js0sws.
lnjd=0.0	Length dependence of njd.
lnjs=0.0	Length dependence of njs.
lvdiffjd=0.0	Length dependence of vdiffjd.
lvdiffjs=0.0	Length dependence of vdiffjs.
pcisbkd=0.0	Cross-term dependence of cisbkd.
pcisbks=0.0	Cross-term dependence of cisbks.
pjs0d=0.0	Cross-term dependence of js0d.
pjs0s=0.0	Cross-term dependence of js0s.
pjs0swd=0.0	Cross-term dependence of js0swd.
pjs0swg=0.0	Cross-term dependence of js0wg.
pjs0sws=0.0	Cross-term dependence of js0sws.
pnjd=0.0	Cross-term dependence of njd.
pnjs=0.0	Cross-term dependence of njs.
pvdiffjd=0.0	Cross-term dependence of vdiffjd.
pvdiffjs=0.0	Cross-term dependence of vdiffjs.
wcisbkd=0.0	Width dependence of cisbkd.

© 2023 Cadence Design Systems, Inc.

wcisbks=0.0	Width dependence of cisbks.
wjs0d=0.0	Width dependence of js0d.
wjs0s=0.0	Width dependence of js0s.
wjs0swd=0.0	Width dependence of js0swd.
wjs0swg=0.0	Width dependence of js0swg.
wjs0sws=0.0	Width dependence of js0sws.
wnjd=0.0	Width dependence of njd.
wnjs=0.0	Width dependence of njs.
wvdiffjd=0.0	Width dependence of vdiffjd.
wvdiffjs=0.0	Width dependence of vdiffjs.

Auto Model Selector parameters

wmax=1 m	Maximum channel width for which the model is valid.
wmin=0 m	Minimum channel width for which the model is valid.
lmax=1 m	Maximum channel length for which the model is valid.
lmin=0 m	Minimum channel length for which the model is valid.
nsubcsti1=0.0 m	STI Stress Parameter for Nsubc [-].
nsubcsti2=0.0 m	STI Stress Parameter for Nsubc [-].
nsubcsti3=1.0 m	STI Stress Parameter for Nsubc [-].
gidl6=0	Parameter for GIDL [-].
gidl7=1	Parameter for GIDL [-].
coerrrep=1	Selector for error report.
cofixcss=0	Selector for Css problem.
info=0	Print information.
nsubpdlt=0.01	Delta for nsubp smoothing [-].
vfbcl=0.0	Gate-length dependence of VFBC [um].
vfbclp=1.0	Gate-length dependence of VFBC [-].
depddlt=3.0	Smoothing coefficient for Vds, res.

© 2023 Cadence Design Systems, Inc.

`depmue0tmp=0.0`	Temperature dependence of DEPmue0.
`depmue2=1E3`	Coulomb scattering of the resistor part.
`depmue2tmp=0.0`	Temperature dependence of DEPmue2.
`depmuea1=0.0`	Modification of mures.
`depninvd=0`	NINVD for Mu_res depmos3.
`depninvdc=0`	Modification of Vdse dependence on Eeff (for Mu_res) (CODEP=3).
`depninvdh=0`	Modification of Vdse dependence on Eeff (for Mu_res) (CODEP=3).
`depninvdl=0`	NINVDL for Mu_res depmos3.
`depninvdlp=1.0`	NINVDLP for Mu_res depmos3.
`depninvdw=0.0`	Coefficient of modification of Vdse dependence on Eeff; Mu_res (CODEP=3).
`depninvdwp=1.0`	Coefficient of modification of Vdse dependence on Eeff; Mu_res (CODEP=3).
`deprbr=1`	Parameter for resistance effect along substrate (for minority carrier).
`depps=0.05`	Ps_delta for smoothing charge depmos3.
`depsubsl=2.0`	Factor of the sub-threshold slope.
`depsubsl0=2.0`	Factor of the sub-threshold slope (CODEP=2,3).
`depvfbc=0.2`	Flat-band voltage of the resistor part.
`depvgpsl=0.0`	Smoothing coefficient for gm.
`depvsata=0.0`	Vdssat shift depmos3.
`depvsatr=0.0`	Vbs dependence of subVds,sat of the resistor part.
`depvtmp=0.0`	Temperature dependence of DEPVMAX.
`gdl=0.0`	Strength of high-field effect.
`gdld=0.0`	Channel-length dependence of high-field effect.
`gdlp=0.0`	Channel-length dependence of high-field effect.
`gmin=0.0`	Minimum conductance.
`muephw2=0.0`	Phonon related mobility reduction.

© 2023 Cadence Design Systems, Inc.

`muepwp2=1.0`	Phonon related mobility reduction.
`mupt=0.0`	Mobility for deep punchthrough.
`njd=1.0`	Emission coefficient for drain junction.
`njunc=1e20`	Junction doping conc; deep punchthrough.
`nsubcw2=0.0`	Modification of substrate concentration for narrow width.
`nsubcwp2=1.0`	Modification of substrate concentration for narrow width.
`nsubd=5e17`	Substrate conc for Vbs effects of dVth; 0.0 (deactivate this effects).
`nsubdnw=0.0`	Substrate conc for Vbs effects of dVth; narrow W effects (vertDop).
`nsubdw=0.0`	NSUBD W-dependence coefficient. (vertDop).
`nsubdw0=5e17`	NSUBD W-dependence constant term (vertDop).
`nsubdwp=1`	NSUBD W-dependence exponent (vertDop).
`ovinvdlt=75.00`	Analytical overlap inversion when COQOVSM=2.
`pslimpt=0.0`	Ps0 limit for deep punchthrough.
`pt2=0.0`	Vds dependence of punchthrough effect.
`pt4=0.0`	Vbs dependence of punchthrough effect.
`pt4p=1.0`	Vbs dependence of punchthrough effect.
`ptl=0.0`	Strength of punchthrough effect.
`ptlp=1.0`	Channel-length dependence of punchthrough effect.
`ptp=3.5`	Strength of punchthrough effect.
`qyrat=0.5`	Partitioning ratio of Qy between source and drain.
`rmin=1E-4`	Minimum resistance for RS / RD.
`toxov=3E-9`	Oxide thickness of overlap region.
`vbdr_max=vbd_max V`	Maximum allowed reverse voltage across bulk and drain.
`vbsr_max=vbs_max V`	Maximum allowed reverse voltage across bulk and source.
`vbsrfar=(-30.0)`	Reversely biasing Vb[s|d] farthest from 0 (negatively large;nMOS)(positively large; pMOS).
`vfbpt=0.0`	dVfb for deep punchthrough.
`vgbr_max=vgb_max V`	Maximum allowed reverse voltage across gate and bulk.

© 2023 Cadence Design Systems, Inc.

`vsftd=0`	Shift Vth vs sqrt(2/phi-Vbs) line for substrate.
`xjpt=3E-8`	Junction depth; deep punchthrough.
`xldc=0.0`	Lateral diffusion of S/D under the gate (capacitance).
`wdepv=10.0`	Cross point of dVthVertdnw and dVthVertd lines (vertDop).
`xwdc=0.0`	Lateral diffusion along the width dir. (capacitance).

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).
`weff (m)`	Effective channel width.
`leff (m)`	Effective channel length.
`rseff (Ω)`	Effective source resistance.
`rdeff (Ω)`	Effective drain resistance.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`reversed`	Reverse mode indicator. Possible values are `yes` and `no`.
`ids (A)`	Resistive drain-to-source current.
`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`vbs (V)`	Bulk-source voltage.
`vth (V)`	Threshold voltage.
`vdsat (V)`	Drain-source saturation voltage.
`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`gmbs (S)`	Body-transconductance.
`qb (Coul)`	Total bulk charge.
`qd (Coul)`	Total drain charge.
`qg (Coul)`	Total gate charge.
`qs (Coul)`	Total source charge.
`cjd (F)`	Drain-bulk junction capacitance.
`cjs (F)`	Source-bulk junction capacitance.
`cgg (F)`	dQg_dVg.
`cgd (F)`	dQg_dVd.
`cgs (F)`	dQg_dVs.
`cgb (F)`	dQg_dVb.
`cdg (F)`	dQd_dVg.
`cdd (F)`	dQd_dVd.
`cds (F)`	dQd_dVs.
`cdb (F)`	dQd_dVb.
`csg (F)`	dQs_dVg.

© 2023 Cadence Design Systems, Inc.

csd (F)	dQs_dVd.
css (F)	dQs_dVs.
csb (F)	dQs_dVb.
cbg (F)	dQb_dVg.
cbd (F)	dQb_dVd.
cbs (F)	dQb_dVs.
cbb (F)	dQb_dVb.
id (A)	Resistive drain current.
ig (A)	Gate current.
is (A)	Resistive source current.
ibulk (A)	Resistive bulk current.
pwr (W)	Power at operating point.
ps0 (V)	Surface potential at source side.
psl (V)	Surface potential at drain side.
pds (V)	Delta surface potential between psl and ps0.
isub (A)	Substrate current Isub.
gbds (S)	Substrate trans conductance (dIsub/dVds).
gbgs (S)	Substrate trans conductance (dIsub/dVgs).
gbbs (S)	Substrate transconductance (dIsub/dVbs).
igate (A)	Gate current due to tunneling.
igates (A)	Tunneling current from gate to source.
igateb (A)	Tunneling current from gate to bulk.
igated (A)	Tunneling current from gate to drain.
igisl (A)	Gate-induced source leakage current.
igidl (A)	Gate-induced drain leakage current.
ibs (A)	Source-bulk diode current.
ibd (A)	Source-drain diode current.
cgso (F)	Gate-source overlap capacitance.
cgbo (F)	Gate-bulk overlap capacitance.

© 2023 Cadence Design Systems, Inc.

`cgdo (F)`	Gate-drain overlap capacitance.

© 2023 Cadence Design Systems, Inc.

31

HISIM_HV Model (hisim_hv)

HiSIM HVMOS (HiSIM_HV) is an extension of HiSIM model that is a surface potential based MOSFET model. HiSIM_HV adds high voltage device specific feature, like drift region resistance, and so on. It can be used to model both laterally-diffused MOS (LDMOS) and high-voltage MOS (HVMOS) types of device structures. HiSIM_HV is selected as CMC's standard high voltage device model. The latest model version is HiSIM_HV 2.50.

This chapter contains the following information about the HiSIM_HV model:

- Model Concepts on page 2443
- Model Usage on page 2446
  - Instance Syntax on page 2446
  - Model Syntax on page 2447
- Model Version and Development on page 2447
- Version Update and Enhancement on page 2449
  - Version 2.41 Enhancement on page 2449
  - Version 2.40 Enhancement on page 2450
  - Version 2.33 Enhancement on page 2451
  - Version 2.32 Enhancement on page 2451
  - Version 2.31 Enhancement on page 2451
  - Version 2.30 Enhancement on page 2452
  - Version 2.20 Enhancement on page 2452
  - Version 1.24 Enhancement on page 2454
  - Version 2.10 Enhancement on page 2454
  - Version 2.01 Enhancement on page 2455

© 2023 Cadence Design Systems, Inc.

- Version 1.23 Enhancement on page 2455
- Version 2.00 Enhancement on page 2455
- Version 1.22 Enhancement on page 2457
- Version 1.12 Enhancement on page 2458
- Version 1.21 Enhancement on page 2458
- Version 1.20 Enhancement on page 2458

■ Reference on page 2460

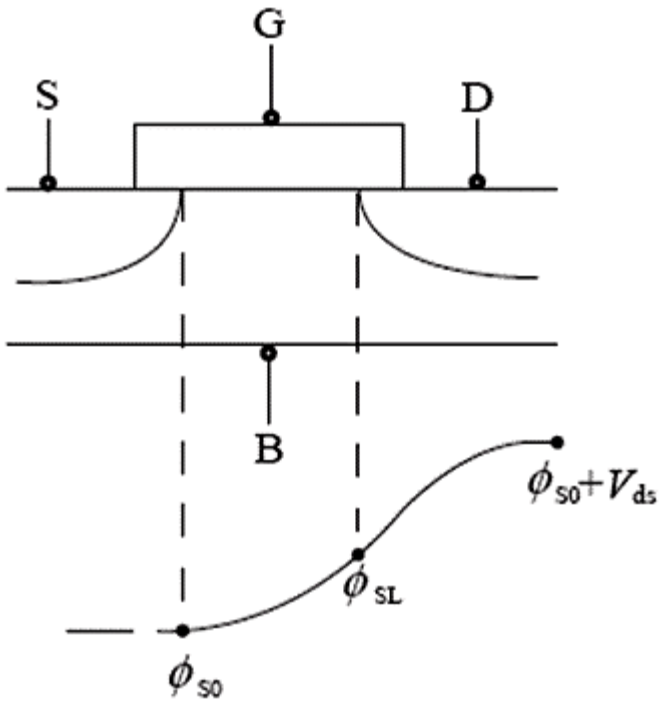
- Model Equations on page 2460
- Component Statements on page 2477

© 2023 Cadence Design Systems, Inc.

Model Concepts

HiSIM (Hiroshima-university STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation based on the drift-diffusion theory, which was originally developed by Pao and Sah. The most important advantage of the surface-potential-based modeling is the unified description of device characteristics for all bias conditions. The physical reliability of the drift-diffusion theory has been proved by 2D device simulations with channel lengths even down to below 0.1um.

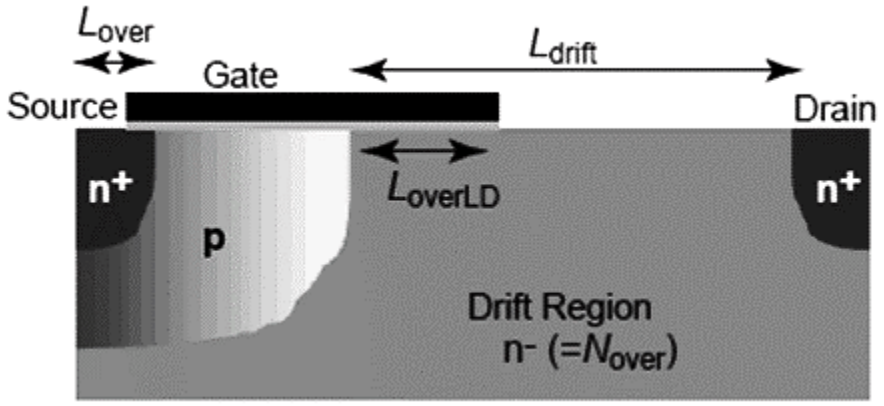
Figure 31-1 Schematic of the surface potential distribution in the channel



The most important feature of LDMOS/HVMOS devices, different from the conventional MOSFET, is that the drift region is introduced to achieve the sustainable high voltages. By varying the length as well as the dopant concentration of the drift region, various devices with various operating bias conditions are realized as shown in Fig. 31-2 or the LDMOS structure. In any cases, the drift region affects as the resistance for the current flow and also induces additional charge, which causes the especially unique features of the LDMOS capacitances. Thus accurate modeling of the drift region is the main task of HiSIM_HV.

© 2023 Cadence Design Systems, Inc.

Figure 31-2 Schematic of the typical LDMOS structure and device parameters



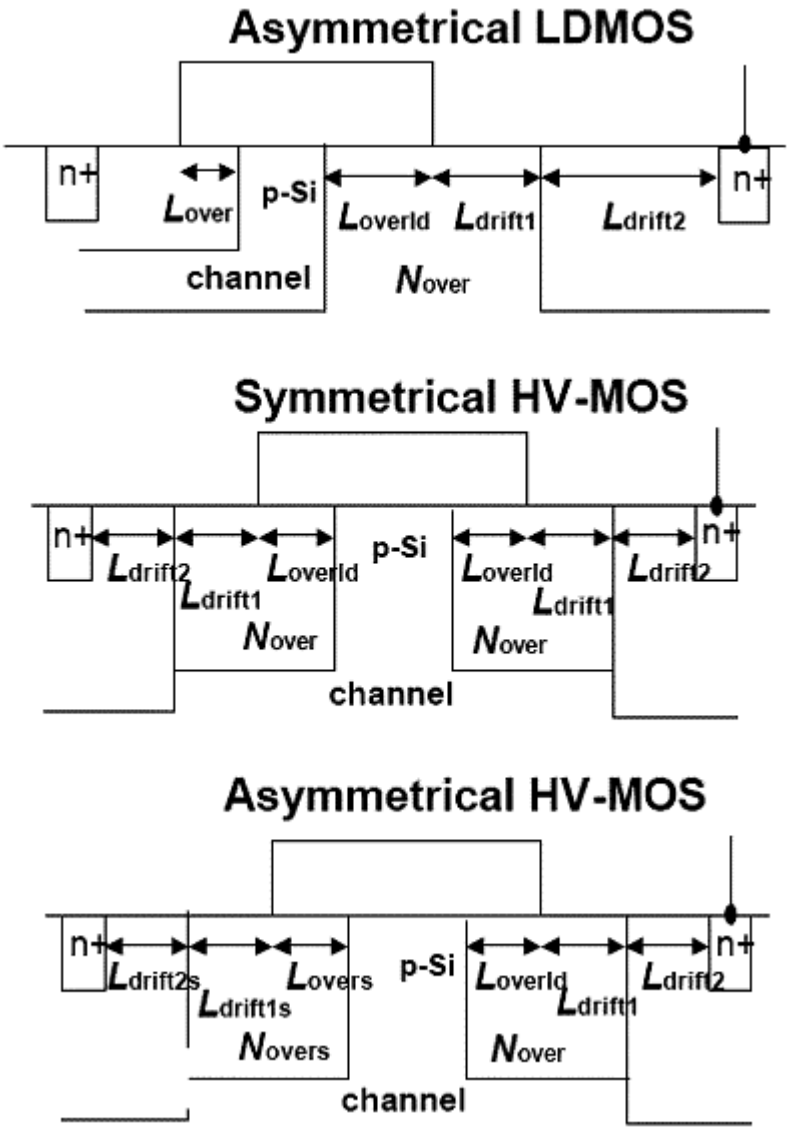
For the LDMOS/HVMOS device the iterative solution is only one possible solution to model the specific features of this device accurately, because the resistance effect in the drift region is dependent on the bias condition as well as the geometrical structure. The basic modeling method is taken over from the HiSIM2 model, and additional equations for capturing the drift-region effects are included. Since the overlap length is relatively long for LDMOS/HVMOS, accurate surface potential calculation for the overlap region is also necessary for accurate prediction of the high-voltage MOS capacitances.

For the LDMOS/HVMOS device the iterative solution is only one possible solution to model the specific features of this device accurately, because the resistance effect in the drift region is dependent on the bias condition as well as the geometrical structure. The basic modeling method is taken over from the HiSIM2 model, and additional equations for capturing the drift-region effects are included. Since the overlap length is relatively long for LDMOS/HVMOS, accurate surface potential calculation for the overlap region is also necessary for accurate prediction of the high-voltage MOS capacitances.

Three types of devices structure can be modeled since HiSIM_HV version 1.2.0 and 1.1.1: Asymmetrical LDMOS, Symmetrical HV-MOS and Asymmetrical HV-MOS. Model parameter **COSYM** determines the devices symmetry and L_{drift}, the overlap length L_{over}, as well as the impurity concentration of the drift region N_{over} determine the characteristics of respectively side. In the LDMOS case independent structures at the source side and the drain side are distinguished, and the L_{drift} region is not introduced at the source side. In the HVMOS case, the parameter values for the drain side have to be determined, and are copied to the source side automatically. If parameters for the source side are determined explicitly, these values are taken. If parameters are not determined, values at the drain side are taken. If the parameter values are not determined, default values are taken. This is valid for any structural cases. Fig. 31-3 shows three different devices structures and table 31-1 shows the model parameters used by different structures.

© 2023 Cadence Design Systems, Inc.

Figure 31-3 Three different devices structure and related model parameters



© 2023 Cadence Design Systems, Inc.

Table 31-1 The different model parameters used by different structures

	Structure	Source	Drain
COSYM=0	LDMOS	LOVERS	LOVERLD
			LDRIFT1
			LDRIFT2
			NOVER
COSYM=1	Symmetrical HVMOS		LOVERLD
			LDRIFT1
			LDRIFT2
			NOVER
COSYM=1	Asymmetrical HVMOS	LOVERS	LOVERLD
		LDRIFT1S	LDRIFT1
		LDRIFT2S	LDRIFT2
		NOVERS	NOVER

Model Usage

HiSIM_HV model definition is used to describe the behavior of devices which has same model characteristics and the instance parameters can be used to describe the characteristics that belong to the specific device.

Instance Syntax

HiSIM_HV instance need specify at least 4 terminals and up to 6 terminals can be supplied. If the 5th terminal is given and **COSUBNODE**=0, it is used as external self-heating node and the self-heating information can be obtained with it when the self-heating effect is activated. If 5th terminal is not given and the self-heating effect is activated, another internal self-heating node is created and used to save related information. If the 5th terminal is given and **COSUBNODE**=1, it is used as substrate node and the self-heating information will be saved with internal node when **COSELFHEAT**=1. If 6 nodes are specified, the 5th node is substrate node and the 6th node is thermal node. To specify HiSIM_HV instance element, the ModelName has to be associated with a HiSIM_HV model card.

```
InstanceName d g s b [sub|th][th] ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

m4 (d g s b) nch w=2u l=0.8u as=250p ad=250p pd=168p ps=168p m=2

Model Syntax

The following syntax specifies HiSIM_HV model:

```
model ModelName hisim_hv parameter=value ...
```

The third parameter, “hisim_hv”, is the master to indicate this model card is a HiSIM_HV model card.

Sample Model Statement

model nch hisim_hv type=n version=2.10 corsrd=3 rs=2.0e-3 rd=1.0e-3 rdtemp1=1e-4 xldld=0

Model Version and Development

Spectre supports all HiSIM_HV versions with different simulator versions. Version control takes effect with all MMSIM versions starting with MMSIM711. Different model versions are supported by different MMSIM releases. For example, MMSIM72 supports version 1.11, 1.12, 1.20, and 1.21 and SPECTRE171 supports version 1.11, 1.12, 1.20, 1.21, 1.22, 1.23, 1.24, 2.00, 2.01, 2.10, 2.20, 2.30, 2.31, 2.32, 2.33, 2.40, 2.41, and 2.50. The latest model version is 2.50 and 2.10 has been kept as the default version. Different model versions can be obtained by setting different model parameter VERSION = 1.11/1.12/1.20/1.21/1.22/1.23/1.24/2.00/2.01/2.10/2.20.2.30/2.31/2.32/2.33/2.40/2.41/2.50. The parameter cannot be parameterized, its value must be constant. If no version is set in the model card, the latest version is used by different versions of simulator. For example, 2.10 is used by MMSIM131 and 1.21 is used by MMSIM72.

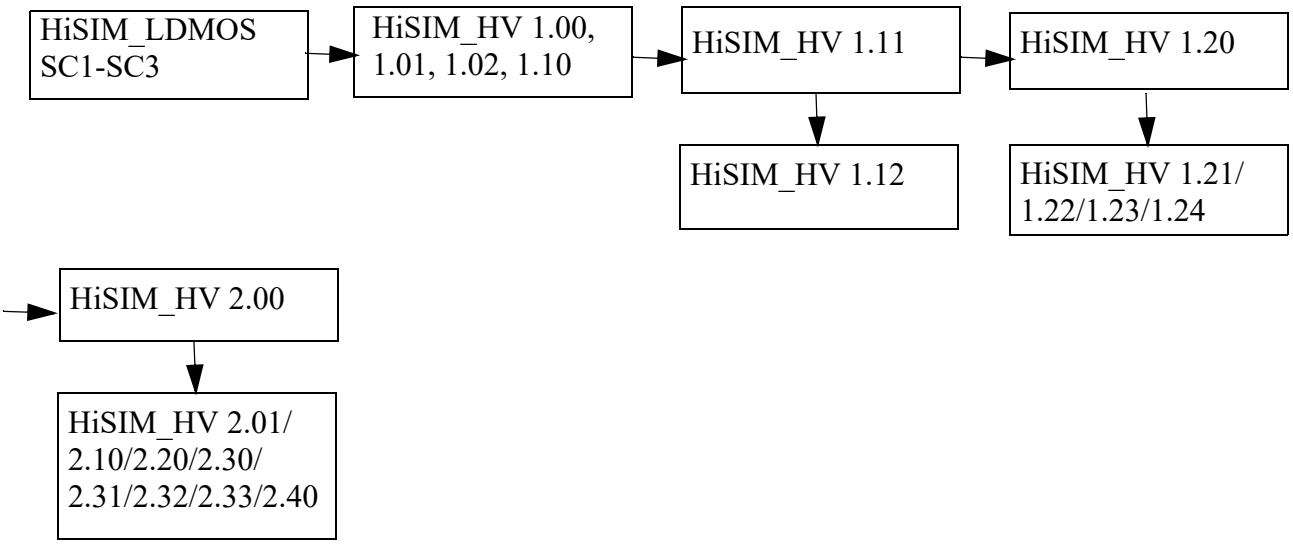
There were some known issues in the old model versions 1.11 and 1.12. These issues have been resolved in versions 1.2X and 2.XX. Therefore, starting with the MMSIM 121 ISR12 release, the old versions 1.11 and 1.12 have been retired. However, you can use the `enable_pre_ver=yes` option to activate these versions.

In the 2.43 beta version, we implemented the enhancement which was released in March 2021 to Spectre hisim_hv version 2.30 – 2.41. Model parameters `covbscl`, `coqovcl`, `vbfwdmx` and `vbfwdbnd` are added in this update. Flag parameter ‘`beta_update`’ is added to control the enhancement.

The following figure shows the model version and development flow for the HiSIM_HV model.

© 2023 Cadence Design Systems, Inc.

Figure 31-4 HiSIM_HV Model Version and Development Flow



Following lists the model versions and their corresponding simulator version for your reference:

HiSIM_LDMOS SC3	MMSIM 7.0
HiSIM_HV 1.00 (LDMOS SC4)	MMSIM 7.0 ISR
HiSIM_HV 1.02	MMSIM 7.1
HiSIM_HV 1.11/1.12	MMSIM 7.1.1
HiSIM_HV 1.11/1.12/1.20/1.21	MMSIM 7.2ISR
HiSIM_HV 1.11/1.12/1.20/1.21/1.22	MMSIM 10.1ISR
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/2.00 beta version	MMSIM 10.1ISR14
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/2.00 final version	MMSIM 10.1ISR17
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/2.00 default	MMSIM 10.1ISR20
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/2.00/ 2.01	MMSIM 11.1 ISR9
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 2.00/2.01	MMSIM 11.1 ISR10

© 2023 Cadence Design Systems, Inc.

HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 2.00/2.01/2.10	MMSIM 12.1 ISR8
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 1.24/2.00/2.01/2.10	MMSIM 12.1 ISR12
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 1.24/2.00/2.01/2.10	MMSIM 13.1
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 1.24/2.00/2.01/2.10/2.20	MMSIM 13.1 ISR10
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 1.24/2.00/2.01/2.10/2.20/2.30/2.31	MMSIM 14.1 ISR6
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 1.24/2.00/2.01/2.10/2.20/2.30/2.31.2.32	MMSIM 15.1 ISR12
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 1.24/2.00/2.01/2.10/2.20/2.30/2.31.2.32/2.33	MMSIM 16.1 ISR5
HiSIM_HV 1.11/1.12/1.20/1.21/1.22/1.23/ 1.24/2.00/2.01/2.10/2.20/2.30/2.31.2.32/ 2.33/2.40	SPECTRE 18.1

For any questions, contact Cadence Customer Support.

Version Update and Enhancement

Version 2.41 Enhancement

The 2.41 version of HiSIM_HV contains the following changes:

Enhancement

Introduced geometry-dependence to NDEPM. New parameters NDEPML and NDEPMLP are added with defaults `0` and `1`, respectively.

$$NDEPM \cdot \left(1 + \frac{NDEPML}{\left(L_{gate} \times 10^{6} \right)^{NDEPMLP}} \right)$$

© 2023 Cadence Design Systems, Inc.

Bug Fix

Improvement on gm at high Vd with back bias dependence.

Note: This improvement may cause backward incompatibility for CODEP=3.

Version 2.40 Enhancement

The 2.40 version of HiSIM_HV contains the following changes:

Enhancements

- Support added for the following models:
  - Depletion mode model (CODEP=3)
  - Resistance model for source drift region (CORDRIFT=1)
  - Snapback model (COSNP=1)
- The new flags CORS and CORD are introduced for activation of the newer model for drift region resistance (CORDRIFT=1) on the source and the drain side, respectively.
- Source/Bulk and Drain/Bulk junction diode's internal node connection (CODIO=1)
- NQS effect in overlap charge (CONQSOV=1)
- Gate/drain overlap capacitance for trench-gate structures (COTRENCH=1)

  Note: Only CVDSOVER=0 (default) is active. Non-zero CVDSOVER for COTRENCH=1 is neglected.
- Implementation of node-collapsing using the port connect mechanism.

Bug fixes

- Parameter boundaries are revised for mitigating possible math errors.
- Some if statements that would potentially hinder Verilog-A's auto-generation of derivatives are revised.
- Some numerical codes for mitigating loss of accuracy are revised.
- Operating variable's sign and missing M-factor are corrected.
- The OP output, Cdd, is enhanced to make it more physical.

© 2023 Cadence Design Systems, Inc.

Version 2.33 Enhancement

The 2.33 version of HiSIM_HV contains the following changes:

Specification change

- The lower boundary of the parameter range for LDRIFT2 has been changed from open boundary (excludes 0) to closed one (includes 0) to match the document description.
- Implemented a parameter range check for LDRIFT1+LDRIFT2 to protect against zero division in subsequent calculations in the drift resistance part.

Version 2.32 Enhancement

The 2.32 version of HiSIM_HV contains the following enhancements and bug fixes:

Enhancements

- Computation of Ps0_iniA
- Small is used in the HiSIM-HV code
- RD/RS calculations in CORDRIFT=0
- Negative Ndrift
- Optimization of the code in “if (mode > 0)” block

Bug fixes

- Non-zero Ids(1e-12) at Vds=0
- Discontinuity in Cox vs Vgb simulation
- Cover limitation according to the overlap depth DDRIFT.
- Discontinuity in Cover at Vfb

Version 2.31 Enhancement

Version 2.31 of HiSIM_HV is an enhanced version of 2.30. In version 2.31, a new value, 2 has been added to the model parameter COSELFHEAT. When COSELFHEAT=2, a different thermal node solution limiting methodology is used than COSELFHEAT=1.

© 2023 Cadence Design Systems, Inc.

Version 2.30 Enhancement

The 2.30 version of HiSIM_HV contains the following enhancements and bug fixes:

Enhancement

- New break down model
- Improvement in the CORDRIFT=1 resistance model with fifth node
- Improvement in the Qover model with Cgd dependency on Vds
- Added TK and DTSH (* Temperature increase due to self-heating *) to OP variables.
- Improvement in the depletion mode model with CODEP=2, where CODEP=1 refers the version 2.2.0 model.
- Improvement in the ranges in the parameter declaration.
- Improvement in the temperature dependence of Isub

Bugfixes

- FPE in the 1/f noise calculation.
- Negative effective channel width (Weff) of the drift region and resulting negative capacitance.
- Discontinuity in capacitances when QY model is activated.
- Discontinuity in the second derivative of Isub in CODEP=1.
- Non-convergence when CODEP=1 and COIIGS=1.
- Removal of the minimum value checking for NINDVT1 and NINVDT2.
- Added range checking of the model parameter value after calculation of Lgate, Wgate, and temperature dependence.

Version 2.20 Enhancement

The 2.20 version of HiSIM_HV contains the following enhancements and bug fixes:

- A new depletion mode device has been added
  - Following new model parameters have been added for the depletion model selection:
    - CODEP=1: use the new depletion mode model

© 2023 Cadence Design Systems, Inc.

- CODEP=0: use the old model

- Following new parameters have been added for the resistor part in the surface layer:
  - DEPMUE0, DEPMUE1: Coulomb scattering
- Following new parameters have been added for the back part in the surface layer:
  - DEPMUEBACK0, DEPMUEBACK1: Coulomb scattering
- Following new parameters have been added for both resistor part and back part:
  - DEPMUEPH0, DEPMUEPH1: Phonon scattering
  - DEPVAMX, DEPBB: High field mobility
  - DEPVDSEF1, DEPVDSEF2: Vds dependence
- Following new parameters have been added for temperature dependence:
  - DEPMUETMP: Temperature dependence on mobility
  - DEPVTEMP: Temperature dependence on the saturation velocity

Note: The current depletion model does not support STI leakage, channel length modulation, thermal noise, and induced gate noise.

- Temperature dependence of drift mobility model has been modified
- Channel length dependence for Gds has been improved.
  - CODDLT=1: use new Vds,eff model (default)
  - CODDLT=0: use previous Vds,eff model
- Range values of the following parameters has been changed:
  - Maximum value of SHEMAX has been changed from 600 to 900
  - Maximum value of XWDC has been changed from -10nm to -500nm
  - Minimum value of VFBOVER has been changed from -1.0 to -1.2
  - Maximum value of VFBC has been changed from -0.4 to 0.0
  - Maximum value of SC3 has been changed from 200n to 20µ
- Following bugs have been fixed:
  - Problem related to division by zero has been resolved
  - Comments for some model parameters have been modified

© 2023 Cadence Design Systems, Inc.

- Invalidation of GMIN parameter
- Charge and capacitance calculation (noise and fringing capacitance)
- Source resistance has been added for noise calculation
- LDRIFT parameter has been removed
- Vbs dependence of the printed output for Vth
- Model names have been changed in the error messages
- The default value of LOVERS parameter is changed. Now, if LOVERS parameter is not specified, the value of LOVER parameter is used.

Version 1.24 Enhancement

The 1.24 version of HiSIM_HV contains the following bug fixes:

- Incorrect referencing to total W instead of W per finger
- Derivative calculations with respect to the temperature

Version 2.10 Enhancement

The 2.10 version of HiSIM_HV contains the following enhancements and bug fixes:

- Degradation of mobility in the drift region with new model parameter `RDRBB`.
- Additional overlap capacitance with new model parameter `QOVADD`.
- Improved smoothness of drift resistance at `Vds=0`.
- Changed default/min/max values of model parameters `NOVER`, `NOVERS`, `SCP1`, `SC1`, `FN1`, `NSTI`, `RDRMAX`, `RDRQOVER`, `QME1` and `QME2` in the source code.
- Changed range check method for model parameter VBFC.
- Bug fixes done for:
  - Range check of `CGSO`, `CGDO`, `CGBO`, `NSUBCDFM`, `SUB2L`, and `SSC4`.
  - Calculation of derivatives
  - Temperature dependence of the output parameter VOH for the threshold voltage
  - NF dependence of RD, RDVD, RD23, and RTH

© 2023 Cadence Design Systems, Inc.

- Calculation of the temperature derivatives
- Temperature dependence of the output parameter Vth
- Calculation of the output parameter Vdsat

Version 2.01 Enhancement

Version 2.01 is a bug fix version of 2.00 and includes the following bug fixes and enhancements:

- Reference voltage (V_{bs} -> V_{bse}) in the Q_{over} model is used when model parameter `CVDSOVER != 0`
- Derivative calculations with respect to temperature
- Derivative calculations in the Q_{over} model code.
- Floating point exception in the QME model code
- Floating point exception in the smoothing functions
- Floating point exception when model parameters `RDVDL << 0` and `RD23L << 0`
- Floating point exception when model flag/parameters `COSUBNODE !=0` , `COSYM=0`, and `NOVER * (NSUBSUB+NOVER) = 0`
- Floating point exception when model flag `CORDRIFT=1` and model parameter `RDRDJUNC = 0`
- Derivative calculations when model parameter `COSUBNODE = 1`

Version 1.23 Enhancement

Version 1.23 is a bug fix version of 1.22, which includes the same bug fixes and enhancement as version 2.01 compared with version 2.00.

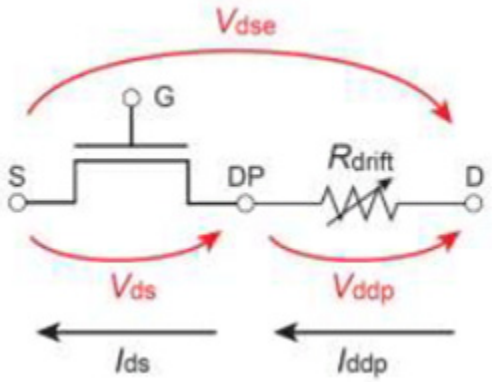
Version 2.00 Enhancement

Based on version 1.22, following enhancements are done in version 2.00:

© 2023 Cadence Design Systems, Inc.

New Rdrift Model

A new Rdrift model has been introduced in version 2.00. A flag `CORDIFT` (default= 1) has been introduced to control the evaluation of R_{drift}. The R_{drift} depends on V_{ddp} as well as the V_g in the new version. The mechanism of R_{drift} is shown as following figure:

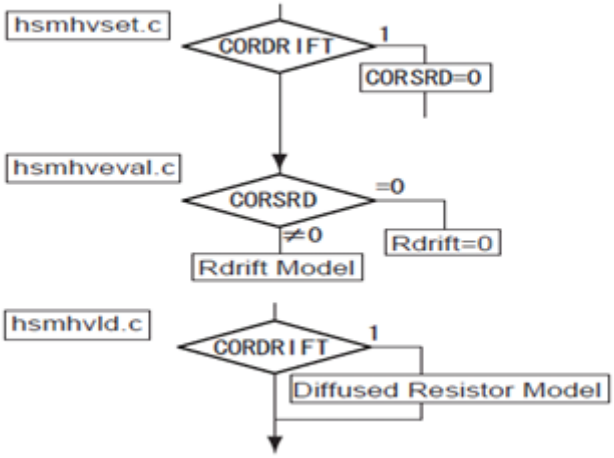


$$I_{ds} = f(V_{ds}, V_{gs}, V_{bs})$$

$$I_{ddp} = f(V_{ddp}) = \frac{V_{ddp}}{R_{drift}}$$

$$R_{drift} = f(V_{ddp}, V_{gse})$$

The usage of the flag is shown in the following figure:



When `CORDIFT=1` (default value), R_{drift} is re-evaluated, otherwise, the old evaluation of R_{drift} is used.

Fitting Improvements

Smoothing of C_{gg} with new model parameter `VGSMIN`.

© 2023 Cadence Design Systems, Inc.

Asymmetrical Diode Model

Introduction of new model parameters for source/drain independently.

Change of Model Descriptions

- Introduction of new impact-ionization description in drift region with new model parameters `XPDV`, `XPVDH`, and `XPVDHG`
- Improvement of the impact-ionization model in channel of core MOSFET with new model parameters `IBPC1L`, `IBPC1LP`, `SUBLDL`, and `SUBLDLP`
- Independent fitting capability for C-V and I-V characteristics by selectively using model parameters `LOVERLD` and `XLDLD`
- Introduction of new punch-through model for core MOSFET
- Improvement of quantum effect model for core MOSFET
- Improvement of gate-poly depletion model for core MOSFET
- Introduction of the channel leakage conductance with new model parameter `DSLEAK`
- Removing of the following model parameters `PGD3`, `PTHROU`, `RD26`, and `QOVSM`
- Resetting of parameter values to within the defined ranges for the following critical model parameters: `VFBC`, `XLDLD`, `SCP22`, and `RDRCX`

Fixed Bugs

Following bugs are fixed in version 2.00:

- Derivative calculation of drain current with respect to the temperature
- Inaccurate capacitance reciprocity when model parameter `CVDSOVER` is not equal to `0`
- Incorrect recognition of the fifth terminal connected to ground (0) when `COSUBNODE=0` is chosen
- Derivative calculation in self-heating model

Version 1.22 Enhancement

Based on version 1.21, following enhancements have been made in version 1.22:

1. The default value of RDSLP1 changed to 1.0

© 2023 Cadence Design Systems, Inc.

2. Qover model is enhanced

Version 1.12 Enhancement

Based on version 1.11, much enhancement is done and some bugs are fixed, thus version 1.12 is presented. The difference from version 1.11 to 1.12 consists of two parts: 1) the bug fix that had been included by version 1.20, refer to session 32.5.5 for the details; 2) the enhancement from version 1.20 to 1.21.

Version 1.21 Enhancement

Based on version 1.20, enhancement is done with the overlap charge and capacitance evaluation, thus latest version 1.21 comes into being to include the change. Following lists the enhancement:

1. Improvements in the lateral-field-induced charge (Qy) model

2. Improvements in the overlap capacitance (Qover) model

New options are provided to calculate Qover. These options are selected by new model parameter COQOVSM:

COQOVSM=0: Qover is calculated with an analytical equation excluding the inversion charge

COQOVSM=1: Qover is calculated with an iterative procedure including the inversion charge (Default)

COQOVSM=2: Qover is calculated with an analytical equation including the inversion charge

Version 1.20 Enhancement

Update information of HiSIM_HV 1.2.0 from HiSIM_HV 1.1.1.

Inclusion of LDMOS-device Structures with a Substrate Node Vsub

HiSIM_HV 1.2.0 additionally covers device structures with a substrate node V_{sub}. The substrate node bias $V_{sub,s}$ increases the depletion width W_{dep} at the drift/substrate (NSUBSUB) junction. The W_{dep} extension into the drift region causes a reduction of the effective drift depth (DDRIFT), and thus an increase of the sheet resistance.

© 2023 Cadence Design Systems, Inc.

Activate 5th and 6th Terminal

With the latest HiSIM_HV 1.20 model, up to 6 terminals are supported.

- If 5 nodes are specified and COSUBNODE=0, the 5th node is thermal node.
- If 5 nodes are specified and COSUBNODE=1, the 5th node is substrate node, if COSELFHEAT=1 is set too, internal thermal node is created.
- If 6 nodes are specified, the 5th node is substrate node and the 6th node is thermal node.

COSUBNODE is a new instance parameter at the same time recognized as a model parameter for the specification and the recognition of the node order.

Model and Instance Parameters Changes

Following new model parameters are added:

- XWDLD: Increase of the effective device width in the drift region due to 2D spreading.
- XWDC: Different effective device width for capacitances.
- NINVDW and NINVDWP: Vds dependence in the low-field-mobility width dependence.
- VMAXT1 and VMAXT2: Temperature dependence of Vmax.
- NINVDT1 and NINVDT2: Temperature dependence in the low-field-mobility Vds dependence.
- RTHTEMP1 and RTHTEMP2: Temperature dependence of the self-heating effect.
- PRATTEMP1 and PRATTEMP1: Temperature dependence of the thermal dissipation.
- COTEMP: The model flag to select different temperature effects of rd, rs, rdvd, rsvd, vmax and ninvd.
- COLDRIFT: The flag to select different Ldrift.
- Following binning option are added for following model parameters: NPEXT FALPH RD RS RD22 RD23 RD24 RDVG11 RDICT1 RDOV13 RDSLP1 RDVB RDVD RTH0 VOVER CGBO CVDSOVER POWRAT
- COSUBNODE: The model and instance flag for substrate node.
- COSELFHEAT: The flag was model parameter with the older version model. New instance flag is added with version 1.20

© 2023 Cadence Design Systems, Inc.

Flag for Temperature Dependent Model Selection

In the HiSIM_HV 1.1.1 versions, temperature dependence of the drift resistance RDVD includes no self-heating effect, whereas RD includes the effect. To treat all temperature dependent models (RD, RDVD, VMAX, NINVD) after users convenience, the flag COTEMP is introduced. Following is the selection of COTEMP:

COTEMP	RD (RS)	RDVD (RSVD)	Vmax	Ninvd
0	T	T0	T0	T0
1	T0	T0	T0	T0
2	T	T	T	T
3	T	T	T0	T0

where T is T0+∂T, and ∂T is the temperature increase due to the self-heating effect.

The Older Version Bug Fix

Following bugs are fixed with the latest 1.20 and the older 1.11 version.

- NF in Diode model
- Ra discontinuity at Vds=0
- Rs temperature dependency
- Smoothing function in overlap capacitance model
- Other minor bugs

Reference

Model Equations

Some important model equations are listed as following for your reference:

© 2023 Cadence Design Systems, Inc.

Charge

All device characteristics are determined on the basis of the charge controlled by applied voltages and by expressing the MOSFET charges as functions of the surface potentials. Under the charge-sheet approximation the charges on the four MOSFET terminals Q_G(gate), Q_B(bulk), Q_D(drain), and Q_S(source), are described for the symmetrical the source/drain contacts as:

$$Q_G = -(Q_B + Q_I)$$
$$Q_B = W_{eff} \int_0^{L_{eff}} Q_b(y)dy$$
$$Q_I = W_{eff} \int_0^{L_{eff}} Q_i(y)dy$$
$$Q_D = W_{eff} \int_0^{L_{eff}} \frac{y}{L_{eff}} Q_i(y)dy$$
$$Q_S = Q_I - Q_D$$

where Q_B and Q_I are the depletion charge and the inversion charge, respectively, and y is the position along the channel. Leff and 0 are the channel-end positions at the drain side and the source side, respectively.

Drain Current

The drift-diffusion theory describes the drain current I_{ds} as:

$$I_{ds} = W_{eff} \cdot NF \cdot q \cdot \mu \cdot n(y) \cdot \left(-\frac{d\phi_s(y)}{dy} + \frac{1}{\beta} \cdot \frac{d \ln n(y)}{dy} \right)$$

where n(y) is the carrier density calculated from the relationship

$$Q_i(y) = q \cdot n(y)$$

© 2023 Cadence Design Systems, Inc.

Under the gradual-channel approximation with further approximations of an idealized gate structure and uniform channel doping, the final equation for I_{ds} is written:

$$I_{ds} = \frac{W_{eff} \cdot NF}{L_{eff}} \cdot \mu \cdot \frac{I_{dd}}{\beta}$$

$$I_{dd} = C_{ox}(\beta V_G' + 1)(\phi_{SL} - \phi_{S0}) - \frac{\beta}{2} C_{ox}\left(\phi_{SL}^2 - \phi_{S0}^2\right)$$
$$- \frac{2}{3} const0\left[\left\{\beta\left(\phi_{SL} - V_{bs}\right) - 1\right\}^{\frac{3}{2}} - \left\{\beta\left(\phi_{S0} - V_{bs}\right) - 1\right\}^{\frac{3}{2}}\right]$$
$$+ const0\left[\left\{\beta\left(\phi_{SL} - V_{bs}\right) - 1\right\}^{\frac{1}{2}} - \left\{\beta\left(\phi_{s0} - V_{bs}\right) - 1\right\}^{\frac{1}{2}}\right]$$

Threshold Voltage Shift

Different from the conventional bsim model, all HiSIM_HV can be determined by oxide thickness Tox and the substrate doping concentration **NSUBC**. The measured V_{th} is influenced by various phenomena such as the short-channel effects, which cause a reduction of V_{th} for short-channel transistors in comparison to long-channel transistors as shown in Figure 31-5. This so-called V_{th} roll-off is dependent on the technology applied for MOSFET fabrication. Therefore, HiSIM can derive many detailed information on the MOSFET fabrication technology, which are relevant for modeling device characteristics, from the V_{th} changes (ΔV_{th}) as a function of gate length (L_{gate}). The modeled V_{th} is incorporated in the ϕS iteration can be viewed as consisting of two main effects or components:

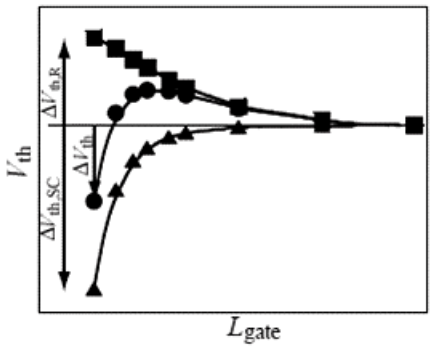
(I) the short-channel effect: $\Delta V_{th, SC}$

(II) the reverse-short-channel effect: $\Delta V_{th, R}$ and $\Delta V_{th, P}$

The separation into these two components ($\Delta V_{th} = \Delta V_{th, SC} + \Delta V_{th, R}$ (or $\Delta V_{th, P}$)) is schematically shown in Figure 31-5.

© 2023 Cadence Design Systems, Inc.

Figure 31-5 Schematic plot of the separation of Vth into the contributions of the short-channel and the reverse short-channel effect.



Mobility Model

The low-field mobility is described with the following expressions and includes the three independent mechanisms of Coulomb, phonon and surface-roughness scattering:

$$\frac{1}{\mu_0} = \frac{1}{\mu_{CB}} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}$$

$$\mu_{CB}(Coulomb) = MUECB0 + MURCB1 \cdot \frac{Q_i}{q \times 10^{11}}$$

$$\mu_{PH}(phonon) = \frac{M_{uephonon}}{E_{eff}^{MUEPH0}}$$

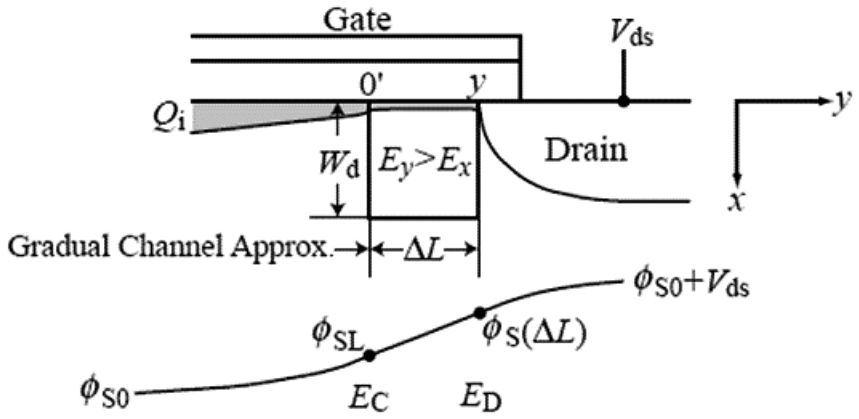
$$\mu_{SR}(surface\ \ roughness) = \frac{MUESR1}{E_{eff}^{Mueserface}}$$

Channel-Length Modulation

As the gradual-channel approximation is not valid for large V_{ds} causing the pinch-off phenomenon in the channel. Without taking into account the pinch-off phenomenon, the calculated channel conductance gds enters abruptly into the saturation condition. To include the pinch-off phenomenon in HiSIM, we apply the conventional method of modeling the pinch-off region (ΔL) separately from the rest of the channel as depicted in Figure 31-6:

© 2023 Cadence Design Systems, Inc.

Figure 31-6 Schematic showing the correlation among physical quantities in the pinch-off region.



After taking into all effects, the final ΔL is derived as:

$$\Delta L = \frac{1}{2}\left[-\frac{1}{L_{eff}}\left(2\frac{I_{dd}}{\beta Q_i} z + 2\frac{N_{sub}}{\varepsilon_{Si}}\left(\phi_S(\Delta L) - \phi_{SL}\right) z^2 + E_0 z^2 \right) \right]$$
$$+ \frac{1}{2}\sqrt{\frac{1}{L_{eff}^2}\left(2\frac{I_{dd}}{\beta Q_i} z - 2\frac{N_{sub}}{\varepsilon_{Si}}(\phi_S(\Delta L) - \phi_{SL}) z^2 \right)^2 + 4\left(2\frac{N_{sub}}{\varepsilon_{Si}}(\phi_s(\Delta L) - \phi_{SL}) z^2 + E_0 z^2 \right)}$$

Narrow-Channel Effects

The shallow-trench-isolation (STI) technology induces a V_{th} reduction for reduced channel width (W_{gate}). This phenomenon is modeled under inclusion of the edge-fringing capacitances C_{ef} at the edge of the trench as:

$$\Delta V_{th,W} = \left(\frac{1}{C_{ox}} - \frac{1}{C_{ox} + 2C_{ef}/(L_{eff} W_{eff})} \right) q N_{sub} W_d + \frac{WVTH0}{W_{gate} \times 10^4}$$

So the total threshold shift becomes:

$$\Delta V_{th} = \Delta V_{th,SC} + \Delta V_{th,R} + \Delta V_{th,P} + \Delta V_{th,W} - \phi_{spg}$$

© 2023 Cadence Design Systems, Inc.

In addition, the mobility should be adjusted with small geometrical size. The shallow trench isolation induces also an undesired hump in the sub-threshold region of the I_{ds}-V_{gs} characteristics.

Temperature Dependences

The temperature dependence is included automatically in the surface potentials through β, which is the inverse of the thermal voltage. Additionally the band gap, the intrinsic carrier concentration, the carrier mobility, and the carrier saturation velocity are also temperature dependent.

$$E_g = EG0 - BGTMP1 \cdot (T - TNOM) - BGTMP2 \cdot (T - TNOM)^2$$

$$\mu_{PH}(phonon) = \frac{M_{uephonon}}{(T/TNOM)^{MUETMP} \times E_{eff}^{MUEPH0}}$$

$$V_{\max} = \frac{VMAX}{1.8 + 0.4(T/TNOM) + 0.1(T/TNOM)^2 - VTMP \times (1 - T/TNOM)}$$

$$E_{gp} = E_{g0} + EGIG + IGTEMP2(1/T - 1/TNOM) + IGTEMP3(1/T^2 - 1/TNOM^2)$$

Resistances

$$R_{d0.temp} = RDTEMP1 \cdot (T - TNOM) + RDTEMP2 \cdot (T - TNOM)^2$$

$$R_{dvd.temp} = RDVDTEMP1 \cdot (TEMP - TNOM) + RDVDTEMP2 \cdot (TEMP^2 - TNOM^2)$$

Junction Capacitance at Drain side

$$CJ = CJ \cdot (1 + TCJBD \cdot (T - TNOM))$$

$$CJSW = CJSW \cdot (1 + TCJBDSW \cdot (T - TNOM))$$

$$CJSWG = CJSWG \cdot (1 + TCJBDSWG \cdot (T - TNOM))$$

© 2023 Cadence Design Systems, Inc.

Junction Capacitance at Drain side

$$CJ = CJ \cdot (1 + TCJBS \cdot (T - TNOM))$$
$$CJSW = CJSW \cdot (1 + TCJBSSW \cdot (T - TNOM))$$
$$CJSWG = CJSWG \cdot (1 + TCJBSSWG \cdot (T - TNOM))$$

Junction Current

$$T_{tnom} = \frac{T}{TNOM}$$
$$j_S = JS0 \exp\left\{\frac{(E_g(T = TNOM) \cdot \beta(T = TNOM) - E_g\beta + XTI \cdot \log(T_{tnom}))}{NJ}\right\}$$
$$j_{SSW} = JS0SW \exp\left\{\frac{(E_g(T = TNOM) \cdot \beta(T = TNOM) - E_g\beta + XTI \cdot \log(T_{tnom}))}{NJSW}\right\}$$
$$j_{S2} = JS0 \exp\left\{\frac{(E_g(T = TNOM) \cdot \beta(T = TNOM) - E_g\beta + XTI2 \cdot \log(T_{tnom}))}{NJ}\right\}$$
$$j_{SSW2} = JS0SW \exp\left\{\frac{(E_g(T = TNOM) \cdot \beta(T = TNOM) - E_g\beta + XTI2 \cdot \log(T_{tnom}))}{NJSW}\right\}$$
$$CISB = CISB \cdot \exp\{(T_{tnom} - 1)CTEMP\}$$
$$VDIFFJ = VDIFFJ \cdot (T_{tnom})^2$$

Resistance

For the symmetrical/asymmetrical HVMOS case, the resistance at the source side is modeled with the same equations for the drain side without the V_{ds} dependence. The source and the drain resistances R_s and R_d are considered by voltage drops on each terminal as

$$V_{gs,eff} = V_{gs} - I_{ds} \cdot R_s$$
$$V_{ds,eff} = V_{ds} - I_{ds} \cdot (R_s + R_{drift})$$
$$V_{bs,eff} = V_{bs} - I_{ds} \cdot R_s$$

© 2023 Cadence Design Systems, Inc.

for the DC condition, where the effective voltages are referred as internal node potentials. The resistance values are modeled as

$$R_s = \frac{RS}{W_{eff}} + NRS \cdot RSH$$

$$R_{drift} = (R_d + V_{ds} \cdot R_{DVD})(1 + RDVG11 - \frac{RDVG11}{RDVG12} \cdot V_{gs}) \cdot (1 - V_{bs} \cdot RDVB)$$

$$R_d = \frac{R_{d0}}{W_{eff}}(1 + \frac{RDS}{(W_{gate} \cdot 10^4 \times L_{gate} \cdot 10^4)^{RDSP}}) + RSH \cdot NRD$$

$$R_{d0} = (RD + R_{d0.temp}) f_1 \cdot f_2$$

$$R_{DVD} = \frac{RDVD + R_{dvd,temp}}{W_{eff}} \cdot \exp(-RDVDL \times (L_{gate} \cdot 10^4)^{RDVDLP}) \cdot \left(1 + \frac{RDVDS}{(W_{gate} \cdot 10^4 \times L_{gate} \cdot 10^4)^{RDVDSP}}\right) \cdot f_1 \cdot f_2 \cdot f_3$$

$$f_1(L_{drift1}) = \frac{LDRIFT1}{1um} \cdot RDSLP1 + RDICT1$$

$$f_2(L_{drift2}) = \frac{LDRIFT2}{1um} \cdot RDSLP2 + RDICT2$$

$$f_3(L_{over}) = 1 + (RDOV11 - \frac{RDOV11}{RDOV12}) \cdot \frac{LOVERLD}{1um} + (1 - RDOV13) \cdot \frac{LOVERLD}{1um}$$

Different resistance effects modeling approaches are supplies by HiSIM_HV model, it can be treated as external resistance or the total current can be obtained by a simple analytical description. Flag **CORSRD** is provided for the selection of one of the possible approaches. In the HiSIM HV 1.1.1 version the resistances is treated only as the extrinsic resistances.

CORSRD=2 is originally introduced to avoid simulation time penalty with an analytical description of the resistance effect as

$$I_{ds} = \frac{I_{ds0}}{1 + I_{ds0} \frac{R_d}{V_{ds}}}$$

© 2023 Cadence Design Systems, Inc.

where I_{ds0} is the drain current without the resistance effect and

$$R_d = \frac{1}{W_{eff}}(R_d^{'} \cdot V_{ds}^{RD21} + V_{bs} \cdot V_{ds}^{RD22D} \cdot RD22)$$

The selection of the resistance model is summarized here:

CORSRD = 0 : no resistance

CORSRD = 1 : solved by circuit simulator with internal nodes

Model parameters are:

RS, NRS, RSH

RDVG11, RDVG12, RDVB, RDS, RDSP, NRD

RD, RDVD, RDVDL, RDVDLP, RDVDS, RDVDSP

RDSLP1, RDICT1, RDSLP2, RDICT2, RDOV11, RDOV12, RDOV13

CORSRD = 2 : solved with the analytical approach

Model parameters are:

RD21, RD22, RD22D, RD23, RD23L, RD23LP

RD23S, RD23SP, RD24, RD25, RD20

CORSRD = 3 : Both **CORSRD** = 1 and **CORSRD** = 2 are considered.

	Structure	**Source**	**Drain**
COSYM=0	LDMOS	RS (bias independent)	RD
COSYM=1	Symmetrical HVMOS		RD
COSYM=1	Asymmetrical HVMOS	RS	RD

© 2023 Cadence Design Systems, Inc.

Capacitance

Intrinsic Capacitance

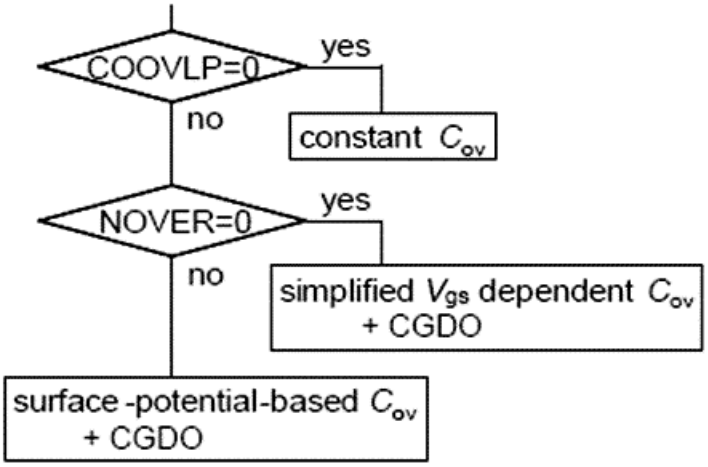
The intrinsic capacitances are derivatives of the node charges determined as

$$C_{jk} = \delta \frac{\partial Q_j}{\partial V_k}$$
$$\delta = -1 \text{ for } j \neq k$$
$$\delta = 1 \text{ for } j = k$$

Overlap Capacitance

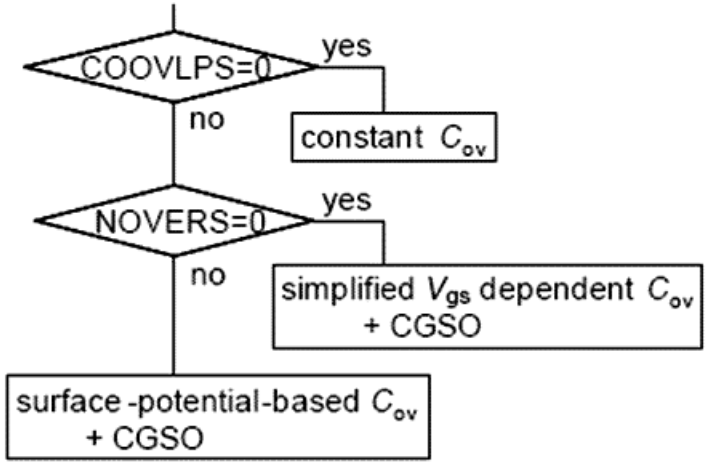
Three different overlap capacitance models are supplied to modeling the overlap capacitance: Constant model, Simplified model and Surface-potential-based model. Flag COOVLP (COOVLPS) and NOVER (NOVERS) are used to select the corresponding model.

Figure 31-7 Model options of the overlap capacitance at the drain side are summarized.



© 2023 Cadence Design Systems, Inc.

Figure 31-8 Model options of the overlap capacitance at the source side are summarized.

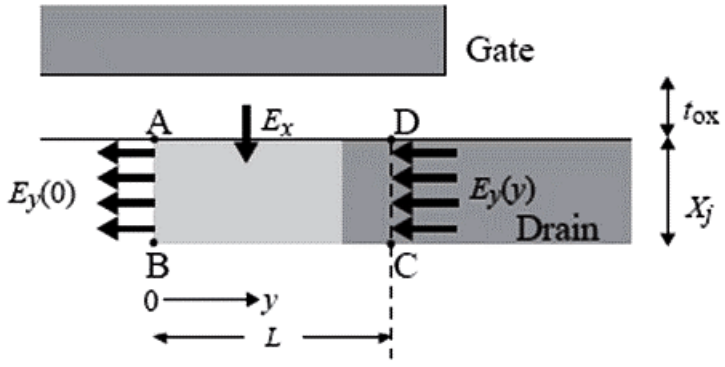


Leakage Currents

Substrate Current

The substrate current Isub is generated by impact ionization in the depletion region at the drain junction

$$I_{\rm sub} = \int_0^{\delta L} I_{\rm ds} C_1 \exp\left(-\frac{C_2}{E_y}\right) dy.$$



where C1 and C2 are fitting parameters.

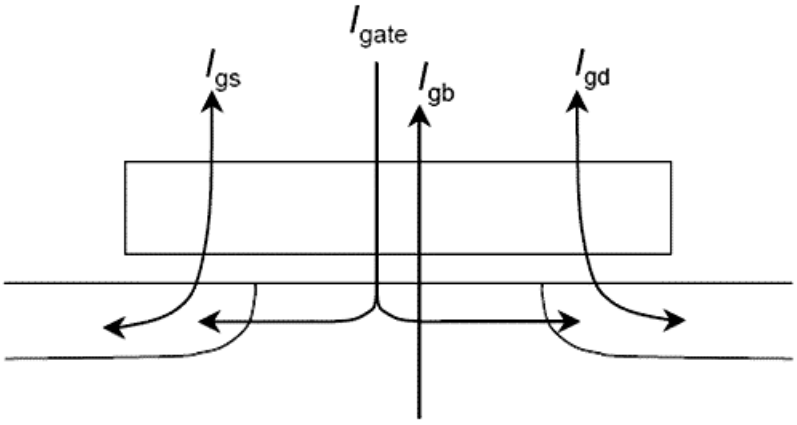
© 2023 Cadence Design Systems, Inc.

Gate Current

All possible gate leakage currents are schematically shown in Fig. 32.8

Between Gate and Channel, I_{gate}

$$I_{gate} = q \cdot GLEAK1 \cdot \frac{E^2}{E_{gp}^{\frac{1}{2}}} \cdot \exp\left(-\frac{E_{gp}^{\frac{3}{2}} \times GLEAK2}{E} \right) \cdot \sqrt{\frac{Q_i}{const0}} \cdot W_{eff} \cdot NF \cdot L_{eff}$$
$$\cdot \frac{GLEAK6}{GLEAK6 + V_{ds}} \cdot \frac{GLEAK7}{GLEAK7 + W_{eff} \cdot NF \cdot L_{eff}}$$



Between Gate and Bulk, I_{gb}

The I_{gb} current under the accumulation condition is modeled as

$$I_{gb} = GLKB1 \cdot E_{gb}^2 \cdot \exp\left(-\frac{GLKB2}{E_{gb}} \right) W_{eff} \cdot NF \cdot L_{eff}$$
$$E_{gb} = -\frac{V_{gs} - VFBC + GLKB3}{T_{ox}}$$

The Fowler-Nordheim tunneling mechanism is also considered

$$I_{FN} = \frac{q \cdot FN1 \cdot E_{FN}^2}{E_{g12}} \cdot \exp\left(-\frac{FN2 \cdot E_{g32}}{E_{FN}} \right) \cdot W_{eff} \cdot NF \cdot L_{eff}$$

© 2023 Cadence Design Systems, Inc.

Total substrate current is the sum of the two components as

$$I_{gb} = I_{gb} + I_{FN}$$

Between Gate and Source/Drain, I_{gs}/I_{gd}

$$I_{gs} = signGIKSD1 \cdot E_{gs}^2 \exp(T_{ox}(GLKSD2 \cdot V_{gs} + GLKSD3)) \cdot W_{eff} \cdot NF$$

$$I_{gd} = signGIKSD1 \cdot E_{gd}^2 \exp(T_{ox}(GLKSD2 \cdot (-V_{gs} + V_{ds}) + GLKSD3)) \cdot W_{eff} \cdot NF$$

GIDL (Gate-Induced Drain Leakage)

$$I_{GIDL} = q \cdot GIDL1 \cdot \frac{E^2}{E_g^{\frac{1}{2}}} \cdot \exp(-GIDL2 \cdot \frac{E_g^{\frac{3}{2}}}{E}) \cdot W_{eff} \cdot NF$$

Source/Bulk and Drain/Bulk Diode Models

Diode Current

$$j_s = JS0$$
$$j_{ssw} = JS0SW$$
$$j_{s2} = JS0$$
$$j_{ssw2} = JS0SW$$

Between Drain and Bulk

$$V_{bd} \geq V_1$$

$$I_{bd} = I_{sbd} \cdot \left\{ \exp\left(\frac{V_1}{N_{vtm}} \right) - 1 \right\} + \frac{I_{sbd}}{N_{vtm}} \exp\left(\frac{V_1}{N_{vtm}} \right) (V_{bd} - V_1)$$
$$+ I_{sbd2} \cdot CISB \cdot \left\{ \exp\left(-\frac{V_{bd} \cdot CVB}{N_{vtm}} \right) - 1 \right\} + CISBK \cdot \left\{ \exp\left(-\frac{V_{bd} \cdot CVB}{N_{vtm}} \right) - 1 \right\}$$

© 2023 Cadence Design Systems, Inc.

$$V_1 \geq V_{bd}$$

$$I_{bd} = I_{sbd} \cdot \left\{ \exp\left(\frac{V_{bd}}{N_{vtm}} \right) - 1 \right\} + I_{sbd2} \cdot CISB \cdot \left\{ \exp\left(-\frac{V_{bd} \cdot CVB}{N_{vtm}} \right) - 1 \right\} + CISBK \cdot \left\{ \exp\left(-\frac{V_{bd} \cdot CVB}{N_{vtm}} \right) - 1 \right\}$$

$$N_{vtm} = \frac{NJ}{\beta}$$

$$V_1 = N_{vtm} \cdot \log\left\{ \frac{VDIFFJ}{I_{sbd}} + 1 \right\}$$

$$I_{bd} = I_{bd} + DIVX \cdot I_{sbd2} \cdot V_{bd}$$

Between Source and Bulk

$$V_{bs} \geq V_2$$

$$I_{bs} = I_{sbs} \cdot \left\{ \exp\left(\frac{V_2}{N_{vtm}} \right) - 1 \right\} + \frac{I_{sbs}}{N_{vtm}} \exp\left(\frac{V_2}{N_{vtm}} \right) (V_{bs} - V_2) + I_{sbs2} \cdot CISB \cdot \left\{ \exp\left(-\frac{V_{bs} \cdot CVB}{N_{vtm}} \right) - 1 \right\} + CISBK \cdot \left\{ \exp\left(-\frac{V_{bs} \cdot CVB}{N_{vtm}} \right) - 1 \right\}$$

$$V_2 \geq V_{bs}$$

$$I_{bs} = I_{sbs} \cdot \left\{ \exp\left(\frac{V_{bs}}{N_{vtm}} \right) - 1 \right\} + I_{sbs2} \cdot CISB \cdot \left\{ \exp\left(-\frac{V_{bs} \cdot CVB}{N_{vtm}} \right) - 1 \right\} + CISBK \cdot \left\{ \exp\left(-\frac{V_{bs} \cdot CVB}{N_{vtm}} \right) - 1 \right\}$$

$$V_2 = N_{vtm} \cdot \log\left\{ \frac{VDIFFJ}{I_{sbs}} + 1 \right\}$$

$$I_{bs} = I_{bs} + DIVX \cdot Isbs2 \cdot V_{bs}$$

© 2023 Cadence Design Systems, Inc.

Noise Models

1/f Noise Models

The 1/f noise is caused by both the carrier fluctuation and the mobility fluctuation. The final description for the drift-diffusion model is

$$S_{I_{ds}} = \frac{I_{ds}^2 NFTRP}{\beta f (L_{eff} - \Delta L) W_{eff} \cdot NF} \left[\frac{1}{(N_0 + N^*)(N_L + N^*)} + \frac{2\mu E_y NFALP}{N_L - N_0} \ln\left(\frac{N_L + N^*}{N_0 + N^*} \right) + (\mu E_y NFALP)^2 \right]$$

where the parameters **NFALP** and **NFTRP** represent the contribution of the mobility fluctuation and the ratio of trap density to attenuation coefficient, respectively.

Thermal Noise Model

Van der Ziel derived the equation for the spectral density of the thermal drain-noise current at temperature T by integrating the trans-conductance along the channel direction y based on the Nyquist theorem

$$S_{id} = 4kT \frac{W_{eff} \cdot NF \cdot C_{ox} \cdot Vg \cdot Vt \cdot \mu}{(L_{eff} - \Delta L)} \frac{(1 + 3\eta + 6\eta^2)\mu_d^2 + (3 + 4\eta + 3\eta^2)\mu_d \mu_s + (6 + 3\eta + \eta^2)\mu_s}{15(1+\eta)\mu_{av}^2}$$

where $?_s$, $?_d$ and $?_{av}$ are mobilities at the source side, the drain side, and averaged, respectively.

Induced Gate Noise Model

$$N_{igate} = S_{igate} / f^2$$

Coupling Noise Model

$$N_{cross} = \frac{S_{igid}}{\sqrt{S_{igate} \cdot S_{id}}}$$

© 2023 Cadence Design Systems, Inc.

Non-Quasi-Static (NQS) Model

Formation of carrier

Carriers in the channel take time to build-up as opposed to the Quasi-Static (QS) approximation. To consider this phenomenon in HiSIM, the carrier formation is modeled as

$$q(t_i) = \frac{q(t_i - 1) + \frac{\Delta t}{\tau} Q(t_i)}{1 + \frac{\Delta t}{\tau}}$$

where $q(t_i)$ and $Q(t_i)$ represent the non-quasi-static and the quasi-static carrier density at time ti, respectively, and $\Delta t = t_i - t_{i-1}$ is valid. Above equation implies that the formation of carriers under the NQS approximation is always delayed in comparison to the QS approximation, which is the basic origin of the NQS effect.

Delay Mechanisms

Weak inversion

$$\tau_{diff} = DLY1$$

Strong inversion

$$\tau_{cond} = DLY2 \cdot \frac{Q_i}{I_{ds}}$$

These two delay mechanisms (diffusion and conduction) are combined using the Matthiessen rule:

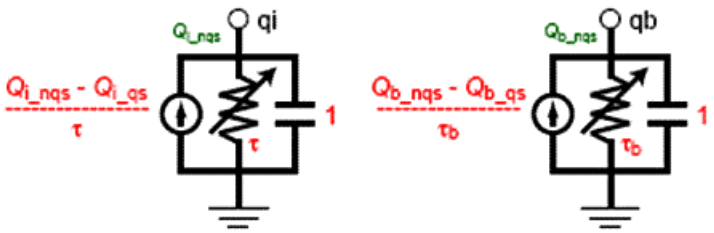
$$\frac{1}{\tau} = \frac{1}{\tau_{diff}} + \frac{1}{\tau_{cond}}$$

Applying the same approach for the formation of bulk carriers, leads to the approximation of the bulk carrier delay as an RC delay in the form

$$\tau_B = DLY3 \cdot C_{ox}$$

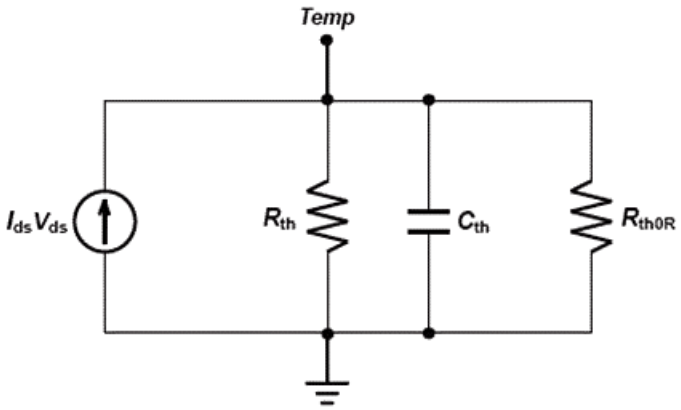
© 2023 Cadence Design Systems, Inc.

NQS model implementation into circuit simulator is listed as following figure:



Self-Heating Effect Model

The self-heating effect is modeled with the thermal network shown in the following figure. The flag COSELFHEAT must be equal to one and RTH0 must not be equal to zero to activate the model.



The total temperature of the devices is the sum of the original temperature and the temperature rise due to self-heating.

$$T = T + R_{th} \cdot I_{ds} \cdot V_{ds}$$

where R_{th} as well as C_{th} are a function of W_{eff} as

$$R_{th} = \frac{RTH0}{W_{eff}} \cdot \left(\frac{1}{NF^{RTHONF}} \right) \left(1 + \frac{RTH0W}{\left(W_{gate} \cdot 10^4 \right)^{RTH0WP}} \right)$$

$$C_{th} = CTH0 \cdot W_{eff}$$

© 2023 Cadence Design Systems, Inc.

HiSIM HV 1.1.1 models the thermal dissipation in a different way with that of previous version as:

$$T = T + R_{th} \cdot I_{ds} \cdot V'_{ds}$$
$$V'_{ds} = V_{dsi} + POWRAT(V_{ds} - V_{dsi})$$

where **POWRAT** is a model parameter. The external node potential is represented by V_{ds} and the internal node potential within the drift region at the channel/drift junction is by V_{dsi}, which is calculated during the simulation.

DFM Model

To support design for manufacturability (DFM) HiSIM introduces an option for considering the variation of device parameters.

$$M_{uephonon} = MUEPH1[MPHDFN\{\ln(NSUBCDFM) - \ln(N_{SUBC})\} + 1]$$
$$NSUBP = NSUBP + (N_{SUBCDFM} - N_{SUBC})$$
$$NEXT = NEXT + (NSUBCDFM - N_{SUBC})$$

Component Statements

Instance Parameters

1	`w (m)`	Gate width.
2	`l (m)`	Gate length.
3	`as` (m^2)	Area of source junction.
4	`ad` (m^2)	Area of drain junction.
5	`ps (m)`	Perimeter of source junction.
6	`pd (m)`	Perimeter of drain junction.
7	`dtemp (C)`	Device temperature rise from ambient.
8	`trise (C)`	Temperature rise from ambient.
9	`nrs=1`	Number of squares of source diffusion.

© 2023 Cadence Design Systems, Inc.

10	`nrd=1`	Number of squares of drain diffusion.
11	`corbnet=0`	Substrate resistance network selector.
12	`rbpb (Ω)`	Substrate resistance network.
13	`rbpd (Ω)`	Substrate resistance network.
14	`rbps (Ω)`	Substrate resistance network.
15	`cosubnode=0`	Instance flag to switch tempnode to subnode. 1: 5th node is subnode; 0: 5th node is thermal node.
16	`coselfheat=0`	Calculation of self-heating model.
17	`corg=0`	Gate-contact resistance selector.
18	`ngcon=1.0`	Number of gate contacts.
19	`xgw=0.0 m`	Distance from gate contact to channel edge.
20	`xgl=0.0 m`	Offset of gate length due to variation in patterning.
21	`nf=1.0`	Number of gate fingers.
22	`lod=1.0e-5 m`	Length of diffusion between gate and STI.
23	`m=1`	Multiplicity factor (number of MOSFETs in parallel).
24	`subld1`	Parameter for impact-ionization current in the drift region.
25	`subld2 ((V^(3/2))/m)`	Parameter for impact-ionization current in the drift region.
26	`ldrift1 (m)`	Parameter for drift region length-1.
27	`ldrift2 (m)`	Parameter for drift region length-2.
28	`lover (m)`	Overlap length on source side.
29	`lovers (m)`	Overlap length on source side.
30	`loverld (m)`	Overlap length on drain side.
31	`ldrift1s (m)`	Parameter for drift region length-1 on source side.
32	`ldrift2s (m)`	Parameter for drift region length-2 on source side.
33	`sa=0.0 m`	Distance from STI edge to Gate edge.
34	`sb=0.0 m`	Distance from STI edge to Gate edge.
35	`sd=0.0 m`	Distance from Gate edge to Gate edge.
36	`nsubcdfm (cm`$^{-3}$`)`	Constant part of Nsub for DFM.

© 2023 Cadence Design Systems, Inc.

37	`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.
38	`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.

Model Definition

```
model modelName hisim_hv parameter=value ...
```

Model Parameters

Device type parameters

1	`type=n`	Transistor type. Possible values are `n` and `p`.
2	`level=73`	Level selector for spice compatible. 73 is valid level for hisim_hv model. The parameter cannot be parameterized, its value must be constant.
3	`version=2.10`	Model parameter "version" only accepts real number value, such as 1.12 for version=1.1.2. The available versions are 1.11(1.1.1)/1.12(1.1.2), 1.20(1.2.0)/1.21(1.2.1)/1.22(1.2.2)/1.23(1.2.3)/1.24(1.2.4), 2.00(2.0.0)/2.01(2.0.1)/2.10(2.1.0)/2.20(2.2.0)/2.30(2.3.0)/2.31(2.3.1)/2.32(2.3.2)/2.33(2.3.3)/2.40(2.4.0)/2.41(2.4.1)/2.50(2.5.0). Version 2.50 is the latest version of HiSIM_HV, and 2.10 is the default version. Version 1.1.1/1.1.2 are no longer maintained. You need to set the value of the 'enable_pre_ver' parameter to 'yes' in the 'options' statement to enable the old versions. The parameter cannot be parameterized, its value must be constant.
4	`corsrd=3`	Contact resistances Rs and Rd selector. 0: no and 1: yes as external resistances. 2: yes, as analytical resistances. 3: yes, as external and analytical resistance.
5	`coiprv=1`	Previous Ids is used for calculating source/drain resistance effect. Possible values are 0: no (default) and 1: yes.

© 2023 Cadence Design Systems, Inc.

6	`copprv=0`	Previous surface potential is used for the initial guess. Possible values are `0: no` and `1: yes`. The default value is `1` for version < 2.3. For other versions, this feature is not supported and it will be always `0: no`.
7	`coadov=1`	Selector for lateral field induced and overlap charges/ capacitances being added to intrinsic ones. Possible values are 0: no and 1: yes (default).
8	`coisub=0`	Substrate current selector. Possible values are 0: no (default) and 1: yes.
9	`cogidl=0`	GIDL current calculation selector. Possible values are 0: no (default) and 1: yes.
10	`coiigs=0`	Gate current calculation selector. Possible values are 0: no (default). 1: yes.
11	`coovlp=1`	Overlap capacitance calculation selector on drain side. Possible values are 0: constant overlap capacitance and 1: including the bias dependent overlap capacitances (default).
12	`coovlps=0`	Overlap capacitance calculation selector on source side. Possible values are 0: constant overlap capacitance (default) and 1: including the bias dependent overlap capacitances.
13	`coflick=0`	1/f noise calculation selector.
14	`coisti=0`	STI leakage current calculation selector. Possible values are 0: no (default) and 1: yes.
15	`conqs=0`	Non-quasi-static mode selector. Possible values are 0: no (default) and 1: yes.
16	`cothrml=0`	Thermal noise calculation selector. Possible values are 0: no (default) and 1: yes.
17	`info`	Debug information flag.
18	`tnom (C)`	Parameters measurement temperature. The default value is set by `options`.
19	`corg=0`	Gate-contact resistance calculation selector. Possible values are 0: no (default) and 1: yes.
20	`corbnet=0`	Substrate resistance network selector.

© 2023 Cadence Design Systems, Inc.

21	`coign=0`	Induced gate and cross correlation noise calculation selector.
22	`compatible`	Compatible with spice3, default is spectre compatible. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, and `sspice`.
23	`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, and `rev`.
24	`codfm=0`	Calculation of model for DFM selector.
25	`coselfheat=0`	Calculation of self heating model.
26	`cosubnode=0`	Flag to switch tempnode to subnode. Possible values are 1: 5th node is subnode and 0: 5th node is thermal node.
27	`cosym=0`	Model selector for symmetry device.
28	`coqovsm=1`	Selector for smoothing method of Qover. Possible values are 0: analytically solved without inversion condition; 1: iteratively solved (default); 2: analytically solved with inversion condition (Old model).
29	`cotemp=0`	Model flag for temperature dependence.
30	`coldrift=0`	Selector for Ldrift parameter.
31	`cordrift=1`	Flag for rdrift evaluation.

Default for instance parameters

32	`w=5e-6 m`	Default gate width.
33	`l=2e-6 m`	Default gate length.
34	`as=0` m^2	Default area of source junction.
35	`ad=0` m^2	Default area of drain junction.
36	`ps=0 m`	Default perimeter of source junction.
37	`pd=0 m`	Default perimeter of drain junction.
38	`temp=27 C`	Default device temperature.
39	`dtemp=0 C`	Default device temperature rise from ambient.
40	`trise (C)`	Alias of dtemp.

© 2023 Cadence Design Systems, Inc.

Basic Device Parameters

41	`tox=3e-8 m`	Physical oxide thickness. The default value is 7e-9 since version 2.00.
42	`xld=3e-8 m`	Gate-overlap length. The default value is 0 for version 2.00/2.01 and 1.23.
43	`xwd=0 m`	Gate-overlap width.
44	`xwdc=0.0 m`	Gate-overlap width, for capacitance.
45	`tpoly=2.0e-7 m`	Height of the gate poly-si for fringing capacitance on source side.
46	`nsubc=1.0e17 cm`$^{-3}$	Substrate-impurity concentration. The default value is 5.0e17 for version 1.23 and 3.0e17 for version 2.00/2.01.
47	`nsubp=1.0e17 cm`$^{-3}$	Maximum pocket concentration. The default value is 1.0e18 for version 2.00/2.01 and version 1.23.
48	`rs=0.0 Ω m`	Source contact resistance in LDD region.
49	`rd=5.0e-3 Ω m`	Drain contact resistance in LDD region. The default value is 0.0 since version 2.00.
50	`vfbc=-1.0 V`	Constant part of flat-band voltage.
51	`lp=0.0 m`	Length of the pocket penetration into the channel. The default value is 1.5e-8 since version 2.00.
52	`xqy=0.0 m`	Distance from channel/drain junction to maximum electric field point.
53	`lover=3.0e-8 m`	Overlap length on source side.
54	`ll=0.0`	Gate length parameter.
55	`lld=0.0 m`	Gate length parameter.
56	`lln=0.0`	Gate length parameter.
57	`wl=0.0`	Gate width parameter.
58	`wld=0.0 m`	Gate width parameter.
59	`wln=0.0`	Gate width parameter.
60	`vbi=1.1 V`	Built-in potential.

© 2023 Cadence Design Systems, Inc.

61	`nsubp0=0.0 cm^-3`	Pocket implant parameter.
62	`nsubwp=1.0`	Pocket implant parameter.
63	`lpext=1.0E-50 m`	Pocket extension.
64	`npext=1.0e17 cm^-3`	Pocket extension. The default value is 5.0e17 starting with version 2.00.
65	`rsh=0.0 V/A m`	Source/drain diffusion sheet resistance.
66	`rshg=0.0 V/A m`	Gate-electrode sheet resistance.
67	`rbpb=50.0 Ω`	Substrate resistance network.
68	`rbpd=50.0 Ω`	Substrate resistance network.
69	`rbps=50.0 Ω`	Substrate resistance network.
70	`gbmin=1.0e-12`	Minimum conductance for substrate resistance network.
71	`xl=0 m`	Gate length offset due to mask/etch effect.
72	`xw=0 m`	Gate width offset due to mask/etch effect.
73	`xqy1=0.0 F m^{XQY2}`	Vbs dependence of Qy.
74	`xqy2=0.0`	Lgate dependence of Qy. The default value is 2.0 since version 2.00.
75	`xldld=1.0e-6 m`	Lateral diffusion of Drain under the gate.
76	`xwdld=1.0e-6 m`	Widening of drift width.
77	`rdov11=0.0`	Dependence coefficient for overlap length.
78	`rdov12=1.0`	Dependence coefficient for overlap length.
79	`rdov13=1.0`	Dependence coefficient for overlap length.
80	`rdslp1=0.0`	LDRIFT1 dependence of resistance for CORSRD=1,3. Default value changed to 1.0 for version 1.22 and later.
81	`rdict1=1.0`	LDRIFT1 dependence of resistance for CORSRD=1,3.
82	`rdslp2=1.0`	LDRIFT2 dependence of resistance for CORSRD=1,3.
83	`rdict2=0.0`	LDRIFT2 dependence of resistance for CORSRD=1,3.
84	`loverld=1.0e-6 m`	Overlap length on the drain side.
85	`lovers=3.0e-8 m`	Overlap length on source side.

© 2023 Cadence Design Systems, Inc.

86	`ldrift1=1.0e-6 m`	Drift region length-1 on the drain side.
87	`ldrift1s=0.0 m`	Drift region length-1 on the source side.
88	`ldrift2=1.0e-6 m`	Drift region length-2 on the drain side.
89	`ldrift2s=1.0e-6 m`	Drift region length-2 on the source side.
90	`subld1=0.0`	Impact-ionization current in the drift region.
91	`subld1l=0.0 μm^subld1lp`	Parameter for impact-ionization current in the drift region.
92	`subld1lp=1.0`	Parameter for impact-ionization current in the drift region.
93	`subld2=0.0 (V^(3/2))/m`	Impact-ionization current in the drift region.
94	`xpdv=0.0 1/m`	Parameter for impact-ionization current in the drift region.
95	`xpvdth=20.0 V`	Parameter for impact-ionization current in the drift region.
96	`xpvdthg (1/V)`	Parameter for impact-ionization current in the drift region.
97	`qovadd=0.0`	Parameter for additional Qover Charge.
98	`rdrbb=1.0`	Degradation of the mobility in drift region.
99	`rdrbbtmp=0 1/K`	Temperature coefficient of RDRBB.

Temperature dependence effects

100	`eg0=1.1785 eV`	Constant bandgap.
101	`bgtmp1=9.025e-5 eV/K`	First order temperature coefficient for band gap.
102	`bgtmp2=1.0e-7 eV/K`^{2}	Second order temperature coefficient for band gap.
103	`igtemp2=0.0 1/K`	Temperature dependence of gate current.
104	`igtemp3=0.0 1/K`^{2}	Temperature dependence of gate current.
105	`vmaxt1=0.0 1/K`	Temperature dependence of velocity.
106	`vmaxt2=0.0 1/K`^{2}	Temperature dependence of velocity.

© 2023 Cadence Design Systems, Inc.

107	`ninvdt1=0.0 1/K`	Temperature dependence of universal mobility model.
108	`ninvdt2=0.0 1/K`^{2}	Temperature dependence of universal mobility model.
109	`rdtemp1=0.0 1/K`	Temperature-dependence of Rd.
110	`rdtemp2=0.0 1/K`^{2}	Temperature-dependence of Rd.
111	`rdvdtemp1=0.0 1/K`	Temperature-dependence of RDVD.
112	`rdvdtemp2=0.0 1/K`^{2}	Temperature-dependence of RDVD.
113	`rthtemp1=0.0 1/K`	Temperature dependence of thermal resistance.
114	`rthtemp2=0.0 1/K`^{2}	Temperature dependence of thermal resistance.
115	`prattemp1=0.0 1/K`	Temperature dependence of thermal dissipation.
116	`prattemp2=0.0 1/K`^{2}	Temperature dependence of thermal dissipation.

Quantum Mechanical Effects

117	`qme1=0.0 m/V`^{2}	Coefficient for quantum mechanical effect.
118	`qme2=1.0 V`	Coefficient for quantum mechanical effect. Default as 0.0 for version 1.23, 2.0 for version 2.10.
119	`qme3=0.0 m`	Coefficient for quantum mechanical effect.
120	`kappa=3.9`	Dielectric constant for high-k stacked gate.

Poly Depletion Effects

121	`pgd1=0.0 V`	Strength of poly depletion.
122	`pgd2=1.0 V`	Threshold voltage of poly depletion.
123	`pgd3=0.8`	Vds dependence of poly depletion.
124	`pgd4=0.0`	Parameter for gate-poly depletion.

© 2023 Cadence Design Systems, Inc.

Short Channel Effects

125	`parl2=1.0e-8 m`	Depletion width of channel/contact junction.
126	`sc1=1.0 1/V`	Short-channel coefficient 1, defaulted as 0 since version 2.10.
127	`sc2=1.0 1/V`^{2}	Short-channel coefficient 2. The default value is 0.0 for version 2.00/2.01 and version 1.23.
128	`sc3=0.0 m/V`^{2}	Short-channel coefficient 3.
129	`sc4=0.0 1/V`	Parameter for SCE.
130	`scp1=1.0 1/V`	Short-channel coefficient 1 for pocket, defaulted as 0.0 since version 2.10.
131	`scp2=0.1 1/V`^{2}	Short-channel coefficient 2 for pocket. The default value is 0.0 for version 2.00/2.01 and version 1.23.
132	`scp3=0.0 m/V`^{2}	Short-channel coefficient 3 for pocket.
133	`scp22=0.0 V`^{4}	Short-channel-effect modification for small Vds.
134	`scp21=0.0 V`	Short-channel-effect modification for small Vds.
135	`bs1=0.0 V`^{2}	Body-coefficient modification by impurity profile.
136	`bs2=0.9 V`	Body-coefficient modification by impurity profile.

Narrow channel effects

137	`wfc=0.0 m F/cm`^{2}	Threshold voltage reduction.
138	`nsubcw=0.0`	Width dependence of substrate-impurity concentration.
139	`nsubcwp=1.0`	Width dependence of substrate-impurity concentration.
140	`nsti=1.0e17 cm`$^{-3}$	Substrate-impurity concentration at the SIT edge, defaulted as 5e17 since version 2.10.
141	`wsti=0.0 m`	Width of the high-field region at STI.
142	`muephw=0.0`	Phonon scattering parameter.
143	`muepwp=1.0`	Phonon scattering parameter.
144	`wvth0=0.0`	Threshold voltage shift.
145	`mueswp=1.0`	Change of surface roughness related mobility.

© 2023 Cadence Design Systems, Inc.

146	`vthsti=0.0`	Parameter for STI.
147	`muesti1=0.0`	STI Stress mobility parameter.
148	`muesti2=0.0`	STI Stress mobility parameter.
149	`muesti3=1.0`	STI Stress mobility parameter.
150	`nsubpsti1=0.0 m`	STI Stress pocket implant parameter.
151	`nsubpsti2=0.0 m`	STI Stress pocket implant parameter.
152	`nsubpsti3=1.0 m`	STI Stress pocket implant parameter.
153	`wstil=0.0`	Parameter for STI.
154	`wstilp=1.0`	Parameter for STI.
155	`scsti1=0.0`	Parameter for STI.
156	`scsti2=0.0 1/V`	Parameter for STI.
157	`saref=1e-6 m`	Reference distance from STI edge to Gate edge.
158	`sbref=1e-6 m`	Reference distance from STI edge to Gate edge.
159	`wstiw=0.0`	Parameter for STI.
160	`wstiwp=1.0`	Parameter for STI.
161	`vdsti=0.0`	Parameter for STI.

Mobility Effects

162	`muecb0=1.0e3` $cm^2/(V\ s)$	Coulomb scattering.
163	`muecb1=1.0e2` $cm^2/(V\ s)$	Coulomb scattering.
164	`mueph0=0.3` cm^2 `(V/cm)^(Muesr1)/(V s)`	Phonon scattering.
165	`mueph1=2.5e4`	Phonon scattering. The default value is 2.0e4 since version 2.00.
166	`muetmp=1.7`	Temperature dependence of phonon scattering. The default value is 1.5 for version 2.00/2.01 and version 1.23.

© 2023 Cadence Design Systems, Inc.

167	`muesr0=2.0 cm^2 (V/cm)^(Muesr1)/(V s)`	Surface-roughness scattering.
168	`muesr1=1.0e16`	Surface-roughness scattering. The default value is 6.0e14 since version 2.00.
169	`ndep=1.0`	Coefficient of effective electric field.
170	`ninv=0.5`	Coefficient of effective electric field.
171	`ninvd=0.0 1/V`	Modification of Vdse dependence on Eeff.
172	`ninvdw=0.0`	Coefficient of modification of Vdse dependence on Eeff.
173	`ninvdwp=1.0`	Coefficient of modification of Vdse dependence on Eeff.
174	`bb=2.0`	High-field mobility degradation.
175	`vmax=1.0e7 cm/s`	Saturation velocity.
176	`vover=0.3 cm^(voverp)`	Parameter for velocity overshoot.
177	`voverp=0.3`	Lgate dependence of velocity overshoot.
178	`vovers=0.0`	Parameter for overshoot.
179	`voversp=0.0`	Parameter for overshoot.
180	`vtmp=0.0 cm/s`	Temperature dependence of the saturation velocity.
181	`muephl=0.0`	Phonon scattering parameter.
182	`mueplp=1.0`	Phonon scattering parameter.
183	`muesrl=0.0`	Surface roughness parameter.
184	`muesrw=0.0`	Change of surface roughness related mobility.
185	`mueslp=1.0`	Surface roughness parameter.
186	`ndepl=0.0`	Modification of Qb contribution for short-channel case.
187	`ndeplp=1.0`	Modification of Qb contribution for short-channel case.

Small size parameters

188	`wl1=0.0`	Threshold voltage shift of STI leakage due to small size effect.

© 2023 Cadence Design Systems, Inc.

189	`wl1p=1.0`	Threshold voltage shift of STI leakage due to small size effect.
190	`wl2=0.0`	Threshold voltage shift due to small size effect.
191	`wl2p=1.0`	Threshold voltage shift due to small size effect.
192	`muephs=0.0`	Mobility modification due to small size.
193	`muepsp=1.0`	Mobility modification due to small size.

Channel Length Modulation Effects

194	`clm1=50e-3`	First parameter for CLM. Default as 0.7 for version 1.23.
195	`clm2=2.0 1/m`	Second parameter for CLM.
196	`clm3=1.0`	Third parameter for CLM.
197	`clm5=1.0`	Effect of pocket implantation.
198	`clm6=0.0`	Effect of pocket implantation.

Substrate Current Effects

199	`sub1=50e-3 1/V`	First parameter for Isub. The default value is 10 for version 2.00/2.01 and version 1.23.
200	`sub2=1.0e2 V`	Second parameter for Isub. The default value is 25 for version 2.00/2.01 and version 1.23.
201	`svgs=0.8`	Substrate current dependence on Vgs.
202	`svbs=0.5`	Substrate current dependence on Vbs.
203	`svbsl=0.0`	Lgate dependence of SVBS.
204	`svds=0.8`	Substrate current dependence on Vds.
205	`slg=3.0e-8`	Substrate current dependence on Lgate.
206	`sub1l=2.5e-3`	Lgate dependence of SUB1.
207	`sub2l=2.0e-6`	Lgate dependence of SUB2.
208	`fn1=50.0`	Coefficient of Fowler-Nordheim-current contribution. The default value is 0.0 since version 2.00.

© 2023 Cadence Design Systems, Inc.

209	`fn2=1.7e-4`	Coefficient of Fowler-Nordheim-current contribution.
210	`fn3=0.0`	Coefficient of Fowler-Nordheim-current contribution.
211	`fvbs=1.2e-2`	Modification of Vbs dependence.
212	`svgsl=0.0`	Lgate dependence of SVGS.
213	`svgslp=1.0`	Lgate dependence of SVGS.
214	`svgswp=1.0`	Wgate dependence of SVGS.
215	`svgsw=0.0`	Wgate dependence of SVGS.
216	`svbslp=1.0`	Lgate dependence of SVBS.
217	`slgl=0.0`	Substrate current dependence on Lgate.
218	`slglp=1.0`	Substrate current dependence on Lgate.
219	`sub1lp=1.0`	Lgate dependence of SUB1.
220	`ibpc1=0.0`	Impact-ionization induced bulk potential change.
221	`ibpc1l=0.0`	Parameter for impact-ionization induced bulk potential change.
222	`ibpc1lp=-1.0`	Parameter for impact-ionization induced bulk potential change.
223	`ibpc2=0.0`	Impact-ionization induced bulk potential change.

Gate Current Effects

224	`glpart1=0.5`	Partitioning of gate current.
225	`gleak1=50.0 A/(V^(3/2) c^(1/2))`	First gate current coefficient.
226	`gleak2=1.0e7 1/(V^(1/2) c^(3/2) m)`	Second gate current coefficient.
227	`gleak3=6.0e-2`	Third gate current coefficient.
228	`gleak4=4.0`	Parameter for gate current.
229	`gleak5=7.5e3`	Parameter for gate current.
230	`glksd1=1.0e-15`	Parameter for gate current.

© 2023 Cadence Design Systems, Inc.

231	`glksd2=5e6`	Parameter for gate current. The default value is 1e3 since version 2.00.
232	`glksd3=-5e6`	Parameter for gate current. The default value is -1e3 since version 2.00.
233	`glkb1=5.0e-16`	Parameter for gate current.
234	`glkb2=1.0`	Parameter for gate current.
235	`gleak6=0.25 V`	Parameter for gate current.
236	`gleak7=1.0e-6` m^2	Parameter for gate current.
237	`glkb3=0.0 V`	Parameter for gate current.
238	`egig=0.0 V`	Parameter for gate current.

GIDL Current Effects

239	`gidl1=2.0 A m/(V^(3/2) c^(1/2))`	First parameter for GIDL.
240	`gidl2=3.0E7 1/(V^(1/2) c^(3/2) m)`	Second parameter for GIDL.
241	`gidl3=0.9`	Third parameter for GIDL.
242	`gidl4=0.9`	Parameter for GIDL. The default value is 0.0 for version 2.00/2.01 and version 1.23.
243	`gidl5=0.2`	Parameter for GIDL.

Noise 1/f Effects

244	`nfalp=1.0e-19`	Flicker (1/f) noise contribution of the mobility fluctuation.
245	`falph=1.0`	Parameter for 1/f noise.
246	`nftrp=1.0e10`	Flicker (1/f) noise ratio of trap density to attenuation coefficient.
247	`cit=0.0`	Flicker (1/f) noise interface trapped carriers capacitance.

© 2023 Cadence Design Systems, Inc.

Subthreshold swing parameters

248	`pthrou=0.0`	Modify subthreshold sloop.

NQS parameters

249	`dly1=1.0e-10`	Parameter for transit time.
250	`dly2=0.7`	Parameter for transit time.
251	`dly3=8.0e-7` Ω	Parameter for transforming bulk charge.
252	`dlyov=0.0` Ω	Parameter for transforming overlap charge.
253	`nqsc`	
254	`minr=1.0e-3`	Minimum parasitic resistance, resistance smaller than minr will be clamped as minr.
255	`minc=1.0e-30`	Minimum diagonal capacitance.
256	`coclampc=1`	The flag of clamp minc.

Symmetry for short-channel mosfet

257	`vzadd0=1.0e-2 V`	Vzadd at Vds=0.
258	`pzadd0=5.0e-3 V`	Pzadd at Vds=0.

P-N junctions parameters

259	`js0=5.0e-7` A/m^2	Junction saturation current density.
260	`js0sw=0.0 A/m`	Side-wall saturation current density.
261	`nj=1.0`	Junction emission coefficient.
262	`njsw=1.0`	Junction emission coefficient (sidewall).
263	`xti=2.0`	Junction saturation current temperature exponent coefficient.
264	`cj=5.0e-4` F/m^2	Bottom junction capacitance per unit area at zero bias.

© 2023 Cadence Design Systems, Inc.

265	`cjsw=5e-10 F/m`	Source/drain sidewall junction capacitance per unit length at zero bias.
266	`cjswg=5e-10 F/m`	Source/drain sidewall junction capacitance grading coefficient per unit length at zero bias.
267	`tcjbd=0.0`	Temperature dependence of czbd.
268	`tcjbdsw=0.0`	Temperature dependence of czbdsw.
269	`tcjbdswg=0.0`	Temperature dependence of czbdswg.
270	`tcjbs=0.0`	Temperature dependence of czbs.
271	`tcjbssw=0.0`	Temperature dependence of czbssw.
272	`tcjbsswg=0.0`	Temperature dependence of czbsswg.
273	`mj=0.5`	Bulk junction bottom grading coefficient.
274	`mjsw=0.33`	Source/drain sidewall junction capacitance grading coefficient.
275	`mjswg=0.33`	Bottom junction capacitance grading coefficient.
276	`pb=1.0 V`	Bottom junction build-in potential.
277	`pbsw=1.0 V`	Source/drain sidewall junction build-in potential.
278	`pbswg=1.0 V`	Source/drain gate sidewall junction build-in potential.
279	`vdiffj=6.0e-4 V`	Threshold voltage for S/D junction diode.
280	`xti2=0.0`	Temperature coefficient.
281	`cisb=0.0`	Reverse bias saturation current.
282	`cvb=0.0`	Bias dependence coefficient of cisb.
283	`ctemp=0.0`	Temperature coefficient.
284	`cisbk=0.0 A`	Reverse bias saturation current.
285	`cvbk=0.0`	Bias dependence coefficient of cisb.
286	`divx=0.0 1/V`	Parameter for junction.

Overlap capacitance parameters

287	`cgso=0.0 F/m`	Gate-source overlap capacitance.
288	`cgdo=0.0 F/m`	Gate-drain overlap capacitance.

© 2023 Cadence Design Systems, Inc.

289	`cgbo=0.0 F/m`	Gate-bulk overlap capacitance.
290	`ovslp=2.0e-8`	Parameter for overlap capacitance. The default value is 2.1e-7 for version 2.00/2.01 and version 1.23.
291	`ovmag=500.0`	Parameter for overlap capacitance. The default value is 0.6 for version 2.00/2.01 and version 1.23.
292	`vfbover=-0.5 V`	Flat-band voltage in overlap region.
293	`nover=3.0e16 cm`$^{-3}$	Impurity concentration in overlap region. The default value is set to 1.0e17 for versions 2.00 and 2.01.
294	`novers=0.0 cm`$^{-3}$	Impurity concentration in overlap region. The default value is set to 1.0e17 since version 2.10.

Smoothing coefficient between linear and saturation

295	`coddlt=1`	Selector for DDLT model, since version 2.20.
296	`ddltmax=1.0`	Coefficient of effective electric field. The default value is 10 for version 2.00/2.01 and 1.23.
297	`ddltslp=0.0`	Lgate dependence of smoothing coefficient.
298	`ddltict=10.0`	Lgate dependence of smoothing coefficient.

DFM parameters

299	`mphdfm=-0.3`	NSUBCDFM dependence of phonon scattering for DFM.

Substrate model parameters

300	`rdvsub=1.0`	Vsub dependence of depletion width.
301	`rdvdsub=0.3`	Vds dependence of depletion width.
302	`ddrift=1.0e-6 m`	Depth of the drift region.
303	`vbisub=0.7 V`	Built-in potential at the drift/substrate junction.
304	`nsubsub=1.0e15 cm`$^{-3}$	

© 2023 Cadence Design Systems, Inc.

		Impurity concentration of the substrate required for Vsub dependence.

Operating region warning control parameters

305	`warn=off`	Parameter to turn warnings on and off. Possible values are `off` and `on`.
306	`bvd (V)`	Drain diode breakdown voltage, take effect when bvj not given.
307	`bvs (V)`	Source diode breakdown voltage, take effect when bvj not given.
308	`bvj (V)`	Junction reverse breakdown voltage.
309	`vbox=3e9 tox V`	Oxide breakdown voltage.

Mismatch parameters

310	`mvtwl=0.0 V m`	Threshold mismatch area dependence.
311	`mvt0=0.0 V`	Threshold mismatch intercept.
312	`mbewl=0.0 m`	Beta mismatch area dependence.
313	`mbe0=0.0`	Beta mismatch intercept.
314	`mvtwl2=0.0 V m^1.5`	Threshold mismatch area square dependence.
315	`mismatchmod=0`	Mismatch mode selector. The available modes are 0, 1, 2 and 3.
316	`mismatchvec1=[...]`	Vector 1 used in mismatch.
317	`mismatchvec2=[...]`	Vector 2 used in mismatch.
318	`mismatchvec3=[...]`	Vector 3 used in mismatch.

© 2023 Cadence Design Systems, Inc.

319	`mismatchvec4=[...]`	Vector 4 used in mismatch.
320	`mismatchdist=0 m`	Mismatch Distance.

LDMOS special parameters

321	`ndepml=0.0`	Lgate dependence of impurity concentration of the surface N^- layer.
322	`ndepmlp=1.0`	Lgate dependence of impurity concentration of the surface N^- layer.
323	`rdvg11=0.0`	Vgs dependence of RD.
324	`rdvg12=1.0e2`	Vgs dependence of RD.
325	`vbsmin=-10.5 V`	Minimum back bias voltage to be treated in hsmhveval.
326	`rth0=0.1 Kcm/W`	Thermal resistance.
327	`cth0=1.0e-7 Ws/Kcm`	Thermal capacitance.
328	`qdftvd=1.0`	Qdrift Vd dependence.
329	`rdvd=7.0e-2`	Vds dependence of RD.
330	`rdvb=0.0`	Vbs dependence of RD.
331	`rd20=0.0`	RD23 boundary.
332	`rd21=1.0`	Vds dependence of RD.
333	`rd22=0.0`	Vbs dependence of RD.
334	`rd22d=0.0`	Vbs dependence of RD.
335	`rd23=5e-3`	Modification of RD.
336	`rd24=0.0`	Vgs dependence of RD.
337	`rd25=0.0`	Vgs dependence of RD.
338	`rd26=0.2`	Smoothing Qover at depletion/inversion transition.
339	`qovsm=0.2`	Smoothing Qover at depletion/inversion transition.
340	`rdvdl=0.0`	Lgate dependence of RD.

© 2023 Cadence Design Systems, Inc.

341	`rdvdlp=1.0`	Lgate dependence of RD.
342	`rdvds=0.0`	Small size dependence of RD.
343	`rdvdsp=1.0`	Small size dependence of RD.
344	`rd23l=0.0`	Lgate dependence of RD23 boundary.
345	`rd23lp=1.0`	Lgate dependence of RD23 boundary.
346	`rd23s=0.0`	Small size dependence of RD23.
347	`rd23sp=1.0`	Small size dependence of RD23.
348	`rds=0.0`	Small size dependence of RD.
349	`rdsp=1.0`	Small size dependence of RD.
350	`ldrift=1.0e-6`	Length of drift region.
351	`rth0r=0.0`	Heat radiation for SHE.
352	`rth0w=0.0`	Width-dependence of RTH0.
353	`rth0wp=1.0`	Width-dependence of RTH0.
354	`rth0nf=0.0`	Nf-dependence of RTH0.
355	`cvdsover=0.0`	Modification of the Cgg spikes for Vds is not zero.
356	`powrat=1.0`	Thermal dissipation.
357	`shemax=500.0 K`	The maximum temperature rise due to the selfheating.
358	`shemaxdlt=0.1 K`	Delta for the SHEMAX smoothing.
359	`vgsmin=-100 V`	Minimal/maximal expected Vgs (NMOS/PMOS).

Auto Model Selector parameters

360	`wmax=1 m`	Maximum channel width for which the model is valid.
361	`wmin=0 m`	Minimum channel width for which the model is valid.
362	`lmax=1 m`	Maximum channel length for which the model is valid.
363	`lmin=0 m`	Minimum channel length for which the model is valid.
364	`ptl=0.0`	Strength for punchthrough effect.
365	`ptp=3.5`	Strength for punchthrough effect.
366	`pt2=0.0`	Vds dependence of punchthrough effect.

© 2023 Cadence Design Systems, Inc.

367	`ptlp=1.0`	Channel-length dependence of punchthrough effect.
368	`gdl=0.0`	Strength of high-field effect.
369	`gdlp=0.0`	Channel-length dependence of high-field effect.
370	`gdld=0.0`	Channel-length dependence of high-field effect.
371	`pt4=0.0`	Vbs dependence of punchthrough effect.
372	`pt4p=1.0`	Vbs dependence of punchthrough effect.
373	`rdrmue=2.0e3`	Field dependent mobility in the drift region for cordrift=1.
374	`rdrvmax=1.0e7`	Saturation velocity in drift region, defaulted as 3e7 since version 2.10.
375	`rdrmuetmp=0.0`	Temperature dependence of resistance for cordrift=1.
376	`rdrvtmp=0.0`	Temperature dependence of resistance for cordrift=1.
377	`rdrdjunc=1.0e-6`	Junction depth at channel/drift region.
378	`rdrcx=0.0`	Exude of current flow from Xov.
379	`rdrcar=0.0`	High field injection in drift region.
380	`rdrdl1=0.0`	Effective ldrift of current in drift region.
381	`rdrdl2=0.0`	Pinch-off length in drift region.
382	`rdrvmaxw=0.0`	Saturation velocity Wgate dependence.
383	`rdrvmaxwp=1.0`	Saturation velocity Wgate dependence.
384	`rdrvmaxl=0.0`	Saturation velocity Lgate dependence.
385	`rdrvmaxlp=1.0`	Saturation velocity Lgate dependence.
386	`rdrmuel=0.0`	Mobility in drift region Lgate dependence.
387	`rdrmuelp=1.0`	Mobility in drift region Lgate dependence.
388	`rdrqover=0.0`	Inclusion of the overlap charge into rdrift. The default value is set to 1.0e5 since version 2.10.
389	`js0d=js0 A/m`^{2}	Saturation current density for drain junction.
390	`js0swd=js0sw A/m`	Side wall saturation current density for drain junction.
39‘	`njd=nj`	Emission coefficient for drain junction.
392	`njswd=njsw`	Emission coefficient for drain junction.
393	`xtid=xti`	Junction current temperature exponent coefficient for drain junction.

© 2023 Cadence Design Systems, Inc.

394	`cjd=cj F/m`^{2}	Bottom junction capacitance per unit area at zero bias for drain junction.
395	`cjswd=cjsw F/m`	Sidewall junction capacitance grading coefficient per unit length at zero bias for drain junction.
396	`cjswgd=cjswg F/m`	Gate sidewall junction capacitance per unit length at zero bias for drain junction.
397	`mjd=mj`	Bottom junction capacitance grading coefficient for drain junction.
398	`mjswd=mjsw`	Sidewall junction capacitance grading coefficient for drain junction.
399	`mjswgd=mjswg`	Gate sidewall junction capacitance grading coefficient for drain junction.
400	`pbd=pb V`	Bottom junction build-in potential for drain junction.
400	`pbswd=pbsw V`	Sidewall junction build-in potential for drain junction.
401	`pbswgd=pbswg V`	Gate sidewall junction build-in potential for drain junction.
402	`xti2d=xti2`	Temperature coefficient for drain junction.
403	`cisbd=cisb`	Reverse bias saturation current for drain junction.
404	`cvbd=cvb`	Bias dependence coefficient of cisb for drain junction.
405	`ctempd=ctemp`	Temperature coefficient for drain junction.
406	`cisbkd=cisbk A`	Reverse bias saturation current for drain junction.
407	`divxd=divx 1/V`	Reverse coefficient for drain junction.
408	`vdiffjd=vdiffj V`	Reverse coefficient for drain junction.
409	`js0s=js0d A/m`^{2}	Saturation current density for source junction.
410	`js0sws=js0swd A/m`	Side wall saturation current density for source junction.
412	`njs=njd`	Emission coefficient for source junction.
413	`njsws=njswd`	Sidewall emission coefficient for source junction.
414	`xtis=xtid`	Junction current temperature exponent coefficient for source junction.
415	`cjs=cjd F/m`^{2}	Bottom junction capacitance per unit area at zero bias for source junction.

© 2023 Cadence Design Systems, Inc.

416	`cjsws=cjswd F/m`	Sidewall junction capacitance grading coefficient per unit length at zero bias for source junction.
417	`cjswgs=cjswgd F/m`	Gate sidewall junction capacitance per unit length at zero bias for source junction.
418	`mjs=mjd`	Bottom junction capacitance grading coefficient for source junction.
419	`mjsws=mjswd`	Sidewall junction capacitance grading coefficient for source junction.
420	`mjswgs=mjswgd`	Gate sidewall junction capacitance grading coefficient for source junction.
421	`pbs=pbd V`	Bottom junction build-in potential for source junction.
422	`pbsws=pbswd V`	Sidewall junction build-in potential for source junction.
423	`pbswgs=pbswgd V`	Gate sidewall junction build-in potential for source junction.
424	`xti2s=xti2d`	Temperature coefficient for source junction.
425	`cisbs=cisbd`	Reverse bias saturation current for source junction.
426	`cvbs=cvbd`	Bias dependence coefficient of cisb for source junction.
427	`ctemps=ctempd`	Temperature coefficient for source junction.
428	`cisbks=cisbkd A`	Reverse bias saturation current for source junction.
429	`divxs=divxd 1/V`	Reverse coefficient for source junction.
430	`vdiffjs=vdiffjd V`	Threshold voltage for junction diode for source junction.

New Depletion Mode Parameters (since version 2.20)

431	`codep=0`	Selector for depletion device.
432	`ndepm=1e17` cm^{-3}	N-layer concentration of the depletion MOS model.
433	`tndep=2e-7 m`	N-layer depth of the depletion MOS model.
434	`depmue0=1e3` $cm^2/(V\ s)$	Coulomb scattering of resistor region.
435	`depmue1=0` $cm^2/(V\ s)$	Coulomb scattering of resistor region.

© 2023 Cadence Design Systems, Inc.

436	`depmueback0=100 cm^2/(V s)`	Coulomb scattering of back region.
437	`depmueback1=0 cm^2/(V s)`	Coulomb scattering of back region.
438	`depleak=0.5`	Leakage current coefficient.
439	`depeta=0 1/V`	Vds dependence.
440	`depvmax=3e7 cm/s`	Velocity saturation.
441	`depvdsef1=2.0 V`	Vds dependence of leakage current.
442	`depvdsef2=0.5`	Vds dependence of leakage current.
443	`depmueph0=0.3`	Phonon scattering.
444	`depmueph1=5e3`	Phonon scattering.
445	`depbb=1`	High field effect coefficient.
446	`depvtmp=0.0`	Temperature dependence of velocity saturation.
447	`depmuetmp=1.5`	Temperature dependence of mobility.
448	`isbreak=1e-12`	Reverse saturation current for breakdown.
449	`rwell=1e3`	Well resistance for breakdown.
450	`mueefb=0 1/V`	Vbs dependence of the phonon scattering.
451	`subtmp=0 1/T`	Temperature dependence of Isub.
452	`rth0l=0.0`	Length dependence of RTH0.
453	`rth0lp=1.0`	Length dependence of RTH0.
454	`tndepv=0.0 1/V`	Vds dependence of TNDEP.
455	`depmue2=1.0e3`	Coulomb scattering of resistor part.
456	`depmuea1=0`	Modification of resistor part mobility.
457	`depddlt=3.0`	Smoothing coefficient for Vds, resistor part.
458	`depvfbc=vfbc V`	Flat bandvoltage of the resistor part.
459	`depsubsl=2.0`	Factor of the sub-threshold slope.
460	`depmue0tmp=0`	Temperature dependence of DEPMUE0.
461	`depmue2tmp=0`	Temperature dependence of DEPMUE2.
462	`depvgpsl=0`	Smoothing coefficient for gm.

© 2023 Cadence Design Systems, Inc.

463	`depvsatr=0`	Vbs dependence of Vds_sat of the resistor part.
464	`qovjunc=0`	Wjunc coefficient for the LoverLD modification.

New Hard BreakDown Voltage Parameters (since version 2.30)

465	`cohbd=0`	Selector for Hard Breakdown Model.
466	`hbda=0`	Coefficient for Hard Breakdown Voltage.
467	`hbdb=0`	Coefficient for Hard Breakdown Voltage.
468	`hbdc=100.0`	Coefficient for Hard Breakdown Voltage.
469	`hbdctmp=0`	Coefficient for Hard Breakdown Voltage.
470	`hbdf=1.0`	Coefficient for Hard Breakdown Voltage.

Binning model parameters

471	`lbinn=1.0`	Length modulation coefficient for binning.
472	`wbinn=1.0`	Width modulation coefficient for binning.
473	`lvmax=0.0 cm/s`	Length dependence of vmax.
474	`lbgtmp1=0.0 eV/K`	Length dependence of bgtmp1.
475	`lbgtmp2=0.0 eV/K`^{2}	Length dependence of bgtmp2.
476	`leg0=0.0 eV`	Length dependence of eg0.
477	`lnovers=0.0 cm`$^{-3}$	Length dependence of novers.
478	`lvfbover=0.0 V`	Length dependence of vfbover.
479	`lnover=0.0 cm`$^{-3}$	Length dependence of nover.
480	`lwl2=0.0`	Length dependence of wl2.
481	`lvfbc=0.0 V`	Length dependence of vfbc.
482	`lnsubc=0.0 cm`$^{-3}$	Length dependence of nsubc.
483	`lnsubp=0.0 cm`$^{-3}$	Length dependence of nsubp.
484	`lscp1=0.0 1/V`	Length dependence of scp1.

© 2023 Cadence Design Systems, Inc.

485	`lscp2=0.0 1/V`^{2}	Length dependence of scp2.
486	`lscp3=0.0 m/V`^{2}	Length dependence of scp3.
487	`lsc1=0.0 1/V`	Length dependence of sc1.
488	`lsc2=0.0 1/V`^{2}	Length dependence of sc2.
489	`lsc3=0.0 m/V`^{2}	Length dependence of sc3.
490	`lpgd1=0.0 V`	Length dependence of pgd1.
491	`lpgd3=0.0`	Length dependence of pgd3.
492	`lndep=0.0`	Length dependence of ndep.
493	`lninv=0.0`	Length dependence of ninv.
494	`lmuecb0=0.0 cm`^{2}`/(V s)`	Length dependence of muecb0.
495	`lmuecb1=0.0 cm`^{2}`/(V s)`	Length dependence of muecb1.
496	`lmueph1=0.0`	Length dependence of mueph1.
497	`lvtmp=0.0 cm/s`	Length dependence of vtmp.
498	`lwvth0=0.0`	Length dependence of wvth0.
499	`lmuesr1=0.0`	Length dependence of muesr1.
500	`lmuetmp=0.0`	Length dependence of muetmp.
501	`lsub1=0.0 1/V`	Length dependence of sub1.
502	`lsub2=0.0 V`	Length dependence of sub2.
503	`lsvds=0.0`	Length dependence of svds.
504	`lsvbs=0.0`	Length dependence of svbs.
505	`lsvgs=0.0`	Length dependence of svgs.
506	`lfn1=0.0`	Length dependence of fn1.
507	`lfn2=0.0`	Length dependence of fn2.
508	`lfn3=0.0`	Length dependence of fn3.
509	`lfvbs=0.0`	Length dependence of fvbs.
510	`lnsti=0.0 cm`$^{-3}$	Length dependence of nsti.
511	`lwsti=0.0 m`	Length dependence of wsti.

© 2023 Cadence Design Systems, Inc.

512	`lscsti1=0.0`	Length dependence of scsti1.
513	`lscsti2=0.0 1/V`	Length dependence of scsti2.
514	`lvthsti=0.0`	Length dependence of vthsti.
515	`lmuesti1=0.0`	Length dependence of muesti1.
516	`lmuesti2=0.0`	Length dependence of muesti2.
517	`lmuesti3=0.0`	Length dependence of muesti3.
518	`lnsubpsti1=0.0 m`	Length dependence of nsubpsti1.
519	`lnsubpsti2=0.0 m`	Length dependence of nsubpsti2.
520	`lnsubpsti3=0.0 m`	Length dependence of nsubpsti3.
521	`lcgso=0.0 F/m`	Length dependence of cgso.
522	`lcgdo=0.0 F/m`	Length dependence of cgdo.
523	`ljs0=0.0 A/m`^{2}	Length dependence of js0.
524	`ljs0sw=0.0 A/m`	Length dependence of js0sw.
525	`lnj=0.0`	Length dependence of nj.
526	`lcisbk=0.0 A`	Length dependence of cisbk.
527	`lclm1=0.0`	Length dependence of clm1.
528	`lclm2=0.0 1/m`	Length dependence of clm2.
529	`lclm3=0.0`	Length dependence of clm3.
530	`lwfc=0.0 m F/cm`^{2}	Length dependence of wfc.
531	`lgidl1=0.0 A m/(V^(3/2) c^(1/2))`	Length dependence of gidl1.
532	`lgidl2=0.0 1/(V^(1/2) c^(3/2) m)`	Length dependence of gidl2.
533	`lgleak1=0.0 A/(V^(3/2) c^(1/2))`	Length dependence of gleak1.
534	`lgleak2=0.0 1/(V^(1/2) c^(3/2) m)`	Length dependence of gleak2.
535	`lgleak3=0.0`	Length dependence of gleak3.
536	`lgleak6=0.0 V`	Length dependence of gleak6.

© 2023 Cadence Design Systems, Inc.

537	`lglksd1=0.0`	Length dependence of glksd1.
538	`lglksd2=0.0`	Length dependence of glksd2.
539	`lglkb1=0.0`	Length dependence of glkb1.
540	`lglkb2=0.0`	Length dependence of glkb2.
541	`lnftrp=0.0`	Length dependence of nftrp.
542	`lnfalp=0.0`	Length dependence of nfalp.
543	`lpthrou=0.0`	Length dependence of pthrou.
544	`lvdiffj=0.0 V`	Length dependence of vdiffj.
545	`libpc1=0.0`	Length dependence of ibpc1.
546	`libpc2=0.0`	Length dependence of ibpc2.
547	`lcgbo=0.0`	Length dependence of cgbo.
548	`lcvdsover=0.0`	Length dependence of cvdsover.
549	`lfalph=0.0`	Length dependence of falph.
550	`lnpext=0.0`	Length dependence of npext.
551	`lpowrat=0.0`	Length dependence of powrat.
552	`lrd=0.0`	Length dependence of rd.
553	`lrd22=0.0`	Length dependence of rd22.
554	`lrd23=0.0`	Length dependence of rd23.
555	`lrd24=0.0`	Length dependence of rd24.
556	`lrdict1=0.0`	Length dependence of rdict1.
557	`lrdov13=0.0`	Length dependence of rdov13.
558	`lrdslp1=0.0`	Length dependence of rdslp1.
559	`lrdvb=0.0`	Length dependence of rdvb.
560	`lrdvd=0.0`	Length dependence of rdvd.
561	`lrdvg11=0.0`	Length dependence of rdvg11.
562	`lrs=0.0`	Length dependence of rs.
563	`lrth0=0.0`	Length dependence of rth0.
564	`lvover=0.0`	Length dependence of vover.
565	`ljs0d=ljs0`	Length dependence of js0d.

© 2023 Cadence Design Systems, Inc.

566	`ljs0swd=ljs0sw`	Length dependence of js0swd.
567	`lnjd=lnj`	Length dependence of njd.
568	`lcisbkd=lcisbk`	Length dependence of cisbkd.
569	`lvdiffjd=lvdiffj`	Length dependence of vdiffjd.
570	`ljs0s=ljs0d`	Length dependence of js0s.
571	`ljs0sws=ljs0swd`	Length dependence of js0sws.
572	`lnjs=lnjd`	Length dependence of njs.
573	`lcisbks=lcisbkd`	Length dependence of cisbks.
574	`lvdiffjs=lvdiffjd`	Length dependence of vdiffjs.
575	`wvmax=0.0 cm/s`	Width dependence of vmax.
576	`wbgtmp1=0.0 eV/K`	Width dependence of bgtmp1.
577	`wbgtmp2=0.0 eV/K`^{2}	Width dependence of bgtmp2.
578	`weg0=0.0 eV`	Width dependence of eg0.
579	`wnovers=0.0 cm`$^{-3}$	Width dependence of novers.
580	`wvfbover=0.0 V`	Width dependence of vfbover.
581	`wnover=0.0 cm`$^{-3}$	Width dependence of nover.
582	`wwl2=0.0`	Width dependence of wl2.
583	`wvfbc=0.0 V`	Width dependence of vfbc.
584	`wnsubc=0.0 cm`$^{-3}$	Width dependence of nsubc.
585	`wnsubp=0.0 cm`$^{-3}$	Width dependence of nsubp.
586	`wscp1=0.0 1/V`	Width dependence of scp1.
587	`wscp2=0.0 1/V`^{2}	Width dependence of scp2.
588	`wscp3=0.0 m/V`^{2}	Width dependence of scp3.
589	`wsc1=0.0 1/V`	Width dependence of sc1.
590	`wsc2=0.0 1/V`^{2}	Width dependence of sc2.
591	`wsc3=0.0 m/V`^{2}	Width dependence of sc3.

© 2023 Cadence Design Systems, Inc.

592	`wpgd1=0.0 V`	Width dependence of pgd1.
593	`wpgd3=0.0`	Width dependence of pgd3.
594	`wndep=0.0`	Width dependence of ndep.
595	`wninv=0.0`	Width dependence of ninv.
596	`wmuecb0=0.0` $cm^2/(V\ s)$	Width dependence of muecb0.
597	`wmuecb1=0.0` $cm^2/(V\ s)$	Width dependence of muecb1.
598	`wmueph1=0.0`	Width dependence of mueph1.
599	`wvtmp=0.0 cm/s`	Width dependence of vtmp.
600	`wwvth0=0.0`	Width dependence of wvth0.
601	`wmuesr1=0.0`	Width dependence of muesr1.
602	`wmuetmp=0.0`	Width dependence of muetmp.
603	`wsub1=0.0 1/V`	Width dependence of sub1.
604	`wsub2=0.0 V`	Width dependence of sub2.
605	`wsvds=0.0`	Width dependence of svds.
606	`wsvbs=0.0`	Width dependence of svbs.
607	`wsvgs=0.0`	Width dependence of svgs.
608	`wfn1=0.0`	Width dependence of fn1.
609	`wfn2=0.0`	Width dependence of fn2.
610	`wfn3=0.0`	Width dependence of fn3.
611	`wfvbs=0.0`	Width dependence of fvbs.
612	`wnsti=0.0` cm^{-3}	Width dependence of nsti.
613	`wwsti=0.0 m`	Width dependence of wsti.
614	`wscsti1=0.0`	Width dependence of scsti1.
615	`wscsti2=0.0 1/V`	Width dependence of scsti2.
616	`wvthsti=0.0`	Width dependence of vthsti.
617	`wmuesti1=0.0`	Width dependence of muesti1.
618	`wmuesti2=0.0`	Width dependence of muesti2.

© 2023 Cadence Design Systems, Inc.

619	`wmuesti3=0.0`	Width dependence of muesti3.
620	`wnsubpsti1=0.0 m`	Width dependence of nsubpsti1.
621	`wnsubpsti2=0.0 m`	Width dependence of nsubpsti2.
622	`wnsubpsti3=0.0 m`	Width dependence of nsubpsti3.
623	`wcgso=0.0 F/m`	Width dependence of cgso.
624	`wcgdo=0.0 F/m`	Width dependence of cgdo.
625	`wjs0=0.0 A/m`^{2}	Width dependence of js0.
626	`wjs0sw=0.0 A/m`	Width dependence of js0sw.
627	`wnj=0.0`	Width dependence of nj.
628	`wcisbk=0.0 A`	Width dependence of cisbk.
629	`wclm1=0.0`	Width dependence of clm1.
630	`wclm2=0.0 1/m`	Width dependence of clm2.
631	`wclm3=0.0`	Width dependence of clm3.
632	`wwfc=0.0 m F/cm`^{2}	Width dependence of wfc.
633	`wgidl1=0.0 A m/(V^(3/2) c^(1/2))`	Width dependence of gidl1.
634	`wgidl2=0.0 1/(V^(1/2) c^(3/2) m)`	Width dependence of gidl2.
635	`wgleak1=0.0 A/(V^(3/2) c^(1/2))`	Width dependence of gleak1.
636	`wgleak2=0.0 1/(V^(1/2) c^(3/2) m)`	Width dependence of gleak2.
637	`wgleak3=0.0`	Width dependence of gleak3.
638	`wgleak6=0.0 V`	Width dependence of gleak6.
639	`wglksd1=0.0`	Width dependence of glksd1.
640	`wglksd2=0.0`	Width dependence of glksd2.
641	`wglkb1=0.0`	Width dependence of glkb1.
642	`wglkb2=0.0`	Width dependence of glkb2.
643	`wnftrp=0.0`	Width dependence of nftrp.

© 2023 Cadence Design Systems, Inc.

644	`wnfalp=0.0`	Width dependence of nfalp.
645	`wpthrou=0.0`	Width dependence of pthrou.
646	`wvdiffj=0.0 V`	Width dependence of vdiffj.
647	`wibpc1=0.0`	Width dependence of ibpc1.
648	`wibpc2=0.0`	Width dependence of ibpc2.
649	`wcgbo=0.0`	Width dependence of cgbo.
650	`wcvdsover=0.0`	Width dependence of cvdsover.
651	`wfalph=0.0`	Width dependence of falph.
652	`wnpext=0.0`	Width dependence of npext.
653	`wpowrat=0.0`	Width dependence of powrat.
654	`wrd=0.0`	Width dependence of rd.
655	`wrd22=0.0`	Width dependence of rd22.
656	`wrd23=0.0`	Width dependence of rd23.
657	`wrd24=0.0`	Width dependence of rd24.
658	`wrdict1=0.0`	Width dependence of rdict1.
659	`wrdov13=0.0`	Width dependence of rdov13.
660	`wrdslp1=0.0`	Width dependence of rdslp1.
661	`wrdvb=0.0`	Width dependence of rdvb.
662	`wrdvd=0.0`	Width dependence of rdvd.
663	`wrdvg11=0.0`	Width dependence of rdvg11.
664	`wrs=0.0`	Width dependence of rs.
665	`wrth0=0.0`	Width dependence of rth0.
666	`wvover=0.0`	Width dependence of vover.
667	`wjs0d=wjs0`	Width dependence of js0d.
668	`wjs0swd`	Width dependence of js0swd.
669	`wnjd`	Width dependence of njd.
670	`wcisbkd`	Width dependence of cisbkd.
671	`wvdiffjd`	Width dependence of vdiffjd.
672	`wjs0s`	Width dependence of js0s.

© 2023 Cadence Design Systems, Inc.

673	`wjs0sws`	Width dependence of js0sws.
674	`wnjs`	Width dependence of njs.
675	`wcisbks`	Width dependence of cisbks.
676	`wvdiffjs`	Width dependence of vdiffjs.
677	`pvmax=0.0 cm/s`	Cross-term dependence of vmax.
678	`pbgtmp1=0.0 eV/K`	Cross-term dependence of bgtmp1.
679	`pbgtmp2=0.0 eV/K`^{2}	Cross-term dependence of bgtmp2.
680	`peg0=0.0 eV`	Cross-term dependence of eg0.
681	`pnovers=0.0 cm`$^{-3}$	Cross-term dependence of novers.
682	`pvfbover=0.0 V`	Cross-term dependence of vfbover.
683	`pnover=0.0 cm`$^{-3}$	Cross-term dependence of nover.
684	`pwl2=0.0`	Cross-term dependence of wl2.
685	`pvfbc=0.0 V`	Cross-term dependence of vfbc.
686	`pnsubc=0.0 cm`$^{-3}$	Cross-term dependence of nsubc.
687	`pnsubp=0.0 cm`$^{-3}$	Cross-term dependence of nsubp.
688	`pscp1=0.0 1/V`	Cross-term dependence of scp1.
689	`pscp2=0.0 1/V`^{2}	Cross-term dependence of scp2.
690	`pscp3=0.0 m/V`^{2}	Cross-term dependence of scp3.
691	`psc1=0.0 1/V`	Cross-term dependence of sc1.
692	`psc2=0.0 1/V`^{2}	Cross-term dependence of sc2.
693	`psc3=0.0 m/V`^{2}	Cross-term dependence of sc3.
694	`ppgd1=0.0 V`	Cross-term dependence of pgd1.
695	`ppgd3=0.0`	Cross-term dependence of pgd3.
696	`pndep=0.0`	Cross-term dependence of ndep.
697	`pninv=0.0`	Cross-term dependence of ninv.
698	`pmuecb0=0.0 cm`^{2}`/(V s)`	Cross-term dependence of muecb0.
699	`pmuecb1=0.0 cm`^{2}`/(V s)`	

© 2023 Cadence Design Systems, Inc.

		Cross-term dependence of muecb1.
700	pmueph1=0.0	Cross-term dependence of mueph1.
701	pvtmp=0.0 cm/s	Cross-term dependence of vtmp.
702	pwvth0=0.0	Cross-term dependence of wvth0.
703	pmuesr1=0.0	Cross-term dependence of muesr1.
704	pmuetmp=0.0	Cross-term dependence of muetmp.
705	psub1=0.0 1/V	Cross-term dependence of sub1.
706	psub2=0.0 V	Cross-term dependence of sub2.
707	psvds=0.0	Cross-term dependence of svds.
708	psvbs=0.0	Cross-term dependence of svbs.
709	psvgs=0.0	Cross-term dependence of svgs.
710	pfn1=0.0	Cross-term dependence of fn1.
711	pfn2=0.0	Cross-term dependence of fn2.
712	pfn3=0.0	Cross-term dependence of fn3.
713	pfvbs=0.0	Cross-term dependence of fvbs.
714	pnsti=0.0 cm^{-3}	Cross-term dependence of nsti.
715	pwsti=0.0 m	Cross-term dependence of wsti.
716	pscsti1=0.0	Cross-term dependence of scsti1.
717	pscsti2=0.0 1/V	Cross-term dependence of scsti2.
718	pvthsti=0.0	Cross-term dependence of vthsti.
719	pmuesti1=0.0	Cross-term dependence of muesti1.
720	pmuesti2=0.0	Cross-term dependence of muesti2.
721	pmuesti3=0.0	Cross-term dependence of muesti3.
722	pnsubpsti1=0.0 m	Cross-term dependence of nsubpsti1.
723	pnsubpsti2=0.0 m	Cross-term dependence of nsubpsti2.
724	pnsubpsti3=0.0 m	Cross-term dependence of nsubpsti3.
725	pcgso=0.0 F/m	Cross-term dependence of cgso.
726	pcgdo=0.0 F/m	Cross-term dependence of cgdo.
727	pjs0=0.0 A/m^2	Cross-term dependence of js0.

© 2023 Cadence Design Systems, Inc.

728	`pjs0sw=0.0 A/m`	Cross-term dependence of js0sw.
729	`pnj=0.0`	Cross-term dependence of nj.
730	`pcisbk=0.0 A`	Cross-term dependence of cisbk.
731	`pclm1=0.0`	Cross-term dependence of clm1.
732	`pclm2=0.0 1/m`	Cross-term dependence of clm2.
733	`pclm3=0.0`	Cross-term dependence of clm3.
734	`pwfc=0.0 m F/cm`^{2}	Cross-term dependence of wfc.
735	`pgidl1=0.0 A m/(V^(3/2) c^(1/2))`	Cross-term dependence of gidl1.
736	`pgidl2=0.0 1/(V^(1/2) c^(3/2) m)`	Cross-term dependence of gidl2.
737	`pgleak1=0.0 A/(V^(3/2) c^(1/2))`	Cross-term dependence of gleak1.
738	`pgleak2=0.0 1/(V^(1/2) c^(3/2) m)`	Cross-term dependence of gleak2.
739	`pgleak3=0.0`	Cross-term dependence of gleak3.
740	`pgleak6=0.0 V`	Cross-term dependence of gleak6.
741	`pglksd1=0.0`	Cross-term dependence of glksd1.
742	`pglksd2=0.0`	Cross-term dependence of glksd2.
743	`pglkb1=0.0`	Cross-term dependence of glkb1.
744	`pglkb2=0.0`	Cross-term dependence of glkb2.
745	`pnftrp=0.0`	Cross-term dependence of nftrp.
746	`pnfalp=0.0`	Cross-term dependence of nfalp.
747	`ppthrou=0.0`	Cross-term dependence of pthrou.
748	`pvdiffj=0.0 V`	Cross-term dependence of vdiffj.
749	`pibpc1=0.0`	Cross-term dependence of ibpc1.
750	`pibpc2=0.0`	Cross-term dependence of ibpc2.
751	`pcgbo=0.0`	Cross-term dependence of cgbo.
752	`pcvdsover=0.0`	Cross-term dependence of cvdsover.

© 2023 Cadence Design Systems, Inc.

753	`pfalph=0.0`	Cross-term dependence of falph.
754	`pnpext=0.0`	Cross-term dependence of npext.
755	`ppowrat=0.0`	Cross-term dependence of powrat.
756	`prd=0.0`	Cross-term dependence of rd.
757	`prd22=0.0`	Cross-term dependence of rd22.
758	`prd23=0.0`	Cross-term dependence of rd23.
759	`prd24=0.0`	Cross-term dependence of rd24.
760	`prdict1=0.0`	Cross-term dependence of rdict1.
761	`prdov13=0.0`	Cross-term dependence of rdov13.
762	`prdslp1=0.0`	Cross-term dependence of rdslp1.
763	`prdvb=0.0`	Cross-term dependence of rdvb.
764	`prdvd=0.0`	Cross-term dependence of rdvd.
765	`prdvg11=0.0`	Cross-term dependence of rdvg11.
766	`prs=0.0`	Cross-term dependence of rs.
767	`prth0=0.0`	Cross-term dependence of rth0.
768	`pvover=0.0`	Cross-term dependence of vover.
769	`pjs0d`	Cross-term dependence of js0d.
770	`pjs0swd`	Cross-term dependence of js0swd.
771	`pnjd`	Cross-term dependence of njd.
772	`pcisbkd`	Cross-term dependence of cisbkd.
773	`pvdiffjd`	Cross-term dependence of vdiffjd.
774	`pjs0s`	Cross-term dependence of js0s.
775	`pjs0sws`	Cross-term dependence of js0sws.
776	`pnjs`	Cross-term dependence of njs.
777	`pcisbks`	Cross-term dependence of cisbks.
778	`pvdiffjs`	Cross-term dependence of vdiffjs.
779	`gdsleak=0.0 S`	Channel leakage conductance.
780	`coerrrep=1`	Selector for error report.

© 2023 Cadence Design Systems, Inc.

Safe Operating Areas Parameters

779	`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
780	`vgd_max=infinity V`	Maximum allowed voltage cross drain and gate.
781	`vgs_max=infinity V`	Maximum allowed voltage cross source/bulk and gate.
782	`vbd_max=infinity V`	Maximum allowed voltage cross drain/source and bulk.
783	`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
784	`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
785	`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
786	`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.
787	`vgbr_max=vgb_max V`	Maximum allowed reverse voltage cross gate and bulk.
788	`vbsr_max=vbs_max V`	Maximum allowed reverse voltage cross bulk and source.
789	`vbdr_max=vbd_max V`	Maximum allowed reverse voltage cross bulk and drain.
790	`vthmod=0`	Vth output selector. `std` outputs model equation Vth. `vthcc` outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter `vthmod`. Possible values are `std` and `vthcc`.
791	`ivth=0.0 A`	Vth current parameter. The default value is taken from the options parameter `ivthn` or `ivthp`, depending on the type of the model.

© 2023 Cadence Design Systems, Inc.

792	`ivthw=0.0 m`	Width offset for constant current Vth. The default value is taken from the options parameter `ivthw`.
793	`ivthl=0.0 m`	Length offset for constant current Vth. The default value is taken from the options parameter `ivthl`.
794	`ivth_vdsmin=0.05 V`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter `ivth_vdsmin`.
795	`ovcap_update=0`	Overlap bug fix special for IFX, default disable, set to 1 enable.

Output Parameters

1	`tempeff (C)`	Effective temperature for a single device.
2	`meff`	Effective multiplicity factor (m-factor).
3	`weff (m)`	Effective channel width.
4	`leff (m)`	Effective channel length.
5	`int_s`	The node index of internal source.
6	`int_d`	The node index of internal drain.

Operating-Point Parameters

1	`temp (C)`	Device temperature.
2	`tk (K)`	Actual device temperature in .
3	`shetemp (C)`	Temperature rise due to self-heating.
4	`dtsh (K)`	Temperature rise due to self-heating.
5	`reversed`	Reverse mode indicator. Possible values are `yes` and `no`.
6	`vdse (V)`	ExtDrain-ExtSource voltage.
7	`vgse (V)`	ExtGate-ExtSource voltage.
8	`vbse (V)`	ExtBulk-ExtSource voltage.

© 2023 Cadence Design Systems, Inc.

9	`ids (A)`	Resistive drain-to-source current.
10	`vds (V)`	Drain-source voltage.
11	`vgs (V)`	Gate-source voltage.
12	`vbs (V)`	Bulk-source voltage.
13	`vgd (V)`	Gate-drain voltage.
14	`vgb (V)`	Gate-bulk voltage.
15	`vdb (V)`	Drain-bulk voltage.
16	`idsres`	Resistor current of Depletion mode MOSFET.
17	`idsacc`	Accumulation current of Depletion mode MOSFET.
18	`vth (V)`	Threshold voltage.
19	`vdsat (V)`	Drain-source saturation voltage.
20	`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, `subth`, and `breakdown`.
21	`gm (S)`	Common-source transconductance.
22	`gds (S)`	Common-source output conductance.
23	`gmbs (S)`	Body-transconductance.
24	`qb (Coul)`	Total bulk charge.
25	`qd (Coul)`	Total drain charge.
26	`qg (Coul)`	Total gate charge.
27	`qs (Coul)`	Total source charge.
28	`qb_itr (Coul)`	Intrinsic bulk charge.
29	`qd_itr (Coul)`	Intrinsic drain charge.
30	`qg_itr (Coul)`	Intrinsic gate charge.
31	`qs_itr (Coul)`	Intrinsic source charge.
32	`qdp (Coul)`	Total external drain charge.
33	`qsp (Coul)`	Total external source charge.
34	`cjd (F)`	Drain-bulk junction capacitance.
35	`cjs (F)`	Source-bulk junction capacitance.
36	`cgg (F)`	Intrinsic dQg_dVg.

© 2023 Cadence Design Systems, Inc.

37	`cgd (F)`	dQg_dVd.
38	`cgs (F)`	dQg_dVs.
39	`cgb (F)`	dQg_dVb.
40	`cdg (F)`	dQd_dVg.
41	`cdd (F)`	Intrinsic dQd_dVd.
42	`cds (F)`	dQd_dVs.
43	`cdb (F)`	dQd_dVb.
44	`csg (F)`	dQs_dVg.
45	`csd (F)`	dQs_dVd.
46	`css (F)`	Intrinsic dQs_dVs.
47	`csb (F)`	dQs_dVb.
48	`cbg (F)`	dQb_dVg.
49	`cbd (F)`	dQb_dVd.
50	`cbs (F)`	dQb_dVs.
51	`cbb (F)`	Intrinsic dQb_dVb.
52	`cdd_tot (F)`	Total dQd_dVd.
53	`cgg_tot (F)`	Total dQg_dVg.
54	`css_tot (F)`	Total dQs_dVs.
55	`cbb_tot (F)`	Total dQb_dVb.
56	`id (A)`	Resistive drain current.
57	`ig (A)`	Gate current.
58	`is (A)`	Resistive source current.
59	`ibulk (A)`	Resistive bulk current.
60	`pwr (W)`	Power at operating point.
61	`ps0 (V)`	Surface potential at source side.
62	`psl (V)`	Surface potential at drain side.
63	`pds (V)`	Delta surface potential between psl and ps0.
64	`isub (A)`	Substrate current Isub.
65	`isubld (A)`	Substrate current IsubLD.

© 2023 Cadence Design Systems, Inc.

66	idsibpc (A)	Impact-Ionization Induced Bulk Potential Change (IBPC).
67	gbds (S)	Substrate trans conductance (dIsub/dVds).
68	gbgs (S)	Substrate trans conductance (dIsub/dVgs).
69	gbbs (S)	Substrate transconductance (dIsub/dVbs).
70	igate (A)	Gate current due to tunneling.
71	igates (A)	Tunneling current from gate to source.
72	igateb (A)	Tunneling current from gate to bulk.
73	igated (A)	Tunneling current from gate to drain.
74	igisl (A)	Gate-induced source leakage current.
75	igidl (A)	Gate-induced drain leakage current.
76	ibs (A)	Source-bulk diode current.
77	ibd (A)	Source-drain diode current.
78	cgso (F)	Gate-source overlap capacitance.
79	cgbo (F)	Gate-bulk overlap capacitance.
80	cgdo (F)	Gate-drain overlap capacitance.
81	rseff (Ω)	Effective source resistance.
82	rdeff (Ω)	Effective drain resistance.
83	rsdrift (Ω)	The resistance of drift region for source side.
84	rdrift (Ω)	The resistance of drift region for drain side.
85	gmt (S)	Temp transconductance.
86	lx4 (A)	Resistive drain-to-source current.
87	lx7 (S)	Common-source transconductance.
88	lx8 (S)	Common-source output conductance.
89	lv9 (V)	Threshold voltage.
90	lx142 (V)	NULL.
91	isub_total (A)	Substrate current Isub.

© 2023 Cadence Design Systems, Inc.

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

ad I-4
ad M-35
alarm M-23
as I-3
as M-34
bb M-174
bgtmp1 M-101
bgtmp2 M-102
bs1 M-135
bs2 M-136
bvd M-306
bvj M-308
bvs M-307
cbb OP-51
cbb_tot OP-55
cbd OP-49
cbg OP-48
lcgso M-519
lcisbk M-524
lcisbkd M-566
lcisbks M-571
lclm1 M-525
lclm2 M-526
lclm3 M-527
lcvdsover M-546
ldrift M-348
ldrift1 I-26
ldrift1 M-86
ldrift1s I-31
ldrift1s M-87
ldrift2 I-27
ldrift2 M-88
ldrift2s I-32
ldrift2s M-89
pclm1 M-729
pclm2 M-730
pclm3 M-731
pcvdsover M-750
pd I-6
pd M-37
pds OP-63
peg0 M-678
pfalph M-751
pfn1 M-708
pfn2 M-709
pfn3 M-710
pfvbs M-711
pgd1 M-121
pgd2 M-122
pgd3 M-123
pgd4 M-124
slg M-205
slgl M-217
slglp M-218
sub1 M-199
sub1l M-206
sub1lp M-219
sub2 M-200
sub2l M-207
subld1 I-24
subld1 M-90
subld1l M-91
subld1lp M-92
subld2 I-25
subld2 M-93
subtmp M-449
svbs M-202
svbsl M-203

© 2023 Cadence Design Systems, Inc.

cbs OP-50
cdb OP-43
cdd OP-41
cdd_tot OP-52
cdg OP-40
cds OP-42
cgb OP-39
cgbo M-289
cgbo OP-79
cgd OP-37
cgdo M-288
cgdo OP-80
cgg OP-36
cgg_tot OP-53
cgs OP-38
cgso M-287
cgso OP-78
cisb M-281
cisbd M-402
cisbk M-284
cisbkd M-405
leff O-4
leg0 M-474
level M-2
lfalph M-547
lfn1 M-504
lfn2 M-505
lfn3 M-506
lfvbs M-507
lgidl1 M-529
lgidl2 M-530
lgleak1 M-531
lgleak2 M-532
lgleak3 M-533
lgleak6 M-534
lglkb1 M-537
lglkb2 M-538
lglksd1 M-535
lglksd2 M-536
libpc1 M-543
libpc2 M-544
ljs0 M-521
pgidl1 M-733
pgidl2 M-734
pgleak1 M-735
pgleak2 M-736
pgleak3 M-737
pgleak6 M-738
pglkb1 M-741
pglkb2 M-742
pglksd1 M-739
pglksd2 M-740
pibpc1 M-747
pibpc2 M-748
pjs0 M-725
pjs0d M-767
pjs0s M-772
pjs0sw M-726
pjs0swd M-768
pjs0sws M-773
pmuecb0 M-696
pmuecb1 M-697
pmueph1 M-698
svbslp M-216
svds M-204
svgs M-201
svgsl M-212
svgslp M-213
svgsw M-215
svgswp M-214
tcjbd M-267
tcjbdsw M-268
tcjbdswg M-269
tcjbs M-270
tcjbssw M-271
tcjbsswg M-272
temp M-38
temp OP-1
tempeff O-1
tk OP-2
tndep M-431
tndepv M-452
tnom M-18
tox M-41

© 2023 Cadence Design Systems, Inc.

cisbks M-426
cisbs M-423
cit M-247
cj M-264
cjd M-392
cjd OP-34
cjs M-413
cjs OP-35
cjsw M-265
cjswd M-393
cjswg M-266
cjswgd M-394
cjswgs M-415
cjsws M-414
clm1 M-194
clm2 M-195
clm3 M-196
clm5 M-197
clm6 M-198
coadov M-7
coclampc M-256
ljs0d M-563
ljs0s M-568
ljs0sw M-522
ljs0swd M-564
ljs0sws M-569
ll M-54
lld M-55
lln M-56
lmax M-360
lmin M-361
lmuecb0 M-492
lmuecb1 M-493
lmueph1 M-494
lmuesr1 M-497
lmuesti1 M-513
lmuesti2 M-514
lmuesti3 M-515
lmuetmp M-498
lndep M-490
lnfalp M-540
lnftrp M-539
pmuesr1 M-701
pmuesti1 M-717
pmuesti2 M-718
pmuesti3 M-719
pmuetmp M-702
pndep M-694
pnfalp M-744
pnftrp M-743
pninv M-695
pnj M-727
pnjd M-769
pnjs M-774
pnover M-681
pnovers M-679
pnpext M-752
pnsti M-712
pnsubc M-684
pnsubp M-685
pnsubpsti1 M-720
pnsubpsti2 M-721
pnsubpsti3 M-722
tpoly M-45
trise I-8
trise M-40
type M-1
vbd_max M-782
vbdr_max M-789
vbi M-60
vbisub M-303
vbox M-309
vbs OP-12
vbs_max M-783
vbse OP-8
vbsmin M-323
vbsr_max M-788
vdb OP-15
vdiffj M-279
vdiffjd M-407
vdiffjs M-428
vds OP-10
vds_max M-779
vdsat OP-19

© 2023 Cadence Design Systems, Inc.

coddlt M-295
codep M-429
codfm M-24
coerrrep M-778
coflick M-13
cogidl M-9
cohbd M-463
coign M-21
coiigs M-10
coiprv M-5
coisti M-14
coisub M-8
coldrift M-30
compatible M-22
conqs M-15
coovlp M-11
coovlps M-12
copprv M-6
coqovsm M-28
corbnet I-11
corbnet M-20
lninv M-491
lnj M-523
lnjd M-565
lnjs M-570
lnover M-477
lnovers M-475
lnpext M-548
lnsti M-508
lnsubc M-480
lnsubp M-481
lnsubpsti1 M-516
lnsubpsti2 M-517
lnsubpsti3 M-518
lod I-22
lover I-28
lover M-53
loverld I-30
loverld M-84
lovers I-29
lovers M-85
lp M-51
powrat M-354
ppgd1 M-692
ppgd3 M-693
ppowrat M-753
ppthrou M-745
prattemp1 M-115
prattemp2 M-116
prd M-754
prd22 M-755
prd23 M-756
prd24 M-757
prdict1 M-758
prdov13 M-759
prdslp1 M-760
prdvb M-761
prdvd M-762
prdvg11 M-763
prs M-764
prth0 M-765
ps I-5
ps M-36
vdse OP-6
vdsti M-161
version M-3
vfbc M-50
vfbover M-292
vgb OP-14
vgb_max M-784
vgbr_max M-787
vgd OP-13
vgd_max M-780
vgdr_max M-785
vgs OP-11
vgs_max M-781
vgse OP-7
vgsmin M-357
vgsr_max M-786
vmax M-175
vmaxt1 M-105
vmaxt2 M-106
vover M-176
voverp M-177

© 2023 Cadence Design Systems, Inc.

cordrift M-31
corg I-17
corg M-19
corsrd M-4
coselfheat I-16
coselfheat M-25
cosubnode I-15
cosubnode M-26
cosym M-27
cotemp M-29
cothrml M-16
csb OP-47
csd OP-45
csg OP-44
css OP-46
css_tot OP-54
ctemp M-283
ctempd M-404
ctemps M-425
cth0 M-325
cvb M-282
lpext M-63
lpgd1 M-488
lpgd3 M-489
lpowrat M-549
lpthrou M-541
lrd M-550
lrd22 M-551
lrd23 M-552
lrd24 M-553
lrdict1 M-554
lrdov13 M-555
lrdslp1 M-556
lrdvb M-557
lrdvd M-558
lrdvg11 M-559
lrs M-560
lrth0 M-561
lsc1 M-485
lsc2 M-486
lsc3 M-487
lscp1 M-482
ps0 OP-61
psc1 M-689
psc2 M-690
psc3 M-691
pscp1 M-686
pscp2 M-687
pscp3 M-688
pscsti1 M-714
pscsti2 M-715
psl OP-62
psub1 M-703
psub2 M-704
psvbs M-706
psvds M-705
psvgs M-707
pt2 M-364
pt4 M-369
pt4p M-370
pthrou M-248
ptl M-362
ptlp M-365
vovers M-178
voversp M-179
vth OP-18
vthmod M-790
vthsti M-146
vtmp M-180
vzadd0 M-257
w I-1
w M-32
warn M-305
wbgtmp1 M-574
wbgtmp2 M-575
wbinn M-470
wcgbo M-647
wcgdo M-622
wcgso M-621
wcisbk M-626
wcisbkd M-668
wcisbks M-673
wclm1 M-627
wclm2 M-628

© 2023 Cadence Design Systems, Inc.

cvbd M-403
cvbk M-285
cvbs M-424
cvdsover M-353
ddltict M-298
ddltmax M-296
ddltslp M-297
ddrift M-302
depbb M-443
depddlt M-455
depeta M-437
depleak M-436
depmue0 M-432
depmue0tmp M-458
depmue1 M-433
depmue2 M-453
depmue2tmp M-459
depmuea1 M-454
depmueback0 M-434
depmueback1 M-435
lscp2 M-483
lscp3 M-484
lscsti1 M-510
lscsti2 M-511
lsub1 M-499
lsub2 M-500
lsvbs M-502
lsvds M-501
lsvgs M-503
lv9 OP-89
lvdiffj M-542
lvdiffjd M-567
lvdiffjs M-572
lvfbc M-479
lvfbover M-476
lvmax M-471
lvover M-562
lvthsti M-512
lvtmp M-495
lwfc M-528
ptp M-363
pvdiffj M-746
pvdiffjd M-771
pvdiffjs M-776
pvfbc M-683
pvfbover M-680
pvmax M-675
pvover M-766
pvthsti M-716
pvtmp M-699
pwfc M-732
pwl2 M-682
pwr OP-60
pwsti M-713
pwvth0 M-700
pzadd0 M-258
qb OP-24
qb_itr OP-28
qd OP-25
qd_itr OP-29
wclm3 M-629
wcvdsover M-648
weff O-3
weg0 M-576
wfalph M-649
wfc M-137
wfn1 M-606
wfn2 M-607
wfn3 M-608
wfvbs M-609
wgidl1 M-631
wgidl2 M-632
wgleak1 M-633
wgleak2 M-634
wgleak3 M-635
wgleak6 M-636
wglkb1 M-639
wglkb2 M-640
wglksd1 M-637
wglksd2 M-638

© 2023 Cadence Design Systems, Inc.

depmueph0 M-441
depmueph1 M-442
depmuetmp M-445
depsubsl M-457
depvdsef1 M-439
depvdsef2 M-440
depvfbc M-456
depvgpsl M-460
depvmax M-438
depvsatr M-461
depvtmp M-444
divx M-286
divxd M-406
divxs M-427
dly1 M-249
dly2 M-250
dly3 M-251
dlyov M-252
dtemp I-7
lwl2 M-478
lwsti M-509
lwvth0 M-496
lx142 OP-90
lx4 OP-86
lx7 OP-87
lx8 OP-88
m I-23
mbe0 M-313
mbewl M-312
meff O-2
minc M-255
minr M-254
mismatchdist M-320
mismatchmod M-315
mismatchvec1 M-316
mismatchvec2 M-317
mismatchvec3 M-318
mismatchvec4 M-319
qdftvd M-326
qdp OP-32
qg OP-26
qg_itr OP-30
qme1 M-117
qme2 M-118
qme3 M-119
qovadd M-97
qovjunc M-462
qovsm M-337
qs OP-27
qs_itr OP-31
qsp OP-33
rbpb I-12
rbpb M-67
rbpd I-13
rbpd M-68
rbps I-14
rbps M-69
wibpc1 M-645
wibpc2 M-646
wjs0 M-623
wjs0d M-665
wjs0s M-670
wjs0sw M-624
wjs0swd M-666
wjs0sws M-671
wl M-57
wl1 M-188
wl1p M-189
wl2 M-190
wl2p M-191
wld M-58
wln M-59
wmax M-358
wmin M-359
wmuecb0 M-594
wmuecb1 M-595

© 2023 Cadence Design Systems, Inc.

dtemp M-39
dtsh OP-4
eg0 M-100
egig M-238
falph M-245
fn1 M-208
fn2 M-209
fn3 M-210
fvbs M-211
gbbs OP-69
gbds OP-67
gbgs OP-68
gbmin M-70
gdl M-366
gdld M-368
gdlp M-367
gds OP-22
gdsleak M-777
gidl1 M-239
gidl2 M-240
gidl3 M-241
mj M-273
mjd M-395
mjs M-416
mjsw M-274
mjswd M-396
mjswg M-275
mjswgd M-397
mjswgs M-418
mjsws M-417
mphdfm M-299
muecb0 M-162
muecb1 M-163
mueefb M-448
mueph0 M-164
mueph1 M-165
muephl M-181
muephs M-192
muephw M-142
mueplp M-182
muepsp M-193
muepwp M-143
rd M-49
rd20 M-329
rd21 M-330
rd22 M-331
rd22d M-332
rd23 M-333
rd23l M-342
rd23lp M-343
rd23s M-344
rd23sp M-345
rd24 M-334
rd25 M-335
rd26 M-336
rdeff OP-82
rdict1 M-81
rdict2 M-83
rdov11 M-77
rdov12 M-78
rdov13 M-79
rdrbb M-98
rdrbbtmp M-99
wmueph1 M-596
wmuesr1 M-599
wmuesti1 M-615
wmuesti2 M-616
wmuesti3 M-617
wmuetmp M-600
wndep M-592
wnfalp M-642
wnftrp M-641
wninv M-593
wnj M-625
wnjd M-667
wnjs M-672
wnover M-579
wnovers M-577
wnpext M-650
wnsti M-610
wnsubc M-582
wnsubp M-583
wnsubpsti1 M-618
wnsubpsti2 M-619

© 2023 Cadence Design Systems, Inc.

gidl4 M-242
gidl5 M-243
gleak1 M-225
gleak2 M-226
gleak3 M-227
gleak4 M-228
gleak5 M-229
gleak6 M-235
gleak7 M-236
glkb1 M-233
glkb2 M-234
glkb3 M-237
glksd1 M-230
glksd2 M-231
glksd3 M-232
glpart1 M-224
gm OP-21
gmbs OP-23
gmt OP-85
hbda M-464
hbdb M-465
mueslp M-185
muesr0 M-167
muesr1 M-168
muesrl M-183
muesrw M-184
muesti1 M-147
muesti2 M-148
muesti3 M-149
mueswp M-145
muetmp M-166
mvt0 M-311
mvtwl M-310
mvtwl2 M-314
ndep M-169
ndepl M-186
ndeplp M-187
ndepm M-430
nf I-21
nfalp M-244
nftrp M-246
ngcon I-18
rdrcar M-377
rdrcx M-376
rdrdjunc M-375
rdrdl1 M-378
rdrdl2 M-379
rdrift OP-84
rdrmue M-371
rdrmuel M-384
rdrmuelp M-385
rdrmuetmp M-373
rdrqover M-386
rdrvmax M-372
rdrvmaxl M-382
rdrvmaxlp M-383
rdrvmaxw M-380
rdrvmaxwp M-381
rdrvtmp M-374
rds M-346
rdslp1 M-80
rdslp2 M-82
rdsp M-347
wnsubpsti3 M-620
wpgd1 M-590
wpgd3 M-591
wpowrat M-651
wpthrou M-643
wrd M-652
wrd22 M-653
wrd23 M-654
wrd24 M-655
wrdict1 M-656
wrdov13 M-657
wrdslp1 M-658
wrdvb M-659
wrdvd M-660
wrdvg11 M-661
wrs M-662
wrth0 M-663
wsc1 M-587
wsc2 M-588
wsc3 M-589
wscp1 M-584

© 2023 Cadence Design Systems, Inc.

hbdc M-466
hbdctmp M-467
hbdf M-468
ibd OP-77
ibpc1 M-220
ibpc1l M-221
ibpc1lp M-222
ibpc2 M-223
ibs OP-76
ibulk OP-59
id OP-56
ids OP-9
idsacc OP-17
idsibpc OP-66
idsres OP-16
ig OP-57
igate OP-70
igateb OP-72
igated OP-73
igates OP-71
igidl OP-75
ninv M-170
ninvd M-171
ninvdt1 M-107
ninvdt2 M-108
ninvdw M-172
ninvdwp M-173
nj M-261
njd M-389
njs M-410
njsw M-262
njswd M-390
njsws M-411
nover M-293
novers M-294
npext M-64
nqsc M-253
nrd I-10
nrs I-9
nsti M-140
nsubc M-46
nsubcdfm I-36
rdtemp1 M-109
rdtemp2 M-110
rdvb M-328
rdvd M-327
rdvdl M-338
rdvdlp M-339
rdvds M-340
rdvdsp M-341
rdvdsub M-301
rdvdtemp1 M-111
rdvdtemp2 M-112
rdvg11 M-321
rdvg12 M-322
rdvsub M-300
region I-38
region OP-20
reversed OP-5
rs M-48
rsdrift OP-83
rseff OP-81
rsh M-65
wscp2 M-585
wscp3 M-586
wscsti1 M-612
wscsti2 M-613
wsti M-141
wstil M-153
wstilp M-154
wstiw M-159
wstiwp M-160
wsub1 M-601
wsub2 M-602
wsvbs M-604
wsvds M-603
wsvgs M-605
wvdiffj M-644
wvdiffjd M-669
wvdiffjs M-674
wvfbc M-581
wvfbover M-578
wvmax M-573
wvover M-664

© 2023 Cadence Design Systems, Inc.

igisl OP-74
igtemp2 M-103
igtemp3 M-104
info M-17
int_d O-6
int_s O-5
is OP-58
isbreak M-446
isnoisy I-37
isub OP-64
isub_total OP-91
isubld OP-65
ivth M-791
ivth_vdsmin M-794
ivthl M-793
ivthw M-792
js0 M-259
js0d M-387
js0s M-408
js0sw M-260
nsubcw M-138
nsubcwp M-139
nsubp M-47
nsubp0 M-61
nsubpsti1 M-150
nsubpsti2 M-151
nsubpsti3 M-152
nsubsub M-304
nsubwp M-62
ovcap_update M-795
ovmag M-291
ovslp M-290
parl2 M-125
pb M-276
pbd M-398
pbgtmp1 M-676
pbgtmp2 M-677
pbs M-419
pbsw M-277
pbswd M-399
rshg M-66
rth0 M-324
rth0l M-450
rth0lp M-451
rth0nf M-352
rth0r M-349
rth0w M-350
rth0wp M-351
rthtemp1 M-113
rthtemp2 M-114
rwell M-447
sa I-33
saref M-157
sb I-34
sbref M-158
sc1 M-126
sc2 M-127
sc3 M-128
sc4 M-129
scp1 M-130
wvth0 M-144
wvthsti M-614
wvtmp M-597
wwfc M-630
wwl2 M-580
wwsti M-611
wwvth0 M-598
xgl I-20
xgw I-19
xl M-71
xld M-42
xldld M-75
xpdv M-94
xpvdth M-95
xpvdthg M-96
xqy M-52
xqy1 M-73
xqy2 M-74
xti M-263
xti2 M-280

© 2023 Cadence Design Systems, Inc.

js0swd M-388
js0sws M-409
kappa M-120
l I-2
l M-33
lbgtmp1 M-472
lbgtmp2 M-473
lbinn M-469
lcgbo M-545
lcgdo M-520
pbswg M-278
pbswgd M-400
pbswgs M-421
pbsws M-420
pcgbo M-749
pcgdo M-724
pcgso M-723
pcisbk M-728
pcisbkd M-770
pcisbks M-775
scp2 M-131
scp21 M-134
scp22 M-133
scp3 M-132
scsti1 M-155
scsti2 M-156
sd I-35
shemax M-355
shemaxdlt M-356
shetemp OP-3
xti2d M-401
xti2s M-422
xtid M-391
xtis M-412
xw M-72
xwd M-43
xwdc M-44
xwdld M-76

© 2023 Cadence Design Systems, Inc.

32

HISIM_SOI Model (hisimsoi)

nHiSIM SOI is valid for all possible SOI-MOSFET structures causing different electrical conditions.

nThis chapter contains the following information about the HiSIM_SOI model:

? Model Concepts on page 2532

? For any questions, contact Cadence Customer Support. on page 2535

? Version Update and Enhancements on page 2535

  ? Version 1.50 Enhancements on page 2535

  ? Version 1.40 Enhancements on page 2536

  ? Version 1.30 Enhancements on page 2536

? Reference on page 2537

  ? Model Equations on page 2537

  ? Component Statements on page 2553

© 2023 Cadence Design Systems, Inc.

Model Concepts

nThe definition of the node potentials are:

n$V_{s:}$ reference

nV_{gs}: gate to source

nV_{ds}: drain to source

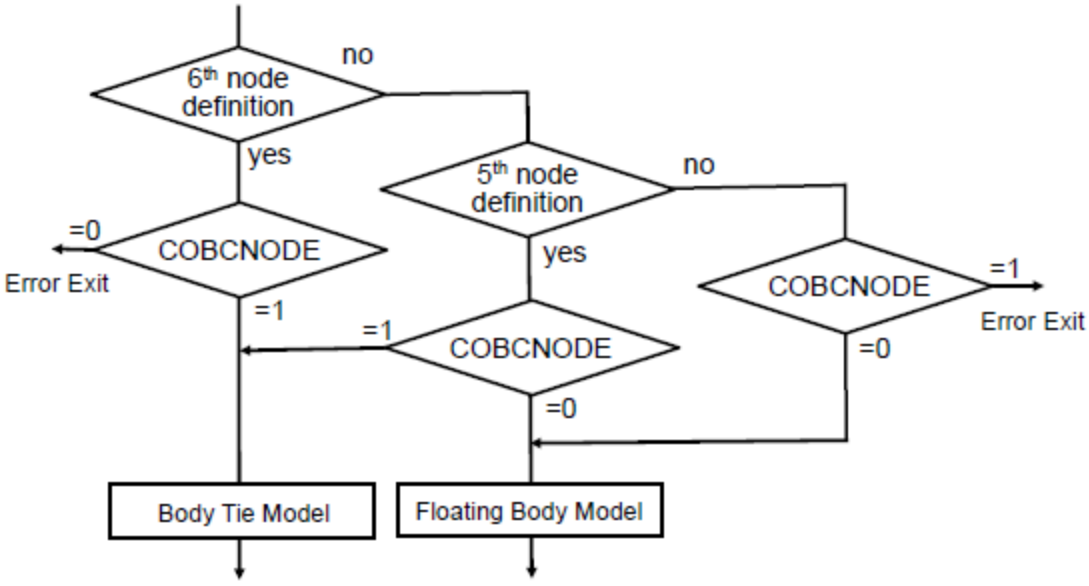
nV_{es}: substrate contact to source

nV_{bcs}: body contact to source

nThe internal node potential is denoted by V_{bs}, which is equal to ϕ_{bSOI} for the floating body and to V_{bcs} for the body tie.

nThe divergence of model branches are summarized are shown in the figure below

Figure 32-1 Model Branches Considered in HiSIM_SOI

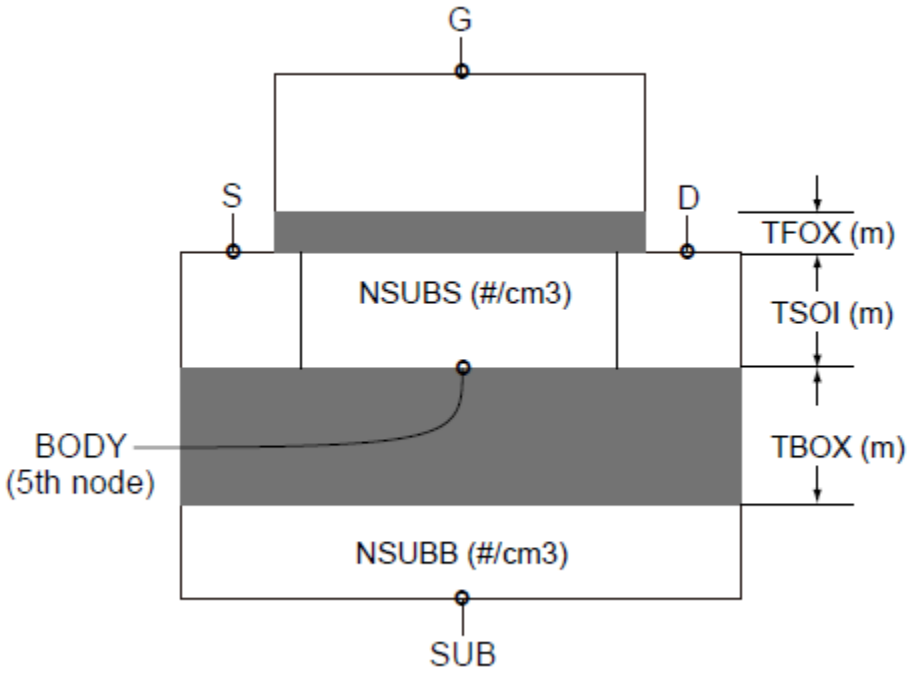


nThe dynamical-depletion condition during switching is also automatically done within the model framework. The impurity concentration difference between the SOI layer NSUBS and the substrate NSUBB determines the built-in potential difference, which is also considered.

© 2023 Cadence Design Systems, Inc.

Figure 32-2 Definitions of device parameters in HiSIM SOI.

n



nThe y-axis is defined along the direction of current flow (source is y=0) and x is defined downwards into the channel (front gate MOS interface is x=0).

nIf TBOX is so thin that the inversion condition occurs even on the backside at BOX, HiSIM SOTB is recommended to apply. HiSIM SOI solves the Poisson equation iteratively from the surface to the bulk substrate [1–3]. The surface potential value, the solution of the Poisson equation, determines the device condition either fully depleted (FD) or partially depleted (PD).

Model Usage

nDetermination of the node sequence is:

nDrain = 1, Gate = 2, Source = 3, Substrate = 4

nIf COBCNODE = 1 Body = 5, Thermal = 6

nIf COBCNODE = 0 Thermal = 5

© 2023 Cadence Design Systems, Inc.

nThe effective channel length L_{Leff} and width W_{eff} are calculated from the gate length L_{gate} and width W_{gate}, where L_{gate}, and W_{gate} are related to the drawn gate length L_{drawn} and width W_{drawn} as:

nL_{gate} = Ldrawn

nW_{gate} = Wdrawn/NF

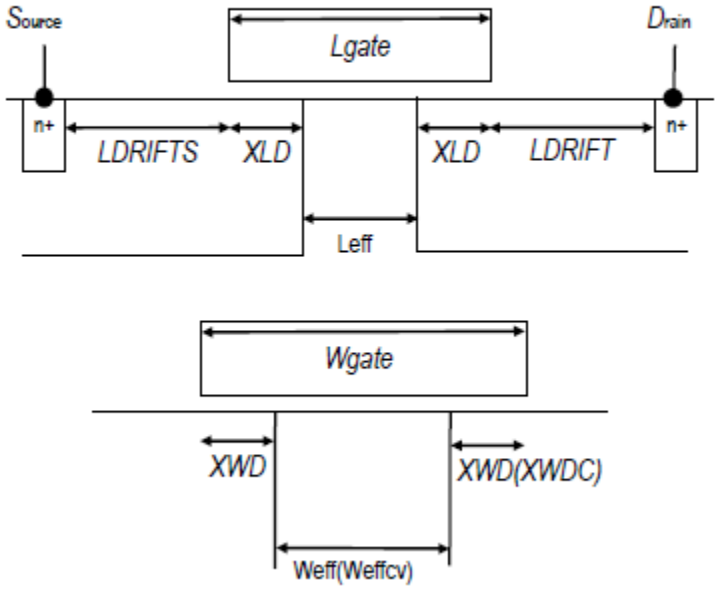
nL_{eff} = L_{gate} - 2 × XLD

nW_{eff} = W_{gate} - 2 × XWD

nW_{effc} = W_{gate} - 2 ·XWDC

nwhere XLD and XWD account for the overlaps of source/drain contact and the gate oxide. The model parameter XWDCis introduced to describe the different width dependence of capacitances from currents. If the value is not given, the same value as XWD is taken. NF is the number of fingers.

Figure 32-3 Cross section of the device structure



© 2023 Cadence Design Systems, Inc.

Table 32-1 HiSIM SOI model parameters indicates parameters

NF	number of gate fingers
XLD	gate overlap length
LDRIFT	length of drift region (drain side)
LDRIFTS	length of drift region (source side)
XWD	gate overlap width
XWDC	different width dependence of capacitance from currents

nFor any questions, contact Cadence Customer Support.

Version Update and Enhancements

Version 1.50 Enhancements

nThe 1.50 version of HiSIM_SOI includes the following changes:

? Two new body network nodes, db, and sb, are added when the values of the parameters COBCNODE and CORBNT are set to 1.

? The node nqs_qhs is introduced in the Body-Tie-Model. The values of COISUB and COFBE parameters must be set to 1 and 2, respectively, to activate the QHS model.

? COISUBFB parameter is introduced to switch Isub for calculation in FB mode: 0 with analytical Ids; 1 with iterative Ids.

? COSUBSCALE parameter is introduced to switch scaling for calculation in the Isub model and Qhs model.

? The new branches, sbbp, sbbc, dbbp, and dbbc, are added to the body resistance network, and sbsp and dbdp are added to the junction diode.

? GIDLVB parameters are introduced in the Igidl calculation.

? New parameters DVGPSUB and DVBSSUB are introduced in the Isub calculation.

? New parameters SLGL and SLGLP are introduced for substrate current dependence in the Isub local calculation.

© 2023 Cadence Design Systems, Inc.

Version 1.40 Enhancements

nThe 1.40 version of HiSIM_SOI includes the following changes:

- Channel length offset parameter for capacitance (XLDC) is introduced.
- Pocket impurity concentration NSUBP will be forcefully set to NSUBS when NSUBP is less than NSUBS. This takes into effect when VERSION > 1.30. (Default: 1.40).
- Pb2 refers to Nsub, SOI impurity concentration with various effects included, such as pocket implantation and STI-induced variation, when VERSION > 1.30 (default: 1.40). When VERSION is less than or equal to 1.30, it refers to NSUBS.
- L-scaling function for SOI impurity concentration is introduced. New model parameters: NSUBCL, NSUBCLP.
- SOI resistance model is introduced. New model flag: CORBULK. New model parameters: RBULK0, RBULKW. New OP variable: Rbulk.
- Deep punchthrough current model is introduced. New model flags: COPT, COPSPT. New model parameters: XJPT, NJUNC, MUPT, VFBPT, PSLIMPT. To activate this model, set COPT=1 and MUPT > 0.0. Previous punchthrough current model continues to exist in the new name “shallow (surface) punchthrough”. To activate this, set COPT=1 and PTL > 0.0.

Version 1.30 Enhancements

nThe 1.30 version of HiSIM_HV includes the following changes:

- Changed Model Descriptions:
  - The source codes of floating-body and body-tie were unified by using $port_connected. A new flag is introduced for model selection

    COBCNODE = 0: Floating Body model (default)

    = 1: Body Tie model
  - Implementation of bias-dependent source and drain resistance models.
  - Improvement of Charge Expression
  - The body and the substrate node potentials are consistently distinguished in all equations. The definition of internal node is also described.
  - To maintain backward compatibility, VERSION=1.20 and 1.21 are maintained in the code.

© 2023 Cadence Design Systems, Inc.

? Code Improvement: ddx() functions were removed from prev calculation

Reference

Model Equations

nSome important model equations are listed as following for your reference:

Basic Equations Solved in the HiSIM SOI Core Part

nThough all following descriptions are written for the n-channel MOSFET, they are also valid for the p-channel case. The Poisson equation solved in HiSIM SOI together with the Gauss law and boundary conditions together with the approximation of the linearly decreasing carrier density to the depth direction are

$$\phi_{\mathrm{s,SOI}} = V'_{\mathrm{G}} + \frac{Q_{\mathrm{s,bulk}} + Q_{\mathrm{i}} + Q_{\mathrm{dep,SOI}} + Q_{\mathrm{h}}}{C_{\mathrm{FOX}}} \tag{6}$$

$$\phi_{\mathrm{b,SOI}} = \phi_{\mathrm{s,SOI}} + \frac{Q_{\mathrm{s,bulk}} + \frac{1}{2}Q_{\mathrm{dep,SOI}}}{C_{\mathrm{SOI}}} \tag{7}$$

$$\phi_{\mathrm{s,bulk}} = \phi_{\mathrm{b,SOI}} + \frac{Q_{\mathrm{s,bulk}}}{C_{\mathrm{BOX}}} \tag{8}$$

nwhere Q's are charges induced within the SOI-MOSFET as depicted in 32-4 and Q_h is the excess charge in the SOI layer due to the impact ionization, and

n

$$V'_{\mathrm{G}} = V_{\mathrm{gs}} - \mathbf{VFBC} + \Delta V_{\mathrm{th}} \tag{9}$$

$$C_{\mathrm{FOX}} = \frac{\epsilon_{\mathrm{ox}}}{\mathbf{TFOX}} \tag{10}$$

$$C_{\mathrm{BOX}} = \frac{\epsilon_{\mathrm{ox}}}{\mathbf{TBOX}} \tag{11}$$

$$C_{\mathrm{SOI}} = \frac{\epsilon_{\mathrm{Si}}}{\mathbf{TSOI}} \tag{12}$$

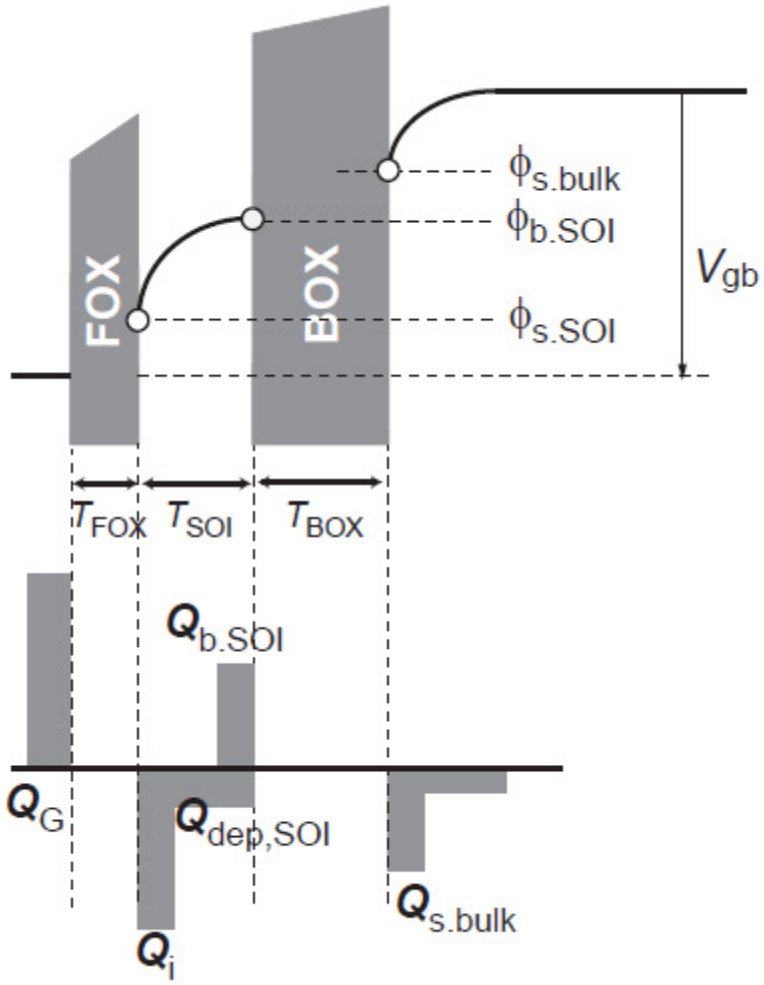
© 2023 Cadence Design Systems, Inc.

nwhere VFBC is the flat-band voltage, TFOX is the physical gate-oxide thickness, and ΔV_{th} is the threshold voltage shift in comparison to the threshold voltage of a long-channel transistor [4]. $\epsilon_{ox}(=\epsilon_0 \cdot \kappa_{Si0_2})$ is the permittivity of $Si0_2$. ϵ_0 and κ_{Si0_2} are the permittivity of vacuum and the dielectric constant of SiO_2, respectively.

nEqs. (6)– (8) are solved simultaneously within HiSIM SOI. For the body-tied case, the potential node $\phi_{b,SOI}$ is connected to the external node potential and solved by the circuit simulator. The solution takes place at source side and drain side. Prior to the Newton iteration, an approximated, analytical initial value for each variable is estimated in the code.

Figure 32-4 Band structure of SOI-MOSFET and generated charges

n



© 2023 Cadence Design Systems, Inc.

nAll device characteristics are determined on the basis of the charge control by applied voltages. All charges induced within SOI-MOSFET are functions of surface potentials written as

n

$$
\begin{aligned}
-Q_{\mathrm{dep,SOI}}(y) &= Q_{\mathrm{s,dep}} + Q_{\mathrm{b,dep}} \\
&= qN_{\mathrm{subs}}T_{\mathrm{SOI}}: \quad \text{fully depleted;} \\
&= \sqrt{\frac{2\epsilon_{\mathrm{Si}}qN_{\mathrm{subs}}}{\beta}}\left[\exp\{-\beta(\phi_{\mathrm{s,SOI}}(y)-\phi_{\mathrm{b,SOI}}(y))\}+\beta(\phi_{\mathrm{s,SOI}}(y)-\phi_{\mathrm{b,SOI}}(y))-1\right]^{\frac{1}{2}} \\
&\qquad\qquad \text{FB partially depleted} \\
&= \sqrt{\frac{2\epsilon_{\mathrm{Si}}qN_{\mathrm{subs}}}{\beta}}\left[\exp\{-\beta(\phi_{\mathrm{s,SOI}}(y)-V_{\mathrm{bcs}})\}+\beta(\phi_{\mathrm{s,SOI}}(y)-V_{\mathrm{bcs}})-1\right]^{\frac{1}{2}}: \\
&\qquad\qquad \text{BC partially depleted}
\end{aligned}
$$

$$
-Q_{\mathrm{i}}(y) = \sqrt{Q_{\mathrm{dep,SOI}}^2 + \frac{2q\epsilon_{\mathrm{Si}}}{\beta}\exp(\beta\phi_{\mathrm{s,SOI}})} - Q_{\mathrm{dep,SOI}}
$$

$$
\begin{aligned}
-Q_{\mathrm{s,bulk}}(y) = \sqrt{\frac{2\epsilon_{\mathrm{Si}}qN_{\mathrm{subb}}}{\beta}}\Big[&\exp\{-\beta(\phi_{\mathrm{s,bulk}}(y)-V_{\mathrm{es}})\}+\beta(\phi_{\mathrm{s,bulk}}(y)-V_{\mathrm{es}})-1 \\
&+\frac{n_{\mathrm{p0}}}{p_{\mathrm{p0}}}\Big\{\exp\big(\beta(\phi_{\mathrm{s,bulk}}(y)-\phi_{\mathrm{f}}(y))\big)-\exp\big(\beta(V_{\mathrm{es}}-\phi_{\mathrm{f}}(y))\big)\Big\}\Big]^{\frac{1}{2}}
\end{aligned}
$$

Drain Current

nUnder the gradual-channel approximation with further approximations of an idealized gate structure and uniform channel doping, the drain current I_{ds} is written as:

$$
I_{\mathrm{ds}} = \frac{W_{\mathrm{eff}}\cdot\mathbf{NF}}{(L_{\mathrm{eff}}-\Delta L)}\cdot\mu\cdot\frac{I_{\mathrm{dd}}}{\beta}
$$

n

$$
I_{\mathrm{dd}} = Q_{\mathrm{i(L)}} - Q_{\mathrm{i(0)}} - \left[\beta\cdot\frac{\left(Q_{\mathrm{i(L)}}+Q_{\mathrm{i(0)}}\right)\cdot(\phi_{\mathrm{sL}}-\phi_{\mathrm{s0}})}{2}\right]
$$

© 2023 Cadence Design Systems, Inc.

Threshold Voltage Shift

nThe surface-potential-based model requires no threshold voltage V_{th} in its core description of the model. However, HiSIM SOI has opted for modeling various submodels such as short-channel effects as a V_{th} shift from an otherwise ideal case.

nThe whole contribution to the V_{th} is summarised as

n$\Delta V_{th} = \Delta V_{th,\,SC} + \Delta V_{th,R} + \Delta V_{th,P} + \Delta V_{th,SCR} + \Delta V_{th,W} + \Delta V_{th,sm} - \phi S_{pg}$

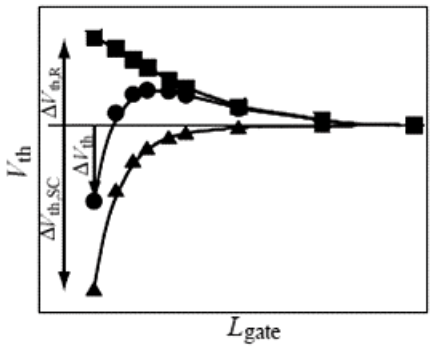
nThe modeled V_{th} is incorporated in the ϕS iteration can be viewed as consisting of two main effects or components:

n(I) the short-channel effect: $\Delta V_{th,\,SC}$

n(II) the reverse-short-channel effect: $\Delta V_{th,\,R}$ and $\Delta V_{th,\,P}$

nThe separation into these two components ($\Delta V_{th} = \Delta V_{th,\,SC} + \Delta V_{th,\,R}$ (or $\Delta V_{th,\,P}$)) is schematically shown in Figure 32-5.

Figure 32-5 Schematic plot of the separation of Vth into the contributions of the short-channel and the reverse short-channel effect.



© 2023 Cadence Design Systems, Inc.

Mobility Model

nThe low-field mobility is described with the following expressions and includes the three independent mechanisms of Coulomb, phonon and surface-roughness scattering:

$$\frac{1}{\mu_0} = \frac{1}{\mu_{CB}} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}$$

$$\mu_{CB}(Coulomb) = MUECB0 + MURCB1 \cdot \frac{Q_i}{q \times 10^{11}}$$

$$\mu_{PH}(phonon) = \frac{M_{uephonon}}{E_{eff}^{MUEPH0}}$$

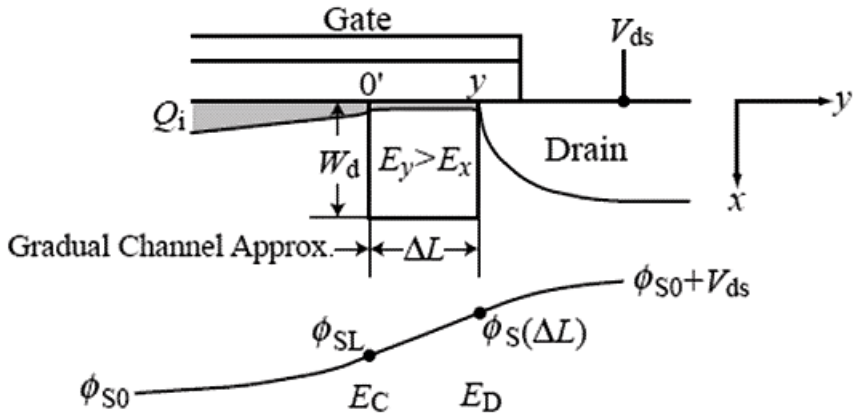
$$\mu_{SR}(surface\ \ roughness) = \frac{MUESR1}{E_{eff}^{Mueserface}}$$

Channel-Length Modulation

nAs the gradual-channel approximation is not valid for large V_{ds} causing the pinch-off phenomenon in the channel. Without taking into account the pinch-off phenomenon, the calculated channel conductance gds enters abruptly into the saturation condition. To include the pinch-off phenomenon in HiSIM, we apply the conventional method of modeling the pinch-off region (ΔL) separately from the rest of the channel as depicted in Figure 32-6:

© 2023 Cadence Design Systems, Inc.

Figure 32-6 Schematic showing the correlation among physical quantities in the pinch-off region.



nAfter taking into all effects, the final ΔL is derived as:

$$\Delta L = \frac{1}{2}\left[-\frac{1}{L_{eff}}\left(2\frac{I_{dd}}{\beta Q_i} z + 2\frac{N_{sub}}{\varepsilon_{Si}}\left(\phi_s(\Delta L) - \phi_{SL}\right) z^2 + E_0 z^2 \right) \right]$$
$$+ \frac{1}{2}\sqrt{\frac{1}{L_{eff}^2}\left(2\frac{I_{dd}}{\beta Q_i} z - 2\frac{N_{sub}}{\varepsilon_{Si}}(\phi_s(\Delta L) - \phi_{SL}) z^2 \right)^2 + 4\left(2\frac{N_{sub}}{\varepsilon_{Si}}(\phi_s(\Delta L) - \phi_{SL}) z^2 + E_0 z^2 \right)}$$

Narrow-Channel Effects

nThe V_{th} reduction for reduced channel width (W_{gate}) is modeled under inclusion of the edge-fringing capacitances C_{ef} at the edge of the trench as:

n

$$\Delta V_{\mathrm{th,W}} = \left(\frac{1}{C_{\mathrm{FOX}}} - \frac{1}{C_{\mathrm{FOX}} + 2C_{\mathrm{ef}}/(L_{\mathrm{eff}} W_{\mathrm{eff}})} \right) qN_{\mathrm{subc}} W_{\mathrm{d}} + \frac{\mathbf{WVTH0}}{W_{\mathrm{gate}} \times 10^6}$$

Temperature Dependences

nThe temperature dependence is included automatically in the surface potentials through β, which is the inverse of the thermal voltage. Additionally the band gap, the intrinsic carrier

© 2023 Cadence Design Systems, Inc.

concentration, the carrier mobility, and the carrier saturation velocity are also temperature dependent.

$$E_g = EG0 - BGTMP1 \cdot (T - TNOM) - BGTMP2 \cdot (T - TNOM)^2$$

$$\mu_{PH}(phonon) = \frac{M_{uephonon}}{(T/TNOM)^{MUETMP} \times E_{eff}^{MUEPH0}}$$

$$V_{\max} = \frac{VMAX}{1.8 + 0.4(T/TNOM) + 0.1(T/TNOM)^2 - VTMP \times (1 - T/TNOM)}$$

$$E_{gp} = E_{g0} + EGIG + IGTEMP2(1/T - 1/TNOM) + IGTEMP3(1/T^2 - 1/TNOM^2)$$

Drain-side resistance

$$R_{\text{drift}} = \left(\frac{V_{\text{ddp}}}{I_{\text{ddp}}} + \mathbf{RSH} \cdot \mathbf{NRD} \right)$$

Source-side resistance

$$R_{\text{source}} = \left(\frac{V_{\text{ssp}}}{I_{\text{ssp}}} + \mathbf{RSH} \cdot \mathbf{NRS} \right)$$

Gate resistance

$$R_{\text{g}} = \frac{\mathbf{RSHG} \cdot \left(\mathbf{XGW} + \frac{W_{\text{eff}}}{3 \cdot \mathbf{NGCON}} \right)}{\mathbf{NGCON} \cdot (L_{\text{drawn}} - \mathbf{XGL}) \cdot \mathbf{NF}}$$

© 2023 Cadence Design Systems, Inc.

Capacitance

Intrinsic Capacitance

nThe intrinsic capacitances are derivatives of the node charges determined as

$$C_{jk} = \delta \frac{\partial Q_j}{\partial V_k}$$

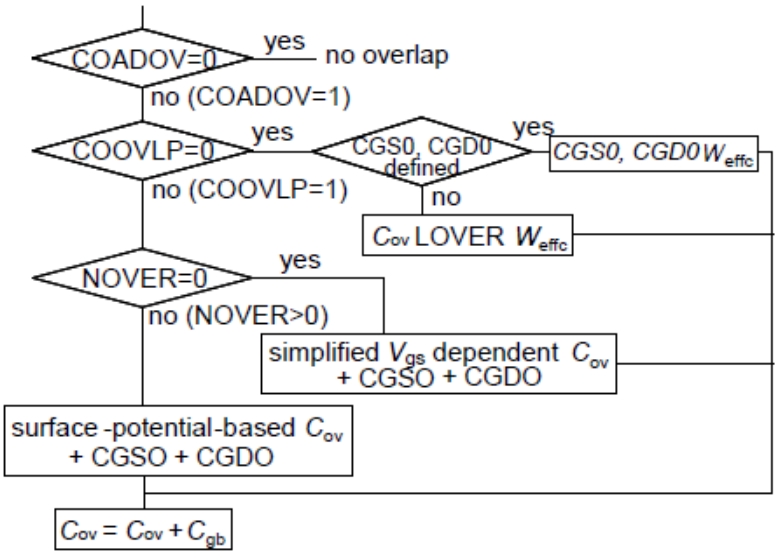
$$\delta = -1 \text{ for } j \neq k$$

$$\delta = 1 \text{ for } j = k$$

Overlap Capacitance

nTo consider the overlap capacitance, the flag COADOV must be selected to 1, which is the default. The overlap capacitance includes three options as summarized in 32-7, where the drain side and the source side are treated as identical. If Flag COOVLP=0, the overlap capacitances are treated to be constant. If CGSO and CGDO are defined, these values are taken. If they are not defined, the values are calculated with the overlap length LOVER and oxide capacitance CFOX.

Figure 32-7 Model options of the overlap capacitance at the drain side are summarized.



© 2023 Cadence Design Systems, Inc.

Gate-Fringing Capacitance

nThe outer fringing capacitance is modeled as

n

$$C_{\text{fring}} = \frac{\epsilon_{\text{ox}}}{\pi/2} W_{\text{gate}} \cdot \mathbf{NF} \cdot \ln\left(1 + \frac{\mathbf{TPOLY}}{T_{\text{FOX}}}\right)$$

Leakage Currents

Substrate Current

nThe substrate current is derived as

$$I_{\text{sub}} = \frac{C_1}{C_2}\left(\phi(y) - \phi(0)\right) I_{\text{ds}} \exp\left(-\frac{\lambda C_2}{\phi(y) - \phi(0)}\right)$$

nwhere

n

$$\lambda^2 = \frac{\epsilon_{\text{Si}} X_{\text{j}} T_{\text{FOX}}}{\epsilon_{\text{ox}}}$$

nand X_j is the junction depth.

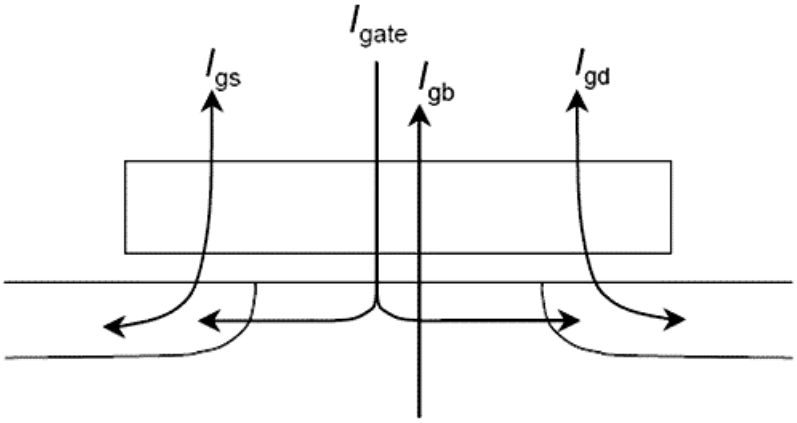
Gate Current

nAll possible gate leakage currents are schematically shown in Fig. 32.8

© 2023 Cadence Design Systems, Inc.

nBetween Gate and Channel, I_{gate}

$$I_{gate} = q \cdot GLEAK1 \cdot \frac{E^2}{E_{gp}^{\frac{1}{2}}} \cdot \exp\left(-\frac{E_{gp}^{\frac{3}{2}} \times GLEAK2}{E} \right) \cdot \sqrt{\frac{Q_i}{const0}} \cdot W_{eff} \cdot NF \cdot L_{eff}$$
$$\cdot \frac{GLEAK6}{GLEAK6 + V_{ds}} \cdot \frac{GLEAK7}{GLEAK7 + W_{eff} \cdot NF \cdot L_{eff}}$$



nBetween Gate and Bulk, I_{gb}

nThe I_{gb} current under the accumulation condition is modeled as

$$I_{gb} = GLKB1 \cdot E_{gb}^2 \cdot \exp\left(-\frac{GLKB2}{E_{gb}} \right) W_{eff} \cdot NF \cdot L_{eff}$$
$$E_{gb} = -\frac{V_{gs} - VFBC + GLKB3}{T_{ox}}$$

nBetween Gate and Source/Drain, I_{gs}/I_{gd}

$$I_{gs} = signGIKSD1 \cdot E_{gs}^2 \exp(T_{ox}(GLKSD2 \cdot V_{gs} + GLKSD3)) \cdot W_{eff} \cdot NF$$
$$I_{gd} = signGIKSD1 \cdot E_{gd}^2 \exp(T_{ox}(GLKSD2 \cdot (-V_{gs} + V_{ds}) + GLKSD3)) \cdot W_{eff} \cdot NF$$

© 2023 Cadence Design Systems, Inc.

GIDL (Gate-Induced Drain Leakage)

$$I_{\mathrm{GIDL}} = q \cdot \mathbf{GIDL1} \cdot \frac{E^2}{E_{\mathrm{g}}^{\frac{1}{2}}} \cdot \exp\left(-\mathbf{GIDL2} \cdot \frac{E_{\mathrm{g}}^{\frac{3}{2}}}{E}\right) \cdot W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot \frac{V_{\mathrm{db}}^3}{V_{\mathrm{db}}^3 + 0.5}$$

Floating-Body Effect Model

nModel selector COFBE as well as COISUB must be set to 1 to activate FBE model. In HiSIM SOI, Q_h is modeled as follows:

$$Q_{\mathrm{h}} = \left\{[\exp[-\beta(\phi_{\mathrm{s0,SOI}} - \Delta V_{\mathrm{sb}})] + \beta(\phi_{\mathrm{s0,SOI}} - \Delta V_{\mathrm{sb}}) - 1]^{1/2} - [\exp[-\beta\phi_{\mathrm{s0,SOI}}] + \beta\phi_{\mathrm{s0,SOI}} - 1]^{1/2}\right\}$$

$$\Delta V_{\mathrm{se}} = \mathbf{QHE1} \cdot \frac{1}{\beta} \log\left[1 + \frac{(I_{\mathrm{sub}} + I_{\mathrm{evb}}) L_{\mathrm{p}} L_{\mathrm{n}}}{q \cdot \mathbf{TSOI} \cdot W_{\mathrm{eff}} \mathrm{e}^{-\beta \cdot \mathbf{QHE2}} (D_{\mathrm{n}} N_{\mathrm{d}} L_{\mathrm{p}} + D_{\mathrm{p}} N_{\mathrm{d}} L_{\mathrm{n}})}\right]$$

History Effect Model

nTime constant for the history effect is modeled as:

$$\begin{aligned} \tau_{\mathrm{h}} &= R_{\mathrm{sb}} \cdot C_{\mathrm{FOX}} \\ R_{\mathrm{sb}} &= \frac{\mathbf{HIST1}}{I_{\mathrm{sub}} + \mathbf{HIST2}} \end{aligned}$$

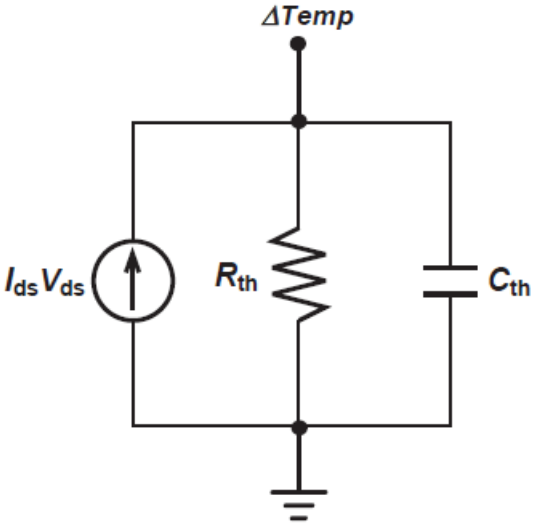
nwhere HIST1 and HIST2 are history effect model parameters.

Self-Heating Effect Model

nThe self-heating effect is modeled as a C-R thermal network with a heat resistance parameter RTH0 and capacitance parameter CTH0. The flag COSELFHEAT must be equal to 1 and RTH0 must not be equal to zero to activate this model. The SHE should be switched on/off only with the model flag COSELFHEAT.

© 2023 Cadence Design Systems, Inc.

Figure 32-8 Thermal Network applied for the self-heating effect



Source/Body and Drain/Body Diode Models

Diode Current

n

$$T_{\mathrm{tnom}} = \frac{T}{\mathrm{TNOM}}$$

$$j_{\mathrm{s}} = \mathrm{JS0} \cdot \exp\left\{\frac{(E_{\mathrm{gtnom}} \cdot \beta_{\mathrm{tnom}} - E_{\mathrm{g}}\beta + \mathrm{XTI} \cdot \log(T_{\mathrm{tnom}}))}{\mathrm{NJ}}\right\}$$

$$j_{\mathrm{s2}} = \mathrm{JS0} \cdot \exp\left\{\frac{(E_{\mathrm{gtnom}} \cdot \beta_{\mathrm{tnom}} - E_{\mathrm{g}}\beta + \mathrm{XTI2} \cdot \log(T_{\mathrm{tnom}}))}{\mathrm{NJ}}\right\}$$

$$E_{\mathrm{gtnom}} = \mathrm{EG0} - 90.25 \times 10^{-6} \cdot \mathrm{TNOM} - 1.0 \times 10^{-7} \cdot \mathrm{TNOM}^2$$

$$\beta_{\mathrm{tnom}} = \frac{q}{k_{\mathrm{B}} \cdot \mathrm{TNOM}}$$

$$N_{\mathrm{vtm}} = \frac{\mathrm{NJ}}{\beta}$$

© 2023 Cadence Design Systems, Inc.

Between drain and body

nThe forward and backward currents between drain and body are calculated as:

$$I_{\rm sbd} = W_{\rm eff} \cdot \mathbf{NF} \cdot \mathbf{TSOI} \cdot j_{\rm s}$$
$$I_{\rm sbd2} = W_{\rm eff} \cdot \mathbf{NF} \cdot \mathbf{TSOI} \cdot j_{\rm s2}$$

nThe drain-body current equations are derived as follows:

$$V_{\rm bcd} = V_{\rm bcs} - V_{\rm ds}$$
$$v_{\rm bdt} = N_{\rm vtm} \cdot \log\left\{\frac{\mathbf{VDIFFJ}}{I_{\rm sbd}} \cdot (T_{\rm tnom})^2 + 1\right\}$$

(i) $V_{\rm bcd} < v_{\rm bdt}$

$$I_{\rm bd} = I_{\rm sbd}\left\{\exp\left(\frac{V_{\rm bcd}}{N_{\rm vtm}}\right) - 1\right\}$$

(ii) $V_{\rm bcd} \geq v_{\rm bdt}$

$$I_{\rm bd} = I_{\rm sbd}\left\{\exp\left(\frac{v_{\rm bdt}}{N_{\rm vtm}}\right) - 1\right\} + \frac{I_{\rm sbd}}{N_{\rm vtm}}\exp\left(\frac{v_{\rm bdt}}{N_{\rm vtm}}\right)(V_{\rm bcd} - v_{\rm bdt})$$

$$I_{\rm bd} = I_{\rm bd} + \mathbf{DIVX} \cdot I_{\rm sbd2} \cdot V_{\rm bcd}$$

© 2023 Cadence Design Systems, Inc.

Between source and body

$$I_{\rm sbs} = W_{\rm eff} \cdot \mathbf{NF} \cdot \mathbf{TSOI} \cdot j_{\rm s}$$
$$I_{\rm sbs2} = W_{\rm eff} \cdot \mathbf{NF} \cdot \mathbf{TSOI} \cdot j_{\rm s2}$$

$$v_{\rm bst} = N_{\rm vtm} \cdot \log\left\{\frac{\mathbf{VDIFFJ}}{I_{\rm sbs}} \cdot (T_{\rm tnom})^2 + 1\right\}$$

(i) $V_{\rm bcs} < v_{\rm bst}$

$$I_{\rm bs} = I_{\rm sbs} \cdot \left\{\exp\left(\frac{V_{\rm bcs}}{N_{\rm vtm}}\right) - 1\right\}$$

(ii) $V_{\rm bcs} \geq v_{\rm bst}$

$$I_{\rm bs} = I_{\rm sbs}\left\{\exp\left(\frac{v_{\rm bst}}{N_{\rm vtm}}\right) - 1\right\} + \frac{I_{\rm sbs}}{N_{\rm vtm}}\exp\left(\frac{v_{\rm bst}}{N_{\rm vtm}}\right)(V_{\rm bcs} - v_{\rm bst})$$

$$I_{\rm bs} = I_{\rm bs} + \mathbf{DIVX} \cdot I_{\rm sbs2} \cdot V_{\rm bcs}$$

Body-Tie Models

nHiSIM SOI considers both the floating-body and the body-tie structures.

Body-Contact Capacitances

nABTN = LBT ·WBTN

nABTP = LBT ·WBTP

Overlap capacitance of body-tie area

nThe capacitance between the body-tied gate (hammer head) and the body-tied well is treated as MOS capacitance.

n$C_{gb,bt}$ = C_{btN} · ABTN + C_{btP} · ABTP

Overlap capacitance of body-tie periphery

nInstance parameters PSBCP and PDBCP are introduced to take into account the overlap capacitance of the periphery of the body-tie contact. These lengths are added to the W_{effc} as:

© 2023 Cadence Design Systems, Inc.

$nW_{effc,source} = W_{effc} + PSBCP$

$nW_{effc,drain} = W_{effc} + PDBCP$

nwhere

$nW_{effc} = W_{gate} - NBT \cdot XWDBT - (2 - NBT) \cdot XWDC$

Diode current of body-tie periphery

nThe diode current also flows at the body-tie periphery. Therefore the lengths determined by the instance parameters PSBCP and PDBCP are added the width as

$nW_{eff,source} = W_{eff} + PSBCP$

$nW_{eff,drain} = W_{eff} + PDBCP$

nwhere

$nW_{eff} = W_{gate} - NBT \cdot XWDBT - (2 - NBT) \cdot XWD$

Gate-Fringing Capacitance

nFor body-tied devices, an additional gate-fringing capacitance is considered between gate and body:

$$C_{\mathrm{fring,bt}} = \frac{\epsilon_{\mathrm{ox}}}{\pi/2}\mathbf{LBT} \cdot \mathbf{NF} \cdot \ln\left(1 + \frac{\mathbf{TPOLY}}{T_{\mathrm{FOX}}}\right)$$

nNoise Models

1/f Noise Models

nThe 1/f noise is caused by both the carrier fluctuation and the mobility fluctuation. The final description for the drift-diffusion model is

$$S_{I_{ds}} = \frac{I_{ds}^2 NFTRP}{\beta f (L_{eff} - \Delta L) W_{eff} \cdot NF}\left[\frac{1}{(N_0 + N^*)(N_L + N^*)} + \frac{2\mu E_y NFALP}{N_L - N_0}\ln\left(\frac{N_L + N^*}{N_0 + N^*}\right) + (\mu E_y NFALP)^2\right]$$

© 2023 Cadence Design Systems, Inc.

nwhere the parameters **NFALP** and **NFTRP** represent the contribution of the mobility fluctuation and the ratio of trap density to attenuation coefficient, respectively.

Thermal Noise Model

nVan der Ziel derived the equation for the spectral density of the thermal drain-noise current at temperature T by integrating the trans-conductance along the channel direction y based on the Nyquist theorem

$$S_{id} = 4kT\frac{W_{eff}\cdot NF\cdot C_{ox}\cdot Vg\cdot Vt\cdot\mu}{(L_{eff}-\Delta L)}\frac{(1+3\eta+6\eta^2)\mu_d^2+(3+4\eta+3\eta^2)\mu_d\mu_s+(6+3\eta+\eta^2)\mu_s}{15(1+\eta)\mu_{av}^2}$$

nwhere μ_s, μ_d and μ_{av} are mobilities at the source side, the drain side, and averaged, respectively.

Induced Gate Noise Model

$$N_{igate} = S_{igate}/f^2$$

Coupling Noise Model

$$N_{cross} = \frac{S_{igid}}{\sqrt{S_{igate}\cdot S_{id}}}$$

Non-Quasi-Static (NQS) Model

Formation of carrier

nCarriers in the channel take time to build-up as opposed to the Quasi-Static (QS) approximation. To consider this phenomenon in HiSIM, the carrier formation is modeled as

$$q(t_i) = \frac{q(t_i-1)+\frac{\Delta t}{\tau}Q(t_i)}{1+\frac{\Delta t}{\tau}}$$

© 2023 Cadence Design Systems, Inc.

nwhere $q(t_i)$ and $Q(t_i)$ represent the non-quasi-static and the quasi-static carrier density at time ti, respectively, and $\Delta t = t_i - t_{i-1}$ is valid. Above equation implies that the formation of carriers under the NQS approximation is always delayed in comparison to the QS approximation, which is the basic origin of the NQS effect.

Delay Mechanisms

nWeak inversion

$$\tau_{diff} = DLY1$$

nStrong inversion

$$\tau_{cond} = DLY2 \cdot \frac{Q_i}{I_{ds}}$$

nThese two delay mechanisms (diffusion and conduction) are combined using the Matthiessen rule:

$$\frac{1}{\tau} = \frac{1}{\tau_{diff}} + \frac{1}{\tau_{cond}}$$

nApplying the same approach for the formation of bulk carriers, leads to the approximation of the bulk carrier delay as an RC delay in the form

$$\tau_{\mathrm{B}} = \mathbf{DLY3} \cdot C_{\mathrm{FOX}}$$

Component Statements

Instance Parameters

nRefer to the following table for Instance Parameter details:

1	`l=5.0E-6 m`	Gate length (Lgate).
2	`w=5.0E-6 m`	Gate width (Wgate).
3	`ad=0.0 m^2`	Area of drain junction.
4	`as=0.0 m^2`	Area of source junction.
5	`pd=0.0 m`	Perimeter of drain junction.

© 2023 Cadence Design Systems, Inc.

6	`ps=0.0 m`	Perimeter of source junction.
7	`ngcon=1.0 -`	Number of gate contacts.
8	`xgw=0E0 m`	Distance from gate contact to channel edge.
9	`xgl=0E0 m`	Offset of gate length.
10	`m=1.0`	multiplicity factor.
11	`nf=1.0 -`	Number of gate fingers.
12	`sa=0 m`	Length of diffusion between gate and STI.
13	`sb=0 m`	Length of diffusion between gate and STI.
14	`sd=0 m`	Length of diffusion between gate and gate.
15	`pdbcp=0.0 m`	Parasitic perimeter length for body contact at drain.
16	`psbcp=0.0 m`	Parasitic perimeter length for body contact at source.
17	`lod=10.0E-6 m`	diffusion length between gate and STI edge.
18	`temp=0.0 C`	Device temperature.
19	`dtemp=0 C`	Device temperature change.
20	`trise=0 C`	Device temperature change.
21	`nbt=1.0`	Number of body contact.
22	`lbt=0.0 m`	Length of gate over body-contact well.
23	`wbtp=0.0 m`	Distance of gate protrusion over body-contact well.
24	`wbtn=0.0 m`	Distance of gate protrusion over body-contact well.
25	`abtn=0.0 m^2`	Area of N^+ poly area of body contact.
26	`abtp=0.0 m^2`	Area of P^+ poly area of body contact.
27	`nrs=1.0`	Number of squares in source .
28	`nrd=1.0`	Number of squares in drain .
29	`ldrift=1.0E-6 m`	Parameter for drift region length (drain) .
30	`ldrifts=1.0E-6 m`	Parameter for drift region length (source) .
31	`rbdb=50.0 Ohm`	Substrate resistance network.
32	`rbsb=50.0 Ohm`	Substrate resistance network.

Model Definition

```
model modelName hisimsoi parameter=value ...
```

Model Parameters

nRefer to the following table for Model Parameter details:

1	`l=5.0E-6 m`	Gate length (Lgate).
2	`w=5.0E-6 m`	Gate width (Wgate).

© 2023 Cadence Design Systems, Inc.

3	`wmax=1.0`	Maximum width for the model.
4	`wmin=0.0`	Minimum width for the model.
5	`lmax=1.0`	Maximum length for the model.
6	`lmin=0.0`	Minimum length for the model.
7	`copprv=0`	Previous phi_s flag.
8	`coadov=1`	Lateral field induced and overlap capacitances are added to intrinsic.
9	`coisub=0`	Substrate current flag.
10	`cofbe=0`	Floating-Body Effect flag.
11	`coiigs=0`	Gate current flag.
12	`cogidl=0`	GIDL current flag.
13	`coovlp=0`	Overlap capacitance model selector.
14	`coign=0`	Induced gate and cross correlation noise flag.
15	`coflick=0`	1/f noise flag.
16	`cothrml=0`	Thermal noise flag.
17	`coisti=0`	STI leakage current flag.
18	`conqs=0`	Non-quasi-static model flag.
19	`corg=0`	Gate-contact resistance flag.
20	`coievb=0`	Valence-band-electron-tunneling-current model flag.
21	`cohist=0`	History Effect flag.
22	`coselfheat=0`	Self-Heating flag.
23	`covbsbiz=0`	Symmetry treatment flag.
24	`colgleff=0`	Lgate to Leff flag.
25	`coqovsm=1`	Qover capacitance model selector.
26	`coqbdsm=1`	Gate/body contact well MOS-capacitance model selector.
27	`cobcnode=0`	Body contact node flag.
28	`cosubscale=0`	Switch scaling for Isub.
29	`coisubfb=0`	Switch Isub in FB mode: 0 with analytical Ids; 1 with iterative Ids.
28	`info=0`	print information selector.
31	`qhsmax=1e-3`	Upper limit Qhs .
32	`dvgpsub=0`	Delta VGPSUB (in addition to VFBSUB).
33	`dvbssub=0`	Delta VBSSUB for Qh effect.
34	`type=1 -`	1 for nMOS and -1 for pMOS. Possible values are p and n.

© 2023 Cadence Design Systems, Inc.

35	`version=1.40 -`	Model parameter version accepts only real number values, like 1.30 for version=1.3.0. The available versions
36	`vmax=7.00E+6 cm s^-1`	Saturation velocity.
37	`bgtmp1=90.25E-6 eV K^-1`	Temperature dependence of bandgap.
38	`bgtmp2=100.0E-9 eV K-2`	Temperature dependence of bandgap.
39	`eg0=1.1785 eV`	Bandgap.
40	`xld=0.0 m`	Gate overlap length.
41	`xldc=0.0 m`	XLD for capacitance.
42	`vfbover=0.0 V`	Flat-band voltage in overlap region.
43	`nover=1E19 cm-3`	Impurity concentration in overlap region.
44	`xwd=0.0 m`	Gate overlap width.
45	`xwdc=0.0 m`	XWD for cap.
46	`saref=1E-6 m`	Reference distance from STI edge to Gate edge.
47	`sbref=1E-6 m`	Reference distance from STI edge to Gate edge.
48	`xqy=0.0 m`	Distance from junction to max field point.
49	`xqy1=0.0 F µm^XQY2-1`	Vbs-dependence of Qy.
50	`xqy2=2.0 -`	Lgate-dependence of Qy.
51	`rshg=0.0 ?/square`	Gate sheet resistance.
52	`vfbc=(-1.0) V`	Flat-band voltage.
53	`vbi=1.1 V`	Built-in potential.
54	`nsubpl=0.001 m^-1`	Modification of pocket-impurity concentration.
55	`nsubpfac=1 -`	Modification of pocket-impurity concentration.
56	`parl1=10.0E-9 cm`	SOI SCE parameter.
57	`parl2=10.0E-9 m`	Depletion width of channel/contact junction.
58	`lp=0.0 m`	Pocket penetration length.
59	`nsubp=1.0E+17 cm-3`	Max pocket concentration.
60	`nsubp0=0.0 -`	Modification of pocket concentration for narrow W.
61	`nsubwp=1.0 -`	Modification of pocket concentration for narrow W.
62	`wl1=0.0 m`	Small-size effect parameter for STI leakage.
63	`wl1p=1.0 -`	Small-size effect parameter for STI leakage.
64	`wl2=0.0 -`	Threshold voltage shift due to small-size effect.
65	`wl2p=1.0 -`	Threshold voltage shift due to small-size effect.
66	`scp1=0.0 -`	Magnitude of short-channel effect due to pocket.
67	`scp2=0.0 V^-1`	Vds-dependence of SCE due to pocket.

© 2023 Cadence Design Systems, Inc.

68	`scp3=0.0 m V^-1`	Vds-dependence of SCE due to pocket.
69	`sc1=0.0 -`	magnitude of short-channel effect.
70	`sc2=0.0 V^-1`	Vds-dependence of short-channel effect.
71	`sc3=0.0 m V^-1`	Vbs dependence of short-channel effect.
72	`scr1=0.0 -`	Parameter for SCE via BOX.
73	`scr2=0.0 -`	Parameter for SCE via BOX.
74	`scr3=0.23 -`	Parameter for SCE via BOX.
75	`pgd1=0.0 V`	Strength of poly-depletion effect.
76	`pgd2=1.0 V`	Threshold voltage of poly-depletion effect.
77	`pgd4=0.0 -`	Lgate-dependence of poly-depletion effect.
78	`ndep=1.0 -`	Depletion charge contribution to Eeff.
79	`ninv=0.5 -`	inversion charge contribution to Eeff.
80	`ninvd=0.0 V^-1`	inversion charge parameter.
81	`muecb0=300.0 cm2V^-1s^-1`	Coulomb scattering.
82	`muecb1=30.0 cm2V^-1s^-1`	Coulomb scattering.
83	`mueph0=300.0E-3 -`	Phonon scattering.
84	`muephw=0.0 -`	Phonon-related mobility reduction.
85	`muepwp=1.0 -`	Phonon-related mobility reduction.
86	`muephl=0.0 -`	L-dependence of phonon mobility reduction.
87	`mueplp=1.0 -`	L-dependence of phonon mobility reduction.
88	`muephs=0.0 -`	Mobility change due to small size.
89	`muepsp=1.0 -`	Mobility change due to small size.
90	`vtmp=0.0 cm s^-1`	Temperature-dependence of saturation velocity.
91	`wvth0=0.0 Vμm`	Threshold voltage shift.
92	`muesr1=2.0E15 cm2V^-1s^-1`	Surface-roughness scattering.
93	`muesr0=2.0 -`	Surface-roughness scattering.
94	`muesrl=0.0 -`	L-dependence of surface roughness on mobility.
95	`muesrw=0.0 -`	Surface roughness-related mobility change.
96	`mueswp=1.0 -`	Surface roughness-related mobility change.
97	`mueslp=1.0 -`	L-dependence of surface roughness on mobility.
98	`muetmp=1.5 -`	Temperature-dependence of phonon scattering.
99	`bb=2.0 -`	High-field-mobility degradation.
100	`ddltmax=10.0 -`	Smoothing coefficient for Vds.
101	`ddltslp=10.0 μm^-1`	Lgate-dependence of smoothing coefficient.

© 2023 Cadence Design Systems, Inc.

102	`ddltict=0.0 -`	Lgate-dependence of smoothing coefficient.
103	`sub1=0.01 V^-1`	Substrate current coefficient of magnitude.
104	`sub2=20.0 V`	Substrate current coefficient of exponential term.
105	`sub1l=2.5E-3 m`	Lgate-dependence of SUB1.
106	`sub1lp=1.0 -`	Lgate-dependence SUB1.
107	`sub2l=2.0E-6 m`	Lgate-dependence of SUB2.
108	`svds=3.0 -`	Substrate current dependence on Vds.
109	`slg=3.0E-8 m`	Substrate current dependence on Lgate.
110	`svbs=0.5 -`	Substrate current dependence on Vbs.
111	`svbsl=0.0 -`	Lgate-dependence of SVBS.
112	`svbslp=1.0 -`	Lgate-dependence of SVBS.
113	`svgs=0.8 -`	Substrate current dependence on Vgs.
114	`svgsl=0.0 -`	Lgate-dependence of SVGS.
115	`svgslp=1.0 -`	Lgate-dependence of SVGS.
116	`svgsw=0.0 -`	Wgate-dependence of SVGS.
117	`svgswp=1.0 -`	Wgate-dependence of SVGS.
118	`slgl=0.0`	Substrate current dependence on Lgate.
119	`slglp=1.0`	Substrate current dependence on Lgate .
120	`vfbsub=(-1.0) V`	Flatband voltage for Isub calculation.
121	`vfbsubl=0.0 –`	Lgate-dependence of VFBSUB.
122	`vfbsublp=1.0 -`	Lgate-dependence of VFBSUB.
123	`subdlt=2.0E-3 -`	Smoothing parameter (hisimsoi_fb only).
124	`hist1=10E-9 V`	History-effect parameter.
125	`hist2=1E-20 A`	History-effect parameter.
126	`qhe1=1.5 -`	FBE parameter.
127	`qhe2=0.35 V`	FBE parameter.
128	`evb1=0.0 V-2s^-1`	Electron tunneling from valence band.
129	`evb2=0.0 V m^-1`	Electron tunneling from valence band.
130	`evb3=0.0 -`	Electron tunneling from valence band.
131	`fvbs=0.0 -`	Vbs dependence of Fowler-Nordheim current.
132	`ibpc1=0.0 ?`	impact-ionization-induced bulk potential change.
133	`ibpc2=0.0 V^-1`	impact-ionization-induced bulk potential change.
134	`nsti=5.0E17 cm-3`	Substrate impurity concentration at STI edge.
135	`wsti=0.0 m`	Width of high-field region at STI edge.
136	`wstil=0.0 –`	Channel-length dependence of WSTI.
137	`wstilp=1.0 -`	Channel-length dependence of WSTI.
138	`wstiw=0.0 –`	Channel-width dependence of WSTI.

© 2023 Cadence Design Systems, Inc.

139	`wstiwp=1.0 -`	Channel-width dependence of WSTI.
140	`scsti1=0.0 -`	The same effect as SC1 but at STI edge.
141	`scsti2=0.0 V^-1`	The same effect as SC2 but at STI edge.
142	`vthsti=0.0 V`	Threshold voltage shift due to STI.
143	`vdsti=0.0 -`	Vds dependence of STI subthreshold.
144	`muesti1=0.0 m`	Mobility change due to diffusion length.
145	`muesti2=0.0 -`	Mobility change due to diffusion length.
146	`muesti3=1.0 -`	Mobility change due to diffusion length.
147	`nsubpsti1=0.0 m`	Pocket concentration modifier.
148	`nsubpsti2=0.0 -`	Pocket concentration modifier.
149	`nsubpsti3=1.0 -`	Pocket concentration modifier.
150	`nsubcsti1=0.0 m`	Channel concentration modifier.
151	`nsubcsti2=0.0 -`	Channel concentration modifier.
152	`nsubcsti3=1.0 -`	Channel concentration modifier.
153	`tpoly=0.0 m`	Height of poly-Si gate for fringing cap.
154	`cgbo=0.0 F m^-1`	Gate-to-B overlap cap.
155	`cgdo=0.0 F m^-1`	Gate-to-drain overlap cap.
156	`cgso=0.0 F m^-1`	Gate-to-source overlap cap.
157	`ovslp=2.1E-7 mV^-1`	Coefficient for overlap capacitance.
158	`ovmag=0.6E0 V`	Coefficient for overlap capacitance.
159	`js0=1.0E-4 A m-2`	Saturation current density.
160	`nj=1.0 -`	Emission coefficient.
161	`xti=2.0 -`	Temp coefficient for forward current densities.
162	`xti2=0.0 -`	Temp coefficient for reverse current densities.
163	`vdiffj=1.6E-3 V`	Diode threshold voltage at junction.
164	`divx=0.0 V^-1`	Reverse current coefficient.
165	`cj=5.0E-04 F m-2`	Bottom junc cap/unit area at zero bias.
166	`cjsw=5.0E-10 F m^-1`	Sidewall junc cap grading coefficient.
167	`cjswg=5.0E-10 F m^-1`	Sidewall junc cap per unit length at zero bias.
168	`mj=0.33 -`	Bottom junc cap grading coefficient.
169	`mjsw=0.33 -`	Sidewall junc cap grading coefficient.
170	`mjswg=0.33 -`	Gate sidewall junc cap grading coefficient.
171	`pb=1.0 V`	Bottom junc built-in potential.
172	`pbsw=1.0 V`	Sidewall junc built-in potential.
173	`pbswg=1.0 V`	Gate sidewall junc built-in potential.
174	`lover=30E-9 m`	Overlap length.

© 2023 Cadence Design Systems, Inc.

175	`clm1=700.0E-3 -`	Hardness coefficient of channel/contact junction.
176	`clm2=2.0 -`	Coefficient for QB contribution.
177	`clm3=1.0 -`	Coefficient for QI contribution.
178	`clm5=1.0 -`	CLM parameter.
179	`clm6=0.0 –`	CLM parameter.
180	`vover=10.0E-3 -`	Velocity overshoot effect parameter.
181	`voverp=100.0E-3 -`	Leff-dependence of velocity overshoot.
181	`vovers=0.0 -`	Modification of max velocity due to small size.
183	`voversp=1.0 -`	Modification of max velocity due to small size.
184	`wfc=0.0 F cm-2 m^-1`	Threshold voltage change due to cap change.
185	`nsubcw=0.0 –`	Substrate concentration modifier.
186	`nsubcwp=1.0 -`	Substrate concentration modifier.
187	`nsubcmax=5E18 cm-3`	Upper limit of substrate concentration.
188	`nsubcl=0.0 -`	Lgate-dependence of substrate concentration .
189	`nsubclp=1.0 -`	Lgate-dependence of substrate concentration .
190	`qme1=0.0 mV`	Vgs-dependence of quantum mechanical effect.
191	`qme2=0.0 V`	Vgs-dependence of quantum mechanical effect.
192	`qme3=0.0 m`	Minimum Tox modification.
193	`gidl1=5.0E-6 A V-3/ 2C^-1m`	Magnitude of GIDL.
194	`gidl2=1.0E6 V-2m^- 1F-3/2`	field-dependence of GIDL.
195	`gidl3=300.0E-3 -`	Vds-dependence of GIDL.
196	`gidl4=0.0 V`	Threshold for Vds dependence.
197	`gidl5=0.2E0 -`	High-field correction.
198	`gidlvb=0.5 V3`	Vb-dependence of GIDL.
199	`gleak1=10.0E3 V-3/2 s^-1`	Gate-to-channel current coefficient.
200	`gleak2=20.0E6 V^-1/ 2 m^-1`	Gate-to-channel current coefficient.
201	`gleak3=300.0E-3 -`	Gate-to-channel current coefficient.
202	`gleak4=4E0 m^-1`	Gate-to-channel current coefficient.
203	`gleak5=7.5E3 V m^-1`	G-t-C short channel correction.
204	`gleak6=250E-3 V`	G-t-C Vds-dependence correction.
205	`gleak7=1E-6 m2`	G-t-C L and W dependence correction.
206	`glksd1=1.0E-15 A m V-2`	G-t-S/D current coefficient.

© 2023 Cadence Design Systems, Inc.

207	`glksd2=5E6 V^-1 m^-1`	G-t-S/D current coefficient.
208	`glksd3=(-5E6) m^-1`	G-t-S/D current coefficient.
209	`glkb1=5E-16 A V-2`	G-t-S/D current coefficient.
210	`glkb2=1E0 m V^-1`	G-t-S/D current coefficient.
211	`glkb3=0E0 V`	G-t-S/D current coefficient.
212	`vzadd0=10.0E-3 V`	Symmetry conservation coefficient.
213	`pzadd0=5.0E-3 V`	Symmetry conservation coefficient.
214	`nftrp=10E9 V^-1`	Ratio of trap density to attenuation coefficient.
215	`nfalp=1.0E-19 cm s`	Contribution of mobility fluctuation.
216	`cit=0.0 F cm-2`	Cap caused by the interface trapped carriers.
217	`falph=1.0 sm3`	Power of f describing deviation of 1/f.
218	`tnom=27.0 C`	Temperature selected as a nominal value.
219	`dly1=100.0E-12 s`	Coefficient for delay due to diffusion of carriers.
220	`dly2=0.7E0 -`	Coefficient for delay due to conduction of carriers.
221	`dly3=0.8E-6 ?`	Coefficient for RC delay of bulk carriers.
222	`tfox=3.5E-9 m`	Front oxide thickness.
223	`tsoi=5.0E-8 m`	Silicon film thickness.
224	`xj=5.0E-8 m`	Impurity doping depth.
225	`tbox=1.1E-7 m`	Buried oxide thickness.
226	`nsubs=3.0E+17 cm-3`	SOI layer impurity concentration.
227	`nsubb=4.0E+14 cm-3`	Substrate impurity concentration.
228	`rth0=0.1 Kcm/W`	Thermal resistance.
229	`cth0=1.0E-7 Ws/(Kcm)`	Thermal capacitance.
230	`sc4=0.0 -`	SCE parameter.
231	`ptl=0.0 V^(1-PTP)`	Punchthrough parameter.
232	`ptp=3.5 -`	Punchthrough parameter.
233	`pt2=0.0 V^-1`	Punchthrough parameter.
234	`ptlp=1.0 -`	Punchthrough parameter.
235	`gdl=0.0 -`	Strength of high-field effect.
236	`gdlp=0.0 -`	Modification of channel conductance.
237	`gdld=0.0 m`	Modification of channel conductance.
238	`pt4=0.0 V^-1`	Punchthrough parameter.
239	`pt4p=1.0 -`	Punchthrough parameter.
240	`vgsmin=(-5.0) V`	Surface potential limiter.
241	`rmin=1E-3 ohm`	Minimum resistance.

© 2023 Cadence Design Systems, Inc.

242	`mueph1=25.0E3 cm2V^-1s^-1`	Phonon scattering.
243	`ldrift=1.0E-6 m`	Parameter for drift region length (drain) .
244	`ldrifts=1.0E-6 m`	Parameter for drift region length (source) .
245	`cors=0 -`	Source side resistance OFF(0)/ON(1).
246	`cord=0 -`	Drain side resistance OFF(0)/ON(1).
247	`corbulk=0 -`	Bulk resistance OFF(0)/ON(1).
248	`corbnet=0 -`	Activate body resistance net (1) or not (0).
249	`rsh=0.0 ohm`	Drain diffusion sheet resistance .
250	`novers=1E19 cm-3`	impurity concentration in overlap region.
251	`rdrmued=1.0E3`	Mobility in drift region (drain).
252	`rdrmues=1.0E3`	Mobility in drift region (source).
253	`rdrvmaxd=3.0E7`	Saturation velocity in drift region (drain).
254	`rdrvmax=3.0E7 cm/s`	Saturation velocity in drift region (drain).
255	`rdrvmaxs=3.0E7`	Saturation velocity in drift region (source).
256	`rdrmuetmp=0.0 -i`	Temperature dependence of resistance.
257	`rdrvtmp=0.0 -`	Temperature dependence of resistance.
258	`rdrdjunc=1.0E-6`	Junction depth at channel/drift region.
259	`rdrbbd=1`	Degradation of the mobility in drift region (drain).
260	`rdrbbs=1 -`	degradation of the mobility in drift region (source).
261	`rdrbbtmp=0 -`	Temperature coefficient of RDRBB.
262	`rdrvmaxw=0.0 -`	Wgate dependence of the saturation velocity in drift region.
263	`rdrvmaxwp=1.0 -`	Wgate dependence of the saturation velocity in drift region.
264	`rdrvmaxl=0.0 -`	Lgate dependence of the saturation velocity in drift region.
265	`rdrvmaxlp=1.0 -`	Lgate dependence of the saturation velocity in drift region.
266	`rdrmuel=0.0 -`	Lgate dependence of the mobility in drift region.
267	`rdrmuelp=1.0 -i`	Lgate dependence of the mobility in drift region.
268	`rbdb=50.0 ?`	Substrate resistance network.
269	`rbsb=50.0 ?`	Substrate resistance network.
270	`copt=0 -`	flag punchthrough.
271	`copspt=0 -`	flag Ps0 method for deep punchthrough.
272	`xjpt=5.0E-8 m`	Junction depth for deep punchthrough.
273	`njunc=1e20 cm-3`	Junction doping conc; deep punchthrough.

© 2023 Cadence Design Systems, Inc.

274	`mupt=0.0 m2/V/s`	Mobility for deep punchthrough.
275	`vfbpt=0.0 V`	dVfb for deep punchthrough.
276	`pslimpt=0.0 V`	Ps0 limit for deep punchthrough.
277	`rbulk0=0.0 ?`	Offset of bulk resistance.
278	`rbulkw=0.0 ?/m`	Bulk resistance per width.
279	`vfbbtp=0.12 V`	Flatband voltage for overlapped MOSFET part.
280	`cbtbn=0.0 F/m2`	N^+ poly capacitance.
281	`cbtbp=0.0 F/m2`	P^+ poly capacitance.
282	`xwdbt=0.0 m`	BT overlap width.

n

Output Parameters

nRefer to the following table for Output Parameter details:

1	`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

nRefer to the following table for Operating-Point Parameter details:

1	`rdd (?)`	Drift Resistance on Drain side.
2	`rsd (?)`	Drift Resistance on Source side.
3	`rbulk (?)`	Body Contact Resistance.
4	`idse (A)`	Drain-Source current.
5	`isuba (A)`	Substrate current.
6	`igidle (A)`	Gate-Induced Drain Leakage current.
7	`igisle (A)`	Gate-Induced Source Leakage current.
8	`igde (A)`	Gate-Drain current.
9	`igse (A)`	Gate-Source current.
10	`igbe (A)`	Gate-Substrate current.
11	`ggm (S)`	Transconductance.
12	`ggds (S)`	Channel conductance.
13	`ggmbs (S)`	Body effect (Back gate) transconductance.
14	`ggmt (S)`	Temperature transconductance.
15	`deltemp (S)`	Temperature.
16	`vone (V)`	Threshold voltage.

© 2023 Cadence Design Systems, Inc.

17	`vdsate (V)`	Saturation voltage.
18	`qge (C)`	Gate charge.
19	`qde (C)`	Drain charge.
20	`qse (C)`	Bulk charge.
21	`cggbd (F)`	g-g MOSFET capacitance.
22	`cgdbd (F)`	g-d MOSFET capacitance.
23	`cgsbd (F)`	g-s MOSFET capacitance.
24	`cbgbd (F)`	b-g MOSFET capacitance.
25	`cbsbd (F)`	b-s MOSFET capacitance.
26	`cbdbd (F)`	b-d MOSFET capacitance.
27	`cdgbd (F)`	d-g MOSFET capacitance.
28	`cddbd (F)`	d-d MOSFET capacitance.
29	`cdsbd (F)`	d-s MOSFET capacitance.
30	`ibdb (A)`	b-d Diode current.
31	`ibsb (A)`	b-s Diode current.
32	`gbd (S)`	b-d Diode conductance.
33	`gbs (S)`	b-s Diode conductance.
34	`capbdb (F)`	b-d Diode capacitance.
35	`capbsb (F)`	b-s Diode capacitance.

n

© 2023 Cadence Design Systems, Inc.

33

HiSIM_IGBT Model (hisim_igbt)

HiSIM_IGBTs (Insulated Gate Bipolar Transistors) have been developed for high voltage applications (500V and above), which require low switching power and fast switching speed. The complicated IGBT structure, which combines a bipolar junction transistor (BJT) with a MOSFET for base-current switching, imposes challenging problems on compact modeling for circuit simulation. HiSIM_IGBT model combines surface-potential-based HiSIM_HV model with a thick base BJT model and make is possible to modeling real device and complicated circuit.

This chapter contains the following information:

- Model Concepts on page 2566
- Model Usage on page 2567
  - Instance Syntax on page 2567
  - Model Syntax on page 2567
  - Sample Model Statement on page 2567
- Component Statements on page 2568

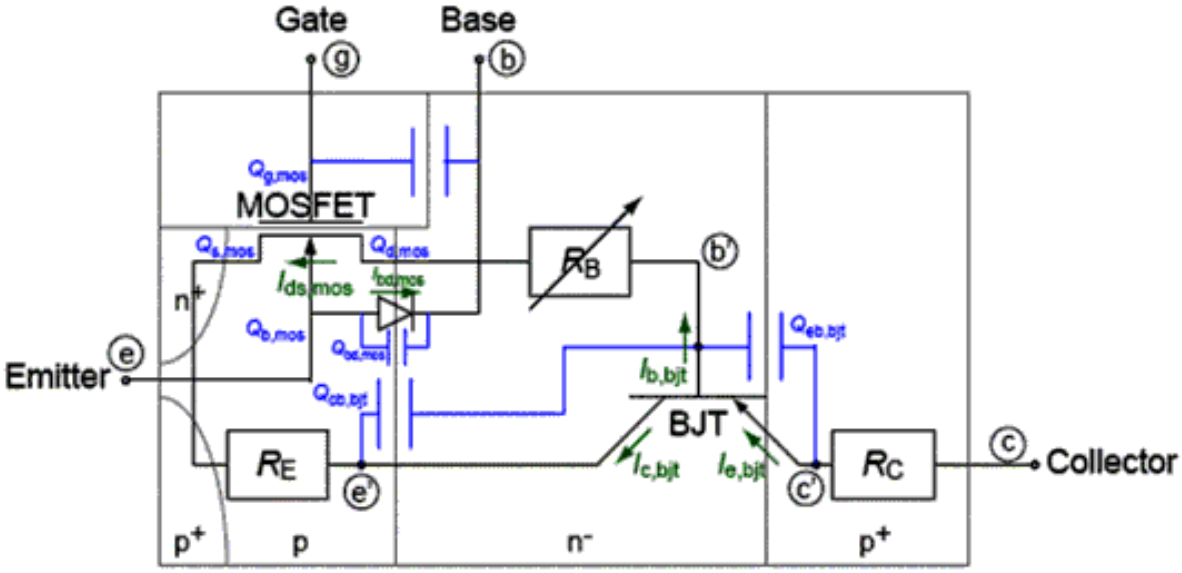
© 2023 Cadence Design Systems, Inc.

Model Concepts

While an IGBT generally has 3 terminals (Collector, Gate, and Emitter), HiSIM_IGBT considers 4 terminals (Collector, Gate, Emitter, and Base). HiSIM_IGBT has been developed based on the MOSFET-model framework, together with the bipolar-junction-transistor (BJT) model. Therefore newly developed MOSFET models as well as BJT models can be easily incorporated with future model extensions. Since the HiSIM_IGBT has been developed as a 4-terminal device, users have to treat the model as a 4-terminal device and let the base terminal float by connecting a zero-ampere current source between the base terminal and the ground, or by not connecting any circuit element to the base terminal.

The circuit diagram of HiSIM-IGBT is shown in Fig. 34.1. In addition to 4 external terminals, three internal nodes (b', c', e') are considered to describe all important features of IGBT. Between the internal and the external nodes, resistances are inserted to describe potential drops. Among the resistances the base resistance between the MOSFET part and the BJT part, determines the most IGBT characteristics. All current flows and induced charges are also considered.

Figure 33-1 Equivalent circuit for HiSIM_IGBT



A surface-potential-based model for high-voltage MOSFET HiSIM_HV 1.1.1 is applied as the MOSFET part. Its source and bulk terminals are connected together and are named as the "emitter" terminal. The drain terminal is connected to the "base" node within the IGBT framework. The surplus models of HiSIM_HV 1.1.1 for HiSIM_IGBT are inactivated by setting model parameters to zero. The activated model parts include: Drain-source current and related conductance; Intrinsic charges/capacitances; Overlap/parasitic charges/

© 2023 Cadence Design Systems, Inc.

capacitances; STI leakage current; Bulk-drain junction diode currents/conductance; Bulk-drain junction diode charges/capacitances; Binning options. The inactivated model parts include: Source/drain drift resistances; Gate resistance; Bulk resistance network; NQS effect; Substrate leakage current; Gate leakage currents; Gate-induced drain leakage currents; Noises; Self-heating effect. As some HiSIM_HV model effects are inactivated in HiSIM_IGBT model, some redundant model parameters exist there, which will be cleaned with coming version. For the effects details of MOSFET part, refer to the HiSIM_HV model.

Model Usage

Instance Syntax

HiSIM_IGBT instance need specify 4 or 5 terminals. The 4th terminal needs to be set as float by connecting a zero-ampere current source between the base terminal and the ground, or by not connecting any circuit element to the base terminal. Although selfheating is inactivate now and being testing, the 5th terminal can be set and will be treated as external selfheating node. To specify HiSIM_IGBT instance element, the Model Name has to be associated with a HiSIM_IGBT model card.

```
InstanceName c g e b ModelName parameter=value ...
```

Sample Instance Statement

```
m1 (vcc vgg vee vbb) n_ch w=0.1u l=0.21 m=1e-7
```

For more instance parameters, refer to the Reference of this model.

Model Syntax

The following syntax specifies HiSIM_IGBT model:

```
model ModelName hisim_igbt parameter=value ...
```

The third parameter, “hisim_igbt”, is the master to indicate this model card is a HiSIM_IGBT model card.

Sample Model Statement

```
model n_ch hisim_igbt coadov=1 tox=1e-7 nsubc=1e17
```

For more model parameters, refer to the Reference of this model.

© 2023 Cadence Design Systems, Inc.

Component Statements

Instance Parameters

1	`w (m)`	Gate width.
2	`l (m)`	Gate length.
3	`as (m^2)`	Area of the source junction.
4	`ad (m^2)`	Area of the drain junction.
5	`ps (m)`	Perimeter of the source junction.
6	`pd (m)`	Perimeter of the drain junction.
7	`temp (C)`	Device temperature.
8	`dtemp (K)`	Device temperature rise from ambient.
9	`nrs=1`	Number of squares of source diffusion.
10	`nrd=1`	Number of squares of drain diffusion.
11	`corbnet`	Substrate resistance network selector. Inactive in HiSIM_IGBT model.
12	`rbpb (Ohm)`	Substrate resistance network.
13	`rbpd (Ohm)`	Substrate resistance network.
14	`rbps (Ohm)`	Substrate resistance network.
15	`rbdb (Ohm)`	Substrate resistance network.
16	`rbsb (Ohm)`	Substrate resistance network.
17	`corg`	Gate-contact resistance selector. Inactive in HiSIM_IGBT model.
18	`ngcon=1.0`	Number of gate contacts.
19	`xgw=0.0 m`	Distance from gate contact to channel edge.
20	`xgl=0.0 m`	Offset of gate length due to variation in patterning.
21	`nf=1.0`	Number of gate fingers.
22	`lod=1.0e-5 m`	Length of diffusion between gate and STI.
23	`m=1`	Multiplicity factor (number of MOSFETs in parallel).

© 2023 Cadence Design Systems, Inc.

24	subld1	Parameter for impact-ionization current in the drift region.
25	subld2 ((V^(3/2))/m)	Parameter for impact-ionization current in the drift region.
26	ldrift1 (m)	Parameter for drift region length-1.
27	ldrift2 (m)	Parameter for drift region length-2.
28	lover (m)	Overlap length on the drain side.
29	lovers (m)	Overlap length on the source side.
30	loverld (m)	Overlap length on the drain side.
31	ldrift1s (m)	Parameter for drift region length-1 on the source side.
32	ldrift2s (m)	Parameter for drift region length-2 on the source side.
33	sa=0.0 m	Distance from STI edge to Gate edge.
34	sb=0.0 m	Distance from STI edge to Gate edge.
35	sd=0.0 m	Distance from Gate edge to Gate edge.
36	nsubcdfm (cm^-3)	Constant part of Nsub for DFM.
37	isnoisy=yes	Should device generate noise? Possible values are yes and no.

Model Parameters

Device type parameters

1	type=n	Transistor type. Possible values are n and p.
2	version=1.00	Model version 1.00. 1.00 is the latest version of HiSIM_IGBT.
3	corsrd=0	Contact resistances Rs and Rd selector. Inactive in HiSIM_IGBT model.
4	coiprv=0	Previous Ids is used for calculating source/drain resistance effect. Possible values are 0= no(default) and 1=yes..
5	copprv=1	Previous surface potential is used for the initial guess. Possible values are 0= no(default) and 1=yes.

© 2023 Cadence Design Systems, Inc.

6	`coadov=1`	Selector for lateral field induced and overlap charges/ capacitances being added to intrinsic ones. Possible values are 0= no and 1=yes (default).
7	`coisub=0`	Substrate current selector. Inactive in HiSIM_IGBT model.
8	`cogidl=0`	GIDL current calculation selector. Inactive in HiSIM_IGBT model.
9	`coiigs=0`	Gate current calculation selector. Inactive in HiSIM_IGBT model.
10	`coovlp=1`	Overlap capacitance calculation selector on drain side. Possible values are 0= constant overlap capacitance(default) and 1= yes.
11	`coovlps=0`	Overlap capacitance calculation selector on source side. Possible values are 0= constant overlap capacitance(default) and 1= yes.
12	`coflick=0`	1/f noise calculation selector. Inactive in HiSIM_IGBT model.
13	`coisti=0`	STI leakage current calculation selector. Possible values are 0=no(default) and 1=yes.
14	`conqs=0`	Non-quasi-static mode selector. Inactive in HiSIM_IGBT model.
15	`cothrml=0`	Thermal noise calculation selector. Inactive in HiSIM_IGBT model.
16	`tnom (C)`	Parameters measurement temperature. Default set by `options'.
17	`corg=0`	Gate-contact resistance calculation selector. Inactive in HiSIM_IGBT model.
18	`corbnet=0`	Substrate resistance network selector. Inactive in HiSIM_IGBT model.
19	`coign=0`	Induced gate and cross correlation noise calculation selector. Inactive in HiSIM_IGBT model.
20	`compatible`	Compatible with spice3, default is spectre compatible. Possible values are spectre, and spice3.
21	`alarm=none`	Forbidden operating region. Possible values are none, off, triode, sat, subth, and rev.

© 2023 Cadence Design Systems, Inc.

22	`codfm=0`	Calculation of model for DFM selector.
23	`coselfheat=0`	Calculation of self-heating model.
24	`cosym=0`	Model selector for symmetry device.

Default for instance parameters

25	`w=5e-6 m`	Default gate width.
26	`l=2e-6 m`	Default gate length.
27	`as=0 m^2`	Default area of the source junction.
28	`ad=0 m^2`	Default area of the drain junction.
29	`ps=0 m`	Default perimeter of the source junction.
30	`pd=0 m`	Default perimeter of the drain junction.
31	`temp=27 C`	Default device temperature.
32	`dtemp=0 K`	Default device temperature rise from ambient.

Basic Device Parameters

33	`tox=1e-7 m`	Physical oxide thickness.
34	`xld=3e-8 m`	Gate-overlap length.
35	`xwd=0 m`	Gate-overlap width.
36	`tpoly=2.0e-7 m`	Height of the gate poly-si for fringing capacitance on the source side.
37	`nsubc=1.0e17 cm^-3`	Substrate-impurity concentration.
38	`nsubp=1.0e17 cm^-3`	Maximum pocket concentration.
39	`rs=0.0 Ohm*m`	Source contact resistance in LDD region.
40	`rd=5.0e-3 Ohm*m`	Drain contact resistance in LDD region.
41	`vfbc=-1.0 V`	Constant part of the flat-band voltage.
42	`lp=0.0 m`	Length of the pocket penetration into the channel.

© 2023 Cadence Design Systems, Inc.

43	`xqy=0.0 m`	Distance from channel/drain junction to maximum electric field point.
44	`lover=3.0e-8 m`	Overlap length on the source side.
45	`ll=0.0`	Gate length parameter.
46	`lld=0.0 m`	Gate length parameter.
47	`lln=0.0`	Gate length parameter.
48	`wl=0.0`	Gate width parameter.
49	`wld=0.0 m`	Gate width parameter.
50	`wln=0.0`	Gate width parameter.
51	`vbi=1.0 V`	Built-in potential.
52	`nsubp0=0.0 cm^-3`	Pocket implant parameter.
53	`nsubwp=1.0`	Pocket implant parameter.
54	`lpext=1.0E-50 m`	Pocket extension.
55	`npext=1.0e17 cm^-3`	Pocket extension.
56	`rsh=0.0 V/A*m`	Source/drain diffusion sheet resistance.
57	`rshg=0.0 V/A*m`	Gate-electrode sheet resistance.
58	`rbpb=50.0 Ohm`	Substrate resistance network.
59	`rbpd=50.0 Ohm`	Substrate resistance network.
60	`rbps=50.0 Ohm`	Substrate resistance network.
61	`rbdb=50.0 Ohm`	Substrate resistance network.
62	`rbsb=50.0 Ohm`	Substrate resistance network.
63	`gbmin=1.0e-12`	Minimum conductance for substrate resistance network.
64	`xl=0 m`	Gate length offset due to mask/etch effect.
65	`xw=0 m`	Gate width offset due to mask/etch effect.
66	`xqy1=0.0 F m^{XQY2}`	Vbs dependence of Qy.
67	`xqy2=2.0`	Lgate dependence of Qy.
68	`xldld=1.0e-6 m`	Lateral diffusion of Drain under the gate.
69	`rd2=0.0 Ohm*m`	Drain contact resistance in LDD region.

© 2023 Cadence Design Systems, Inc.

70	`rd3=0.0 Ohm*m`	Drain contact resistance in LDD region.
71	`rdov11=0.0`	Dependence coeff. for overlap length.
72	`rdov12=1.0`	Dependence coeff. for overlap length.
73	`rdov13=1.0`	Dependence coeff. for overlap length.
74	`rdslp1=0.0`	LDRIFT1 dependence of resistance for CORSRD=1,3.
75	`rdict1=1.0`	LDRIFT1 dependence of resistance for CORSRD=1,3.
76	`rdslp2=1.0`	LDRIFT2 dependence of resistance for CORSRD=1,3.
77	`rdict2=0.0`	LDRIFT2 dependence of resistance for CORSRD=1,3.
78	`loverld=1.0e-6 m`	Overlap length on the drain side.
79	`lovers=3.0e-8 m`	Overlap length on the source side.
80	`ldrift1=1.0e-6 m`	Drift region length-1 on the drain side.
81	`ldrift1s=0.0 m`	Drift region length-1 on the source side.
82	`ldrift2=1.0e-6 m`	Drift region length-2 on the drain side.
83	`ldrift2s=1.0e-6 m`	Drift region length-2 on the source side.
84	`subld1=0.0`	Impact-ionization current in the drift region.
85	`subld2=0.0 (V^(3/2))/m`	Impact-ionization current in the drift region.

Temperature dependence effects

86	`eg0=1.1785 eV`	Constant bandgap.
87	`bgtmp1=9.025e-5 eV/K`	First order temperature coefficient for band gap.
88	`bgtmp2=1.0e-7 eV/K^2`	Second order temperature coefficient for band gap.
89	`rdtemp1=0.0 1/K`	Temperature-dependence of Rd.
90	`rdtemp2=0.0 1/K^2`	Temperature-dependence of Rd.
91	`rdvdtemp1=0.0 1/K`	Temperature-dependence of RDVD.
92	`rdvdtemp2=0.0 1/K^2`	Temperature-dependence of RDVD.

© 2023 Cadence Design Systems, Inc.

Quantum Mechanical Effects

93	`qme1=0.0 m/V^2`	Coefficient for quantum mechanical effect.
94	`qme2=1.0 V`	Coefficient for quantum mechanical effect.
95	`qme3=0.0 m`	Coefficient for quantum mechanical effect.
96	`kappa=3.9`	Dielectric constant for high-k stacked gate.

Poly Depletion Effects

97	`pgd1=0.0 V`	Strength of poly depletion.
98	`pgd2=1.0 V`	Threshold voltage of poly depletion.
99	`pgd3=0.8`	Vds dependence of poly depletion.
100	`pgd4=0.0`	Parameter for gate-poly depletion.

Short Channel Effects

101	`parl2=1.0e-8 m`	Depletion width of channel/contact junction.
102	`sc1=1.0 1/V`	Short-channel coefficient 1.
103	`sc2=1.0 1/V^2`	Short-channel coefficient 2.
104	`sc2b=0.0 1/V^3`	Short-channel coefficient 2 Vb dependency coefficient.
105	`sc3=0.0 m/V^2`	Short-channel coefficient 3.
106	`sc4=0.0 1/V`	Parameter for SCE.
107	`scp1=1.0 1/V`	Short-channel coefficient 1 for pocket.
108	`scp2=0.1 1/V^2`	Short-channel coefficient 2 for pocket.
109	`scp3=0.0 m/V^2`	Short-channel coefficient 3 for pocket.
110	`scp22=0.0 V^4`	Short-channel-effect modification for small Vds.
111	`scp21=0.0 V`	Short-channel-effect modification for small Vds.
112	`bs1=0.0 V^2`	Body-coefficient modification by impurity profile.
113	`bs2=0.9 V`	Body-coefficient modification by impurity profile.

© 2023 Cadence Design Systems, Inc.

Narrow channel effects

114	`wfc=0.0 m*F/cm^2`	Threshold voltage reduction.
115	`nsubcw=0.0`	Parameter for narrow channel effect.
116	`nsubcwp=1.0`	Parameter for narrow channel effect.
117	`mueph2=0.0`	Mobility reduction.
118	`w0=0.0 log(cm)`	Minimum gate width.
119	`wvthsc=0.0`	Short-channel effect at the STI edge.
120	`nsti=1.0e17 cm^-3`	Substrate-impurity concentration at the SIT edge.
121	`wsti=0.0 m`	Width of the high-field region at STI.
122	`muephw=0.0`	Phonon scattering parameter.
123	`muepwp=1.0`	Phonon scattering parameter.
124	`wvth0=0.0`	Threshold voltage shift.
125	`mueswp=1.0`	Change of surface roughness related mobility.
126	`vthsti=0.0`	Parameter for STI.
127	`muesti1=0.0`	STI Stress mobility parameter.
128	`muesti2=0.0`	STI Stress mobility parameter.
129	`muesti3=1.0`	STI Stress mobility parameter.
130	`nsubpsti1=0.0 m`	STI Stress pocket implant parameter.
131	`nsubpsti2=0.0 m`	STI Stress pocket implant parameter.
132	`nsubpsti3=1.0 m`	STI Stress pocket implant parameter.
133	`wstil=0.0`	Parameter for STI.
134	`wstilp=1.0`	Parameter for STI.
135	`scsti1=0.0`	Parameter for STI.
136	`scsti2=0.0 1/V`	Parameter for STI.
137	`scsti3=0.0 m/V`	Parameter for STI.
138	`saref=1e-6 m`	Reference distance from STI edge to Gate edge.
139	`sbref=1e-6 m`	Reference distance from STI edge to Gate edge.
140	`wstiw=0.0`	Parameter for STI.

© 2023 Cadence Design Systems, Inc.

141	`wstiwp=1.0`	Parameter for STI.
142	`vdsti=0.0`	parameter for STI.

Mobility Effects

143	`vds0=0.05 V`	Drain voltage for extracting the low-field mobility.
144	`muecb0=1.0e3 cm^2/(V*s)`	Coulomb scattering.
145	`muecb1=1.0e2 cm^2/(V*s)`	Coulomb scattering.
146	`mueph0=0.3 cm^2*(V/cm)^(Muesr1)/(V*s)`	Phonon scattering.
147	`mueph1=2.5e4`	Phonon scattering.
148	`muetmp=1.7`	Temperature dependence of phonon scattering.
149	`muesr0=2.0 cm^2*(V/cm)^(Muesr1)/(V*s)`	Surface roughness scattering.
150	`muesr1=1.0e16`	Surface roughness scattering.
151	`ndep=1.0`	Coefficient of effective electric field.
152	`ninv=0.5`	Coefficient of effective electric field.
153	`ninvd=0.0 1/V`	Modification of Vdse dependence on Eeff.
154	`bb=2.0`	High-field mobility degradation.
155	`vmax=1.0e7 cm/s`	Maximum of electron saturation velocity.
156	`vover=0.3 cm^(voverp)`	Parameter for velocity overshoot.
157	`voverp=0.3`	Lgate dependence of velocity overshoot.
158	`vovers=0.0`	Parameter for overshoot.
159	`voversp=0.0`	Parameter for overshoot.
160	`vtmp=0.0 cm/s`	Temperature dependence of the saturation velocity.
161	`muephl=0.0`	Phonon scattering parameter.
162	`mueplp=1.0`	Phonon scattering parameter.
163	`muesrl=0.0`	Surface roughness parameter.

© 2023 Cadence Design Systems, Inc.

164	`muesrw=0.0`	Change of surface roughness related mobility.
165	`mueslp=1.0`	Surface roughness parameter.
166	`ndepl=0.0`	Modification of Qb contribution for short-channel case.
167	`ndeplp=1.0`	Modification of Qb contribution for short-channel case.

Small size parameters

168	`wl1=0.0`	Threshold voltage shift of STI leakage due to small size effect.
169	`wl1p=1.0`	Threshold voltage shift of STI leakage due to small size effect.
170	`wl2=0.0`	Threshold voltage shift due to small size effect.
171	`wl2p=1.0`	Threshold voltage shift due to small size effect.
172	`muephs=0.0`	Mobility modification due to small size.
173	`muepsp=1.0`	Mobility modification due to small size.

Channel Length Modulation Effects

174	`clm1=50e-3`	First parameter for CLM.
175	`clm2=2.0 1/m`	Second parameter for CLM.
176	`clm3=1.0`	Third parameter for CLM.
177	`clm4=5.0e-4`	Smoothing coefficient for gds.
178	`clm5=1.0`	Effect of pocket implantation.
179	`clm6=0.0`	Effect of pocket implantation.

Substrate Current Effects

180	`sub1=50e-3 1/V`	First parameter for Isub.

© 2023 Cadence Design Systems, Inc.

181	`sub2=1.0e2 V`	Second parameter for Isub.
182	`svgs=0.8`	Substrate current dependence on Vgs.
183	`svbs=0.5`	Substrate current dependence on Vbs.
184	`svbsl=0.0`	Lgate dependence of SVBS.
185	`svds=0.8`	Substrate current dependence on Vds.
186	`slg=3.0e-8`	Substrate current dependence on Lgate.
187	`sub1l=2.5e-3`	Lgate dependence of SUB1.
188	`sub2l=2.0e-6`	Lgate dependence of SUB2.
189	`fn1=50.0`	Coefficient of Fowler-Nordheim-current contribution.
190	`fn2=1.7e-4`	Coefficient of Fowler-Nordheim-current contribution.
191	`fn3=0.0`	Coefficient of Fowler-Nordheim-current contribution.
192	`fvbs=1.2e-2`	Modification of Vbs dependence.
193	`svgsl=0.0`	Lgate dependence of SVGS.
194	`svgslp=1.0`	Lgate dependence of SVGS.
195	`svgswp=1.0`	Wgate dependence of SVGS.
196	`svgsw=0.0`	Wgate dependence of SVGS.
197	`svbslp=1.0`	Lgate dependence of SVBS.
198	`slgl=0.0`	Substrate current dependence on Lgate.
199	`slglp=1.0`	Substrate current dependence on Lgate.
200	`sub1lp=1.0`	Lgate dependence of SUB1.
201	`ibpc1=0.0`	Impact-ionization induced bulk potential change.
202	`ibpc2=0.0`	Impact-ionization induced bulk potential change.

© 2023 Cadence Design Systems, Inc.

Gate Current Effects

203	`glpart1=0.5`	Partitioning of gate current.
204	`gleak1=50.0 A/(V^(3/2)*c^(1/2))`	First gate current coefficient.
205	`gleak2=1.0e7 1/(V^(1/2)*c^(3/2)*m)`	Second gate current coefficient.
206	`gleak3=6.0e-2`	Third gate current coefficient.
207	`gleak4=4.0`	Parameter for gate current.
208	`gleak5=7.5e3`	Parameter for gate current.
209	`glksd1=1.0e-15`	Parameter for gate current.
210	`glksd2=5e6`	Parameter for gate current.
211	`glksd3=-5e6`	Parameter for gate current.
212	`glkb0=0.0 V`	Parameter for gate current.
213	`glkb1=5.0e-16`	Parameter for gate current.
214	`glkb2=1.0`	Parameter for gate current.
215	`igtemp1=0.0`	Temperature dependence of gate current.
216	`igtemp2=0.0 1/K`	Temperature dependence of gate current.
217	`igtemp3=0.0 1/K^2`	Temperature dependence of gate current.
218	`gleak6=0.25 V`	Parameter for gate current.
219	`gleak7=1.0e-6 m^2`	Parameter for gate current.
220	`glkb3=0.0 V`	Parameter for gate current.
221	`egig=0.0 V`	Parameter for gate current.

GIDL Current Effects

222	`gidl1=2.0 A*m/(V^(3/2)*c^(1/2))`	First parameter for GIDL.
223	`gidl2=3.0E7 1/(V^(1/2)*c^(3/2)*m)`	Second parameter for GIDL.

© 2023 Cadence Design Systems, Inc.

224	`gidl3=0.9`	Third parameter for GIDL.
225	`gidl4=0.9`	Parameter for GIDL.
226	`gidl5=0.2`	Parameter for GIDL.

Noise 1/f Effects

227	`nfalp=1.0e-19`	Flicker (1/f) noise contribution of the mobility fluctuation.
228	`falph=1.0`	Parameter for 1/f noise.
229	`nftrp=1.0e10`	Flicker (1/f) noise ratio of trap density to attenuation coefficient.
230	`cit=0.0`	Flicker (1/f) noise interface trapped carriers capacitance.

Subthreshold swing parameters

231	`pthrou=0.0`	Modify subthreshold slope.
232	`pthroub=0.0 1/V`	Modify subthreshold slope.

NQS parameters

233	`dly1=1.0e-10`	Parameter for transit time.
234	`dly2=0.7`	Parameter for transit time.
235	`dly3=8.0e-7 Ohm`	Parameter for transforming bulk charge.
236	`dlyov=0.0 Ohm`	Parameter for transforming overlap charge.

Symmetry for short-channel mosfet

237	`vzadd0=1.0e-2 V`	Vzadd at Vds=0.
238	`pzadd0=5.0e-3 V`	Pzadd at Vds=0.

© 2023 Cadence Design Systems, Inc.

P-N junctions parameters

239	`js0=5.0e-7 A/m^2 J`	unction saturation current density.
240	`js0sw=0.0 A/m`	Side-wall saturation current density.
241	`nj=1.0`	Junction emission coefficient.
242	`njsw=1.0`	Junction emission coefficient (sidewall).
243	`xti=2.0`	Junction saturation current temperature exponent coefficient.
244	`cj=5.0e-4 F/m^2`	Bottom junction capacitance per unit area at zero bias.
245	`cjsw=5e-10 F/m`	Source/drain sidewall junction capacitance per unit length at zero bias.
246	`cjswg=5e-10 F/m`	Source/drain sidewall junction capacitance grading coefficient per unit length at zero bias.
247	`tcjbd=0.0`	Temperature dependence of czbd.
248	`tcjbdsw=0.0`	Temperature dependence of czbdsw.
249	`tcjbdswg=0.0`	Temperature dependence of czbdswg.
250	`tcjbs=0.0`	Temperature dependence of czbs.
251	`tcjbssw=0.0`	Temperature dependence of czbssw.
252	`tcjbsswg=0.0`	Temperature dependence of czbsswg.
253	`mj=0.5`	Bulk junction bottom grading coefficient.
254	`mjsw=0.33`	Source/drain sidewall junction capacitance grading coefficient.
255	`mjswg=0.33`	Bottom junction capacitance grading coefficient.
256	`pb=1.0 V`	Bottom junction build-in potential.
257	`pbsw=1.0 V`	Source/drain sidewall junction build-in potential.
258	`pbswg=1.0 V`	Source/drain gate sidewall junction build-in potential.
259	`vdiffj=6.0e-4 V`	Threshold voltage for S/D junction diode.
260	`xti2=0.0`	Temperature coefficient.
261	`cisb=0.0`	Reverse bias saturation current.
262	`cvb=0.0`	Bias dependence coefficient of cisb.

© 2023 Cadence Design Systems, Inc.

263	`ctemp=0.0`	Temperature coefficient.
264	`cisbk=0.0 A`	Reverse bias saturation current.
265	`cvbk=0.0`	Bias dependence coefficient of cisb.
266	`divx=0.0 1/V`	Parameter for junction.

Overlap capacitance parameters

267	`cgso=0.0 F/m`	Gate-source overlap capacitance.
268	`cgdo=0.0 F/m`	Gate-source overlap capacitance.
269	`cgbo=0.0 F/m`	Gate-source overlap capacitance.
270	`ovslp=2.0e-8`	Parameter for overlap capacitance.
271	`ovmag=500.0`	Parameter for overlap capacitance.
272	`vfbover=-0.5 V`	Flat-band voltage in overlap region.
273	`nover=1.0e14 cm^-3`	Impurity concentration in overlap region.
274	`novers=0.0 cm^-3`	Impurity concentration in overlap region.

Smoothing coefficient between linear and saturation

275	`ddltmax=1.0`	Coefficient of effective electric field.
276	`ddltslp=0.0`	Lgate dependence of smoothing coefficient.
277	`ddltict=10.0`	Lgate dependence of smoothing coefficient.

DFM parameters

278	`mphdfm=-0.3`	NSUBCDFM dependence of phonon scattering for DFM.

© 2023 Cadence Design Systems, Inc.

Operating region warning control parameters

279	`warn=off`	Parameter to turn warnings on and off. Possible values are off and on.
280	`bvd (V)`	Drain diode breakdown voltage.
281	`bvs (V)`	Source diode breakdown voltage.
282	`bvj (V)`	Junction reverse breakdown voltage, take effect when bvd and bvs not given.
283	`vbox=3e9*tox V`	Oxide breakdown voltage.

Mismatch parameters

284	`mvtwl=0.0 V*m`	Threshold mismatch area dependence.
285	`mvt0=0.0 V`	Threshold mismatch intercept.
286	`mbewl=0.0 m`	Beta mismatch area dependence.
287	`mbe0=0.0`	Beta mismatch intercept.
288	`mvtwl2=0.0 V*m^1.5`	Threshold mismatch area square dependence.
289	`mismatchmod=0`	Mismatch mode selector. The available modes are 0, 1, 2 and 3.
290	`mismatchdist=0 m`	Mismatch Distance.

LDMOS special parameters

291	`rdvg11=0.0`	Vgs dependence of RD.
292	`rdvg12=1.0e2`	Vgs dependence of RD.
293	`vbsmin=-10.5 V`	Minimum back bias voltage to be treated in hsmigbteval.
294	`rth0=0.1 Kcm/W`	Thermal resistance.
295	`cth0=1.0e-7 Ws/Kcm`	Thermal capacitance.

© 2023 Cadence Design Systems, Inc.

296	`qdftvd=1.0`	Qdrift Vd dependence.
297	`rdvd=7.0e-2`	Vds dependence of RD.
298	`rdvb=0.0`	Vbs dependence of RD.
299	`rd20=0.0`	RD23 boundary.
300	`rd21=1.0`	Vds dependence of RD.
301	`rd22=0.0`	Vbs dependence of RD.
302	`rd22d=0.0`	Vbs dependence of RD.
303	`rd23=5e-3`	Modification of RD.
304	`rd24=0.0`	Vgs dependence of RD.
305	`rd25=0.0`	Vgs dependence of RD.
306	`rd26=0.2`	Smoothing Qover at depletion/inversion transition.
307	`qovsm=0.2`	Smoothing Qover at depletion/inversion transition.
308	`rdvdl=0.0`	Lgate dependence of RD.
309	`rdvdlp=1.0`	Lgate dependence of RD.
310	`rdvds=0.0`	Small size dependence of RD.
311	`rdvdsp=1.0`	Small size dependence of RD.
312	`rd23l=0.0`	Lgate dependence of RD21 boundary.
313	`rd23lp=1.0`	Lgate dependence of RD21 boundary.
314	`rd23s=0.0`	Small size dependence of RD21.
315	`rd23sp=1.0`	Small size dependence of RD21.
316	`rds=0.0`	Small size dependence of RD.
317	`rdsp=1.0`	Small size dependence of RD.
318	`ldrift=1.0e-6`	Length of drift region.
319	`rth0r=0.0`	Heat radiation for SHE.
320	`rth0w=0.0`	Width-dependence of RTH0.
321	`rth0wp=1.0`	Width-dependence of RTH0.
322	`rth0nf=0.0`	Nf-dependence of RTH0.
323	`cvdsover=0.0`	Modification of the Cgg spikes for Vds is not zero.
324	`powrat=1.0`	Thermal dissipation.

© 2023 Cadence Design Systems, Inc.

Parameters for bjt part

325	`bjtninj=0`	Electron injection into the depletion layer.
326	`bjtninjmax=1.0`	Parameter for Wdep.
327	`bjtwdepmax=1.0`	Parameter for Wdep.
328	`bjtmuep=50.0 cm^2/(V*s)`	Hole mobility in the quasi-neutral region.
329	`bjtmuen=100.0 cm^2/(V*s)`	Electron mobility in the quasi-neutral region.
330	`bjtmueqn=1.0`	Parameter for mobility.
331	`bjttaue=3.0e-5 s`	Basic lifetime in the emitter.
332	`bjttaub=1.0e-5 s`	Basic lifetime in the base.
333	`bjttauc=3.0e-5 s`	Basic lifetime in the collector.
334	`bjtnref=1.0e17 cm^-3`	Reference doping concentration.
335	`bjtgminc=0`	Coefficient for minimum conductance.
336	`bjtgmine=0`	Coefficient for minimum conductance.
337	`bjtldec=1.0`	Parameter for excess carrier distribution.
338	`bjtpmin=1.0e14 cm^-3`	Minimum carrier density in the base.
339	`bjtrb=1.0`	Coefficient for base resistance.
340	`bjtrbvg11=0`	Gate-voltage dependence on RBase.
341	`bjtrbvg12=20.0 V`	Gate-voltage dependence on RBase.
342	`bjtrc=1.0e4 Ohm*m`	Collector resistance.
343	`bjtre=0 Ohm*m`	Emitter resistance.
344	`bjtqdep=1.0`	Coefficient for Qdep.
345	`bjtqex=1.0`	Coefficient for Qexcess.
346	`bjtne=1.0e17 cm^-3`	Emitter impurity concentration.

© 2023 Cadence Design Systems, Inc.

347	`bjtnb=1.0e14 cm^-3`	Base impurity concentration.
348	`bjtnc=1.0e18 cm^-3`	Base impurity concentration.
349	`bjtwb=1.0e-4 m`	Base width.
350	`bjtwhalfcell=2.0e-6 m`	Half cell width.

Auto Model Selector parameters

351	`wmax=1 m`	Maximum channel width for which the model is valid.
352	`wmin=0 m`	Minimum channel width for which the model is valid.
353	`lmax=1 m`	Maximum channel length for which the model is valid.
354	`lmin=0 m`	Minimum channel length for which the model is valid.

Safe Operating Areas Parameters

355	`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
356	`vgd_max=infinity V`	Maximum allowed voltage cross drain and gate.
357	`vgs_max=infinity V`	Maximum allowed voltage cross source/bulk and gate.
358	`vbd_max=infinity V`	Maximum allowed voltage cross drain/source and bulk.

Binning model parameters

359	`lbinn=1.0`	L modulation coefficient for binning.
360	`wbinn=1.0`	W modulation coefficient for binning.

© 2023 Cadence Design Systems, Inc.

361	`lvmax=0.0 cm/s`	Length dependence of vmax.
362	`lbgtmp1=0.0 eV/K`	Length dependence of bgtmp1.
363	`lbgtmp2=0.0 eV/K^2`	Length dependence of bgtmp2.
364	`leg0=0.0 eV`	Length dependence of eg0.
365	`lnovers=0.0 cm^-3`	Length dependence of novers.
366	`lvfbover=0.0 V`	Length dependence of vfbover.
367	`lnover=0.0 cm^-3`	Length dependence of nover.
368	`lwl2=0.0`	Length dependence of wl2.
369	`lvfbc=0.0 V`	Length dependence of vfbc.
370	`lnsubc=0.0 cm^-3`	Length dependence of nsubc.
371	`lnsubp=0.0 cm^-3`	Length dependence of nsubp.
372	`lscp1=0.0 1/V`	Length dependence of scp1.
373	`lscp2=0.0 1/V^2`	Length dependence of scp2.
374	`lscp3=0.0 m/V^2`	Length dependence of scp3.
375	`lsc1=0.0 1/V`	Length dependence of sc1.
376	`lsc2=0.0 1/V^2`	Length dependence of sc2.
377	`lsc3=0.0 m/V^2`	Length dependence of sc3.
378	`lpgd1=0.0 V`	Length dependence of pgd1.
379	`lpgd3=0.0`	Length dependence of pgd3.
380	`lndep=0.0`	Length dependence of ndep.
381	`lninv=0.0`	Length dependence of ninv.
382	`lmuecb0=0.0 cm^2/(V*s)`	Length dependence of muecb0.
383	`lmuecb1=0.0 cm^2/(V*s)`	Length dependence of muecb1.
384	`lmueph1=0.0`	Length dependence of mueph1.
385	`lvtmp=0.0 cm/s`	Length dependence of vtmp.
386	`lwvth0=0.0`	Length dependence of wvth0.

© 2023 Cadence Design Systems, Inc.

387	`lmuesr1=0.0`	Length dependence of muesr1.
388	`lmuetmp=0.0`	Length dependence of muetmp.
389	`lsub1=0.0 1/V`	Length dependence of sub1.
390	`lsub2=0.0 V`	Length dependence of sub2.
391	`lsvds=0.0`	Length dependence of svds.
392	`lsvbs=0.0`	Length dependence of svbs.
393	`lsvgs=0.0`	Length dependence of svgs.
394	`lfn1=0.0`	Length dependence of fn1.
395	`lfn2=0.0`	Length dependence of fn2.
396	`lfn3=0.0`	Length dependence of fn3.
397	`lfvbs=0.0`	Length dependence of fvbs.
398	`lnsti=0.0 cm^-3`	Length dependence of nsti.
399	`lwsti=0.0 m`	Length dependence of wsti.
400	`lscsti1=0.0`	Length dependence of scsti1.
401	`lscsti2=0.0 1/V`	Length dependence of scsti2.
402	`lvthsti=0.0`	Length dependence of vthsti.
403	`lmuesti1=0.0`	Length dependence of muesti1.
404	`lmuesti2=0.0`	Length dependence of muesti2.
405	`lmuesti3=0.0`	Length dependence of muesti3.
406	`lnsubpsti1=0.0 m`	Length dependence of nsubpsti1.
407	`lnsubpsti2=0.0 m`	Length dependence of nsubpsti2.
408	`lnsubpsti3=0.0 m`	Length dependence of nsubpsti3.
409	`lcgso=0.0 F/m`	Length dependence of cgso.
410	`lcgdo=0.0 F/m`	Length dependence of cgdo.
411	`ljs0=0.0 A/m^2`	Length dependence of js0.
412	`ljs0sw=0.0 A/m`	Length dependence of js0sw.
413	`lnj=0.0`	Length dependence of nj.
414	`lcisbk=0.0 A`	Length dependence of cisbk.
415	`lclm1=0.0`	Length dependence of clm1.

© 2023 Cadence Design Systems, Inc.

416	`lclm2=0.0 1/m`	Length dependence of clm2.
417	`lclm3=0.0`	Length dependence of clm3.
418	`lwfc=0.0 m*F/cm^2`	Length dependence of wfc.
419	`lgidl1=0.0 A*m/(V^(3/2)*c^(1/2))`	Length dependence of gidl1.
420	`lgidl2=0.0 1/(V^(1/2)*c^(3/2)*m)`	Length dependence of gidl2.
421	`lgleak1=0.0 A/(V^(3/2)*c^(1/2))`	Length dependence of gleak1.
422	`lgleak2=0.0 1/(V^(1/2)*c^(3/2)*m)`	Length dependence of gleak2.
423	`lgleak3=0.0`	Length dependence of gleak3.
424	`lgleak6=0.0 V`	Length dependence of gleak6.
425	`lglksd1=0.0`	Length dependence of glksd1.
426	`lglksd2=0.0`	Length dependence of glksd2.
427	`lglkb1=0.0`	Length dependence of glkb1.
428	`lglkb2=0.0`	Length dependence of glkb2.
429	`lnftrp=0.0`	Length dependence of nftrp.
430	`lnfalp=0.0`	Length dependence of nfalp.
431	`lpthrou=0.0`	Length dependence of pthrou.
432	`lvdiffj=0.0 V`	Length dependence of vdiffj.
433	`libpc1=0.0`	Length dependence of ibpc1.
434	`libpc2=0.0`	Length dependence of ibpc2.
435	`wvmax=0.0 cm/s`	Width dependence of vmax.
436	`wbgtmp1=0.0 eV/K`	Width dependence of bgtmp1.
437	`wbgtmp2=0.0 eV/K^2`	Width dependence of bgtmp2.
438	`weg0=0.0 eV`	Width dependence of eg0.
439	`wnovers=0.0 cm^-3`	Width dependence of novers.

© 2023 Cadence Design Systems, Inc.

440	`wvfbover=0.0 V`	Width dependence of vfbover.
441	`wnover=0.0 cm^-3`	Width dependence of nover.
442	`wwl2=0.0`	Width dependence of wl2.
443	`wvfbc=0.0 V`	Width dependence of vfbc.
444	`wnsubc=0.0 cm^-3`	Width dependence of nsubc.
445	`wnsubp=0.0 cm^-3`	Width dependence of nsubp.
446	`wscp1=0.0 1/V`	Width dependence of scp1.
447	`wscp2=0.0 1/V^2`	Width dependence of scp2.
448	`wscp3=0.0 m/V^2`	Width dependence of scp3.
449	`wsc1=0.0 1/V`	Width dependence of sc1.
450	`wsc2=0.0 1/V^2`	Width dependence of sc2.
451	`wsc3=0.0 m/V^2`	Width dependence of sc3.
452	`wpgd1=0.0 V`	Width dependence of pgd1.
453	`wpgd3=0.0`	Width dependence of pgd3.
454	`wndep=0.0`	Width dependence of ndep.
455	`wninv=0.0`	Width dependence of ninv.
456	`wmuecb0=0.0 cm^2/(V*s)`	Width dependence of muecb0.
457	`wmuecb1=0.0 cm^2/(V*s)`	Width dependence of muecb1.
458	`wmueph1=0.0`	Width dependence of mueph1.
459	`wvtmp=0.0 cm/s`	Width dependence of vtmp.
460	`wwvth0=0.0`	Width dependence of wvth0.
461	`wmuesr1=0.0`	Width dependence of muesr1.
462	`wmuetmp=0.0`	Width dependence of muetmp.
463	`wsub1=0.0 1/V`	Width dependence of sub1.
464	`wsub2=0.0 V`	Width dependence of sub2.
465	`wsvds=0.0`	Width dependence of svds.
466	`wsvbs=0.0`	Width dependence of svbs.

© 2023 Cadence Design Systems, Inc.

467	`wsvgs=0.0`	Width dependence of svgs.
468	`wfn1=0.0`	Width dependence of fn1.
469	`wfn2=0.0`	Width dependence of fn2.
470	`wfn3=0.0`	Width dependence of fn3.
471	`wfvbs=0.0`	Width dependence of fvbs.
472	`wnsti=0.0 cm^-3`	Width dependence of nsti.
473	`wwsti=0.0 m`	Width dependence of wsti.
474	`wscsti1=0.0`	Width dependence of scsti1.
475	`wscsti2=0.0 1/V`	Width dependence of scsti2.
476	`wvthsti=0.0`	Width dependence of vthsti.
477	`wmuesti1=0.0`	Width dependence of muesti1.
478	`wmuesti2=0.0`	Width dependence of muesti2.
479	`wmuesti3=0.0`	Width dependence of muesti3.
480	`wnsubpsti1=0.0 m`	Width dependence of nsubpsti1.
481	`wnsubpsti2=0.0 m`	Width dependence of nsubpsti2.
482	`wnsubpsti3=0.0 m`	Width dependence of nsubpsti3.
483	`wcgso=0.0 F/m`	Width dependence of cgso.
484	`wcgdo=0.0 F/m`	Width dependence of cgdo.
485	`wjs0=0.0 A/m^2`	Width dependence of js0.
486	`wjs0sw=0.0 A/m`	Width dependence of js0sw.
487	`wnj=0.0`	Width dependence of nj.
488	`wcisbk=0.0 A`	Width dependence of cisbk.
489	`wclm1=0.0`	Width dependence of clm1.
490	`wclm2=0.0 1/m`	Width dependence of clm2.
491	`wclm3=0.0`	Width dependence of clm3.
492	`wwfc=0.0 m*F/cm^2`	Width dependence of wfc.
493	`wgidl1=0.0 A*m/(V^(3/2)*c^(1/2))`	Width dependence of gidl1.
494	`wgidl2=0.0 1/(V^(1/2)*c^(3/2)*m)`	

© 2023 Cadence Design Systems, Inc.

		Width dependence of gidl2.
495	`wgleak1=0.0 A/(V^(3/2)*c^(1/2))`	Width dependence of gleak1.
496	`wgleak2=0.0 1/(V^(1/2)*c^(3/2)*m)`	Width dependence of gleak2.
497	`wgleak3=0.0`	Width dependence of gleak3.
498	`wgleak6=0.0 V`	Width dependence of gleak6.
499	`wglksd1=0.0`	Width dependence of glksd1.
500	`wglksd2=0.0`	Width dependence of glksd2.
501	`wglkb1=0.0`	Width dependence of glkb1.
502	`wglkb2=0.0`	Width dependence of glkb2.
503	`wnftrp=0.0`	Width dependence of nftrp.
504	`wnfalp=0.0`	Width dependence of nfalp.
505	`wpthrou=0.0`	Width dependence of pthrou.
506	`wvdiffj=0.0 V`	Width dependence of vdiffj.
507	`wibpc1=0.0`	Width dependence of ibpc1.
508	`wibpc2=0.0`	Width dependence of ibpc2.
509	`pvmax=0.0 cm/s`	Cross-term dependence of vmax.
510	`pbgtmp1=0.0 eV/K`	Cross-term dependence of bgtmp1.
511	`pbgtmp2=0.0 eV/K^2`	Cross-term dependence of bgtmp2.
512	`peg0=0.0 eV`	Cross-term dependence of eg0.
513	`pnovers=0.0 cm^-3`	Cross-term dependence of novers.
514	`pvfbover=0.0 V`	Cross-term dependence of vfbover.
515	`pnover=0.0 cm^-3`	Cross-term dependence of nover.
516	`pwl2=0.0`	Cross-term dependence of wl2.
517	`pvfbc=0.0 V`	Cross-term dependence of vfbc.
518	`pnsubc=0.0 cm^-3`	Cross-term dependence of nsubc.
519	`pnsubp=0.0 cm^-3`	Cross-term dependence of nsubp.

© 2023 Cadence Design Systems, Inc.

520	`pscp1=0.0 1/V`	Cross-term dependence of scp1.
521	`pscp2=0.0 1/V^2`	Cross-term dependence of scp2.
522	`pscp3=0.0 m/V^2`	Cross-term dependence of scp3.
523	`psc1=0.0 1/V`	Cross-term dependence of sc1.
524	`psc2=0.0 1/V^2`	Cross-term dependence of sc2.
525	`psc3=0.0 m/V^2`	Cross-term dependence of sc3.
526	`ppgd1=0.0 V`	Cross-term dependence of pgd1.
527	`ppgd3=0.0`	Cross-term dependence of pgd3.
528	`pndep=0.0`	Cross-term dependence of ndep.
529	`pninv=0.0`	Cross-term dependence of ninv.
530	`pmuecb0=0.0 cm^2/(V*s)`	Cross-term dependence of muecb0.
531	`pmuecb1=0.0 cm^2/(V*s)`	Cross-term dependence of muecb1.
532	`pmueph1=0.0`	Cross-term dependence of mueph1.
533	`pvtmp=0.0 cm/s`	Cross-term dependence of vtmp.
534	`pwvth0=0.0`	Cross-term dependence of wvth0.
535	`pmuesr1=0.0`	Cross-term dependence of muesr1.
536	`pmuetmp=0.0`	Cross-term dependence of muetmp.
537	`psub1=0.0 1/V`	Cross-term dependence of sub1.
538	`psub2=0.0 V`	Cross-term dependence of sub2.
539	`psvds=0.0`	Cross-term dependence of svds.
540	`psvbs=0.0`	Cross-term dependence of svbs.
541	`psvgs=0.0`	Cross-term dependence of svgs.
542	`pfn1=0.0`	Cross-term dependence of fn1.
543	`pfn2=0.0`	Cross-term dependence of fn2.
544	`pfn3=0.0`	Cross-term dependence of fn3.
545	`pfvbs=0.0`	Cross-term dependence of fvbs.
546	`pnsti=0.0 cm^-3`	Cross-term dependence of nsti.

© 2023 Cadence Design Systems, Inc.

547	`pwsti=0.0 m`	Cross-term dependence of wsti.
548	`pscsti1=0.0`	Cross-term dependence of scsti1.
549	`pscsti2=0.0 1/V`	Cross-term dependence of scsti2.
550	`pvthsti=0.0`	Cross-term dependence of vthsti.
551	`pmuesti1=0.0`	Cross-term dependence of muesti1.
552	`pmuesti2=0.0`	Cross-term dependence of muesti2.
553	`pmuesti3=0.0`	Cross-term dependence of muesti3.
554	`pnsubpsti1=0.0 m`	Cross-term dependence of nsubpsti1.
555	`pnsubpsti2=0.0 m`	Cross-term dependence of nsubpsti2.
556	`pnsubpsti3=0.0 m`	Cross-term dependence of nsubpsti3.
557	`pcgso=0.0 F/m`	Cross-term dependence of cgso.
558	`pcgdo=0.0 F/m`	Cross-term dependence of cgdo.
559	`pjs0=0.0 A/m^2`	Cross-term dependence of js0.
560	`pjs0sw=0.0 A/m`	Cross-term dependence of js0sw.
561	`pnj=0.0`	Cross-term dependence of nj.
562	`pcisbk=0.0 A`	Cross-term dependence of cisbk.
563	`pclm1=0.0`	Cross-term dependence of clm1.
564	`pclm2=0.0 1/m`	Cross-term dependence of clm2.
565	`pclm3=0.0`	Cross-term dependence of clm3.
566	`pwfc=0.0 m*F/cm^2`	Cross-term dependence of wfc.
567	`pgidl1=0.0 A*m/(V^(3/2)*c^(1/2))`	Cross-term dependence of gidl1.
568	`pgidl2=0.0 1/(V^(1/2)*c^(3/2)*m)`	Cross-term dependence of gidl2.
569	`pgleak1=0.0 A/(V^(3/2)*c^(1/2))`	Cross-term dependence of gleak1.
570	`pgleak2=0.0 1/(V^(1/2)*c^(3/2)*m)`	Cross-term dependence of gleak2.
571	`pgleak3=0.0`	Cross-term dependence of gleak3.

© 2023 Cadence Design Systems, Inc.

572	`pgleak6=0.0 V`	Cross-term dependence of gleak6.
573	`pglksd1=0.0`	Cross-term dependence of glksd1.
574	`pglksd2=0.0`	Cross-term dependence of glksd2.
575	`pglkb1=0.0`	Cross-term dependence of glkb1.
576	`pglkb2=0.0`	Cross-term dependence of glkb2.
577	`pnftrp=0.0`	Cross-term dependence of nftrp.
578	`pnfalp=0.0`	Cross-term dependence of nfalp.
579	`ppthrou=0.0`	Cross-term dependence of pthrou.
580	`pvdiffj=0.0 V`	Cross-term dependence of vdiffj.
581	`pibpc1=0.0`	Cross-term dependence of ibpc1.
582	`pibpc2=0.0`	Cross-term dependence of ibpc2.

© 2023 Cadence Design Systems, Inc.

Operating Point Parameters

1	`shetemp (C)`	Temperature rise due to self-heating.
2	`reversed`	Reverse mode indicator. Possible values are `yes` and `no`.
3	`ids (A)`	Resistive drain-to-source current.
4	`vgs (V)`	Gate-source voltage.
5	`vds (V)`	Drain-source voltage.
6	`vbs (V)`	Bulk-source voltage.
7	`vth (V)`	Threshold voltage.
8	`vdsat (V)`	Drain-source saturation voltage.
9	`gm (S)`	Common-source transconductance.
10	`gds (S)`	Common-source output conductance.
11	`gmbs (S)`	Body-transconductance.
12	`qb (Coul)`	Total bulk charge.
13	`qd (Coul)`	Total drain charge.
14	`qg (Coul)`	Total gate charge.
15	`qs (Coul)`	Total source charge.
16	`qb_itr (Coul)`	Intrinsic bulk charge.
17	`qd_itr (Coul)`	Intrinsic drain charge.
18	`qg_itr (Coul)`	Intrinsic gate charge.
19	`qs_itr (Coul)`	Intrinsic source charge.
20	`qdp (Coul)`	Total external drain charge.
21	`qsp (Coul)`	Total external source charge.
22	`cjd (F)`	Drain-bulk junction capacitance.
23	`cjs (F)`	Source-bulk junction capacitance.
24	`cgg (F)`	Intrinsic dQg_dVg.
25	`cgd (F)`	dQg_dVd.
26	`cgs (F)`	dQg_dVs.
27	`cgb (F)`	dQg_dVb.
28	`cdg (F)`	dQd_dVg.

© 2023 Cadence Design Systems, Inc.

29	`cdd (F)`	Intrinsic dQd_dVd.
30	`cds (F)`	dQd_dVs.
31	`cdb (F)`	dQd_dVb.
32	`csg (F)`	dQs_dVg.
33	`csd (F)`	dQs_dVd.
34	`css (F)`	Intrinsic dQs_dVs.
35	`csb (F)`	dQs_dVb.
36	`cbg (F)`	dQb_dVg.
37	`cbd (F)`	dQb_dVd.
38	`cbs (F)`	dQb_dVs.
39	`cbb (F)`	Intrinsic dQb_dVb.
40	`cdd_tot (F)`	Total dQd_dVd.
41	`cgg_tot (F)`	Total dQg_dVg.
42	`css_tot (F)`	Total dQs_dVs.
43	`cbb_tot (F)`	Total dQb_dVb.
44	`id (A)`	Resistive drain current.
45	`ig (A)`	Gate current.
46	`is (A)`	Resistive source current.
47	`ibulk (A)`	Resistive bulk current.
48	`pwr (W)`	Power at operating point.
49	`ps0 (V)`	Surface potential at source side.
50	`psl (V)`	Surface potential at drain side.
51	`pds (V)`	Delta surface potential between psl and ps0.
52	`isub (A)`	Substrate current Isub.
53	`gbds (S)`	Substrate trans conductance (dIsub/dVds).
54	`gbgs (S)`	Substrate trans conductance (dIsub/dVgs).
55	`gbbs (S)`	Substrate transconductance (dIsub/dVbs).
56	`igate (A)`	Gate current due to tunneling.
57	`igates (A)`	Tunneling current from gate to source.

© 2023 Cadence Design Systems, Inc.

58	`igateb (A)`	Tunneling current from gate to bulk.
59	`igated (A)`	Tunneling current from gate to drain.
60	`igisl (A)`	Gate-induced source leakage current.
61	`igidl (A)`	Gate-induced drain leakage current.
62	`ibs (A)`	Source-bulk diode current.
63	`ibd (A)`	Source-drain diode current.
64	`cgso (F)`	Gate-source overlap capacitance.
65	`cgbo (F)`	Gate-bulk overlap capacitance.
66	`cgdo (F)`	Gate-drain overlap capacitance.
67	`cggo (F)`	Gate-gate overlap capacitance.
68	`cddo (F)`	Drain-drain overlap capacitance.
69	`weff (m)`	Effective channel width.
70	`leff (m)`	Effective channel length.
71	`rseff (Ohm)`	Effective source resistance.
72	`rdeff (Ohm)`	Effective drain resistance.
73	`rsdrift (Ohm)`	The resistance of drift region for source side.
74	`rdrift (Ohm)`	The resistance of drift region for drain side.
75	`gmt (S)`	Temp transconductance.
76	`ic_bjt (A)`	Internal collector current of BJT.
77	`ie_bjt (A)`	Internal emitter current of BJT.
78	`ibase_bjt (A)`	Internal base current of BJT.
79	`ice (A)`	Collector-Emitter current of HiSIM_IGBT.
80	`vce (A)`	Collector-Emitter voltage of HiSIM_IGBT.
81	`qex (Coul)`	Excess charge in the base.
82	`qdep (Coul)`	Depletion charge in the base at the emitter side.
83	`rbase (Ohm)`	Effective internal base resistance.

© 2023 Cadence Design Systems, Inc.

Parameter Index

In the following index, `I` refers to instance parameters, `M` refers to the model parameters section, `O` refers to the output parameters section, and `OP` refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of `M-35` means the 35th model parameter.

ad I-4	isub OP-52	pclm1 M-563	scsti1 M-135
ad M-28	js0 M-239	pclm2 M-564	scsti2 M-136
alarm M-21	js0sw M-240	pclm3 M-565	scsti3 M-137
as I-3	kappa M-96	pd I-6	sd I-35
as M-27	l I-2	pd M-30	shetemp OP-1
bb M-154	l M-26	pds OP-51	slg M-186
bgtmp1 M-87	lbgtmp1 M-362	peg0 M-512	slgl M-198
bgtmp2 M-88	lbgtmp2 M-363	pfn1 M-542	slglp M-199
bjtgminc M-335	lbinn M-359	pfn2 M-543	sub1 M-180
bjtgmine M-336	lcgdo M-410	pfn3 M-544	sub1l M-187
bjtldec M-337	lcgso M-409	pfvbs M-545	sub1lp M-200
bjtmuen M-329	lcisbk M-414	pgd1 M-97	sub2 M-181
bjtmuep M-328	lclm1 M-415	pgd2 M-98	sub2l M-188
bjtmueqn M-330	lclm2 M-416	pgd3 M-99	subld1 I-24
bjtnb M-347	lclm3 M-417	pgd4 M-100	subld1 M-84
bjtnc M-348	ldrift M-318	pgidl1 M-567	subld2 I-25

© 2023 Cadence Design Systems, Inc.

bjtne M-346
bjtninj M-325
bjtninjmax M-326
bjtnref M-334
bjtpmin M-338
bjtqdep M-344
bjtqex M-345
bjtrb M-339
bjtrbvg11 M-340
bjtrbvg12 M-341
bjtrc M-342
bjtre M-343
bjttaub M-332
bjttauc M-333
bjttaue M-331
bjtwb M-349
bjtwdepmax M-327
bjtwhalfcell M-350
bs1 M-112
bs2 M-113
ldrift1 I-26
ldrift1 M-80
ldrift1s I-31
ldrift1s M-81
ldrift2 I-27
ldrift2 M-82
ldrift2s I-32
ldrift2s M-83
leff OP-70
leg0 M-364
lfn1 M-394
lfn2 M-395
lfn3 M-396
lfvbs M-397
lgidl1 M-419
lgidl2 M-420
lgleak1 M-421
lgleak2 M-422
lgleak3 M-423
lgleak6 M-424
pgidl2 M-568
pgleak1 M-569
pgleak2 M-570
pgleak3 M-571
pgleak6 M-572
pglkb1 M-575
pglkb2 M-576
pglksd1 M-573
pglksd2 M-574
pibpc1 M-581
pibpc2 M-582
pjs0 M-559
pjs0sw M-560
pmuecb0 M-530
pmuecb1 M-531
pmueph1 M-532
pmuesr1 M-535
pmuesti1 M-551
pmuesti2 M-552
pmuesti3 M-553
subld2 M-85
svbs M-183
svbsl M-184
svbslp M-197
svds M-185
svgs M-182
svgsl M-193
svgslp M-194
svgsw M-196
svgswp M-195
tcjbd M-247
tcjbdsw M-248
tcjbdswg M-249
tcjbs M-250
tcjbssw M-251
tcjbsswg M-252
temp I-7
temp M-31
tnom M-16
tox M-33

© 2023 Cadence Design Systems, Inc.

bvd M-280
bvj M-282
bvs M-281
cbb OP-39
cbb_tot OP-43
cbd OP-37
cbg OP-36
cbs OP-38
cdb OP-31
cdd OP-29
cdd_tot OP-40
cddo OP-68
cdg OP-28
cds OP-30
cgb OP-27
cgbo M-269
cgbo OP-65
cgd OP-25
cgdo M-268
cgdo OP-66
cgg OP-24
lglkb1 M-427
lglkb2 M-428
lglksd1 M-425
lglksd2 M-426
libpc1 M-433
libpc2 M-434
ljs0 M-411
ljs0sw M-412
ll M-45
lld M-46
lln M-47
lmax M-353
lmin M-354
lmuecb0 M-382
lmuecb1 M-383
lmueph1 M-384
lmuesr1 M-387
lmuesti1 M-403
lmuesti2 M-404
lmuesti3 M-405
lmuetmp M-388
pmuetmp M-536
pndep M-528
pnfalp M-578
pnftrp M-577
pninv M-529
pnj M-561
pnover M-515
pnovers M-513
pnsti M-546
pnsubc M-518
pnsubp M-519
pnsubpsti1 M-554
pnsubpsti2 M-555
pnsubpsti3 M-556
powrat M-324
ppgd1 M-526
ppgd3 M-527
ppthrou M-579
ps I-5
ps M-29
ps0 OP-49
tpoly M-36
type M-1
vbd_max M-358
vbi M-51
vbox M-283
vbs OP-6
vbsmin M-293
vce OP-80
vdiffj M-259
vds OP-5
vds0 M-143
vds_max M-355
vdsat OP-8
vdsti M-142
version M-2
vfbc M-41
vfbover M-272
vgd_max M-356
vgs OP-4
vgs_max M-357
vmax M-155

© 2023 Cadence Design Systems, Inc.

cgg_tot OP-41
cggo OP-67
cgs OP-26
cgso M-267
cgso OP-64
cisb M-261
cisbk M-264
cit M-230
cj M-244
cjd OP-22
cjs OP-23
cjsw M-245
cjswg M-246
clm1 M-174
clm2 M-175
clm3 M-176
clm4 M-177
clm5 M-178
clm6 M-179
coadov M-6
codfm M-22
lndep M-380
lnfalp M-430
lnftrp M-429
lninv M-381
lnj M-413
lnover M-367
lnovers M-365
lnsti M-398
lnsubc M-370
lnsubp M-371
lnsubpsti1 M-406
lnsubpsti2 M-407
lnsubpsti3 M-408
lod I-22
lover I-28
lover M-44
loverld I-30
loverld M-78
lovers I-29
lovers M-79
lp M-42
psc1 M-523
psc2 M-524
psc3 M-525
pscp1 M-520
pscp2 M-521
pscp3 M-522
pscsti1 M-548
pscsti2 M-549
psl OP-50
psub1 M-537
psub2 M-538
psvbs M-540
psvds M-539
psvgs M-541
pthrou M-231
pthroub M-232
pvdiffj M-580
pvfbc M-517
pvfbover M-514
pvmax M-509
pvthsti M-550
vover M-156
voverp M-157
vovers M-158
voversp M-159
vth OP-7
vthsti M-126
vtmp M-160
vzadd0 M-237
w I-1
w M-25
w0 M-118
warn M-279
wbgtmp1 M-436
wbgtmp2 M-437
wbinn M-360
wcgdo M-484
wcgso M-483
wcisbk M-488
wclm1 M-489
wclm2 M-490
wclm3 M-491

© 2023 Cadence Design Systems, Inc.

coflick M-12
cogidl M-8
coign M-19
coiigs M-9
coiprv M-4
coisti M-13
coisub M-7
compatible M-20
conqs M-14
coovlp M-10
coovlps M-11
copprv M-5
corbnet I-11
corbnet M-18
corg I-17
corg M-17
corsrd M-3
coselfheat M-23
cosym M-24
cothrml M-15
csb OP-35
lpext M-54
lpgd1 M-378
lpgd3 M-379
lpthrou M-431
lsc1 M-375
lsc2 M-376
lsc3 M-377
lscp1 M-372
lscp2 M-373
lscp3 M-374
lscsti1 M-400
lscsti2 M-401
lsub1 M-389
lsub2 M-390
lsvbs M-392
lsvds M-391
lsvgs M-393
lvdiffj M-432
lvfbc M-369
lvfbover M-366
lvmax M-361
pvtmp M-533
pwfc M-566
pwl2 M-516
pwr OP-48
pwsti M-547
pwvth0 M-534
pzadd0 M-238
qb OP-12
qb_itr OP-16
qd OP-13
qd_itr OP-17
qdep OP-82
qdftvd M-296
qdp OP-20
qex OP-81
qg OP-14
qg_itr OP-18
qme1 M-93
qme2 M-94
qme3 M-95
qovsm M-307
weff OP-69
weg0 M-438
wfc M-114
wfn1 M-468
wfn2 M-469
wfn3 M-470
wfvbs M-471
wgidl1 M-493
wgidl2 M-494
wgleak1 M-495
wgleak2 M-496
wgleak3 M-497
wgleak6 M-498
wglkb1 M-501
wglkb2 M-502
wglksd1 M-499
wglksd2 M-500
wibpc1 M-507
wibpc2 M-508
wjs0 M-485
wjs0sw M-486

© 2023 Cadence Design Systems, Inc.

csd OP-33
csg OP-32
css OP-34
css_tot OP-42
ctemp M-263
cth0 M-295
cvb M-262
cvbk M-265
cvdsover M-323
ddltict M-277
ddltmax M-275
ddltslp M-276
divx M-266
dly1 M-233
dly2 M-234
dly3 M-235
dlyov M-236
dtemp I-8
dtemp M-32
eg0 M-86
lvthsti M-402
lvtmp M-385
lwfc M-418
lwl2 M-368
lwsti M-399
lwvth0 M-386
m I-23
mbe0 M-287
mbewl M-286
mismatchdist M-290
mismatchmod M-289
mj M-253
mjsw M-254
mjswg M-255
mphdfm M-278
muecb0 M-144
muecb1 M-145
mueph0 M-146
mueph1 M-147
mueph2 M-117
qs OP-15
qs_itr OP-19
qsp OP-21
rbase OP-83
rbdb I-15
rbdb M-61
rbpb I-12
rbpb M-58
rbpd I-13
rbpd M-59
rbps I-14
rbps M-60
rbsb I-16
rbsb M-62
rd M-40
rd2 M-69
rd20 M-299
rd21 M-300
rd22 M-301
rd22d M-302
wl M-48
wl1 M-168
wl1p M-169
wl2 M-170
wl2p M-171
wld M-49
wln M-50
wmax M-351
wmin M-352
wmuecb0 M-456
wmuecb1 M-457
wmueph1 M-458
wmuesr1 M-461
wmuesti1 M-477
wmuesti2 M-478
wmuesti3 M-479
wmuetmp M-462
wndep M-454
wnfalp M-504
wnftrp M-503

© 2023 Cadence Design Systems, Inc.

egig M-221
falph M-228
fn1 M-189
fn2 M-190
fn3 M-191
fvbs M-192
gbbs OP-55
gbds OP-53
gbgs OP-54
gbmin M-63
gds OP-10
gidl1 M-222
gidl2 M-223
gidl3 M-224
gidl4 M-225
gidl5 M-226
gleak1 M-204
gleak2 M-205
gleak3 M-206
gleak4 M-207
gleak5 M-208
muephl M-161
muephs M-172
muephw M-122
mueplp M-162
muepsp M-173
muepwp M-123
mueslp M-165
muesr0 M-149
muesr1 M-150
muesrl M-163
muesrw M-164
muesti1 M-127
muesti2 M-128
muesti3 M-129
mueswp M-125
muetmp M-148
mvt0 M-285
mvtwl M-284
mvtwl2 M-288
ndep M-151
ndepl M-166
rd23 M-303
rd23l M-312
rd23lp M-313
rd23s M-314
rd23sp M-315
rd24 M-304
rd25 M-305
rd26 M-306
rd3 M-70
rdeff OP-72
rdict1 M-75
rdict2 M-77
rdov11 M-71
rdov12 M-72
rdov13 M-73
rdrift OP-74
rds M-316
rdslp1 M-74
rdslp2 M-76
rdsp M-317
rdtemp1 M-89
wninv M-455
wnj M-487
wnover M-441
wnovers M-439
wnsti M-472
wnsubc M-444
wnsubp M-445
wnsubpsti1 M-480
wnsubpsti2 M-481
wnsubpsti3 M-482
wpgd1 M-452
wpgd3 M-453
wpthrou M-505
wsc1 M-449
wsc2 M-450
wsc3 M-451
wscp1 M-446
wscp2 M-447
wscp3 M-448
wscsti1 M-474
wscsti2 M-475

© 2023 Cadence Design Systems, Inc.

gleak6 M-218
gleak7 M-219
glkb0 M-212
glkb1 M-213
glkb2 M-214
glkb3 M-220
glksd1 M-209
glksd2 M-210
glksd3 M-211
glpart1 M-203
gm OP-9
gmbs OP-11
gmt OP-75
ibase_bjt OP-78
ibd OP-63
ibpc1 M-201
ibpc2 M-202
ibs OP-62
ibulk OP-47
ic_bjt OP-76
ice OP-79
ndeplp M-167
nf I-21
nfalp M-227
nftrp M-229
ngcon I-18
ninv M-152
ninvd M-153
nj M-241
njsw M-242
nover M-273
novers M-274
npext M-55
nrd I-10
nrs I-9
nsti M-120
nsubc M-37
nsubcdfm I-36
nsubcw M-115
nsubcwp M-116
nsubp M-38
nsubp0 M-52
rdtemp2 M-90
rdvb M-298
rdvd M-297
rdvdl M-308
rdvdlp M-309
rdvds M-310
rdvdsp M-311
rdvdtemp1 M-91
rdvdtemp2 M-92
rdvg11 M-291
rdvg12 M-292
reversed OP-2
rs M-39
rsdrift OP-73
rseff OP-71
rsh M-56
rshg M-57
rth0 M-294
rth0nf M-322
rth0r M-319
rth0w M-320
wsti M-121
wstil M-133
wstilp M-134
wstiw M-140
wstiwp M-141
wsub1 M-463
wsub2 M-464
wsvbs M-466
wsvds M-465
wsvgs M-467
wvdiffj M-506
wvfbc M-443
wvfbover M-440
wvmax M-435
wvth0 M-124
wvthsc M-119
wvthsti M-476
wvtmp M-459
wwfc M-492
wwl2 M-442
wwsti M-473

© 2023 Cadence Design Systems, Inc.

id OP-44
ids OP-3
ie_bjt OP-77
ig OP-45
igate OP-56
igateb OP-58
igated OP-59
igates OP-57
igidl OP-61
igisl OP-60
igtemp1 M-215
igtemp2 M-216
igtemp3 M-217
is OP-46
isnoisy I-37
nsubpsti1 M-130
nsubpsti2 M-131
nsubpsti3 M-132
nsubwp M-53
ovmag M-271
ovslp M-270
parl2 M-101
pb M-256
pbgtmp1 M-510
pbgtmp2 M-511
pbsw M-257
pbswg M-258
pcgdo M-558
pcgso M-557
pcisbk M-562
rth0wp M-321
sa I-33
saref M-138
sb I-34
sbref M-139
sc1 M-102
sc2 M-103
sc2b M-104
sc3 M-105
sc4 M-106
scp1 M-107
scp2 M-108
scp21 M-111
scp22 M-110
scp3 M-109
wwvth0 M-460
xgl I-20
xgw I-19
xl M-64
xld M-34
xldld M-68
xqy M-43
xqy1 M-66
xqy2 M-67
xti M-243
xti2 M-260
xw M-65
xwd M-35

© 2023 Cadence Design Systems, Inc.

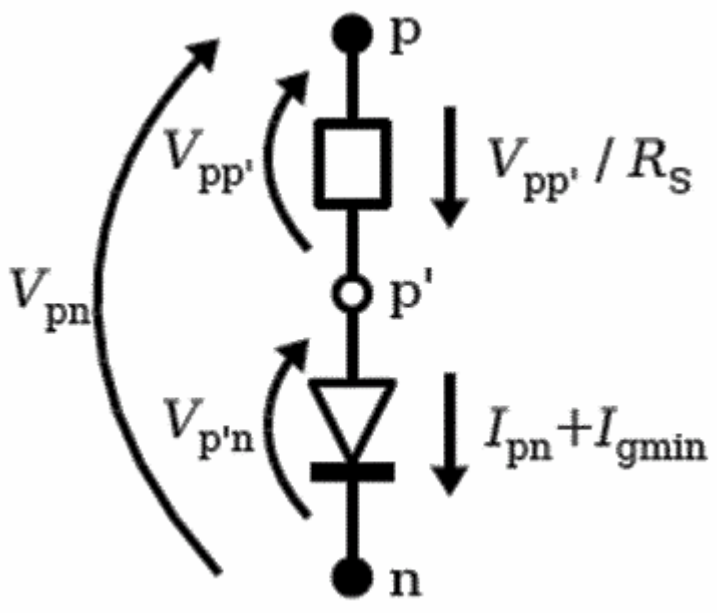
© 2023 Cadence Design Systems, Inc.

34

HiSIM_Diode Model (hisim_diode)

HiSIM_Diode is a compact diode model with reverse recovery. It supports DC, AC, and transient analyses.

Elements considered in HiSIM_Diode model are summarized in the figure below. The internal node p' is determined when the parasitical resistor is given. The applied voltage V_{pn} is reduced effectively to $V_{p'n}$ due to the potential drop $V_{pp'}$ induced by the resistance R_s.



The basic model concept is consistent with that of conventional diode. The reverse recovery effect is additionally introduced in the HiSIM_Diode model. A high voltage p-i-n structure operating in high level injection is assumed as typical for most power diodes. In actual diodes, reverse recovery is caused by diffusion of charge from the center of the i region, thus, one or more charge storage nodes must be added to provide for this diffusion current. In HiSIM_Diode model, modified lumped charge concept is implemented and charge storage node is adopted. Two model parameters are introduced in the model: The carrier transit time TAUTRAN and the recovery time TAUREC.

© 2023 Cadence Design Systems, Inc.

Related Topics

Model Usage

Component Statements

Model Usage

Instance Syntax

HiSIM_Diode instances must specify 2 terminals, anode and cathode node respectively. To specify an HiSIM_Diode instance element, the Model Name has to be associated with a HiSIM_Diode model card.

```
InstanceName p n ModelName parameter=value ...
```

Sample Instance Statement

```
d1 (vpp vnn) n_dio area=1e-12
```

Model Syntax

The following syntax specifies HiSIM_Diode model:

```
model ModelName hisim_diode parameter=value ...
```

The third parameter, `hisim_diode`, is the master to indicate this model card is a HiSIM_Diode model card.

Sample Model Statement

```
model n_dio hisim_diode eg0=1.17 rs=1e-1 bgtmp1=1e-4 rst1=1e-3
```

Related Topics

HiSIM_Diode Model (hisim_diode)

Component Statements

© 2023 Cadence Design Systems, Inc.

Component Statements

Instance Parameters

`area=1.0 m^2`	Junction area.
`trise=0 C`	Temperature rise from ambient.

Model Parameters

Junction hsmdiode model parameters

`compatible=spectre`	Spice compatible flag. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, `sspice`, and `mica`.
`js0=5.0e-7 A/m^2`	Saturation current.
`eg0=1.1785 V`	Band gap.
`nj=1`	Emission coefficient.
`vdiffj=0.6e-3 V`	Diode threshold voltage.
`cj=5.0e-4 F/m^2`	Bottom junction capacitance per unit area at zero bias.
`pb=1.0 V`	Bottom junction build-in potential.
`mj=0.5`	Bottom junction capacitance grading coefficient.
`divx=0.0 1/V`	Reverse current coefficient.
`tautran=5.0e-8 s`	Transit time.
`taurec=1.0e-9 s`	Recovery time.

Parasitic resistance parameters

`rs=0 ohmm^2`	Series resistance per unit area.
`rsv1=0 1/C`	Voltage dependence for the resistance.

© 2023 Cadence Design Systems, Inc.

`rsv2=0 C^-2`	Voltage dependence for the resistance.
`rsi1=0 1/C`	Current dependence for the resistance.
`rsi2=0 C^-2`	Current dependence for the resistance.

Temperature effects parameters

`tnom (C)`	Parameters measurement temperature. Default set by `options'.
`bgtmp1=90.25e-6 1/C`	Temperature dependence of bandgap.
`bgtmp2=1.0e-7 C^-2`	Temperature dependence of bandgap.
`rst1=0 1/C`	Temperature dependence for the resistance.
`rst2=0 C^-2`	Temperature dependence for the resistance.
`tcjbd=0 1/C`	Temperature dependence of hsmdiode capacitance.
`xti=2`	Temperature coefficient for forward-current densities.

Operating Point Parameters

`vd (V)`	Diode voltage.
`id (A)`	Diode current.
`gd (S)`	Diode conductance.
`cd (F)`	Diode capacitance.
`rdio (Ohm)`	Diode equivalent resistance.
`charge (Coul)`	Diode capacitor charge.
`p (W)`	Diode power.
`region`	Estimated operating region. Spectre generates output number (0-2) in a rawfile. Possible values are off and on.

Related Topics

HiSIM_Diode Model (hisim_diode)

© 2023 Cadence Design Systems, Inc.

Model Usage

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

35

Surface Potential Based Compact MOSFET Model (spmos)

This chapter contains the following information about the SPMOS model:

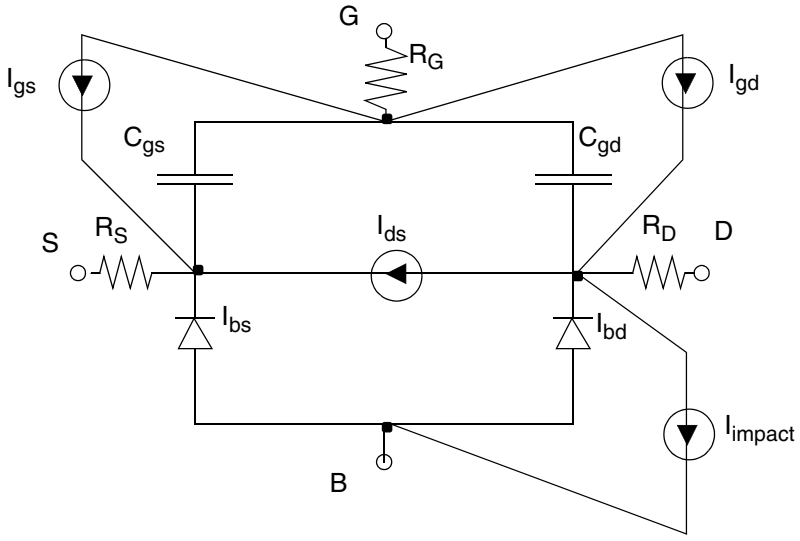
- Core Model on page 2617
  - Equivalent Circuit on page 2617
  - Lateral Gradient Factor on page 2617
  - Effective Drain-Source Voltage on page 2618
  - Surface Potential on page 2619
  - Quantum Mechanical Corrections on page 2624
  - Polysilicon Depletion on page 2626
  - Drain Current on page 2628
  - Intrinsic Charges on page 2629
  - Bias-Dependent Body Factor on page 2630
- Extrinsic Model on page 2630
  - Charge Model on page 2633
  - Gate Current Model on page 2634
  - Substrate Current Model on page 2637
  - Total Terminal Currents on page 2638
  - Noise Model on page 2638
  - Gate Induced Drain/Source Leakage Current Model on page 2641
- Parameter Descriptions on page 2647
  - New Parameters for SPMOS Version 34 on page 2653

© 2023 Cadence Design Systems, Inc.

- Parameters with Different Default Values for SPMOS Version 34 on page 2655

© 2023 Cadence Design Systems, Inc.

Equivalent Circuit



Core Model

Lateral Gradient Factor

The lateral field gradient in SPMOS is reduced with surface potential through the following semi-empirical formula:

$$f = f_0 + B_t x_f$$

where

$$f_0 = \frac{F_0}{1 + B_f V_{sbx1} + (C_f V_{dsx} + A_f V_{sbx1})(1 + EF \cdot A_f V_{sbx1}) + h_{lo}} + 0.01$$

$$h_{lo} = Hlo1 \cdot V_{hlo}^2 \left| Hlo2 \cdot \sqrt{V_{hlo}} \right.$$

$$V_{hlo} = \frac{V_{dsx} \cdot W_{hlo}}{V_{dsx} + W_{hlo} + 10^{-8}}$$

© 2023 Cadence Design Systems, Inc.

$$V_{dsx} = \sqrt{V_{hlo}^2 + 0.01} - 0.1$$

$$V_{sbx1} = MAXA(V_{sbx}, 0, 10^{-4})$$

$$v_{sbx} = V_{sb} + \frac{1}{2}(V_{ds} - V_{dsx})$$

$$B_t = (f_0 - 0.01)B_f V_t$$

$$x_f = \frac{\phi_f}{V_t}$$

Effective Drain-Source Voltage

The saturation voltage is given by

$$V_{dsat} = \phi_{sat} - V_t \cdot \ln\left[1 + \frac{\phi_{sat} \cdot (\phi_{sat} - (2 \cdot a_{sat} \cdot V_t))}{G_f^2 \cdot \Delta_s \cdot V_t^2}\right]$$

where

$$a_{sat} = x_{gs} + \frac{1}{2} \cdot G_f^2$$

$$\phi_{sat} = \frac{2 \cdot \phi_0 \cdot \phi_2}{\phi_0 + \phi_2 + \sqrt{(\phi_0 + \phi_2)^2 - 3.96 \cdot \phi_0 \cdot \phi_2}}$$

$$\phi_0 = \psi_0 \cdot \frac{V_c + \frac{V_2}{4} + \psi_0 \cdot \left(\frac{1}{8} + \frac{\delta_0^2}{2}\right)}{V_c + V_2 \cdot \delta_0 \cdot (1 - \delta_0) + \psi_0 \cdot \delta_0^2}$$

$$\phi_2 = \frac{V_t \cdot G_f^2 \cdot \Delta_s \cdot S0}{a_{sat} + \sqrt{a_{sat}^2 - G_f^2 \cdot \Delta_s \cdot S0}}$$

© 2023 Cadence Design Systems, Inc.

$$\delta_0 = \frac{\psi_0}{\psi_0 + G_{hf} V_c}$$

$$\psi_0 = \frac{2 \cdot V_2}{1 + \frac{V_2}{4 \cdot V_c} + \sqrt{1 + \frac{V_2}{V_c} + \left(\frac{V_2}{4 \cdot V_c}\right)^2}}$$

$$V_2 = \frac{V_1}{\alpha_s} + V_t$$

$$V_c = \frac{u_{sat} L}{\mu_s}$$

$$u_{sat} = \frac{VSAT}{1 + K_{sm} \cdot w_{sat}}$$

$$w_{sat} = \frac{100 \cdot V_1 \cdot (1 + STX \cdot V_{sbx})}{100 + V_1 \cdot (1 + STX \cdot V_{sbx})}$$

$$\alpha_s = 1 + \frac{G_f \cdot (1 - E_s)}{2 \cdot S_s}$$

The effective drain-source voltage is given by

$$V_{dse} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{a_x}\right]^{\frac{1}{a_x}}}$$

Surface Potential

Surface Potential at Source End of Channel

The approximate analytical solution for surface potential is

$$x = \theta(V_{gb}, \phi_n)$$

© 2023 Cadence Design Systems, Inc.

where the normalized imref splitting is

$$\phi_n = (F_p - F_n)/q$$

$$x_s = \theta(V_{gb}, V_{sb})$$

In the process of computing surface potential, the following are computed as well

$$E_s = \exp(-x_s)$$

$$\Delta_s = \Delta_{ns}/E_s$$

$$D_s = (E_s^{-1} + E_s - 2x_s) \cdot \Delta_{ns}$$

where

$$\Delta_{ns} = \frac{1}{f} \cdot \exp(-x_{ns})$$

and

$$x_{ns} = (2\phi_b + V_{sb})/V_t$$

The evaluation of E_s, Δ_s, Δ_{ns} is carefully ordered to avoid over/underflow problems.

After evaluating surface potential x_s, you can compute the normalized inversion charge at the source

$$V_1 = \frac{G_f^2 V_t D_s}{x_{gs} + G_f S_s}$$

where

$$S_s = \sqrt{P_s}$$

$$P_s = x_s - 1 + E_s$$

© 2023 Cadence Design Systems, Inc.

$$x_{gs} = G_f\sqrt{D_s + P_s}$$

$$G_f = G\sqrt{f}$$

Series resistance is given by:

$$R_t = \frac{R_{t1}(1 + RB \cdot V_{sbx})}{1 + R_g V_1}$$

Series resistance factor is given by:

$$\rho = MU0(C_{ox}/L)R_t V_1$$

Effective vertical field is given by:

$$E_{eff} = E_{eff0}(q_b + \eta_\mu V_1)$$

$$q_b = V_t G_f S_s$$

where $\eta_\mu = 1/2$ for n-channel and $\eta_\mu = 1/3$ for p-channel MOSFETs.

Effective mobility at the source end of the channel is given by:

$$\mu_s = \frac{MU0 \cdot \mu_x}{1 + (\mu_E \cdot E_{eff})^{\theta_{MU}} + CS \cdot \dfrac{q_b^2}{(V_1 + q_b)^2} + \rho}$$

The variable is given by

$$\mu_x = (1 + X_{cor} \cdot V_{sbx})/(1 + 0.2X_{cor} \cdot V_{sbx})$$

where the term $(1 + X_{cor} \cdot V_{sbx})$ introduces non-universality. The denominator assures that μ_x does not exceed 5 for extreme (and unphysical) V_{sbx}.

V_1 and μ_s are temporary variables. Eventually these will be changed to assure the symmetry of the model. Also, $\rho = 0$ if external model of series resistance is used.

© 2023 Cadence Design Systems, Inc.

Surface Potential at Drain End of Channel

Surface potential at the drain end of the channel is

$$\phi_{sd} = x_d V_t$$

where

$$x_d = \theta(V_{gb}, V_{sb} + V_{dse})$$

The above equation is used when

$$x_g > x_{g23} = x_{g23} + G\sqrt{f_{23}(x_{23} - 1)}$$

where

$$f_{23} = f_0 + B_t x_{23}$$

$$x_{23} = \begin{cases} (\phi_b + V_{sb})/V_t & for V_{sb} \geq 0 \\ (\phi_b + 0.5V_{sb})/V_t & for V_{sb} < 0 \end{cases}$$

For $x_g < x_{g23}$, it is more efficient to:

1. Compute x_s
2. Determine normalized drain-source surface potential difference $\varphi = \phi/V_t$
3. Compute $x_d = x_s + \varphi$.

While computing x_d , the following variables are computed as well:

$$E_d = \exp(-x_d)$$

$$D_d = (E_d^{-1} - E_d - 2x_d)\Delta_{nd}$$

where

$$\Delta_{nd} = \frac{1}{f}\exp(-x_{nd})$$

© 2023 Cadence Design Systems, Inc.

$$x_{nd} = (2\phi_b + V_{sb} + V_{dse})/V_t$$

Mid-Point Surface Potential

$$\phi_m = \frac{1}{2}(\phi_{ss} + \phi_{sd})$$

The following variables are used:

$$x_m = \frac{1}{2}(x_s + x_d)$$

$$E_m = \sqrt{E_s E_d}$$

$$D_m = \frac{1}{2}(D_s + D_d) + \frac{1}{8}\varphi^2\left(E_m - \frac{2}{G_f^2}\right)$$

$$P_m = x_m - 1 + E_m$$

$$x_{gm} = G_f\sqrt{D_m + P_m}$$

$$S_m = \sqrt{P_m}$$

Normalized inversion charge is calculated by:

$$V_m = \frac{G_f^2 V_t D_m}{x_{gm} + G_f S_m}$$

Linearization coefficient is

$$\alpha = 1 + \frac{G_f(1 - E_m)}{2S_m}$$

Series resistance:

© 2023 Cadence Design Systems, Inc.

$$R_t = \frac{R_{t1}(1 + RB \cdot V_{sbx})}{1 + R_g V_m}$$

Series resistance factor:

$$\rho = MU0(C_{ox}/L)R_t V_m$$

Effective vertical field is

$$E_{eff} = E_{eff0}(q_b + \eta_\mu V_m)$$

$$q_b = V_t G_f S_m$$

where $\eta_\mu = 1/2$ for n-channel and $\eta_\mu = 1/3$ for p-channel MOSFETs.

Effective mobility

$$\mu_m = \frac{MU0 \cdot \mu_x}{1 + (\mu_E \cdot E_{eff})^{\theta_{MU}} + CS \cdot \dfrac{q_b^2}{(V_m + q_b)^2} + \rho}$$

Quantum Mechanical Corrections

In SPMOS quantum-mechanical (QM) corrections are considered in the most common case $\phi_s \geq 3V_t$ which is of interest for the charge-sheet models.

QM corrections are directly used for $x_m = \phi_m/V_t$ and $\varphi = (\phi_{sd} - \phi_{ss})/V_t$.

This is preferable to correcting ϕ_{ss} and ϕ_{sd}, especially in the case when φ is a small difference of two large variables.

In the following equations, superscript 0 refers to variables uncorrected for QM effects.

For $x_g \geq 0$ (i.e. for $V_{gb} \geq V_{fb}$)

$$x_m = x_m^{(0)} + u_{QM}$$

© 2023 Cadence Design Systems, Inc.

$$\varphi = \varphi^{(0)} \cdot \frac{k_m(\overline{D} + d_0)}{d + k_m \overline{D} \alpha_{QM}}$$

where

$$u_{QM} = \frac{q_{QM}}{p_{QM} - q_{QM}/p_{QM}}$$

$$q_{QM} = G_f^2 D_m^{(0)} \Delta e_g'$$

$$\Delta e_g' = g_{QMP} \Delta e_g$$

$$\Delta e_g = q_q x_{gm}^{2/3}$$

$$g_{QMP} = \frac{D_m^{(0)}}{D_m^{(0)} + P_m^{(0)}}$$

$$p_{QM} = 2x_{gm} + G_f^2 [1 - E_m^{(0)} + D_m^{(0)} \alpha_{QM}]$$

$$\alpha_{QM} = 1 + \frac{2\Delta e_g'}{3x_{gm}}$$

$$k_m = \exp(\alpha_{QM} u_{QM} - \Delta e_g')$$

$$\overline{D} = \frac{D_s + D_d}{2}$$

$$d_0 = 1 - E_m^{(0)} + 2x_{gm}/G_f^2$$

$$d = d_0 + (E_m^{(0)} - 2/G_f^2) u_{QM}$$

© 2023 Cadence Design Systems, Inc.

For $x_g < 0$,

$$x_m = x_m^{(0)} - \frac{\Delta e_g' \phi_m^2}{\phi_m^2 + \frac{0.04}{1 + 3|\phi_m|}}$$

There is no correction for φ. This form is introduced to eliminate the singularity or unphysical behavior near $V_{gb} = V_{fb}$. Coefficients 0.04 and 3 are not affected by model parameters and are fixed.

In addition to correcting ϕ_m and x_m, QM effects are introduced into

$$D_m = k_m D_m^{(0)}$$

and variables P_m, x_{gm}, which are given by the above expressions but with x_m corrected for QM effects.

Polysilicon Depletion

In SPMOS polysilicon depletion equations are conditioned to provide smooth device characteristics for a wide voltage range but at present the poly effects are only included for $\upsilon_{gb} > V_{fb}$.

The normalized poly surface potential at midpoint

$$x_{pm} = k_p \left[\frac{x_{gm}^{(0)}}{1 + \eta_p^{-1}} \right]^2$$

where

$$\eta_p = [1 + k_p x_{gm}^{(0)}]^{-1/2}$$

In this section the superscript 0 indicates that the variable is not corrected for poly depletion effect.

Poly corrections are introduced into $x_m = \phi_m / V_t$ and $\varphi = (\phi_{sd} - \phi_{ss})/V_t$ rather than into ϕ_{ss} and ϕ_{sd} directly.

© 2023 Cadence Design Systems, Inc.

The corrected midpoint surface potential is

$$x_m = x_m^{(0)} + u_p$$

where

$$u_p = \frac{q}{p - q/p}$$

$$p = 2[x_{gm}^{(0)} - x_{pm}] + G_f^2[1 - E_m^{(0)} + D_m^{(0)}]$$

$$q = x_{pm}[x_{pm} - 2x_{gm}^{(0)}]$$

The correction to normalized surface potential difference φ is as follows

$$\varphi = \varphi^{(0)} \cdot \frac{k_m(d_0 + \bar{D})}{d + k_m\bar{D}}$$

where d_0 is given in section "Quantum Mechanical Corrections" on page 2624 with superscript 0 indicating that the variable is not corrected for poly depletion effect

$$d = 1 + E_m^{(0)} - 2\eta_p x_{gm}/G_f^2$$

$$k_m = \exp(u_p)$$

In addition to changing the surface potentials, poly correction affects the linearization of inversion charge and intrinsic charges. The expressions in sections "Drain Current" on page 2628 and "Intrinsic Charges" on page 2629 include these corrections.

The case of no poly effect can be recovered by setting $\eta_p = 1$. While physically this corresponds to $NP \to \infty$, in SPMOS eliminating poly effects is formally prescribed by setting $NP = 0$ in the parameter file.

© 2023 Cadence Design Systems, Inc.

Drain Current

$$V_c = L \cdot \frac{u_{sat}}{\mu_m}$$

$$u_{sat} = \frac{VSAT}{1 + K_{sm} \cdot w_{sat}}$$

$$w_{sat} = \frac{100 \cdot V_m \cdot (1 + STX \cdot V_{sbx})}{100 + V_m \cdot (1 + STX \cdot V_{sbx})}$$

This ensures that $w_{sat} < 100$ and $u_{sat} < 0.3VSAT$ during SPICE convergence when V_m can be unphysically high.

$$\delta = \frac{\phi}{\phi + G_{hf} \cdot V_c}$$

$$L_{sat} = \frac{\delta\phi\mu_m}{u_{sat}}$$

The channel length modulation factor is calculated by the following equation:

$$L_{CLM} = \delta L_{q2d} \ln[1 + CLM3 \cdot (V_{ds} - \phi)]$$

Drain current is calculated by

$$I_d = \frac{\mu_m W C_{OX} (V_m + \alpha V_t)\phi}{L_{red} + L_{sat}}$$

where the inversion charge linearization (including polysilicon depletion effect) is:

$$\alpha = \eta_p + \frac{G_f(1 - E_m)}{2S_m}$$

The reduced channel length is

$$L_{red} = \frac{L}{1 + \frac{L_{CLM}}{L}}$$

© 2023 Cadence Design Systems, Inc.

Intrinsic Charges

All charges are normalized to C_{oxt}.

$$C_{oxt} = C_{ox}(L + 10^{-6}DLQ)(W + 10^{-6}DWQ)$$

Gate charge

$$Q_g = x_{gm}V_t + \frac{\eta_p\phi}{2}\left(\frac{\phi r_L}{6H} - 1 + r_L\right)$$

where

$$H = \frac{V_m/\alpha + V_t}{1 + L_{sat}/L_{red}}$$

$$r_L = L_{red}/L$$

Inversion layer charge

$$\left|Q_I\right| = r_L(V_m + \alpha\phi^2/12H) + Q_{CLM}$$

$$Q_{CLM} = (1 - r_L)(V_m - 0.5\alpha\phi)$$

Drain charge (computed using Ward-Dutton partition)

$$\left|Q_D\right| = \frac{1}{2}r_L^2\left\{V_m - \frac{\alpha\phi}{6}\left[1 - \frac{\phi}{2H} - \frac{1}{5}\left(\frac{\phi}{2H}\right)^2\right]\right\} + \frac{1}{2}Q_{CLM}(1 + r_L)$$

Source charge

$$\left|Q_S\right| = \left|Q_I\right| - \left|Q_D\right|$$

Bulk charge

$$\left|Q_B\right| = Q_G - \left|Q_I\right|$$

© 2023 Cadence Design Systems, Inc.

Bias-Dependent Body Factor

If NSLP>10^{-3},

$$\gamma = \gamma_0\sqrt{1 + D_{nsub}}$$

$$D_{nsub} = D_{nsubL} \cdot MAXA(0, (V_{gs} + VNSUB) \cdot NSLP, 0.1)$$

Otherwise

$$\gamma = \gamma_0$$

Normalized body factor is

$$G = \gamma/(\sqrt{V_t})$$

Extrinsic Model

Bias-Independent Variables

Overlap capacitance

$$C_{oxov} = \frac{\varepsilon_{ox}}{TOXOV}$$

Overlap body factor

$$\gamma_{ov} = \frac{\sqrt{2q\varepsilon_{Si}NOV}}{C_{oxov}}$$

Normalized overlap body factor ° °°°°°

$$G_{ov} = \frac{\gamma_{ov}}{\sqrt{V_t}}$$

Tunneling current density constant (in A/m^2)

© 2023 Cadence Design Systems, Inc.

$$J_0 = \frac{qm_0 k_B^2 TABS^2}{2\pi^2 h^3} = 1.082 \cdot 10^{11} \cdot \left(\frac{TABS}{300}\right)^2$$

Channel tunneling current density exponential constant (dimensionless)

$$B = 2TOX(2qm_0\chi_B)^{1/2}/h = 6.831 \cdot 10^9 \cdot TOX \cdot \sqrt{\chi_B}$$

Overlap tunneling current density exponential constant (dimensionless)

$$B_{ov} = 2TOXOV((2qm_0\chi_B)^{1/2}/h) = 6.831 \cdot 10^9 TOXOV\sqrt{\chi_B}$$

Auxiliary variable of gate current model

$$\alpha_b = E_g/(2q) + \phi_b$$

The Si / SiO_2 conduction band offset

$$\chi_B = 3.13V$$

Streamlined Surface Potential Approximation

The availability of the surface potential in the overlap regions is essential to the physical modeling of the charge and gate current components. The streamlined analytical approximation of the surface potential excludes the effects of minority carriers and consequently is even simpler and more efficient than the one employed in the channel region.

Let

$$\xi = 1 + G_{ov}/\sqrt{2}$$

and

$$x_{margin} = 10^{-7}\xi$$

If $|x| < x_{margin}$

$$x = -x_g/\xi$$

© 2023 Cadence Design Systems, Inc.

For $x_g < -x_{margin}$, proceed in the follow steps

$$y_g = -x_g$$

$$z = 1.25 y_g / \xi$$

$$\eta = \frac{1}{2}\{z + 10 - [(z-6)^2 + 64]^{1/2}\}$$

$$a = (y_g - \eta)^2 + G_{ov}^2(\eta + 1)$$

$$c = 2(y_g - \eta) - G_{ov}^2$$

$$\tau = -\eta + \log\left(\frac{a}{G_{ov}^2}\right)$$

$$y_0 = \eta + \sigma(a, c, \tau)$$

$$\Delta_0 = \exp(y_o)$$

$$p = 2(y_g - y_0) + G_{ov}^2(\Delta_0 - 1)$$

$$q = (y_g - y_0)^2 + G_{ov}^2(y_0 - \Delta_0 + 1)$$

$$x = -y_0 - \frac{2q}{p + \sqrt{p^2 - 2q(2 - G_{ov}^2\Delta_0)}}$$

For $x_g > x_{margin}$, compute

$$x_1 = 1.25$$

$$x_{g1} = x_1 + G_{ov}\sqrt{\exp(-x_1) + x_1 - 1}$$

© 2023 Cadence Design Systems, Inc.

$$\bar{x} = \left(\frac{x_g}{\xi}\right)\left[1 + x_g\frac{(\xi x_1 - x_{g1})}{x_{g1}^2}\right]$$

$$\bar{E} = \exp(-\bar{x})$$

$$\omega = 1 - \bar{E}$$

$$x_0 = x_g + \frac{G_{ov}^2}{2} - G_{ov}\left(x_g + \frac{G_{ov}^2}{4} - \omega\right)^{1/2}$$

$$\Delta_1 = \exp(-x_0)$$

$$p = 2(x_g - x_0) + G_{ov}^2(1 - \Delta_1)$$

$$q = (x_g - x_0)^2 - G_{ov}^2(x_o + \Delta_1 - 1)$$

$$x = x_0 + \frac{2q}{p + \sqrt{p^2 - 2q(2 - G_{ov}^2\Delta_1)}}$$

The evaluation of Δ_0 and Δ_1 is carefully ordered to avoid over/underflow problems.

Charge Model

Source overlap region charge

$$Q_{sov} = W \cdot LOV \cdot C_{oxov} \cdot (V_{gs} - \phi_{sov})$$

Drain overlap region charge

$$Q_{dov} = W \cdot LOV \cdot C_{oxov} \cdot (V_{gd} - \phi_{dov})$$

Bulk overlap region charge

$$Q_{bov} = L \cdot CGBO \cdot V_{gb}$$

© 2023 Cadence Design Systems, Inc.

Inner fringe charge correction

$$\Delta Q_G = -\Delta Q_S - \Delta Q_D$$

$$\Delta Q_S = IFKJ \cdot W(1 + IFCJV_{sb})(IFVBI + V_{sb} - \phi_{ss})^{1/2}$$

$$\Delta Q_D = IFKJ \cdot W(1 + IFCJV_{db})(IFVBI + V_{db} - \phi_{sd})^{1/2}$$

Outer fringe charge

$$Q_{ofs} = W \cdot CF \cdot V_{gs}$$

$$Q_{ofd} = W \cdot CF \cdot V_{gd}$$

Terminal charges

$$Q_G = Q_G^{(i)} + Q_{sov} + Q_{dov} + \Delta Q_G + Q_{ofs} + Q_{ofd} + Q_{bov}$$

$$Q_S = Q_S^{(i)} - Q_{sov} + \Delta Q_S - Q_{ofs}$$

$$Q_D = Q_D^{(i)} - Q_{dov} + \Delta Q_D - Q_{ofd}$$

$$Q_B = Q_B^{(i)} - Q_{bov}$$

where the superscript *(i)* indicates that the value for that parameter is taken from the SP intrinsic model.

Gate Current Model

$$I_g = I_{gc} + I_{gsov} + I_{gdov}$$

Channel contribution

$$I_{gc} = I_{gc0} \cdot i_{gc}$$

$$I_{gc0} = W \cdot L \cdot J_{gc}$$

© 2023 Cadence Design Systems, Inc.

$$J_{gc} = (J_0 \cdot F_s) \cdot \exp\left\{B \cdot \left[-GC1 + \frac{U_{oxm}}{\chi_B}\left(GC2 + \frac{GC3 \cdot U_{oxm}}{\chi_B}\right)\right]\right\}$$

$$U_{oxm} = \sqrt{V_{oxm}^2 + 10^{-6}}$$

where F_s is the supply function describing the difference of the population of carriers across the oxide at mid-point and is given by

$$F_s = \ln\left[\frac{1 + \Delta_{Si}}{1 + \Delta_{Si}\exp(-V_{gs}/V_t)}\right]$$

$$\Delta_{Si} = \exp\left[\frac{\phi_{ss} - \alpha_b - V_x - \psi_t}{V_t}\right]$$

$$\psi_t = MINA(0, V_{ox} + D, 0.05)$$

$$D = GC0 \cdot V_t$$

$$i_{gc} = (1 - b)\frac{\sinh(x)}{x} + b \cdot \cosh(x)$$

$$x = \frac{\phi}{2u_0}$$

$$b = \frac{u_0}{H}$$

$$u_0 = \frac{\chi_B}{[GC2 + 2GC3 \cdot (U_{oxm}/\chi_B)]}$$

Source-Drain Partition

The partition of the gate current in the channel area into the source and drain is essential for the MOSFET compact modeling, which is accomplished in SPMOS using the symmetrical linearization method.

© 2023 Cadence Design Systems, Inc.

The drain portion is given by

$$I_{gcd} = I_{gc0} i_{gcd}$$

$$i_{gcd} = \frac{i_{gc}}{2} - B_g \sinh(x) - A_g \frac{\sinh(x)}{x}\left[\coth(x) - \frac{1}{x}\right]$$

$$A_g = (1 - 3b + 3b^2)/2$$

$$B_g = b(1-b)/2$$

and the source portion is given by

$$I_{gcs} = I_{gc} - I_{gcd}$$

Source Overlap Region Contribution

$$I_{gsov} = W \cdot LOV \cdot J_{gsov}$$

$$J_{gsov} = J_0 F_{sovs} \exp\left\{B_{ov} \cdot \left[-GC1 + \frac{U_{oxovs}}{\chi_B}\left(GC2 + \frac{GC3 \cdot U_{oxovs}}{\chi_B}\right)\right]\right\}$$

$$U_{oxovs} = \sqrt{V_{oxovs}^2 + 10^{-6}}$$

The supply function, F_{sovs}, describing the difference of the population of carriers across the oxide in the source overlap region, given by

$$F_{sovs} = \ln\left[\frac{1 + \Delta_{Siovs}}{1 + \Delta_{Siovs}\exp(-V_{gs}/V_t)}\right]$$

$$\Delta_{Siovs} = \exp\left[\frac{3.0 + \phi_{sov} + \psi_{tovs}]}{V_t}\right]$$

$$\psi_{tovs} = MINA(0, Voxovs + GC0 \cdot V_t, 0.05)$$

© 2023 Cadence Design Systems, Inc.

Drain overlap region contribution

$$I_{gdov} = W \cdot LOV \cdot J_{gdov}$$

$$J_{gdov} = J_0 F_{sovd} \exp\left\{B_{ov} \cdot \left[-GC1 + \frac{U_{oxovd}}{\chi_B}\left(GC2 + \frac{GC3 \cdot U_{oxovd}}{\chi_B}\right)\right]\right\}$$

$$U_{oxovd} = \sqrt{V_{oxovd}^2 + 10^{-6}}$$

The supply function, F_{sovd}, describing the difference of the population of carriers across the oxide in the drain overlap region, given by

$$F_{sovd} = \ln\left[\frac{1 + \Delta_{Siovd}}{1 + \Delta_{Siovd}\exp(-V_{gd}/V_t)}\right]$$

$$\Delta_{Siovd} = \exp\left[\frac{3.0 + \phi_{dov} + \psi_{tovd}]}{V_t}\right]$$

$$\psi_{tovd} = MINA(0, V_{oxovd} + GC0 \cdot V_t, 0.05)$$

By setting SW_IGATE to 0 (default value) gate current model is turned off.

Substrate Current Model

The substrate current of MOSFETs due to impact ionization is given by

$$I_b = a_1 \cdot (V_{ds} - a3\phi) \cdot \exp\left(-\frac{a_2}{(V_{ds} - a_3\phi)}\right) \cdot I_d$$

$$a_1 = IIA1 + IIA1L \cdot A_L + IIA1W \cdot B_w + IIA1P \cdot A_L \cdot B_w$$

$$a_2 = IIA2[1 + a_4(\sqrt{V_{sb} + 2\phi_b} - \sqrt{2\phi_b})]\left(\frac{TABS}{T_n}\right)^{TK_IIA2}$$

© 2023 Cadence Design Systems, Inc.

$$a_3 = IIA3 + IIA3L \cdot A_L$$

$$a_4 = IIA4 + IIA4L \cdot A_L$$

Total Terminal Currents

The effect of I_b and I_g on the gate, source, drain and body components are as follows

$$I_G = I_{gc} + I_{gsov} + I_{gdov}$$

$$I_S = I_S^{(i)} - (1 - IIPARTITION)I_b - I_{gcs}S_g(x_g) - I_{gsov}$$

$$I_D = I_d^{(i)} + I_b - I_{gcd}S_g(x_g) - I_{gdov}$$

$$I_B = I_B^{(i)} - IIPARTITION \cdot I_b - I_{gc}[1 - S_g(x_g)]$$

where $I_S^{(i)}$, $I_D^{(i)}$ and $I_B^{(i)}$ are terminal currents produced by the intrinsic (core) SPMOS model and

$$S_g(x_g) = \frac{1}{2}\left(1 + \frac{x_g}{\sqrt{x_g^2 + \varepsilon}}\right)$$

The computation of the impact ionization current be turned off by setting the parameter SW_IMPACT to 0 (default) and turned on by setting SW_IMPACT to 1.

Noise Model

Channel Thermal Noise

$$S_{I_d^2} = \frac{4k_B \cdot TABS}{L_{red}^2} \cdot \left(\mu_m Q_{inv} + NDELTA\frac{I_{d/m}\phi}{E_{crit}^2}\right)$$

$$Q_{inv} = WLC_{ox}(Q_I - Q_{CLM})$$

© 2023 Cadence Design Systems, Inc.

$$E_{crit} = VSAT/\mu_m$$

Flicker Noise

if SW_FLICKER = 0 (default)

$$S_{I_d^2}(f) = S_{I_d^2}(drift) + S_{I_d^2}(diff)$$

$$S_{I_d^2}(drift) = \frac{C_{ox}\phi_t I_d \mu_m}{\alpha_m \gamma_{FN} L_{red}^2 f^{NEF}} \left\{ [NOIC \cdot (V_m - 2 \cdot V_*) + B^* - u_n V_*]\alpha_m \phi + \left(A^* - 2B^* \cdot V_* + 3 \cdot NOIC \cdot V_*^2\right) \ln(q_+/q_-) \right\}$$

$$S_{I_d^2}(diff) = \frac{C_{ox}\phi_t^2 I_d \mu_m}{\gamma_{FN} L_{red}^2 f^{NEF}} \{[(NOIC + u_n)\alpha_m \phi + (B^* - 2 \cdot NOIC \cdot V_*) \ln(q_+/q_-)]\}$$

$$\gamma_{FN} = 10^{10}[m^{-1}]$$

$$V_* = \phi_t \left(1 + \frac{G}{\sqrt[2]{x_m + 10^{-6}}}\right)$$

$$A^* = NOIA \cdot q^2/C_{ox}^2$$

$$B^* = NOIB \cdot q/C_{ox}$$

$$u_n = (A^* - B^* \cdot V_* + NOIC \cdot V_*^2)/(q_+ q_-)$$

$$q_+ = V_* + V_m + \alpha_m \phi$$

$$q_- = V_* + V_m - \alpha_m \phi$$

© 2023 Cadence Design Systems, Inc.

If SW_FLICKER is set to 1 then

$$S_{I_d^2} = \frac{KF \cdot g_m^2}{C_{ox} W L f^{NEF}}$$

Series resistance thermal noise

$$S_{R_D} = \frac{4kT}{r_{drain}}$$

$$S_{R_S} = \frac{4kT}{r_{source}}$$

$$S_{R_G} = \frac{4kT}{r_{gate}}$$

where

$$r_{drain} = RSH \cdot NRD$$

$$r_{source} = RSH \cdot NRS$$

$$r_{gate} = RGSH \cdot \frac{W_{drawn}}{L_{drawn} \cdot NF}$$

Channel induced gate noise

$$S_{I_g^2} = DVDZ \cdot \frac{TABS \cdot 16 k_B \pi^2 f^2 W C_{ox} L_{red}^3}{\mu_m \alpha_m H^3} \left[\frac{\phi^4}{1728 H^2} - \phi^2 \left(\frac{1}{720} + \frac{H'}{144 H} \right) + \frac{H H'}{12} \right]$$

where

$$H' = \frac{V_m / \alpha - V_t L_{sat} / L_{red}}{1 + L_{sat} / L_{red}}$$

© 2023 Cadence Design Systems, Inc.

Cross correlation coefficient

$$S_{I_gI_d} = j \cdot \frac{TABS \cdot 8k_B \pi f W C_{ox} L_{red}}{H^2}\left(\frac{H\phi}{12} - \frac{\phi^3}{144H}\right)$$

$$c = \frac{S_{I_gI_d}}{\sqrt{S_{I_g}^2 \cdot S_{I_d}^2}}$$

Gate Induced Drain/Source Leakage Current Model

GIDL Model Equations

For $V_{oxovd} \geq 0$

$$I_{GIDL} = 0$$

For $V_{oxovd} < 0$

$$I_{GIDL} = -A_{GIDL0} V_{db} V_{oxovd} V_{tovd} \exp\left(-\frac{B_{GIDL0}}{V_{tovd}}\right)$$

$$A_{GIDL0} = 10^{13} \cdot AGIDL \cdot W_{eff} L_{OV}$$

$$B_{GIDL0} = BGIDL \cdot (1 + dt \cdot TK_\text{BGIDL})$$

$$V_{tovd} = \sqrt{V_{oxovd}^2 + CGIDL^2 \cdot V_{db}^2 + 10^{-6}}$$

GISL Model Equations

$$I_{GISL} = -A_{GIDL0} V_x V_{oxovs}^2 \exp\left(-\frac{B_{GIDL0}}{V_{tovs}}\right)$$

$$V_{tovs} = \sqrt{V_{oxovs}^2 + CGIDL^2 \cdot V_{sb}^2 + 10^{-6}}$$

© 2023 Cadence Design Systems, Inc.

Scaling Equations

The drawn channel dimensions are denoted as L_{DR}, W_{DR} (in m) or as $L_{DR,\mu m}$, $W_{DR,\mu m}$ (in µm). The minimum device dimensions for a given technology are L_{REF}, W_{REF} (in m) or as $L_{REF,\mu m}$, $W_{REF,\mu m}$ (in µm).

Effective channel length in µm

$$L_{\mu m} = L_{DR,\mu m} - DL0 - DLL \cdot A_L - DLW \cdot B_w$$

where

$$A_L = \frac{1}{L_{REF,\mu m}} - \frac{1}{L_{DR,\mu m}}$$

$$B_W = \frac{1}{W_{REF,\mu m}} - \frac{1}{W_{DR,\mu m}}$$

Effective channel length in m

$$L = 10^{-6} L_{\mu m}$$

Effective channel width in µm,

$$W_{\mu m} = W_{DR,\mu m} - DW0 - DWL \cdot A_l - DWW \cdot B_W - DWP \cdot A_L \cdot B_W$$

Effective channel width in m

$$W = 10^{-6} W_{\mu m}$$

Total oxide capacitance,

$$C_{oxt} = C_{ox}(L + 10^{-6} \cdot DLQ)(W + 10^{-6} \cdot DWQ)$$

Flat-band voltage (which in SPMOS includes reverse short-channel effect if any)

$$V_{fb} = FB0 + \frac{FB1}{W_{\mu m}} + \frac{FB2}{W_{\mu m}^2} + \Delta V_{RSE}$$

© 2023 Cadence Design Systems, Inc.

$$\Delta V_{RSE} = \left(1 + \frac{FB3}{W_{\mu m}} + \frac{FB4}{W_{\mu m}^2}\right) \cdot \left(\frac{FB5}{L_{DR,\,\mu m}} + \frac{FB6}{L_{DR,\,\mu m}^2} + \frac{FB7}{L_{DR,\,\mu m}^3}\right)$$

Drift velocity local parameters

$$K_{sm} = ST0 + ST1 \cdot B_W$$

$$G_{hf} = \left(GH0 + \frac{GH1}{L_{\mu m}} + \frac{GH2}{L_{\mu m}^2}\right) \cdot \left(1 + \frac{GH3}{W_{\mu m}}\right) + \frac{GH4}{L_{\mu m}^2 W_{\mu m}^2}$$

Local parameters for the lateral field gradient

$$F_0 = 1 - \frac{FL1}{L_{\mu m}} - \frac{FL2}{L_{\mu m}^2}$$

$$A_f = \left(AF0 + \frac{AFL}{L_{\mu m}^2}\right) \cdot C_{LW}$$

$$B_f = min\left\{\frac{BFL}{L_{\mu m}^2}, \frac{1 - F_0}{F_0 + 0.01}\right\}$$

$$C_f = \left(CF0 + \frac{CFL}{L_{\mu m}^2}\right)\left(1 + KL \cdot \frac{AL}{L_{\mu m}}\right) C_{LW}$$

and

$$C_{LW} = \frac{1}{1 + KW / W_{\mu m}}$$

Mobility model parameter

$$\mu_E = MU1\left(1 + \frac{MU1W}{W_{\mu m}}\right)$$

$$\theta_{MU} = MU2\left(1 + \frac{MU3}{W_{\mu m}}\right)$$

© 2023 Cadence Design Systems, Inc.

Mobility model parameter (correction for “non-universality”)

$$X_{cor} = NU0 + \frac{NUL}{L_{\mu m}}(1 + NUW \cdot W_{\mu m})$$

Bias-independent part of the series resistance

$$R_{t1} = R0 + R1 \cdot A_L + R2 \cdot B_W + R3 \cdot A_L \cdot B_W$$

Constant used to describe gate bias dependence of the series resistance

$$R_g = R4 + R5 \cdot A_L + R6 \cdot W_{\mu m}$$

Triode-saturation transition variable

$$a_x = \frac{AS0}{1 + ASL/L_{\mu m}}$$

Characteristic length of the quai-2D theory

$$L_{q2d} = (1 + GDL \cdot L_{\mu m})(CLM0 + CLM1 \cdot A_L + CLM2 \cdot B_W)\sqrt{2 \cdot 10^{-7}\varepsilon_{si}/C_{OX}}$$

Subthreshold slope parameter

$$cT = 1 + \frac{T_n}{TABS} \cdot \frac{ITL}{L_{\mu m}^2}$$

Substrate doping variable

$$D_{nsubL} = (1 + NPKT \cdot A_L)^{-1}$$

Halo-doping effect parameters

$$Hl01 = GDS1 + GDS1L \cdot L_{DR,\,\mu m} + GDS1A \cdot A_L$$

$$Hl02 = GDS2 + GDS2L \cdot L_{DR,\,\mu m} + GDS2A \cdot A_L$$

Effective doping

© 2023 Cadence Design Systems, Inc.

$$Nsub = NSUB\left[1 + \frac{LPKT}{L_{\mu m}}(1 - e^{-L_{\mu m}/(YPKT)})\right]$$

Temperature Dependence (-55°°° to 150°°°)

SPMOS uses up to 13 temperature coefficients.×

Flat-band voltage: TK_VFB0, TK_VFBL, TK_VFBW, TK_VFBP.

Mobility: TK_MU0, TK_MUW, TK_MUL, TK_MUP, TK_MU1, TK_THM, TK_CS.

Saturation velocity: TK_VS, TK_AS.

Coefficients TK_VFBL, TK_VFBW, TK_VFBP, TK_MUL, TK_MUP and TK_AS are expected to be zero for mature processes.

The temperature dependence of bulk and surface potentials is not adjusted and is obtained essentially from the first principles. The temperature dependence of the flat-band voltage, mobility and saturation velocity is as follows. In these equations Tn is nominal temperature and

$$\Delta T = TABS - T_n$$

Flat-band voltage

$$V_{fb} = V_{fb}(T_n) + \frac{k_B \Delta T}{q}\left(TK_\mathrm{VFB} + \frac{TK_\mathrm{VFBL}}{L_{\mu m}} + \frac{TK_\mathrm{VFBW}}{W_{\mu m}} + \frac{TK_\mathrm{VFBP}}{W_{\mu m}L_{\mu m}}\right)$$

Mobility

$$\mathrm{MU0} = \mathrm{MU0}(T_n)\left(\frac{T_n}{TABS}\right)^{n_{\mu 0}}$$

$$n_{\mu 0} = TK_\mathrm{MU0} + \frac{\Delta T}{T_n}\left(\frac{TK_\mathrm{MUL}}{L_{\mu m}} + \frac{TK_\mathrm{MUW}}{W_{\mu m}} + \frac{TK_\mathrm{MUP}}{W_{\mu m}L_{\mu m}}\right)$$

$$\theta_{mu} = \theta_{mu}(T_n)\left(\frac{T_n}{TABS}\right)^{TK_\mathrm{THM}}$$

$$\mu_E = \mu_E(T_n)\frac{1 + TK_\mathrm{MU1}\exp(\Delta T/20)}{1 + TK_\mathrm{MU1}}$$

© 2023 Cadence Design Systems, Inc.

$$X_{cor} = X_{cor}(T_n)\left(\frac{T_n}{TABS}\right)^{n_{\mu 0}}$$

$$CS = CS(T_n)\left(\frac{T_n}{TABS}\right)^{TK_\mathrm{CS}}$$

Saturation velocity

$$VSAT = VSAT(T_n)(1 + TK_\mathrm{VS} \cdot \Delta T)$$

$$G_{hf} = G_{hf}(T_n)\frac{1 + TK_\mathrm{VS}/W_{\mu m}}{1 + (TK_\mathrm{VS}/W_{\mu m})\exp(\Delta T/20)}$$

The default values and ranges for temperature coefficients are given in the table below.

Table 35-1 Temperature Coefficients

Parameter	Unit	Description	Default	MIN	MAX
TK_VFB0	None	V_{fb}(T) parameter	0	None	None
TK_VFBL	µm	V_{fb}(T) scaling parameter (L)	0	None	None
TK_VFBW	µm	V_{fb}(T) scaling parameter (W)	0	None	None
TK_VFBP	μm^2	V_{fb}(T) scaling parameter (LW)	0	None	None
TK_MU0	None	MU0(T) parameter	1.5	See Note [1]	
TK_MUL	µm	MU0(T) scaling parameter (L)	0		
TK_MUW	µm	MU0(T) scaling parameter (W)	0		
TK_MUP	μm^2	MU0(T) scaling parameter (LW)	0		
TK_MU1	None	μ_E(T) parameter	0	0	0.1
TK_THM	None	θ_{mu}(T) parameter	0	-5	5
TK _CS	None	CS(T) parameter	0	-5	5

© 2023 Cadence Design Systems, Inc.

TK_VS	K^{-1}	VSAT(T) parameter	0	-0	005
TK_AS	µm	A_s(T) parameter	0	0	0.1

1. Instead of limiting TK_MU0, TK_MUL, TK_MUW and TK_MUP, SPMOS sets

$$n_{\mu 0} = min\left\{5, max\left[-5, TK_\mathrm{MU0} + \frac{\Delta T}{T_n}\left(\frac{TK_\mathrm{MUL}}{L_{\mu m}} + \frac{TK_\mathrm{MUW}}{W_{\mu m}} + \frac{TK_\mathrm{MUP}}{L_{\mu m} W_{\mu m}}\right)\right]\right\}$$

Parameter Descriptions

Table 35-2 Process Parameters Group

Parameter	Unit	Description	Default	MIN	MAX
ITL	μm^2	Interface states scaling factor	0	0	$2P_L^2 L_{CLAMP}^2, \mu m$
LPKT	µm	Pocket length	0	$-\frac{3}{4}PL_L L_{CLAMP}, \mu m$	$9L_{CLAMP}, \mu m$
NP	cm^{-3}	Polysilicon doping	10^{22}	$max(3 \cdot 10^{19}, 80/TOX^2)$ (See Note[1])	None
NSUB	cm^{-3}	Substrate doping	$5 \cdot 10^{17}$	10^{15}	$5 \cdot 10^{18}$
QMC None	None	QM correction factor	0	0	$min(0.6, 3 \cdot 10^{26} \cdot TOX/\mathrm{NSUB})$
TOX	m	Oxide thickness	$4 \cdot 10^{-9}$	10^{-9}	$2 \cdot 10^{-7}$

1. Setting NP=0 or NP > $10^{28} m^{-3}$ turns off polysilicon depletion effect.

At present, PL = 0.2.

© 2023 Cadence Design Systems, Inc.

Table 35-3 Effective Geometry Group

Parameter	Unit	Description	Default	MIN	MAX
DL0	µm	Channel length offset	0	See Note[1]	
DLL	μm^2	Channel length adjustment (L)	0		
DLW	μm^2	Channel length adjustment (W)	0	See Note[2]	
DW0	µm	Channel width offset	0		
DWL	μm^2	Channel width adjustment (L)	0		
DWW	μm^2	Channel width adjustment (W)	0		
DWP	μm^3	Channel width perimeter factor	0		
DLQ	µm	Decoupling parameter	0	$-L_{\mu m}/2$	none
DWQ	µm	Decoupling parameter	0	$-W_{\mu m}/2$	none

1. Instead of limiting the values of DL0, DLL and DLW, SPMOS sets the channel length offset as

   $$DL_{\mu m} = DLO + DLL \cdot A_L + DLW \cdot B_W$$

   and the effective channel length (in µm) as

   $$L_{\mu m} = max\{L_{DR,\,\mu m} - DL_{\mu m}, P_L L_{CLAMP,\,\mu m}\}$$

2. Instead of limiting parameter values of DW0, DWL, DWW and DWP, SPMOS sets the channel width offset as

   $$DW_{\mu m} = DW0 + DWL \cdot A_L + DWW \cdot B_W + DWP \cdot A_L \cdot B_W$$

   and the effective channel length (in µm) as

   $$W_{\mu m} = max\{W_{DR,\,\mu m} - DW_{\mu m}, P_W L_{CLAMP,\,\mu m}\}$$

   At present, P_w=1/4.

© 2023 Cadence Design Systems, Inc.

Table 35-4 Mobility Group

Parameter	Unit	Description	Default	MIN	MAX
MU0	cm^2/Vs	Low-field mobility	500	0.01	10^4
NU0	V^{-1}	Non-universality factor	0	0	1
NUL	μm	Non-universality factor (L)	0	See Note[1]	
NUW	μm^{-1}	Non-universality factor (W)	0		
MU1	m/V	Magnitude of the vertical field dependence	0.5	0	$5 \cdot 10^8 TOX$
MU1W	μm	Scaling parameter (W)	0	$-0.9 P_W W_{CLAMP} \mu m$	$0.9 P_W W_{CLAMP} \mu m$
MU2	None	Sharpness of the vertical field dependence	1.5	0	3
MU3	μm	Scaling parameter (W)	0	$-0.9 P_W W_{CLAMP} \mu m$	$0.9 P_W W_{CLAMP} \mu m$
CS	None	Coulomb scattering	0	0	10

1. Instead of limiting NU0, NUL and NUW, SPMOS sets

$$X_{cor} = max\{X_{cor}, 0\}$$

© 2023 Cadence Design Systems, Inc.

Table 35-5 Series Resistance Group

Parameter	Unit	Description	Default	MIN	MAX
R0	$\Omega \cdot m$	Fixed component of series resistance	$2 \cdot 10^{-3}$	See Note[1]	
R1	$\Omega \cdot m \cdot \mu m$	Scaling factor (L)	0		
R2	$\Omega \cdot m \cdot \mu m$	Scaling factor (W)	0		
R3	$\Omega \cdot m \cdot \mu m^2$	Scaling factor (L,W)	0		
R4	V^{-1}	Gate bias dependence	0	0	None
R5	$\mu m/V$	Scaling factor (L) gate bias dependence	0.02	$-\frac{P_L}{2}R_4 L_{CLAMP,\mu m}$	$\frac{R_4}{2A_{mr}}$
R6	$\mu m/V$	Scaling factor (W) for gate bias dependence	0	See Note[2]	
RB	V^{-1}	Back bias factor	0	0	1.0

1. Instead of limiting the values of R0, R1, R2, and R3, SPMOS sets

$$R_{t1} = max\{R_0 + R_1 \cdot A_L + R_2 \cdot B_W + R_3 \cdot A_L \cdot B_W, 0\}$$

2. Instead of limiting the values of R6, SPMOS sets

$$R_g = max\{R_4 + R_5 \cdot A_L + R_6 \cdot W_{\mu m}, 0\}$$

Table 35-6 Velocity Saturation Group

Parameter	Unit	Description	Default	MIN	MAX
VSAT	m/s	Saturation velocity	80,000	50,000	150,000
ST0	V^{-1}	Gate bias dependence of saturation velocity	0	0	0.3
ST1	$\mu m/V$	Adjustment of saturation velocity (W)	0	$ST1_{min}$ See Note[1]	$ST1_{max}$ See Note[2]

© 2023 Cadence Design Systems, Inc.

Parameter	Unit	Description	Default	MIN	MAX
STX	V^{-1}	Back bias dependence of saturation velocity	0	0	1
GH0	None	Grotjohn/Hofflinger (GH) factor	0.5	0.05	5
GH1	μm	GH Scaling parameter (L^{-1})	0	See Note[3]	
GH2	μm^2	GH Scaling parameter (L^{-2})	0		
GH3	μm^3	GH Scaling parameter ($L^{-2}W^{-1}$)	0		
GH4	μm^4	GH Scaling parameter ($L^{-2}W^{-2}$)	0		
AS0	None	Transition from triode to saturation	12	6	100
ASL	None	Scaling factor (L) for triode-saturation	0.6	See Note[4]	
S0	None	V_{dsat} adjustment	0.98	0.9	0.99

1. $ST1_{min} = -min\{(0.3 - ST0)/B_{mr}, ST0 \cdot W_{CLAMP,\mu m}\}$

2. $ST1_{max} = min\{(0.3 - ST0)W_{CLAMP,\mu m}, ST0/B_{mr}\}$

3. Instead of limiting the values of GH1, GH2, GH3, and GH4, SPMOS forces G_{hf} to be in the range [0.05, 5]

$$G_{hf} = min\left\{5, max\left[0.05, \left(GH0 + \frac{GH1}{L_{\mu m}} + \frac{GH2}{L_{\mu m}^2}\right)\left(\left(1 + \frac{GH3}{W_{\mu m}}\right) + \frac{GH4}{L_{\mu m}^2 W_{\mu m}^2}\right)\right]\right\}$$

4. Instead of limiting the values of ASL, SPMOS forces a_x to be in the range [2,20]

$$a_x = min\{20, max\{2, a_x\}\}$$

© 2023 Cadence Design Systems, Inc.

Table 35-7 Flat-band Voltage Group

Parameter	Unit	Description	Default
FB0	V	V_{fb} for long wide devices $L, W \to \infty$	-1
FB1	$V \cdot \mu m$	Scaling parameter (W^{-1})	0
FB2	$V \cdot \mu m^2$	Scaling parameter (W^{-2})	0
FB3	μm	RSE parameter (W^{-1})	0
FB4	μm^2	RSE parameter (W^{-2})	0
FB5	$V \cdot \mu m$	RSE parameter (L^{-1})	0
FB6	$V \cdot \mu m^2$	RSE parameter (L^{-2})	0
FB7	$V \cdot \mu m^2$	RSE parameter (L^{-3})	0

There are no limits on flat-band voltage parameters.

Table 35-8 Lateral Gradient Factor Group

Parameter	Unit	Description	Default	MIN	MAX
FL1	μm	Scaling parameter for F_0	0.1	See Note[1]	
FL2	μm^2	Scaling parameter for F_0	0.01		
AF0	V^{-1}	Scaling parameter for A_f	0.004	0	10
AFL	$\mu m^2/V$	Scaling parameter for A_f	0	$-AF0 \cdot P_L^2 L_{CLAMP, \mu m}^2$	10
BFL	$\mu m^2/V$	Scaling parameter for B_f	0.015	0	10
CF0	V^{-1}	Scaling parameter for C_f	0.0005	0	10
CFL	$\mu m^2/V$	Scaling parameter for C_f	0.01	$-CF0 \cdot P_L^2 L_{CLAMP, \mu m}^2$	10
KL	μm^2	Scaling parameter for C_{LW}	0	-KL0 (See Note[2])	KLO

© 2023 Cadence Design Systems, Inc.

Parameter	Unit	Description	Default	MIN	MAX
KW	μm	Scaling parameter for C_{LW}	0	$-0.9P_W W_{CLAMP,\,\mu m}$	10
DF	None	Sharpness of f(V_{ds}) dependence	0	0	3
EF	None	Sharpness of f(V_{sb}) dependence	0	0	3

1. Instead of limiting the values of FL1 and FL2, SPMOS forces F_0 to be in the range [0.001, 1]

$$F_0 = min\{1, max\{0.001, F_0\}\}$$

2. Instead of limiting the values of GDS1 and GDS2, SPMOS forces

$$\frac{\partial}{\partial V_{dsx}}\left(\frac{F_0}{f_0} - 1 - B_f V_{sbx1}\right) > 0$$

$$KL0 = min\left\{3.6L^2_{CLAMP,\,\mu m},\, 0.9L_{CLAMP,\,\mu m}/A_{mr}\right\}$$

Table 35-9 Channel Length Modulation Group

Parameter	Unit	Description	Default	MIN	MAX
CLM0	None	L_{q2d} parameter	0.1	0	none
CLM1	μm	L_{q2d} scaling parameter (L)	0	$-\frac{1}{2}CLM0 \cdot L_{CLAMP,\,\mu m}$	$min\{10, CLM0/2A_{mr}\}$
CLM2	μm	L_{q2d} scaling parameter (W)	0	$-\frac{1}{2}CLM0 \cdot W_{CLAMP,\,\mu m}$	$min\{10, CLM0/2B_{mr}\}$
CLM3	V^{-1}	Logarithm dependence factor	10	0	1000
GDL	μm^{-1}	Scaling parameter (L)	0	0	0.9

New Parameters for SPMOS Version 34

The following parameters have been added to version 34.

© 2023 Cadence Design Systems, Inc.

I

Parameter	Unit	Description	Default	MIN	MAX
NCG		Instance parameter for factor of Rgate	1	1	2
SW_GIDL		Flag og gidl	0	0	1
IT0		Interface states scaling factor	0	0	2
NPKT	um	Effective doping parameter	1.0	0	2
NSLP	1/V	Effective doping parameter	0	0	2
YPKT		Effective doping parameter	0.001	0.001	2
VNSUB	V	Effective doping parameter	0		
GDS1		V_{ds} dependence of G_{ds} slope	0		
GDS2		V_{ds} dependence of G_{ds} slope	0		
GDS1L	$1/\mu m$	Scaling parameter for Hlo1	0		
GDS2L	$1/\mu m$	Scaling parameter for Hlo2	0		
GDS1A	μm	Scaling parameter for Hlo1	0		

© 2023 Cadence Design Systems, Inc.

Parameter	Unit	Description	Default	MIN	MAX
GDS2A	μm	Scaling parameter for Hlo1	0		
TK_BGIDL	1/K	Temperature dependence	0.0	0.0	1.0
TK_IIA2		Substrate current scaling parameter	0.0	0.0	1.0
KGOV		Decouples tunneling and CV overlap fitting	1	0.1	10
CHIB	eV	Band offset	3.13	2.5	4
AGIDL		I_{GIDL} coefficient	0.7	0	
BGIDL	V	Tunneling barrier adjustment	28	1	100
CGIDL	1/V	Lateral field dependence	0.007	0	1
IIA1W	$\mu m / V^{1/2}$	Substrate current scaling parameter	0	-1	1
IIA1P	$\mu m / V^{1/2}$	Substrate current scaling parameter	0	-1	1

Parameters with Different Default Values for SPMOS Version 34

Model Parameter	Old Default Value	New Default Value
noia	0.0	1.0e+20
noib	0.0	5.0e+04
noic	0.0	1.4e-12

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

36

MOS Level-0 Transistor (mos0)

The MOS0 model is a simplified MOS level-1 model. The MOS0 DC drain current model is different from the Shichman and Hodges model because body effects are not modeled in MOS0. The intrinsic MOS gate capacitances are replaced by the following linear overlap capacitances:

- Gate to source/drain (`capmod` = `overlap`)
- Gate to bulk (`capmod` = `bulk`
- Gate, source, and drain to ground (`capmod` = `gnd`)

MOS0 is usually used as a MOS switch. This model recognizes all the MOS and BSIM instance parameters but only uses `l` and `w`, ignoring all other parameters. MOS0 transistors require that you use a model statement.

This device is not supported within altergroup.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Sample Instance Statement

```
mp1 (0 1 2 2) pchmod0 l=2u w=30u ad=120p as=75p pd=36u ps=6u
```

Instance Parameters

`w (m)`	Channel width.
`l (m)`	Channel length.
`m=1`	Multiplicity factor (number of MOSFETs in parallel).
`trise=0.0 K`	Temperature rise from ambient
`dtemp=0.0 K`	Alias for `trise`.

© 2023 Cadence Design Systems, Inc.

Model Syntax

```
model modelName mos0 parameter=value ...
```

Sample Model Statement

```
model pchmod0 mos0 type=p vto=-0.683 tox=0.21e-7 ld=0.45e-6 tnom=27
```

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

Drain current model parameters

`vto=0 V`	Threshold voltage at zero body bias.
`kp=2.0718e-5 A/V`^{2}	Transconductance parameter.
`lambda=0.02 1/V`	Channel length modulation parameter.
`tox=1e-7 m`	Gate oxide thickness.
`ld=0 m`	Lateral diffusion.
`wd=0 m`	Field-oxide encroachment.

Charge model selection parameters

`capmod=gnd`	Intrinsic charge model. Possible values are `none`, `overlap`, `bulk`, or `gnd`.

Temperature parameters

`tnom (C)`	Parameters measurement temperature. Default set by `options`.
`trise=0 C`	Temperature rise from ambient.

© 2023 Cadence Design Systems, Inc.

Default device parameters

`w=3e-6 m`	Default channel width.
`l=3e-6 m`	Default channel length.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.
`id (A)`	Resistive drain current.
`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`vbs (V)`	Bulk-source voltage.
`vth (V)`	Threshold voltage.
`vdsat (V)`	Drain-source saturation voltage.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`cgate (F)`	Gate-Ground capacitance.
`ron (Ω)`	On-resistance.
`pwr (W)`	Power at op point.

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

37

MOS Level-15 Transistor (mos15)

The MOS15 model is the AMS level 15 model which is the modified Berkeley SPICE level-2 model with the DC model replaced by that of AMS. It is an analytical one-dimensional model that incorporates most of the second-order small-size effects. A smoother version of the level-15 model (with continuous Gds at Vdsat) was also developed. Three charge models are available. MOS15 transistors require the use of a model statement.

This device is not supported within altergroup.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so.

Instance Syntax

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

w (m)	Channel width.
l (m)	Channel length.
as (m^2)	Area of source diffusion.
ad (m^2)	Area of drain diffusion.
ps (m)	Perimeter of source diffusion.
pd (m)	Perimeter of drain diffusion.
nrd (m/m)	Number of squares of drain diffusion.
nrs (m/m)	Number of squares of source diffusion.
ld (m)	Length of drain diffusion region.
ls (m)	Length of source diffusion region.
m=1	Multiplicity factor (number of MOSFETs in parallel).

© 2023 Cadence Design Systems, Inc.

region=triode	Estimated operating region. Spectre generates output number (0-3) in a rawfile. Possible values are off, triode, sat, or subth.
trise	Temperature rise from ambient.

Model Syntax

```
model modelName mos15 parameter=value ...
```

Model Parameters

Device type parameters

ype=n	Transistor type. Possible values are n or p.

Drain current model parameters

vto=0.5 V	Threshold voltage at zero body bias.
kp=2.0718e-5 A/V^2	Transconductance parameter.
lambda=0.5 1/V	Channel length modulation parameter.
phi=0.7 V	Surface potential at strong inversion.
gamma=1.0 $\sqrt{V}$	Body-effect parameter.
uo=600 $cm^2/V\ s$	Carrier surface mobility.
vmax=8.0e4 m/s	Carrier saturation velocity.
ucrit=2.0e6 V/cm	Critical field for mobility degradation.
uexp=0	Critical field exponent for mobility degradation.
utra=0 1/V	Transverse field for mobility.
neff=1	Total channel charge coefficient.
delta=0	Width effect on threshold voltage.

© 2023 Cadence Design Systems, Inc.

Process parameters

`nsub=1.13e16 cm^-3`	Channel doping concentration.
`nss=0 cm^-2`	Surface state density.
`nfs=0 cm^-2`	Fast surface state density.
`tpg=+1`	Type of gate (+1 = opposite of substrate, -1 = same as substrate, 0 = aluminum).
`tox=1e-7 m`	Gate oxide thickness.
`ld=0 m`	Lateral diffusion.
`wd=0 m`	Field-oxide encroachment.
`xw=0 m`	Width variation due to masking and etching.
`xl=0 m`	Length variation due to masking and etching.
`xj=0.15e-6 m`	Source/drain junction depth.

Impact ionization parameters

`ai0=0 1/V`	Impact ionization current coefficient.
`lai0=0 µm/V`	Length sensitivity of `ai0`.
`wai0=0 µm/V`	Width sensitivity of `ai0`.
`bi0=0 V`	Impact ionization current exponent.
`lbi0=0 µm V`	Length sensitivity of `bi0`.
`wbi0=0 µm V`	Width sensitivity of `bi0`.

Overlap capacitance parameters

`cgso=0 F/m`	Gate-source overlap capacitance.
`cgdo=0 F/m`	Gate-drain overlap capacitance.
`cgbo=0 F/m`	Gate-bulk overlap capacitance.
`meto=0 m`	Metal overlap in fringing field.

© 2023 Cadence Design Systems, Inc.

Charge model selection parameters

`capmod=bsim`	Intrinsic charge model. Possible values are `none`, `meyer`, `yang`, or `bsim`.
`xpart=1`	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.
`xqc=0`	Drain/source channel charge partition in saturation for charge models, e.g. use 0.4 for 40/60, 0.5 for 50/50, 0 for 0/100.

Parasitic resistance parameters

`rs=0` Ω	Source resistance.
`rd=0` Ω	Drain resistance.
`rsh=0` Ω`/sqr`	Source/drain diffusion sheet resistance.
`rss=0` Ω `m`	Scalable source resistance.
`rdd=0` Ω `m`	Scalable drain resistance.
`rsc=0` Ω	Source contact resistance.
`rdc=0` Ω	Drain contact resistance.
`minr=0.1` Ω	Minimum source/drain resistance.
`ldif=0 m`	Lateral diffusion beyond the gate.
`hdif=0 m`	Length of heavily doped diffusion.
`lgcs=0 m`	Gate-to-contact length of source side.
`lgcd=0 m`	Gate-to-contact length of drain side.
`sc=`∞ `m`	Spacing between contacts.

Junction diode model parameters

`js (A/m`^{2}`)`	Bulk junction reverse saturation current density.
`is=1e-14 A`	Bulk junction reverse saturation current.
`n=1`	Junction emission coefficient.

© 2023 Cadence Design Systems, Inc.

`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*iabstol. Possible values are `no` or `yes`.
`imax=1 A`	Explosion current.
`jmax=1e8 A/m`^{2}	Explosion current density.

© 2023 Cadence Design Systems, Inc.

Junction capacitance model parameters

`cbs=0 F`	Bulk-source zero-bias junction capacitance.
`cbd=0 F`	Bulk-drain zero-bias junction capacitance.
`cj=0 F/m`^{2}	Zero-bias junction bottom capacitance density.
`mj=1/2`	Bulk junction bottom grading coefficient.
`pb=0.8 V`	Bulk junction built-in potential.
`fc=0.5`	Forward-bias depletion capacitance threshold.
`cjsw=0 F/m`	Zero-bias junction sidewall capacitance density.
`mjsw=1/3`	Bulk junction sidewall grading coefficient.
`pbsw=0.8 V`	Side-wall junction built-in potential.
`fcsw=0.5`	Side-wall forward-bias depletion capacitance threshold.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, or `rev`.
`bvj=∞ V`	Junction reverse breakdown voltage.

Temperature effects parameters

`tnom (C)`	Parameters measurement temperature. Default set by options.
`trise=0 C`	Temperature rise from ambient.
`uto=0 C`	Mobility temperature offset.
`ute=-1.5`	Mobility temperature exponent.
`tlev=0`	DC temperature selector.
`tlevc=0`	AC temperature selector.
`eg=1.12452 V`	Energy band gap.
`gap1=7.02e-4 V/C`	Band gap temperature coefficient.
`gap2=1108 C`	Band gap temperature offset.
`f1ex=0`	Temperature exponent for `ucrit`.

© 2023 Cadence Design Systems, Inc.

`lamex=0 1/C`	Temperature parameter for `lambda` and `kappa`.
`trs=0 1/C`	Temperature parameter for source resistance.
`trd=0 1/C`	Temperature parameter for drain resistance.
`xti=3`	Saturation current temperature exponent.
`ptc=0 V/C`	Surface potential temperature coefficient.
`tcv=0 V/C`	Threshold voltage temperature coefficient.
`pta=0 V/C`	Junction potential temperature coefficient.
`ptp=0 V/C`	Sidewall junction potential temperature coefficient.
`cta=0 1/C`	Junction capacitance temperature coefficient.
`ctp=0 1/C`	Sidewall junction capacitance temperature coefficient.

© 2023 Cadence Design Systems, Inc.

Default instance parameters

`w=3e-6 m`	Default channel width.
`l=3e-6 m`	Default channel length.
`as=0 m`^{2}	Default area of source diffusion.
`ad=0 m`^{2}	Default area of drain diffusion.
`ps=0 m`	Default perimeter of source diffusion.
`pd=0 m`	Default perimeter of drain diffusion.
`nrd=0 m/m`	Default number of squares of drain diffusion.
`nrs=0 m/m`	Default number of squares of source diffusion.
`ldd=0 m`	Default length of drain diffusion region.
`lds=0 m`	Default length of source diffusion region.

Noise model parameters

`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`ef=1`	Flicker (1/f) noise frequency exponent.
`noisemod=1`	Noise model selector.

The `imax` (`jmax`) parameter is used to aid convergence and prevent numerical overflow. The junction characteristics of the FET are accurately modeled for current (density) up to `imax` (`jmax`). For currents (density) above `imax` (`jmax`), the junction is modeled as a linear resistor and a warning is printed.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`weff (m)`	Effective channel width.
`leff (m)`	Effective channel length.
`rseff (Ω)`	Effective source resistance.
`rdeff (Ω)`	Effective drain resistance.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.
`region=triode`	Estimated operating region. Spectre generates output number (0-3) in a rawfile. Possible values are `off`, `triode`, `sat`, or `subth`.
`reversed`	Reverse mode indicator. Possible values are `no` or `yes`.
`id (A)`	Resistive drain current.
`ds (A)`	Resistive current from drain to source.
`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`vbs (V)`	Bulk-source voltage.
`vth (V)`	Threshold voltage.
`vdsat (V)`	Drain-source saturation voltage.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`gmbs (S)`	Body-transconductance.
`gameff (√V )`	Effective body effect coefficient.
`betaeff (A/V`^{2}`)`	Effective beta.
`cbd (F)`	Drain-bulk junction capacitance.
`cbs (F)`	Source-bulk junction capacitance.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`cgb (F)`	Gate-bulk capacitance.

© 2023 Cadence Design Systems, Inc.

`ron (Ω)`	On-resistance.
`ib (A)`	Resistive bulk current.
`pwr (W)`	Power at operating point.

© 2023 Cadence Design Systems, Inc.

38

GaAs Model (gaas)

The GaAs MESFET model is derived from the model by H. Statz and others at Raytheon. The model is completely symmetric and is slightly modified to make it conserve charge.

Related Topics

Model Equations

Scaling Effects

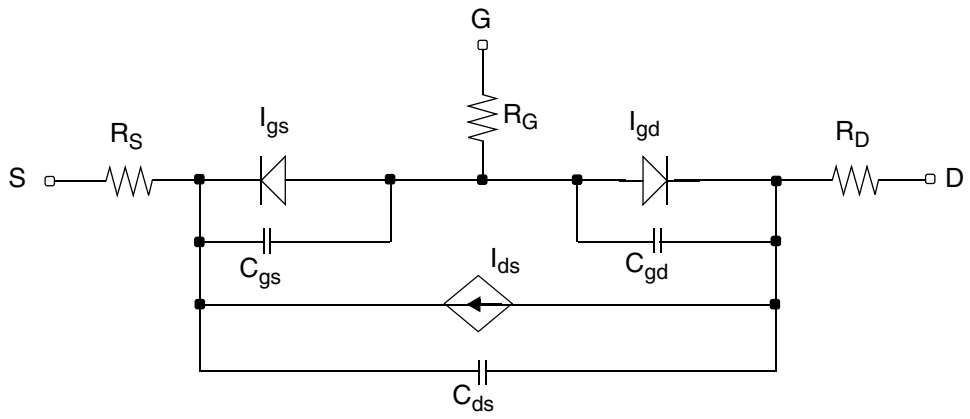
Component Statements

Instance

Model

© 2023 Cadence Design Systems, Inc.

Model Equations



The charge model in GaAs is a charge-conserving model. The capacitances are nonreciprocal.

(38-1)

$$V_{GST} \equiv V_{GS} - vto$$

(38-2)

$$V_{GDT} \equiv V_{GST} - V_{DS}$$

Drain Current for the Subthreshold Region

Note: This equation applies when $V_{GST} \leq 0$.

(38-3)

© 2023 Cadence Design Systems, Inc.

$$I_{DS} = 0$$

Drain Current for the Triode Region

Note: These equations apply when $V_{GST} \geq 0$, $V_{DS} \leq 3/alpha$.

(38-4)

$$I_{DS} = \frac{betaV_{GST}^2}{1 + bV_{GST}}(1 + lambdaV_{DS})(1 - Fac^3)$$

where

(38-5)

$$Fac = 1 - \frac{alphaV_{DS}}{3}$$

Drain Current for the Saturation Region

Note: This equation applies when $V_{GST} \geq 0$ and $V_{DS} \geq 3/alpha$.

(38-6)

$$I_{DS} = \frac{betaV_{GST}^2}{1 + bV_{GST}}(1 + lambdaV_{DS})$$

Gate Junction Currents

(38-7)

© 2023 Cadence Design Systems, Inc.

$$I_{GS(GD)} = \begin{cases} is\left(e^{\frac{V_{GS(GD)}}{nV_t}} - 1\right) & \text{if } V_{GS(GD)} \le V_{Expl} \\ I_{offset} + G_{Expl} V_{GS(GD)} & \text{otherwise} \end{cases}$$

where V_t is the thermal voltage given by

(38-8)

$$V_t = \frac{kT}{q} \quad ,$$

(38-9)

$$V_{Expl} = nV_t \ln\left[1 + \frac{imelt}{is}\right]$$

is the forward explosion voltage,

(38-10)

$$G_{Expl} = \frac{(imelt + is)}{nV_t}$$

is the conductance at V_{Expl}, and

(38-11)

$$I_{offset} = imelt - V_{Expl} G_{Expl}$$

is the current linearly extrapolated to V = 0 from V_{Expl}.

© 2023 Cadence Design Systems, Inc.

Gate Junction Capacitance

(38-12)

$$C_{GS(V)} = \begin{cases} C_{gs,\,Fwd} & \text{if } V_{DS} \geq 1/alpha \\ cgs & \text{if } V_{DS} \leq -1/alpha \\ T_{fs}C_{gs,\,Fwd} + T_{fd}cgs & \text{otherwise} \end{cases}$$

(38-13)

$$C_{GD(V)} = \begin{cases} cgd & \text{if } V_{DS} \geq 1/alpha \\ C_{gd,\,Fwd} & \text{if } V_{DS} \leq -1/alpha \\ T_{fs}cgd + T_{fd}C_{gd,\,Fwd} & \text{otherwise} \end{cases}$$

where

(38-14)

$$C_{GS,\,Fwd} = \begin{cases} \dfrac{cgsV_{GST}}{2\sqrt{1 - V_{ps}/pb}\sqrt{V_{GST}^2 + delta^2}} & \text{if } V_{ps} \leq fc * pb \\ \dfrac{cgsV_{GST}}{2\sqrt{1 - fc}\sqrt{V_{GST}^2 + delta^2}} & \text{otherwise} \end{cases}$$

(38-15)

© 2023 Cadence Design Systems, Inc.

$$C_{GD,\,Fwd} = \begin{cases} \dfrac{cgdV_{GDT}}{2\sqrt{1 - V_{pd}/pb}\sqrt{V_{GDT}^2 + delta^2}} & \text{if } V_{pd} \le fc * pb \\ \dfrac{cgdV_{GDT}}{2\sqrt{1 - fc}\sqrt{V_{GDT}^2 + delta^2}} & \text{otherwise} \end{cases}$$

(38-16)

$$V_{ps} \equiv \frac{1}{2}[V_{GS} + vto + \sqrt{V_{GST}^2 + delta^2}]$$

(38-17)

$$V_{pd} \equiv \frac{1}{2}[V_{GD} + vto + \sqrt{V_{GDT}^2 + delta^2}]$$

(38-18)

$$T_{fs} = \frac{1}{4}[2 + 3alphaV_{DS} - (alphaV_{DS})^3]$$

(38-19)

$$T_{fd} = 1 - T_{fs}$$

Temperature Effect

Junction Potential

(38-20)

© 2023 Cadence Design Systems, Inc.

$$pb = pb_{nom}\left(\frac{T}{Tnom}\right) - 3V_t\ln\left[\frac{T}{Tnom}\right] - E_{g,nom}\left(\frac{T}{Tnom}\right) + E_g$$

Gate Junction Current

(38-21)

$$is = is_{nom}\left(\frac{T}{Tnom}\right)^{xti}\exp\left[\frac{E_{g,nom}}{V_{t,nom}} - \frac{E_g}{V_t}\right]$$

where, if SPICE compatibility is required (set by the options),

(38-22)

$$E_g = 1.16 - \frac{7.02\times10^{-4}T^2}{1108+T}$$

(38-23)

$$E_{g,nom} = 1.16 - \frac{7.02\times10^{-4}Tnom^2}{1108+Tnom}$$

otherwise,

(38-24)

$$E_g = 1.17 - \frac{4.73\times10^{-4}T^2}{636+T}$$

(38-25)

© 2023 Cadence Design Systems, Inc.

$$E_{g,nom} = 1.17 - \frac{4.73 \times 10^{-4} Tnom^2}{636 + Tnom}$$

Noise Model

Source Series Resistance Thermal Noise

(38-26)

$$\overline{i_{R_S}^2} = \frac{4kT}{rs}\Delta f$$

Drain Series Resistance Thermal Noise

(38-27)

$$\overline{i_{R_D}^2} = \frac{4kT}{rd}\Delta f$$

Channel Conductance Thermal and Flicker Noise

(38-28)

$$\overline{i_{DS}^2} = \frac{8kT(g_m + g_{ds})}{3}\left(\frac{3}{2} - \frac{V'_{DS}}{2V_{DSAT}}\right) + kf\frac{I_{DS}^{af}}{f}\Delta f$$

where

(38-29)

© 2023 Cadence Design Systems, Inc.

$$V'_{DS} = MAX(V_{DS}, V_{DSAT})$$

g_m is the transconductance, g_{ds} is the channel conductance, and kf and af are constants for a given device. The Spectre® circuit simulator defaults for kf and af are 0.0 and 1.0, respectively.

Related Topics

GaAs Model (gaas)

Scaling Effects

Component Statements

Instance

Model

Scaling Effects

The following are the Spectre scaling effects:

- is, cgs, cgd, and $beta$ are multiplied by $area$.
- rs and rd are divided by $area$.
- All noises are multiplied by $area$.

Related Topics

GaAs Model (gaas)

Model Equations

Component Statements

Instance

Model

© 2023 Cadence Design Systems, Inc.

Component Statements

This device is supported within altergroups.

There are some convergence problems with this model because of `Cgs` going to zero beyond pinch off. The problems occur when the gate is driven from an inductive source, and there is no other capacitance at the gate. To prevent these problems, avoid setting `Cgd` to zero and add side wall capacitance to the gate-source and gate-drain junctions. A good estimate for these capacitors is C = pi*epsilon*w/2 where w is the gate width in microns and epsilon = 0.116 fF/micron.

Instance

Sample Instance Statement

```
m1 (1 2 0) nmes area=1 m=2
```

Instance Syntax

```
Name  d  g  s ModelName parameter=value ...
```

Instance Parameters

`area=1`	Junction area factor.
`m=1`	Multiplicity factor.
`trise`	Temperature rise from ambient.
`isnoisy=yes`	Should the device generate noise? Possible values are `no` or `yes`.
`region=fwd`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, or `breakdown`.

Related Topics

GaAs Model (gaas)

Model Equations

© 2023 Cadence Design Systems, Inc.

Scaling Effects

Component Statements

Model

Model

Model Syntax

```
model modelName gaas parameter=value ...
```

Sample Model Statement

```
model nmes gaas type=n vto=-2 beta=0.06 lambda=0 b=0.25 rs=3.65 alpha=1.9 rd=1.98
is=1.1e-9 n=1.28 fc=0.5 cgs=0.365e-12
```

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

Drain current parameters

`vto=-2 V`	Pinch off voltage.
`beta=0.0001 A/V`^{2}	Transconductance parameter.
`lambda=0 1/V`	Channel length modulation parameter.
`b=0.3 1/V`	Doping tail extending parameter.
`alpha=2 1/V`	Saturation voltage parameter.

Parasitic resistance parameters

`rd=0` Ω	Drain resistance (/area).
`rs=0` Ω	Source resistance (/area).

© 2023 Cadence Design Systems, Inc.

`rg=0 Ω`	Gate resistance (/area).
`minr=0.1 Ω`	Minimum source/drain/gate resistance.

Junction diode model parameters

`is=1e-14 A`	Gate saturation current (*area).
`n=1`	Emission coefficient for the gate junction.
`imelt=`imax' A`	Explosion current (*area).
`dskip=yes`	Use simple piecewise linear model for diode currents below 0.1*`iabstol`. Possible values are `yes` and `no`.

Junction capacitance model parameters

`capmod=2`	Charge model selector.
`cgs=0 F`	Gate-source zero-bias junction capacitance (*area).
`cgd=0 F`	Gate-drain zero-bias junction capacitance (*area).
`pb=1 V`	Gate junction potential.
`fc=0.5`	Junction capacitor forward-bias threshold.
`delta=0.2 V`	Gate capacitance pinch-off transition width.

Temperature effects parameters

21	`tnom (C)`	Parameters measurement temperature. Default set by options.
22	`trise=0 C`	Temperature rise from ambient.
23	`xti=3`	Temperature exponent for effect on `is`.

© 2023 Cadence Design Systems, Inc.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, or `rev`.
`imax=1 A`	Maximum allowable current (*area).
`bvj=∞ V`	Junction reverse breakdown voltage.

Noise model parameters

`kf=0`	Flicker noise (1/f) coefficient.
`af=1`	Flicker noise (1/f) exponent.

Imax and Imelt:

The `imax` parameter aids in convergence and prevents numerical overflow. The junction characteristics of the device are accurately modeled for the value of the current up to `imax`. If the value of `imax` exceeds during iterations, the linear model is substituted until the current drops below `imax` or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and Spectre prints a warning.

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, given that base and collector currents are composed of many exponential terms, the results become inaccurate and Spectre issues a warning. The junction current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

The `bv` parameter detects the junction breakdown only. The breakdown currents of the junctions are not modeled.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

© 2023 Cadence Design Systems, Inc.

`region=fwd`	Estimated operating region. Spectre generates output number (0-4) in a rawfile. Possible values are `off`, `triode`, `sat`, `subth`, or `breakdown`.
`ids (A)`	Resistive drain current.
`vth (V)`	Threshold voltage.
`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`vdsat (V)`	Drain saturation voltage.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`ig (A)`	Resistive gate current.
`pwr (W)`	Power at operating point.
`meff`	Effective multiplicity factor (m-factor).

Related Topics

GaAs Model (gaas)

Model Equations

Scaling Effects

Component Statements

Instance

© 2023 Cadence Design Systems, Inc.

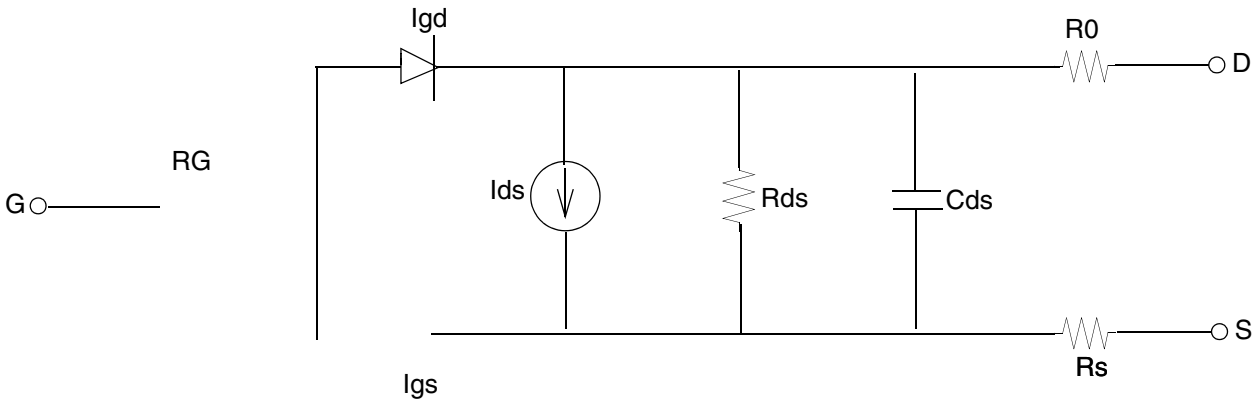
39

TriQuint Owned Models (tom2 and tom3/ tom3v1)

The TOM2 and TOM3/TOM3V1 models are developed by TriQuint.

Circuit Diagrams

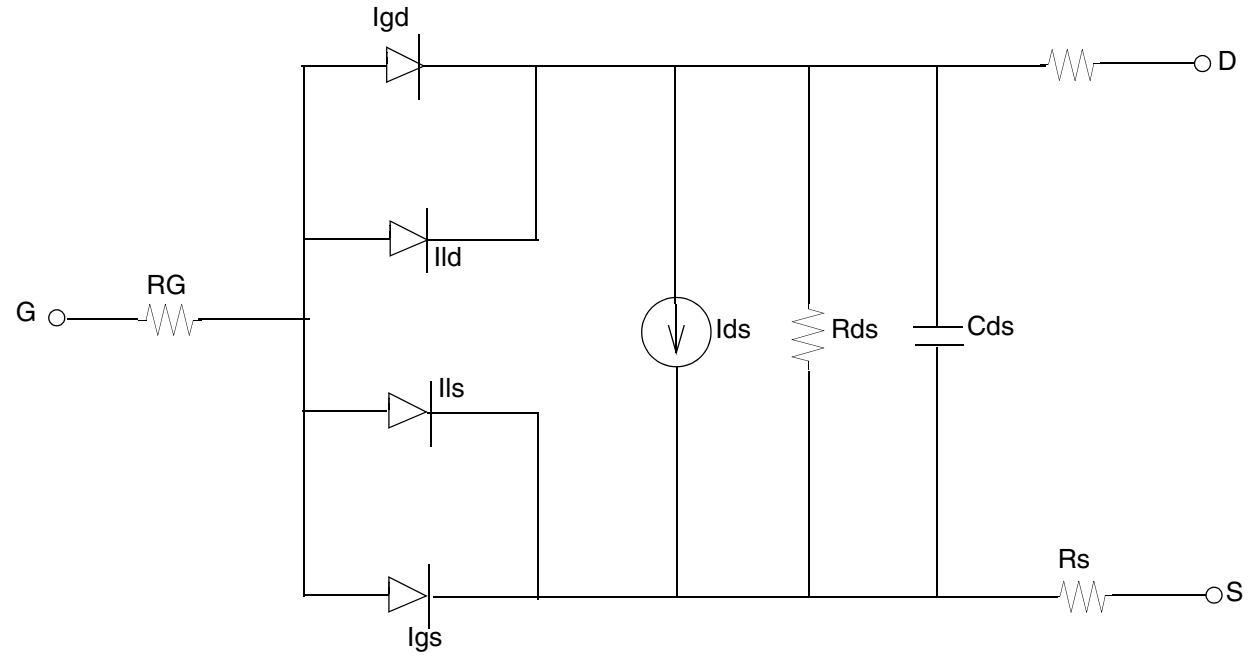
TOM2



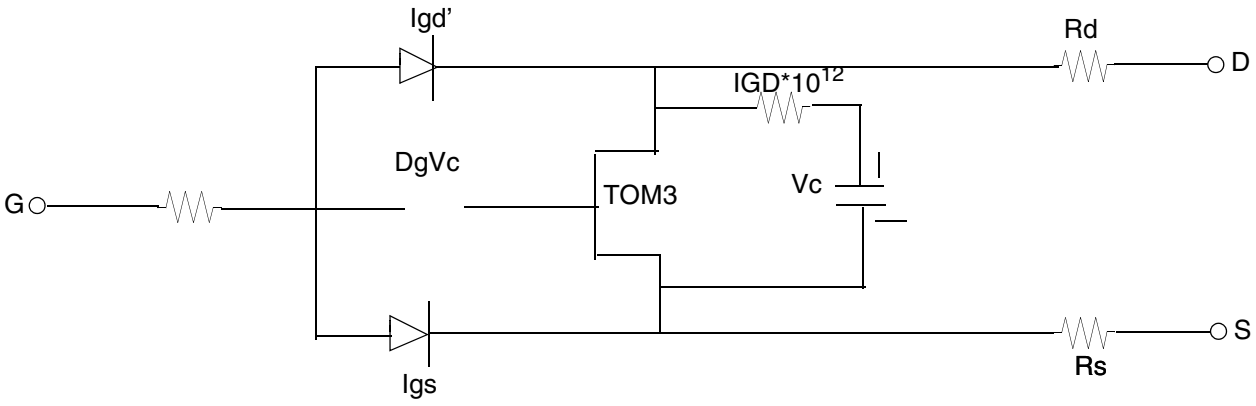
© 2023 Cadence Design Systems, Inc.

TOM3

Spectre Implementation

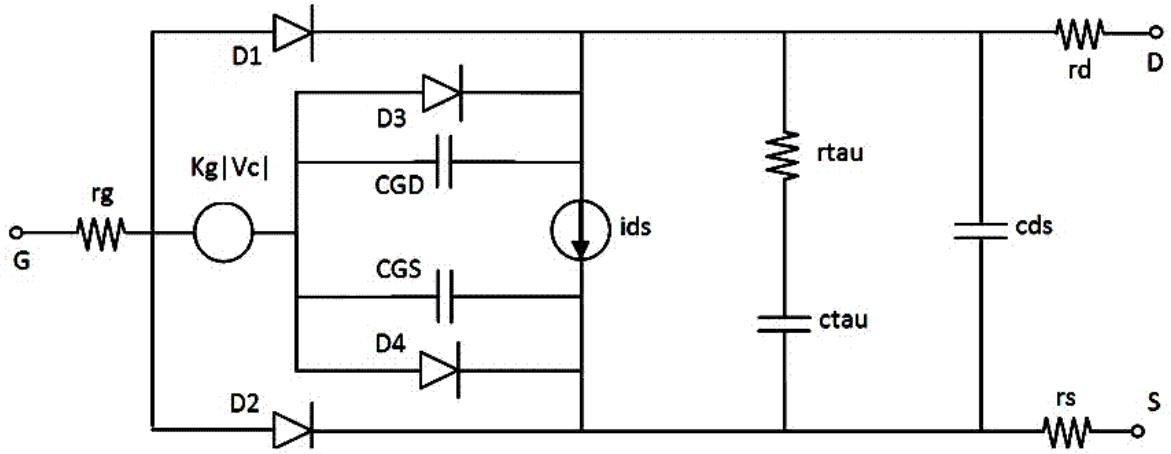


TOM3 with SubCircuit



TOM3V1

© 2023 Cadence Design Systems, Inc.



Related Topics

Model Equations

Scaling Effects

New features from TOM3 to TOM3v1

Model Usage (tom2)

Component Statements

GaAs MESFET (tom3)

Model Equations

Channel Current Ids

TOM2

(39-1)

© 2023 Cadence Design Systems, Inc.

$$I_{DS} = \frac{I_{ds0}}{1 + \delta V_{ds} I_{ds0}}$$

where

(39-2)

$$I_{ds0} = \beta V_{gsteff}^{Q} \frac{\alpha V_{ds}}{\sqrt{(\alpha V_{ds})^2 + 1}}$$

TOM3/TOM3V1

(39-3)

$$I_{DS} = I_0(1 + \lambda V_{ds})$$

where

(39-4)

$$I_0 = \beta (V_G)^{Q} f_k$$

(39-5)

$$f_k = \frac{\alpha V_{ds}}{\left[1 + (\alpha V_{ds})^k\right]^{1/k}}$$

(39-6)

© 2023 Cadence Design Systems, Inc.

$$V_G = QV_{ST}\log[1 + \exp(u)]$$

(39-7)

$$u = \frac{V_{GSI} - V_{TO} + \gamma V_{ds}}{QV_{ST}}$$

(39-8)

$$V_{ST} = V_{ST0}(1 + M_{ST0}V_{ds})$$

Gate Current Ig

TOM2

(39-9)

$$I_{gs} = I_s\left(e^{\frac{V_{gs}}{\eta V_T}} - 1\right)$$

(39-10)

$$I_{gd} = I_s\left(e^{\frac{V_{gd}}{\eta V_T}} - 1\right)$$

TOM3/TOM3V1

(39-11)

© 2023 Cadence Design Systems, Inc.

$$I_{gs} = I_s\left(e^{\frac{V_{gs}}{\eta V_T}} - 1\right)$$

(39-12)

$$I_{gd} = I_s\left(e^{\frac{V_{gd}}{\eta V_T}} - 1\right)$$

(39-13)

$$I_{ls} = I_{LK}\left(1 - e^{\frac{-V_{gsi}}{\varphi LK}}\right)$$

(39-14)

$$I_{ld} = I_{LK}\left(1 - e^{\frac{-V_{gdi}}{\varphi LK}}\right)$$

Gate Capacitance

TOM2

In the TOM2 model, the calculation of capacitances follows the Statz charge model.

(39-15)

© 2023 Cadence Design Systems, Inc.

$$C_{gs} = \frac{C_{gs0}(T)}{\sqrt{1 - V_1/(V_{bi}(T))}} F_1 F_2 + C_{gs0}(T) F_3$$

(39-16)

$$C_{gd} = \frac{C_{gd0}(T)}{\sqrt{1 - V_1/(V_{bi}(T))}} F_1 F_2 + C_{gd0}(T) F_3$$

where

(39-17)

$$F_1 = 0.5 \frac{\partial V_2}{\partial x} \left(1 + \frac{V_2 - V_{toeff}}{\sqrt{(V_2 - V_{toeff})^2 + V_\delta^2}} \right)$$

(39-18)

$$x = V_{gs}, V_{gd}$$

(39-19)

$$F_2 = 0.5 \left[1 + \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + (1/(\alpha(T)))^2}} \right]$$

(39-20)

© 2023 Cadence Design Systems, Inc.

$$F_3 = 1 - F_2$$

(39-21)

$$V_1 = \begin{matrix} A_1, A_1 < V_{max} \\ V_{max}, A_1 \geq V_{max} \end{matrix}$$

(39-22)

$$A_1 = 0.5\left[V_2 + V_{toeff} + \sqrt{(V_2 - V_{toeff})^2 + V_\delta^2}\right]$$

(39-23)

$$V_2 = 0.5\left[V_{gs} + V_{gd} + \sqrt{(V_{gs} - V_{gd})^2 + (1/(\alpha(T)))^2}\right]$$

TOM3/TOM3V1

In the TOM3 model, the low and high power capacitance is combined with a transition function.

High power gate charge/capacitance

(39-24)

$$Q_{GH} = Q_{GQH}\log\left(1 + \frac{I_{ds}}{Q_{GIO}}\right) + Q_{GSH}V_{GSI} + Q_{GDH}V_{GDI}$$

(39-25)

© 2023 Cadence Design Systems, Inc.

$$C_{GSH} = (g_m + g_{ds})\left(\frac{Q_{GQH}}{I_{ds} + Q_{GIO}}\right) + Q_{GSH}$$

(39-26)

$$C_{GDH} = -g_{ds}\left(\frac{Q_{GQH}}{I_{ds} + Q_{GIO}}\right) + Q_{GDH}$$

Low Power Gate Charge

(39-27)

$$Q_{GL} = qgl + Q_{GCL}(V_{GSI} + V_{GDI})$$

where

(39-28)

$$qgl = Q_{GQL}e^{[Q_{GAG}(V_{gsi} + V_{gdi})]}\cosh(Q_{GAD}Vds)$$

(39-29)

$$C_{GSL} = qgl[Q_{GAG} + Q_{GAD}\tanh(Q_{GAD}V_{ds})] + Q_{GCL}$$

(39-30)

$$C_{GDL} = qgl[Q_{GAG} - Q_{GAD}\tanh(Q_{GAD}V_{ds})] + Q_{GCL}$$

Transition Function

(39-31)

© 2023 Cadence Design Systems, Inc.

$$f_T = \exp[-Q_{GCB} I_{ds} V_{ds}]$$

The derivatives are as follows:

(39-32)

$$\frac{\partial f_T}{\partial V_{GSI}} = -Q_{GGB}[I_{ds} + (g_m + g_{ds})V_{ds}]f_T$$

(39-33)

$$\frac{\partial f_T}{\partial V_{GDI}} = Q_{GGB}[I_{ds} + g_{ds} V_{ds}]f_T$$

Combined Gate Charge/Capacitance

(39-34)

$$Q_{GG} = Q_{GL} f_T + Q_{GH}(1 - f_T) + Q_{GG0}(V_{GSI} + V_{GDI})$$

(39-35)

$$C_{GS} = C_{GSL} f_T + C_{GSH}(1 - f_T) + (Q_{GL} - Q_{GH})\left(\frac{\partial f_T}{\partial V_{GSI}}\right) + Q_{GG0}$$

(39-36)

© 2023 Cadence Design Systems, Inc.

$$C_{GD} = C_{GDL} f_T + C_{GDH}(1 - f_T) + (Q_{GL} - Q_{GH})\left(\frac{\partial f_T}{\partial V_{GDI}}\right) + Q_{GG0}$$

TOM3V1

capmod=1

(39-37)

$$I_{CGS} = CGS \frac{dV_{gm,si}}{dt}$$

$$I_{CGD} = CGD \frac{dV_{gm,di}}{dt}$$

capmod=2

(39-38)

$$I_{CGS} = \frac{1}{2} \frac{dQGG}{dt}$$

$$I_{CGD} = \frac{1}{2} \frac{dQGG}{dt}$$

Temperature Effect

(39-39)

$$\alpha(T) = \alpha_0 \cdot 1.01^{\alpha_{tce}\Delta T}$$

(39-40)

© 2023 Cadence Design Systems, Inc.

$$\Gamma(T) = \Gamma_0 + \Gamma_{tc}\Delta T$$

TOM2

(39-41)

$$V_{bi}(T) = V_{bi0} + V_{bitc}\Delta T$$

TOM3/TOM3V1

(39-42)

$$V_{st}(T) = V_{st}(T_{nom}) + T_{V_{st}}(T - T_{nom})$$

(39-43)

$$M_{st}(T) = M_{st}(T_{nom}) + T_{M_{st}}(T - T_{nom})$$

Noise Model

Source Resistance Thermal Noise

(39-44)

$$i^2_{R_s} = \frac{4kT}{Rs}\Delta f$$

Drain Resistance Thermal Noise

(39-45)

© 2023 Cadence Design Systems, Inc.

$$i_{R_d}^2 = \frac{4kT}{Rd}\Delta f$$

Channel Conductance Thermal and Flicker Noise

(39-46)

$$i_{DS}^2 = \frac{8kT(g_m + g_{ds})}{3}\left(\frac{3}{2} - \frac{V_{ds}^{'}}{2V_{DSAT}}\right) + k_f\frac{I_{DS}^{af}}{f}\Delta f$$

where

(39-47)

$$V_{DS}^{'} = MAX(V_{DS}, V_{DSAT})$$

Gate Resistance Thermal Noise (TOM3V1)

(39-48)

$$i_{Rg}^2 = \frac{4kT}{Rd}\Delta f$$

Channel Conductance Thermal and Flicker Noise (TOM3V1)

(39-49)

$$i_{DS}^2 = 4kTg_mP + k_f\frac{I_{DS}^{af}}{f}\Delta f$$

© 2023 Cadence Design Systems, Inc.

Related Topics

TriQuint Owned Models (tom2 and tom3/tom3v1)

Scaling Effects

New features from TOM3 to TOM3v1

Model Usage (tom2)

Component Statements

GaAs MESFET (tom3)

Scaling Effects

The following are the Spectre scaling effects:

- is and $beta$ are multiplied by $area$.
- rs and rd are divided by $area$.
- All noises are multiplied by $area$.

Related Topics

TriQuint Owned Models (tom2 and tom3/tom3v1)

Model Equations

New features from TOM3 to TOM3v1

Model Usage (tom2)

Component Statements

GaAs MESFET (tom3)

New features from TOM3 to TOM3v1

1. Added capmod to run a capacitance or charge based models for the gate-drain and gate-source reactance.
2. Noise implementation is enhanced.

© 2023 Cadence Design Systems, Inc.

Related Topics

TriQuint Owned Models (tom2 and tom3/tom3v1)

Model Equations

Scaling Effects

Model Usage (tom2)

Component Statements

GaAs MESFET (tom3)

Model Usage (tom2)

Instance Syntax

```
Name  d  g  s ModelName parameter=value ...
```

Sample Instance Statement

```
mt1 (2 1 0) tom2mos area=1 region=fwd
```

Model Syntax

```
model modelName tom2 parameter=value ...
```

Sample Model Statement

```
model tom2mos tom2 vto=-0.55 alpha=3.9 beta=0.001 gamma=0.075 delta=100 ng=1 rd=550
rs=550 rg=1 is=0.295e-14 n=1.2 cgs=1.4e-15 cgd=2e-16 cds=3e-16
```

Related Topics

TriQuint Owned Models (tom2 and tom3/tom3v1)

Model Equations

Scaling Effects

New features from TOM3 to TOM3v1

© 2023 Cadence Design Systems, Inc.

Component Statements

GaAs MESFET (tom3)

© 2023 Cadence Design Systems, Inc.

Component Statements

Instance Parameters

`m=1`	Multiplicity factor.
`w=50 µm`	Gate width.
`ng=6`	Number of gate fingers.
`trise=0 C`	Temperature rise from ambient.
`isnoisy=yes`	Should the device generate noise. Possible values are `no` or `yes`.

Model Parameters

`tnom=25 C`	Parameters measurement temperature. Default set by options.
`vto=-2.0 V`	Threshold voltage.
`alpha=3.0 1/V`	Knee-voltage parameter.
`beta=0.05 A/V^q`	Transconductance parameter.
`lambda=0.0 1/V`	Slope of drain characteristic.
`gamma=0.1`	Threshold shifting parameter.
`q=2.0`	Power-law parameter.
`k=3.0`	Knee-function factor.
`vst=0.05 V`	Subthreshold slope.
`mst=0.0 1/V`	Subthreshold slope drain parameter.
`ilk=1.0e-7 A/µm`	Gate leakage diode saturation current (/w).
`plk=2.25 V`	Gate leakage diode potential.
`kgamma=0.33`	Internal vcvs parameter.
`taugd=1.0e-9 s`	Time constant for Ctau.
`ctau=1.0e-15 F`	Darin-to-source dispersion capacitance.
`qgql=5.0e-16 Coul/µm`	Charge parameter.

© 2023 Cadence Design Systems, Inc.

qgqh=-2.0e-16 Coul/µm	Charge parameter.
qgi0=1.0e-16 A/µm	Charge parameter.
qgag=1.0 1/V	Charge parameter.
qgad=1.0 1/V	Charge parameter.
qggb=100.0 µm/W	Charge parameter.
qgcl=2.0e-16 F/µm	Charge parameter.
qgsh=1.0e-16 F/µm	Charge parameter.
qgdh=0.0 F/µm	Charge parameter.
qgg0=0.0 F/µm	Charge parameter.
capmod=1	Capacitance model selector.
cds=0.0 F	Drain-to-source capacitance.
tau=1.0e-12 s	Conduction current delay time.
rd=0.0 Ω µm	Drain resistance (*w).
rg=0.0 Ω µm	Gate resistance (*w).
rgmet=0.0 Ω/µm	Metal resistance in gate (/w).
rs=0.0 Ω µm	Source resistance (*w).
is=1.0e-12 A/µm	Gate diode saturation current (/w).
eta=1.0	Parameter for is.
alphatce=7.7337e-3 1/C	Temperature parameter for alpha.
gammatc=0.0 1/C	Temperature parameter for gamma.
msttc=0.0 1/(VC)	Temperature parameter for mst.

© 2023 Cadence Design Systems, Inc.

`vsttc=0.0 V/C`	Temperature parameter for vst.
`vtotc=-1.49e-4 V/C`	Temperature parameter for vto.
`betatce=0.0 1/C`	Temperature coefficient for beta.
`rdtc=0.0 1/C`	Temperature parameter for rd.
`rstc=0.0 1/C`	Temperature parameter for rs.
`xti=0.0`	Temperature exponent for effect on is.
`eg=1.11 V`	Energy band gap.
`p=0.32`	White noise coefficient.
`af=1.0`	Flicker (1/f) noise exponent.
`kf=0.0`	Flicker (1/f) noise coefficient.
`ffe=1.0`	Flicker (1/f) noise coefficient.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`id (A)`	Drain current.
`ig (A)`	Gate current.
`is (A)`	Source current.
`ids (A)`	Drain-to-source current.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`vth (V)`	Threshold voltage.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`pwr (W)`	Power at operating point.
`vgsi`	Voltage between internal G-S.
`vgdi`	Voltage between internal G-D.
`vgst`	Vgsi after Tau's delay.
`vgdt`	Vgdi after Tau's delay.

Related Topics

TriQuint Owned Models (tom2 and tom3/tom3v1)

Model Equations

Scaling Effects

New features from TOM3 to TOM3v1

Model Usage (tom2)

GaAs MESFET (tom3)

© 2023 Cadence Design Systems, Inc.

GaAs MESFET (tom3)

TOM3 stands for Triquint Own Model version 3. It is an improved GaAs MESFET developed by David H. Smith.

This device is supported within altergroups.

Sample Instance Statement

```
mt1 (2 1 0) tom3mos area=1 region=fwd
```

Sample Model Statement

```
model tom3mos tom3 vto=-0.55 alpha=3.9 beta=0.001 gamma=0.075 delta=100 rd=550
rs=550 rg=1 is=1.0e-30 cds=3e-16
```

Instance Syntax

```
Name  d  g  s ModelName parameter=value ...
```

Instance Parameters

`area=1`	Junction area factor.
`m=1`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise? Possible values are `yes` and `no`.
`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, or `subth`.
`trise=0 C`	Temperature rise from ambient.

Model Syntax

```
model modelName tom3 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

Drain current parameters

`vto=-2.5 V`	Threshold voltage.
`alpha=2 1/V`	Knee-voltage parameter.
`beta=0.1 A/V`^{2}	Transconductance parameter.
`gamma=0 1/V`	Threshold shifting parameter.
`lambda=0.0 V`	Slope of drain characteristic.
`q=2`	Power-law parameter.
`k=2.0`	knee-function factor.

Subthreshold parameters

`vst=1 V`	Subthreshold slope.
`mst=0 1/V`	Subthreshold slope drain parameter.

Parasitic resistance parameters

`rd=0` Ω	Drain resistance (/area).
`rs=0` Ω	Source resistance (/area).
`rg=0` Ω	Gate resistance (/area).
`minr=0.1` Ω	Minimum source/drain/gate resistance.

Junction diode model parameters

`is=0.0 A`	Gate diode saturation current (*area).
`n=1`	Emission coefficient for the gate junction.

© 2023 Cadence Design Systems, Inc.

`imelt=`imax' A`	Explosion current (*area).
`dskip=yes`	Use simple piece-wise linear model for diode currents below 0.1*`iabstol`. Possible values are `no` or `yes`.
`ilk=0.0 A`	Gate leakage diode saturation current (*area).
`plk=1.0 V`	Gate leakage diode potential.

© 2023 Cadence Design Systems, Inc.

Junction capacitance model parameters

`cds=0 F`	Drain-to-source capacitance.
`tau=0 s`	Conduction current delay time.
`qgqh=0.0`	Charge parameter.
`qgsh=0.0`	Charge parameter.
`qgdh=0.0`	Charge parameter.
`qgio=1.0e-06`	Charge parameter.
`qgql=0.0`	Charge parameter.
`qgag=1.0`	Charge parameter.
`qgad=1.0`	Charge parameter.
`qgcl=0.0`	Charge parameter.
`qggb=1.0`	Charge parameter.
`qggo=0.0`	Charge parameter.

Temperature effects parameters

`tnom (C)`	Parameters measurement temperature. Default set by options.
`xti=0`	Temperature exponent for effect on `is`.
`eg=1.11 V`	Energy band gap.
`vtotc=0 V/C`	Temperature coefficient for `vto`.
`alphatce=0 1/C`	Temperature coefficient for `alpha`.
`betatce=0 1/C`	Temperature coefficient for `beta`.
`gammatc=0 1/C`	Temperature coefficient for `gamma`.
`trs1=0 1/C`	Temperature parameter for source resistance.
`trd1=0 1/C`	Temperature parameter for drain resistance.
`trg1=0 1/C`	Temperature parameter for gate resistance.
`vsttc=0 1/C`	Temperature coefficient for Vst.
`msttc=0 1/C`	Temperature coefficient for Mst.

© 2023 Cadence Design Systems, Inc.

Operating region warning control parameters

`imax=1 A`	Maximum allowable current (*area).
`bvj=∞ V`	Junction reverse breakdown voltage.

Noise model parameters

`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`kfd=0`	Flicker noise (1/f) coefficient for gate diodes.
`afd=1`	Flicker noise (1/f) exponent for gate diodes.

The `imax` parameter aids convergence and prevents numerical overflow. The junction characteristics of the FET are accurately modeled for currents up to `imax`. For currents above `imax`, the junction is modeled as a linear resistor and a warning is printed. The `bv` parameter detects the junction breakdown only. The breakdown currents of the junctions are not modeled.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.
`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, or `subth`.
`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`id (A)`	Drain current.
`ig (A)`	Gate current.
`ids (A)`	Drain-to-source current.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`vth (V)`	Threshold voltage.
`cgs (F)`	Gate-source capacitance.
`cgd (F)`	Gate-drain capacitance.
`cds (F)`	Drain-source capacitance.
`qg (Coul)`	Gate charge.
`qd (Coul)`	Drain charge.
`qs (Coul)`	Source charge.
`pwr (W)`	Power at op point.

GaAs MESFET (TOM3V1)

TOM3_V1 stands for Triquint Own Model version-3. It is an improved GaAs MESFET.

This device is supported within altergroups.

Sample Instance Statement

```
mt1 (2 1 0) tom3v1mos w=5 ng=2 m=2
```

Sample Model Statement

```
model tom3v1mos tom3v1 vto=-1.9 alpha=2.8 beta=0.01 lambda=-0.044 gamma=0.2
q=2.5 k=3.5 vst=0.03 mst=0.1 ilk=5.0e-7 plk=2 kgamma=0.66 taugd=5.0e-9
```


© 2023 Cadence Design Systems, Inc.

```
ctau=5.0e-15 qgql=1.0e-16 qgqh=-3.0e-16 qgi0=3.0e-16 qgag=3.0 qgad=2.3
qggb=90.0 qgcl=3.0e-16 qgsh=5.0e-16 qgdh=1e-16 qgg0=3e-16 capmod=2 cds=0.26e-15
tau=3.0e-12 rd=0.01 rg=0.01 rgmet=0 rs=0.01 is=7.0e-12 eta=1.9
alphatce=6.7337e-3 gammatc=2.3e-3 msttc=2e-3 vsttc=0.00031 vtotc=-119e-6
betatce=1e-3 rdtc=3e-3 rstc=3e-3 xti=2.0 eg=1.91 p=0.5 af=1.3 kf=3.86e-11 ffe=2.0
```

Instance Syntax

```
Name ( d g s ) ModelName <parameter=value> ...
```

Instance Parameters

`m=1`	Multiplicity factor.
`w=50 um`	Gate width.
`ng=6`	Number of gate fingers.
`trise=0.0 C`	Temperature rise from ambient.

Model Syntax

```
model ModelName tom3v1 <parameter=value> ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

tnom=25 C	Parameters measurement temperature.
vto=-2.0 V	Threshold voltage.
alpha=3.0 1/V	Knee-voltage parameter.
beta=0.05 A/V^q	Transconductance parameter.
lambda=0.0 1/V	Slope of drain characteristic.
gamma=0.1	Threshold shifting parameter.
q=2.0	Power-law parameter.
k=3.0	knee-function factor.
vst=0.05 V	Subthreshold slope.
mst=0.0 1/V	Subthreshold slope drain parameter.
ilk=1.0e-7 A/um	Gate leakage diode saturation current (/w).
plk=2.25 V	Gate leakage diode potential.
kgamma=0.33	Internal vcvs parameter.
taugd=1.0e-9 s	Time constant for Ctau.
ctau=1.0e-15 F	Drain-to-source dispersion capacitance.
qgql=5.0e-16 Coul/um	Charge parameter.
qgqh=-2.0e-16 Coul/um	Charge parameter.
qgi0=1.0e-16 A/um	Charge parameter.
qgag=1.0 1/V	Charge parameter.
qgad=1.0 1/V	Charge parameter.
qggb=100.0 um/W	Charge parameter.
qgcl=2.0e-16 F/um	Charge parameter.
qgsh=1.0e-16 F/um	Charge parameter.
qgdh=0.0 F/um	Charge parameter.
qgg0=0.0 F/um	Charge parameter.
capmod=1	Capacitance model selector.

© 2023 Cadence Design Systems, Inc.

cds=0.0 F	Drain-to-source capacitance.
tau=1.0e-12 s	Conduction current delay time.
rd=0.0 Ohm*um	Drain resistance (*w).
rg=0.0 Ohm*um	Gate resistance (*w).
rgmet=0.0 Ohm/um	Metal resistance in gate (/w).
rs=0.0 Ohm*um	Source resistance (*w).
is=1.0e-12 A/um	Gate diode saturation current (/w).
eta=1.0	Parameter for 'is'.
alphatce=7.7337e-3 1/C	Temperature parameter for `alpha'.
gammatc=0.0 1/C	Temperature parameter for `gamma'.
msttc=0.0 1/(V*C)	Temperature parameter for 'mst'.
vsttc=0.0 V/C	Temperature parameter for 'vst'.
vtotc=-1.49e-4 V/C	Temperature parameter for `vto'.
betatce=0.0 1/C	Temperature coefficient for `beta'.
rdtc=0.0 1/C	Temperature parameter for rd.
rstc=0.0 1/C	Temperature parameter for rs.
xti=0.0	Temperature exponent for effect on `is'.
eg=1.11 V	Energy band gap.
p=0.32	White noise coefficient.
af=1.0	Flicker (1/f) noise exponent.
kf=0.0	Flicker (1/f) noise coefficient.
ffe=1.0	Flicker (1/f) noise coefficient.

© 2023 Cadence Design Systems, Inc.

Operating-Point Parameters

vgs (V)	Gate-source voltage.
vds (V)	Drain-source voltage.
id (A)	Drain current.
ig (A)	Gate current.
is (A)	Source current.
ids (A)	Drain-to-source current.
gm (S)	Common-source transconductance.
gds (S)	Common-source output conductance.
vth (V)	Threshold voltage.
cgs (F)	Gate-source capacitance.
cgd (F)	Gate-drain capacitance.
pwr (W)	Power at operating point.

Related Topics

TriQuint Owned Models (tom2 and tom3/tom3v1)

Model Equations

Scaling Effects

New features from TOM3 to TOM3v1

Model Usage (tom2)

Component Statements

© 2023 Cadence Design Systems, Inc.

40

RPI TFT Models

The Poly-Si (PSITFT) and amorphous-Si (ATFT) TFT models are developed by the Semiconductor Devices Research Group at Rensselaer Polytechnic Institute (RPI). This chapter contains the following information for these models:

- Poly-Si TFT Model (PSITFT) on page 2717
  - Equivalent Circuit on page 2717
  - Model Features on page 2717
  - Channel Width and Length on page 2718
  - Drain and Source Parasitic Resistance on page 2718
  - Threshold Voltage on page 2720
  - Effective Mobility on page 2720
  - Unified Electron Sheet Charge Density Per Unit Area on page 2721
  - Channel Conductance on page 2722
  - Saturation Voltage on page 2722
  - Channel Current on page 2723
  - Kink Effect Current on page 2724
  - Subthreshold Leakage Current on page 2725
  - Parasitic Resistance Dependence on page 2727
  - Gate-Drain/Source Resistance on page 2728
  - Temperature Dependence on page 2728
  - Capacitance on page 2729
  - ACM Option on page 2735
  - Scaling Effects on page 2736

© 2023 Cadence Design Systems, Inc.

? Component Statements on page 2736

? Amorphous-Si TFT Model (ATFT) on page 2744

? Equivalent Circuit on page 2744

? Model Features on page 2744

? Drain Current on page 2746

? Temperature Dependence on page 2751

? Capacitance on page 2751

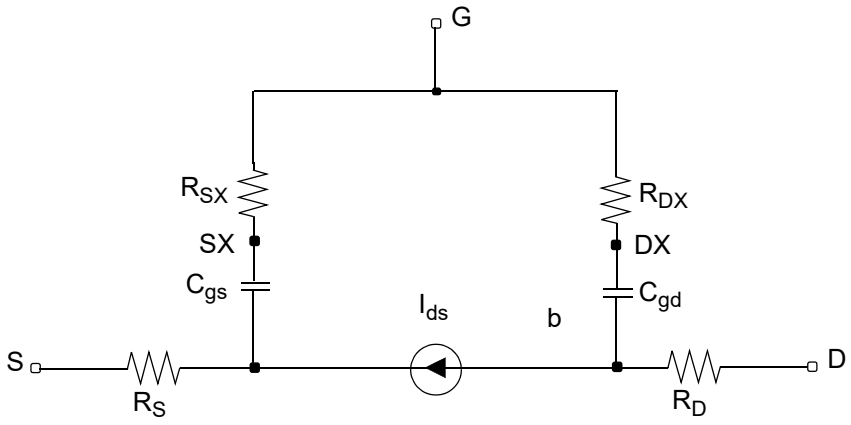
? Component Statements on page 2752

? Component Statements on page 2752

© 2023 Cadence Design Systems, Inc.

Poly-Si TFT Model (PSITFT)

Equivalent Circuit



Model Features

- Unified DC Model includes all four regimes for channel lengths down to 4 um
  - Leakage (thermionic emission)
  - Sub-threshold (diffusion like model)
  - Above threshold (c-Si like with m FET)
  - Kink (impact ionization with feedback)
- AC model accurately reproduces C_{gs} frequency dispersion
- Automatic scaling of model parameters to accurately model a wide range of device geometries.
- Above threshold
  - Based on the crystalline MOSFET Model
  - Field effect mobility becomes a funcion of gate bias
  - Field effect mobility accounts for trap states
- Sub-threshold
  - Diffusion like model

© 2023 Cadence Design Systems, Inc.

- Leakage Current
  - Reverse bias drain current function of
    - Electric field near drain
    - Temperature
  - Independent of channel length

Channel Width and Length

(40-1)

$$w = \begin{cases} w \cdot Wmlt + Xw - 2Wd \text{ , if ACM is given} \\ w \text{ , if ACM is not given} \end{cases}$$

(40-2)

$$l = \begin{cases} l \cdot Lmlt + Xl - 2Ld \text{ , if ACM is given} \\ l \text{ , if ACM is not given} \end{cases}$$

Drain and Source Parasitic Resistance

If ACM is not given,

(40-3)

$$rd = \begin{cases} rd \text{ , if rd is given} \\ rsh \cdot nrd \text{ , otherwise} \end{cases}$$

(40-4)

$$rs = \begin{cases} rs \text{ , if rs is given} \\ rsh \cdot nrs \text{ , otherwise} \end{cases}$$

ACM=0:

© 2023 Cadence Design Systems, Inc.

(40-5)

$$rd = \begin{cases} nrd \cdot rsh + rdc \text{ , if } (nrd \cdot rsh) > 0 \\ rd + rdc \text{ , otherwise} \end{cases}$$

(40-6)

$$rs = \begin{cases} nrs \cdot rsh + rsc \text{ , if } (nrs \cdot rsh) > 0 \\ rs + rsc \text{ , otherwise} \end{cases}$$

If ACM=1,

(40-7)

$$rd = (Ld + Ldif) \cdot rd/w + nrd \cdot rsh + rdc$$

(40-8)

$$rs = (Ld + Ldif) \cdot rs/w + nrs \cdot rsh + rsc$$

If ACM=2, 3,

(40-9)

$$rd = \begin{cases} (Ld + Ldif) \cdot rd/w + nrd \cdot rsh + rdc \text{ , if nrd is given} \\ rdc + \dfrac{Hdif \cdot rsh + (Ld + Ldif) \cdot rd}{w} \text{ , otherwise} \end{cases}$$

(40-10)

© 2023 Cadence Design Systems, Inc.

$$rs = \begin{cases} (Ld + Ldif) \cdot rs/w + nrs \cdot rsh + rsc \text{ , if nrd is given} \\ rsc + \dfrac{Hdif \cdot rsh + (Ld + Ldif) \cdot rs}{w} \text{ , otherwise} \end{cases}$$

Threshold Voltage

(40-11)

$$V_{TH} = V_{thx} - \frac{at \cdot V_{ds}^{2} + bt}{l \cdot \left(1 + e^{\left(\frac{V_{gs} - V_{thx} - vsigmat}{vsigma}\right)}\right)}$$

Effective Mobility

(40-12)

$$mueff = mus + \frac{mufet}{1 + \frac{theta}{tox} \cdot V_{gte}}$$

(40-13)

$$\frac{1}{mufet} = \frac{1}{mu0} + \frac{1}{\mu_1 \cdot \left(\frac{2 \cdot V_{gte}}{eta_f \cdot V_t}\right)^{mmu}}$$

where

(40-14)

$$V_t = k \cdot T/q$$

(40-15)

© 2023 Cadence Design Systems, Inc.

$$V_{gte} = eta \cdot V_t \cdot \left(1 + \frac{\alpha_{sat} \cdot V_{gt}}{2 \cdot eta \cdot V_t} + \sqrt{delta^2 + \left[\frac{\alpha_{sat} \cdot V_{gt}}{2 \cdot eta \cdot V_t} - 1 \right]^2} \right)$$

(40-16)

$$V_{gt} = V_{gs} - V_{th}$$

Unified Electron Sheet Charge Density Per Unit Area

(40-17)

$$eta_f = \frac{eta}{1 + meta \cdot reta \cdot \frac{i1}{1 + i1}}$$

where

(40-18)

$$reta = (eta - 1)/(eta)$$

(40-19)

$$i1 = Kinkfac \cdot (V_{ds} - V_{dse}) \cdot e^{-vkink/(V_{ds} - V_{dse})}$$

(40-20)

$$Kinkfac = A_{kink} \cdot w/l$$

(40-21)

$$A_{kink} = \frac{(lkink/l)^{mkink}}{vkink}$$

(40-22)

© 2023 Cadence Design Systems, Inc.

$$V_{dse} = \frac{V_{ds}}{\left(1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{mss}\right)^{1/mss}}$$

where

(40-23)

$$V_{sat} = V_{gte}$$

(40-24)

$$n_s = 2 \cdot n_0 \cdot \log\left(1 + \frac{1}{2} \cdot e^{\frac{V_{gt}}{etaf \cdot V_t}}\right)$$

(40-25)

$$n_0 = \frac{\varepsilon_{SiO_2} \cdot eta \cdot V_t}{2 \cdot q \cdot tox}$$

Channel Conductance

(40-26)

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi} \cdot RT}$$

(40-27)

$$g_{chi} = q \cdot \frac{w}{l} \cdot mueff \cdot n_s$$

Saturation Voltage

(40-28)

© 2023 Cadence Design Systems, Inc.

$$V_{DSAT} = \frac{Isat}{g_{ch}}$$

(40-29)

$$I_{sat} = \frac{g_{chi} \cdot V_{gte}}{\left(1 + \frac{V_{gte}}{V_l}\right) + g_{chi} \cdot RSS + \sqrt{1 + 2 \cdot RSS \cdot g_{chi} + (1 + V_{gte} / V_l)^2}}$$

(40-30)

$$V_l = \frac{vmax \cdot l}{mueff}$$

Channel Current

(40-31)

$$i_{choo} = \frac{g_{ch} \cdot V_{ds} \cdot (1 + lambda \cdot V_{ds})}{\left[1 + \left(\frac{Vds}{V_{dsat}}\right)^{me}\right]^{1/(me)}}$$

(40-32)

$$V_{satnew} = \frac{2 \cdot vmax \cdot l \cdot q \cdot (n_s - i_{choo} \cdot CRC)}{q \cdot (n_s - i_{choo} \cdot CRC) \cdot mueff + 2 \cdot vmax \cdot l \cdot \frac{C_{ox}}{\alpha_{sat}}}$$

where

(40-33)

$$C_{ox} = \frac{\varepsilon_{SiO_2}}{tox}$$

If Isubmod=1

© 2023 Cadence Design Systems, Inc.

lambda=0

(40-34)

$$I_{ds} = \frac{i_{choo}}{1 - deltal/l}$$

(40-35)

$$deltal = \frac{ls \cdot \log\left(1 + \frac{V_{disi} - V_{dsenew}}{vp}\right)}{1 + \frac{V_{dsenew}}{V_p} + w \cdot CRL \cdot mueff \cdot V_{dsenew}}$$

(40-36)

$$V_{disi} = V_{ds} - i_{choo} \cdot RT$$

(40-37)

$$V_{dsenew} = \frac{V_{disi}}{\left(1 + \left(\frac{V_{disi}}{V_{satnew}}\right)^{mss}\right)^{1/mss}}$$

else

(40-38)

$$I_{ds} = i_{choo}$$

Kink Effect Current

(40-39)

© 2023 Cadence Design Systems, Inc.

$$I_{kink} = A_{kink} \cdot I_{ds} \cdot (V_{ds} - V_{dsenew}) \cdot e^{\left(-\frac{vkink}{V_{ds} - V_{dsenew}}\right)}$$

Kink effect current is added to the drain current

Subthreshold Leakage Current

(40-40)

$$I_{leak} = clk \cdot w \cdot \left[e^{\frac{blk \cdot V_{ds}}{V_t}} - 1 \right] \cdot [X_{TFE} + X_{TE}] + I_{diode}$$

(40-41)

$$X_{TFE} = \frac{X_{TFE,\,lo} \cdot X_{TFE,\,hi}}{X_{TFE,\,lo} + X_{TFE,\,hi}}$$

(40-42)

$$X_{TE} = e^{-W_C}$$

(40-43)

$$W_C = (E_c - E_t)/(k \cdot T) = 0.55eV/(k \cdot T)$$

(40-44)

$$X_{TFE,\,lo} = \begin{cases} \frac{4\sqrt{\pi}}{3} \cdot f \cdot e^{\left(\frac{4}{27} \cdot f^2 - W_C\right)} & \text{for f <= flo} \\ X_{TFE,\,lo}(f_{lo}) \cdot e^{\left[\left(\frac{1}{f_{lo}} + \frac{8}{27} \cdot f_{lo}\right) \cdot (f - f_{lo})\right]} & \text{for f > flo} \end{cases}$$

(40-45)

© 2023 Cadence Design Systems, Inc.

$$f = \frac{1}{2} \cdot FMIN \cdot \left(1 + \frac{f_0}{FMIN} + \sqrt{delta^2 + \left(\frac{f_0}{FMIN} - 1 \right)^2} \right)$$

where FMIN=0.0001

(40-46)

$$f_0 = \left(\frac{V_{ds}}{dd} - \frac{V_{gs} - vfb}{dg} \right) / F_0$$

where

(40-47)

$$F_0 = (k \cdot T)^{3/2} \cdot \frac{4}{3} \cdot \frac{2\pi\sqrt{2m}}{qh}$$

(40-48)

$$m = 0.27 \cdot m_0$$

(40-49)

$$f_{lo} = \frac{3}{2} \cdot (\sqrt{W_C + 1} - 1)$$

(40-50)

$$X_{TFE,hi} = \begin{cases} \dfrac{2 \cdot W_c}{3} \cdot e^{\left(1 - \frac{2 \cdot W_C}{3}\right)} & \text{for f <= fhi} \\ \left(1 - \dfrac{W_c^{1/3}}{2 \cdot f}\right)^{-1} \cdot e^{\left(\frac{-W_C^{3/2}}{f}\right)} & \text{for f > fhi} \end{cases}$$

(40-51)

© 2023 Cadence Design Systems, Inc.

$$f_{hi} = 3 \cdot \left(\frac{W_C^{3/2}}{2 \cdot W_C - 3} \right)$$

(40-52)

$$I_{diode} = i00 \cdot w \cdot e^{\left(\frac{eb}{k \cdot T}\right)} \cdot \left[1 - e^{\left(-\frac{V_{ds}}{V_t}\right)} \right]$$

Parasitic Resistance Dependence

If intdsnod=0 , extrinsic characteristics are used.

(40-53)

$$RSS = rs$$

(40-54)

$$RT = rs + rd$$

(40-55)

$$CRC = C_{ox} \cdot rd/q$$

(40-56)

$$CRL = C_{ox} \cdot rs/l$$

Else, intrinsic characteristics are used.

(40-57)

© 2023 Cadence Design Systems, Inc.

$$RSS = RT = CRC = CRL = 0.0$$

Gate-Drain/Source Resistance

(40-58)

$$\frac{1}{R_{ch}} = \frac{dI_d}{dV_{ds}}$$

If rsx is not specified,

(40-59)

$$rsx = \left.\frac{Rch}{kss}\right|_{V_{ds}= 0V}$$

If rdx is not specified

(40-60)

$$rdx = \left.\frac{Rch}{kss}\right|_{V_{ds}}$$

Temperature Dependence

(40-61)

$$V_{thx} = vto - dvto \cdot (T - T_{nom})$$

(40-62)

$$\mu_1 = mu1 + dmu1 \cdot (T - T_{nom})$$

(40-63)

© 2023 Cadence Design Systems, Inc.

$$\alpha_{sat} = asat - \frac{lasat}{l} - dasat \cdot (T - T_{nom})$$

Capacitance

When `capmod=0`,

(40-64)

$$C_{gs} = C_f + \frac{2}{3} \cdot C_{gcs} \cdot \left[1 - \left(\frac{V_{dsat} - V_{dse}}{2 \cdot V_{dsat} - V_{dse}}\right)^2\right]$$

(40-65)

$$C_{gd} = C_f + \frac{2}{3} \cdot C_{gcd} \cdot \left[1 - \left(\frac{V_{dsat}}{2 \cdot V_{dsat} - V_{dse}}\right)^2\right]$$

(40-66)

$$C_f = \frac{1}{2} \cdot \varepsilon_{si} \cdot w$$

(40-67)

$$C_{gcs} = \frac{w \cdot l \cdot \varepsilon_{SiO_2} / tox}{1 + etac0 \cdot e^{\left(-\frac{V_{gt}}{etac0 \cdot V_t}\right)}}$$

(40-68)

$$C_{gcd} = \frac{w \cdot l \cdot \varepsilon_{SiO_2} / tox}{1 + \eta_{cd} \cdot e^{\left(-\frac{V_{gt} - V_{dse}}{\eta_{cd} \cdot V_t}\right)}}$$

(40-69)

© 2023 Cadence Design Systems, Inc.

$$\eta_{cd} = etac0 + etac00 \cdot V_{dse}$$

(40-70)

$$V_{dsex} = \frac{V_{ds}}{\left(1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{mc}\right)^{1/mc}}$$

(40-71)

$$V_{gt} = Vgs - Vthx$$

When `capmod=1`

If `ZEROC=1`,

(40-72)

$$C_{gcs} = C_{gcd} = 0$$

(40-73)

If `ZEROC=0`,

(40-74)

$$C_{gs} = C_{gd} = 0 \ \textbf{\textit{if}} \ V_{gt} < -\frac{phi}{2} \ \textbf{\textit{where}} \ phi = 0.6$$

(40-75)

$$C_{gs} = w \cdot l \cdot \varepsilon_{SiO_2}/tox \cdot \left(\frac{4 \cdot V_{gt}}{3 \cdot phi} + \frac{2}{3}\right) \ C_{gd} = 0 \ \textbf{\textit{if}} \ \frac{-phi}{2} \le V_{gt} < 0$$

(40-76)

© 2023 Cadence Design Systems, Inc.

if $V_{gt} < -\frac{phi}{2}$

(40-77)

$$\begin{cases} C_{gs} = \frac{2 \cdot w \cdot l \cdot \varepsilon_{SiO_2}}{3 \cdot tox}, C_{gd} = 0, V_{ds} \geq V_{dsat} \\ C_{gs} = \frac{2 \cdot w \cdot l \cdot \varepsilon_{SiO_2}}{3 \cdot tox} \cdot \left[1 - \left(\frac{V_{dsat} - V_{dse}}{2 \cdot V_{dsat} - V_{dse}} \right)^2 \right], C_{gs} = \frac{2 \cdot w \cdot l \cdot \varepsilon_{SiO_2}}{3 \cdot tox} \cdot \left[1 - \left(\frac{V_{dsat}}{2 \cdot V_{dsat} - V_{dse}} \right)^2 \right] \\ V_{ds} < V_{dsat} \end{cases}$$

When `capmod=2`

Charge conservation capacitance model

(40-78)

$$V_{gsteff,cv} = noff \cdot eta \cdot V_t \cdot log\left(1 + e^{\left(\frac{V_{gs} - V_{thx} - voffcv}{noff \cdot eta \cdot V_t} \right)} \right)$$

(40-79)

$V_{gs} = V_{sxs}$ ***for Qs evaluation***

(40-80)

$V_{gs} = V_{dxs}$ ***for Qd evaluation***

(40-81)

$$V_{dsat,cv} = \frac{V_{gsteff,cv}}{A_{sat}}$$

(40-82)

© 2023 Cadence Design Systems, Inc.

$$A_{sat} = \left(1 + \left(\frac{CLC}{L_{activ}}\right)^{CLE}\right) / \alpha_{sat}$$

(40-83)

$$V_{cveff} = V_{dsat,\,cv} - 0.5\left(V_4 + \sqrt{V_4^2 + 4\delta_4 V_{dsat,\,cv}}\right)$$

where

(40-84)

$$V_4 = V_{dsat,\,cv} - V_{ds} - \delta_4$$

(40-85)

$$\delta_4 = 0.02$$

(40-86)

$$L_{active} = l \cdot LMLT + XL - 2DLC$$

(40-87)

$$W_{active} = w \cdot WMLT + XW - 2DWC$$

(40-88)

$$Q_g = -W_{active} \cdot L_{active} \cdot \varepsilon_{SiO_2} / tox \left(\left(V_{gsteff,\,cv} - \frac{1}{2} V_{cveff}\right) + \frac{A_{sat} V^2_{cveff}}{12\left(V_{gsteff,\,cv} - \frac{A_{sat}}{2} V_{cveff}\right)} \right)$$

(40-89)

© 2023 Cadence Design Systems, Inc.

$$Q_s = -\left(\frac{W_{active} \cdot L_{active} \cdot \varepsilon_{SiO_2}/tox}{2\left(V_{gsteff,cv} - \frac{A_{sat}}{2}V_{cveff}\right)^2}\left(V^3_{gsteff,cv} - \frac{1}{3}V^2_{gsteff,cv}V_{cveff} - V^2_{gsteff,cv}A_{sat}V_{cveff} + \frac{5}{12}V_{gsteff,cv}A_{sat}V^2_{cveff} + \frac{1}{4}V_{gsteff,cv}(A_{sat}V_{cveff})^2 - \frac{2}{15}(A_{sat}V_{cveff})^2 V_{cveff}\right)\right)$$

(40-90)

$$Q_d = -\left(\frac{W_{active} \cdot L_{active} \cdot \varepsilon_{SiO_2}/tox}{2\left(V_{gsteff,cv} - \frac{A_{sat}}{2}V_{cveff}\right)^2}\left(V^3_{gsteff,cv} - \frac{2}{3}V^2_{gsteff,cv}V_{cveff} - V^2_{gsteff,cv}A_{sat}V_{cveff} + \frac{3}{4}V_{gsteff,cv}A_{sat}V^2_{cveff} + \frac{1}{4}V_{gsteff,cv}(A_{sat}V_{cveff})^2 - \frac{1}{5}(A_{sat}V_{cveff})^2 V_{cveff}\right)\right)$$

(40-91)

$$Q_{sx} = -Q_s \; Q_{dx} = -Q_d$$

(40-92)

$$Q_{dx} = -Q_d$$

(40-93)

$$C_{ss} = \frac{dQ_s}{dV_s} \; C_{sd} = \frac{dQ_s}{dV_d} \; C_{ssx} = \frac{dQ_s}{dV_{sx}} \; C_{sdx} = 0$$

(40-94)

$$C_{ds} = \frac{dQ_d}{dV_s} \; C_{dd} = \frac{dQ_d}{dV_d} \; C_{ddx} = \frac{dQ_d}{dV_{dx}} \; C_{dsx} = 0$$

(40-95)

© 2023 Cadence Design Systems, Inc.

$$C_{sxs} = \frac{dQ_{sx}}{dV_s} C_{sxd} = \frac{dQ_{sx}}{dV_d} C_{sxsx} = \frac{dQ_{sx}}{dV_{sx}} C_{sxdx} = 0$$

(40-96)

$$C_{dxs} = \frac{dQ_{dx}}{dV_s} C_{dxd} = \frac{dQ_{dx}}{dV_d} C_{dxdx} = \frac{dQ_{dx}}{dV_{dx}} C_{dxsx} = 0$$

(40-97)

$$C_{gs} = C_{sxs} + C_{dxs} \; C_{gd} = C_{dxd} + C_{sxd} \; C_{gg} = C_{gs} + C_{gd}$$

Overlap Capacitances

When `capmod=2`

(40-98)

$$OverlapC_{gs} = Cgso \cdot W_{active}$$

(40-99)

$$OverlapC_{gd} = Cgdo \cdot W_{active}$$

For other values of `capmod`

If Acm parameter is given,

(40-100)

$$OverlapC_{gs} = \begin{cases} (w + 2Wd) \cdot Cgso \text{ , if Cgso is given} \\ (w + 2Wd) \cdot (Ld + Meto) \cdot \varepsilon_{SiO_2} / tox, \text{ if Cgso is not given} \end{cases}$$

(40-101)

© 2023 Cadence Design Systems, Inc.

$$OverlapC_{gd} = \begin{cases} (w + 2Wd) \cdot Cgdo \text{ , if Cgdo is given} \\ (w + 2Wd) \cdot (Ld + Meto) \cdot \varepsilon_{SiO_2} / tox, \text{ if Cgdo is not given} \end{cases}$$

Else,

(40-102)

$$OverlapC_{gs} = w \cdot Cgso$$

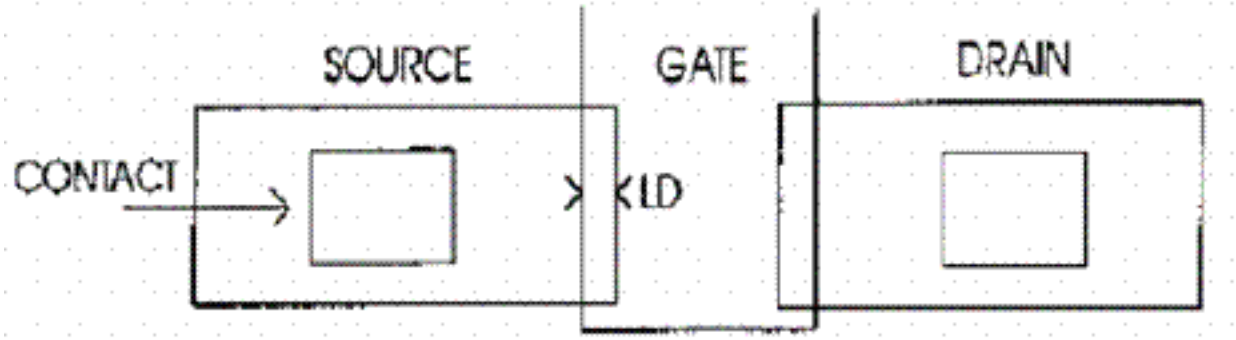
(40-103)

$$OverlapC_{gd} = w \cdot Cgdo$$

ACM Option

When ACM=0

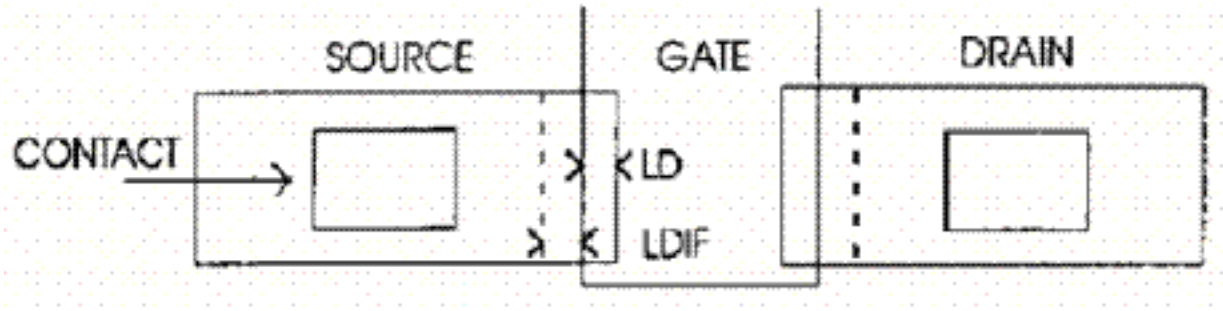
(40-104)



When ACM=1

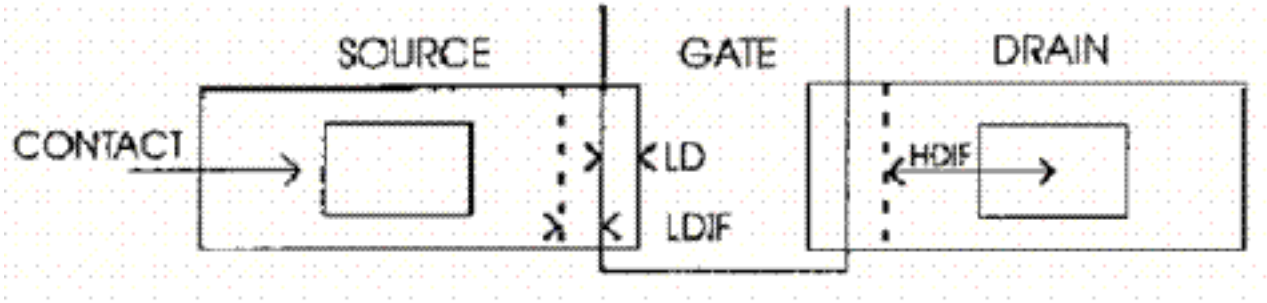
© 2023 Cadence Design Systems, Inc.

(40-105)



When ACM=2

(40-106)



Scaling Effects

For scaling effects, see Scaling Factors (scale and scalem) on page 286.

Component Statements

This device is supported within altergroups.

Sample Instance Statement

```
m4 (0 2 1 1) nch w=2u l=0.8u
```

Sample Model Statement

```
model nch psitft type=p
```


© 2023 Cadence Design Systems, Inc.

Instance Syntax

```
Name  d  g  s  [b]  [t] ModelName parameter=value ...
```

Instance Parameters

w (m)	Channel width.
l (m)	Channel length.
nrd (m/m)	Drain squares.
nrs (m/m)	Source squares.
m=1	Multiplicity factor (number of MOSFETs in parallel).
region=triode	Estimated operating region. Possible values are off, triode, sat, or subth.
isnoisy=yes	Should resistor generate noise. Possible values are no or yes.
rth0 (Ω)	Thermal resistance.
cth0 (F)	Thermal capacitance.
nseg=1 m/m	Number of segments for channel width partitioning.

Model Syntax

```
model modelName psitft parameter=value ...
```

Model Parameters

Device type parameters

type=n	Transistor type. Possible values are n or p.

Drain current model parameters

vto=0 V	Threshold voltage at zero body bias (BIN).
lambda=0.048 1/V	Channel length modulation parameter (BIN).

© 2023 Cadence Design Systems, Inc.

`tox=1e-7 m`	Gate oxide thickness.
`eta=7`	Subthreshold ideality factor (BIN).
`etai`	Alias to eta (BIN).
`asat=1`	Proportionality constant of Vsat (BIN).
`alphasat`	Alias to asat (BIN).
`delta=4`	Transition width parameter (BIN).
`mus=1 cm`^{2}`/V s`	Subthreshold mobility (BIN).
`mu0=100 cm`^{2}`/V s`	High field mobility (BIN).
`muo (cm`^{2}`/V s)`	Alias to mu0 (BIN).
`mu1=0.004 cm`^{2}`/V s`	Low field mobility parameter (BIN).
`mmu=1.7`	Low field mobility exponent (BIN).
`m`	Alias to mmu (BIN).
`vfb=-0.1 V`	Flat band voltage (BIN).
`dd=1400e-10 m`	Vds field constant (BIN).
`dg=2000e-10 m`	Vds field constant (BIN).
`blk=0.001`	Leakage barrier lowering constant (BIN).
`clk=6 A/m`	Leakage scaling constant (BIN).
`i0=6.0 A/m`	Alias of clk (BIN).
`lkink=19e-6 m`	Kink effect constant (BIN).
`mkink=1.3`	Kink effect exponent (BIN).
`mk=1.3`	Alias of mkink (BIN).
`vkink=9.1 V`	Kink effect voltage (BIN).
`rs=0 Ω`	Source resistance.
`rd=0 Ω`	Drain resistance.
`rsx=0 Ω`	Resistance in series with Cgs.
`rdx=0 Ω`	Resistance in series with Cgd.
`at=3e-8 m/V`	DIBL parameter 1 (BIN).
`bt=1.9e-6 m/V`	DIBL parameter 2 (BIN).

© 2023 Cadence Design Systems, Inc.

`eb=0.68 eV`	Barrier height of diode (BIN).
`i00=150 A/m`	Reverse diode saturation current (BIN).
`ioo (A/m)`	Alias to i00 (BIN).
`etac0`	Capacitance subthreshold ideality factor at zero drain bias (BIN).
`etac00=0 1/V`	Capacitance subthreshold coefficient of drain bias (BIN).
`mc=3`	Capacitance knee shape parameter (BIN).
`dvto=0 V/C`	Temperature coefficient of VTO (BIN).
`dmu1=0 cm`^{2}`/V s C`	Temperature coefficient of MU1 (BIN).
`dasat=0 1/C`	Temperature coefficient of ASAT (BIN).
`lasat=0 m`	Coefficient of length dependence of ASAT (BIN).
`von=0 V`	On-Voltage (BIN).
`cgso=0 F/m`	Gate-source overlap capacitance.
`cgdo=0 F/m`	Gate-drain overlap capacitance.
`vsigma=0.2 V`	Above threshold DIBL parameter (BIN).
`vsigmat=1.7 V`	Above threshold DIBL parameter (BIN).
`me=2.5`	Long channel saturation transition parameter (BIN).
`ms`	Alias to me (BIN).
`minme=2.0`	Minimum value of me parameter..
`meta=1`	ETA floating-body parameter (BIN).
`ls=35e-9 m`	Channel-length modulation coefficient 1 (BIN).
`vp=0.2 V`	Channel-length modulation coefficient 2 (BIN).
`isubmod=0`	Channel-length modulation model version.
`vmax=4e4 m/s`	Carrier saturation velocity (BIN).
`theta=0 1/V`	Mobility modulation coefficient (BIN).
`mss=1.5`	Vdse transition parameter (BIN).
`kss=0`	Fractions of the channel resistance coefficient.
`rsh=0 Ω/sqr`	Source/drain diffusion sheet resistance.
`capmod=0`	Intrinsic charge model.

© 2023 Cadence Design Systems, Inc.

`zeroc=0`	Zero gate-source (gate-drain) capacitance flag (Cgs=Cgd=0 if zeroc=1 and capmod=1).
`intdsnod=0`	Intrinsic source and drain nodes usage flag.
`minr=0.1 Ω`	Minimum source/drain resistance.
`version=2`	Version control parameter. The available versions are 1, 2.
`compatible=spectre`	Spice compatible flag. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, or `sspice`.
`cdnver=1`	Cadence version flag, 0 without improvement, 1 with improvement.

Temperature effects parameters

`tnom (C)`	Parameter measurement temperature.
`trise=0 C`	Temperature rise from ambient.
`shmod=0`	Self-heating selector.
`cth0=0.0 F`	Self-heating thermal capacitance.
`rth0=0 Ω`	Self-heating thermal resistance.
`wth0=0.0 µm`	Minimum width for thermal resistance calculation..
`tmax=500 C`	Maximum device temperature above ambient.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, or `rev`.

Default device parameters

`w=3e-6 m`	Default channel width.
`l=3e-6 m`	Default channel length.

© 2023 Cadence Design Systems, Inc.

`nrd=1 m/m`	Default drain squares.
`nrs=1 m/m`	Default source squares.

Auto Model Selector parameters

`wmax=1 m`	Maximum channel width for which the model is valid.
`wmin=0 m`	Minimum channel width for which the model is valid.
`lmax=1 m`	Maximum channel length for which the model is valid.
`lmin=0 m`	Minimum channel length for which the model is valid.

Acm related parameters

`acm=0`	Area calculation method.
`xl=0.0 m`	Accounts for masking and etching effects.
`xw=0.0 m`	Accounts for masking and etching effects.
`ld (m)`	Lateral diffusion into channel from source and drain diffusion.
`wd=0.0 m`	Lateral diffusion into channel from bulk along width.
`lmlt=1.0`	Length diffusion layer shrink reduction factor.
`wmlt=1.0`	Width diffusion layer shrink reduction factor.
`ldif=0.0 m`	Length of heavily doped diffusion adjacent to gate (BIN).
`hdif=0.0 m`	Length of heavily doped diffusion from contact to lightly doped region.
`xj=1.5E-7 m`	Metallurgical junction depth.
`meto=0.0 m`	Fringing field factor for gate to source and gate to drain overlap capacitance.
`rdc=0.0 Ω`	Additional drain resistance due to contact resistance.
`rsc=0.0 Ω`	Additional source resistance due to contact resistance.

© 2023 Cadence Design Systems, Inc.

Capmod=2 related parameters

Special parameters of version 1

`dvt=0 V`	The difference between von and the threshold (BIN).
`vsi=2.0 V`	Above threshold DIBL parameter (BIN).
`vst=2.0 V`	Above threshold DIBL parameter (BIN).

Binning parameters

`binunit=1`	Bin parameter unit selector. 1 for microns and 2 for meters.
`binflag=0`	Binflag=2 is to open xl/xw binning.

Output Parameters

`rtheff (Ω)`	Effective thermal resistance.
`Ctheff (F)`	Effective thermal capacitance.
`weff (m)`	Effective channel width.
`leff (m)`	Effective channel length.
`rseff (m)`	Effective source resistance.
`rdeff (m)`	Effective drain resistance.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.
`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, or `subth`.
`reversed`	Reverse mode indicator. Possible values are `no` or `yes`.
`ids (A)`	Resistive drain-to-source current (alias = lx4).

© 2023 Cadence Design Systems, Inc.

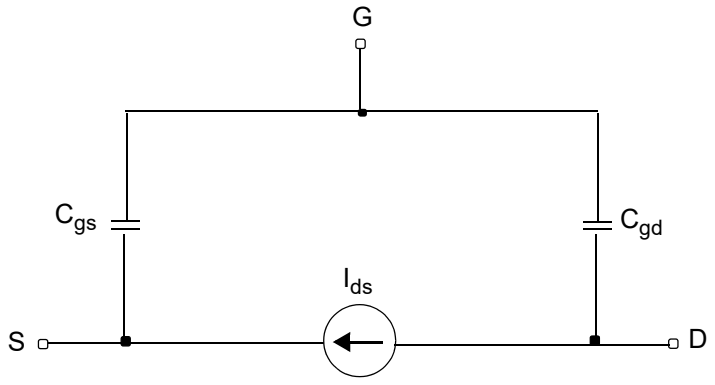
`vgs (V)`	Gate-source voltage (alias = lx2).
`vds (V)`	Drain-source voltage (alias = lx3).
`vth (V)`	Threshold voltage (alias = lv9).
`vdsat (V)`	Drain-source saturation voltage (alias = lv10).
`gm (S)`	Common-source transconductance (alias = lx7).
`gds (S)`	Common-source output conductance (alias = lx8).
`tdev (C)`	Temperature rise from ambient.
`cgd (F)`	Gate-drain capacitance (alias = lx19).
`cgs (F)`	Gate-source capacitance (alias = lx20).
`cgg (F)`	Cgg (only for capmod=2).
`css (F)`	Intrinsic capacitance dQs_dVs (only for capmod=2).
`csd (F)`	Intrinsic capacitance dQs_dVd (only for capmod=2).
`cssx (F)`	Intrinsic capacitance dQs_dVsx (only for capmod=2).
`csdx (F)`	Intrinsic capacitance dQs_dVdx (only for capmod=2).
`cds (F)`	Intrinsic capacitance dQd_dVs (only for capmod=2).
`cdd (F)`	Intrinsic capacitance dQd_dVd (only for capmod=2).
`cdsx (F)`	Intrinsic capacitance dQd_dVsx (only for capmod=2).
`cddx (F)`	Intrinsic capacitance dQd_dVdx (only for capmod=2).
`csxs (F)`	Intrinsic capacitance dQsx_dVs (only for capmod=2).
`csxd (F)`	Intrinsic capacitance dQsx_dVd (only for capmod=2).
`csxsx (F)`	Intrinsic capacitance dQsx_dVsx (only for capmod=2).
`csxdx (F)`	Intrinsic capacitance dQsx_dVdx (only for capmod=2).
`cdxs (F)`	Intrinsic capacitance dQdx_dVs (only for capmod=2).
`cdxd (F)`	Intrinsic capacitance dQdx_dVd (only for capmod=2).
`cdxsx (F)`	Intrinsic capacitance dQdx_dVsx (only for capmod=2).
`cdxdx (F)`	Intrinsic capacitance dQdx_dVdx (only for capmod=2).
`cgso (F)`	Gate-Source overlap capacitance.
`cgdo (F)`	Gate-Drain overlap capacitance.
`qs (Coul)`	Qs (only for capmod=2).

© 2023 Cadence Design Systems, Inc.

`qd (Coul)`	Qd (only for capmod=2).
`qg (Coul)`	Qg (only for capmod=2).
`qsx (Coul)`	Charge of sx internal node (only for capmod=2).
`qdx (Coul)`	Charge of dx internal node (only for capmod=2).
`ron (Ω)`	On-resistance.
`id (A)`	Resistive drain current.
`is (A)`	Resistive source current.
`pwr (W)`	Power at op point.
`igs (A)`	Gate-to-source current.
`igd (A)`	Gate-to-drain current.
`i1 (A)`	Resistive drain current.

Amorphous-Si TFT Model (ATFT)

Equivalent Circuit



Model Features

Features of the ATFT model include:

? The unified DC model covers all regimes of operation

© 2023 Cadence Design Systems, Inc.

- The model parameters are automatically scaled to accurately model a wide range of device geometries
- The modified charge control model includes induced charge trapped in localized states
- Above threshold includes:
  - Field effect mobility becoming a function of gate bias
  - Band mobility dominated by lattice scattering
- Below threshold includes:
  - Fermi level located in deep localized states
  - Realting position of fermi level, incluing deep DOS, back to the gate bias
- Emperical expression for current at large negative gate biases for hole-induced leakage current
- Temperature effects include:
  - Linear dependence of threshold voltage
  - Temperature activated field-effect mobility
  - Temperature activated leakage current
  - Dependence of subthreshold slope includinga possible back channel effect.

© 2023 Cadence Design Systems, Inc.

Drain Current

(40-107)

$$I_{ds} = I_{leakage} + I_{ab}$$

(40-108)

$$I_{leakage} = I_{hl} + I_{min}$$

where

(40-109)

$$I_{min} = sigma0 \cdot V_{ds}$$

(40-110)

$$I_{hl} = IOL\left[\exp\left(\frac{V_{ds}}{VDSL}\right) - 1\right]\exp\left(-\frac{V_{gs}}{VGSL}\right)\exp\left[\frac{EL}{q}\left(\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right)\right]$$

(40-111)

$$I_{ab} = g_{ch}V_{dse}(1 + LAMBDA \cdot V_{ds})$$

(40-112)

$$V_{dse} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_{sate}}\right)^{M}\right]^{\frac{1}{M}}}$$

(40-113)

© 2023 Cadence Design Systems, Inc.

$$V_{sate} = \alpha_{sat} V_{gte}$$

(40-114)

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}$$

(40-115)

$$g_{chi} = q \cdot n_s \cdot MUBAND \cdot \frac{W}{L}$$

(40-116)

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

(40-117)

$$n_{sa} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX} \left(\frac{V_{gte}}{V_{aat}} \right)^{GAMMA}$$

(40-118)

$$n_{sb} = n_{so} \left(\frac{t_m}{TOX} \frac{V_{gfbe}}{V0} \frac{EPSI}{EPS} \right)^{\frac{2VO}{V}}$$

(40-119)

$$n_{so} = N_c t_m \frac{V_e}{V_0} \exp\left(-\frac{DEF0}{V_{th}} \right)$$

(40-120)

© 2023 Cadence Design Systems, Inc.

$$N_c = 3.0 \cdot 10^{25} m^{-3}$$

(40-121)

$$V_e = \frac{2 \cdot V_0 \cdot V_{tho}}{2 \cdot V0 - V_{th}}$$

(40-122)

$$t_m = \sqrt{\frac{EPS}{2q \cdot GMIN}}$$

(40-123)

$$V_{gte} = \frac{VMIN}{2}\left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1\right)^2}\right]$$

(40-124)

$$V_{gt} = V_{gs} - V_T$$

(40-125)

$$V_{gfbe} = \frac{VMIN}{2}\left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1\right)^2}\right]$$

(40-126)

$$V_{gfb} = V_{gs} - VFB$$

Drain and Source Parasitic Resistance

If ACM is not given,

© 2023 Cadence Design Systems, Inc.

(40-127)

$$rd = \begin{cases} rd \text{ , if rd is given} \\ rsh \cdot nrd \text{ , otherwise} \end{cases}$$

(40-128)

$$rs = \begin{cases} rs \text{ , if rs is given} \\ rsh \cdot nrs \text{ , otherwise} \end{cases}$$

ACM=0:

(40-129)

$$rd = \begin{cases} nrd \cdot rsh + rdc \text{ , if } (nrd \cdot rsh) > 0 \\ rd + rdc \text{ , otherwise} \end{cases}$$

(40-130)

$$rs = \begin{cases} nrs \cdot rsh + rsc \text{ , if } (nrs \cdot rsh) > 0 \\ rs + rsc \text{ , otherwise} \end{cases}$$

If ACM=1,

(40-131)

$$rd = (Ld + Ldif) \cdot rd/w + nrd \cdot rsh + rdc$$

(40-132)

$$rs = (Ld + Ldif) \cdot rs/w + nrs \cdot rsh + rsc$$

If ACM=2, 3,

(40-133)

© 2023 Cadence Design Systems, Inc.

$$rd = \begin{cases} (Ld + Ldif) \cdot rd/w + nrd \cdot rsh + rdc & \text{, if nrd is given} \\ rdc + \dfrac{Hdif \cdot rsh + (Ld + Ldif) \cdot rd}{w} & \text{, otherwise} \end{cases}$$

(40-134)

$$rs = \begin{cases} (Ld + Ldif) \cdot rs/w + nrs \cdot rsh + rsc & \text{, if nrd is given} \\ rsc + \dfrac{Hdif \cdot rsh + (Ld + Ldif) \cdot rs}{w} & \text{, otherwise} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Temperature Dependence

(40-135)

$$V_{tho} = k_B \cdot TNOM/q$$

(40-136)

$$V_{th} = k_B \cdot T/q$$

(40-137)

$$V_{aat} = VAA \cdot \exp\left[\frac{EMU}{q \cdot GAMMA}\left(\frac{1}{V_{th}} - \frac{1}{V_{tho}}\right)\right]$$

(40-138)

$$V_T = VTO + KVT(TEMP - TNOM)$$

(40-139)

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM)$$

Capacitance

(40-140)

$$C_{gs} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}}\right)\right]$$

(40-141)

© 2023 Cadence Design Systems, Inc.

$$C_{gd} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}} \right) \right]$$

(40-142)

$$C_f = 0.5 \cdot EPS \cdot W$$

(40-143)

$$C_{gc} = q \frac{dn_{sc}}{dV_{gs} \cdot L_{eff} \cdot W_{eff}}$$

(40-144)

$$n_{sc} = \frac{n_{sac} n_{sbc}}{n_{sac} + n_{sbc}}$$

(40-145)

$$n_{sac} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX}$$

(40-146)

$$n_{sbc} = n_{sb}$$

Component Statements

This device is supported within altergroups.

Sample Instance Statement:

```
m4 (0 2 1 1) nch w=2u l=0.8u
```


© 2023 Cadence Design Systems, Inc.

Sample Model Statement

model nch atft type=n

Instance Syntax

```
Name  d  g  s  [b] ModelName parameter=value ...
```

Instance Parameters

`w (m)`	Channel width.
`l (m)`	Channel length.
`m=1`	Multiplicity factor (number of MOSFETs in parallel).
`trise=0`	Temperature rise from ambient.
`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, or `subth`.
`nrd (m/m)`	Drain squares.
`nrs (m/m)`	Source squares.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Syntax

```
model modelName atft parameter=value ...
```

Model Parameters

Device type parameters

`type=n`	Transistor type. Possible values are `n` or `p`.

Drain current model parameters

`compatible=spectre`

© 2023 Cadence Design Systems, Inc.

	Spice compatible flag. Possible values are `spectre`, `spice2`, `spice3`, `cdsspice`, `spiceplus`, `eldo`, or `sspice`.
`cdnver=1`	Cadence version selector.
`vto=0 V`	Zero-bias threshold voltage.
`lambda=0.0008 1/V`	Channel length modulation parameter.
`tox=1e-7 m`	Thin-oxide thickness.
`def0=0.6 eV`	Dark Fermi level position.
`alphasat=0.6`	Saturation modulation parameter.
`delta=5`	Transition width parameter.
`el=0.35 eV`	Activation energy of the hole leakage current.
`emu=0.06 eV`	Field effect mobility activation energy.
`eps=11`	Relative dielectric constant of substrate.
`epsi=7.4`	Relative dielectric constant of gate insulator.
`vfb=-3 V`	Flat band voltage.
`gamma=0.4`	Power law mobility parameter.
`gmin=1.0e23 1/m`^{3} `eV`	Minimum density of deep states.
`iol=3.0e-14 A`	Zero bias leakage current parameter.
`kasat=0.006 1/C`	Temperature coefficient of ALPHASAT.
`kvt=-0.036 V/C`	Threshold voltage temperature coefficient.
`m=2.5`	Knee shape parameter.
`muband=0.001 m`^{2}`/V s`	Conduction band mobility.
`rs=0 Ω`	Source resistance.
`rd=0 Ω`	Drain resistance.
`sigma0=1.0e-14 A`	Minimum leakage current parameter.
`v0=0.12 V`	Characteristic voltage for deep states.
`vaa=7.5e3 V`	Characteristic voltage for field effect mobility.

© 2023 Cadence Design Systems, Inc.

`vdsl=7 V`	Hole leakage current drain voltage parameter.
`vgsl=7 V`	Hole leakage current drain voltage parameter.
`vmin=0.3 V`	Convergence parameter.
`cgdo=0 F/m`	Gate-drain overlap capacitance.
`cgso=0 F/m`	Gate-source overlap capacitance.

ACM parameters

`acm=0`	Area calculation method.
`xw=0.0 m`	Accounts for masking and etching effects.
`xl=0.0 m`	Accounts for masking and etching effects.
`ld (m)`	Lateral diffusion into channel from source and drain diffusion.
`wd=0.0 m`	Lateral diffusion into channel from bulk along width.
`lmlt=1.0`	Length diffusion layer shrink reduction factor.
`wmlt=1.0`	Width diffusion layer shrink reduction factor.
`rsh=0 Ω/sqr`	Source/drain diffusion sheet resistance.
`rdc=0.0 Ω`	Additional drain resistance due to contact resistance.
`rsc=0.0 Ω`	Additional source resistance due to contact resistance.
`ldif=0.0 m`	Length of heavily doped diffusion adjacent to gate.
`hdif=0.0 m`	Length of heavily doped diffusion from contact to lightly doped region.
`meto=0.0 m`	Fringing field factor for gate to source and gate to drain overlap capacitance.
`xj=0.0 m`	Metallurgical junction depth.

Temperature effects parameters

`tnom (C)`	Parameter measurement temperature.
`trise=0 C`	Temperature rise from ambient.

© 2023 Cadence Design Systems, Inc.

Operating region warning control parameters

`alarm=none`	Forbidden operating region. Possible values are `none`, `off`, `triode`, `sat`, `subth`, or `rev`.

Auto Model Selector parameters

`wmax=1 m`	Maximum channel width for which the model is valid.
`wmin=0 m`	Minimum channel width for which the model is valid.
`lmax=1 m`	Maximum channel length for which the model is valid.
`lmin=0 m`	Minimum channel length for which the model is valid.

Noise model parameters

`noisemod=1`	Noise model selector.
`kf=0`	Flicker (1/f) noise coefficient.
`af=1`	Flicker (1/f) noise exponent.
`ef=1`	Flicker (1/f) noise frequency exponent.
`wnoi=1e-5 m`	Channel width at which noise parameters were extracted.

Operating-Point Parameters

`type=n`	Transistor type. Possible values are `n` or `p`.
`region=triode`	Estimated operating region. Possible values are `off`, `triode`, `sat`, or `subth`.
`reversed`	Reverse mode indicator. Possible values are `no` or `yes`.
`ids (A)`	Resistive drain-to-source current.
`vgs (V)`	Gate-source voltage.
`vds (V)`	Drain-source voltage.
`vth (V)`	Threshold voltage.

© 2023 Cadence Design Systems, Inc.

`vdsat (V)`	Drain-source saturation voltage.
`gm (S)`	Common-source transconductance.
`gds (S)`	Common-source output conductance.
`cgd (F)`	Gate-drain capacitance.
`cgs (F)`	Gate-source capacitance.
`ron (Ω)`	On-resistance.
`id (A)`	Resistive drain current.
`pwr (W)`	Power at op point.
`i1 (A)`	Resistive drain current.

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

41

Three-Terminal Nonlinear (Diffused and Poly-Silicon) Resistor Model and JFET Model (r3)

The r3 model is a nonlinear 3-terminal resistor model that includes self-heating, velocity saturation, statistical variations, and parasitic capacitances and currents. The core depletion pinching model formulation is for p-n junctions of diffused resistors, but is also applicable for the MOS behavior of polysilicon resistors. As p-n junction depletion pinching controls JFET device behavior, the r3 model is also applicable to JFETs.

This chapter covers the following information about the r3 model:

- Usage on page 2760
- Bias Dependence of Resistor Body Current on page 2761
- Bias Dependence of Parasitics on page 2765
- Geometry Dependence on page 2766
- Temperature Dependence on page 2771
- Noise on page 2774
- Operating Point Information on page 2776
- Statistical Variation on page 2776
- Notes on Parameter Extraction on page 2779
- Reference on page 2786
  - Component Statements on page 2786

© 2023 Cadence Design Systems, Inc.

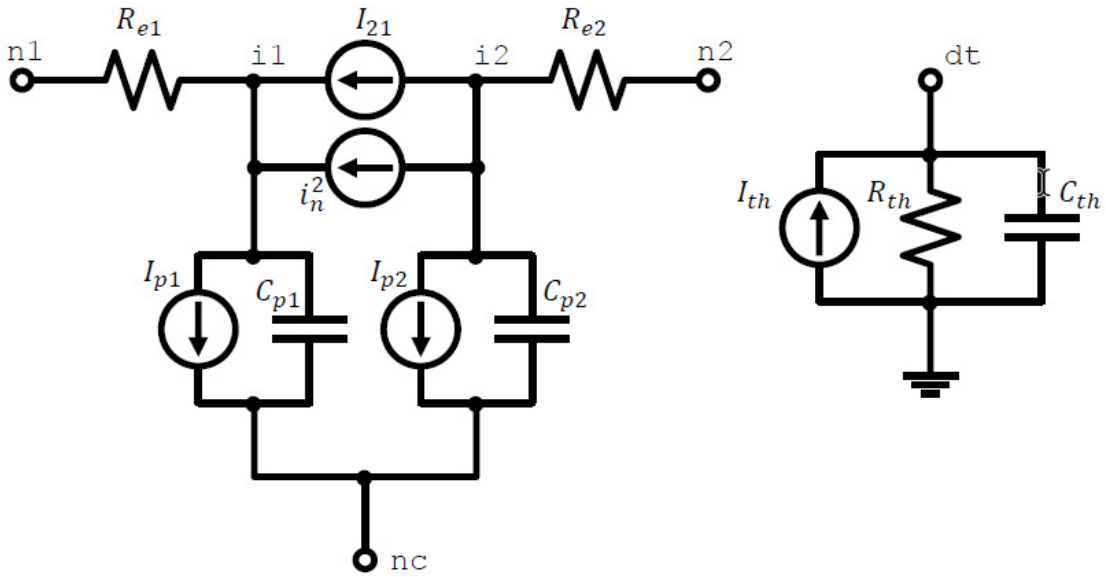
Usage

Exact usage may be simulator dependent. For example, whether the local temperature rise node for self-heating is made available or not, and whether the initial instance key-letter “r” is required.)

```
r<instanceName>  (<n1>  <nc>  <n2> [dt])  <modelName>  <instanceParameters>
.model  <modelName>  r3 <modelParameters>
```

The `dt` node is the rise above the local temperature caused by the thermal power dissipated by the device being modeled.

Figure 41-1 r3 Model Equivalent Network



Example

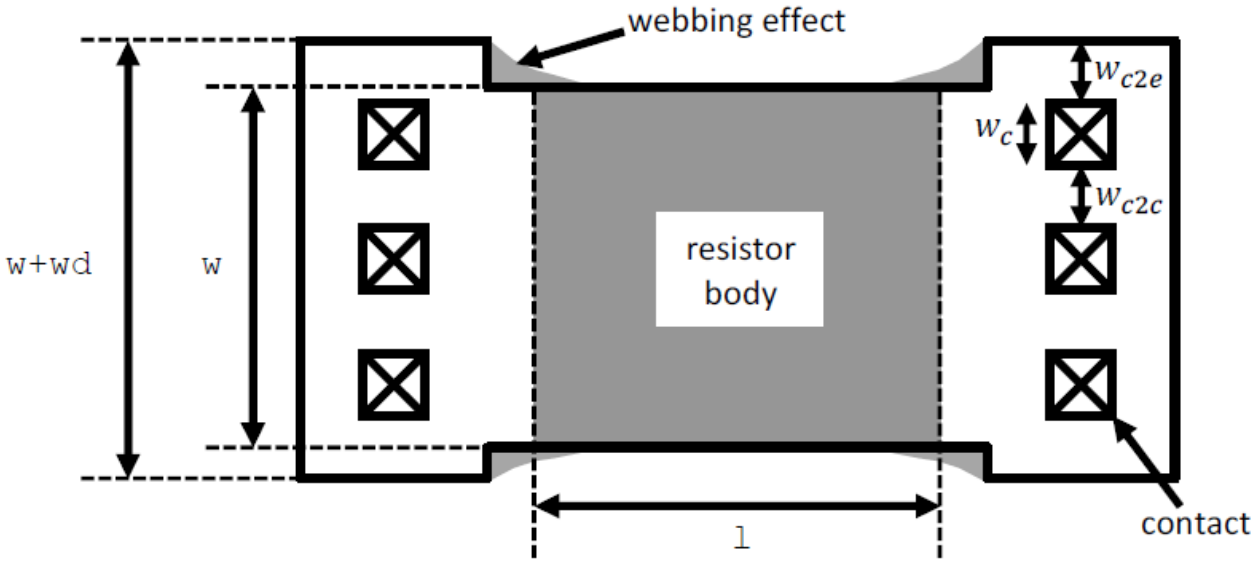
```
r00 n1 n2 n3 p0  l = 2e-6 w = 10e-6 m = 10 sw_et = 1

model p0 r3 type=1 shrink=50 xw=0.01 nwxw=0.1 wexw=0.1 xl=0.01xlw=0.2 dxlsat=0.01
+rcw=0.01 ca=1e-4 cja=1e-4 cp=1e-10 cjp=1e-10 dfw=1e-3 dfl=1e-3 dfwl=1e-3
+tc1=1e-3 tc2=1e-4 tc1l=1e-3 tc2l=1e-4 tc1w=1e-3 tc2w=1e-4 tc1rc=1e-3 tc2rc=1e-4
tc1kfn=1e-3
+tc1vbv=1e-3 tc2vbv=1e-4 tc1nbv=1e-3 sw_dfgeo=0 rc=1
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

The parameter examples are given below..

Figure 41-2 Instance Parameter Examples (End region dogbone may be asymmetric.)



Bias Dependence of Resistor Body Current

The r3 model includes three basic forms of bias dependence. First, from the depletion (p-n junction or MOS) pinching of the conducting channel of the resistor. Second, from velocity saturation. And third, from self-heating.

The basic p-n junction depletion pinching bias dependence comes from the analysis of [1], with the simplification of [2] (which merges the vertical and lateral bias dependence into a single bias dependent form with geometry dependent parameters). The applicability of the same general form of bias dependence for poly resistors, where the MOS depletion effect pinches the resistor body, was shown in [3]. The fundamental form of the depletion pinching model is

(41-1)

$$I_{depl} = gV_{21}, \quad g = gf \cdot \left(1 - df\sqrt{dp + V_i}\right), \quad V_i = V_{21} + 2V_{1c}$$

© 2023 Cadence Design Systems, Inc.

where V_{21} = V(i2) - V(i1) and V_{1c} = V(i1) - V(nc). Here, dp is the depletion potemtial (which is just the model parameter dp), df is the depletion factor, and gf is the conductance factor; these are determined from instance and model parameters as detailed in the section on geometry dependence.

The velocity saturation model is a mobility reduction term that divides the conductance factor. The model is smooth and symmetric, has value 1 when V_{21} = 0 , and asymptotically approaches 1+(E-ecorn)/ecrit for large field E= V_{21}/(leff_um + dx1sat) (leff_um is defined in the next section).

(41-2)

$$\mu_{red} = 1 + \sqrt{\left(\frac{E - E_{ce}}{2\,\mathrm{ecrit}}\right)^2 + \frac{\mathrm{du}\,E_{ce}}{\mathrm{ecrit}}} + \sqrt{\left(\frac{E + E_{ce}}{2\,\mathrm{ecrit}}\right)^2 + \frac{\mathrm{du}\,E_{ce}}{\mathrm{ecrit}}} - \sqrt{\left(\frac{E_{ce}}{\mathrm{ecrit}}\right)^2 + \frac{4\,\mathrm{du}\,E_{ce}}{\mathrm{ecrit}}}$$

where

(41-3)

$$E_{ce} = \sqrt{\mathrm{ecorn}^2 + (2\,\mathrm{du}\cdot\mathrm{ecrit})^2} - 2\,\mathrm{du}\cdot\mathrm{ecrit}.$$

The V_{21} used in the above expressions is smoothly limited so as not to exceed a saturation voltage V_{sat} , which is calculated as the V_{21} at which the output conductance becomes zero. To determine V_{sat} a slightly modified form of the velocity saturation model is used (the asymptotic form noted above), that allows closed form solution and guarantees that any imprecision in calculation of V_{sat} is such that the output conductance at saturation is positive, so that there are no “wiggles” around the transition to saturation. The smooth transition is implemented via [8]

(41-4)

$$V_{21,eff} = \frac{2V_{21}V_{sat}}{\sqrt{(V_{21} - V_{sat})^2 + 4\,\mathrm{ats}^2} + \sqrt{(V_{21} + V_{sat})^2 + 4\,\mathrm{ats}^2}}$$

© 2023 Cadence Design Systems, Inc.

where $\texttt{ats}_i$ `= ats=/(1 + atsl=leff_um)` is a model parameter that controls the limiting. This limiting function differs from those often used in compact MOSFET models; it preserves symmetry. The control voltage used is also limited, to the pinch-off voltage

(41-5)

$$V_{1c,eff} = V_{po} - \texttt{nst}V_{tv} \ln\left(1+\exp\left(\frac{V_{po}-V_{1c}}{\texttt{nst}V_{tv}}\right)\right), \quad V_{po} = \frac{1}{2df^2} - 0.5dp, \quad V_{tv} = kT/q\,.$$

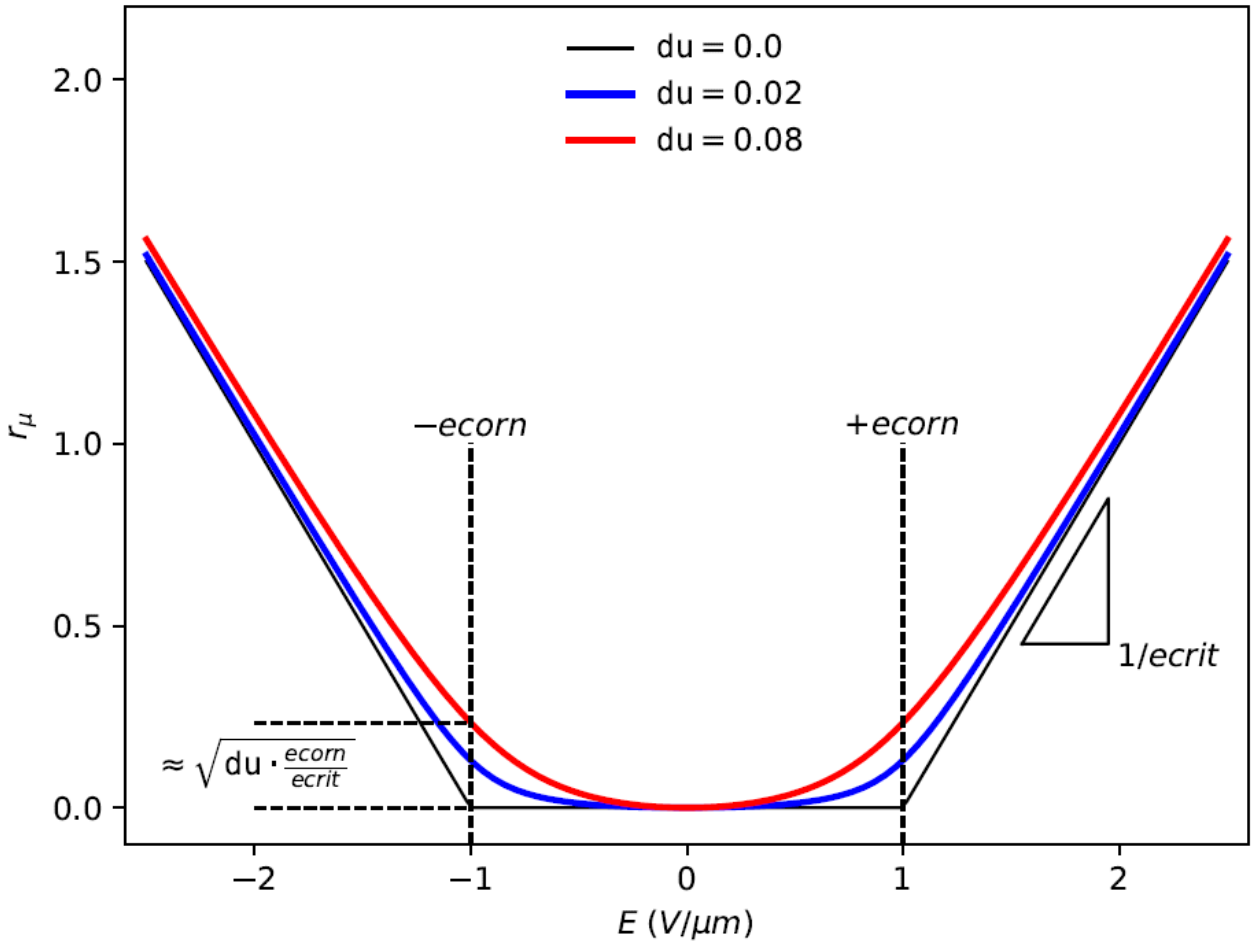
The self-heating affects the current through the temperature variation of the model parameters, primarily the sheet resistance. The current flowing between nodes n2 and n1 in see Figure 41-1 is then

(41-6)

$$I_{21} = I_{depl} \,/\, \mu_{red}$$

© 2023 Cadence Design Systems, Inc.

Figure 41-3 r_μ factor used in the velocity saturation model



Pinch-off behavior is primarily of importance for JFETs, and four models, selectable via the sw accpo switch, are available. The default is `sw_accpo = 0`, which is backwards-compatible with version 1.0.0. The next computationally simplest, and therefore fastest to simulate, limiting is selected with `sw_accpo = 1`, however this model only fairly crudely approximates the physically expected `1 - exp(-`V_{21}`/`ϕ_t`)` variation of I_{21} with V_{21} in full pinch-off. Setting `sw_accpo = 2` selects a model that more accurately approximates that behavior, at the expense of increased computation time, and `sw_accpo = 3` selects an even more accurate, but slightly more computationally expensive, form. A minimum conductance is enforced in full pinch-off to avoid numerical computation issues.

The self-heating affects the current through the temperature variation of the model parameters, primarily the sheet resistance. The current flowing between ports n2 and n1 in see Figure 41-1 is then

© 2023 Cadence Design Systems, Inc.

$$I_{21} = \frac{I_{depl}}{1 + r_{\mu}}.$$

Bias Dependence of Parasitics

If there are no area or perimeter component of saturation current, e.g. for poly resistors,

(41-7)

$$I_{p1} = I_{p2} = 0$$

If there are area and/or perimeter components of saturation current, e.g. as for diffused resistors, the parasitic diode currents are

(41-8)

$$I_{p1} = p1_um \cdot I_{sp}(T)\left(\exp(V_{c1}/(\mathrm{np} \cdot V_{tv})) - 1\right) + a1_um2 \cdot I_{sa}(T)\left(\exp(V_{c1}/(\mathrm{na} \cdot V_{tv})) - 1\right) + \mathrm{gmin} \cdot V_{c1}$$

$$I_{p2} = p2_um \cdot I_{sp}(T)\left(\exp(V_{c2}/(\mathrm{np} \cdot V_{tv})) - 1\right) + a2_um2 \cdot I_{sa}(T)\left(\exp(V_{c2}/(\mathrm{na} \cdot V_{tv})) - 1\right) + \mathrm{gmin} \cdot V_{c2}$$

where V_{c1} =V(nc)-V(i1), V_{c2} =V (nc)-V(i2), and gmin is a small conductance added by some simulators to improve convergence. Note that, when sw_accpo > 0, V_{c1} and V_{c2} are limited to pinch-off by a smoothing equation. Each individual component of the diode currents is linearized for forward biases greater than the voltage at which the component is imax.

The breakdown currents, which are added to each parasitic current, are

(41-9)

$$I_{b1} = -\mathrm{ibv}\left(\exp(-(V_{c1} + V_{bv}(T))/(n_{bv}(T)V_{tv})) - \exp(-V_{bv}(T)/(n_{bv}(T)V_{tv}))\right),$$

$$I_{b2} = -\mathrm{ibv}\left(\exp(-(V_{c2} + V_{bv}(T))/(n_{bv}(T)V_{tv})) - \exp(-V_{bv}(T)/(n_{bv}(T)V_{tv}))\right)$$

© 2023 Cadence Design Systems, Inc.

and each of these is linearized for reverse biases greater than the voltage as which the magnitude of the current is imax.

The parasitic capacitances comprise a bias independent component (intended for poly resistor modeling) and a bias dependent component (intended for diffused resistor modeling). The capacitances are implemented as bias dependent charges, but the resulting capacitances are given here

(41-10)

$$C_{p1} = p1_um\left(\texttt{cp}+\frac{C_{jp}(T)}{\left(1-V_{c1}/P_p(T)\right)^{\texttt{mp}}}\right)+a1_um2\left(\texttt{ca}+\frac{C_{ja}(T)}{\left(1-V_{c1}/P_a(T)\right)^{\texttt{ma}}}\right)$$

$$C_{p2} = p2_um\left(\texttt{cp}+\frac{C_{jp}(T)}{\left(1-V_{c2}/P_p(T)\right)^{\texttt{mp}}}\right)+a2_um2\left(\texttt{ca}+\frac{C_{ja}(T)}{\left(1-V_{c2}/P_a(T)\right)^{\texttt{ma}}}\right).$$

The forward bias junction capacitance components are modified so that when the junction voltage (V_{c1} or V_{c2}) reaches `fc` multiplied by the associated built-in potential, the capacitance becomes linear in voltage, to avoid the singularity at the built-in potential. If the smoothing parameters `aja` and `ajp` are positive, then the transition from depletion to linear capacitance is done smoothly and not abruptly.

The thermal resistance and capacitance for the self-heating model are linear, and do not depend on temperature. The thermal power used for self-heating modeling is the sum of the powers of all dissipative (non-storage) elements in the equivalent circuit; i.e. the resistor body, the two end resistances, and two parasitic current sources.

Geometry Dependence

Unless otherwise noted, all `r3` model quantities scale with the multiplicity parameter m as defined in the *Verilog-A Language Reference Manual (LRM)*, version 2.4.

The `r3` model includes several mechanisms for deviations of the effective electrical length and width of a resistor from the drawn (design, or mask) values. The drawn length and width of the resistor, in units of microns, are

© 2023 Cadence Design Systems, Inc.

(41-11)

$$l_um = \mathtt{l} \cdot \mathtt{scale} \cdot (1 - \mathtt{shrink}/100) \cdot 10^6 ,$$

$$w_um = \mathtt{w} \cdot \mathtt{scale} \cdot (1 - \mathtt{shrink}/100) \cdot 10^6$$

Because subcircuit models for resistors can consist of multiple resistance sections connected in series, it is desirable to be able to switch on and off the “end corrections” for length to facilitate implementation of such multi-section models. This is the function of the `c1` and `c2` instance parameters of the `r3` model. The effective length offset is

(41-12)

$$xleff = (\mathtt{xl} + \mathtt{xlw}/w_um)((\mathtt{c1} > 0) + (\mathtt{c2} > 0))/2$$

(which is zero if neither end is contacted, `xl+xlw/w_um` if both ends are contacted, and one half of the latter if only one end is contacted). The effective electrical length, in microns, is

(41-13)

$$leff_um = l_um + xleff$$

For flexibility of separately fitting low bias resistance and velocity saturation, an additional offset `dxlsat` is added to `leff _ um` for calculation of the electric field used in the velocity saturation model.

The effective width offset includes the physical effect models derived in [4]. These comprise a fixed offset for mask bias, lithography, and etching effects, and geometry dependent offsets for LOCOS, the webbing effect, and the finite dopant source effect. The effective electrical width, in microns, is

(41-14)

$$weff_um = \frac{w_um + \mathtt{xw} + (\mathtt{nwxw}/w_um) + \mathtt{fdxwinf}(1 - \exp(-w_um/\mathtt{fdrw}))}{1 - \mathtt{wexw} \cdot wd_um/(l_um \cdot w_um)}$$

where the width of the dogbone, for the webbing effect model, in units of microns, is

© 2023 Cadence Design Systems, Inc.

(41-15)

$$wd_um = \texttt{wd} \cdot \texttt{scale} \cdot (1 - \texttt{shrink}/100) \cdot 10^6$$

The depletion factor depends on geometry as

$$df = \texttt{dfinf} + \frac{\texttt{dfw}}{W} + \frac{\texttt{dfl}}{L} + \frac{\texttt{dfwl}}{WL}$$

where the width `W` and length `L` are effective geometries if `sw_geo=1` and design geometries otherwise (in units of micron).

The depletion potential depends on geometry in version 1.1.0 as

(41-16)

$$dp_i = \texttt{dp} \cdot \left(1 + \frac{\texttt{dpw}}{W^{\texttt{dpwe}}}\right) \cdot \left(1 + \frac{\texttt{dpl}}{L^{\texttt{dple}}}\right) \cdot \left(1 + \frac{\texttt{dpwl}}{W^{\texttt{dpwe}} L^{\texttt{dple}}}\right)$$

(In version 1.0.0, `dpi = dp`.)

The zero-bias resistance, which factors in the zero-bias depletion pinching, is then

(41-17)

$$R_0 = \texttt{rsh} \frac{leff_um}{weff_um}\left(1.0 - df\sqrt{dp}\right), \quad gf = 1/R_0$$

Although end effects, such as spreading resistance and contact resistance, are assumed to be modeled via the `xl` parameter, the temperature coefficients of the end effects may differ from those of the body of the resistor. Simple analysis shows that these different temperature coefficients can be accounted for by introducing inverse length dependence to the temperature coefficients. A width dependence of temperature coefficients of resistance is also included in the model, and version 1.1.0 also includes an area dependence. Therefore, in `r3_cmc ->r3`

© 2023 Cadence Design Systems, Inc.

(41-18)

$$T_{C1}^{eff} = \texttt{tc1} + \frac{\texttt{tc1w}}{weff_um} + \frac{0.5 \cdot [(c1 > 0) + (c2 > 0)]}{leff_um} \cdot \left(\texttt{tc1l} + \frac{\texttt{tc1wl}}{weff_um}\right),$$
$$T_{C2}^{eff} = \texttt{tc2} + \frac{\texttt{tc2w}}{weff_um} + \frac{0.5 \cdot [(c1 > 0) + (c2 > 0)]}{leff_um} \cdot \left(\texttt{tc2l} + \frac{\texttt{tc2wl}}{weff_um}\right)$$

where the length dependence is switched on, off, or halved, depending on whether the resistor is contacted at both ends, not contacted, or contacted at only one end, respectively. The dependence of the temperature coefficients on whether a resistor is contacted or not enables consistent modeling of temperature coefficients for single or multiple section models.

The thermal conductance and capacitance include area, perimeter, contact, and fixed components. Asymptotically for a large area device, the heat flow is perpendicular to the plane of heat generation in the resistor, and the heat energy stored in a device depends on its volume, hence the area dependent component. For a long resistor, as it becomes narrower more of the heat flow is conducted by a “fringe” path at the edges of the device, hence the perimeter dependent component. As both length and width decrease, the thermal conditions in the device asymptotically approach that of a point source in an infinite medium, hence the fixed component. Contacts conduct heat flow, hence the contact component. The thermal conductance and capacitance are therefore

(41-19)

$$g_{TH} = \texttt{gth0} + \texttt{gthp} \cdot p_um + \texttt{gtha} \cdot a_um2 + \texttt{gthc} \cdot (\texttt{c1} + \texttt{c2})$$
$$c_{TH} = \texttt{cth0} + \texttt{cthp} \cdot p_um + \texttt{ctha} \cdot a_um2 + \texttt{cthc} \cdot (\texttt{c1} + \texttt{c2})$$

the area and perimeter are calculated as

(41-20)

$$a_um2 = l_um \cdot w_um$$

$$p_um = 2l_um + \big((\texttt{c1} > 0) + (\texttt{c2} > 0)\big)w_um\ .$$

The calculated perimeter therefore depends on whether the ends are contacted or not. Often, the design dimensions of the body of a resistor differ from the overall dimensions of the device, for example if the design length is considered to be the unsalicided length of a poly resistor, the total resistor length will typically include silicided contact regions. So it is not

© 2023 Cadence Design Systems, Inc.

readily apparent what dimension should be used in calculation of the thermal conductance and capacitance. That is why the design dimensions, rather than some effective dimensions (whose value is calculated to best fit DC electrical data), are used. This turns out to be reasonable (with the exception that differences between the perimeter components along length and width dimensions are ignored), because if there is some difference Δ between design and effective dimensions for thermal conductance modeling, then for a device contacted at both ends

(41-21)

$$g_{TH} = \mathtt{gth0} + \mathtt{gthp}(2l_um + 2w_um + 4\Delta) + \mathtt{gtha}(l_um + \Delta)(w_um + \Delta)$$
$$= \left(\mathtt{gth0} + 4\mathtt{gthp}\cdot\Delta + \mathtt{gtha}\cdot\Delta^2\right) + (\mathtt{gthp} + 0.5\mathtt{gtha}\cdot\Delta)p_um + \mathtt{gtha}\cdot a_\mathtt{um2}$$

therefore any difference between design and effective dimensions can be taken into account by appropriate characterization of the fixed, perimeter, and area component parameters.

Because the *local* thermal conductance differs between the edge of a device and the center of a device, it is higher at the edge because of *fringing* conductance, the temperature of a resistor undergoing self-heating is not spatially uniform, but is lower at the edges than in the middle. This is not taken into account in the `r3` model.

The end resistances are calculated from the resistance per contact and the number of contacts (parallel to the width dimension; adding contacts parallel to the length dimension, which can be done for reliability purposes, does not alter the resistance much – unless the contact adjacent to the resistor body fails)

(41-22)

$$R_{e1} = \frac{\mathtt{rc} + \mathtt{rcw}/w_um}{\mathtt{c1}}, \quad R_{e2} = \frac{\mathtt{rc} + \mathtt{rcw}/w_um}{\mathtt{c2}}$$

The velocity saturation model includes geometry dependence in the bias dependent portion of the model evaluation, as it is formulated in terms of the electric field $\mathtt{E}=V_{21}/(\mathtt{leff_um+dxlsat})$.

The areas and perimeters of the end region partitions, used in parasitic calculations, are in units of microns

© 2023 Cadence Design Systems, Inc.

(41-23)

$$p1_um = \texttt{p1}\cdot\texttt{scale}\cdot(1-\texttt{shrink}/100)\cdot 10^6,$$

$$a1_um2 = \texttt{a1}\cdot\left(\texttt{scale}\cdot(1-\texttt{shrink}/100)\cdot 10^6\right)^2,$$

$$p2_um = \texttt{p2}\cdot\texttt{scale}\cdot(1-\texttt{shrink}/100)\cdot 10^6,$$

and

(41-24)

$$a2_um2 = \texttt{a2}\cdot\left(\texttt{scale}\cdot(1-\texttt{shrink}/100)\cdot 10^6\right)^2.$$

If the number of contacts is not known, it can be calculated (see Figure 41-2). Let the contact width (in the direction parallel to the resistor width) be w_c, the minimum spacing from a contact to the edge of the region it is in at the contact head of the resistor be w_{c2e}, and the (minimum) spacing between contacts be w_{c2c}. If (as in some older technologies) contacts can be scaled, then `rc` should be set to be the resistance of a minimum width contact and

(41-25)

$$c[1,2] = \frac{\max(\mathrm{w}+\mathrm{wd}, w_c + 2w_{c2e}) - 2w_{c2e}}{w_c}$$

and for technologies where the contact width is fixed (assuming the maximum possible number of contacts are places)

(41-26)

$$c[1,2] = \mathrm{int}\left(\frac{\max(\mathrm{w}+\mathrm{wd}, w_c + 2w_{c2e}) - 2w_{c2e} + w_{c2c}}{w_c + w_{c2c}}\right).$$

Temperature Dependence

The zero-bias resistance $\texttt{R}_0$ varies with temperature as

© 2023 Cadence Design Systems, Inc.

(41-27)

$$R_0(T) = R_0 \cdot tfac$$

where R_0 is the nominal value of the zero-bias resistance at the nominal temperature `tnom` and `tfac` is the resister temperature factor, given by

$$tfac = \left(1 + T_{C1}^{eff} \cdot dT + T_{C2}^{eff} \cdot dT^2\right)$$

where `dT` is the temperature difference (including self-heating) with respect to `tnom`, and T^{eff}_{C1} and T^{eff}_{C2} are first (linear) and second (quadratic) order effective temperature coefficients. Smooth limiting of the resistance temperature factor `tfac` is implemented to a minimum value of 0.01. The conductance factor is then

(41-28)

$$gf = 1/R_0(T).$$

The depletion potential has a temperature dependence in version 1.1.0, given by

$$dp(T) = dp_i \cdot \left(1 + \texttt{tc1dp} \cdot dT + \texttt{tc2dp} \cdot dT^2\right).$$

The velocity saturation temperature dependence in version 1.1.0 is activated by the parameter `sw_vsatt`. If `sw_vsatt` = 0, then there is no temperature dependence; this is the default for compatibility reasons. If `sw_vsatt` = 1, then the corner and critical fields for velocity saturation are adjusted according to

$$\begin{aligned} ecorn(T) &= \texttt{ecorn} \cdot rT^{\texttt{xvsat}} \cdot tfac \\ ecrit(T) &= \texttt{ecrit} \cdot rT^{\texttt{xvsat}} \cdot tfac \end{aligned}$$

where `rT` is the ratio of device to nominal temperature (in Kelvin), `xvsat` is a model parameter, and `tfac` is the same temperature factor as the resistor body.

© 2023 Cadence Design Systems, Inc.

The end resistances vary with temperature as

(41-29)

$$R_{e[1,2]}(T) = R_{e[1,2]}\left(1 + \mathtt{tc1rc}\cdot dT + \mathtt{tc2rc}\cdot dT^2\right)$$

and again the temperature coefficient in (30) is limited to a lower value of 0.01. The anomalous increase in conductance with Vds for some p-body resistors is due to contact resistance self-heating and negative temperature coefficients; this was pointed out in [3].

The parasitic diode saturation currents vary with temperature as

(41-30)

$$I_{sa}(T) = \mathtt{isa}\cdot rT^{\mathtt{xis/na}} \exp\left(-\mathtt{ea}\frac{1-rT}{\mathtt{na}\cdot V_{tv}}\right)$$

$$I_{sp}(T) = \mathtt{isp}\cdot rT^{\mathtt{xis/np}} \exp\left(-\mathtt{ea}\frac{1-rT}{\mathtt{np}\cdot V_{tv}}\right)$$

where `rT` is the ratio ofdevicetonominal temperature (in Kelvin), and $\mathtt{V_{tv}}$= `kT/q` is the thermal voltage. The temperature dependence of the junction built-in potentials is

(41-31)

$$P_a(T) = \mathtt{pa}\cdot rT - 3V_{tv}\ln(rT) - \mathtt{ea}\,(rT-1)$$

$$P_p(T) = \mathtt{pp}\cdot rT - 3V_{tv}\ln(rT) - \mathtt{ea}\,(rT-1)$$

with a physically based modification to smoothly limit the potential to zero for high temperatures, and not allow it to become negative. The area and perimeter junction zero-bias capacitance temperature variations are

© 2023 Cadence Design Systems, Inc.

(41-32)

$$C_{ja}(T) = \mathtt{cja}\left(\frac{\mathtt{pa}}{P_a(T)}\right)^{\mathtt{ma}}$$

and

(41-33)

$$C_{jp}(T) = \mathtt{cjp}\left(\frac{\mathtt{pp}}{P_p(T)}\right)^{\mathtt{mp}}.$$

The flicker noise coefficient varies with temperature as

(41-34)

$$K_{FN}(T) = \mathtt{kfn}\left(1 + \mathtt{tc1kfn}\cdot dT\right)$$

where `kfn` and `tc1kfn` are model parameters (and the resulting $\mathtt{K_{FN}}$ is clipped to zero as a lower limit).

The breakdown voltage and ideality factor vary with temperature as

(41-35)

$$V_{bv}(T) = \mathtt{vbv}\left(1 + \mathtt{tc1vbv}\cdot dT + \mathtt{tc2vbv}\cdot dT^2\right),$$

$$n_{bv}(T) = \mathtt{nbv}\left(1 + \mathtt{tc1nbv}\cdot dT\right).$$

Noise

The noise model comprises two body components, a thermal (white) noise component and a flicker (`1/f`) noise component, thermal noise components for each contact resistance, and short noise components for each parasitic diode. These components are noise current spectral density (in $\mathtt{A^2/Hz}$) that are implemented as a noise current sources in parallel with the associated element.

© 2023 Cadence Design Systems, Inc.

The thermal noise component of the resistor body is based on its DC conductance,

(41-36)

$$i^2_{thermal,body} = 4kT_K G_{eff}(T)$$

where `k` is Boltzmann's constant, T_K is the device temperature (in Kelvin, including the effect of self-heating), and G_{eff} is the effective conductance of the resistor (at the temperature `T`). Similarly the thermal noise of each end resistances is

(41-37)

$$i^2_{thermal,end} = 4kT_K / R_e(T) .$$

The flicker noise component is DC current dependent and scales with geometry per the physical restrictions mentioned earlier.

(41-38)

$$i^2_{flicker,body} = K_{FN}(T)\left(\frac{I_{21}}{W}\right)^{\mathtt{afn}} \frac{W}{L}\frac{1}{f^{\mathtt{bfn}}}$$

where `f` is frequency (in Hz), `afn` and `bfn` are model parameters, K_{FN}`(T )` is the temperature dependent flicker noise coefficient, I_{21} is the DC current in the resistor body, and `W` and `L` are the resistor width and length respectively, in units micron (µm). If the switch parameter for flicker noise geometry calculation `sw_fngeo` is 0 (false) then `W` and `L` are design geometries, `w_um` and `l_um` respectively, else if it is 1 (true) then `W` and `L` are effective geometries, `weff_um` and `leff_um` respectively.

The shot noise components are

(41-39)

$$i^2_{shot,diode} = 2qI_{diode}$$

for each parasitic diode, where I_{diode} is the current in the diode.

© 2023 Cadence Design Systems, Inc.

Note: If self-heating is included, then possibly there is a frequency dependence to the flicker noise because of the thermal time constant. There is no data to verify this at present so a frequency independent noise current spectral density is used.

Operating Point Information

Name	Units	Description
`v`	V	voltage across resistor
`ibody`	A	current through resistor body
`power`	W	dissipated power
`leff_um`	μm	effective electrical length in μm
`weff_um`	μm	effective electrical width in μm
`r0`	Ω	zero-bias resistance
`r_dc`	Ω	DC Resistance (including bias dependence)
`r_ac`	Ω	AC Resistance (including bias dependence)
`rth`	K/W	thermal resistance
`cth`	sW/K	thermal capacitance
`dt_et`	K	self-heating temperature rise
`linearity_factor`		

Table 41-1 Operating Point Parameters

All flow and parameter quantities are for the overall device and include the rffect of the multliplicity parameter `m`.

Statistical Variation

The `r3` model includes both global (inter-die, correlated between individual devices) and local (mismatch, uncorrelated between individual devices) variations. These can be added “on top” of a core model using subcircuits, however this can involve increased complexity in model parameter files and increased computational overhead during simulation. Therefore statistical variation is “built-in” to the `r3` model, including instance parameters for control of mismatch variation for individual devices.

© 2023 Cadence Design Systems, Inc.

Besides convenience and efficiency, the statistical variation modeling in `r3` naturally embodies the geometry dependence of total variation in a device, which is not possible with statistical modeling based on a geometry-independent global variation and geometry dependent correlation coefficients. Since it is based on independent statistical parameters for global variation and instance specific local variation, it does not require generation of correlated samples for distributional (i.e. Monte Carlo-like) simulation; if correlations were used then N (N ?1) 2 of them are required for each statistical parameter for each of N devices.

Statistical variations are modeled in three parameters; the sheet resistance, the effective length variation, and the effective width variation. These are considered as the primary physical process parameters that determine the resistor behavior. At present, there is no variation (global or local) in other physical quantities such as contact resistance, other parasitics (zero-bias depletion capacitance for diffused resistors varies with doping), or the parameters that control the nonlinearity of the model. If experimental data shows that linkage to more fundamental physical quantities such as doping levels and layer thicknesses is required to model correlations and statistical variations, this will be added in the future.

The local variation of the effective width is controlled by line edge roughness in the length dimension; its variance is therefore inversely proportional to the resistor length `L`. The local variation of the effective length is controlled by line edge roughness in the width dimension; its variance is therefore inversely proportional to the resistor width `W`.The local variation of the sheet resistance is controlled by random dopant fluctuations; its variance is therefore inversely proportional to the area of the resistor, `WL`. For flexibility in fitting experimental data, the `sw_mmgeo` flag allows the controlling geometries `W` and `L` to be either drawn or effective (as calculated before the statistical variations are applied, to avoid an implicit dependency that requires an iterative solution).

The total variance of a parameter is the sum of the variances of the global variance (which is independent of geometry) and the local variance (which depends on geometry `g` , which can include area, width, and length),

(41-40)

$$\sigma^2_{total} = \sigma^2_{global} + \sigma^2_{local}(\vec{g}) .$$

This naturally embodies the geometry dependence of the overall variance of a particular parameter. For statistical simulation, the perturbations of the global variation and the individual instance variation are expected to be statistically independent. But “proper” statistical simulation of a circuit requires inclusion of both global parameters and local parameters for every instance of a device type in a circuit. This can cause the number of statistical parameters included in a statistical simulation to increase proportionally with the number of devices in the circuit, with a concomitant explosion in the number of (local)

© 2023 Cadence Design Systems, Inc.

statistical parameters needed to be included for a “proper” analysis. This is, for brute force statistical simulation, clearly impractical.

The `r3` model therefore includes a mechanism for more efficiently accounting for the geometry dependence of the overall variation. The `sw_mman` switch is provided to allow specification on an instance-by-instance basis of whether a device is being included in mismatch analysis. If yes, then both global and local (instance specific) statistical variation parameters are expected to be generated for each device instance, and the global and local variations are modeled separately. If no, which is appropriate for devices for which local variation is not expected to affect circuit performance, then the global variance for a device is adjusted to be the total variance for that device. This appropriately models the geometry dependent total variance for the device, with the consequence that it makes the total variation completely

correlated between all devices (that are not selected for individual mismatch analysis); this will cause overestimation of the variation of the circuit performances, i.e. the simulations from this will be pessimistic.

If mismatch analysis is selected, then the statistical variations are

(41-41)

$$weff_um = weff_um_{nom} + \texttt{nsig_w} \cdot \texttt{sig_w} + \frac{\texttt{nsmm_w} \cdot \texttt{smm_w}}{\sqrt{\texttt{m} \cdot L}}$$

$$leff_um = leff_um_{nom} + \texttt{nsig_l} \cdot \texttt{sig_l} + \frac{\texttt{nsmm_l} \cdot \texttt{smm_l}}{\sqrt{\texttt{m} \cdot W}}$$

$$rsh = \texttt{rsh}_{nom} \exp\left(0.01\left(\texttt{nsig_rsh} \cdot \texttt{sig_rsh} + \frac{\texttt{nsmm_rsh} \cdot \texttt{smm_rsh}}{\sqrt{\texttt{m} \cdot WL}}\right)\right)$$

where the nominal values are those defined in the section on geometry dependence. (The above expressions are used to update the effective geometries and resistance values, and all previous model equations use the values calculated earlier. However, for clarity of presentation and ease of interpretation, the previous equations are not cluttered with the statistical variations).

The variations in effective length and width are absolute, and are additive, and that the variation in sheet resistance is multiplicative. For small variations $\exp \langle \chi \rangle \approx \langle 1 + \chi \rangle$ hence the `rsh` variation is relative (it is more natural to think in terms of a % variation than an

© 2023 Cadence Design Systems, Inc.

absolute variation). For large variations, as can be seen in some resistors, statistical sampling can generate small or negative values of `rsh`, which are unphysical. Quantities with large variations typically exhibit a log-normal distribution, and the exponential mapping transforms the normally distributed basic statistical parameters into a log-normal distribution for `rsh` if the variation is large.

Note: Strictly the unit "%" for the standard deviations of rsh is only for a small variation; if the variation is large then the exponential transformation modifies this.

This approach allows statistical modeling via uncorrelated normal variables, yet can capture log-normal distributions and correlations between parameters, via the dependencies on the fundamental process parameters that control the device behavior. Mismatch is modeled via independent perturbations in individual devices, which is physically correct. To simulate mismatch between two devices the mismatch instance parameters for both devices must be selected for statistical perturbation, and this easily extends to more than two devices, and implicitly accounts for geometry differences between different devices. If mismatch is characterized from differential measurements between two identically sized devices, then the measured standard deviations need to be divided by 2 when mapped into the model parameters `smm_w`, `smm_l`, and `smm_rsh`.

If mismatch analysis is not selected, then the total variance is used as the global variance,

(41-42)

$$weff_um = weff_um_{nom} + \mathtt{nsig_w}\sqrt{\mathtt{sig_w}^2 + \mathtt{smm_w}^2/(\mathtt{m}\cdot L)}$$

$$leff_um = leff_um_{nom} + \mathtt{nsig_l}\sqrt{\mathtt{sig_l}^2 + \mathtt{smm_l}^2/(\mathtt{m}\cdot W)}$$

$$rsh = \mathtt{rsh}_{nom}\exp\left(0.01\cdot\mathtt{nsig_rsh}\left(\mathtt{sig_rsh}^2 + \mathtt{smm_rsh}^2/(\mathtt{m}\cdot WL)\right)\right).$$

The `nsig` parameters should be equated to global statistical variables in model files, as they are model parameters, not instance parameters. These parameters then should vary with case/corner and distributional simulations.

Notes on Parameter Extraction

This section provides some information that can help in setting up parameter extraction algorithms. It describes techniques to get initial values that can then be refined by

© 2023 Cadence Design Systems, Inc.

optimization. It does not give a complete and perfect procedure for parameter extraction. As this section does not deal with the details of the model, but how to determine parameters from measured data, `V` and `I` have been used in this section only as the voltage across, and current through, the complete resistor (and not just the core resistor body, as is done in previous sections).

Techniques for extraction of basic parameters, such as `rsh`, `xl`, and `xw`, some temperature coefficients and their geometric scaling, etc. are provided earlier and are not repeated here. Additional extraction techniques for the core bias dependence are provided here.

The fundamental depletion (`p-n` junction or MOS) pinching component of the model is given earlier. Velocity saturation and self-heating affect the bias dependence for `E=VL` significantly different from zero. Therefore the basic parameters of the model for one geometry, `gf`, `df`, and `dp`, should come from analysis of data where depletion pinching dominates, i.e. from low `V`, ideally extrapolated to, or measured (from small-signal AC excitation) at `V=0`. (The large signal conductanc `eg=IV` cannot be directly calculated at `V=0`, but is equal to the small signal conductance `g=I/V` at that bias).

There are at least three approaches to determine the basic depletion pinching parameters, for diffused resistors. If the conductanc `eg` is known from measurements at three different biases, then the parameters can be calculated as follows. For these biases, (V_i=V+2V_{1c} for the i^{th} values of `V` and V_{1c})

(41-43)

$$g_i = gf\left(1 - df\sqrt{dp + V_i}\right)$$

therefore

(41-44)

$$g_i - g_j = gf\ df\left(\sqrt{dp + V_j} - \sqrt{dp + V_i}\right)$$

and manipulating the above equation for two pairs of biases, and forming the difference, gives

(41-45)

$$\frac{\sqrt{dp + V_2} - \sqrt{dp + V_1}}{g_1 - g_2} - \frac{\sqrt{dp + V_3} - \sqrt{dp + V_1}}{g_1 - g_3} = 0\,.$$

© 2023 Cadence Design Systems, Inc.

Starting with an initial estimate of `dp` = 2 , the equation can be solved using Newton-Raphson iteration. Then

(41-46)

$$df = \frac{g_1 - g_3}{g_1\sqrt{dp + V_3} - g_3\sqrt{dp + V_1}}$$

and

(41-47)

$$gf = \frac{g_1}{1 - df\sqrt{dp + V_1}}.$$

An alternative is to, assuming that the depletion pinching effect is small, initialize `gf` to `g` at the lowest (zero) V_i, set `dp` = 2 , and then calculate an initial `df` at the highest V_i.A 3 dimensional Newton-Raphson iteration can then be used to solve for `gf`, `df`, and `dp` at the three V_i values.

A direct solution also exists.

(41-48)

$$\frac{1}{df^2} + \frac{g_i^2}{df^2 gf^2} - \frac{2g_i}{df^2 gf} = dp + V_i$$

and forming the difference between this quantity for two combinations of the selected three bias points gives

(41-49)

$$\begin{bmatrix} g_1^2 - g_2^2 & 2(g_2 - g_1) \\ g_1^2 - g_3^2 & 2(g_3 - g_1) \end{bmatrix} \begin{bmatrix} p_1 \\ p_2 \end{bmatrix} = \begin{bmatrix} V_1 - V_2 \\ V_1 - V_3 \end{bmatrix}$$

where

© 2023 Cadence Design Systems, Inc.

(41-50)

$$\text{where } p_1 = 1/df^2 gf^2 \text{ and } p_2 = 1/df^2 gf .$$

These two quantities can be calculated from the V_i and gi data using the above equation

(41-51)

$$gf = p_2 / p_1 ,$$

$$df = 1/\sqrt{p_2 gf} ,$$

$$dp = \frac{1}{df^2} + \frac{g_1^2}{df^2 gf^2} - \frac{2g_1}{df^2 gf} - V_i .$$

The nonlinearity from the depletion pinching has the greatest sensitivity to dp for small V_i, therefore one bias should be at as small a V as possible (zero, if small-signal conductance is being used as opposed to large signal conductance) and $V_{1c}=0$.

Preferably data should be taken for 3 or more V_{1c} values (including zero). If such data are available then the other points used for extraction should be at the smallest V_{ds} and the second lowest V_{1c}, and the smallest V and the highest V_{1c}. If data for only two V_{1c} values (including zero) are available, besides the lowest V and lowest V_{1c} point, use the lowest V_{1c} point with a V higher than the smallest value and both small enough to ensure self-heating and velocity saturation effects are negligible and large enough to be sufficiently different from the lowest V value (so as not to be sensitive to measurement noise), and again as a third bias use the smallest V and the highest V1c point.

For poly resistors, the *pinching* effect is from the depletion region at the bottom of the resistor, and the conductance of a poly resistor is

(41-52)

$$g = \frac{XW}{\rho L}\left(1 - \frac{k_{Si} T_{ox}}{k_{ox} X \sqrt{V_0}} \sqrt{V_0 + 2V_{1c}}\right)$$

© 2023 Cadence Design Systems, Inc.

where X, W and L are the thickness, width, and length of the polysilicon film that makes up the resistor, k_{Si} and k_{ox} are the relative dielectric permittivities of silicon and silicon dioxide, T_{ox} is the oxide thickness, ρ is the resistivity, and $V_0 = q\varepsilon_{Si}N/C^2_{ox}$. This can be seen to have the same general form, which is why the basic depletion pinching bias dependence of the r3 model is also, with appropriate parameters, suitable for modeling poly resistors.

For typical poly resistors on relatively thick oxides, the V_0, which can be identified as the several tens or hundreds of volts, compared to the 1-2V value (twice the built-in potential) for dp resistor. Therefore the resistor conductance is

(41-53)

$$g \approx gf\left(1 - df\sqrt{dp} - df V_{1c}/\sqrt{dp}\right).$$

which, as measured data also shows, has a linear $g(V_{1c})$ dependence. This means that there are only two independent quantities that can be extracted from measured data, the zero-bias value $g_0 = gf\langle 1 - df\sqrt{dp}\rangle$ and the slope $s = -(gfdf)/(\sqrt{dp})$ .Yet thereare three parameters for the model. Physical quantities areneeded tobreak this indeterminacy.

The value of $V_0 = q\varepsilon_{Si}N/C^2_{ox}$ can be calculated; however because of incomplete dopant activation this can overestimate its value. It is better to calculate it from the poly sheet resistance

(41-54)

$$dp = \frac{\varepsilon_{Si} T_{ox}^2}{\mu_0 X \rho_s \varepsilon_{ox}^2}$$

where μ_0 and ρ_s are the low field mobility and sheet resistance of the poly, respectively. Therefore from the slope and zero-bias conductance

(41-55)

$$df = -\frac{s\sqrt{dp}}{g_0 - s\sqrt{dp}}$$

Calculating large signal conductance g=I/V for small V can be problematic; V needs to be small enough so that self-heating and velocity saturation effects do not affect the device, but large enough so that g can be calculated reliably. For poly resistors, there is an alternative method to characterize the depletion pinching parameters. If $V_{1c}=0$, and V is swept from a

© 2023 Cadence Design Systems, Inc.

negative to a positive value (this is not possible for diffused resistors, as the parasitic junction diodes would become forward biased), then the conductance `g(V)` has a roughly parabolic shape near `V=0`. For poly resistors with negative temperature coefficients of resistance, the conductance increases (from self-heating) as the magnitude of the applied `V` bias increases (for sufficiently high `V` the conductance starts to decrease from velocity saturation, leading to a *horned* characteristic in the plot). If the temperature coefficient of resistance is positive, the conductance will decrease as `V` increases (in roughly the same manner as the effect of velocity saturation, which makes them difficult to distinguish, without including additional data such as the frequency dependence of the output conductance).

For some magnitude of applied `V`, of both positive and negative signs, the effects of velocity saturation and self-heating should be the same (with the difference noted below). Therefore the plot of `g(V)` should, to first order, be symmetric about `V=0`.

However because the V_{2c} bias differs between the positive and negative `V` cases, the amount of depletion pinching is different, and this introduces a slight asymmetry in the characteristic. (If the currents differ then so will the self-heating, but this should be a second order effect and so is ignored here). Because the effects of velocity saturation and self-heating affect the zero bias conductance and the mobility reduction parts of the model, the ratio of the magnitudes of currents with positive and negative `V` of equal magnitude cancel these

(41-56)

$$gf = \frac{g_0}{1 - df\sqrt{dp}}.$$

and therefore reveal the effect of depletion pinching. As with the low `V` bias analysis above, `dp` can be calculated and then `df`, or at least in initial value of it for optimization, can be determined from the slope of the ratio in the above equation versus `V` (once it stabilizes, the ratio tends to be *noisy* for low `V`).

For poly resistors where self-heating dominates the non-linearity, at low `V`, the `g(V)` parabolic shape is primarily determined from mobility reduction due to self-heating, therefore

(41-57)

$$\frac{I_p}{I_m} = \frac{I(+V)}{I(-V)}\bigg|_{V_{c1}=0} = \frac{1 - df\sqrt{dp + V}}{1 - df\sqrt{dp - V}} \approx 1 - V\frac{df}{\sqrt{dp}}$$

`gtha` is allowed to be estimated.

© 2023 Cadence Design Systems, Inc.

One other recommendation is that one basic goal of the model is to model the deviation from linearity (which is important for distortion modeling), and to extract model parameters.

Because of local variation (mismatch), it can be difficult to merge data from different devices for model parameter extraction. Therefore extraction from individual devices can be beneficial. Modeling the deviation from linearity for individual devices does both of these.

© 2023 Cadence Design Systems, Inc.

Reference

Component Statements

Instance Parameters

`w=1.0e-06 m`	Design width of resistor body.
`l=1.0e-06 m`	Design length of resistor body.
`wd=0 m`	Dogbone width (total; not per side).
`a1=0` m^2	Area of node n1 partition.
`p1=0 m`	Perimeter of node n1 partition.
`c1=0`	Number of contacts at node n1 terminal.
`a2=0` m^2	Area of node n2 partition.
`p2=0 m`	Perimeter of node n2 partition.
`c2=0`	Number of contacts at node n2 terminal.
`trise=0 degC`	Local temperature delta to ambient (before self-heating).
`sw_noise=1`	Switch for including noise: 0=no and 1=yes.
`sw_et=1`	Switch for self-heating: 0=no and 1=yes.
`sw_mman=0`	Switch for mismatch analysis: 0=no and 1=yes.
`resform1=0`	Use the resistance form for n1 and i1 branch: 0=no and 1=yes.
`resform2=0`	Use the resistance form for n2 and i2 branch: 0=no and 1=yes.
`nsmm_rsh=0`	Number of standard deviations of local variation for rsh.
`nsmm_w=0`	Number of standard deviations of local variation for w.
`nsmm_l=0`	Number of standard deviations of local variation for l.
`m=1`	Number of devices in parallel.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

© 2023 Cadence Design Systems, Inc.

Model Parameters

`version=1`	Model version.
`subversion=0`	Model subversion.
`revision=0`	Model revision.
`level=1003`	Model level.
`type=(-1)`	Resistor type: -1=n-body and +1=p-body.
`scale=1.0`	Scale factor for instance geometries.
`shrink=0 %`	Shrink percentage for instance geometries.
`tmin=(-100) degC`	Minimum ambient temperature.
`tmax=500 degC`	Maximum ambient temperature.
`rthresh=1.0e-03 Ω`	Threshold to switch end resistance to V=I*R form.
`gmin=1.0e-12 S`	Minimum conductance.
`imax=1.0 A`	Current at which to linearize diode currents.
`tnom=27.0 degC`	Nominal (reference) temperature.
`lmin=0 µm`	Minimum allowed drawn length.
`lmax=9.9e09 µm`	Maximum allowed drawn length.
`wmin=0 µm`	Minimum allowed drawn width.
`wmax=9.9e09 µm`	Maximum allowed drawn width.
`jmax=100 A/µm`	Maximum current density.
`vmax=9.9e09 V`	Maximum voltage w.r.t. control node nc.
`tminclip=(-100) degC`	Clip minimum temperature.
`tmaxclip=500 degC`	Clip maximum temperature.
`rsh=100 Ω/sq`	Sheet resistance.
`xw=0 µm`	Width offset (total).
`nwxw=0` μm^2	Narrow width offset correction coefficient.
`wexw=0 µm`	Webbing effect width offset correction coefficient (for dogboned devices).
`fdrw=1.0 µm`	Finite doping width offset reference width.
`fdxwinf=0 µm`	Finite doping width offset width value for wide devices.

© 2023 Cadence Design Systems, Inc.

`xl=0 µm`	Length offset (total).
`xlw=0`	Width dependence of length offset.
`dxlsat=0 µm`	Additional length offset for velocity saturation calculation.
`nst=1.0`	Subthreshold slope parameter.
`ats=0 V`	Saturation smoothing parameter.
`atsl=0 Vµm`	Saturation smoothing parameter 1/l coefficient
`dfinf=0.01 /V^0.5`	Depletion factor for wide/long device.
`dfw=0 µm/V^0.5`	Depletion factor 1/w coefficient.
`dfl=0 µm/V^0.5`	Depletion factor 1/l coefficient.
`dfwl=0` μm^2`/V^0.5`	Depletion factor 1/(w*l) coefficient.
`sw_dfgeo=1`	Switch for depletion factor geometry dependence: 0=drawn and 1=effective.
`dp(dpinf)=2.0 V`	Depletion potential.
`dpl=0 (Vµm)^dple`	Depletion potential l dependence coefficient.
`dple=1.0`	Depletion potential l dependence exponent.
`dpw=0 (Vµm)^dple`	Depletion potential w dependence coefficient.
`dpwe=1.0`	Depletion potential w dependence exponent.
`dpwl=0 (Vµm)^dpwe+dple`	Depletion potential wl dependence coefficient.
`sw_vsatt=0`	Switch for vsat temperature effects: 0=none and 1=link with body resistance.
`sw_accpo=0`	Switch for pinch-off modeling.
`grpo=10^-12`	Minimum body conductance in pinch-off.
`ecrit=4.0 V/µm`	Velocity saturation critical field.
`ecorn=0.4 V/µm`	Velocity saturation corner field.
`du=0.02`	Mobility reduction at ecorn.
`rc=0 Ω`	Resistance per contact.
`rcw=0 Ω µm`	Width adjustment for contact resistance.
`fc=0.9`	Depletion capacitance linearization factor.
`isa=0 A/`μm^2	Diode saturation current per unit area.

© 2023 Cadence Design Systems, Inc.

na=1.0	Ideality factor for isa.
ca=0 F/μm^2	Fixed capacitance per unit area.
cja=0 F/μm^2	Depletion capacitance per unit area.
pa=0.75 V	Built-in potential for cja.
ma=0.33	Grading coefficient for cja.
aja=(-0.5) V	Smoothing parameter for cja.
isp=0 A/µm	Diode saturation current per unit perimeter.
np=1.0	Ideality factor for isp.
cp=0 F/µm	Fixed capacitance per unit perimeter.
cjp=0 F/µm	Depletion capacitance per unit perimeter.
pp=0.75 V	Built-in potential for cjp.
mp=0.33	Grading coefficient for cjp.
ajp=(-0.5) V	Smoothing parameter for cjp.
vbv=0 V	Breakdown voltage.
ibv=1.0e-06 A	Current at breakdown.
nbv=1.0	Ideality factor for breakdown current.
kfn=0	Flicker noise coefficient (unit depends on afn).
afn=2.0	Flicker noise current exponent.
bfn=1.0	Flicker noise 1/f exponent.
sw_fngeo=0	Switch for flicker noise geometry calculation: 0=drawn and 1=effective.
ea=1.12 V	Activation voltage for diode temperature dependence.
xis=3.0	Exponent for diode temperature dependence.
tc1=0/K	Resistance linear TC.
tc2=0/K^2	Resistance quadratic TC.
tc1l=0 µm/K	Resistance linear TC length coefficient.
tc2l=0 µm/K^2	Resistance quadratic TC length coefficient.
tc1w=0 µm/K	Resistance linear TC width coefficient.
tc2w=0 µm/K^2	Resistance quadratic TC width coefficient.

© 2023 Cadence Design Systems, Inc.

`tc1wl=0` $\mu m^2/K$	Resistance linear TC 1/(wl) coefficient
`tc2wl=0` $\mu m^2/K^2$	Resistance quadratic TC 1/(wl) coefficient
`tc1rc=0/K`	Contact resistance linear TC.
`tc2rc=0/K`^{2}	Contact resistance quadratic TC.
`tc1dp=0/K`	Depletion potential linear TC
`tc2dp=0/K`^{2}	Depletion potential quadratic TC
`tc1kfn=0/K`	Flicker noise coefficient linear TC.
`tc1vbv=0/K`	Breakdown voltage linear TC.
`tc2vbv=0/K`^{2}	Breakdown voltage quadratic TC.
`tc1nbv=0/K`	Breakdown ideality factor linear TC.
`tegth=0` ∞	Thermal conductance temperature exponent.
`gth0=1.0e+06 W/K`	Thermal conductance fixed component.
`gthp=0 W/K/`µm	Thermal conductance perimeter component.
`gtha=0 W/K/`μm^2	Thermal conductance area component.
`gthc=0 W/K`	Thermal conductance contact component.
`cth0=0 s W/K`	Thermal capacitance fixed component.
`cthp=0 s W/K/`µm	Thermal capacitance perimeter component.
`ctha=0 s W/K/`μm^2	Thermal capacitance area component.
`cthc=0 s W/K`	Thermal capacitance contact component.
`nsig_rsh=0`	Number of standard deviations of global variation for rsh.
`nsig_w=0`	Number of standard deviations of global variation for w.
`nsig_l=0`	Number of standard deviations of global variation for l.
`sig_rsh=0 %`	Global variation standard deviation for rsh (relative).
`sig_w=0` µm	Global variation standard deviation for w (absolute).
`sig_l=0` µm	Global variation standard deviation for l (absolute).
`smm_rsh=0 %`µm	Local variation standard deviation for rsh (relative).
`smm_w=0` µm`^1.5`	Local variation standard deviation for w (absolute).
`smm_l=0` µm`^1.5`	Local variation standard deviation for l (absolute).

© 2023 Cadence Design Systems, Inc.

`sw_mmgeo=0`	Switch for flicker noise geometry calculation: 0=drawn and 1=effective.
`mr=0`	Resistor mismatch dependence.
`mrl=0`	Resistor mismatch length dependence.
`mrlp=0`	Resistor mismatch length power dependence.
`mrw=0`	Resistor mismatch width dependence.
`mrwp=0`	Resistor mismatch width power dependence.
`mrlw1=0`	Resistor mismatch area 1 dependence.
`mrlw1p=0`	Resistor mismatch area 1 power dependence.
`mrlw2=0`	Resistor mismatch area 2 dependence.
`mrlw2p=0`	Resistor mismatch area 2 power dependence.
`xvsat=0`	Exponent for saturation velocity temperature dependence.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

© 2023 Cadence Design Systems, Inc.

Operating Point Parameters

`v (V)`	Voltage across resistor.
`ibody (A)`	Current through resistor body.
`power (W)`	Dissipated power.
`pwr (W)`	Dissipated power, alias of `power`.
`leff_um (μm)`	Effective electrical length in um.
`weff_um (μm)`	Effective electrical width in um.
`r0 (Ω)`	Zero-bias resistance (per segment).
`r_dc (Ω)`	DC resistance (including bias dependence and m).
`r_ac (Ω)`	AC resistance (including bias dependence and m).
`rth (K/W)`	Thermal resistance.
`cth (s W/K)`	Thermal capacitance.
`dt_et (C)`	Self-heating temperature rise.

© 2023 Cadence Design Systems, Inc.

42

IGBT0 Model (igbt0)

The IGBT0 (Insulated Gate Bipolar Transistor Level 0) model is a simplified IGBT model that is compatible with Cadence PSpice IGBT model. IGBT0 model was introduced to model the application of high voltage and current. The voltage can be up to several thousand volts and the current up to several hundred amperes.

This chapter contains the following information:

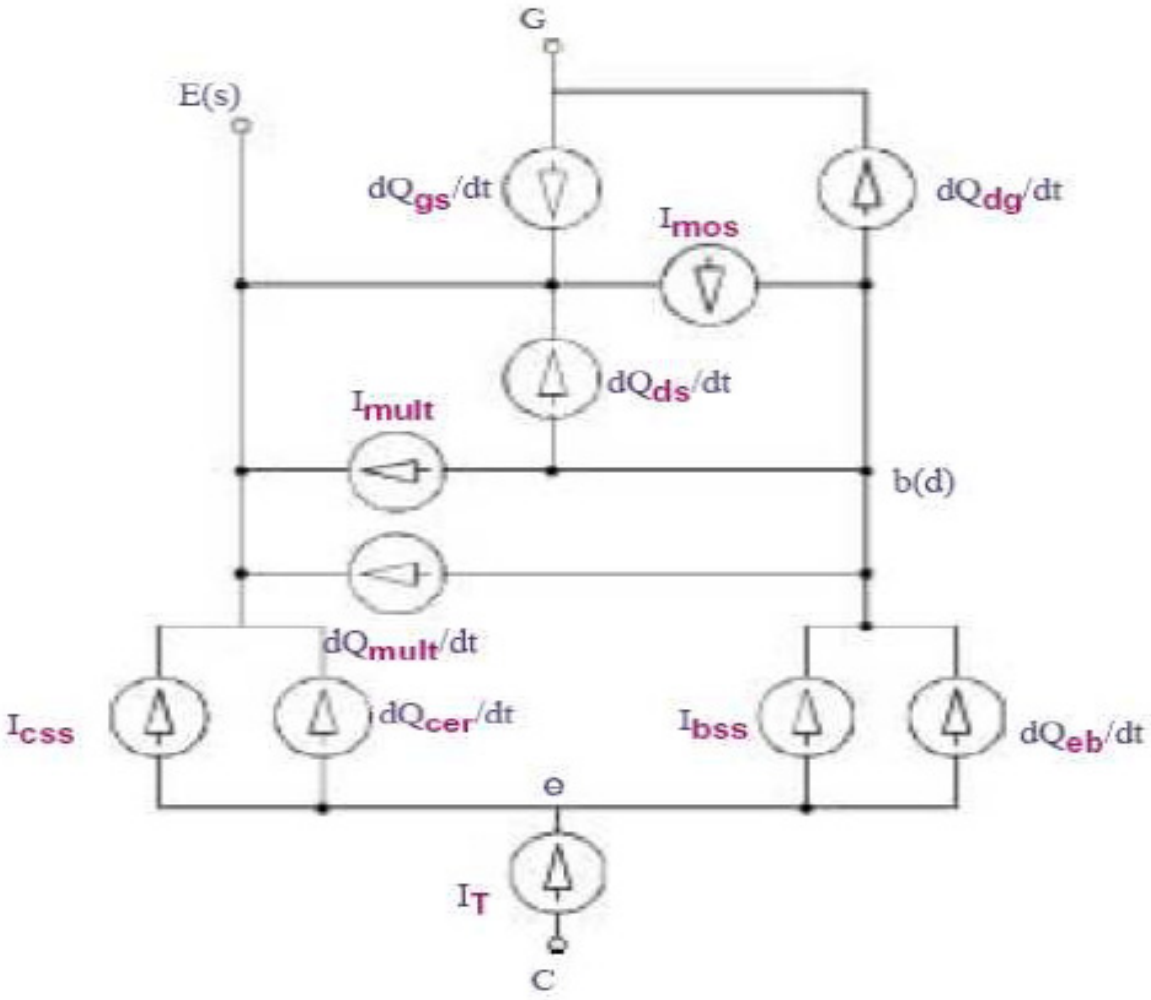
- Model Concepts
- Component Statements
  - Instance Syntax
  - Model Syntax
- Reference
  - Model Equations
  - Instance Parameters
  - Model Parameters
  - Operating Point Parameters

© 2023 Cadence Design Systems, Inc.

Model Concepts

The equivalent circuit for the IGBT is shown below. It is modeled as a thick base BJT driven by MOSFET. Five DC current components and six charge (capacitive) components are included in the model. For the meaning of specific component, refer to the Model Equation part of the model.

As the simplified IGBT model, only the basic characteristics are modeled by IGBT0 model. Combining BJT with MOSFET, p_type IGBT0 devices are hard to modeling and seldom used. Only N-type devices are supported. Different with MOSFET, there's only the leakage current exist when the devices are reversed (Vc < Ve).



© 2023 Cadence Design Systems, Inc.

Related Topics

IGBT0 Model (igbt0)

© 2023 Cadence Design Systems, Inc.

Component Statements

Instance Syntax

IGBT0 instance requires 3 terminals and the number cannot be changed. To specify IGBT0 instance element, the Model Name has to be associated with a IGBT0 model card.

```
InstanceName c g e ModelName parameter=value ...
```

Sample Instance Statement

```
m1 (vcc vgg vee) n_ch area=0.1u kp=0.21 tau=1e-7 agd=1e-8
```

For more instance parameters, refer to Reference.

Model Syntax

The following syntax specifies IGBT0 model:

```
model ModelName igbt0 parameter=value ...
```

The third parameter, "igbt0", is the master to indicate this model card is a IGBT0 model card.

Sample Model Statement

```
model n_ch igbt0 vt=4.5 mun=1.7e3 mup=5e2 cgs=1e-10 nb=3e14 jsne=1e-13
```

For more model parameters, refer to Reference.

Related Topics

IGBT0 Model (igbt0)

© 2023 Cadence Design Systems, Inc.

Reference

Model Equations

Some important model equations are listed as following for your reference:

Equations for DC current

MOSFET channel current

(42-1)

$$\begin{cases} 0 & \text{For } V_{gs} < \mathrm{VT} \\ \dfrac{\mathrm{KF}\cdot\mathrm{KP}\cdot\left((V_{gs}-\mathrm{VT})\cdot V_{ds}-\dfrac{\mathrm{KF}\cdot V_{ds}^{2}}{2}\right)}{1+\mathrm{THETA}\cdot(V_{gs}-\mathrm{VT})} & \text{For } V_{ds} \le (V_{gs}- \\ \dfrac{\mathrm{KP}\cdot(V_{gs}-\mathrm{VT})^{2}}{2\cdot(1+\mathrm{THETA}\cdot(V_{gs}-\mathrm{VT}))} & \text{For } V_{ds} > (V_{gs}- \end{cases}$$

Anode current: current through the resistor Rb

(42-2)

$$I_T = \frac{V_{Ce}}{R_b}$$

© 2023 Cadence Design Systems, Inc.

Steady-state collector current

(42-3)

$$I_{css} = \begin{cases} 0 & \text{For } V_{eb} \le 0 \\ \left(\frac{1}{1+b}\right)\cdot I_T + \left(\frac{b}{1+b}\right)\cdot\left(\frac{4\cdot D_p}{W^2}\right)\cdot Q_{eb} & \text{For } V_{eb} > 0 \end{cases}$$

Steady-state base current

(42-4)

$$I_{bss} = \begin{cases} 0 & \text{For } V_{eb} \le 0 \\ \frac{Q_{eb}}{\mathbf{TAU}} + \left(\frac{Q_{eb}^2}{Q_B}\right)\cdot\left(\frac{4\cdot \mathbf{NB}^2}{n_i^2}\right)\cdot(\mathbf{JSNE}\cdot\mathbf{AREA}) & \text{For } V_{eb} > 0 \end{cases}$$

Avalanche multiplication current

(42-5)

$$I_{mult} = (M-1)\cdot(I_{mos} + I_{css}) + M\cdot I_{gen}$$

Equations for capacitance and charge

Gate Source

(42-6)

$$C_{gs} = \mathrm{CGS} \qquad Q_{gs} = \mathbf{CGS}\cdot V_{gs}$$

© 2023 Cadence Design Systems, Inc.

Drain Source

(42-7)

$$C_{ds} = \frac{(\mathbf{AREA} - \mathbf{AGD}) \cdot \varepsilon_{si}}{W_{dsj}} \qquad Q_{ds} = q \cdot (\mathbf{AREA} - \mathbf{AGD}) \cdot \mathbf{NB} \cdot W_{dsj}$$

Where

(42-8)

$$W_{dsj} = \sqrt{\frac{2 \cdot \varepsilon_{si} \cdot (V_{ds} + 0.6)}{q \cdot \mathbf{NB}}}$$

© 2023 Cadence Design Systems, Inc.

Gate Drain

(42-9)

For $V_{ds} < V_{gs} - \mathbf{VTD}$

$$C_{dg} = \mathrm{COXD} \qquad Q_{dg} = \mathbf{COXD} \cdot V_{dg}$$

For $V_{ds} \geq V_{gs} - \mathbf{VTD}$

$$C_{dg} = \frac{C_{dgj} \cdot \mathbf{COXD}}{C_{dgj} + \mathbf{COXD}}$$

$$Q_{dg} = \frac{q \cdot \mathbf{NB} \cdot \varepsilon_{si} \cdot \mathbf{AGD}^2}{\mathbf{COXD}} \left(\frac{\mathbf{COXD} \cdot W_{dgj}}{\varepsilon_{si} \cdot \mathbf{AGD}} - \log\left(1 + \frac{\mathbf{COXD} \cdot W_{dgj}}{\varepsilon_{si} \cdot \mathbf{AGD}}\right)\right) - \mathbf{COXD} \cdot \mathbf{VTD}$$

where

$$C_{dgj} = \frac{\mathbf{AGD} \cdot \varepsilon_{si}}{W_{dgj}}$$

$$W_{dgj} = \sqrt{\frac{2 \cdot \varepsilon_{si} \cdot (V_{dg} + \mathbf{VTD})}{q \cdot \mathbf{NB}}}$$

Instance Parameters

area (m^2)	Area of the device.
wb (m)	Metallurgical base width.
tau (s)	Ambipolar recombination lifetime.
agd (m^2)	Gate-drain overlap area.
kp (A/V^2)	MOS transconductance.
trise (C)	Device temperature increased.

© 2023 Cadence Design Systems, Inc.

Model Parameters

Default for instance parameters

area=1.0e-5 m^2	Default area of the device.
wb=9.0e-5 m	Default metallurgical base width.
tau=7.1e-6 s	Default ambipolar recombination lifetime.
agd=5.0e-6 m^2	Default gate-drain overlap area.
kp=0.38 A/V^2	Default MOS transconductance.

Basic Device Parameters

vt=4.7 V	Threshold voltage.
kf=1.0	Triode region factor.
theta=0.02 1/V	Transverse field factor.
nb=2.0e14 cm^-3	Base doping.
mun=1.5e3 cm^2/(V*s)	Electron mobility.
mup=4.5e2 cm^2/(V*s)	Hole mobility.
jsne=6.5e-13 A/(cm^2)	Emitter saturation current density.
bvn=4.0	Avalanche multiplication exponent.
bvf=1.0	Avalanche uniformity exponent.
cgs=1.24e-8 F/(cm^2)	Gate-source capacitance per unit area.
coxd=3.5e-8 F/(cm^2)	Gate-drain oxide capacitance per unit area.
vtd=1.0e-3 V	Gate-drain overlap depletion threshold.

Operating Point Parameters

ice (A)	Collector-emitter current.
vce (V)	Collector-emitter voltage.

© 2023 Cadence Design Systems, Inc.

vds (V)	Internal Vds of mosfet.
vge (V)	Gate-emitter voltage.
vdsat (V)	Drain-source saturation voltage.
gm (S)	Common-source transconductance.
ic_bjt (A)	Resistive collector current.
ie (A)	Resistive emitter current.
imult (A)	Avalanche multiplication current.
ib_bjt (A)	Steady-state base current.
imos (A)	MOSFET channel current.
cge (F)	dQg_dVe.
cgg (F)	dQg_dVg.
pwr (W)	Power at operating point.
cdg (F)	dQd_dVg.
cds (F)	dQd_dVs.
qgs (Coul)	Qgs for mosfet.
qds (Coul)	Qds for mosfet.
qdg (Coul)	Qdg for mosfet.
qeb (Coul)	Qeb for bjt.

Related Topics

IGBT0 Model (igbt0)

© 2023 Cadence Design Systems, Inc.

43

Distributed Components

This chapter describes component statements for the following components:

- Microstrip Line (msline)
- Multi-Conductor Transmission Line (mtline)
- Delay Line (delay)
- Four Terminal Relay (relay)
- Linear Two Winding Ideal Transformer (transformer)

© 2023 Cadence Design Systems, Inc.

Microstrip Line (msline)

This is a microstrip line based on the equations of Hammerstad and Jensen. The model contains a thickness correction to the width and frequency dependent permittivity and characteristic impedance. The dispersion equations are those of Kirschning and Jansen.

This device is supported within altergroups.

Instance Syntax

```
Name  t1  b1  t2  b2 msline parameter=value ...
```

Sample Instance Statement

```
tl1 (in 0 out 0) msline l=0.15 w=0.01 h=0.01
```

Instance Parameters

`l=0 m`	Length.
`w (m)`	Width.
`h (m)`	Substrate height.
`t=0 m`	Conductor thickness.
`eps=1`	Substrate permittivity relative to a vacuum.
`m=1`	Multiplicity factor.
`fmax=10e9 Hz`	Maximum signal frequency.

Related Topics

Distributed Components

Multi-Conductor Transmission Line (mtline)

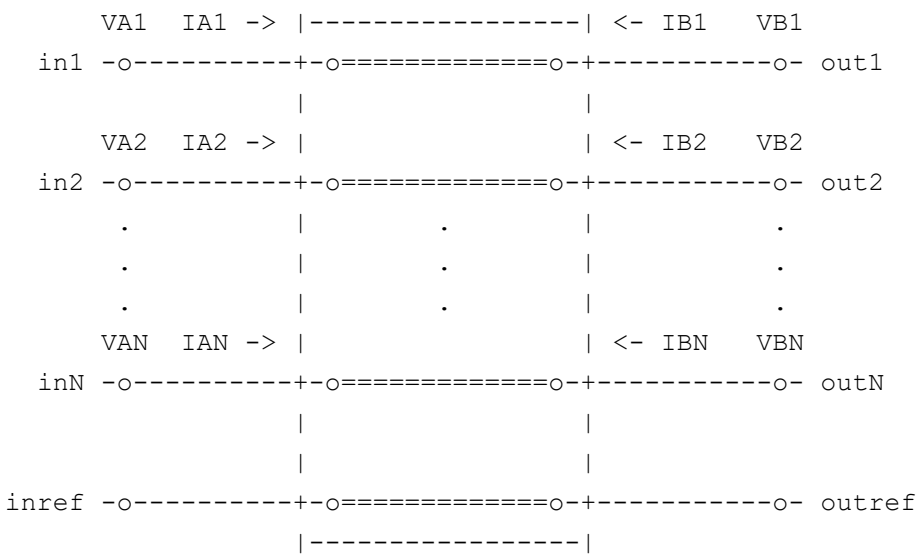
Delay Line (delay)

Four Terminal Relay (relay)

Linear Two Winding Ideal Transformer (transformer)

© 2023 Cadence Design Systems, Inc.

Multi-Conductor Transmission Line (mtline)



A multi-conductor transmission line (MTLINE) is characterized by constant RLGC matrices or frequency-dependent RLGC data. An MTLINE can have as many conductors as there are described in the input. However, there must be at least two conductors with one conductor used as reference to define terminal voltages. The reference conductor can be ground. The order of the conductors is the same as the order of the data in the input.

All of the conductors are assumed to have the same length, and to be uniform along the length.

MTLINE accepts five different types of input: per-unit-length constant RLGC matrices, per-unit-length frequency-dependent RLGC data, 2-D field solver geometry and material property information, S-parameter data, and the old single-conductor TLINE parameters. These inputs are explained below.

All transmission line parameters (other than conductor length) can be provided through an instance line or model line. When a parameter is specified on both the instance and the model lines, the parameter specified on the instance line takes higher priority.

Constant RLGC Matrices

For narrow band applications, transmission line characteristics are often assumed to be constant over the frequency of interest. The input to MTLINE are per-unit-length resistance (R), inductance (L), conductance (G), and capacitance (C) matrices, and they are usually

© 2023 Cadence Design Systems, Inc.

generated by a third-party field solver. Because these matrices are generally symmetric, MTLINE accepts both full matrix description and lower half matrix description.

For example, the following describes the resistance matrix of a four conductor line system:

```
            [ 50 10 1  ]
       R = [ 10 50 10 ] Ohm/meter
            [ 1  10 50 ]
```

The following two model descriptions are equivalent:

```
model line mtline
+ r=[ 50 10 1
+     10 50 10
+     1  10 50 ]
+ ...
model line mtline
+ r=[ 50
+     10 50
+     1  10 50 ]
+ ...
```

Skin Effect and Dielectric Loss

The following equations are used to model skin effect and dielectric loss in addition to the constant RLGC matrices:

If `rskin` matrix is given, then:

```
R(f) = r + sqrt(f) * (1 + j) * rskin
```

If `gdloss` matrix is given, then:

```
G(f) = g + f * gdloss
```


© 2023 Cadence Design Systems, Inc.

Note: This dielectric loss term is noncausal, because it's imaginary part is zero. Using this overly simplified and non-physical version of the dielectric loss model often produces inaccurate results.

Physical dielectric loss model requires you to specify the cut-off frequency `fgdloss` and the onset frequency `fgdloss1`. Dielectric loss equation then becomes:

```
G(f) = g + f * gdloss * 2/pi*j*log((fgdgloss+jf)/(fgdgloss1+jf))
```

Frequency-Dependent RLGC Data

Frequency-dependent RLGC data is described in a data file through a parameter `file`. The frequency axis can be scaled with the `scale` parameter. The frequencies in the data file are then multiplied by `scale` before the simulator uses them. The default scale factor is unity.

An example data file is listed below:

```
: Comments: rlc.dat
FORMAT FREQ:  R1:1  R2:1  R2:2
    L1:1  L2:1  L2:2
    C1:1  C2:1  C2:2
0.001e+9:    4.444  0.000383  4.444
    4.565  0.3545  4.565
    4.565  0.3545  4.565
0.010e+9:    4.447  0.003834  4.447
    4.565  0.3545  4.565
    4.565  0.3545  4.565
0.100e+9:    4.476  0.03834  4.476
    4.565  0.3545  4.565
    4.565  0.3545  4.565
1.000e+9:    4.762  0.3834  4.762
    3.103  0.2357  3.103
    3.103  0.2357  3.103
10.00e+9:    13.96  1.082  13.96
    2.718  0.2058  2.718
    2.718  0.2058  2.718
100.0e+9:   56.88  3.294  56.88
    2.531  0.1866  2.531
    2.531  0.1866  2.531
: end of file rlc.dat
```


© 2023 Cadence Design Systems, Inc.

Note: Lines starting with : are interpreted as comment lines. The data file has a format section and a data section. In addition, both full matrix and lower half matrix descriptions are accepted.

You can mix the constant RLGC parameters with frequency-dependent RLGC data. When a particular parameter (R, L, G or C) is specified in both constant matrix and frequency-dependent data file, the constant matrix is the first choice of input. If only one frequency point is specified in the file, the RLGC data is assumed to be constant over the frequency of interest.

When providing the frequency-dependent RLGC data, one should always try to provide accurate and sufficient data points. There should be enough data points to cover low-frequency characteristics, and there should be enough data points to capture the changing nature in the high-frequency range. A rule of thumb is that the lowest frequency point should be down to 1kHz, and there should be at least 5 points per decade, particularly in the high-frequency range where RLGC data tends to change rapidly.

2-D Field Solver Information

MTLINE directly supports a built-in 2-D field solver. The output of the 2-D field solver is RLGC data. The data can be stored for re-use through the `file` parameter if the global option `mtlinereuse` is set to `no`. If the global option `mtlinereuse` is set to `yes`, the RLGC data can be stored for re-use through a file which is located in the path specified by `mtlinecachedir`. This makes the actual RLGC model generation a one-time cost, provided the field solver input is unchanged.

Line Configuration (linetype)

MTLINE supports four interconnect line configurations: microstrip line, strip line, coplanar waveguide, and substrate lossy line.

Model Type (modeltype)

For each line configuration, you can choose between three model types. In the lossless model, the internal inductance of the conductor is disregarded by setting the frequency value high; 50 GHz for cases without substrate loss and 15 GHz for cases with substrate loss, and ignoring the value of `fmax`. For the narrow band model, the RLGC data is calculated at frequency `fmax` and assumed to be constant over the frequency of interest. The third choice is the wideband model where true frequency dependent RLGC data is calculated over the frequency of interest. For most applications, you should choose the wideband model as it provides the best model accuracy.

© 2023 Cadence Design Systems, Inc.

Ground Plane (numgnd)

For microstrip line, the number of ground planes is fixed to 1, at the bottom of the 2-D interconnect cross section.

For strip line, the number of ground planes is fixed to 2, at both the bottom and top of the 2-D interconnect cross section.

For coplanar waveguide and substrate lossy line, the number of ground planes can be 1 or 2, at the bottom and top of the 2-D interconnect cross section. For coplanar waveguide, you can also specify 0 ground planes because there will be two ground strips added automatically to the cross section. The width, height, thickness, and spacing of these ground strips can be specified in the same way as conductors are specified.

The `gndthickness` parameter can be used to specify the thickness of the ground plane(s), and the `gndsigma` parameter can be used to specify the ground plane conductivity.

Dielectric Layer (numlayer)

Dielectric layers are either stacked above the ground plane (when `numgnd=1`), or between the ground planes (when `numgnd=2`). There can be many dielectric layers.

The thickness of the dielectric layer can be provided through the `layerthickness` parameter, and the relative dielectric constant of the dielectric layer can be provided through the `er` parameter. Both the `layerthickness` and `er` parameters are of vector type to handle different layer geometries and layer properties. When the number of elements in the vector is less than the number of layers, the value of the last element in the vector is applied to all of the remaining layers.

A particular dielectric layer can be lossy, and either the loss tangent parameter (tan = sigma/(w*ep0)) or the loss sigma parameter (sigma = tan*w*ep0) can be used. This is decided through the `dlosstype` parameter and the actual loss value(s) is provided through the `dloss` vector parameter.

Signal Line

The signal line conductivity can be specified using the `linesigma` parameter.

There can be many signal lines. The geometry of the signal line(s) are decided through parameters `linewidth`, `linethickness`, `lineheight`, and `linespace`. The parameter `lineheight` specifies the distance between the signal line and ground plane at the bottom

© 2023 Cadence Design Systems, Inc.

of the 2-D interconnect cross section. The parameter `linespace` specifies the distance between the signal lines; it can be set to a negative value to describe overlapping signal lines.

RLGC Reuse

If the geometry and material property information of the mtline instance is not specified, the `file` parameter must be given. Spectre reads the `file` parameter to reuse the RLGC data directly. If any one of the geometry and material property information of the mtline instance is specified and the global option parameter `mtlinereuse` is set to `yes`, you can calculate the MD5 code by using this information. If the MD5 file exists in the path set by the global option parameter `mtlinecachedir`, Spectre reads the MD5 file directly.

The parameter `mtlinecachedir` can be used to specify the directory where the mtline RLGC data file will be written to or reused from. If an absolute path is not given, the file will be written to the `/home/<`*`username`*`>/.cadence/mmsim/` directory. If the MD5 file is not specified using `mtlinecachedir`, Spectre checks for the existence of the file . If the file does not exist, the RLGC model is generated by the field solver and the output is stored in the directory specified by `mtlinecachedir`. However if the file exists, Spectre checks if the RLGC data stored in the file matches the MTLINE 2-D field solver input. If the data does not match, a new set of RLGC data is generated and the MD5 file is stored in the directory specified by `mtlinecachedir`. Otherwise, the data is re-used from the file. If the `mtlinereuse` option is set to `no`, Spectre stores the RLGC data in the specified file or `%C:t:r_InstanceName.rlgc` file after the simulation.

Stackup-based Input of Cross-section Geometry and Material Properties

The side dielectric always has the thickness of the conductor and cannot be changed. The side dielectric is always the same material on both sides. The field solver cannot handle different materials on the two sides.

The names definition describes the `stackup` from bottom to top. The next dielectric name after the conductor is the side dielectric.

If you want to have side dielectrics in the top layer, add a very thin dielectric layer above the top conductor, which causes the side dielectric to be added automatically. The material must be the same on both sides.

The `stackup` and `layer` parameters can be used to specify the cross-section geometry and material properties for the 2-D field solver. Three extra Spectre primitives: `stackup`, `conductor`, and `dielectric` have been added for this purpose.

© 2023 Cadence Design Systems, Inc.

The `stackup` parameter is used to specify the ID (name) of the stackup instance that contains the cross-section geometry and material properties. The syntax is:

```
stackup=<ID of stackup instance>
```

Example: `stackup=stk1`

`layer=[<vector of layer names >]`. The size of this vector should be equal to the number of signal conductors. If the size of `layer` vector is less than the number of signal conductors, the last value is used.

Example: `layer=["Strip"]`

For more information on `stackup`, `dielectric`, and `conductor` , use

`spectre -h stackup`, `spectre -h conductor`, and `spectre -h` dielectric respectively.

S-Parameter Data File

MTLINE also supports S-parameter data file input describing a transmission line system using the `file` parameter. MTLINE converts the frequency-dependent S-parameter to frequency-dependent RLGC data and stores the results in the file `%C:t:r_InstanceName.rlgc` for reuse in subsequent simulations.

If the `file` parameter corresponds to S-parameter data, MTLINE first checks the existence of the file `%C:t:r_InstanceName.rlgc` to determine if the S-to-RLGC extraction has been performed in a previous simulation.

The S-parameter data file formats supported include Touchstone, Spectre, and Citi.

The physical length of the line must also be specified using the `len` parameter.

The ordering of the S-parameter input file should be in the format of input ports followed by the output ports of the transmission line system, for example, `Pin1, Pin2, Pin3, ..., Pout1, Pout2, Pout3, ...`

Old TLINE Parameters

MTLINE directly supports the old single-conductor TLINE parameters to ease migration, as MTLINE has a more accurate and robust modeling algorithm.

Due to a name conflict, the TLINE parameter `r` has been renamed to `seriesr` in MTLINE, and the TLINE parameter `g` has been renamed to `shuntg` in MTLINE.

© 2023 Cadence Design Systems, Inc.

In addition, the terminal maps between TLINE and MTLINE are different. The following TLINE syntax

```
Name ( t1 b1 t2 b2 ) tline <parameter=value> ...
```

should be mapped to the following MTLINE syntax

```
Name ( t1 t2 b1 b2 ) mtline <parameter=value> ...
```

For a detailed explanation of TLINE parameters, refer to the TLINE help page (`spectre -h tline`).

This device is not supported within altergroup.

Sample Instance Statement

```
x1 (a1 b1 a2 b2 0 0) mtline len=0.01
+ r=[ 0.3
+     0.0 0.3 ]
+ c=[ 0.35p
+    -0.03p 0.35p ]
MTL1 (net01 net02 0 0) mtline len=0.1 linewidth=[ 79u ]
 stackup=stk layer=["Strip"]

stk stackup
 names=["RefBottom" "dielBelow" "Strip" "dielStrip"  "dielAbove" "RefTop" ]
 thickness=[15u 138u 5u 5u 60u 10u]
 type=["Ref" "Diel" "Cond"  "Diel" "Diel" "Ref"]
 material=[cu d34 cu d34 d34 cu]
d34 dielectric type= "const" nd=2 data= [3.4 0]
cu conductor nd=1 data=[ 5.8e7] type="smooth"

MTL2 (a1 b1 a2 b2 0 0) mtline len=0.037  linewidth=[ 101.6u ]
 stackup=stack1 layer=["top" "top"] linespace=[ 203.2u ]
// linespace is the edge to edge distance, *not* between the
// centerlines of the conductors.
stack1 stackup
 type=["Ref" "Diel" "Cond"] thickness=[19.558u 58.42u 30.48u]
 names=["reference"  "dielectric" "top"] material=[copper wd4p1 copper]
wd4p1 dielectric type= "wideband_debye" nd=5
 data= [1e9 4.1 0.01 628318.5307179586 6.283185307179586e12]
// Note: both 'hammerstad' and 'hammerstadt'  work correctly
copper conductor nd=1 data=[ 5.8e7 1u] type="hammerstad"
```


© 2023 Cadence Design Systems, Inc.

Sample Model Statement

model mtmodel mtline

```
+ r=[ 0.3
+     0.0 0.3 ]
+ c=[ 0.35p
+    -0.03p 0.35p ]
```

model mtmodel mtline

```
+ r=[ 0.3 0.0
+     0.0 0.3 ]
+ c=[ 0.35p -0.03p
+    -0.03p  0.35p ]
```

model mtmodel mtline

```
+ c=[ 0.35p
+    -0.03p 0.35p ]
+ file="rl.data" scale=1
```

Instance Syntax

```
Name  in1  out1  in2  [out2] ... ModelName parameter=value ...
Name  in1  out1  in2  [out2] ... mtline parameter=value ...
```

The last two terminals are used as `refin` and `refout` respectively.

Instance Parameters

`len=0.01 m`	Physical length of line.
`m=1`	Multiplicity factor.
`isnoisy=yes`	Should mtline generate noise. Possible values are `yes` and `no`.

© 2023 Cadence Design Systems, Inc.

RLGC data parameters

`r=[...] Ω/m`	Resistance matrix per unit length.
`l=[...] H/m`	Inductance matrix per unit length.
`g=[...] S/m`	Conductor matrix per unit length.
`c=[...] F/m`	Capacitance matrix per unit length.
`rskin=[...] Ω/m |Hz`	Skin effect resistance matrix per unit length.
`gdloss=[...] S/m Hz`	Dielectric loss conductance matrix per unit length.
`fgdloss (Hz)`	Dielectric loss cut-off frequency.
`fgdloss1 (Hz)`	Dielectric loss onset frequency.
`file`	RLGC data file that contains the frequency-dependent RLGC data or S-parameter data file.
`freqscale=1`	Frequency scale factor for frequency-dependent RLGC data and S-parameter data.

2-D Field Solver parameters

`linetype=sublossline`	Transmission line type. Possible values are `microstrip`, `stripline`, `coplanar`, and `sublossline`.
`modeltype=wideband`	Model type. Possible values are `lossless`, `narrowband`, and `wideband`.
`numlayer`	Number of dielectric layers.
`numgnd`	Number of ground planes.
`er=[...]`	Relative dielectric constant.
`layerthickness=[...] m`	Dielectric layer thickness.
`dlosstype=tangent`	Dielectric loss type. The loss value is specified using the `dloss` parameter. Possible values are `sigma` and `tangent`.
`dloss=[...]`	Dielectric layer loss. The loss can be in terms of dielectric conductivity or tangent loss, determined by the `dlosstype` parameter.

© 2023 Cadence Design Systems, Inc.

`linewidth=[...] m`	Signal line width.
`linethickness=[...] m`	Signal line thickness.
`lineheight=[...] m`	Signal line height.
`linespace=[...] m`	Signal line spacing.
`linesigma (S/m)`	Signal line conductivity.
`gndthickness=[...] m`	Ground plane thickness.
`gndsigma (S/m)`	Ground plane conductivity.

© 2023 Cadence Design Systems, Inc.

Rational fitting parameters

`fmax=2.5e10 Hz`	Maximum signal frequency used to determine the relevant range of rational fitting or used in the 2D field solver.

TLINE-related parameters

`z0=50 Ω`	Characteristic impedance of lossless line.
`td (s)`	Time delay of a lossless line in seconds; a measure of the electrical length.
`f (Hz)`	Reference frequency (used in conjunction to the normalized length to specify electrical length of line).
`nl=0.25`	Normalized electrical length in wavelengths at `f` of a lossless line.
`vel=1`	Propagation velocity of the line given as a multiple of `c`, the speed of light in free space. (vel <= 1).

TLINE conductor loss parameters

`corner=0 Hz`	Corner frequency for skin effect; frequency where skin depth equals the conductor's wall thickness.
`dcr=0 Ω/m`	DC series resistance per unit length.
`fc (Hz)`	Conductor loss measurement frequency (use with `r`, `qc`, or `alphac`).
`seriesr=0 Ω/m`	Conductor (series) resistance per unit length at `fc`.
`alphac=0 dB/m`	Conductor loss at `fc` (low loss approximation).
`qc=infinity`	Conductor loss quality factor at `fc` (low loss approximation).

TLINE dielectric loss parameters

`fd (Hz)`	Dielectric loss measurement frequency (use with `qd`).
`shuntg=0 S/m`	Dielectric (shunt) conductance per unit length.
`alphad=0 dB/m`	Dielectric loss (low loss approximation).

© 2023 Cadence Design Systems, Inc.

`qd=infinity`	Dielectric loss quality factor at `fd` (low loss approximation).

Noise parameters

`trise (C)`	Temperature rise from ambient.
`thermalnoise=yes`	Should mtline generate noise. Possible values are `yes` and `no`.
`noisemodel`	Use the internal thermal noise model, or the externally-supplied noise data in the S-parameter data file. The default behavior is to use external data whenever it is available. Possible values are `internal` and `external`.
`formulation=state space`	Recursive convolution can be used instead of state space formulation. Possible values are `statespace` and `recursive`.

Stackup Parameters

`layer=[...]`	Layer name for the signal conductor.
`stackup`	The name of the stackup instance.

Model Syntax

```
model modelName mtline parameter=value ...
```

Model Parameters

This topic lists the model parameters for mtline.

© 2023 Cadence Design Systems, Inc.

RLGC data parameters

`r=[...] Ω/m`	Resistance matrix per unit length.
`l=[...] H/m`	Inductance matrix per unit length.
`g=[...] S/m`	Conductor matrix per unit length.
`c=[...] F/m`	Capacitance matrix per unit length.
`rskin=[...] Ω/m Hz`	Skin effect resistance matrix per unit length.
`gdloss=[...] S/m Hz`	Dielectric loss conductance matrix per unit length.
`fgdloss (Hz)`	Dielectric loss cut-off frequency.
`fgdloss1 (Hz)`	Dielectric loss onset frequency.
`file`	RLGC data file that contains the frequency-dependent RLGC data or S-parameter data file.
`freqscale=1`	Frequency scale factor for frequency-dependent RLGC data and S-parameter data.

2-D Field Solver parameters

`linetype=sublossline`	Transmission line type. Possible values are `microstrip`, `stripline`, `coplanar`, and `sublossline`.
`modeltype=wideband`	Model type. Possible values are `lossless`, `narrowband`, and `wideband`.
`numlayer`	Number of dielectric layers.
`numgnd=1`	Number of ground planes.
`er=[...]`	Relative dielectric constant.
`layerthickness=[...] m`	Dielectric layer thickness.
`dlosstype=tangent`	

© 2023 Cadence Design Systems, Inc.

	Dielectric loss type. The loss value is specified using the `dloss` parameter. Possible values are `sigma` and `tangent`.
`dloss=[...]`	Dielectric layer loss. Loss can be in terms of dielectric conductivity or tangent loss determined by `dlosstype` parameter.
`linewidth=[...] m`	Signal line width.
`linethickness=[...] m`	Signal line thickness.
`lineheight=[...] m`	Signal line height.
`linespace=[...] m`	Signal line spacing.
`linesigma (S/m)`	Signal line conductivity.
`gndthickness=[...] m`	Ground plane thickness.
`gndsigma (S/m)`	Ground plane conductivity.

© 2023 Cadence Design Systems, Inc.

Rational fitting parameters

`fmax=2.5e10 Hz`	Maximum signal frequency used to determine the relevant range of rational fitting used in the 2-D field solver.

TLINE-related parameters

`z0=50 Ω`	Characteristic impedance of lossless line.
`f (Hz)`	Reference frequency (used in conjunction to the normalized length to specify electrical length of line).
`vel=1`	Propagation velocity of the line given as a multiple of `c`, the speed of light in free space. (vel <= 1).

TLINE conductor loss parameters

`corner=0 Hz`	Corner frequency for skin effect; frequency where skin depth equals the conductor's wall thickness.
`dcr=0 Ω/m`	DC series resistance per unit length.
`fc (Hz)`	Conductor loss measurement frequency (use with `r`, `qc`, or `alphac`).
`seriesr=0 Ω/m`	Conductor (series) resistance per unit length at `fc`.
`alphac=0 dB/m`	Conductor loss at `fc` (low loss approximation).
`qc=infinity`	Conductor loss quality factor at `fc` (low loss approximation).

TLINE dielectric loss parameters

`fd (Hz)`	Dielectric loss measurement frequency (use with `qd`).
`shuntg=0 S/m`	Dielectric (shunt) conductance per unit length.
`alphad=0 dB/m`	Dielectric loss (low loss approximation).
`qd=infinity`	Dielectric loss quality factor at `fd` (low loss approximation).

© 2023 Cadence Design Systems, Inc.

Noise parameters

`trise=0 C`	Default temperature rise from ambient.
`thermalnoise=yes`	Should mtline generate noise. Possible values are `yes` and `no`.
`isnoisy=yes`	Thermal noise. Possible values are `yes` and `no`.
`noisemodel`	To use the internal thermal noise model, or the externally supplied noise data in the S-parameter data file. The default behavior is to use external data whenever it is available. Possible values are `internal` and `external`.

Rational Fitting

Spectre uses rational fitting algorithm to build a stable model that approximates the desired transmission line characteristics. Maximum signal frequency `fmax` is used to determine the relevant range of rational fitting. The accuracy of the mtline model is solely dependent on how well the rational approximation is over the frequency range [`fmin`, `fmax`].

When constant RLGC matrices are provided, 1Hz is used as `fmin` and `fmax` defaults to 25GHz. Three times the inverse of rise time in the input signal can be used as a good estimation of `fmax`. When RLGC data file is provided, the lowest frequency point in the data file is used as `fmin`, and the largest frequency point in the data file is used as `fmax`. You should provide sufficient data points to cover both low frequency and high frequency for an accurate, stable model.

Modeling Frequency Dependent Effects

One can model the frequency-dependent RLGC matrices by providing data using the `file` parameter. One should always try to provide accurate and sufficient data to describe the frequency-dependent RLGC matrices.

Related Topics

Distributed Components

© 2023 Cadence Design Systems, Inc.

Delay Line (delay)

Sample Instance Statement

```
dl1(outp outn cntrlp cntrln) delay td=10n gain=1.5
```

Instance Syntax

```
Name  p  n  ps  ns delay parameter=value ...
```

Instance Parameters

`td=0.0 s`	Time delay.
`gain=1`	Gain parameter.
`m=1`	Multiplicity factor.

Operating-Point Parameters

`v (V)`	Output voltage.

Related Topics

Distributed Components

© 2023 Cadence Design Systems, Inc.

Four Terminal Relay (relay)

The four-terminal relay is a voltage controlled relay tied between terminals `t1` and `t2`. The voltage between terminals `ps` and `ns` controls the relay resistance. The relay resistance varies nonlinearly between `ropen` and `rclosed`, the open relay resistance and closed relay resistance, respectively. These resistance values correspond to control voltages of `vt1` and `vt2` respectively. The four parameters, `vt1`, `vt2`, `ropen`, and `rclosed`, can be instance or model parameters.

As an alternative, you can specify the threshold voltage, `vth`, and the transition width, `trans`, rather than specifying `vt1` and `vt2`. These two parameters are then calculated from `vth` and `trans`: vt1=vth, vt2=vth+trans. If all four parameters are specified, `vth` and `trans` override `vt1` and `vt2`. However, the values you specify for 'vt1' and 'vt2' on the instance override any model parameter specifications.

The final model parameter, `hysteresis`, designates a hysteresis with the on voltage shifted from `vth` by an amount `hysteresis` and the off voltage shifted by the same amount in the opposite direction. The direction of shift depends on the sign of `trans` (or the relative magnitudes of `vt1` and `vt2`): if `trans` is positive, the on voltage shifts by `+hysteresis`; if trans is negative (implying that the relay is "normally on"), the on-voltage shifts by `-hysteresis`.

This device is not supported within altergroup.

Operating conductance is calculated from the instance parameters as follows:

When `Vc` lies between `vt1` and `vt2`,

```
G = Gmin + (Gmin - Gmax) * [ 2 * (Vc - vt1)^3
    - 3 * (vt2 - vt1) * (Vc - vt1)^2] / (vt2 - vt1)^3
```

Otherwise, if `vt1` < `vt2`, then

```
G = Gmin    for Vc < vt1 and
G = Gmax    for Vc > vt2.
```

If `vt1` > `vt2`,

```
G = Gmin    for Vc > vt1 and
G = Gmax    for Vc < vt2.
```

where `Gmin = 1 / ropen, Gmax = 1 / rclosed, and Vc = V(ps) - V(ns).`

© 2023 Cadence Design Systems, Inc.

Sample Instance Statement

```
rel1 (1 2 ps ns) my_relay ropen=1G rclosed=2
```

Sample Model Statement

```
model my_relay relay vt1=2.5 vt2=5 ropen=100M rclosed=0.1
```

Instance Syntax

```
Name  1  2  ps  ns ModelName parameter=value ...
Name  1  2  ps  ns relay parameter=value ...
```

Instance Parameters

vt1 (V)	Relay resistance is ropen at this voltage.
vt2=vt1+1.0 V	Relay resistance is rclosed at this voltage.
ropen=∞ Ω	Resistance of a fully open relay.
rclosed=1.0 Ω	Resistance of a fully closed relay.
m=1.0	Multiplicity factor.
region=off	Estimated operating region. Spectre generates output number (0-1) in a rawfile. Possible values are off or on.
isnoisy=no	Determines if the device should generate noise. Possible values are yes and no.

Model Syntax

```
model modelName relay parameter=value ...
```

Model Parameters

vt1 (V)	Relay resistance is ropen at this voltage.
vt2=vt1+1.0 V	Relay resistance is rclosed at this voltage.
ropen=∞ Ω	Resistance of a fully open relay.
rclosed=1.0 Ω	Resistance of a fully closed relay.
hysteresis=0.0 V	Switching Hysteresis.

© 2023 Cadence Design Systems, Inc.

`vth=0.0 V`	Threshold Voltage.
`trans=0.0 V`	Switch Transition Region Width.

Operating-Point Parameters

`region=off`	Estimated operating region. Spectre generates output number (0-1) in a rawfile. Possible values are `off` or `on`.
`res (Ω)`	Relay resistance.

Related Topics

Distributed Components

© 2023 Cadence Design Systems, Inc.

Linear Two Winding Ideal Transformer (transformer)

Winding 1 connects terminals `t1` and `b1`, and winding 2 connects terminals `t2` and `b2`. The number of turns on winding 1 and winding 2 is given by `n1` and `n2`, respectively, where `n2` must not be zero. The absolute number of turns of each winding is not important; only the ratio of `n1` to `n2`. Current through winding 1 is computed.

This device is not supported within altergroup.

An ideal transformer is modeled, so it acts as a transformer at DC. Thus

(43-1)

$$\frac{v_1}{v_2} = \frac{t_1}{t_2} = \frac{i_2}{i_1}$$

To model a physical transformer with L_1 and L_2 as the inductance of the windings and *k* as the coupling coefficient, add an inductor $L_m = k.L_1$ in parallel with winding 1 and inductors $L_{e1} = L_1.(1 - k)$ and $L_{e2} = L_2.(1 - k)$ in series with windings 1 and 2, respectively. The ratio of the turns can be computed, as shown below.

(43-2)

$$\frac{n_1}{n_2} = \sqrt{\frac{L_1}{L_2}}$$

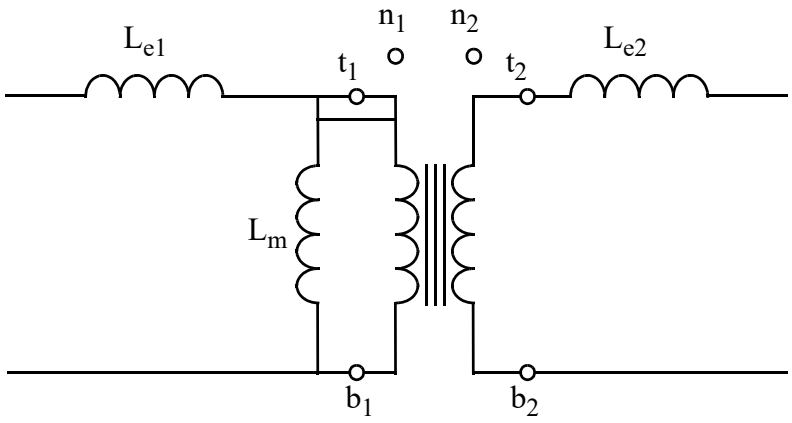
k can be calculated from L_1 (inductance of winding 1 with

(43-3)

$$k = \sqrt{1 - \frac{L_s}{L_1}}$$

(43-4)

© 2023 Cadence Design Systems, Inc.



Instance Syntax

```
Name  t1  b1  t2  b2 transformer parameter=value ...
```

Instance Parameters

`n1=1`	Number of turns on winding 1.
`n2=1`	Number of turns on winding 2.
`m=1`	Multiplicity factor.

Related Topics

Distributed Components

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

44

Other Models

This chapter describes component statements for the following models:

- High-Voltage MOSFET Model (hvmos) on page 2830
- MISN Field Effect Transistor (misnan) on page 2858
- Diffusion Resistor Model (rdiff) on page 2867

© 2023 Cadence Design Systems, Inc.

High-Voltage MOSFET Model (hvmos)

HV (High-Voltage) MOS transistor model is a deep submicron, high-voltage MOSFET model. It is based on the BSIM3v3 version 3.1. Major enhancements include current-crowding effect at high gate bias, asymmetric source-drain structure, mobility reduction, transconductance reduction under high Vgs at saturation region, forward and reverse mode, self-heating, and more flexible gate-dependent output characteristics. HVMOS can be used for high voltage IC design applications such as Flash memory with asymmetric LDD structures, LCD drivers, CCD, E2PROM and LDMOS applications.

Like BSIM3v3, the HVMOS transistor model also allows the binning option to achieve even higher accuracy. The binning equation is given by

P = P0 + Pl / Leff + Pw / Weff + Pp / (Leff * Weff)

Only the P0 parameters are listed. Pl, Pw, and Pp are not shown but can be recognized. The names of Pl, Pw, and Pp are identical to that of P0 but with a prefix of l, w, and p, respectively. HVMOS transistors require that you use a model statement.

This device is supported within altergroups.

Sample Instance Statement

```
m1 (1 2 0 0) hvnmos w=1.5u l=1u ad=2.6p as=2.6p pd=6.6p ps=6.6p nrd=1.54 nrs=1.54
```

Sample Model Statement

```
model hvnmos hvmos vtho=0.53 w0=2.14e-6 nlx=1.8e-7 nch=2.3e18 xj=0.22e-6 k1=0.48
k2=-0.02 drout=1.1 rsh=10 cgso=2.4e-10 cgdo=2.4e-10
```

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

w	(m)	Channel width.
l	(m)	Channel length.
as	(m^2)	Area of source diffusion.
ad	(m^2)	Area of drain diffusion.
ps	(m)	Perimeter of source diffusion.
pd	(m)	Perimeter of drain diffusion.
nrd	(m/m)	Number of squares of drain diffusion.
nrs	(m/m)	Number of squares of source diffusion.
ld	(m)	Length of drain diffusion region.
ls	(m)	Length of source diffusion region.
isnoisy	yes	Should device generate noise.Possible values are no and yes.
m	1	Multiplicity factor (number of MOSFETs in parallel).
region	triode	Estimated operating region. Spectre outputs number (0-3) in a rawfile.Possible values are off, triode, sat and subth.
nqsmod		NQS flag.
trise		Temperature rise from ambient.
dtemp		alias of trise.

Model Definition

```
model modelName hvmos parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Device type parameters

type	n	Transistor type.Possible values are n and p.
hvmosver	2.0	HVMOS Model version selector. The available versions are 1.0, 2.0.

Threshold voltage parameters

vtho	(V)	Threshold voltage at zero body bias for long-channel devices. For enhancement-mode devices, vtho > 0 for n-channel and vtho < 0 for p-channel.
k1	0.5 √V	Body-effect coefficient, default is 0.53 for hvmosver >=2.0 .
k2	-0.0186	Charge-sharing parameter.
k3	80	Narrow width coefficient.
k3b	0 1/V	Narrow width coefficient.
w0	2.5e-6 m	Narrow width coefficient.
nlx	1.74e-7 m	Lateral nonuniform doping coefficient.
gamma1	1.0 √V	Body-effect coefficient near the surface.
gamma2	0 √V	Body-effect coefficient in the bulk.
vbx	-3 V	Threshold voltage transition body voltage.
vbm	-3 V	Maximum applied body voltage.

© 2023 Cadence Design Systems, Inc.

dvt0	2.2	First coefficient of short-channel effects.
dvt1	0.53	Second coefficient of short-channel effects.
dvt2	-0.032 1/V	Body-bias coefficient of short-channel effects.
a0f	1	Forward nonuniform depletion width effect coefficient.
a0r	a0f	Reverse nonuniform depletion width effect coefficient.
b0	0 m	Bulk charge coefficient due to narrow width effect.
b1	0 m	Bulk charge coefficient due to narrow width effect.
a1	0	No-saturation coefficient.
a2	1	No-saturation coefficient.
ags	0 F/m^2 V	Gate-bias dependence of Abulk.
ketaf	-0.047 1/V	Body-bias coefficient for non-uniform depletion width effect.
ketar	ketaf 1/V	Reverse body-bias coefficient for non-uniform depletion width effect.

© 2023 Cadence Design Systems, Inc.

Process parameters

nsub	6e16 cm^{-3}	Substrate doping concentration.
nch	1.7e17 cm^{-3}	Peak channel doping concentration.
xj	0.15e-6 m	Source/drain junction depth.
lint	0 m	Lateral diffusion for one side.
wint	0 m	Width reduction for one side.
ll	0 m	Length dependence of delta L.
lln	1	Length exponent of delta L.
lw	0 m	Width dependence of delta L.
lwn	1	Width exponent of delta L.
lwl	0 m^2	Area dependence of delta L.
lmin	0 m	The minimum channel length for which the model is still valid.
lmax	1 m	The maximum channel length for which the model is still valid.
wl	0 m	Length dependence of delta W.
wln	1	Length exponent of delta W.
ww	0 m	Width dependence of delta W.
wwn	1	Width exponent of delta W.
wwl	0 m^2	Area dependence of delta W.

© 2023 Cadence Design Systems, Inc.

wmin	0 m	The minimum channel width for which the model is still valid.
wmax	1 m	The maximum channel width for which the model is still valid.
dwg	0 m/v	Gate-bias dependence of channel width.
dwb	0 m/√v	Body-bias dependence of channel width.
tox	1.5e-8 m	Gate oxide thickness.
xt	1.55e-7 m	Doping depth.
rd0	0 Ω	Fixed drain resistance.
rs0	0 Ω	Fixed source resistance.
rdw	0 Ω µm	Width dependence of drain resistance.
rsw	0 Ω µm	Width dependence of source resistance.
rdsw	0 Ω µm	Width dependence of drain-source resistance.
prwb	0 1/√v	Body-effect coefficient for Rds.
prwg	0 1/√v	Gate-effect coefficient for Rds.
wr	1	Width offset for parasitic resistance.
binunit	2	Bin parameter unit selector. 1 for microns and 2 for meters.

© 2023 Cadence Design Systems, Inc.

Mobility parameters

mobmod	1	Mobility model selector.
u0f	670 $cm^2/V\ s$	Forward low-field surface mobility at tnom. Default is 250 for PMOS.
u0r	u0f $cm^2/V\ s$	Reverse low-field surface mobility at tnom.
vsatf	8e4 m/s	Forward carrier saturation velocity at tnom.
dvsatf	0 m/s	Forward gate-bias dependence of saturation velocity.
dvsatbf	0 m/s	Forward body-bias dependence of saturation velocity.
vsatr	vsatf m/s	Reverse carrier saturation velocity at tnom.
dvsatr	dvsatf m/s	Reverse gate-bias dependence of saturation velocity.
dvsatbr	dvsatbf m/s	Reverse body-bias dependence of saturation velocity.
uaf	2.25e-9 m/v	Forward first-order mobility reduction coefficient.
ubf	5.87e-19 m^2/v^2	Forward second-order mobility reduction coefficient.
ucf	-4.65e-11 m/v^2	Forward body-bias dependence of mobility. Default is -0.046 and unit is 1/V for mobmod=3.
udf	0 m/v^2	Forward source-resistance dependence of mobility.
uar	uaf m/v	Reverse first-order mobility reduction coefficient.

© 2023 Cadence Design Systems, Inc.

ubr	ubf m^2/v^2	Reverse second-order mobility reduction coefficient.
ucr	ucf m/v^2	Reverse body-bias dependence of mobility.
udr	udf m/v^2	Reverse source-resistance dependence of mobility.

© 2023 Cadence Design Systems, Inc.

Output resistance parameters

drout	0.56	DIBL effect on output resistance coefficient.
pclmf	1.3	Forward channel length modulation coefficient.
pclmr	pclmf	Reverse channel length modulation coefficient.
pdiblc1f	0.39	Forward first coefficient of drain-induced barrier lowering.
pdiblc1r	pdiblc1f	Reverse first coefficient of drain-induced barrier lowering.
pdiblc2f	8.6e-3	Forward second coefficient of drain-induced barrier lowering.
pdiblc2r	pdiblc2f	Reverse second coefficient of drain-induced barrier lowering.
pdiblcbf	0 1/V	Body-effect coefficient for DIBL.
pdiblcbr	pdiblcbf 1/V	Reverse body-effect coefficient for DIBL.
pscbe1f	4.24e8 V/m	First coefficient of substrate current body effect.
pscbe2f	1e-5 m/v	Second coefficient of substrate current body effect.
pscbeg	0 V/m	Third coefficient of substrate current body effect.
pscbe1r	pscbe1f V/m	Reverse first coefficient of substrate current body effect.
pscbe2r	pscbe2f m/v	Reverse second coefficient of substrate current body effect.
pvag	0	Gate-dependence of Early voltage.

© 2023 Cadence Design Systems, Inc.

`pclmgf`	`0`	Forward gate dependence of Vaclm.
`pclmgr`	`pclmgf`	Reverse gate dependence of Vaclm.
`pclmbf`	`0`	Forward body dependence of Vaclm.
`pclmbr`	`pclmbf`	Reverse body dependence of Vaclm.
`pdiblgf`	`0`	Forward gate dependence of Vadibl.
`pdiblgr`	`pdiblgf`	Reverse gate dependence of Vadibl.
`delta`	`0.01 V`	Effective drain voltage smoothing parameter.

© 2023 Cadence Design Systems, Inc.

Subthreshold parameters

cdsc	2.4e-4 F/m^2	Source/drain and channel coupling capacitance.
cdscb	0 F/m^2 V	Body-bias dependence of cdsc.
cdscd	0 F/m^2 V	Drain-bias dependence of cdsc.
nfactor	1	Subthreshold swing coefficient.
cit	0 F	Interface trap parameter for subthreshold swing.
voff	-0.08 V	Threshold voltage offset.
dsub	drout	DIBL effect in subthreshold region.
eta0f	0.08	DIBL coefficient subthreshold region.
etabf	-0.07 1/V	Body-bias dependence of et0.
eta0r	eta0f	Reverse DIBL coefficient subthreshold region.
etabr	etabf 1/V	Body-bias dependence of eta0r.

Substrate current parameters

alpha0	0 m/v	Substrate current impact ionization coefficient.
alpha1	0 1/V	substrate current model parameter.
beta0	30 1/V	Substrate current impact ionization exponent.

© 2023 Cadence Design Systems, Inc.

Parasitic resistance parameters

`rsh`	`0` Ω`/sqr`	Drain diffusion sheet resistance.
`rshs`	`0` Ω`/sqr`	Source diffusion sheet resistance.
`rs`	`0` Ω	Source resistance.
`rd`	`0` Ω	Drain resistance.
`lgcs`	`0 m`	Gate-to-contact length of source side.
`lgcd`	`0 m`	Gate-to-contact length of drain side.
`rsc`	`0` Ω	Source contact resistance.
`rdc`	`0` Ω	Drain contact resistance.
`rss`	`0` Ω `m`	Scalable source resistance.
`rdd`	`0` Ω `m`	Scalable drain resistance.
`sc`	`infinity m`	Spacing between contacts.
`ldif`	`0 m`	Lateral diffusion beyond the gate.
`hdif`	`0 m`	Length of heavily doped diffusion .
`minr`	`0.1` Ω	Minimum source/drain resistance.

Junction diode model parameters

`js`	`(A/m`^{2}`)`	Bulk junction reverse saturation current density.
`jsw`	`0 A/m`	Sidewall junction reverse saturation current density.

© 2023 Cadence Design Systems, Inc.

is	1e-14 A	Bulk junction reverse saturation current.
n	1	Junction emission coefficient.
nj	1	alias of n.
dskip	yes	Use simple piece-wise linear model for diode currents below 0.1*iabstol.Possible values are no and yes.
imelt	`imaxA'	Explosion current, default is 0.1 for hvmosver >=2.0.
ijth	`imax` A	Junction threshold current.
jmelt	`jmaxA/m'^{2}	Explosion current density.
jtss	0 A/m^2	Source bottom trap-assisted saturation current density.
jtsd	jtss A/m^2	Drain bottom trap-assisted saturation current density.
jtssws	0.0 A/m	Source isolation-edge sidewall trap-assisted saturation current density.
jtsswd	jtssws A/m	Drain isolation-edge sidewall trap-assisted saturation current density.
jtsswgs	0.0 A/m	Source Gate-edge isolation-edge sidewall trap-assisted saturation current density.
jtsswgd	jtsswgs A/m	Drain isolation-edge sidewall trap-assisted saturation current density.
njts	20.0	Non-ideality factor for jtss.
njtssw	20.0	Non-ideality factor for jtssws.

© 2023 Cadence Design Systems, Inc.

njtsswg	20.0	Non-ideality factor for jtsswgs.
njtsd	njts	Non-ideality factor for jtsd .
njtsswd	njtssw	Non-ideality factor for jtsswd.
njtsswgd	njtsswg	Non-ideality factor for jtsswgd .
xtss	0.02	Power dependence of jtss on temperature.
xtsd	xtss	Power dependence of jtsd on temperature.
xtssws	0.02	Power dependence of jtssws on temperature.
xtsswd	xtssws	Power dependence of jtsswd on temperature.
xtsswgs	0.02	Power dependence of jtsswgs on temperature.
xtsswgd	xtsswgs	Power dependence of jtsswgd on temperature.
vtss	10.0 V	Source bottom trap-assisted voltage dependent parameter.
vtsd	vtss V	Drain bottom trap-assisted voltage dependent parameter.
vtssws	10.0 V	Source STI sidewall trap-assisted voltage dependent parameter.
vtsswd	vtssws V	Drain STI sidewall trap-assisted voltage dependent parameter.
vtsswgs	10.0 V	Source gate-edge sidewall trap-assisted voltage dependent parameter.
vtsswgd	vtsswgs V	Drain gate-edge sidewall trap-assisted voltage dependent parameter.
tnjts	0.0	Temperature coefficient for njts.

© 2023 Cadence Design Systems, Inc.

`tnjtssw`	`0.0`	Temperature coefficient for njtssw.
`tnjtsswg`	`0.0`	Temperature coefficient for njtsswg.
`tnjtsd`	`tnjts`	Temperature coefficient for njtsd.
`tnjtsswd`	`tnjtsssw`	Temperature coefficient for njtsswd.
`tnjtsswgd`	`tnjtsswg`	Temperature coefficient for njtsswgd.

© 2023 Cadence Design Systems, Inc.

Overlap capacitance parameters

cgso	(F/m)	Gate-source overlap capacitance.
cgdo	(F/m)	Gate-drain overlap capacitance.
cgbo	(F/m)	Gate-bulk overlap capacitance.
meto	0 m	Metal overlap in fringing field.
cgsl	0 F/m	Gate-source overlap capacitance in LDD region.
cgdl	0 F/m	Gate-drain overlap capacitance in LDD region.
ckappa	0.6	Overlap capacitance fitting parameter.
deltaacc	0.1 V	Capacitance smoothing parameter.

Junction capacitance model parameters

cbs	0 F	Bulk-source zero-bias junction capacitance.
cbd	0 F	Bulk-drain zero-bias junction capacitance.
cj	5e-4 F/ m^2	Zero-bias junction bottom capacitance density.
mj	1/2	Bulk junction bottom grading coefficient.
pb	0.8 V	Bulk junction built-in potential, default is 1.0 for hvmosver >=2.0.
fc	0.5	Forward-bias depletion capacitance threshold.
cjsw	5e-10 F/ m	Zero-bias junction sidewall capacitance density.

© 2023 Cadence Design Systems, Inc.

`mjsw`	`1/3`	Bulk junction sidewall grading coefficient.
`pbsw`	`0.8 V`	Side-wall junction built-in potential, default is 1.0 for hvmosver >=2.0.
`fcsw`	`0.5`	Side-wall forward-bias depletion capacitance threshold.
`cjswg`	`cjsw F/m`	Zero-bias gate-side junction capacitance density.
`mjswg`	`mjsw`	Gate-side junction grading coefficient.
`pbswg`	`pbsw V`	Gate-side junction built-in potential.

© 2023 Cadence Design Systems, Inc.

Charge model selection parameters

capmod	2	Intrinsic charge model.
nqsmod	0	Non-quasi static model selector. Set to 1 to turn on nqs.
dwc	wint m	Delta W for capacitance model.
dlc	lint m	Delta L for capacitance model.
clc	1e-7 m	Intrinsic capacitance fitting parameter.
cle	0.6	Intrinsic capacitance fitting parameter.
cf	(F/m)	Fringe capacitance parameter.
a0cvf	a0f	A0 for C-V calculation.
a0cvr	a0r	Reverse A0 for C-V calculation.
qgvd0f	1	Cgd fitting parameter.
qgvd0r	qgvd0f	Reverse Cgd fitting parameter.
elm	5	Elmore constant of the channel.
vfbcv	-1	Flat-band voltage for capmod=0.
acde	0.5 1/V	Exponential coefficient for finite charge thickness.
moin	15 1/V	Coefficient for Vgs dependent surface potential.
xpart	0	Drain/source channel charge partition in saturation for BSIM charge model, use 0.0 for 40/60, 0.5 for 50/50, or 1.0 for 0/100.

© 2023 Cadence Design Systems, Inc.

Default instance parameters

w	5e-6 m	Default channel width.
l	5e-6 m	Default channel length.
as	0 m^2	Default area of source diffusion.
ad	0 m^2	Default area of drain diffusion.
ps	0 m	Default perimeter of source diffusion.
pd	0 m	Default perimeter of drain diffusion.
nrd	0 m/m	Default number of squares of drain diffusion.
nrs	0 m/m	Default number of squares of source diffusion.
xw	0 m	Width variation due to masking and etching.
xl	0 m	Length variation due to masking and etching.

Temperature effects parameters

tnom	(C)	Parameters measurement temperature. Default set by `options`.
trise	0 C	Temperature rise from ambient.
tlev	0	DC temperature selector.
tlevc	0	AC temperature selector.
eg	1.12452 V	Energy band gap.

© 2023 Cadence Design Systems, Inc.

gap1	7.02e-4 V/C	Band gap temperature coefficient.
gap2	1108 C	Band gap temperature offset.
kt1	-0.11 V	Temperature coefficient for threshold voltage.
kt11	0 v m	Temperature coefficient for threshold voltage.
kt2	0.022	Temperature coefficient for threshold voltage.
atf	3.3e4 m/s	Temperature coefficient for vsatf.
atr	atf m/s	Temperature coefficient for vsatr.
at1f	0 m/s	Temperature coefficient for dvsatf.
at1r	at1f m/s	Temperature coefficient for dvsatr.
ua1f	4.31e-9 m/v	Temperature coefficient for uaf.
ub1f	-7.61e-18 m^2/v^2	Temperature coefficient for ubf.
uc1f	-5.5e-11 m/v^2	Temperature coefficient for ucf. Default is -0.056 for mobmod=3.
ud1f	0 m/v^2	Temperature coefficient for udf.
ua1r	ua1f m/v	Temperature coefficient for uar.
ub1r	ub1f m^2/v^2	Temperature coefficient for ubr.
uc1r	uc1f m/v^2	Temperature coefficient for ucr.

© 2023 Cadence Design Systems, Inc.

ud1r	0 m/v^2	Temperature coefficient for udr.
rth	0 Ω	Self-heating thermal resistance.
rthg	0 1/V	Gate-effect coefficient for Rth.
rthb	0 $1/\sqrt{v}$	Body-effect coefficient for Rth.
prt	0 Ω	Temperature coefficient for Rds.
trs	0 1/C	Temperature parameter for source resistance.
trd	0 1/C	Temperature parameter for drain resistance.
ute	-1.5	Mobility temperature exponent.
xti	3	Saturation current temperature exponent.
ptc	0 V/C	Surface potential temperature coefficient.
tcv	0 V/C	Threshold voltage temperature coefficient.
pta	0 V/C	Junction potential temperature coefficient.
tpb	0 V/C	Junction potential temperature coefficient.
ptp	0 V/C	Sidewall junction potential temperature coefficient.
tpbsw	0 V/C	Sidewall junction potential temperature coefficient.
cta	0 1/C	Junction capacitance temperature coefficient.
tcj	0 1/C	Junction capacitance temperature coefficient.
ctp	0 1/C	Sidewall junction capacitance temperature coefficient.

© 2023 Cadence Design Systems, Inc.

`tcjsw`	`0 1/C`	Sidewall junction capacitance temperature coefficient.
`tcjswg`	`0 1/C`	Temperature coefficient for `cjswg`.
`tpbswg`	`0 V/C`	Temperature coefficient for `pbswg`.

© 2023 Cadence Design Systems, Inc.

Noise model parameters

noimod	1	Noise model selector.
kf	0	Flicker (1/f) noise coefficient.
em	4.1e7 V/m	Maximum electric field.
af	1	Flicker (1/f) noise exponent.
ef	1	Flicker (1/f) noise frequency exponent.
noia	1e20	Oxide trap density coefficient. Default is 9.9e18 for pmos.
noib	5e4	Oxide trap density coefficient. Default is 2.4e3 for pmos.
noic	-1.4e-8	Oxide trap density coefficient. Default is 1.4e-8 for pmos. Default is -1.4-12 for hvmosver >=2.0.

Operating region warning control parameters

alarm	none	Forbidden operating region.Possible values are none, off, triode, sat, subth and rev.
imax	1 A	Maximum allowable current, default is 0.1 for hvmosver >=2.0 .
jmax	1e8 A/m^2	Maximum allowable current density.
bvj	infinity V	Junction reverse breakdown voltage.
vbox	1e9*tox V	Oxide breakdown voltage.

© 2023 Cadence Design Systems, Inc.

vds_max	infinity V	Maximum allowed voltage cross source and drain.
vgd_max	infinity V	Maximum allowed voltage cross gate and drain.
vgs_max	infinity V	Maximum allowed voltage cross gate and source/bulk.
vbd_max	infinity V	Maximum allowed voltage cross source/drain and bulk.
vbs_max	vbd_max V	Maximum allowed voltage cross source and bulk.
vgb_max	infinity V	Maximum allowed voltage cross gate and bulk.
vgsr_max	vgs_max V	Maximum allowed reverse voltage cross gate and source.
vgdr_max	vgd_max V	Maximum allowed reverse voltage cross gate and drain.
vgbr_max	vgb_max V	Maximum allowed reverse voltage cross gate and bulk.
vbsr_max	vbs_max V	Maximum allowed reverse voltage cross bulk and source.
vbdr_max	vbd_max V	Maximum allowed reverse voltage cross bulk and drain.
noid	2.0e14	flicker noise subthreshold-above threshold transition coefficient.

The imax (jmax) parameter is used to aid convergence and prevent numerical overflow. The junction characteristics of the FET are accurately modeled for current (density) up to imax (jmax). For currents (density) above imax (jmax), the junction is modeled as a linear resistor and a warning is printed.

© 2023 Cadence Design Systems, Inc.

Output Parameters

weff	(m)	Effective channel width.
leff	(m)	Effective channel length.
rseff	(Ω)	Effective source resistance.
rdeff	(Ω)	Effective drain resistance.

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

a0cvf M-192
a0cvr M-193
a0f M-17
a0r M-18
a1 M-21
a2 M-22
acde M-198
ad I-4
ad M-204
af M-256
ags M-23
elm M-196
em M-255
eta0f M-104
eta0r M-106
etabf M-105
etabr M-107
fc M-177
fcsw M-181
gamma1 M-10
gamma2 M-11
gap1 M-216
noia M-258
noib M-259
noic M-260
noid M-277
noimod M-253
nqsmod I-14
nqsmod M-186
nrd I-7
nrd M-207
nrs I-8
nrs M-208
tpb M-244
tpbsw M-246
tpbswg M-252
trd M-238
trise I-15
trise M-212
trs M-237
type M-1
type OP-1
u0f M-59
u0r M-60

© 2023 Cadence Design Systems, Inc.

alarm M-261
alpha0 M-108
alpha1 M-109
as I-3
as M-203
at1f M-223
at1r M-224
atf M-221
atr M-222
b0 M-19
b1 M-20
beta0 M-110
betaeff OP-13
binunit M-57
bvj M-264
capmod M-185
cbb OP-32
cbd M-173
cbd OP-30
cbg OP-29
cbs M-172
gap2 M-217
gds OP-11
gm OP-10
gmbs OP-12
gmoverid OP-37
hdif M-123
hvmosver M-2
ibd OP-40
ibs OP-39
ibulk OP-35
id OP-34
ids OP-4
ijth M-132
imax M-262
imelt M-131
is M-127
isnoisy I-11
isub OP-38
jmax M-263
jmelt M-133
js M-125
nsub M-26
pb M-176
pbsw M-180
pbswg M-184
pclmbf M-92
pclmbr M-93
pclmf M-76
pclmgf M-90
pclmgr M-91
pclmr M-77
pd I-6
pd M-206
pdiblc1f M-78
pdiblc1r M-79
pdiblc2f M-80
pdiblc2r M-81
pdiblcbf M-82
pdiblcbr M-83
pdiblgf M-94
pdiblgr M-95
prt M-236
ua1f M-225
ua1r M-229
uaf M-67
uar M-71
ub1f M-226
ub1r M-230
ubf M-68
ubr M-72
uc1f M-227
uc1r M-231
ucf M-69
ucr M-73
ud1f M-228
ud1r M-232
udf M-70
udr M-74
ute M-239
vbd_max M-269
vbdr_max M-276
vbm M-13
vbox M-265

© 2023 Cadence Design Systems, Inc.

cbs OP-31
cdb OP-24
cdd OP-22
cdg OP-21
cds OP-23
cdsc M-97
cdscb M-98
cdscd M-99
cf M-191
cgb OP-20
cgbo M-166
cgc OP-18
cgd OP-17
cgdl M-169
cgdo M-165
cgg OP-16
cgs OP-19
cgsl M-168
cgso M-164
cit M-101
cj M-174
jsw M-126
jtsd M-135
jtss M-134
jtsswd M-137
jtsswgd M-139
jtsswgs M-138
jtssws M-136
k1 M-4
k2 M-5
k3 M-6
k3b M-7
ketaf M-24
ketar M-25
kf M-254
kt1 M-218
kt1l M-219
kt2 M-220
l I-2
l M-202
ld I-9
ldif M-122
prwb M-54
prwg M-55
ps I-5
ps M-205
pscbe1f M-84
pscbe1r M-87
pscbe2f M-85
pscbe2r M-88
pscbeg M-86
pta M-243
ptc M-241
ptp M-245
pvag M-89
pwr OP-36
qgvd0f M-194
qgvd0r M-195
rd M-114
rd0 M-49
rdc M-118
rdd M-120
rdeff O-4
vbs OP-7
vbs_max M-270
vbsr_max M-275
vbx M-12
vds OP-6
vds_max M-266
vdsat OP-9
vfbcv M-197
vgb_max M-271
vgbr_max M-274
vgd_max M-267
vgdr_max M-273
vgs OP-5
vgs_max M-268
vgsr_max M-272
voff M-102
vsatf M-61
vsatr M-64
vth OP-8
vtho M-3
vtsd M-153

© 2023 Cadence Design Systems, Inc.

cjd OP-14
cjs OP-15
cjsw M-178
cjswg M-182
ckappa M-170
clc M-189
cle M-190
csb OP-28
csd OP-26
csg OP-25
css OP-27
cta M-247
ctp M-249
delta M-96
deltaacc M-171
dlc M-188
drout M-75
dskip M-130
dsub M-103
dtemp I-16
dvsatbf M-63
leff O-2
lgcd M-116
lgcs M-115
lint M-29
ll M-31
lln M-32
lmax M-37
lmin M-36
ls I-10
lw M-33
lwl M-35
lwn M-34
m I-12
meff OP-41
meto M-167
minr M-124
mj M-175
mjsw M-179
mjswg M-183
mobmod M-58
moin M-199
rdsw M-53
rdw M-51
region I-13
region OP-2
reversed OP-3
ron OP-33
rs M-113
rs0 M-50
rsc M-117
rseff O-3
rsh M-111
rshs M-112
rss M-119
rsw M-52
rth M-233
rthb M-235
rthg M-234
sc M-121
tcj M-248
tcjsw M-250
tcjswg M-251
vtss M-152
vtsswd M-155
vtsswgd M-157
vtsswgs M-156
vtssws M-154
w I-1
w M-201
w0 M-8
weff O-1
wint M-30
wl M-38
wln M-39
wmax M-44
wmin M-43
wr M-56
ww M-40
wwl M-42
wwn M-41
xj M-28
xl M-210
xpart M-200

© 2023 Cadence Design Systems, Inc.

dvsatbr M-66
dvsatf M-62
dvsatr M-65
dvt0 M-14
dvt1 M-15
dvt2 M-16
dwb M-46
dwc M-187
dwg M-45
ef M-257
eg M-215
n M-128
nch M-27
nfactor M-100
nj M-129
njts M-140
njtsd M-143
njtssw M-141
njtsswd M-144
njtsswg M-142
njtsswgd M-145
nlx M-9
tcv M-242
tlev M-213
tlevc M-214
tnjts M-158
tnjtsd M-161
tnjtssw M-159
tnjtsswd M-162
tnjtsswg M-160
tnjtsswgd M-163
tnom M-211
tox M-47
xt M-48
xti M-240
xtsd M-147
xtss M-146
xtsswd M-149
xtsswgd M-151
xtsswgs M-150
xtssws M-148
xw M-209

MISN Field Effect Transistor (misnan)

Cadence plans to stop supporting this model and recommends that it no longer be used.

The MISN model is formulated in terms of solutions for the boundary surface potentials of the channel and has the inherent property of continuous modeling. It is an inhouse MOSFET model of NORTEL. The MISN model requires a model statement.

This device is not supported within altergroup.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so

Sample Instance Statement:

mn1 (1 2 0 0) nch w=1.5u l=1u ad=2.6p as=2.6p pd=6.6p ps=6.6p

Sample Model Statement:

© 2023 Cadence Design Systems, Inc.

model nch misnan type=n cox=4.4e-6 dop=2e17 phi=-0.43 xj=0.23 scrat=1.4 mu=400 rws=250 is=0.98e-13 cjgo=2e-13 noimdl=1

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

1	`w=1e-5 m`	Channel width.
2	`l=3e-6 m`	Channel length.
3	`as=3e-11` m^2	Area of source diffusion.
4	`ad=3e-11` m^2	Area of drain diffusion.
5	`ps=2.6e-5 m`	Perimeter of source diffusion.
6	`pd=2.6e-5 m`	Perimeter of drain diffusion.
7	`m=1`	Multiplicity factor (number of MOSFETs in parallel).
8	`region=triode`	Estimated DC operating region, used as a convergence aid. Possible values are `off`, `triode`, `sat`, or `subthresh`.

Model Definition

```
model modelName misnan parameter=value ...
```

Model Parameters

Intrinsic MOS parameters

1	`type=n`	Transistor gender. Possible values are `n` or `p`.
2	`cox=4.309e-7` F/cm^2	Gate oxide cap per unit area.
3	`dop=1.665e17` cm^{-3}	

© 2023 Cadence Design Systems, Inc.

		Substrate doping. Default = 2.58e17 for pmos.
4	`phi=-0.55 V`	Gate Fermi potential.
5	`qss=-5.078e-8 Coul/cm`^{2}	Effective gate oxide charge per unit area. Default = 1.05e-8 for pmos.
6	`dopldd=3.2e17 cm`$^{-3}$	LDD region doping concentration. Default = 3.2e19 for pmos.

Geometry parameters

7	`lvar=0 µm`	Gate length correction.
8	`wvar=0 µm`	Gate width correction.
9	`dls=0.0273 µm`	Sideway diffusion length of source region. Default = 0.037 for pmos.
10	`dld=0.0273 µm`	Sideway diffusion length of drain region. Default = 0.037 for pmos.
11	`dl=0.07 µm`	Sideways diffusion length of S/D regions. Default = 0.04 for pmos.
12	`dw=0.032 µm`	Electrical channel width correction. Default = 0.018 for pmos.

Threshold voltage parameters

13	`xj=0.24 µm`	Source/drain-to-substrate junction depth. Default = 0.31 for pmos.
14	`scrat=1.5`	Short channel threshold voltage ratio. Default = 0.7 for pmos.
15	`scind=1.45`	Short channel threshold voltage index. Default = 1.42 for pmos.
16	`ncrat=0.17`	Narrow channel threshold voltage ratio. Default = 0.095 for pmos.

© 2023 Cadence Design Systems, Inc.

17	`athp=7.5`	Factor controlling peak magnitude effect. Default = 3.5 for pmos.
18	`athl=2e4 1/cm`	Factor controlling channel length dependence effect. Default = 4e4 for pmos.
19	`athb=-1.7e-3`	Factor controlling substrate bias dependence effect. Default = -6e-3.

Mobility parameters

20	`mu=577 cm`^{2}`/V s`	Low-field carrier mobility. Default = 120 for pmos.
21	`mutxp=1.72`	Temperature coefficient for the carrier mobility. Default = 1.01 for pmos.
22	`kg=1.4e-7 cm/V`	Gate field factor. Default = 1.685e-7.
23	`v0=3.21e7 cm/s`	Scattering limited velocity. Default = 2.45e7.
24	`v0txp=-6.3`	Temp coefficient for scattering limited velocity. Default = -5 for pmos.
25	`find=1.25`	Field mobility index factor. Default = 1.9 for pmos.
26	`gfc=9.1e-10`	Gate voltage dependence of enhanced gate-field scattering. Default = 1.05e-10 for pmos.
27	`gfcm=3e-5`	Drain voltage dependence of enhanced gate-field scattering. Default = 2.3e-3 for pmos.
28	`gfmb=1.45e-3`	Factor controlling substrate bias dependence of enhanced gate-field scattering. Default 3.3e-3 for pmos.
29	`csf=1.06e-11`	Drain voltage dependence of coulomb scattering. Default = 1.35e-12 for pmos.
30	`csfb=1.61e-3`	Body voltage dependence of coulomb scattering. Default = 8.5e-3 for pmos.

Saturation parameters

31	`dprat=15`	Drain region/channel doping ration. Default = 2 for pmos.

© 2023 Cadence Design Systems, Inc.

32	satpr=0.2	Saturation region shaping factor. Default = 1.0 for pmos.
33	sbdr=0.3535534	Primary parameter controlling the onset of saturation.
34	sadr=5	Secondary parameter controlling the onset of saturation.

Capacitance parameters

35	sccf=0.25	Inner fringing factor for the N+ S/D.

Extrinsic parameters

36	rws=480 Ω μm	Source series resistance. Default = 1180 for pmos.
37	rwd=480 Ω μm	Drain series resistance. Default = 1180 for pmos.
38	rsd=-1 Ω μm	Drain/source series resistance. Negative value for asymmetrical devices.
39	rgsh=0 Ω μm	Gate series resistance.
40	wtgf=0.28 μm	Width of transition from gate to field oxide under poly.
41	cpts=5.7e-9 F/cm^2	Poly-to-substrate capacitance per unit area.
42	cgfrs=1e-12 F/cm	Gate-source overlap fringing field capacitance.
43	cgfrd=1e-12 F/cm	Gate-drain overlap fringing field capacitance.
44	cgfr=1.36e-12 F/cm	Gate overlap fringing field capacitance.

Junction parameters

45	is=1.02e-12 A/cm^2	Sat current per unit area of S/D region-injection component. Default = 9.21e-13 for pmos.

© 2023 Cadence Design Systems, Inc.

46	`isg=1e-20 A/cm`	Sat current per unit length of gate oxide periphery-injection component. Default = 1.17e-20.
47	`isf=1e-20 A/cm`	Sat current per unit length of field oxide periphery-injection component. Default = 1.17e-20.
48	`ig=1.31e-10 A/cm`^{2}	Sat current per unit area of S/D region-generation component. Default = 8.27e-10.
49	`igg=6.99e-14 A/cm`	Sat current per unit length of gate oxide periphery-generation/recombination component. Default = 6.47e-14.
50	`igf=6.99e-14 A/cm`	Sat current per unit length of field oxide periphery-generation/recombination component. Default = 6.47e-14.
51	`cjo=9.39e-8 F/cm`^{2}	Zero bias junction capacitance per unit area. Default = 1.273e-7 for pmos.
52	`ena=0.387`	Junction capacitance coefficient for the area component. Default = 0.472 for pmos.
53	`cjgo=2.085e-12 F/cm`	Zero bias junction cap per unit length of gate oxide periphery. Default = 1.864e-12 for pmos.
54	`eng=0.322`	Junction cap coefficient for gate oxide periphery component. Default = 0.334 for pmos.
55	`cjfo=3.037e-12 F/cm`	Zero bias junction cap per unit length of field oxide periphery. Default = 3.077e-12 for pmos.
56	`enf=0.322`	Junction cap coefficient for field oxide periphery component. Default = 0.334 for pmos.

Noise parameters

57	`noimdl=1`	Noise model selector.
58	`nt=1.6e10 cm`$^{-2}$	Surface trap density. Default = 4e9 for pmos.

© 2023 Cadence Design Systems, Inc.

59	`nttx=-4`	Surface trap density temperature coefficient.
60	`fidx=0.85`	Flicker noise frequency coefficient.
61	`beta=1`	Thermal noise proportional constant.
62	`sgma=3e-16`	Capture cross section. Default = 3e-15 for pmos.
63	`xtau=1e-8`	1/E depth.
64	`wbar=1`	Barrier height for tunneling. Default = 4 for pmos.
65	`dept=3e-7`	Depth of trap distribution.

Operating-Point Parameters

1	`vgs (V)`	Gate-source voltage.
2	`vds (V)`	Drain-source voltage.
3	`vbs (V)`	Bulk-source voltage.
4	`id (A)`	Drain current.
5	`vth (V)`	Threshold voltage.
6	`vdsat (V)`	Drain-source saturation voltage.
7	`gm (S)`	Common-source transconductance.
8	`gd (S)`	Common-source output conductance.
9	`gs (S)`	Body-transconductance.
10	`gmb (S)`	Body transconductance.
11	`gjs (S)`	Drain-bulk junction conductance.
12	`ibs (A)`	Drain-bulk junction current.
13	`gjd (S)`	Source-bulk junction conductance.
14	`ibd (A)`	Source-bulk junction current.
15	`qgg (Coul)`	Gate charge.
16	`qss (Coul)`	Source charge.
17	`qdd (Coul)`	Drain charge.
18	`qbb (Coul)`	Bulk charge.
19	`cgg (F)`	Cgg.

© 2023 Cadence Design Systems, Inc.

20	cgs (F)	Cgs.
21	cgd (F)	Cgd.
22	cgb (F)	Cgb.
23	csg (F)	Csg.
24	css (F)	Css.
25	csd (F)	Csd.
26	csb (F)	Csb.
27	cdg (F)	Cdg.
28	cds (F)	Cds.
29	cdd (F)	Cdd.
30	cdb (F)	Cdb.
31	cbg (F)	Cbg.
32	cbs (F)	Cbs.
33	cbd (F)	Cbd.
34	cbb (F)	Cbb.

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

ad I-4
as I-3
athb M-19
athl M-18
athp M-17
csd OP-25
csf M-29
csfb M-30
csg OP-23
css OP-24
ibd OP-14
ibs OP-12
id OP-4
ig M-48
igf M-50
region I-8
rgsh M-39
rsd M-38
rwd M-37
rws M-36

© 2023 Cadence Design Systems, Inc.

beta M-61
cbb OP-34
cbd OP-33
cbg OP-31
cbs OP-32
cdb OP-30
cdd OP-29
cdg OP-27
cds OP-28
cgb OP-22
cgd OP-21
cgfr M-44
cgfrd M-43
cgfrs M-42
cgg OP-19
cgs OP-20
cjfo M-55
cjgo M-53
cjo M-51
cox M-2
cpts M-41
dept M-65
dl M-11
dld M-10
dls M-9
dop M-3
dopldd M-6
dprat M-31
dw M-12
ena M-52
enf M-56
eng M-54
fidx M-60
find M-25
gd OP-8
gfc M-26
gfcm M-27
gfmb M-28
gjd OP-13
gjs OP-11
gm OP-7
gmb OP-10
igg M-49
is M-45
isf M-47
isg M-46
kg M-22
l I-2
lvar M-7
m I-7
mu M-20
mutxp M-21
ncrat M-16
noimdl M-57
nt M-58
nttx M-59
pd I-6
phi M-4
ps I-5
qbb OP-18
qdd OP-17
qgg OP-15
qss M-5
sadr M-34
satpr M-32
sbdr M-33
sccf M-35
scind M-15
scrat M-14
sgma M-62
type M-1
v0 M-23
v0txp M-24
vbs OP-3
vds OP-2
vdsat OP-6
vgs OP-1
vth OP-5
w I-1
wbar M-64
wtgf M-40
wvar M-8
xj M-13
xtau M-63

© 2023 Cadence Design Systems, Inc.

```
csb  OP-26          gs   OP-9           qss  OP-16
```

Diffusion Resistor Model (rdiff)

The rdiff model is a diffusion resistor model, which accurately models the temperature, applied bias and back-bias dependencies of NWell, N+, and P+ resistors. It is described in the paper MODEL FOR DIFFUSION RESISTORS (NWell, N+, P+) USED IN CMOS IC DESIGNS by M.J.B.Bolt, FASELEC Process Development Group, PDG-93029, Modified 3rd May 1995.

Some extensions to that description are applied:

Appropriate model and instance parameter default values are used.

No clipping of parameters is performed. Parameter values are checked for validity. If invalid parameter values occur, the job is aborted with an error message.

For exact inverse behavior of the model in case of Vh less than Vl, the setting of Vbl=abs(Vb-Vl) is replaced by Vbl=min(abs(Vb-Vh),abs(Vb-Vl)). Additionally, the direction of Ih is inverted in this case.

Note: In noise analysis, rdiff instances will not generate any contribution, since there are no noise sources included in the rdiff model.

(c) Philips Electronics N.V. 1993, 1995

This device is supported within altergroups.

This device is dynamically loaded from the shared object /<install_dir>/tools.lnx86/cmi/lib/5.0/libphilips_sh.so

Sample Instance Statement

```
r2 (1 2 0) rdsn l=9u w=2u nb=0 m=1
```

Sample Model Statement

```
model rdsn rdiff level=1 tr=27 dta=0 rshr=2.5e3 wtol=0.22u rint=3.5u swvp=13.4u
power=2 tcr1=1.5e-3 tcr2=1e-5 vpr=40
```


© 2023 Cadence Design Systems, Inc.

Instance Definition

```
Name  h  l  [b] ModelName parameter=value ...
```

Instance Parameters

1	`l=1.0 scale m`	Drawn length of resistor. Must be greater than zero. Scale set by option scale.
2	`w=1.0 scale m`	Drawn width of resistor. Must be greater than zero. Scale set by option scale.
3	`nb=0.0`	Number of bends in the resistor. Must be greater or equal zero.
4	`m=1.0`	Multiplicity factor. Must be greater than zero.

Model Definition

```
model modelName rdiff parameter=value ...
```

Model Parameters

1	`level=1.0`	`Level` of this model. Must be 1.
2	`tr (C)`	Reference temperature. Default set by option `tnom`.
3	`tref (C)`	Alias of `tr`. Default set by option `tnom`.
4	`tnom (C)`	Alias of `tr`. Default set by option `tnom`.
5	`dta=0 K`	Temperature offset of the device.
6	`trise=0 K`	Alias of dta.
7	`rshr=1.0e+3 Ω/sqr`	Sheet resistance at reference temperature. Must be greater than zero.
8	`wtol=0.0 m`	Offset between the drawn and effective resistor width.
9	`tcr1=0.0 1/K`	Linear temperature coefficient of the resistor.
10	`tcr2=0.0` $1/K^2$	Quadratic temperature coefficient of the resistor.
11	`vpr=100.0 V`	Reference Pinch-off voltage.
12	`swvp=0.0 V/m`	Coefficient of the width dependence of `vp`.

© 2023 Cadence Design Systems, Inc.

13	`power=1.5`	Voltage exponent. Must be greater than zero.
14	`vdr=1.0 V`	Diffusion voltage at reference temperature.
15	`rint=0.0 Ω m`	Interface resistance at reference temperature.
16	`tcrint1=0.0 1/K`	Linear temperature coefficient of the interface resistor.

Output Parameters

1	`vd (V)`	Diffusion voltage. Must be greater than zero.
2	`rsh (Ω/sqr)`	Sheet resistance. Must be greater than zero.
3	`vp (V)`	Pinch-off voltage. Must be greater than zero.
4	`r0 (Ω)`	Zero bias resistance. Must be greater than zero.

Operating-Point Parameters

1	`vhl (V)`	Absolute value of the applied bias across the resistor.
2	`vbl (V)`	Absolute value of the back-bias across the resistor.
3	`ih (A)`	DC current into the resistor.
4	`r (Ω)`	Actual resistance value.
5	`pwr (W)`	Power.

Parameter Index

In the following index, `I` refers to instance parameters, `M` refers to the model parameters section, `O` refers to the output parameters section, and `OP` refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of `M-35` means the 35th model parameter.

dta	M-5	r	OP-4	tcrint1	M-16	vhl	OP-1
ih	OP-3	r0	O-4	tnom	M-4	vp	O-3

© 2023 Cadence Design Systems, Inc.

l I-1
level M-1
m I-4
nb I-3
power M-13
pwr OP-5
rint M-15
rsh O-2
rshr M-7
swvp M-12
tcr1 M-9
tcr2 M-10
tr M-2
tref M-3
trise M-6
vbl OP-2
vd O-1
vdr M-14
vpr M-11
w I-2
wtol M-8

© 2023 Cadence Design Systems, Inc.

45

BSIM-CMG

This chapter contains the following information about the BSIM-CMG model:

- Model Overview on page 2873
- TMI Support on page 2873
- OMI Support on page 2874
- BSIM-CMG Model Equations on page 2875
  - Bias Independent Calculations on page 2875
  - Terminal Voltages on page 2878
  - Short Channel Effects on page 2879
  - Surface Potential Calculation on page 2880
  - Drain Saturation Voltage on page 2880
  - Average Potential and Charge on page 2883
  - Quantum Mechanical Effects on page 2884
  - Mobility Degradation and Series Resistance on page 2886
  - Lateral Non-uniform Doping Model on page 2887
  - Body Effect Model on page 2887
  - Output Conductance on page 2887
  - Velocity Saturation on page 2888
  - Drain Current Model on page 2889
  - Intrinsic Capacitance Model on page 2889
  - Parasitic resistances and capacitance models on page 2891
  - Impact Ionization and GIDL/GISL Model on page 2898

© 2023 Cadence Design Systems, Inc.

- Gate Tunneling Current on page 2900
- Non Quasi-static Models on page 2901
- Generation-recombination Component on page 2903
- Junction Current and Capacitances on page 2904
- Self-heating Model on page 2904
- Noise Models on page 2904

- Model Version Update on page 2906
  - Version 105.02 Update on page 2906
  - Version 105.03 update on page 2906
  - Version 105.031 update on page 2907
  - Version 105.04 update on page 2908
  - Version 106.0.0 update on page 2909
  - Version 106.1.0 update on page 2910
  - Version 107.0.0 update on page 2911
  - Version 108.0.0 update on page 2912
  - Version 110.0.0 update on page 2912
- Component tatements on page 2915

© 2023 Cadence Design Systems, Inc.

Model Overview

BSIM-CMG is a SPICE compact model for modeling the electrical characteristics of common gate MG structures, developed by UC Berkeley.

Physical surface potential-based formulations are derived for both intrinsic and extrinsic models with finite body doping. The surface potentials at the source and drain ends are solved analytically with poly-depletion and quantum mechanical effects. The effect of finite body doping is captured through a perturbation approach. The analytic surface potential solution agrees with 2-D device simulation results well. If the channel doping concentration is low enough to be neglected, computational efficiency can be further improved by setting `COREMOD = 1`.

All the important MG transistor behaviors are captured by this model. Volume inversion is included in the solution of the Poisson's equation, hence the subsequent I-V formulation automatically captures the volume inversion effect. Analysis of the electrostatic potential in the body of MG MOSFETs provided the model equation for the short channel effects (SCE). The extra electrostatic control from the end-gates (top/bottom gates) (triple or quadruple-gate) is also captured in the short channel model.

Users can specify the MG structure of interest via a geometry mode selector (`GEOMOD`, `DG = 0`, `TG = 1`, `QG = 2`, `CG = 3`). Hybrid-surface-orientation mobility, corner-induced effective width reduction, and end-channel-enhanced electrostatic control are considered to address the physics of tri-gate (TG) and quadruple-gate (QG) devices.

BSIM-CMG provides the flexibility to model devices with novel materials. This includes parameters for non-silicon channel devices and High-K/ Metal-gate stack.

Other important effects, such as, mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, gate tunneling current, gate-induced-drain-leakage, temperature effects, channel thermal noise, flicker noise, noise associated with device parasitics, and parasitic capacitance, are also incorporated in the model.

BSIM-CMG has been verified with industrial experimental data. The model is continuous and symmetric at `Vds = 0`. This physics-based model is scalable and predictive over a wide range of device parameters.

TMI Support

Starting with the MMSIM 14.1 release, support for the TMI model has been added in the BSIM-CMG model. TMI is a modeling application programming interface (API) that supports extensions of standard compact models.

© 2023 Cadence Design Systems, Inc.

TMI provides an alternative approach to support model equations for advanced technologies in addition to adding more macro models. It provides flexibility as macro model and good simulation efficiency as a built-in standard model at the same time.

To use the TMI for the BSIM-CMG model, you need to correctly set the TMI options and parameters. For more information on TMI options and parameters, refer to the TMI documentation.

OMI Support

Starting with the SPECTRE 19.1 ISR8 release, support for the OMI model has been added in the BSIM-CMG model. OMI (Open Model Interface) is CMC standard modeling application programming interface (API) that supports extensions of standard compact models.

OMI provides an alternative approach to support model equations for advanced technologies in addition to adding more macro models. It provides flexibility as a macro model and good simulation efficiency as a built-in standard model at the same time.

To use the OMI for the BSIM-CMG model, you need to correctly set the OMI options and parameters. For more information on OMI options and parameters, refer to the OMI documentation.

© 2023 Cadence Design Systems, Inc.

BSIM-CMG Model Equations

Bias Independent Calculations

Physical constants

Physical quantities in BSIM-CMG are in M.K.S units unless specified otherwise.

$$q = 1.6 \times 10^{-19}$$

$$\varepsilon_0 = 8.8542 \times 10^{-12}$$

$$h = 1.05457 \times 10^{-34}$$

$$m_e = 9.11 \times 10^{-31}$$

$$\varepsilon_{sub} = EPSRSUB \cdot \varepsilon_0$$

$$\varepsilon_{ox} = EPSROX \cdot \varepsilon_0$$

$$C_{ox} = \frac{3.9 \cdot \varepsilon_0}{EOT}$$

$$C_{si} = \frac{\varepsilon_{sub}}{TFIN}$$

$$\varepsilon_{ratio} = \frac{EPSRSUB}{3.9}$$

© 2023 Cadence Design Systems, Inc.

Effective Channel Width, Channel Length and Fin Number

$$\Delta L = LINT + \frac{LL}{(L + XL)^{LLN}}$$

$$\Delta LCV = DLC + \frac{LLC}{(L + XL)^{LLN}}$$

$$L_{eff} = L + XL + -2\Delta L$$

$$L_{eff,\,CV} = L + XL + -2\Delta LCV$$

If BULKMOD=1 and CAPMOD=1 then

$$L_{eff,\,CV,\,acc} = L_{eff,\,CV} - DLCACC$$

If GEOMOD=0 then

$$W_{eff0} = 2 \cdot HFIN - DELTAW$$

$$W_{eff,\,CV0} = 2 \cdot HFIN - DELTAWCV$$

If GEOMOD=1 then

$$W_{eff0} = 2 \cdot HFIN + FECH \cdot TFIN - DELTAW$$

$$W_{eff,\,CV0} = 2 \cdot HFIN + FECH \cdot TFIN - DELTAWCV$$

If GEOMOD=2 then

$$W_{eff0} = 2 \cdot HFIN + 2 \cdot FECH \cdot TFIN - DELTAW$$

$$W_{eff,\,CV0} = 2 \cdot HFIN + 2 \cdot FECH \cdot TFIN - DELTAWCV$$

© 2023 Cadence Design Systems, Inc.

If GEOMOD=3 then

$$R = \frac{D}{2}$$

$$W_{eff0} = \pi \cdot D - DELTAW$$

$$W_{eff,\,CV0} = \pi \cdot D - DELTAWCV$$

$$NFINtotal = NFIN \times NF$$

Quantum Mechanical Effects

The following bias-independent calculations are for the threshold voltage shift and bias dependence of inversion charge centroid due to quantum mechanical confinement.

If GEOMOD=0 then

$$MTcen = 1 + AQMTCEN \cdot \exp\left(-\frac{TFIN}{BQMTCEN}\right)$$

$$T_{cen0} = TFIN \cdot MTcen$$

If GEOMOD=1 then

$$MTcen = 1 + AQMTCEN \cdot \exp\left(-\frac{min(HFIN, TFIN)}{BQMTCEN}\right)$$

$$T_{cen0} = min(HFIN, TFIN) \cdot MTcen$$

If GEOMOD=2 then

$$MTcen = 1 + AQMTCEN \cdot \exp\left(-\frac{min(HFIN, TFIN)}{BQMTCEN}\right)$$

$$T_{cen0} = min(HFIN, TFIN) \cdot MTcen$$

© 2023 Cadence Design Systems, Inc.

If GEOMOD=3 then

$$MTcen = 1 + AQMTCEN \cdot \exp\left(-\frac{R}{BQMTCEN}\right)$$

$$T_{cen0} = R \cdot MTcen$$

Binning Calculations

For given L and NFIN, each model parameter $PARAM_i$ is calculated as a function of PARAM, a length dependent term, LPARAM, a number of fin per finger(NFIN) dependent term, NPARAM, product L x NFIN term, and PPARAM:

$$PARAM_i = PARAM + \frac{1.0e^{-6}}{L_{eff} + DLBIN} \cdot LPARAM + \frac{1.0}{NFIN} \cdot NPARAM + \frac{1.0e^{-6}}{(L_{eff} + DLBIN) \cdot NFIN} \cdot PPARAM$$

Terminal Voltages

Terminal Voltages and V_{dsx} Calculation

$$V_{gs} = V_g - V_s$$

$$V_{gd} = V_g - V_d$$

$$V_{gb} = V_g - V_b$$

$$V_{ds} = V_d - V_s$$

$$V_{dsx} = \sqrt{v_{ds}^2 + 0.01} - 0.1$$

© 2023 Cadence Design Systems, Inc.

Short Channel Effects

Weighting Function for Forward and Reverse Mode

$$T0 = \tanh(0.6*\mathrm{q}*V_{ds}/kT)$$

$$Wf = 0.5 + 0.5T0$$

$$Wr = 0.5 - 0.5T0$$

Asymmetric Parameters

If `ASYMMOD=1` then

$$CDSCDa = CDSCDi*\mathrm{Wf} + CDSCDRi*\mathrm{Wr}$$

$$ETAa = ETA0i*\mathrm{Wf} + ETA0Ri*\mathrm{Wr}$$

$$PDIBL1a = PDIBL1i*\mathrm{Wf} + PDIBL1Ri*\mathrm{Wr}$$

$$PTWGa = PTWG(T)*\mathrm{Wf} + PTWGR(T)*\mathrm{Wr}$$

$$VSAT1a = VSAT1(T)*\mathrm{Wf} + VSAT1R(T)*\mathrm{Wr}$$

$$RSDRa = RSDR(T)*\mathrm{Wf} + RSDRR(T)*\mathrm{Wr}$$

$$RDDRa = RDDR(T)*\mathrm{Wf} + RDDRR(T)*\mathrm{Wr}$$

Else

All above `PARAMa=PARAM` and reverse mode parameter `PAPAMR` are ignored.

© 2023 Cadence Design Systems, Inc.

Vt Roll-off, DIBL, and Subthreshold Slope Degradation

$$\Delta V_{th,\,SCE} = -\frac{0.5 \cdot DVT0_i}{\cosh\left(DVT1_i \cdot \frac{Leff}{\lambda}\right) - 1} \cdot (V_{bi} - \Psi_{st})$$

$$\Delta V_{th,\,DIBL} = \left(\frac{-0.5 \cdot ETA0}{\cosh\left(\frac{DSUB \times L_{eff}}{\lambda}\right) - 1} \cdot V_{dsx}\right) + \frac{DVTP0 \times V_{dsx}^{DVTP1}}{\left(1 + DVTP2\left(\cosh\left(\frac{DSUB \times L_{eff}}{\lambda}\right) - 2\right)\right)}$$

$$V_{th,\,RSCE} = K1RSCE_i \cdot \left[\sqrt{1 + \frac{LPE0_i}{Leff}} - 1\right] \cdot \sqrt{\Psi_{st}}$$

$$\Delta V_{th,\,all} = \Delta V_{th,\,SCE} + \Delta V_{th,\,DIBL} + \Delta V_{th,\,RSCE} + \Delta V_{th,\,temp}$$

$$V_{gsfb} = V_{gs} - \Delta q\Phi - \Delta V_{th,\,all} - DVTHSHIFT$$

Surface Potential Calculation

Surface potentials at the source and drain ends are derived from the Poisson's equation with a perturbation method and computed using the Householder's cubic iteration method. Perturbation allows accurate modeling of finite body doping.

When the body is lightly-doped, a simplified surface potential algorithm can be activated by setting `COREMOD=1` to enhance computational efficiency.

Drain Saturation Voltage

Electric Field Calculations

Electric Field is in MV/cm

© 2023 Cadence Design Systems, Inc.

If GEOMOD is not equal to 3 then

$$E_{effs} = 10^{-8} \cdot \left(\frac{q_{bs} + \eta \cdot q_{is}}{\varepsilon_{ratio} \cdot EOT} \right)$$

Drain Saturation Voltage (V_{dsat}) Calculations

$$D_{mobs} = \begin{cases} 1 + UA(T) \cdot (E_{effs})^{EU} + \dfrac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_{is}}{q_{im,\,th}} \right) \right)^{UCS(T)}} & \textbf{BULKMOD=0} \\ 1 + (UA(T) + UC(T) \cdot V_{eseff}) \cdot (E_{effs})^{EU} + \dfrac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_{is}}{q_{im,\,th}} \right) \right)^{UCS(T)}} & \textbf{BULKMOD=1} \end{cases}$$

$$D_{mobs} = \frac{D_{mobs}}{U0MULT}$$

If RDSMOD=0 then

$$R_{ds,\,s} = frac1(W_{eff0}(\mu m))^{WR_i} \cdot \left(RDSWMIN(T) + \frac{RDSW(T)}{1 + PRWG_i \cdot q_{is}} \right)$$

© 2023 Cadence Design Systems, Inc.

If RDSMOD=1 then

$$R_{ds,\,s} = 0$$

$$E_{sat} = \frac{2 \cdot VSAT(T)}{\mu o(T) / D_{mobs}}$$

$$E_{satL} = E_{sat} \cdot L_{eff}$$

If $R_{ds,s}$=0 then

$$V_{dsat} = \frac{E_{satL} \cdot KSATIV_i \cdot \left(V_{gsfbeff} - \Psi_s + 2\frac{kT}{q} \right)}{E_{satL} + KSATIV_i \cdot \left(V_{gsfbeff} - \Psi_s + 2\frac{kT}{q} \right)}$$

Else

$$WVC_{ox} = W_{eff0} \cdot V_{SAT}(T) \cdot C_{ox}$$

© 2023 Cadence Design Systems, Inc.

$$T_a = 2 \cdot WVC_{ox} \cdot R_{ds,s}$$

$$T_b = KSATIV_i \cdot (V_{gsfbeff} - \varphi_s + 2kT/q) \cdot (1 + 3 \cdot WVC_{ox} \cdot R_{ds,s}) + E_{satL}$$

$$T_c = KSATIV_i \cdot (V_{gsfbeff} - \varphi_s + 2kT/q) \cdot (E_{satL} + T_a \cdot KSATIV_i \cdot (V_{gsfbeff} - \varphi_s + 2kT/q))$$

$$V_{dsat} = \frac{\left(T_b - \sqrt{T_b^{\,2} - 2T_aT_c}\right)}{T_a}$$

$$V_{dseff} = \frac{Vds}{\left(1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{MEXP(T)}\right)^{1/MEXP(T)}}$$

Average Potential and Charge

$$\Delta\Psi = \Psi_d - \Psi_s$$

$$q_{ba} = q_{bs}$$

If GEOMOD is not equal to 3 then

If $NGATE_i$>0 then

$$T_{polyd} = \sqrt{1 + \frac{V_{gsfbeff} - \Psi_d}{V_{poly0}}} - 1$$

$$V_{polyd} = V_{poly0} \cdot T^2_{polyd}$$

else

© 2023 Cadence Design Systems, Inc.

V_{polyd}=0

$$q_{id} = \begin{cases} V_{gsfbeff} - \Psi_d - q_{bm} - V_{polyd} & ifCOREMOD = 0 \\ V_{gsfbeff} - \Psi_d - V_{polyd} & ifCOREMOD = 1 \end{cases}$$

$$q_{ia} = 0.5 \cdot (q_{is} + q_{id})$$
$$\Delta q_i = q_{is} - q_{id}$$

Quantum Mechanical Effects

Charge Centroid Calculation

$$T4 = \frac{q_{im} + ETAQM \cdot q_{bm}}{QM0}$$

$$T5 = 1 + T4^{ALPHAQM}$$

$$T_{cen} = \frac{T_{cen0}}{T5}$$

Effective Width Model

If GEOMOD=0 then

$$W_{eff} = W_{eff0}$$
$$W_{eff,\,CV} = W_{eff,\,CV0}$$

If GEOMOD=1 then

$$W_{eff} = W_{eff0} - 4 \cdot QMTCENIV_i \cdot T_{cen}$$
$$W_{ef,\,CV} = W_{eff,\,CV0} - 4 \cdot QMTCENCV_i \cdot T_{cen}$$

© 2023 Cadence Design Systems, Inc.

If GEOMOD=2

$$W_{eff} = W_{eff0} - 8 \cdot QMTCENIV_i \cdot T_{cen}$$
$$W_{ef,\,CV} = W_{eff,\,CV0} - 8 \cdot QMTCENCV_i \cdot T_{cen}$$

If GEOMOD=3 then

$$W_{eff} = W_{eff0} - 2\pi \cdot QMTCENIV_i \cdot T_{cen}$$

$$W_{eff,\,CV} = W_{eff0,\,CV0} - 2\pi \cdot QMTCENCV_i \cdot T_{cen}$$

Effective Oxide Thickness/Effective Capacitance

If $QMTCENCV_i$ is not equal to 0 then

$$C_{ox,\,eff} = \begin{cases} \dfrac{3.9 \cdot \varepsilon_0}{TOXP\dfrac{3.9}{EPSROX} + T_{cen}\dfrac{QMTCENCV_i}{\varepsilon_{ratio}}} & GEOMOD \neq 3 \\ \dfrac{3.9 \cdot \varepsilon_0}{R \cdot \left[\dfrac{1}{\varepsilon_{ratio}} ln\left(\dfrac{R}{R - T_{cen}}\right) + \dfrac{3.9}{EPSROX} ln\left(1 + \dfrac{T_{oxp}}{R}\right)\right]} & GEOMOD = 3 \end{cases}$$

Charge Centroid Calculation for Accumulation

$$C_{ox,\,acc} = \begin{cases} \dfrac{3.9 \cdot \varepsilon_0}{TOXP\dfrac{3.9}{EPSROX} + \dfrac{T_{cen0}}{T6}\dfrac{QMTCENCVA_i}{\varepsilon_{ratio}}} & GEOMOD \neq 3 \\ \dfrac{3.9 \cdot \varepsilon_0}{R \cdot \left[\dfrac{1}{\varepsilon_{ratio}} ln\left(\dfrac{R}{R - T_{cen0}/T6}\right) + \dfrac{3.9}{EPSROX} ln\left(1 + \dfrac{T_{oxp}}{R}\right)\right]} & GEOMOD = 3 \end{cases}$$

© 2023 Cadence Design Systems, Inc.

If QMTCENCVi=0 then

$$C_{ox \cdot eff} = C_{ox}$$

$$C_{ox \cdot acc} = \frac{3.9 \cdot \varepsilon_0}{EOTACC}$$

Mobility Degradation and Series Resistance

Mobility Degradation

$$\eta = \begin{cases} \frac{1}{2} \cdot ETAMOB_i & NMOS \\ \frac{1}{3} \cdot ETAMOB_i & PMOS \end{cases}$$

$$E_{effa} = 10^{-8} \cdot \left(\frac{q_{ba} + \eta \cdot q_{ia}}{\varepsilon_{ratio} \cdot EOT} \right)$$

$$D_{mob} = \begin{cases} 1 + UA(T) \cdot (E_{effa})^{EU} + \dfrac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_{ia}}{q_{ba}} \right) \right)^{UCS(T)}} & \textbf{BULKMOD=0} \\ 1 + (UA(T) + UC(T) \cdot V_{eseff}) \cdot (E_{effa})^{EU} + \dfrac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_{ia}}{q_{ba}} \right) \right)^{UCS(T)}} & \textbf{BULKMOD=1} \end{cases}$$

$$D_{mob} = \frac{D_{mob}}{U0MULT}$$

© 2023 Cadence Design Systems, Inc.

Lateral Non-uniform Doping Model

$$M_{nud} = \exp\left(-\frac{K0_i}{K0SI_i \cdot q_{ia} + 2.0 \cdot \frac{nkT}{q}}\right)$$

Body Effect Model

$$V_{esx} = V_{es} - 0.5 \cdot (V_{ds} - V_{dsx})$$

$$V_{eseff} = min(V_{esx}, 0.95 \cdot PHIBE_i)$$

$$dVth_{BE} = \sqrt{PHIBE_i - V_{eseff}} - \sqrt{PHIBE_i}$$

$$M_{ob} = \exp\left(-dVth_{BE}\frac{K1_i + K1SAT_i \cdot V_{dsx}}{K0SI_i \cdot q_{ia} + 2.0 \cdot \frac{nkT}{q}}\right)$$

Output Conductance

Channel Length Modulation

$$C_{clm} = \begin{cases} PCLM_i \cdot (1 + PCLMG_i \cdot q_{ia}) & for \quad PCLMG > 0 \\ \dfrac{1}{\dfrac{1}{PCLM_i} - PCLMG_i \cdot q_{ia}} & for \quad PCLMG < 0 \end{cases}$$

$$M_{clm} = 1 + \frac{1}{C_{clm}} 1n\left[1 + \frac{V_{ds} - V_{dseff}}{V_{ASAT} + E_{satL}}\right] \cdot C_{clm}$$

© 2023 Cadence Design Systems, Inc.

Output Conductance due to DBL

$$PVAG_{factor} = \begin{cases} 1 + PVAG_i \cdot \dfrac{q_{ia}}{E_{sat} L_{eff}} & for \quad PVAG_i > 0 \\ \dfrac{1}{1 - PVAG_i \cdot \dfrac{q_{ia}}{E_{sat} L_{eff}}} & for \quad PVAG_i < 0 \end{cases}$$

$$\theta_{rout} = \frac{0.5 \cdot PDIBL1_a}{\cosh\left(DROUT_i \cdot \dfrac{L_{eff}}{\lambda}\right) - 1} + PDIBL2_i$$

$$V_{ADIBL} = \frac{q_{ia} + 2kT/q}{\theta_{rout}} \cdot \left(1 - \frac{V_{dsat}}{V_{dsat} + q_{ia} + 2kT/q}\right) \cdot PVAG_{factor}$$

$$M_{oc} = \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \cdot M_{clm}$$

Velocity Saturation

Current Degradation Due to Velocity Saturation

$$E_{sat1} = \frac{2 \cdot VSAT1_a \cdot D_{mob}}{\mu_0(T)}$$

$$\delta_{vsat} = DELTAVSAT_i$$

© 2023 Cadence Design Systems, Inc.

$$D_{vsat} = \frac{1 + \left(\delta_{vsat} + \left(\frac{\Delta q_i}{E_{sat1} L_{eff}}\right)^{PSAT(L)}\right)^{\frac{1}{PSAT(L)}}}{1 + (\delta_{vsat})^{\frac{1}{PSAT(L)}}} + \frac{1}{2} \cdot PTWG_a \cdot q_{ia} \cdot \Delta\varphi^2$$

Non-Saturation Effect

$$T_0 = max\left[\left(A1_i + \frac{A2_i}{q_{ia} + 2.0 \cdot \frac{nkT}{q}}\right) \cdot \Delta q_i^2, -1\right]$$

$$N_{sat} = \frac{1 + \sqrt{1 + T0}}{2}$$

$$D_{vsat} = D_{vsat} \cdot N_{sat}$$

Drain Current Model

$$I_{ds} = IDS0MULT \cdot \mu_0(T) \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot i_{ds0} \cdot \frac{M_{oc} M_{ob} M_{nud}}{D_{vsat} D_r D_{mob}} \times NFIN_{total}$$

Intrinsic Capacitance Model

Channel Length Modulation

$$M_{clm,\,CV} = 1 + \frac{1}{PCLMCV} ln\left[1 + \frac{V_{ds} - V_{dseff}}{V_{dsat} + E_{satCVL}}\right] \cdot PCLMCV$$

© 2023 Cadence Design Systems, Inc.

$$I_{ds,\,CV} = T1 \cdot \frac{M_{clm,\,cv}}{D_{r,\,CV}}$$

Intrinsic (Normalized) Charge

$$q_b = q_{bs}$$

$$q_g = \left[q_{ia} + T0 \cdot \frac{\Delta q^2 i}{12 \cdot i_{ds,\,CV}} \right] \cdot \frac{1}{M_{clm,\,CV}} + (M_{clm,\,CV} - 1) \cdot qid$$

$$q_d = \left[0.5 \cdot q_{ia} - \frac{\Delta q_i}{12} \cdot \left(1 - T1 \frac{\Delta q_i}{30 \cdot i_{ds,\,CV}} - T2 \frac{\Delta q^2 i}{1260 \cdot i^2_{ds,\,CV}} \right) \right] \cdot \frac{1}{M^2_{clm,\,CV}} + \left[M_{clm,\,CV} - \frac{1}{M_{clm,\,CV}} \right] \cdot q_{id}$$

Accumulation Charge

If GEOMOD=3 then

$$q_{0,\,acc} = \frac{2 \cdot kT \cdot r1_{acc}}{q}$$

Terminal Charges

For GEOMOD not equal to 3

$$q_{i,\,acc} = V_{gsfbeff,\,ac} - \frac{2kT}{q}[1n(\beta)] - 1n(\cos(\beta)) + F_{1.acc}$$

© 2023 Cadence Design Systems, Inc.

For GEOMOD=3

$$q_{i,\,acc} = q_{0,\,acc} \cdot g$$

Terminal Charges

$$Q_{g,\,intrinsic} = NFIN_{total} \cdot C_{ox,\,eff} \cdot W_{eff,\,CV} \cdot L_{eff,\,CV} \cdot (q_g)$$

$$Q_{d,\,intrinsic} = NFIN_{total} \cdot C_{ox,\,eff} \cdot W_{eff,\,CV} \cdot L_{eff,\,CV} \cdot (-q_d)$$

$$Q_{b,\,intrinsic} = NFIN_{total} \cdot C_{ox,\,eff} \cdot W_{eff,\,CV} \cdot L_{eff,\,CV} \cdot (-q_b)$$

$$Q_{s,\,intrinsic} = -Q_{g,\,intrinsic} - Q_{d,\,intrinsic} - Q_{b,\,intrinsic}$$

$$Q_{g,\,acc} = NFIN_{total} \cdot C_{ox,\,acc} \cdot W_{eff,\,CV0} \cdot L_{eff,\,CV} \cdot (-q_{i,\,acc})$$

$$Q_{b,\,acc} = NFIN_{total} \cdot C_{ox,\,acc} \cdot W_{eff,\,CV0} \cdot L_{eff,\,CV} \cdot (-q_{i,\,acc})$$

Parasitic resistances and capacitance models

BSIM-CMG models the parasitic source/drain resistance in two components: a bias dependent extension resistance and a bias independent diffusion resistance. Parasitic gate resistance is modeled as well.

RDSMOD=0 (Internal)

$$R_{source} = R_{s,\,geo}$$

$$R_{drain} = R_{d,\,geo}$$

© 2023 Cadence Design Systems, Inc.

$$R_{ds} = \frac{1}{NFIN_{total} \cdot W_{eff0}^{WR_i}} \cdot \left(RDSWMIN(T) + \frac{RDSW(T)}{1 + PRWG_i \cdot q_{ia}} \right)$$

$$D_r = 1.0 + NFIN_{total} \cdot \mu_0(T) \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{i_{ds0}}{\Delta q_i} \cdot \frac{Rd_s}{D_{vsat} \cdot D_{mob}}$$

RDSMOD=1 (External)

$$R_{source} = \frac{1}{W_{eff0}^{WR_i} \times NFIN_{total}} \cdot \left(RSWMIN(T) + \frac{RSW(T)}{1 + PRWG_i \cdot V_{gs,\,eff}} \right) + R_{s,\,geo}$$

$$R_{drain} = \frac{1}{W_{eff0}^{WR_i} \times NFIN_{total}} \cdot \left(RSWMIN(T) + \frac{RSW(T)}{1 + PRWG_i \cdot V_{gd,\,eff}} \right) + R_{d,\,geo}$$

$R_{s,geo}$ and $R_{d,geo}$ are the source and drain diffusion resistances, described as follows:

Velocity saturation effect in drain/source resistances

This model only works for RDSMOD = 1. At high current levels, the charge carriers in drain/source resistances may undergo velocity saturation. To this end, two resistances Rvs;d and Rvs;s are added at the drain and source sides, and expressed as follows.

© 2023 Cadence Design Systems, Inc.

Drain side

$$R_{vs,d} = R_{0d}\left[1 + \left(\frac{\delta_{vs,rd}^{\frac{1}{MVSRSD}} \cdot |V_{di1,di}|}{V_{sat,rd}}\right)^{MVSRSD}\right]^{\frac{1}{MVSRSD}}$$

$$R_{0d} = RDLCW \cdot rdstempvs(T) \cdot \frac{1}{NFINtotal \cdot Weff0^{WR}}$$

$$rdstempvs = 1 + PRTVSRSD \cdot (T - T_{nom})$$

$$\delta_{vs,rd} = \frac{|V_{di1,di}|^{4-MVSRSD}}{|V_{di1,di}|^{4-MVSRSD} + VSRDFACTOR \cdot V_{sat,rd}^{4-MVSRSD}}$$

Source side

$$R_{vs,s} = R_{0s}\left[1 + \left(\frac{\delta_{vs,rs}^{\frac{1}{MVSRSD}} \cdot |V_{si,si1}|}{V_{sat,rs}}\right)^{MVSRSD}\right]^{\frac{1}{MVSRSD}}$$

$$R_{0s} = RSLCW \cdot rdstempvs(T) \cdot \frac{1}{NFINtotal \cdot Weff0^{WR}}$$

$$\delta_{vs,rs} = \frac{|V_{si,si1}|^{4-MVSRSD}}{|V_{si,si1}|^{4-MVSRSD} + VSRSFACTOR \cdot V_{sat,rs}^{4-MVSRSD}}$$

$$I_{sat,rs} = q \cdot NVSRS \cdot Weff0 \cdot NFINtotal \cdot VSATRSD_{eff}$$

$$V_{sat,rs} = R_{0s} \cdot I_{sat,rs}$$

© 2023 Cadence Design Systems, Inc.

Sheet Resistance Model

RGEOMOD = 0 (sheet resistance model)

$$R_{s,\,geo} = NRS \cdot RSHS$$

$$R_{d,\,geo} = NRD \cdot RSHD$$

Diffusion Resistance Model for Variability Modeling

RGEOMOD=1

$$R_{s,\,geo} = R_{dgeo} = \frac{R_{rsd} + R_{ext}}{NF} \cdot \left[\begin{array}{l} RGEOA + RGEOB \times TFIN + RGEOC \times FPITCH + \\ RGEOD \times LRSD + RGEOE \times HEPI \end{array} \right]$$

Gate Electrode Resistance Model

$$R_{geltd} = \begin{cases} \dfrac{RGEXT + RGFIN \cdot NFIN}{3 \cdot NF} & for\ \ NGCON = 1 \\ \dfrac{RGEXT + RGFIN \cdot NFIN}{12 \cdot NF} & for\ NGCON = 2 \end{cases}$$

Bias-dependent Overlap Capacitance Model

The bias-dependent overlap capacitance model in BSIM-CMG is adopted from BSIM4 for CGEOMOD = 0 and CGEOMOD = 2. The overlap charge is given by:

$$\frac{Q_{gs,\,ov}}{NFIN_{total} \cdot W_{effCV}} = CGSO \cdot V_{gs} + CGSL \cdot \left[\begin{array}{l} V_{gs} - V_{fbsd} - V_{gs,\,overlap} - \dfrac{CKAPPAS}{2} X \\ \left(\sqrt{1 - \dfrac{4 V_{gs,\,overlap}}{CKAPPAS}} - 1 \right) \end{array} \right]$$

© 2023 Cadence Design Systems, Inc.

$$\frac{Q_{gd,\,ov}}{NFIN_{total}\cdot W_{effCV}} = CGDO\cdot V_{gd} + CGDL\cdot\left[\frac{V_{gd} - V_{fbsd} - V_{gd,\,overlap} - \frac{CKAPPAD}{2}\,X}{\left(\sqrt{1 - \frac{4V_{gd,\,overlap}}{CKAPPAD}} - 1\right)}\right]$$

Substrate Parasitics

$$C_{sbox} = C_{box}\cdot ASEO + C_{box,\,sw}\cdot(PSEO - FPITCH\times NFINtotal)$$

$$C_{dbox} = C_{box}\cdot ADEO + C_{box,\,sw}\cdot(PDEO - FPITCH\times NFINtotal)$$

$$C_{box,\,sw} = CSDESW\cdot 1n\left(1 + \frac{HFIN}{EOTBOX}\right)$$

$$C_{ge,\,overlap,\,1} = (CGBO\cdot NF + NGCON + CGBN\cdot NFIN_{total})\cdot L_{eff,\,CV}$$

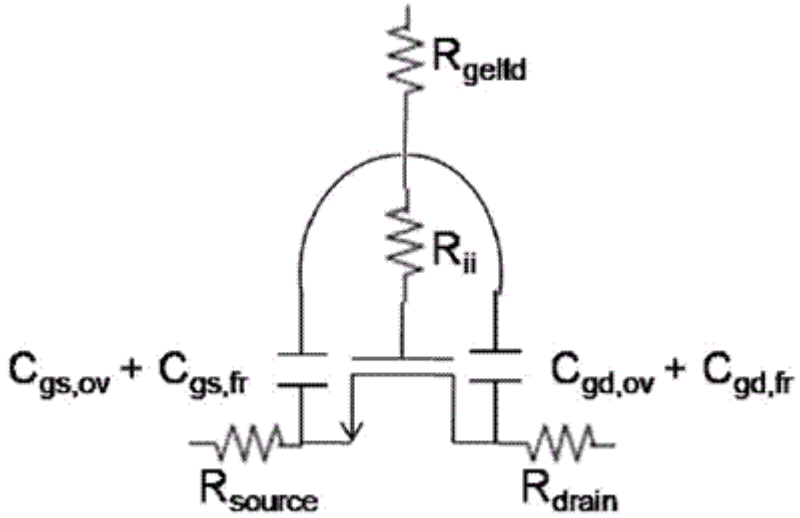
© 2023 Cadence Design Systems, Inc.

Fringe Capacitances and Capacitance Model Selectors

CGEOMOD=0

$$C_{gs,fr} = NFIN_{total} \cdot W_{eff,CV} \cdot CFS_i$$

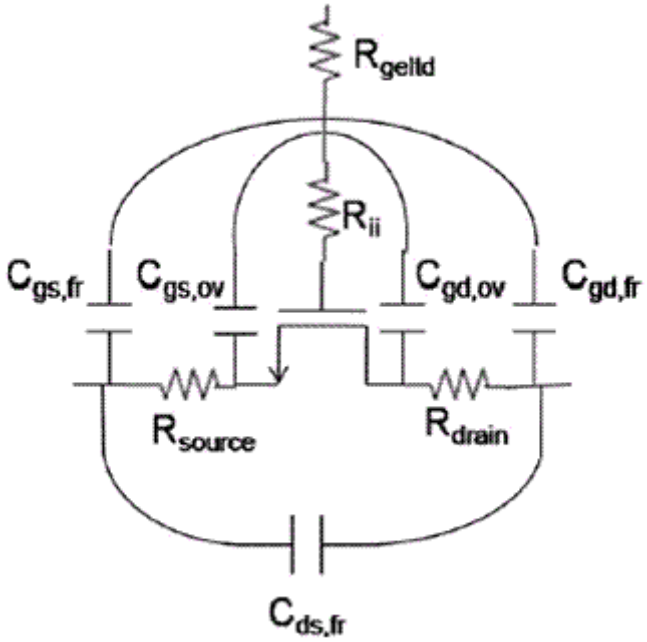
$$C_{gd,fr} = NFIN_{total} \cdot W_{eff,CV} \cdot CFD_i$$



R-C network for CGEOMOD=0, NQSMOD=1, RGATEMOD=1 and RDSMOD=1.

© 2023 Cadence Design Systems, Inc.

If NQSMOD, RGATEMOD or RDSMOD is 0, then the corresponding resistances become 0 and the nodes collapse.



R-C network for CGEOMOD=1, NQSMOD=1, RGATEMOD=1 andRDSMOD=1.

If NQSMOD, RGATEMOD or RDSMOD is 0, then the corresponding resistances become 0 and the nodes collapse.

CGEOMOD = 1

$$C_{gs,ov} = COVS_i$$
$$C_{gd,ov} = COVD_i$$
$$C_{gs,fr} = CGSP$$
$$C_{gd,fr} = CGDP$$
$$C_{ds,fr} = CDSP$$

© 2023 Cadence Design Systems, Inc.

In CGEOMOD=2

$$C_{fr,\,top} = C_{fringe,\,2D}(H_g, H_{rsd}, LRSD) \times TFIN \times NFIN$$

$$C_{fr,\,side} = 2 \times C_{fringe,\,2D}(W_g, T_{rsd}, LRSD) \times HFIN \times NFIN$$

$$C_{corner} = \frac{\varepsilon_{sp}}{LSP} \cdot [A_{corner} \times HFIN + ARSDEND + ASILIEND]$$

$$C_{fr,\,geo} = \begin{array}{l}(C_{corner} + C_{fr,\,top} + CGEOE \cdot C_{fr,\,side}) \times NF \text{ x} \\ [CGEOA + CGEOB \cdot TFIN + CGEOC \cdot FPITCH + CGEOD \cdot LRSD]\end{array}$$

$$C_{fr,\,top} = \left\{3.467 \times 10^{-11} \cdot 1n\left(\frac{EPSRSP \cdot 10^{-7}}{3.9 \cdot LSP}\right) + 0.942 \cdot H_{rsd} \cdot \frac{\varepsilon_{sp}}{LSP}\right\} \cdot \begin{array}{l} \\ ([TFIN + (FPITCH - TFIN) \cdot CRATIO] \cdot NFIN)\end{array}$$

CGEOMOD=0/1/2

$$C_{ds,\,fr} = CDSP$$

Impact Ionization and GIDL/GISL Model

Impact Ionization Current

I_{ii} can be switched off by setting IIMOD = 0

Case: IIMOD = 1

$$Iii = \frac{ALPHA0_i + ALPHA1_i \cdot L_{eff}}{L_{eff}}(V_{ds} - V_{dseff}) \cdot e^{\frac{BETA0(T)}{V_{ds} - V_{dseff}}} \cdot Ids$$

© 2023 Cadence Design Systems, Inc.

Case: IIMOD=2

$$I_{ii} = ALPHAII_i \cdot I_{ds} \cdot \exp\left(\frac{V_{diff}}{BETAII2_i + BETAII1_i V_{diff} + BETAII0_i V^2_{diff}}\right)$$

Gate-Induced-Drain/Source-Leakage Current

GIDL/GISL are calculated only for GIDLMOD = 1

$$T0 = \frac{AGIDL_i \cdot W_{eff0} \cdot \frac{V_{ds} - V_{fgs} - EGIDL_i + V_{fbsd}}{\varepsilon_{ratio} \cdot EOT} \times \exp\left(-\frac{\varepsilon_{ratio} \cdot EOT \cdot BGIDL(T)}{V_{ds} - V_{gs} - EGIDL_i + V_{fbsd}}\right) \text{ x}}{NFIN_{total}}$$

$$I_{gidl} = \begin{cases} T0 \cdot \frac{V_{de}^3}{CGIDL + V_{de}^3} & BULKMOD = 1 \\ T0 \cdot V_{ds} & \text{BULKMOD=0} \end{cases}$$

$$T1 = \frac{AGISL_i \cdot W_{eff0} \cdot \left(\frac{-V_{ds} - V_{gd} - EGISL_i + V_{fbsd}}{\varepsilon_{ratio} \cdot EOT}\right)^{PGISL_i} \times \exp\left(-\frac{\varepsilon_{ratio} \cdot EOT \cdot BGIDL(T)}{-V_{ds} - V_{gd} - EGIDL_i + V_{fbsd}}\right)}{NIFN_{total}}$$

$$I_{gisl} = \begin{cases} T1 \cdot \frac{V_{se}^3}{CGISL + V_{se}^3} & BULKMOD = 1 \\ T1 \cdot V_{ds} & \text{BULKMOD=0} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Gate Tunneling Current

Gate to body current I_{gbinv} and I_{gbacc} is calculated only if IGBMOD = 1

$$I_{gbinv} = \begin{array}{l} W_{eff0} \cdot L_{eff} \cdot A \cdot T_{ox,\,ratio} \cdot V_{ge} \cdot V_{aux,\,igbinv} \cdot I_{gtemp} \times NFIN_{total} \cdot \\ \exp(-B \cdot TOXP \cdot (AIGBINV_i - BIGBINV_i \cdot q_{ia})) \cdot (1 + CIGBINV_i \cdot q_{ia}) \end{array}$$

$$I_{gbacc} = \begin{array}{l} W_{eff0} \cdot L_{eff} \cdot A \cdot T_{ox,\,ratio} \cdot V_{ge} \cdot V_{aux,\,igbacc} \cdot I_{gtemp} \times NFIN_{total} \cdot \\ \exp(-B \cdot TOXP \cdot (AIGBINV_i - BIGBINV_i \cdot V_{oxacc})) \cdot (1 + CIGBINV_i \cdot V_{oxacc}) \end{array}$$

Gate to channel current I_{gc} is calculated only for IGCMOD = 1.

$$I_{gcs0} = \begin{array}{l} W_{eff0} \cdot L_{eff} \cdot A \cdot T_{ox,\,ratio} \cdot I_{gtemp} \times NFIN_{total} \cdot T0 \\ \cdot \exp(-B \cdot TOXP \cdot (AIGC_i - BIGC_i \cdot V_{oxm})) \cdot (1 + CIGC_i \cdot V_{oxm}) \end{array}$$

$$I_{gcs} = I_{gc0} \cdot \frac{PIGCD_i \cdot V_{dseffx} + \exp(PIGCD_i \cdot V_{dseffx}) - 1.0 + 1.0e-4}{PIGCD_i^{\,2} \cdot V^2_{dseffx} + 2.0e-4}$$

$$I_{gcd} = I_{gc0} \cdot \frac{1.0 - (PIGCD_i \cdot V_{dseffx} + 1.0) + \exp(-PIGCD_i \cdot V_{dseffx}) + 1.0e-4}{PIGCD_i^{\,2} \cdot V^2_{dseffx} + 2.0e-4}$$

Gate to source/drain current I_{gs}, I_{gd} are calculated only for IGCMOD = 1

$$i_{gsd,\,mult} = I_{gtemp} \cdot \frac{W_{eff0} \cdot A}{(TOXP \cdot POXEDGE_i)^2} \left(\frac{TOXREF}{(TOXP \cdot POXEDGE_i)^2} \right)^{NTOXi}$$

$$I_{gs} = \begin{array}{l} i_{gsd,\,mult} \cdot DLCIGS \cdot V'_{gs} \mathrm{X}\, NFIN_{total} \cdot \\ \exp(-B \cdot TOXP \cdot POXEDGE_i \cdot (AIGS_i - BIGS_i \cdot V'_{gs}) \cdot (1 + CIGS_i \cdot V'_{gs})) \end{array}$$

© 2023 Cadence Design Systems, Inc.

$$I_{gd} = \begin{array}{l} i_{gsd,\,mult} \cdot DLCIGD \cdot V_{gd} \cdot V'_{gd} \mathrm{X}\, NFIN_{total} \cdot \\ \exp(-B \cdot TOXP \cdot POXEDGE_i \cdot (AIGS_i - BIGS_i \cdot V'_{gd}) \cdot (1 + CIGS_i \cdot V'_{gd})) \end{array}$$

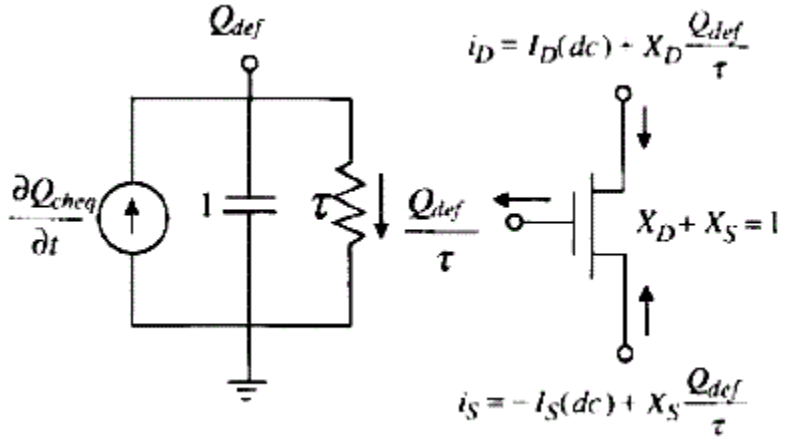
Non Quasi-static Models

This version offers three different non quasi-static (NQS) models. Each of these can be turned on/off using the NQSMOD switch. Setting NQSMOD = 0 turns off all NQS models and switches to plain quasi-static calculations.

Gate Resistance Model (NQSMOD = 1)

$$I_{dovVds} = \mu_0(T) C_{ox} \frac{W_{eff}}{L_{eff}} q_{ia} \frac{M_{oc}}{G_{vsat}}$$

$$\frac{1}{R_{ii}} = \frac{NF}{NFIN} \cdot XRCRG1_i \cdot \left(I_{dovVds} + XRCRG2 \cdot \frac{\mu_{eff} C_{oxe} W_{eff} kT}{q L_{eff}} \right)$$



R-C network for calculating deficient charge Q_{def} and the instantaneous charge, Q_{def}/τ is used in place of the quasi-static charges.

© 2023 Cadence Design Systems, Inc.

Charge Deficit Model (NQSMOD = 2)

$$X_{d,\,part} = \frac{q_d}{q_g}$$

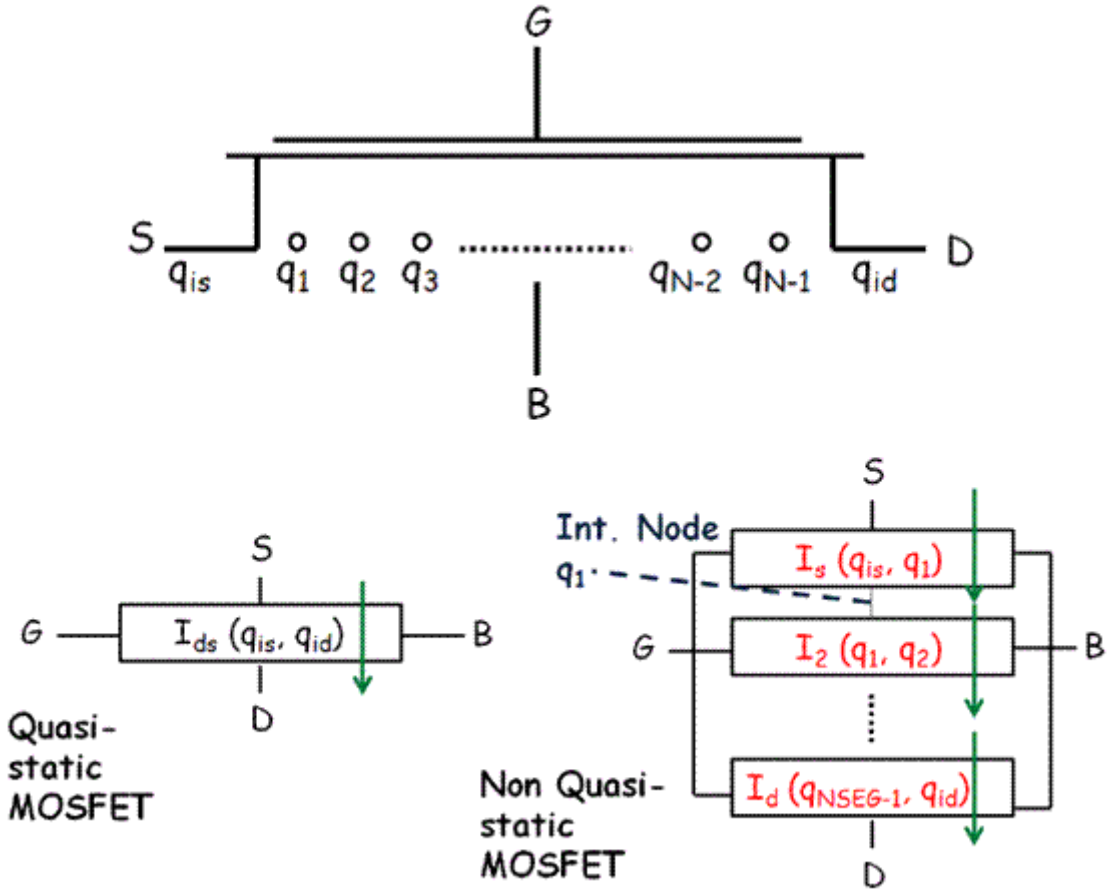
$$I_{dovVds} = \mu_0(T) C_{ox} \frac{W_{eff}}{L_{eff}} q_{ia} \frac{M_{oc}}{D_{vsat}}$$

$$\frac{1}{R_{ii}} = \frac{NF}{NFIN} \cdot XRCRG1_i \cdot \left(I_{dovVds} + XRCRG2 \cdot \frac{\mu_{eff} C_{oxe} W_{eff} kT}{q L_{eff}} \right)$$

$$\frac{1}{\tau} = \frac{1}{R_{ii} \cdot C_{ox} \cdot W_{eff} \cdot L_{eff}}$$

© 2023 Cadence Design Systems, Inc.

Charge Segmentation Model (NQSMOD = 3)



A N-segment charge-segmented MOSFET with N-1 internal nodes.

Note: This model is not supported for COREMOD = 1 && GEOMOD not equal to 3. That is, for double gate and likes together with the simplified surface potential solution.

Generation-recombination Component

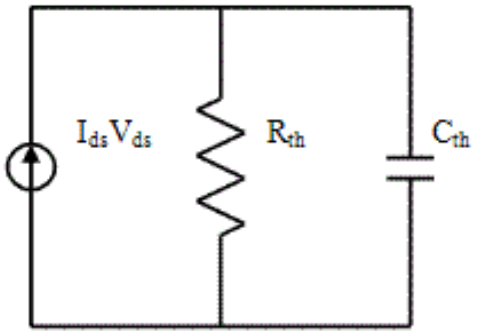
$$I_{ds,gen} = \frac{HFIN \cdot TFIN \cdot (L_{eff} - LINTIGEN) \cdot (AIGEN_i \cdot V_{ds} + BIGEN_i \cdot V^3_{ds}).}{\exp\left[\frac{qE_g}{NTGEN_i \cdot kT}\left(\frac{T}{TNOM} - 1\right)\right] \times NFIN_{total}}$$

© 2023 Cadence Design Systems, Inc.

Junction Current and Capacitances

The junction current and capacitances are only calculated for bulk multi-gate devices (BULKMOD = 1).

Self-heating Model



Thermal resistance and capacitance calculations:

$$R_{th} = \frac{RTH0}{(WTH0 \cdot NF^{BSHEXP} + FPITCHNFIN_{total}{}^{ASHEXP})}$$

$$C_{th} = C_{TH0} + (WTH0 + FPITCH \cdot NFIN_{total})$$

Noise Models

Noise models in BSIM-CMG are based on BSIM4. The following table lists the origin of each noise model:

Model in BSIM-CMG105.0 alpha	**Origin**
Flicker noise model	BSIM4 Unified Model (FNOIMOD=1)
Thermal noise	BSIM4 TNOIMOD=0
Gate current shot noise	BSIM4 gate current noise
Noise associated with parasitic resistances	BSIM4 parasitic resistance noise

© 2023 Cadence Design Systems, Inc.

Flicker Noise Model

$$S_{si} = \frac{kTq^2 \mu_{eff} I_{ds}}{C_{oxe} L^2_{eff,noif}{}^{EF} \cdot 10^{10}} \cdot FN1 + \frac{kTI^2_{ds} \Delta L_{clm}}{W_{eff} \cdot NFIN_{total} \cdot L^2_{eff,noif}{}^{EF} \cdot 10^{10}} \cdot FN2$$

$$S_{wi} = \frac{NOIA \cdot kT \cdot I^2_{ds}}{W_{eff} \cdot NFIN_{total} \cdot L^2_{eff,noif}{}^{EF} \cdot 10^{10} \cdot N^{*2}}$$

$$S_{id,flicker} = \frac{S_{wi} S_{si}}{S_{wi} + S_{si}}$$

Thermal noise model (TNOIMOD = 0)

$$Q_{inv} = \left| Q_{s,intrinsic} + Q_{d,intrinsic} \right| \times NFIN_{total}$$

$$\overline{i^2_d} = \begin{cases} NTNOI \cdot \dfrac{4kT\Delta f}{R_{ds} + \dfrac{L^2_{eff}}{\mu_{eff} Q_{inv}}} & if \quad RDSMOD = 0 \\ NTNOI \cdot \dfrac{4kT\Delta f}{L^2_{eff}} \cdot \mu_{eff} Q_{inv} & if \quad RDSMOD = 1 \end{cases}$$

Gate Current Shot Noise

$$\overline{i^2_{gs}} = 2q(I_{gcs} + I_{gs})$$

$$\overline{i^2_{gd}} = 2q(I_{gcd} + I_{gd})$$

$$\overline{i^2_{gb}} = 2qI_{gbinv}$$

© 2023 Cadence Design Systems, Inc.

Resistor Noise

The noise associated with each parasitic resistors in BSIM-CMG is calculated.

If RDSMOD = 1 then

$$\frac{\overline{i^2_{RS}}}{\Delta f} = 4kT \cdot \frac{1}{R_{source}}$$

$$\frac{\overline{i^2_{RD}}}{\Delta f} = 4kT \cdot \frac{1}{R_{drain}}$$

If RGATEMOD = 1 then

$$\frac{\overline{i^2_{RG}}}{\Delta f} = 4kT \cdot \frac{1}{R_{geltd}}$$

Model Version Update

Version 105.02 Update

- Added binning along NFIN for all the binnable parameters
- Introduced Gate-to-Substrate Bias dependent parasitic capacitance through parameters CGBL and CKAPPA (both binned)
- Introduced a second-step-junction to S-B and D-B diodes through parameters SJS, MJS2, SJSWS, MJSWS2, SJSWGS, MJSWGS2?SJD, MJD2, SJSWD, MJSWD2, SJSWGD, MJSWGD2
- Source/Drain Junction Tunneling Currents have been introduced (Refer to the BSIM4 model for equations, parameters and binning)

Version 105.03 update

- PCLMG, VASAT, ETAMOB have been added to the list of binnable parameters.
- DVTSHIFT parameter introduced as a handle to create Vth shift.

© 2023 Cadence Design Systems, Inc.

- All older mobility models replaced with one single new mobility model. The new mobility model uses UA, EU, UD and UCS parameters from MOBMOD=0 of 105.02 release if MOBMOD=1 is used from the previous version.
- New velocity saturation (Ion degradation) model. Parameters VSAT1 (binned), DELTAVSAT replace old parameter THETASAT. This change is not backward compatible.
- RDSMOD=0 implementation changed for better accuracy.
- CLM Model modified to prevent cross-correlation of binning parameters.
- Igb accumulation component added for IGBMOD=1. Available for both BULKMOD=0 and 1.
- Vds asymmetric function changed for better higher order derivative predictivity.
- Accumulation side charge centroid incorporated for better fitting of accumulation capacitance.
- Old parameter ALPHAQM replaced by PQM for the inversion side charge centroid equation.
- Definition of TNOM changed from Kelvin to Celsius to be consistent with BSIM4/ BSIMSOI.

Version 105.031 update

- Limited the exponential function in TANH(x) definition
- GIDL Current Model modified for zero current at zero bias.
- Gate Current Model modified, as follows:
  - Default values of `BIGBINV`, `AIGBACC`, `BIGBACC`, `NIGBACC` changed
  - Gate-to-Channel Current, Igcs/Igcd. Partition function implemented with parameter PIGCD (Binned)
  - Gate Edge Leakage Igs changed
  - Gate Edge Leakage Igd changed
- Removed CLM effect in Charge Model due to wrong implementation.
- Fixed discontinuity in implementation at PCLMG=0 for CLM Model

© 2023 Cadence Design Systems, Inc.

Version 105.04 update

- Built-in tanh() function used instead of ((exp(x) - exp(-(x))) / (exp(x) + exp(-(x))))
- GIDL Current Model modified. New parameter PGIDL/PGISL introduced.
- Gate Current Model modified. Equations around BSIM4 parameters NTOX (binned) and TOXREF added
- CLM Model modified.
  - Fixed discontinuity in implementation at PCLMG=0 for CLM Model
  - CLM Model for I-V Modified.
- Parameter VASAT removed. The old equation was known to case unphysical wiggles.
- ETAMOB binning corrected and linear temperature dependence added with new parameter EMOBT
- Velocity Saturation Model for better Id,sat and Gm,sat fitting
- Parameters DELTAVSAT, DVTSHIFT and KT1 are now binned
- CGEOMOD=0 case; removed QM effects in Fringe Caps
- Drain-to-Source Fringe Cap now available for all CGEOMOD
- Introduced DLCACC parameter for accumulation region capacitance (CAPMOD=1 and BULKMOD=1)
- Velocity Saturation Model for Short Channel C-V introduced. New parameter VSATCV (binned) added
- CLM Model for C-V Modified.
  - MclmCV factor simplified. Parameters VASATCV and PCLMGCV removed
  - Corrected the wrong implementation of in the charge equations
  - For NQSMOD=3, a simple change has been made
- Added relevant equations for Short Channel CV.
- Parameter NFIN has been converted from integer to real to enable optimization
- Gate-to-Substrate Overlap cap scalability corrected. New parameter CGBN introduced.
- Temperature Dependence for Subthreshold Swing enhanced with new parameter TSS (binned)

© 2023 Cadence Design Systems, Inc.

- RDSMOD=1 enhanced to capture quasi-saturation / current crowding for high voltage devices. New parameters RSDR, RDDR, PRSDR, PRDDR introduced and new equations added. Temperature dependence through TRSDR and TRDDR parameters
- Asymmetric Model - ASYMMOD Switch.
  - In order to model highly asymmetric devices, seven parameters identified in the model and their reverse mode equivalents created. These parameters are: CDSCDR, ETA0R, PDIBL1R, PTWGR, VSAT1R, RSDRR, and RDDRR (Original parameters + 'R' in the end)
  - Additional parameter PRWG split into PRWGS and PRWGD for source and drain side in RDSMOD=1
- Some cosmetic changes to Impact Ionization model (especially IIMOD=1), implementing smooth functions
- Body Effect for BULKMOD=1. New parameters introduced: PHIBE, K1, K1ST, K1SAT.
- Removed nVtm in the poly-depletion correction term.
- Changed the value of q from 1.6e-19 to 1.60219e-19 (Coulombs)
- Quantum Mechanical Effects
  - Introduced new parameter QMTCENCVA (binned) to replace QMTCENCV for the accumulation region capacitance;
  - Some bug fixes done for variable 'Tcen' calculations in both inversion and accumulation region
- Introduced Non-saturation effect with new parameters A1 and A2. To be used to improve Id,sat and Gm,sat fitting.
- Lateral NUD Model introduced to create IV-CV Vth shift.

Version 106.0.0 update

BSIMCMG 106.0.0 is the first standard model for FinFETs. It is based on the version 105.031. Following are the changes from its base version:

- Used built-in hyperbolic functions instead of macros
- Added more significant digits to definition of electronic charge
- Fixed usage of parameter "CIT" in noise model

© 2023 Cadence Design Systems, Inc.

- Clamped phib and vbi to positive. Current expressions can be negative with SHMOD=1 at high temperature
- Fixed some typo bugs

Version 106.1.0 update

BSIMCMG 106.1.0 is the second standard model for FinFETs. It is based on the version 105.04. Following are the changes from its base version:

- The definitions of the physical intrinsic capacitances, CEDI and CEEI have been corrected.
- Gate resistance model has been corrected.
- Vfbsd equation for poly and metal gates has been changed.
- For `_BINNABLE_` parameters, the bounds are now applied to the "Effective PARAM" (PARAM_i) instead of the root term (PARAM). These include K0SI, DSUB, DVT1, PSAT, and PHIBE.
- The effects of mobility, series resistances, and velocity saturation degradation terms on C-V calculations have been commented out for now (a roll back to BSIM-CMG105.031) to investigate those terms more carefully.
- Effective Channel Length equation has been changed.
- Coulomb scattering term has been changed for correct weak-inversion ID-VG slop/ behavior.
- Threshold voltage definition has been introduced.
- Temperature dependence of gate tunneling current has been introduced.
- Temperature dependence of the body effect model, lateral non-uniform doping model, and non-saturation effect model has been introduced.
- The temperature effect on U0 now affects UTL.
- Temperature and length dependence of the impact ionization current has been introduced.
- The oxide thickness TOXG is now used in the gate tunneling current, instead of physical oxide thickness TOXP.
- The impact of series resistance on C-V model has been introduced. To enhance the fitting accuracy, a new parameter (correction factor) RCVFAC has been introduced and used in equation for RDSMOD=0.

© 2023 Cadence Design Systems, Inc.

- To accurately capture the transition region between subthreshold and strong inversion in I-V when a forward body bias is taken into account, a new model parameter K1SI has been introduced and used in Mob.
- The value of Is (Id) at accumulation region has been clamped at the fixed value of 1.0E-15. In this version, a new model parameter IMIN has been introduced to specify this value.
- NQSMOD=3 has been disabled to perform an offline study.
- A more careful examination of the C-V model derivation revealed that 1) dividing the term idscv by Dmob_cv and Dr_CV and 2) multiplying it by MclmCV were implementation mistakes. This has been corrected.
- To enhance the fitting accuracy, two new parameters DELTAVSATCV and PSATCV have been introduced in Dvsat and CV.
- When the argument x is too huge, the built-in cosh(x) could cause arithmetic point error due to overflow. To protect the code, for x > 40, 0.5/(cosh(x)-1) has been replaced by exp(-x).
- Gate-induced source and drain leakage current equations have been changed.

Version 107.0.0 update

BSIMCMG 107.0.0 is the third standard model for FinFETs. It is based on the version 105.04. Following are the changes from its previous version 106.1.0:

- Lower `COVS`, `COVD`; defaults to 0 from 25pF.
- For `CGEOMOD=1` only, `GEO1SW=1` now enables the parameters `COVS`, `COVD`, `CGSP`, and `CGDP` to be in F per fin per gate-finger per unit channel width. The default value of the `GEO1SW` switch is zero.
- New NFIN scaling equations have been added for the following parameters: `PHIG`, `CDSC`, `CDSCD`, `CDSCDR`, `NBODY`, `VSAT`, `VSAT1`, `VSAT1R`, `ETA0`, and `U0`.
- The length scaling of SCE and SS has been decoupled. The new binnable parameter `DVT1SS` has been introduced.
- Temperature dependence of DIBL coefficient and Reverse-mode DIBL coefficient has been added. Two new parameters `TETA0` and `TETA0R` have been introduced.
- Long channel DIBL, also called Drain-Induced Vth Shift (DITS) has been added. Two new parameters `DVTP0` and `DVTP1` have been added.

© 2023 Cadence Design Systems, Inc.

- The average charge weighing factor has been added through the new parameter `CHARGEWF`.
- Support for the length dependence of the `Gate` workfunction has been added. A new parameters `PHIGL` has been added.
- To be consistent with SOI, RTH and CTH equations in the self-heating sub-model have been updated.
- The initial guess for the surface potential calculation has been improved. The model is now infinitely scalable with respect to `TFIN` and `NBODY` without any clamping on `NBODY`.

Version 108.0.0 update

BSIMCMG 108.0.0 is the fourth standard model for FinFETs. It is based on the version 105.04. Following are the changes from its previous version 107.0.0:

- A new parameter `TEMPMOD` has been introduced that enables switching between two types of temperature-dependent parameters.
- Thermal noise parameters `TNOIMOD=1` and `TNOIMOD=2` have been introduced.
- Support for `RDSMOD=1` has been added to avoid introducing extra nodes.
- New parameters have been added to `ASYMMOD=1`.

Version 110.0.0 update

BSIMCMG 110.0.0 is the fifth standard model for FinFETs. It is based on the version 105.04. Following are the changes from its previous version 108.0.0:

Bug Fixes:

- T9 equation in BULKMOD=1 code now uses `K1_t` instead of `K1`.
- Charge term `qis` in thermal noise changed to `qia`.
- For NOIMOD=1, `max()` is now applied to `Vds/Ids` instead of only `Ids`.
- Lower clamp limits on two model parms, `ALPHAII0` and `ALPHAII1` fixed.
- Possible missing terms in `Xpart/Qbul` calculations fixed.
- Added initialization to `LK2SAT`, `NK2SAT`, `PK2SAT`, `LK2SAT1`, `NK2SAT1`, `PK2SAT1`.
- Hidden variables `Qdep_ov_Cins`, `qb_acc_s`, and `qb_acc_d` fixed.

© 2023 Cadence Design Systems, Inc.

- Smooth clamp implemented on gate current to prevent large values.
- Model parameter initialization updated.
- Comment text on BULKMOD= 1,2 related model parameters updated.
- Code updated to account for missing mobility term in noise model.
- TNOIMOD=2 fixed for divide by zero when ROIA or ROIB =0.
- Redundant variables from Model code removed.
- Fatal warning message for `PDIBL2_i` removed.
- TNOIMOD = 1removed.
- For ASYMMOD=1, parameters such as MEXPR, UCR and their binning terms have been updated.
- `NBODY_i` is misplaced before `Inv_L, Inv_NFIN` and `Inv_LNFIN` are declared.
- `Theta_RSCE` should not be put within the same begin/end block as `Theta_DIBL`.
- Fix typo of number with `CIGD_i` clamping.

Enhancements

- Better modeling of body bias effects in I-V and C-V.
- Model parameters increased to support ASYMMOD=1.
- Use 'defines "macros" in place of conventional Verilog-A instance/model parameter definitions.
- Added optional temperture node for self-heating analysis.
- Added BSIM4-like support for VFBSD in gate-channel tunneling current.
- Collapsed `bsimcmg_main.va` into `bsimcmg.va`
- DITS implemented.
- NFIN scaling of additional parameters; `NFINNOM` added as an instance parameter.
- Addition of output parameters: `T_TOTAL_K`, `T_TOTAL_C`, and `T_DELTA_SH`.
- RTH Dependence on NFIN, FPITCH.
- Better description of parameters.

© 2023 Cadence Design Systems, Inc.

Version 111.0.0 update

Following are the changes from its previous version 110.0.0:

Bug Fixes:

- Fixed `noiGd0` expression and possible nonphysical behavior in `TNOIMOD = 1`.
- Fixed expressions of `CGG`, `CDG`, `CSG`, `CEG` output variables.
- Included CLM/DIBL effects in Gamma.
- Fixed correlation coefficient issue that affects Sid level.
- Aligned GIDL/GISL parameters master/slave relations according to manual.
- Corrected the units of N-term and P-term binning parameters.
- Fixed `Rsourcegeo`/`Rdraingeo` multiplication with `W`.
- Corrected mobility degradation in accumulation at `Vb!=0`.
- Assigned unique noise names.
- Renamed “bsimcmg_PSS_initialization.include: to “bsimcmg_initialization.include”.
- Fixed bug in DITS module leading to kink in current derivative.
- Fixed bug in operating point variable GDS.
- Aligned units of master and slave parameters.

Enhancements:

- Improved clamping on Dmob.
- Separate bias-dependent/bias-independent parts of junction capacitance.
- Renamed model parameter `Imin` to `IMIN`.
- Added `VDSEFF` a built-in output variable.
- Improved fitting flexibility of `NF50` at low `Ids`.
- Added an equation reference for output variables in manual.
- `Igate` current clamp concern.
- Separate both model/instance parameters and pure model, pure instance parameters.

© 2023 Cadence Design Systems, Inc.

- Collapse `t` terminal when `SHMOD = 0` or `RTH0 = 0`.
- Remove `DEVTYPE`, use -1 for `ptype`.
- Aligned units of xxxR with xxx model parameters.
- Removed `ifdef` statements.
- Replaced functions with macros and added some macros.
- Added parameters to BPxxx category.
- Parameters range updated to avoid divide by zero or other possible numerical exceptions.
- Initialized variables to prevent hidden states.
- Correctly added drain-source fringing capacitance to the OP variable.
- Added binning for `DVTP0` and `DVTP1`.
- Improved `NQSMOD=2` convergence.
- Addressed numerical issue due to $\sqrt{e^{-x}+x-1}$.
- Corrected output variable `ITH` definition for `RDSMOD=1`.
- Replaced `if($param_given(PARAMETER))` conditions with `if(PARAMETER)` for parameters `NVTM`, `NFINNOM` and `TFIN_TOP/TFIN_BASE`.
- L offset parameters, `LINT`, `DLBIN` and `XL` are made binnable.
- Binning CV parameter values made default to DC counterpart.
- Introduced gate current scaling/adjustment factors- `IGB0MULT` and `IGC0MULT`.

Component tatements

This device is supported within altergroups.

Instance Syntax

```
Name  d  g  s  e  [t] ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

m	1.0	Multiplicity factor (number of FINFETs in parallel).
l	(30*1.0e-9) m	Designed gate length.
d	(40*1.0e-9) m	Diameter of the cylinder (GEOMOD=3).
tfin	(15*1.0e-9) m	Body (Fin) thickness.
fpitch	(80*1.0e-9) m	Fin pitch.
nf	1	Number of fingers.
nfin	1.0	Number of fins per finger.
ngcon	1	Number of gate contacts (1 or 2 sided).
aseo	0 m^2	Source-to-substrate overlap area through oxide.
adeo	0 m^2	Drain-to-substrate overlap area through oxide.
pseo	0 m	Perimeter of source-to-substrate overlap region.
pdeo	0 m	Perimeter of drain-to-substrate overlap region.
asej	0 m^2	Source junction area (BULKMOD=1 or 2).
adej	0 m^2	Drain junction area (BULKMOD=1 or 2).
psej	0 m	Source-to-substrate PN junction perimeter (BULKMOD=1 or 2).
pdej	0 m	Drain-to-substrate PN junction perimeter (BULKMOD=1 or 2).

© 2023 Cadence Design Systems, Inc.

cgsp	0.0 F	Constant gate-to-source fringe capacitance (CGEOMOD=1).
cgdp	0.0 F	Constant gate-to-drain fringe capacitance (CGEOMOD=1).
cdsp	0.0 F	Constant drain-to-source fringe capacitance (All CGEOMOD).
nrs	0.0	Number of source diffusion squares.
nrd	0.0	Number of drain diffusion squares.
lrsd	(30*1.0e-9) m	Length of the source/drain.
nfinnom	1.0	Nominal number of fins per finger.
rsc	0.0 Ω	Source contact resistance.
rdc	0.0 Ω	Drain contact resistance.
xl	0 m	L offset for channel length due to mask/etch effect.
dtemp	0 C	Variability in device temperature.
trise	0 C	Variability in device temperature.
delvtrand	0 V	Variability in Vth.
u0mult	1	Variability in carrier mobility.
ids0mult	1	Variability in drain current for miscellaneous reasons.
mulid0	1	Variability in drain current for miscellaneous reasons (alias to ids0mult).
rtn_m	1	Number of od.

© 2023 Cadence Design Systems, Inc.

delvfb	0 V	Flatband voltage shift.
mulmu0	1	Mobility multiplier.
mulbeta	1	Beta multiplier.
isnoisy	yes	Should device generate noise.Possible values are no and yes.
covs	0	Constant g/s overlap capacitance.
covd	0	Constant g/d overlap capacitance.
igc0mult	1	Gate to channel current scale factor.
igb0mult	1	Gate to body current scale factor.
region	triode	Estimated operating region. %Z outputs the number (0-4) in a rawfile.Possible values are off, triode, sat and subth.
tgaa	5.0e-9 m	Thickness of individual GAA bodies.
tsus	2.0e-9 m	Separation between GAA bodies.
hpff	5.0e-9 m	Fin-height of parasitic finFET.
wgaa	6.0e-9 m	GAA body width.
dws1	0 m	Total width correction for 1st GAA body.
dach1	0 m^2	Total area correction for 1st GAA body.
dws2	0 m	Total width correction for 2nd GAA body.
dach2	0 m^2	Total area correction for 2nd GAA body.
dws3	0 m	Total width correction for 3rd GAA body.

© 2023 Cadence Design Systems, Inc.

dach3	0 m^2	Total area correction for 3rd GAA body.
ngaa	1	Number of GAA bodies per fin.
subbandmod	0	Switch for GAAFET quantum subband model (0: off; 1: on).
mobscmod	0	Switch for GAAFET geometry dependent mobility model (0: off; 1: on).
xw	0 m	W offset for GAA channel width due to mask/etch effect.
dws4	0 m	Total width correction for 4th GAA body.
dach4	0 m^2	Total area correction for 4th GAA body.
dws5	0 m	Total width correction for 5th GAA body.
dach5	0 m^2	Total area correction for 5th GAA body.
dws6	0 m	Total width correction for 6th GAA body.
dach6	0 m^2	Total area correction for 6th GAA body.

Model Syntax

```
model modelName bsimcmg parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

version	105.03	The model parameter "version" only accepts a real number value, like 106.1 for version=106.1.0. The available versions are 105.03, 105.031, 105.04, 106.0(106.0.0), 106.1(106.1.0), 107.0(107.0.0), 108.0(108.0.0), 110.0(110.0.0), 111.0(111.0.0), 111.1(111.1.0), 111.2(111.2.0) and 111.21(111.2.1).
binunit	1	Bin parameter unit selector. 1 for microns and 2 for meters.
l	(30*1.0e-9)	Designed Gate Length.
d	(40*1.0e-9)	Diameter of the cylinder (GEOMOD=3).
tfin	(15*1.0e-9)	Body (Fin) thickness.
fpitch	(80*1.0e-9)	Fin pitch.
nfin	1	Number of fins per finger.
ngcon	1	number of gate contact (1 or 2 sided).
aseo	0	Source to substrate overlap area through oxide.
adeo	0	Drain to substrate overlap area through oxide.
pseo	0	Perimeter of source to substrate overlap region.
pdeo	0	Perimeter of drain to substrate overlap region.
asej	0	Source junction area (BULKMOD=1 or 2).
adej	0	Drain junction area (BULKMOD=1 or 2).

© 2023 Cadence Design Systems, Inc.

psej	0	Source to substrate PN junction perimeter (BULKMOD=1 or 2).
pdej	0	Drain to substrate PN junction perimeter (BULKMOD=1 or 2).
cgsp	0.0	Constant gate-to-source fringe capacitance (CGEOMOD=1).
cgdp	0.0	Constant gate-to-drain fringe capacitance (CGEOMOD=1).
cdsp	0.0	Constant drain-to-source fringe capacitance (CGEOMOD=1).
nrs	0.0	Number of source diffusion squares.
nrd	0.0	Number of source diffusion squares.
lrsd	(30*1.0e-9)	Length of the source/drain.
delvtrand	0	Variability in Vth.
u0mult	1	Variability in carrier mobility.
ids0mult	1	Variability in Drain current for misc. reasons.
xl	0 m	L offset for channel length due to mask/etch effect.
type	n	Device doping type. p|0: ptype, n|1: ntype.Possible values are p and n.
devtype	n	Device doping type(the same usage as type). p|0: ptype, n|1: ntype.Possible values are p and n.
bulkmod	0	0: SOI multi-gate, 1: Bulk multi-gate, 2: for decoupled bulk multi-gate.

© 2023 Cadence Design Systems, Inc.

igc0mult	1	Gate to channel current scale factor.
igb0mult	1	Gate to body current scale factor.
coremod	0	0: Default surface potential algorithm, 1: Simplified (efficient) surface potential algorithm.
geomod	1	Structure selector. 0: Double gate, 1: Triple gate, 2: Quadruple gate, 3: Cylindrical gate, 4: Unified Fin Shape (since version 110.0.0).
mobmod	0	0: BSIM4-based mobility model, 1: PSP-based mobility model.
rdsmod	0	Internal s/d resistance model, 1: External s/d resistance model , 2: Both bias dependent and independent part of source/drain resistance internal.
asymmod	0	0: Asymmetry Model turned off - forward mode parameters used, 1: Asymmetry Model turned on.
igcmod	0	0: Turn off Igc, Igs and Igd, 1: Turn on Igc, Igs and Igd.
igbmod	0	0: Turn off Igb, 1: Turn on Igb.
gidlmod	0	0: Turn off GIDL/GISL current, 1: Turn on GIDL/GISL current, 2: Turn on GIDL/GISL with parasitic substrate component for GEOMOD = 2 or 3 or 5 and BULKMOD != 0.
iimod	0	0: No impact ionization current, 1: BSIM4-based model, 2: BSIMSOI-based model, 3: TSMC specific model.
nqsmod	0	0: NQS models turned off, 1: NQS gate resistance / gi node turned on, 2: NQS charge deficit model (BSIM4) / q node turned on, 3: //NQS charge segmentation model / Nseg nodes turned on.

© 2023 Cadence Design Systems, Inc.

shmod	0	0: No self-heating, 1: Self-heating turned on.
rgatemod	0	0: Gate electrode resistance / ge node turned off, 1: Gate electrode resistance / ge node turned on.
rgeomod	0	Geometry-dependent source/drain resistance. 0: RSH-based, 1: Holistic.
cgeomod	0	Geometry-dependent parasitic capacitance,model selector.
capmod	0	0: No accumulation capacitance, 1: Accumulation capacitance included. Available only for BULKMOD = 1.
sh_warn	0	0: Self-Heating Warnings disabled; 1: Self-Heating Warnings enabled.
igclamp	1	0: Gate Current clamps disabled; 1: Gate Current Clamps enabled.
fnmod	0	0: Old flicker noise model; 1: New flicker noise model.
lint	0	Length reduction parameter (dopant diffusion effect).
ll	0	Length reduction parameter (dopant diffusion effect).
lln	1	Length reduction parameter (dopant diffusion effect).
dlc	0	Delta L for C-V model.
dlcacc	0	Delta L for C-V model in accumulation region (CAPMOD=1, BULKMOD=1 or 2).
dlbin	0	Delta L for Binning.

© 2023 Cadence Design Systems, Inc.

`llc`	`0`	Length reduction parameter (dopant diffusion effect).
`eot`	`(1.0*1.0e-9) m`	Equivalent oxide thickness.
`toxp`	`(1.2*1.0e-9) m`	Physical oxide thickness.
`eotbox`	`(140*1.0e-9) m`	Equivalent oxide thickness of the buried oxide (SOI FinFET) or STI (bulk FinFET).
`hfin`	`(30*1.0e-9) m`	FinFET height.
`fech`	`1`	End-channel factor, for different orientation/shape.
`deltaw`	`0`	Change of effective width due to shape of fin/cylinder.
`fechcv`	`1`	CV end-channel factor, for different orientation/shape.
`deltawcv`	`0`	CV change of effective width due to shape of fin/cylinder.
`nbody`	`1e22`	Channel (body) doping.
`nsd`	`2e26 1/m`^{3}	Source/drain active doping concentration.
`phig`	`4.61 eV`	Gate workfunction.
`epsrox`	`3.9`	Relative dielectric constant of the gate dielectric.
`epsrsub`	`11.9`	Relative dielectric constant of the channel material.
`easub`	`4.05 eV`	Electron affinity of substrate.

© 2023 Cadence Design Systems, Inc.

ni0sub	1.1e16 $1/m^3$	Intrinsic carrier constant at 300.15K.
bg0sub	1.12 eV	Band gap of substrate at 300.15K.
nc0sub	2.86e25 $1/m^3$	Conduction band density of states.
ngate	0.0	Parameter for poly gate doping. For metal gate please set NGATE = 0.
cit	0.0	Parameter for interface trap.
cdsc	7e-3	Coupling capacitance between S/D and channel.
cdscd	7e-3	Drain-bias sensitivity of CDS.
cdscdr	cdscd	Reverse-mode drain-bias sensitivity of CDSC (Experimental).
dvt0	0.0	SCE exponent coefficient, after binning should be in (0:inf).
dvt1	0.60	SCE exponent coefficient.
phin	0.05 V	Non-uniform vertical doping effect on surface potential.
eta0	0.60	DIBL coefficient.
eta0r	eta0	Reverse-mode DIBL coefficient (Experimental).
dsub	1.06	DIBL exponent coefficient.
k1rsce	0.0	K1 for reverse short channel effect calculation.
lpe0	(5.0*1.0 e-9)	Equivalent length of pocket region at zero bias.

© 2023 Cadence Design Systems, Inc.

dvtshift	0	Vth shift handle.
k0	0.0	Lateral NUD voltage parameter, V.
k0si	1.0	Correction factor for strong inversion, used in Mnud, after binning should be from (0:inf).
phibe	0.7 V	Body effect voltage parameter, after binning should be from [0.2:1.2].
k1	0.0	Body effect coefficient for sub-threshold region.
k1si	1.0	Correction factor for strong inversion, used in Mob.
k1sat	0.0	Correction factor for K1 in saturation (high Vds).
dvtb	0.60	Body effect roll-off coefficient.
lpeb	0.0	Lateral non-uniform doping effect on K1.
qmfactor	0.0	Prefactor + switch for QM Vth correction.
qmtceniv	0.0	Prefactor + switch for QM Width correction for IV.
qmtcencv	0.0	Prefactor + switch for QM Width and Toxeff correction for CV.
qmtcencva	0.0	Prefactor + switch for QM Width and Toxeff correction for CV (accumulation region).
aqmtcen	0.0	Parameter for geometric dependence of Tcen on R/TFIN/HFIN.
bqmtcen	12.0e-9	Parameter for geometric dependence of Tcen on R/TFIN/HFIN.
etaqm	0.54	Bulk charge coefficient for Tcen.

© 2023 Cadence Design Systems, Inc.

qm0	1.00e-3	Knee-Point for Tcen in inversion (Charge normalized to Cox).
pqm	0.66	Slope of normalized Tcen in inversion.
qm0acc	1.00e-3	Knee-Point for Tcen in accumulation (Charge normalized to Cox).
pqmacc	0.66	Slope of normalized Tcen in accumulation.
alphaqm	0.66	Slope of normalized Tcen in strong inversion/ accumulation.
vsat	85000 m/s	Saturation velocity for the saturation region.
avsat	0.0	Pre-exponential coefficient for VSAT.
bvsat	100.0e-9	Exponential coefficient for VSAT.
vsat1	vsat	Velocity saturation parameter for I_on degradation - forward mode.
vsat1r	vsat1	Velocity saturation parameter for I_on degradation - reverse mode.
avsat1	avsat	Pre-exponential coefficient for VSAT1.
bvsat1	bvsat	Exponential coefficient for VSAT1.
deltavsat	1.0	Velocity saturation parameter in the linear region.
psat	2.0	Velocity saturation exponent for C-V.
apsat	0.0	Pre-exponential coefficient for PSAT.
bpsat	1.0	Exponential coefficient for PSAT.
ksativ	1.0	Parameter for long channel Vdsat.

© 2023 Cadence Design Systems, Inc.

vsatcv	vsat	Velocity saturation parameter for CV.
avsatcv	avsat	Length dependence of VSATCV.
bvsatcv	bvsat	Length dependence of VSATCV.
mexp	4	Smoothing function factor for Vdsat.
amexp	0.0	Length dependence of MEXP.
bmexp	1.0	Length dependence of MEXP.
ptwg	0.0	Gmsat degradation parameter - forward mode.
ptwgr	ptwg	Gmsat degradation parameter - reverse mode.
aptwg	0.0	Length dependence of PTWG.
bptwg	100.0e-9	Length dependence of PTWG.
thetasat	2.0	Velocity saturation parameter.
athetasat	0.0	Length dependence of THETASAT.
bthetasat	100.0e-9	Length dependence of THETASAT.
u0	0.03 $m^2/V\ s$	Shared: low-field mobility.
etamob	2.0	Effective field parameter.
up	0 μm^LPA	Shared: Mobility L coefficient.
lpa	1.0	Shared: Mobility L power coefficient.
ua	0.3	MOD0: Mobility reduction coefficient.
aua	0.0	MOD0: Length dependence of UA.

© 2023 Cadence Design Systems, Inc.

bua	100.0e-9	Length dependence of UA.
uc	0.0	Body effect for mobility degradation parameter - BULKMOD=1 or 2.
eu	2.5	MOD0: Mobility reduction exponent.
aeu	0.0	Length dependence of EU.
beu	100.0e-9	Length dependence of EU.
ud	0.0	MOD0: Coulomb scattering parameter.
aud	0.0	MOD0: Length dependence of UD.
bud	50.0e-9	Length dependence of UD.
ucs	1.0	MOD0: Coulomb scattering parameter.
mue	1.2	MOD1: Mobility reduction coefficient.
thetamu	1.0	MOD1: Mobility reduction exponent.
athetamu	0.0	MOD1: Length dependence of THETAMU.
bthetamu	100.0e-9	Length dependence of THETAMU.
cs	0	MOD1: Coulomb scattering parameter.
acs	0.0	MOD1: Length dependence of CS.
bcs	50.0e-9	Length dependence of CS.
pclm	0.013	CLM prefactor.
apclm	0.0	Length dependence of PCLM.
bpclm	100.0e-9	Length dependence of PCLM.

© 2023 Cadence Design Systems, Inc.

pclmg	0.0	CLM prefactor gate voltage dependence.
vasat	0.2	CLM log dependence parameter.
pclmcv	pclm	CLM parameter for short channel CV.
pclmgcv	0.0	CLM prefactor gate voltage dependence.
vasatcv	0.2	CLM log dependence parameter.
a1	0.0	Non-saturation effect parameter for strong inversion region.
a2	0.0	Non-saturation effect parameter for moderate inversion region.
rdswmin	0.0 ohm(μm)^WR	S/D extension resistance per unit width at high Vgs.
rdsw	100.0 ohm(μm)^WR	Zero bias S/D extension resistance per unit width.
ardsw	0.0	Geometrical scaling of RDSW.
brdsw	100.0e-9	Geometrical scaling of RDSW.
rswmin	0.0	Source resistance for RDSMOD=1.
rsw	50.0	Zero bias source resistance for RDSMOD=1.
arsw	0.0	Geometrical scaling of RSW.
brsw	100.0e-9	Geometrical scaling of RSW.
rdwmin	0.0	Drain resistance for RDSMOD=1.
rdw	50.0	Zero bias drain resistance for RDSMOD=1.

© 2023 Cadence Design Systems, Inc.

ardw	0.0	Geometrical scaling of RDW.
brdw	100.0e-9	Geometrical scaling of RDW.
prwg	0 1/V	Gate bias dependence of S/D extension resistance.
rsdr	0.0 V^(-prsdr)	Source side drift resistance parameter - forward mode.
rsdrr	rsdr V^(-prsdr)	Source side drift resistance parameter - reverse mode.
rddr	rsdr V^(-prddr)	Drain side drift resistance parameter - forward mode.
rddrr	rddr V^(-prddr)	Drain side drift resistance parameter - reverse mode.
prsdr	1.0	Source side quasi-saturation parameter.
prddr	prsdr	Drain side quasi-saturation parameter.
prwgs	0.0 1/V	Gate bias dependence of source extension resistance.
prwgd	prwgs 1/V	Gate bias dependence of drain extension resistance.
wr	1.0	W dependence parameter of S/D extension resistance.
trsdr	0.0 /K	Temperature dependence of RSDR.
trddr	trsdr /K	Temperature dependence of RDDR.
rgext	0.0	Effective gate electrode external resistance.

© 2023 Cadence Design Systems, Inc.

rgfin	1.0e-3	Effective gate electrode per finger per fin resistance.
rshs	0.0	Source-side sheet resistance.
rshd	rshs	Drain-side sheet resistance.
hepi	(10.0*1.0e-9)	Height of the raised source/drain on top of the fin.
tsili	(10.0*1.0e-9)	Thickness of the silicide on top of the raised source/drain.
rhoc	1.0e-12	Contact resistivity at the silicon/silicide interface.
rhorsd	1.0	Average resistivity of silicon in the raised source/drain region.
rhoext	1.0	Average resistivity of silicon in the fin extension region.
cratio	0.5	Ratio of the corner area filled with silicon to the total corner area.
deltaprsd	0.0	Change in silicon/silicide interface length due to non-rectangular epi.
sdterm	0	Indicator of whether the source/drain are terminated with silicide.
lsp	0.2*(L + XL)	Thickness of the gate sidewall spacer.
ldg	5.0e-9	Lateral diffusion gradient in the fin extension region.
epsrsp	3.9	Relative dielectric constant of the spacer.
tgate	(30.0*1.0e-9)	Gate height on top of the hard mask.

© 2023 Cadence Design Systems, Inc.

tmask	(30.0*1.0e-9)	Height of hard mask on top of the fin.
asiliend	0.0	Extra silicide cross-sectional area at the two ends of the FinFET.
arsdend	0.0	Extra raised source/drain cross-sectional area at the two ends of the FiinFET.
prsdend	0.0	Extra silicon/silicide interface perimeter at the two ends of the FinFET.
nsde	2e25	Source/drain active doping concentration at Leff edge.
rgeoa	1.0	Fitting parameter for RGEOMOD=1.
rgeob	0.0	Fitting parameter for RGEOMOD=1.
rgeoc	0.0	Fitting parameter for RGEOMOD=1.
rgeod	0.0	Fitting parameter for RGEOMOD=1.
rgeoe	0.0	Fitting parameter for RGEOMOD=1.
cgeoa	1.0	Fitting parameter for CGEOMOD=2 and 3.
cgeob	0.0	Fitting parameter for CGEOMOD=2 and 3.
cgeoc	0.0	Fitting parameter for CGEOMOD=2 and 3.
cgeod	0.0	Fitting parameter for CGEOMOD=2 and 3.
cgeoe	1.0	Fitting parameter for CGEOMOD=2 and 3.
pdibl1	1.30	DIBL output conductance parameter - forward mode.

© 2023 Cadence Design Systems, Inc.

pdibl1r	pdibl1	DIBL output conductance parameter - reverse mode.
pdibl2	2.0e-4	DIBL output conductance parameter.
drout	1.06	L dependence of DIBL effect on Rout.
pvag	1.0	Vg dependence on early voltage.
aigbinv	1.11e-2	Parameter for Igb in inversion.
bigbinv	9.49e-4	Parameter for Igb in inversion.
cigbinv	6.00e-3	Parameter for Igb in inversion.
eigbinv	1.1	Parameter for Igb in inversion.
nigbinv	3.0	Parameter for Igb in inversion.
aigbacc	1.36e-2	Parameter for Igb in accumulation.
bigbacc	1.71e-3	Parameter for Igb in accumulation.
cigbacc	7.5e-2	Parameter for Igb in accumulation.
nigbacc	1.0	Parameter for Igb in accumulation.
igbinvclamp	1.0e-3	Clamping value of the exponent for Igb in inversion.
igbaccclamp	1.0e-3	Clamping value of the exponent for Igb in accumulation.
igcinvclamp	5.0e-4	Clamping value of the exponent for Igc in inversion.
aigc	1.36e-2	Parameter for Igc in inversion.
bigc	1.71e-3	Parameter for Igc in inversion.

© 2023 Cadence Design Systems, Inc.

cigc	0.075	Parameter for Igc in inversion.
nigc	1.0	Parameter for Igc in inversion.
pigcd	1.0	Parameter for Igc partition.
dlcigs	0	Delta L for Igs model.
aigs	1.36e-2	Parameter for Igs in inversion.
bigs	1.71e-3	Parameter for Igs in inversion.
cigs	0.075	Parameter for Igs in inversion.
dlcigd	dlcigs	Delta L for Igd model.
aigd	aigs ((F s^2/ g)^0.5) m^-1	Parameter for Igd in inversion.
bigd	bigs ((F s^2/ g)^0.5) (m V)^-1	Parameter for Igd in inversion.
cigd	cigs /V	Parameter for Igd in inversion.
toxref	(1.2*1.0e-9) m	Target tox value.
ntox	1.0	Exponent for Tox ratio.
poxedge	1.0	Factor for the gate edge Tox.
agisl	(6.055*1.0e-12) Ω	Pre-exponential coefficient for GISL.

© 2023 Cadence Design Systems, Inc.

bgisl	0.3e9 V/m	Exponential coefficient for GISL.
cgisl	0.5 V^3	Parameter for body-effect of GISL.
egisl	0.2 V	Band bending parameter for GISL.
pgisl	1.0	Parameter for body-bias effect on GISL.
agidl	agisl Ω	Pre-exponential coefficient for GIDL.
bgidl	bgisl V/m	Exponential coefficient for GIDL.
cgidl	cgisl V^3	Parameter for body-effect of GIDL.
egidl	egisl V	Band bending parameter for GIDL.
pgidl	pgisl	Parameter for body-bias effect on GIDL.
alpha0	0.0 m/V	First parameter of Iii.
alpha1	0.0 1/V	L Scaling parameter of Iii.
beta0	0.0 1/V	Vds-dependent parameter of Iii.
alphaii	0.0	Pre-exponential constant of Iii.
betaii0	0.0 1/V	Vds-dependent parameter of Iii.
betaii1	0.0	Vds-dependent parameter of Iii.
betaii2	0.1 V	Vds-dependent parameter of Iii.
esatii	1.0e7 V/m	Saturation channel E-Field for Iii.
lii	0.5E-9 V m	Channel length dependent parameter of Iii.

© 2023 Cadence Design Systems, Inc.

sii0	0.5 1/V	Vgs dependent parameter of Iii.
sii1	0.1 1/V	First Vgs-dependent parameter of Iii.
sii2	0.0	Sencond Vgs-dependent parameter of Iii.
siid	0.0 1/V	Third Vds-dependent parameter of Iii.
eotacc	eot m	Equivalent oxide thickness for accumulation region.
delvfbacc	0.0	Change in Flatband Voltage; Vfb_accumulation-Vfb_inversion.
cfs	2.5e-11 F/m	Outer fringe capacitance (source side).
cfd	cfs F/m	Outer fringe capacitance (drain side).
covs	2.5e-11	Constant g/s overlap capacitance. Default value is 0.0 since version 107.0.0.
covd	covs	Constant g/d overlap capacitance.
cgso	0.0 F/m	Non-LDD region source-gate overlap capacitance per unit channel width.
cgdo	cgso F/m	Non-LDD region drain-gate overlap capacitance per unit channel width.
cgsl	0.0 F/m	Overlap capacitance between gate and lightly-doped source region (for GEOMOD = 0, 2).
cgdl	cgsl F/m	Overlap capacitance between gate and lightly-doped drain region (for GEOMOD = 0, 2).
ckappas	0.6 V	Coefficient of bias-dependent overlap capacitance for the source side (for CGEOMOD = 0, 2).

© 2023 Cadence Design Systems, Inc.

ckappad	ckappasV	Coefficient of bias-dependent overlap capacitance for the drain side (for CGEOMOD = 0, 2).
cgbo	0.0 F/m	Gate-to-substrate overlap capacitance per unit channel length per finger per NGCON.
cgbn	0.0 F/m	Gate-to-substrate overlap capacitance per unit channel length per fin per finger.
cgbl	0.0 F/m	Bias dependent component of gate-to-substrate overlap cap per unit channel length per fin per finger.
ckappab	0.6	Coefficient for gate-to-substrate bias-dependent overlap capacitance (for BULKMOD = 1).
csdesw	0.0 F/m	Coefficient for source/drain-to-substrate sidewall cap.
cjs	5.0e-4 F/m^2	Unit area source-side junction capacitance at zero bias.
cjd	cjs F/m^2	Unit area drain-side junction capacitance at zero bias.
cjsws	5.0e-10 F/m	Unit length source-side sidewall junction capacitance at zero bias.
cjswd	cjsws F/m	Unit length drain-side sidewall junction capacitance at zero bias.
cjswgs	0.0 F/m	Unit length source-side gate sidewall junction capacitance at zero bias.
cjswgd	cjswgs F/m	Unit length drain-side gate sidewall junction capacitance at zero bias.
pbs	1.0 V	Source-side bulk junction built-in potential.

© 2023 Cadence Design Systems, Inc.

pbd	pbs V	Drain-side bulk junction built-in potential.
pbsws	1.0 V	Built-in potential for source-side sidewall junction capacitance.
pbswd	pbsws V	Built-in potential for drain-side sidewall junction capacitance.
pbswgs	pbsws V	Built-in potential for source-side gate sidewall junction capacitance.
pbswgd	pbswgs V	Built-in potential for drain-side gate sidewall junction capacitance.
mjs	0.5	Source bottom junction capacitance grading coefficient.
mjd	mjs	Drain bottom junction capacitance grading coefficient.
mjsws	0.33	Source sidewall junction capacitance grading coefficient.
mjswd	mjsws	Drain sidewall junction capacitance grading coefficient.
mjswgs	mjsws	Source-side gate sidewall junction capacitance grading coefficient.
mjswgd	mjswgs	Drain-side gate sidewall junction capacitance grading coefficient.
sjs	0.0	Constant for source-side two-step second junction capacitance.
sjd	sjs	Constant for drain-side two-step second junction capacitance.

© 2023 Cadence Design Systems, Inc.

sjsws	0.0	Constant for sidewall two-step second junction capacitance (source-side).
sjswd	sjsws	Constant for sidewall two-step second junction capacitance (drain-side).
sjswgs	0.0	Constant for gate sidewall two-step second junction capacitance (source-side).
sjswgd	sjswgs	Constant for gate sidewall two-step second junction capacitance (drain-side).
mjs2	0.125	Source bottom two-step second junction capacitance grading coefficient.
mjd2	mjs2	Drain bottom two-step second junction capacitance grading coefficient.
mjsws2	0.083	Isolation-edge sidewall two-step second junction capacitance grading coefficient (source-side).
mjswd2	mjsws2	Isolation-edge sidewall two-step second junction capacitance grading coefficient (drain-side).
mjswgs2	mjsws2	Gate-edge sidewall two-step second junction capacitance grading coefficient (source-side).
mjswgd2	mjswgs2	Gate-edge sidewall two-step second junction capacitance grading coefficient (drain-side).
jss	1.0e-4 A/m^2	Bottom source junction reverse saturation current density.
jsd	jss A/m^2	Bottom drain junction reverse saturation current density.
jsws	0.0 A/m	Unit length reverse saturation current for sidewall source junction.

© 2023 Cadence Design Systems, Inc.

`jswd`	`jsws A/m`	Unit length reverse saturation current for sidewall drain junction.
`jswgs`	`0.0 A/m`	Unit length reverse saturation current for gate-edge sidewall source junction.
`jswgd`	`jswgs A/m`	Unit length reverse saturation current for gate-edge sidewall drain junction.
`njs`	`1.0`	Source junction emission coefficient.
`njd`	`njs`	Drain junction emission coefficient.
`ijthsfwd`	`0.1 A`	Forward source diode breakdown limiting current.
`ijthdfwd`	`ijthsfwd A`	Forward drain diode breakdown limiting current.
`ijthsrev`	`0.1 A`	Reverse source diode breakdown limiting current.
`ijthdrev`	`ijthsrev A`	Reverse drain diode breakdown limiting current.
`bvs`	`10.0 V`	Source diode breakdown voltage.
`bvd`	`bvs V`	Drain diode breakdown voltage.
`xjbvs`	`1.0`	Fitting parameter for source diode breakdown current.
`xjbvd`	`xjbvs`	Fitting parameter for drain diode breakdown current.
`jtss`	`0.0 A/m`^{2}	Bottom source junction trap-assisted saturation current density.
`jtsd`	`jtss A/m`^{2}	Bottom drain junction trap-assisted saturation current density.

© 2023 Cadence Design Systems, Inc.

jtssws	0.0 A/m	Unit length trap-assisted saturation current for isolation-edge source side-wall junction.
jtsswd	jtssws A/m	Unit length trap-assisted saturation current for isolation-edge drain side-wall junction.
jtsswgs	0.0 A/m	Unit length trap-assisted saturation current for gate-edge source sidewall junction.
jtsswgd	jtsswgs A/m	Unit length trap-assisted saturation current for gate-edge drain sidewall junction.
jtweff	0.0	Trap-assisted tunneling current width dependence.
njts	20.0	Non-ideality factor for JTSS.
njtsd	njts	Non-ideality factor for JTSD.
njtssw	20.0	Non-ideality factor for JTSSWS.
njtsswd	njtssw	Non-ideality factor for JTSSWD.
njtsswg	20.0	Non-ideality factor for JTSSWGS.
njtsswgd	njtsswg	Non-ideality factor for JTSSWGD.
vtss	10.0	Bottom source junction trap-assisted current voltage dependent parameter.
vtsd	vtss	Bottom drain junction trap-assisted current voltage dependent parameter.
vtssws	10.0	Unit length trap-assisted current voltage dependent parameter for isolation-edge source sidewall junction.
vtsswd	vtssws	Unit length trap-assisted current voltage dependent parameter for isolation-edge drain sidewall junction.

© 2023 Cadence Design Systems, Inc.

vtsswgs	10.0	Unit length trap-assisted current voltage dependent parameter for gate-edge source sidewall junction.
vtsswgd	vtsswgs	Unit length trap-assisted current voltage dependent parameter for gate-edge drain sidewall junction.
lintigen	0	Lint for thermal generation current.
ntgen	1.0	Thermal generation current parameter.
aigen	0	Thermal generation current parameter.
bigen	0	Thermal generation current parameter.
xrcrg1	12.0	Parameter for non quasi-static gate resistance NQSMOD = 1 and NQSMOD = 2.
xrcrg2	1.0	Parameter for non quasi-static gate resistance NQSMOD = 1 and NQSMOD = 2.
nseg	4	Number of segments for NQSMOD=3 (3,5 & 10 supported).
ef	1.0	Flicker noise frequency exponent.
em	4.1e7	Flicker noise parameter.
noia	6.250e+39	Flicker noise parameter.
noib	3.125e+24	Flicker noise parameter.
noic	8.750e+07	Flicker noise parameter.
rtnmod	0	0: RTN Mode off, 1: RTN Mode on.
rtnfmod	0	0: RTN 1ovf Mode off, 1: RTN 1ovf Mode on.

© 2023 Cadence Design Systems, Inc.

rtnmcmod	0	0: RTN MC Mode off, 1: RTN MC Mode on.
rtnmcloop	0	0: RTN loop MC Mode off, 1: RTN loop MC Mode on.
rtn_mc	0	RTN random number.
rtnfc	10000	RTN corner frequency (Hz).
rtnamp	0	RTN amplitude (V).
rtnpr	100	RTN probability rate (%).
rtnfcmc	0	RTN corner frequency 3-sigma (log).
rtnampmc	0	RTN amplitude 3-sigma (ratio).
fnoik	0.0	TMEMOD noise parameter.
kfrs	0.0	TMEMOD noise parameter.
kfrd	0.0	TMEMOD noise parameter.
kfds	0.0	TMEMOD noise parameter.
afrs	2.0	TMEMOD noise parameter.
afrd	2.0	TMEMOD noise parameter.
afds	2.0	TMEMOD noise parameter.
efrs	1.0	TMEMOD noise parameter.
efrd	1.0	TMEMOD noise parameter.
efds	1.0	TMEMOD noise parameter.
af_hv	2.0	Flicker noise parameter.

© 2023 Cadence Design Systems, Inc.

kf_hv	0	Flicker noise parameter.
lintnoi	0.0	L offset for flicker noise calculation.
noia2	6.250e+39	Flicker noise parameter for sub-threshold region.
smooth	2.0	Smoothing Parameter.
mpower	1.2	Sub-threshold to strong inversion transition slope Parameter.
noiua	3.0	Noise parameter.
qsref	5.0e-2	Charge at threshold condition.
ntnoi	1.0	Thermal noise parameter.
tnoimod	0	Before version 110.0.0, 0: charge-based, 1: holistic thermal noise based on BSIM4 noise model, 2: correlated noise. Since version 110.0.0, 0: charge-based, 1: correlated thermal noise model.
fnoimod	0	0: Enhanced Mode off (standard BSIMCMG model), 91: (TSMC HV flicker noise model).
tnoia	1.5	Thermal noise parameter.
tnoib	3.5	Thermal noise parameter.
rnoia	0.577	Thermal noise parameter.
rnoib	0.37	Thermal noise parameter.
nidsmin	1.0e-9	Lower limit of the clamping function in noise calculation.
tnom	27.0 C	Temperature at which the model is extracted.

© 2023 Cadence Design Systems, Inc.

tbgasub	7.02e-4 eV/C	Bandgap temperature coefficient.
tbgbsub	1108.0 C	Bandgap temperature coefficient.
kt1	0.0 V	Vth temperature coefficient.
kt1l	0.0 m V	Vth temperature L coefficient.
tss	0.0 1/C	Swing temperature coefficient.
ute	0.0	Mobility temperature coefficient.
utl	(-1.5e-3)	Mobility temperature coefficient.
emobt	0.0	Mobility temperature coefficient.
ua1	1.032e-3	Mobility temperature coefficient.
uc1	0.056e-9	Mobility temperature coefficient.
ud1	0.0	Mobility temperature coefficient.
ucste	(-4.775e-3)	Mobility temperature coefficient.
stthetamu	1.5	Mobility temperature coefficient.
stmue	0.0	Mobility temperature coefficient.
stcs	0.0	Mobility temperature coefficient.
at	(-1.56e-3)	Saturation velocity temperature coefficient.
tmexp	0.0	Temperature coefficient for Vdseff.

© 2023 Cadence Design Systems, Inc.

dvsatclamp	0.01 m	Minimum clamp on Dvsat.
dmobclamp	0.01 m	Minimum clamp on Dmob.
ptwgt	0.004	Temperature dependence of PTWG.
abulkmod	0	0: Original BSIM-CMG CV model; 1: TSMC CV enhancement model.
abulkcon	(-1.0e-6)	Coefficient for TSMC CV enhancement model, should not be 0.
voffmod	0	0: Original BSIM-CMG lateral NUD effect model; 1: TSMC lateral NUD effect enhancement model.
a0cv	0.0	
agscv	0.0	
mexpcv	4.0	
amexpcv	0.0	
bmexpcv	1.0	
tmexpcv	0.0	
k1sisat	0.0	
k1sisat1	0.0	
ldvtp0	0.0 m	L-term of DVTP0.
ndvtp0	0.0	
pdvtp0	0.0 m	P-term of DVTP0.
wdvtp0	0.0 m	W-term of DVTP0.

© 2023 Cadence Design Systems, Inc.

p2dvtp0	0.0 m^2	WL-term of DVTP0.
ldvtp1	0.0 m	L-term of DVTP1.
ndvtp1	0.0	
pdvtp1	0.0 m	P-term of DVTP1.
wdvtp1	0.0 m	W-term of DVTP1.
p2dvtp1	0.0 m^2	WL-term of DVTP1.
stthetasat	0.0217	Saturation velocity temperature coefficient.
prt	0.001 /K	Series resistance temperature coefficient.
iit	(-0.5)	Impact ionization temperature dependence, IIMOD=1.
tii	0.0	Impact ionization temperature dependence, IIMOD=2.
tgidl	(-0.003)	GIDL/GISL temperature dependence.
igt	2.5	Gate current temperature dependence.
tcj	0.0	Temperature coefficient for CJS/CJD.
tcjsw	0.0	Temperature coefficient for CJSWS/CJSWD.
tcjswg	0.0	Temperature coefficient for CJSWGS/CJSWGD.
tpb	0.0	Temperature coefficient for PBS/PBD.
tpbsw	0.0	Temperature coefficient for PBSWS/PBSW.
tpbswg	0.0	Temperature coefficient for PBSWGS/PBSWGD.

© 2023 Cadence Design Systems, Inc.

xtis	3.0	Source junction current temperature exponent.
xtid	xtis	Drain junction current temperature exponent.
xtss	0.02	Power dependence of JTSS on temperature.
xtsd	xtss	Power dependence of JTSD on temperature.
xtssws	0.02	Power dependence of JTSSWS on temperature.
xtsswd	xtssws	Power dependence of JTSSWG on temperature.
xtsswgs	0.02	Power dependence of JTSSWGS on temperature.
xtsswgd	xtsswgs	Power dependence of JTSSWGD on temperature.
tnjts	0.0	Temperature coefficient for NJTS.
tnjtsd	tnjts	Temperature coefficient for NJTSD.
tnjtssw	0.0	Temperature coefficient for NJTSSW.
tnjtsswd	tnjtssw	Temperature coefficient for NJTSSWD.
tnjtsswg	0.0	Temperature coefficient for NJTSSWG.
tnjtsswgd	tnjtsswg	Temperature coefficient for NJTSSWGD.
rth0	0.01 ohm m K/W	Thermal resistance for self-heating calculation.
cth0	1.0E-05 W s/m/K	Thermal capacitance for self-heating calculation.
wth0	0.0	Width-dependence coefficient for self-heating calculation.
toxg	toxp m	Oxide thickness for gate current model.

© 2023 Cadence Design Systems, Inc.

k01	0.0 V	Temperature dependence of lateral NUD voltage parameter.
k0si1	0.0 1/K	Temperature dependence of K0SI.
k1si1	0.0 1/K	Temperature dependence of K1SI.
k11	0.0	Temperature dependence of K1.
k1sat1	0.0	Temperature dependence of K1SAT1.
rcvfac	1.0	Series resistance correction factor for CV.
a11	0.0	Temperature dependence of A1.
a21	0.0	Temperature dependence of A2.
aigbinv1	0	Parameter for Igb in inversion.
aigbacc1	0	Parameter for Igb in accumulation.
aigc1	0	Parameter for Igc in inversion.
aigs1	0	Parameter for Igs in inversion.
aigd1	aigs1 ((F s^2/ g)^0.5) m^-1/K	Parameter for Igd in inversion.
alpha01	0.0 m/V/ C	Temperature dependence of ALPHA0.
alpha11	0.0 1/V/ C	Temperature dependence ALPHA1.
alphaii0	0.0 m/V	First parameter of Iii for IIMOD=2.

© 2023 Cadence Design Systems, Inc.

alphaii01	0.0 m/V/C	Temperature dependence of ALPHAII0.
alphaii1	0.0 1/V	L scaling parameter of Iii for IIMOD=2.
alphaii11	0.0 1/V/C	Temperature dependence of ALPHAII1.
imin	1.0E-15	Parameter for Vgs clamping for inversion region calculated in accumulation.
deltavsatcv	deltavsat	Parameter for VSATCV.
psatcv	psat	Velocity saturation exponent for C-V.
apsatcv	apsat	Length dependence of PVSATCV.
bpsatcv	bpsat	Length dependence of PVSATCV.
cgeo1sw	0	For CGEOMOD=1 only, this switch enables the parameters COVS, COVD, CGSP,and CGDP to be in F per fin, per gate-finger, per unit channel width.
nbodyn1	0	NFIN dependence of channel (body) doping.
nbodyn2	1.0e5	NFIN dependence of channel (body) doping.
phigl	0 eV/m	Length dependence of gate workfunction.
phign1	0	NFIN dependence of gate workfunction.
phign2	1.0e5	NFIN dependence of gate workfunction.
cdscn1	0	NFIN dependence of CDSC.
cdscn2	1.0e5	NFIN dependence of CDSC.
cdscdn1	0	NFIN dependence of CDSCD.

© 2023 Cadence Design Systems, Inc.

cdscdn2	1.0e5	NFIN dependence of CDSCD.
cdscdrn1	cdscdn1	NFIN dependence of CDSCD.
cdscdrn2	cdscdn2	NFIN dependence of CDSCD.
dvt1ss	dvt1	Subthreshold swing exponent coefficient; after binning should be in (0:inf).
eta0n1	0	NFIN dependence of ETA0.
eta0n2	1.0e5	NFIN dependence of ETA0.
teta0	0.0 1/K	Temperature dependence of DIBL coefficient.
teta0r	teta0 1/K	Temperature dependence of Reverse-mode DIBL coefficient.
dvtp0	0	Coefficient for drain-induced Vth shift (DITS).
dvtp1	0	DITS exponent coefficient.
vsatn1	0	NFIN dependence of VSAT.
vsatn2	1.0e5	NFIN dependence of VSAT.
vsat1n1	vsatn1	NFIN dependence of VSAT1.
vsat1n2	vsatn2	NFIN dependence of VSAT1.
vsat1rn1	vsat1n1	NFIN dependence of VSAT1R.
vsat1rn2	vsat1n2	NFIN dependence of VSAT1R.
mexpr	mexp	Coefficient for Vdseff.
amexpr	amexp	Coefficient for Vdseff.

© 2023 Cadence Design Systems, Inc.

bmexpr	bmexp	Coefficient for Vdseff.
tmexpr	tmexp	Coefficient for Vdseff.
u0n1	0	NFIN dependence of U0.
u0n2	1.0e5	NFIN dependence of U0.
chargewf	0	Average Channel Charge Weighting Factor, +1:source-side, 0:middle, -1:drain-side.
minr	0.001 Ω	minr is the value below which the simulator expects elimination of source/drain resistance and it will improve simulation efficiency without significantly altering the results.
compatible	spectre	Compatibility parameters.Possible values are spectre, spice2, spice3, cdsspice, hspice, spiceplus, eldo, sspice and mica.
vthmod	0	Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'.Possible values are std, vthcc and vthcc_ext.
ivth	0.0 A	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
ivthw	0.0 m	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
ivthl	0.0 m	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
ivth_vdsmin	0.05 V	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.

© 2023 Cadence Design Systems, Inc.

vdsatmod	0	Vdsat output selector. Possible values are std, gds, and slow_gds.Possible values are std, gds and slow_gds.
vdsat_c	0.0	Coefficient for Gds based Vdsat.
vdsat_vdl	0.0	Coefficient for Gds based Vdsat.
vdsat_vadj	0.0	Coefficient for Gds based Vdsat.
tfindrw	1e-8	Drawn fin thickness.
ithx	1e-8	Vth current parameter.
im	0	Flag for the terminal current used in Vth calculation. 0 for electrical Is, 1for electrical Id and 2 for electrical (Id+Is)/2.
dlthx	0	Length shift in Vth calculation.
tempmod	0	Temperature dependency.
thetasce	0	Vth roll-off length dependence. If defined by user, will overwrite Theta_SCE in the code.
thetadibl	0	DIBL length dependence. If defined by user, will overwrite Theta_DIBL in the code.
thetasw	0	Subthreshold swing length dependence. If defined by user, will overwrite Theta_SW in the code.
nvtm	0	Subthreshold swing factor multiplied by Vtm. If defined by user, will overwrite nVtm in the code.
atcv	at	AT for CV.
citr	0.0	Parameter for interface trap in reverse mode for asymmetric model.

© 2023 Cadence Design Systems, Inc.

dvtshiftr	dvtshift	Vth shift handle for asymmetric mode.
vsatr	vsat m/s	Saturation velocity for the saturation region in the reverse mode.
vsatrn1	vsatn1	NFIN dependence of VSATR.
vsatrn2	vsatn2	NFIN dependence of VSATR.
ksativr	ksativ	KSATIV in asymmetric mode.
u0r	u0	U0 in reverse mode.
upr	up	UP in reverse mode.
lpar	lpa	LPA in reverse mode.
uar	ua	UA in reverse mode.
auar	aua	AUA in reverse mode.
buar	bua	BUA in reverse mode.
ucr	uc	UC in reverse mode.
eur	eu	EU in reverse mode.
aeur	aeu	AEU in reverse mode.
beur	beu	BEU in reverse mode.
udr	ud	UD in reverse mode.
audr	aud	AUD in reverse mode.
budr	bud	BUD in reverse mode.
pclmr	pclm	CLM prefactor for reverse mode.

© 2023 Cadence Design Systems, Inc.

apclmr	apclm	Length dependence of PCLM for reverse mode.
bpclmr	bpclm	Length dependence of PCLM for reverse mode.
pdibl2r	pdibl2	DIBL output conductance parameter - reverse mode.
uter	ute	UTE in reverse mode.
utlr	utl	UTL in reverse mode.
ua1r	ua1	UA1 in reverse mode.
uc1r	uc1	UC1 in reverse mode.
ud1r	ud1	UD1 in reverse mode.
atr	at	AT in reverse mode.
u0n1r	u0n1	U0N1 in reverse mode.
u0n2r	u0n2	U0N2 in reverse mode.
tnoic	3.5	Thermal noise parameter for TNOIMOD=2.
rnoic	0.395	Thermal noise coefficient for TNOIMOD=2.
tnoik2	0.1	Empirical parameter for sensitivity of RNOIK.
rnoik	0.0	Thermal noise coefficient for (TNOIMOD=92).
tnoik	1.0	Thermal noise parameter for (TNOIMOD=92).
phiglt	0.0 1/m	Coupled NFIN and length dependence of gate workfunction.
eta0lt	0.0 1/m	Coupled NFIN and Length dependence of ETA0.

© 2023 Cadence Design Systems, Inc.

advtp0	0.0	Pre-exponential coefficient for DITS.
bdvtp0	100.0e-9	Exponential coefficient for DITS.
advtp1	0.0	Pre-exponential coefficient for DVTP1.
bdvtp1	100.0e-9	Exponential coefficient for DVTP1.
dvtp2	0.0	DITS model parameter.
devmod	0	TSMC special device.
gislfactor	1.0	TSMC gisl factor.
gidlfactor	1.0	TSMC gidl factor.
kgisl	1.0	TSMC vds power dependence in gisl.
kgidl	1.0	TSMC vds power dependence in gidl.
mgisl	3.0	TSMC vds power dependence in gisl.
mgidl	3.0	TSMC vds power dependence in gidl.
iiratio	0	TSMC ii ratio.
igbratio	0	TSMC igb ratio.
covmod	0	TSMC overlap capacitance.
qmtcencvo	0.0	Prefactor + switch for QM Width for overlap capacitance.
k2si	k0si	Correction factor for strong inversion, used in mob.
k2si1	k0si1 1/K	Temperature dependence of K2SI.

© 2023 Cadence Design Systems, Inc.

k0sisat	0.0	Correction factor for strong inversion, used in mnud.
k0sisat1	0.0 1/K	Temperature dependence of K0SISAT.
k2sisat	k0sisat	Correction factor for strong inversion, used in mob.
k2sisat1	k0sisat1 1/K	Temperature dependence of K2SISAT.
k2sat	0.0	Correction factor for K2 in saturation (high Vds).
k2sat1	0.0	Temperature dependence of K2SAT1.
k2	0.0	Body effect coefficient for BULKMOD==2.
k21	0.0	Temperature dependence of K2.
u0lt	0.0 1/m	Coupled NFIN and length dependence of U0.
vfbsd	0.0 V	Flat band voltage for S/D region.
vfbsdcv	vfbsd V	Flat band voltage for S/D region for C-V calculations.
ashexp	1.0 m^2	Exponent to tune RTH dependence of NFINTOTAL.
bshexp	1.0 m^2	Exponent to tune RTH dependence of NF.
ach_ufcm	1.0 m^2	Area of the channel for the unified model.
cins_ufcm	1.0 F/m	Insulator capacitance for the unified model.
w_ufcm	1.0 m	Effective channel width for the unified model.
tfin_top	15e-9 m	Top body (fin) thicknes, for trapezoidal triple gate.
tfin_base	15e-9 m	Base body (fin) thickness, for trapezoidal triple gate.

© 2023 Cadence Design Systems, Inc.

qmfactorcv	0.0	Charge dependence taking QM effects into account.
alpha_ufcm	0.5556	Mobile charge scaling term taking QM effects into account.
iimod2clamp1	0.1	Clamp1 of SII1*Vg term in IIMOD=2 model.
iimod2clamp2	0.1	Clamp2 of SII0*Vg term in IIMOD=2 model.
iimod2clamp3	0.1	Clamp3 of Ratio term in IIMOD=2 model.
tgaa	5.0e-9 m	Thickness of individual GAA bodies.
tsus	2.0e-9 m	Separation between GAA bodies.
hpff	5.0e-9 m	Fin-height of parasitic finFET.
wgaa	6.0e-9 m	GAA body width.
dws1	0 m	Total width correction for 1st GAA body.
dach1	0 m^2	Total area correction for 1st GAA body.
dws2	0 m	Total width correction for 2nd GAA body.
dach2	0 m^2	Total area correction for 2nd GAA body.
dws3	0 m	Total width correction for 3rd GAA body.
dach3	0 m^2	Total area correction for 3rd GAA body.
ngaa	1	Number of GAA bodies per fin.
subbandmod	0	Switch for GAAFET quantum subband model (0: off; 1: on).
mobscmod	0	Switch for GAAFET geometry dependent mobility model (0: off; 1: on).

© 2023 Cadence Design Systems, Inc.

etamobthin	2.0	Effective field parameter for thin GAA bodies.
etamobtni	7.5e-9 m	Critical TGAA for non-ideality.
etamobir	0.1 nm	Ideality parameter.
uathin	0.3 (cm/MV)^EU	Phonon/surface roughness scattering parameter for thin GAA bodies.
uatsat	9e-9 m	Critical TGAA for UA saturation.
uartsc	0.09 1/nm	Rate of UA decay with TGAA scaling.
uatni	6.4e-9 m	Critical TGAA for non-ideality.
uair	0.2 nm	Ideality parameter.
euthin	2.5 cm/MV	Phonon/surface roughness scattering parameter for thin GAA bodies.
euptsc	3.5	Exponent for TGAA scaling power law.
eutni	6e-9 m	Critical TGAA for non-ideality.
euir	0.2 nm	Ideality parameter.
udthin	0.0 cm/MV	Coulomb scattering parameter for thin GAA bodies.
udtsat	8.1e-9 m	Crtitcal TGAA for UD saturation.
udptsc	1.3	Exponent for UD power law.
u0etawsc	1.5	Ratio of primary carrier low-field mobilities: U0_[110]/U0_[100].
egbulk	1.1 eV	Bulk band-gap.

© 2023 Cadence Design Systems, Inc.

u0emsm1	26.6 $meVnm^2$	Parameter for effective mass scaling.
u0emsm2	4	Parameter for effective mass scaling.
lnbody	0	Length dependence of nbody.
nnbody	0	NFIN dependence of nbody.
pnbody	0	Cross-term dependence of nbody.
lphig	0	Length dependence of phig.
nphig	0	NFIN dependence of phig.
pphig	0	Cross-term dependence of phig.
wphig	0	W-term dependence of phig.
p2phig	0	WL-term dependence of phig.
lxl	0.0 m^2	L-term of XL.
nxl	0.0 m	N-term of XL.
pxl	0.0 m^2	P-term of XL.
llint	0.0 m^2	L-term of LINT.
nlint	0.0 m	N-term of LINT.
plint	0.0 m^2	P-term of LINT.
ldlbin	0.0 m^2	L-term of DLBIN.
ndlbin	0.0 m	N-term of DLBIN.
pdlbin	0.0 m^2	P-term of DLBIN.

© 2023 Cadence Design Systems, Inc.

lngate	0	Length dependence of ngate.
nngate	0	NFIN dependence of ngate.
pngate	0	Cross-term dependence of ngate.
wngate	0	W-term dependence of ngate.
p2ngate	0	WL-term dependence of ngate.
lcit	0	Length dependence of cit.
ncit	0	NFIN dependence of cit.
pcit	0	Cross-term dependence of cit.
wcit	0	W-term dependence of cit.
p2cit	0	WL-term dependence of cit.
lcdsc	0	Length dependence of cdsc.
ncdsc	0	NFIN dependence of cdsc.
pcdsc	0	Cross-term dependence of cdsc.
wcdsc	0	W-term dependence of cdsc.
p2cdsc	0	WL-term dependence of cdsc.
lcdscd	0	Length dependence of cdscd.
ncdscd	0	NFIN dependence of cdscd.
pcdscd	0	Cross-term dependence of cdscd.
wcdscd	0	W-term dependence of cdscd.

© 2023 Cadence Design Systems, Inc.

p2cdscd	0	WL-term dependence of cdscd.
lcdscdr	0	Length dependence of cdscdr.
ncdscdr	0	NFIN dependence of cdscdr.
pcdscdr	0	Cross-term dependence of cdscdr.
wcdscdr	0	W-term dependence of cdscdr.
p2cdscdr	0	WL-term dependence of cdscdr.
ldvt0	0	Length dependence of dvt0.
ndvt0	0	NFIN dependence of dvt0.
pdvt0	0	Cross-term dependence of dvt0.
wdvt0	0	W-term dependence of dvt0.
p2dvt0	0	WL-term dependence of dvt0.
ldvt1	0	Length dependence of dvt1.
ndvt1	0	NFIN dependence of dvt1.
pdvt1	0	Cross-term dependence of dvt1.
wdvt1	0	W-term dependence of dvt1.
p2dvt1	0	WL-term dependence of dvt1.
ldvt1ss	0	Length dependence of dvt1ss.
ndvt1ss	0	NFIN dependence of dvt1ss.
pdvt1ss	0	Cross-term dependence of dvt1ss.

© 2023 Cadence Design Systems, Inc.

wdvt1ss	0	W-term dependence of dvt1ss.
p2dvt1ss	0	WL-term dependence of dvt1ss.
lphin	0	Length dependence of phin.
nphin	0	NFIN dependence of phin.
pphin	0	Cross-term dependence of phin.
wphin	0	W-term dependence of phin.
p2phin	0	WL-term dependence of phin.
leta0	0	Length dependence of eta0.
neta0	0	NFIN dependence of eta0.
peta0	0	Cross-term dependence of eta0.
weta0	0	W-term dependence of eta0.
p2eta0	0	WL-term dependence of eta0.
leta0r	0	Length dependence of eta0r.
neta0r	0	NFIN dependence of eta0r.
peta0r	0	Cross-term dependence of eta0r.
weta0r	0	W-term dependence of eta0r.
p2eta0r	0	WL-term dependence of eta0r.
ldsub	0	Length dependence of dsub.
ndsub	0	NFIN dependence of dsub.

© 2023 Cadence Design Systems, Inc.

pdsub	0	Cross-term dependence of dsub.
wdsub	0	W-term dependence of dsub.
p2dsub	0	WL-term dependence of dsub.
lk1rsce	0	Length dependence of lk1rsce.
nk1rsce	0	NFIN dependence of lk1rsce.
pk1rsce	0	Cross-term dependence of lk1rsce.
wk1rsce	0	W-term dependence of lk1rsce.
p2k1rsce	0	WL-term dependence of lk1rsce.
llpe0	0	Length dependence of lpe0.
nlpe0	0	NFIN dependence of lpe0.
plpe0	0	Cross-term dependence of lpe0.
wlpe0	0	W-term dependence of lpe0.
p2lpe0	0	WL-term dependence of lpe0.
ldvtshift	0	Length dependence of dvtshift.
ndvtshift	0	NFIN dependence of dvtshift.
pdvtshift	0	Cross-term dependence of dvtshift.
wdvtshift	0	W-term dependence of dvtshift.
p2dvtshift	0	WL-term dependence of dvtshift.
lphibe	0	Length dependence of phibe.

© 2023 Cadence Design Systems, Inc.

nphibe	0	NFIN dependence of phibe.
pphibe	0	Cross-term dependence of phibe.
wphibe	0	W-term dependence of phibe.
p2phibe	0	WL-term dependence of phibe.
lk0	0	Length dependence of k0.
nk0	0	NFIN dependence of k0.
pk0	0	Cross-term dependence of k0.
wk0	0	W-term dependence of k0.
p2k0	0	WL-term dependence of k0.
lk0si	0	Length dependence of k0si.
nk0si	0	NFIN dependence of k0si.
pk0si	0	Cross-term dependence of k0si.
wk0si	0	W-term dependence of k0si.
p2k0si	0	WL-term dependence of k0si.
lk1	0	Length dependence of k1.
nk1	0	NFIN dependence of k1.
pk1	0	Cross-term dependence of k1.
wk1	0	W-term dependence of k1.
p2k1	0	WL-term dependence of k1.

© 2023 Cadence Design Systems, Inc.

lk1si	0	Length dependence of k1si.
nk1si	0	NFIN dependence of k1si.
pk1si	0	Cross-term dependence of k1si.
lk1sat	0	Length dependence of k1sat.
nk1sat	0	NFIN dependence of k1sat.
pk1sat	0	Cross-term dependence of k1sat.
ldvtb	0	Length dependence of dvtb.
ndvtb	0	NFIN dependence of dvtb.
pdvtb	0	Cross-term dependence of dvtb.
llpeb	0	Length dependence of lpeb.
nlpeb	0	NFIN dependence of lpeb.
plpeb	0	Cross-term dependence of lpeb.
lqmfactor	0.0	Length dependence of qmfactor.
nqmfactor	0.0	NFIN dependence of qmfactor.
pqmfactor	0.0	Cross-term dependence of qmfactor.
wqmfactor	0.0	W-term dependence of qmfactor.
p2qmfactor	0.0	WL-term dependence of qmfactor.
lqmtceniv	0.0	Length dependence of qmtceniv.
nqmtceniv	0.0	NFIN dependence of qmtceniv.

© 2023 Cadence Design Systems, Inc.

pqmtceniv	0.0	Cross-term dependence of qmtceniv.
lqmtcencv	0.0	Length dependence of qmtcencv.
nqmtcencv	0.0	NFIN dependence of qmtcencv.
pqmtcencv	0.0	Cross-term dependence of qmtcencv.
wqmtcencv	0.0	W-term dependence of qmtcencv.
lqmtcencvo	0.0	Length dependence of qmtcencvo.
nqmtcencvo	0.0	NFIN dependence of qmtcencvo.
pqmtcencvo	0.0	Cross-term dependence of qmtcencv.
p2qmtcencv	0.0	WL-term dependence of qmtcencv.
lqmtcencva	0.0	Length dependence of qmtcencva.
nqmtcencva	0.0	NFIN dependence of qmtcencva.
pqmtcencva	0.0	Cross-term dependence of qmtcencva.
wqmtcencva	0.0	W-term dependence of qmtcencva.
p2qmtcencva	0.0	WL-term dependence of qmtcencva.
lvsat	0	Length dependence of vsat.
nvsat	0	NFIN dependence of vsat.
pvsat	0	Cross-term dependence of vsat.
wvsat	0	W-term dependence of vsat.
p2vsat	0	WL-term dependence of vsat.

© 2023 Cadence Design Systems, Inc.

lvsat1	0	Length dependence of vsat1.
nvsat1	0	NFIN dependence of vsat1.
pvsat1	0	Cross-term dependence of vsat1.
wvsat1	0	W-term dependence of vsat1.
p2vsat1	0	WL-term dependence of vsat1.
lvsat1r	0	Length dependence of vsat1r.
nvsat1r	0	NFIN dependence of vsat1r.
pvsat1r	0	Cross-term dependence of vsat1r.
wvsat1r	0	W-term dependence of vsat1r.
p2vsat1r	0	WL-term dependence of vsat1r.
lpsat	0	Length dependence of psat.
npsat	0	NFIN dependence of psat.
ppsat	0	Cross-term dependence of psat.
wpsat	0	W-term dependence of psat.
p2psat	0	WL-term dependence of psat.
ldeltavsat	0	Length dependence of deltavsat.
ndeltavsat	0	NFIN dependence of ndetavsat.
pdeltavsat	0	Cross-term dependence of deltavsat.
wdeltavsat	0	W-term dependence of deltavsat.

© 2023 Cadence Design Systems, Inc.

p2deltavsat	0	WL-term dependence of deltavsat.
lksativ	0	Length dependence of ksativ.
nksativ	0	NFIN dependence of ksativ.
pksativ	0	Cross-term dependence of ksativ.
wksativ	0	W-term dependence of ksativ.
p2ksativ	0	WL-term dependence of ksativ.
lvsatcv	0	Length dependence of vsatcv.
nvsatcv	0	NFIN dependence of vsatcv.
pvsatcv	0	Cross-term dependence of vsatcv.
wvsatcv	0	W-term dependence of vsatcv.
p2vsatcv	0	WL-term dependence of vsatcv.
lmexp	0	Length dependence of mexp.
nmexp	0	NFIN dependence of mexp.
pmexp	0	Cross-term dependence of mexp.
wmexp	0	W-term dependence of mexp.
p2mexp	0	WL-term dependence of mexp.
lmexpr	0	Length dependence of mexpr.
nmexpr	0	NFIN dependence of mexpr.
pmexpr	0	Cross-term dependence of mexpr.

© 2023 Cadence Design Systems, Inc.

wmexpr	0	W-term dependence of mexpr.
p2mexpr	0	WL-term dependence of mexpr.
lptwg	0.0	Length dependence of ptwg.
nptwg	0.0	NFIN dependence of ptwg.
pptwg	0.0	Cross-term dependence of ptwg.
wptwg	0.0	W-term dependence of ptwg.
p2ptwg	0.0	WL-term dependence of ptwg.
lptwgr	0.0	Length dependence of ptwgr.
nptwgr	0.0	NFIN dependence of ptwgr.
pptwgr	0.0	Cross-term dependence of ptwgr.
wptwgr	0.0	W-term dependence of ptwgr.
p2ptwgr	0.0	WL-term dependence of ptwgr.
lthetasat	0	Length dependence of thetasat.
nthetasat	0	NFIN dependence of thetasat.
pthetasat	0	Cross-term dependence of thetasat.
lu0	0	Length dependence of u0.
nu0	0	NFIN dependence of u0.
pu0	0	Cross-term dependence of u0.
wu0	0	W-term dependence of u0.

© 2023 Cadence Design Systems, Inc.

p2u0	0	WL-term dependence of u0.
letamob	0	Length dependence of letamob.
netamob	0	NFIN dependence of netamob.
petamob	0	Cross-term dependence of petamob.
wetamob	0	W-term dependence of petamob.
p2etamob	0	WL-term dependence of petamob.
lup	0	Length dependence of up.
nup	0	NFIN dependence of up.
pup	0	Cross-term dependence of up.
wup	0	W-term dependence of up.
p2up	0	WL-term dependence of up.
lua	0	Length dependence of ua.
nua	0	NFIN dependence of ua.
pua	0	Cross-term dependence of ua.
wua	0	W-term dependence of ua.
p2ua	0	WL-term dependence of ua.
luc	0	Length dependence of uc.
nuc	0	NFIN dependence of uc.
puc	0	Cross-term dependence of uc.

© 2023 Cadence Design Systems, Inc.

wuc	0	W-term dependence of uc.
p2uc	0	WL-term dependence of uc.
leu	0	Length dependence of eu.
neu	0	NFIN dependence of eu.
peu	0	Cross-term dependence of eu.
weu	0	W-term dependence of eu.
p2eu	0	WL-term dependence of eu.
lud	0	Length dependence of ud.
nud	0	NFIN dependence of ud.
pud	0	Cross-term dependence of ud.
wud	0	W-term dependence of ud.
p2ud	0	WL-term dependence of ud.
lucs	0	Length dependence of ucs.
nucs	0	NFIN dependence of ucs.
pucs	0	Cross-term dependence of ucs.
wucs	0	W-term dependence of ucs.
p2ucs	0	WL-term dependence of ucs.
lmue	0	Length dependence of mue.
nmue	0	NFIN dependence of mue.

© 2023 Cadence Design Systems, Inc.

pmue	0	Cross-term dependence of mue.
lcs	0	Length dependence of cs.
ncs	0	NFIN dependence of cs.
pcs	0	Cross-term dependence of cs.
lpclm	0	Length dependence of pclm.
npclm	0	NFIN dependence of pclm.
ppclm	0	Cross-term dependence of pclm.
wpclm	0	W-term dependence of pclm.
p2pclm	0	WL-term dependence of pclm.
lpclmg	0	Length dependence of pclmg.
npclmg	0	Length dependence of nclmg.
ppclmg	0	Length dependence of pclmg.
wpclmg	0	W-term dependence of pclmg.
p2pclmg	0	WL-term dependence of pclmg.
lvasat	0	Length dependence of lvasat.
nvasat	0	Length dependence of nvasat.
pvasat	0	Length dependence of pvasat.
lpclmcv	0	Length dependence of pclmcv.
npclmcv	0	NFIN dependence of pclmcv.

© 2023 Cadence Design Systems, Inc.

ppclmcv	0	Cross-term dependence of pclmcv.
wpclmcv	0	W-term dependence of pclmcv.
p2pclmcv	0	WL-term dependence of pclmcv.
la1	0	Length dependence of a1.
na1	0	NFIN dependence of a1.
pa1	0	Cross-term dependence of a1.
wa1	0	W-term dependence of a1.
p2a1	0	WL-term dependence of a1.
la2	0	Length dependence of a2.
na2	0	NFIN dependence of a2.
pa2	0	Cross-term dependence of a2.
wa2	0	W-term dependence of a2.
p2a2	0	WL-term dependence of a2.
lrdsw	0	Length dependence of rdsw.
nrdsw	0	NFIN dependence of rdsw.
prdsw	0	Cross-term dependence of rdsw.
wrdsw	0	W-term dependence of rdsw.
p2rdsw	0	WL-term dependence of rdsw.
lrsw	0.0	Length dependence of rsw.

© 2023 Cadence Design Systems, Inc.

nrsw	0.0	NFIN dependence of rsw.
prsw	0.0	Cross-term dependence of rsw.
wrsw	0.0	W-term dependence of rsw.
p2rsw	0.0	WL-term dependence of rsw.
lrdw	0.0	Length dependence of rdw.
nrdw	0.0	NFIN dependence of rdw.
prdw	0.0	Cross-term dependence of rdw.
wrdw	0.0	W-term dependence of rdw.
p2rdw	0.0	WL-term dependence of rdw.
lprwg	0	Length dependence of prwg.
nprwg	0	NFIN dependence of prwg.
pprwg	0	Cross-term dependence of prwg.
lprwgs	0	Length dependence of prwgs.
nprwgs	0	NFIN dependence of prwgs.
pprwgs	0	Cross-term dependence of prwgs.
wprwgs	0	W-term dependence of prwgs.
p2prwgs	0	WL-term dependence of prwgs.
lprwgd	0	NFIN dependence of prwgd.
nprwgd	0	NFIN dependence of prwgd.

© 2023 Cadence Design Systems, Inc.

pprwgd	0	Cross-term dependence of prwgd.
wprwgd	0	W-term dependence of prwgd.
p2prwgd	0	WL-term dependence of prwgd.
lwr	0	Length dependence of wr.
nwr	0	NFIN dependence of wr .
pwr	0	Cross-term dependence of wr.
wwr	0	W-term dependence of wr.
p2wr	0	WL-term dependence of wr.
lpdibl1	0	Length dependence of pdibl1.
npdibl1	0	NFIN dependence of pdibl1.
ppdibl1	0	Cross-term dependence of pdibl1.
wpdibl1	0	W-term dependence of pdibl1.
p2pdibl1	0	WL-term dependence of pdibl1.
lpdibl1r	0	Length dependence of pdibl1r.
npdibl1r	0	NFIN dependence of pdibl1r.
ppdibl1r	0	Cross-term dependence of pdibl1r.
wpdibl1r	0	W-term dependence of pdibl1r.
p2pdibl1r	0	WL-term dependence of pdibl1r.
lpdibl2	0	Length dependence of pdibl2.

© 2023 Cadence Design Systems, Inc.

npdibl2	0	NFIN dependence of pdibl2.
ppdibl2	0	Cross-term dependence of pdibl2.
wpdibl2	0	W-term dependence of pdibl2.
p2pdibl2	0	WL-term dependence of pdibl2.
ldrout	0	Length dependence of drout.
ndrout	0	NFIN dependence of drout.
pdrout	0	Cross-term dependence of drout.
wdrout	0	W-term dependence of drout.
p2drout	0	WL-term dependence of drout.
lpvag	0	Length dependence of pvag.
npvag	0	NFIN dependence of pvag.
ppvag	0	Cross-term dependence of pvag.
wpvag	0	W-term dependence of pvag.
p2pvag	0	WL-term dependence of pvag.
laigbinv	0	Length dependence of aigbinv.
naigbinv	0	NFIN dependence of aigbinv.
paigbinv	0	Cross-term dependence of aigbinv.
waigbinv	0	W-term dependence of aigbinv.
p2aigbinv	0	WL-term dependence of aigbinv.

© 2023 Cadence Design Systems, Inc.

lbigbinv	0	Length dependence of bigbinv.
nbigbinv	0	NFIN dependence of bigbinv.
pbigbinv	0	Cross-term dependence of bigbinv.
wbigbinv	0	W-term dependence of bigbinv.
p2bigbinv	0	WL-term dependence of bigbinv.
lcigbinv	0	Length dependence of cigbinv.
ncigbinv	0	NFIN dependence of cigbinv.
pcigbinv	0	Cross-term dependence of cigbinv.
wcigbinv	0	W-term dependence of cigbinv.
p2cigbinv	0	WL-term dependence of cigbinv.
leigbinv	0	Length dependence of eigbinv.
neigbinv	0	NFIN dependence of eigbinv.
peigbinv	0	Cross-term dependence of eigbinv.
weigbinv	0	W-term dependence of eigbinv.
p2eigbinv	0	WL-term dependence of eigbinv.
lnigbinv	0	Length dependence of nigbinv.
nnigbinv	0	NFIN dependence of nigbinv.
pnigbinv	0	Cross-term dependence of nigbinv.
wnigbinv	0	W-term dependence of nigbinv.

© 2023 Cadence Design Systems, Inc.

p2nigbinv	0	WL-term dependence of nigbinv.
laigbacc	0	Length dependence of aigbacc.
naigbacc	0	NFIN dependence of aigbacc.
paigbacc	0	Cross-term dependence of aigbacc.
waigbacc	0	W-term dependence of aigbacc.
p2aigbacc	0	WL-term dependence of aigbacc.
lbigbacc	0	Length dependence of bigbacc.
nbigbacc	0	NFIN dependence of bigbacc.
pbigbacc	0	Cross-term dependence of bigbacc.
wbigbacc	0	W-term dependence of bigbacc.
p2bigbacc	0	WL-term dependence of bigbacc.
lcigbacc	0	Length dependence of cigbacc.
ncigbacc	0	NFIN dependence of cigbacc.
pcigbacc	0	Cross-term dependence of cigbacc.
wcigbacc	0	W-term dependence of cigbacc.
p2cigbacc	0	WL-term dependence of cigbacc.
lnigbacc	0	Length dependence of nigbacc.
nnigbacc	0	NFIN dependence of nigbacc.
pnigbacc	0	Cross-term dependence of nigbacc.

© 2023 Cadence Design Systems, Inc.

wnigbacc	0	W-term dependence of nigbacc.
p2nigbacc	0	WL-term dependence of nigbacc.
laigc	0	Length dependence of aigc.
naigc	0	NFIN dependence of aigc.
paigc	0	Cross-term dependence of aigc.
waigc	0	W-term dependence of aigc.
p2aigc	0	WL-term dependence of aigc.
laigc1	0	Length dependence of aigc1.
naigc1	0	NFIN dependence of aigc1.
paigc1	0	Cross-term dependence of aigc1.
waigc1	0	W-term dependence of aigc1.
p2aigc1	0	WL-term dependence of aigc1.
lbigc	0	Length dependence of bigc.
nbigc	0	NFIN dependence of bigc.
pbigc	0	Cross-term dependence of bigc.
wbigc	0	W-term dependence of bigc.
p2bigc	0	WL-term dependence of bigc.
lcigc	0	Length dependence of cigc.
ncigc	0	NFIN dependence of cigc.

© 2023 Cadence Design Systems, Inc.

pcigc	0	Cross-term dependence of cigc.
wcigc	0	W-term dependence of cigc.
p2cigc	0	WL-term dependence of cigc.
lnigc	0	Length dependence of nigc.
nnigc	0	NFIN dependence of nigc.
pnigc	0	Cross-term dependence of nigc.
lpigcd	0	Length dependence of pigcd.
npigcd	0	NFIN dependence of pigcd.
ppigcd	0	Cross-term dependence of pigcd.
wpigcd	0	W-term dependence of pigcd.
p2pigcd	0	WL-term dependence of pigcd.
laigs	0	Length dependence of aigs.
naigs	0	NFIN dependence of aigs.
paigs	0	Cross-term dependence of aigs.
waigs	0	W-term dependence of aigs.
p2aigs	0	WL-term dependence of aigs.
laigs1	0	Length dependence of aigs1.
naigs1	0	NFIN dependence of aigs1.
paigs1	0	Cross-term dependence of aigs1.

© 2023 Cadence Design Systems, Inc.

waigs1	0	W-term dependence of aigs1.
p2aigs1	0	WL-term dependence of aigs1.
lbigs	0	Length dependence of bigs.
nbigs	0	NFIN dependence of bigs.
pbigs	0	Cross-term dependence of bigs.
wbigs	0	W-term dependence of bigs.
p2bigs	0	WL-term dependence of bigs.
lcigs	0	Length dependence of cigs.
ncigs	0	NFIN dependence of cigs.
pcigs	0	Cross-term dependence of cigs.
wcigs	0	W-term dependence of cigs.
p2cigs	0	WL-term dependence of cigs.
laigd	0	Length dependence of aigd.
naigd	0	NFIN dependence of aigd.
paigd	0	Cross-term dependence of aigd.
waigd	0	W-term dependence of aigd.
p2aigd	0	WL-term dependence of aigd.
lbigd	0	Length dependence of bigd.
nbigd	0	NFIN dependence of bigd.

© 2023 Cadence Design Systems, Inc.

pbigd	0	Cross-term dependence of bigd.
wbigd	0	W-term dependence of bigd.
p2bigd	0	WL-term dependence of bigd.
lcigd	0	Length dependence of cigd.
ncigd	0	NFIN dependence of cigd.
pcigd	0	Cross-term dependence of cigd.
wcigd	0	W-term dependence of cigd.
p2cigd	0	WL-term dependence of cigd.
lntox	0	Length dependence of ntox.
nntox	0	NFIN dependence of ntox.
pntox	0	Cross-term dependence of ntox.
wntox	0	W-term dependence of ntox.
p2ntox	0	WL-term dependence of ntox.
lpoxedge	0	Length dependence of poxedge.
npoxedge	0	NFIN dependence of poxedge.
ppoxedge	0	Cross-term dependence of poxedge.
wpoxedge	0	W-term dependence of poxedge.
p2poxedge	0	WL-term dependence of poxedge.
lagidl	0	Length dependence of agidl.

© 2023 Cadence Design Systems, Inc.

nagidl	0	NFIN dependence of agidl.
pagidl	0	Cross-term dependence of agidl.
wagidl	0	W-term dependence of agidl.
p2agidl	0	WL-term dependence of agidl.
lbgidl	0	Length dependence of bgidl.
nbgidl	0	NFIN dependence of bgidl.
pbgidl	0	Cross-term dependence of bgidl.
wbgidl	0	W-term dependence of bgidl.
p2bgidl	0	WL-term dependence of bgidl.
legidl	0	Length dependence of egidl.
negidl	0	NFIN dependence of egidl.
pegidl	0	Cross-term dependence of egidl.
wegidl	0	W-term dependence of egidl.
p2egidl	0	WL-term dependence of egidl.
lcgidl	0	Length dependence of cgidl.
ncgidl	0	NFIN dependence of cgidl.
pcgidl	0	Cross-term dependence of cgidl.
wcgidl	0	W-term dependence of cgidl.
p2cgidl	0	WL-term dependence of cgidl.

© 2023 Cadence Design Systems, Inc.

lpgidl	0	Length dependence of pgidl.
npgidl	0	NFIN dependence of pgidl.
ppgidl	0	Cross-term dependence of pgidl.
wpgidl	0	W-term dependence of pgidl.
p2pgidl	0	WL-term dependence of pgidl.
lagisl	0	Length dependence of agisl.
nagisl	0	NFIN dependence of agisl.
pagisl	0	Cross-term dependence of agisl.
wagisl	0	W-term dependence of agisl.
p2agisl	0	WL-term dependence of agisl.
lbgisl	0	Length dependence of bgisl.
nbgisl	0	NFIN dependence of bgisl.
pbgisl	0	Cross-term dependence of bgisl.
wbgisl	0	W-term dependence of bgisl.
p2bgisl	0	WL-term dependence of bgisl.
legisl	0	Length dependence of egisl.
negisl	0	NFIN dependence of egisl.
pegisl	0	Cross-term dependence of egisl.
wegisl	0	W-term dependence of egisl.

© 2023 Cadence Design Systems, Inc.

p2egisl	0	WL-term dependence of egisl.
lcgisl	0	Length dependence of cgisl.
ncgisl	0	NFIN dependence of cgisl.
pcgisl	0	Cross-term dependence of cgisl.
wcgisl	0	W-term dependence of cgisl.
p2cgisl	0	WL-term dependence of cgisl.
lpgisl	0	Length dependence of pgisl.
npgisl	0	NFIN dependence of pgisl.
ppgisl	0	Cross-term dependence of pgisl.
wpgisl	0	W-term dependence of pgisl.
p2pgisl	0	WL-term dependence of pgisl.
lalpha0	0.0	Length dependence of alpha0.
nalpha0	0.0	NFIN dependence of alpha0.
palpha0	0.0	Cross-term dependence of alpha0.
walpha0	0.0	W-term dependence of alpha0.
p2alpha0	0.0	WL-term dependence of alpha0.
lalpha1	0.0	Length dependence of alpha1.
nalpha1	0.0	NFIN dependence of alpha1.
palpha1	0.0	Cross-term dependence of alpha1.

© 2023 Cadence Design Systems, Inc.

walpha1	0.0	W-term dependence of alpha1.
p2alpha1	0.0	WL-term dependence of alpha1.
lbeta0	0.0	Length dependence of beta0.
nbeta0	0.0	NFIN dependence of beta0.
pbeta0	0.0	Cross-term dependence of beta0.
wbeta0	0.0	W-term dependence of beta0.
p2beta0	0.0	WL-term dependence of beta0.
lalphaii	0.0	Length dependence of alphaii.
nalphaii	0.0	NFIN dependence of alphaii.
palphaii	0.0	Cross-term dependence of alphaii.
walphaii	0.0	W-term dependence of alphaii.
p2alphaii	0.0	WL-term dependence of alphaii.
lbetaii0	0.0	Length dependence of betaii0.
nbetaii0	0.0	NFIN dependence of betaii0.
pbetaii0	0.0	Cross-term dependence of betaii0.
wbetaii0	0.0	W-term dependence of betaii0.
p2betaii0	0.0	WL-term dependence of betaii0.
lbetaii1	0.0	Length dependence of betaii1.
nbetaii1	0.0	NFIN dependence of betaii1.

© 2023 Cadence Design Systems, Inc.

pbetaii1	0.0	Cross-term dependence of betaii1.
wbetaii1	0.0	W-term dependence of betaii1.
p2betaii1	0.0	WL-term dependence of betaii1.
lbetaii2	0.0	Length dependence of betaii2.
nbetaii2	0.0	NFIN dependence of betaii2.
pbetaii2	0.0	Cross-term dependence of betaii2.
wbetaii2	0.0	W-term dependence of betaii2.
p2betaii2	0.0	WL-term dependence of betaii2.
lesatii	0.0	Length dependence of esatii.
nesatii	0.0	NFIN dependence of esatii.
pesatii	0.0	Cross-term dependence of esatii.
wesatii	0.0	W-term dependence of esatii.
p2esatii	0.0	WL-term dependence of esatii.
llii	0.0	Length dependence of lii.
nlii	0.0	NFIN dependence of lii.
plii	0.0	Cross-term dependence of lii.
wlii	0.0	W-term dependence of lii.
p2lii	0.0	WL-term dependence of lii.
lsii0	0.0	Length dependence of sii0.

© 2023 Cadence Design Systems, Inc.

nsii0	0.0	NFIN dependence of sii0.
psii0	0.0	Cross-term dependence of sii0.
wsii0	0.0	W-term dependence of sii0.
p2sii0	0.0	WL-term dependence of sii0.
lsii1	0.0	Length dependence of sii1.
nsii1	0.0	NFIN dependence of sii1.
psii1	0.0	Cross-term dependence of sii1.
wsii1	0.0	W-term dependence of sii1.
p2sii1	0.0	WL-term dependence of sii1.
lsii2	0.0	Length dependence of sii2.
nsii2	0.0	NFIN dependence of sii2.
psii2	0.0	Cross-term dependence of sii2.
wsii2	0.0	W-term dependence of sii2.
p2sii2	0.0	WL-term dependence of sii2.
lsiid	0.0	Length dependence of siid.
nsiid	0.0	NFIN dependence of siid.
psiid	0.0	Cross-term dependence of siid.
wsiid	0.0	W-term dependence of siid.
p2siid	0.0	WL-term dependence of siid.

© 2023 Cadence Design Systems, Inc.

lcfs	0.0	Length dependence of cfs.
ncfs	0.0	NFIN dependence of cfs.
pcfs	0.0	Cross-term dependence of cfs.
wcfs	0.0	W-term dependence of cfs.
p2cfs	0.0	WL-term dependence of cfs.
lcfd	0.0	Length dependence of cfd.
ncfd	0.0	NFIN dependence of cfd.
pcfd	0.0	Cross-term dependence of cfd.
wcfd	0.0	W-term dependence of cfd.
p2cfd	0.0	WL-term dependence of cfd.
lcovs	0.0	Length dependence of covs.
ncovs	0.0	NFIN dependence of covs.
pcovs	0.0	Cross-term dependence of covs.
wcovs	0.0	W-term dependence of covs.
p2covs	0.0	WL-term dependence of covs.
lcovd	0.0	Length dependence of covd.
ncovd	0.0	NFIN dependence of covd.
pcovd	0.0	Cross-term dependence of covd.
wcovd	0.0	W-term dependence of covd.

© 2023 Cadence Design Systems, Inc.

p2covd	0.0	WL-term dependence of covd.
lcgsl	0.0	Length dependence of cgsl.
ncgsl	0.0	NFIN dependence of cgsl.
pcgsl	0.0	Cross-term dependence of cgsl.
wcgsl	0.0	W-term dependence of cgsl.
p2cgsl	0.0	WL-term dependence of cgsl.
lcgdl	0.0	Length dependence of cgdl.
ncgdl	0.0	NFIN dependence of cgdl.
pcgdl	0.0	Cross-term dependence of cgdl.
wcgdl	0.0	W-term dependence of cgdl.
p2cgdl	0.0	WL-term dependence of cgdl.
lckappas	0.0	Length dependence of ckappas.
nckappas	0.0	NFIN dependence of ckappas.
pckappas	0.0	Cross-term dependence of ckappas.
wckappas	0.0	W-term dependence of ckappas.
p2ckappas	0.0	WL-term dependence of ckappas.
lckappad	0.0	Length dependence of ckappad.
nckappad	0.0	NFIN dependence of ckappad.
pckappad	0.0	Cross-term dependence of ckappad.

© 2023 Cadence Design Systems, Inc.

wckappad	0.0	W-term dependence of ckappad.
p2ckappad	0.0	WL-term dependence of ckappad.
lcgbl	0.0	Length dependence of cgbl.
ncgbl	0.0	NFIN dependence of cgbl.
pcgbl	0.0	Cross-term dependence of cgbl.
wcgbl	0.0	W-term dependence of cgbl.
p2cgbl	0.0	WL-term dependence of cgbl.
lckappab	0.0	Length dependence of ckappab.
nckappab	0.0	NFIN dependence of ckappab.
pckappab	0.0	Cross-term dependence of ckappab.
wckappab	0.0	W-term dependence of ckappab.
p2ckappab	0.0	WL-term dependence of ckappab.
lntgen	0	Length dependence of ntgen.
nntgen	0	NFIN dependence of ntgen.
pntgen	0	Cross-term dependence of ntgen.
wntgen	0	W-term dependence of ntgen.
p2ntgen	0	WL-term dependence of ntgen.
laigen	0	Length dependence of aigen.
naigen	0	NFIN dependence of aigen.

© 2023 Cadence Design Systems, Inc.

paigen	0	Cross-term dependence of aigen.
waigen	0	W-term dependence of aigen.
p2aigen	0	WL-term dependence of aigen.
lbigen	0	Length dependence of bigen.
nbigen	0	NFIN dependence of bigen.
pbigen	0	Cross-term dependence of bigen.
wbigen	0	W-term dependence of bigen.
p2bigen	0	WL-term dependence of bigen.
lxrcrg1	0.0	Length dependence of xrcrg1.
nxrcrg1	0.0	NFIN dependence of xrcrg1.
pxrcrg1	0.0	Cross-term dependence of xrcrg1.
wxrcrg1	0.0	W-term dependence of xrcrg1.
p2xrcrg1	0.0	WL-term dependence of xrcrg1.
lxrcrg2	0.0	Length dependence of xrcrg2.
nxrcrg2	0.0	NFIN dependence of xrcrg2.
pxrcrg2	0.0	Cross-term dependence of xrcrg2.
wxrcrg2	0.0	W-term dependence of xrcrg2.
p2xrcrg2	0.0	WL-term dependence of xrcrg2.
lute	0.0	Length dependence of ute.

© 2023 Cadence Design Systems, Inc.

nute	0.0	NFIN dependence of ute.
pute	0.0	Cross-term dependence of ute.
wute	0.0	W-term dependence of ute.
p2ute	0.0	WL-term dependence of ute.
lutl	0.0	Length dependence of utl.
nutl	0.0	NFIN dependence of utl.
putl	0.0	Cross-term dependence of utl.
wutl	0.0	W-term dependence of utl.
p2utl	0.0	WL-term dependence of utl.
lemobt	0	Length dependence of emobt.
nemobt	0	NFIN dependence of emobt.
pemobt	0	Cross-term dependence of emobt.
wemobt	0	W-term dependence of emobt.
p2emobt	0	WL-term dependence of emobt.
lua1	0.0	Length dependence of ua1.
nua1	0.0	NFIN dependence of ua1.
pua1	0.0	Cross-term dependence of ua1.
wua1	0.0	W-term dependence of ua1.
p2ua1	0.0	WL-term dependence of ua1.

© 2023 Cadence Design Systems, Inc.

luc1	0.0	Length dependence of uc1.
nuc1	0.0	NFIN dependence of uc1.
puc1	0.0	Cross-term dependence of uc1.
wuc1	0.0	W-term dependence of uc1.
p2uc1	0.0	WL-term dependence of uc1.
lud1	0.0	Length dependence of ud1.
nud1	0.0	NFIN dependence of ud1.
pud1	0.0	Cross-term dependence of ud1.
wud1	0.0	W-term dependence of ud1.
p2ud1	0.0	WL-term dependence of ud1.
lucste	0.0	Length dependence of ucste.
nucste	0.0	NFIN dependence of ucste.
pucste	0.0	Cross-term dependence of ucste.
wucste	0.0	W-term dependence of ucste.
p2ucste	0.0	WL-term dependence of ucste.
lptwgt	0	Length dependence of ptwgt.
nptwgt	0	NFIN dependence of ptwgt.
pptwgt	0	Cross-term dependence of ptwgt.
wptwgt	0	W-term dependence of ptwgt.

© 2023 Cadence Design Systems, Inc.

p2ptwgt	0	WL-term dependence of ptwgt.
lat	0	Length dependence of at.
nat	0	NFIN dependence of at.
pat	0	Cross-term dependence of at.
wat	0	W-term dependence of at.
p2at	0	WL-term dependence of at.
lstthetasat	0	Length dependence of stthetasat.
nstthetasat	0	NFIN dependence of stthetasat.
pstthetasat	0	Cross-term dependence of stthetasat.
lprt	0	Length dependence of prt.
nprt	0	NFIN dependence of prt.
pprt	0	Cross-term dependence of prt.
wprt	0	W-term dependence of prt.
p2prt	0	WL-term dependence of prt.
lkt1	0	Length dependence of kt1.
nkt1	0	NFIN dependence of kt1.
pkt1	0	Cross-term dependence of kt1.
wkt1	0.0 m V	W-term of KT1.
p2kt1	0.0 (m^2) V	WL-term of KT1.

© 2023 Cadence Design Systems, Inc.

ltss	0	Length dependence of tss.
ntss	0	NFIN dependence of tss.
ptss	0	Cross-term dependence of tss.
wtss	0.0 m/K	W-term of TSS.
p2tss	0.0 $(m^2)/K$	WL-term of TSS.
liit	0	Length dependence of iit.
niit	0	NFIN dependence of iit.
piit	0	Cross-term dependence of iit.
wiit	0.0 m	W-term of IIT.
p2iit	0.0 m^2	WL-term of IIT.
ltii	0.0	Length dependence of tii.
ntii	0.0	NFIN dependence of tii.
ptii	0.0	Cross-term dependence of tii.
wtii	0.0 m	W-term of TII.
p2tii	0.0 m^2	WL-term of TII.
ltgidl	0	Length dependence of tgidl.
ntgidl	0	NFIN dependence of tgidl.
ptgidl	0	Cross-term dependence of tgidl.
wtgidl	0.0 m/K	W-term of TGIDL.

© 2023 Cadence Design Systems, Inc.

p2tgidl	0.0 $(m^2)/K$	WL-term of TGIDL.
ligt	0	Length dependence of igt.
nigt	0	NFIN dependence of igt.
pigt	0	Cross-term dependence of igt.
wigt	0.0 m	W-term of IGT.
p2igt	0.0 m^2	WL-term of IGT.
lnoia2	0.0	Length dependence of noia2.
nnoia2	0.0 s^(1-EF)/(eV m^3)	NFIN dependence of noia2.
pnoia2	0.0	Cross-term dependence of noia2.
wnoia2	0.0 s^(1-EF)/(eV m^2)	W-term for NOIA2.
p2noia2	0.0 s^(1-EF)/(eV m)	WL-term for NOIA2.
lmpower	0.0	Length dependence of mpower.
nmpower	0.0	NFIN dependence of mpower.
pmpower	0.0	Cross-term dependence of mpower.
wmpower	0.0 m	W-term for MPOWER.

© 2023 Cadence Design Systems, Inc.

p2mpower	0.0 m^2	WL-term for MPOWER.
lqsref	0.0	Length dependence of qsref.
nqsref	0.0	NFIN dependence of qsref.
pqsref	0.0	Cross-term dependence of qsref.
wqsref	0.0 m	W-term for QSREF.
p2qsref	0.0 m^2	WL-term for QSREF.
lk01	0	Length dependence of k01.
nk01	0	NFIN dependence of k01.
pk01	0	Cross-term dependence of k01.
wk01	0	W-term dependence of k01.
p2k01	0	WL-term dependence of k01.
lk0si1	0	Length dependence of k0si1.
nk0si1	0	NFIN dependence of k0si1.
pk0si1	0	Cross-term dependence of k0si1.
wk0si1	0	W-term dependence of k0si1.
p2k0si1	0	WL-term dependence of k0si1.
lk1si1	0	Length dependence of k1si1.
nk1si1	0	NFIN dependence of k1si1.
pk1si1	0	Cross-term dependence of k1si1.

© 2023 Cadence Design Systems, Inc.

lk11	0	Length dependence of k11.
nk11	0	NFIN dependence of k11.
pk11	0	Cross-term dependence of k11.
wk11	0	W-term dependence of k11.
p2k11	0	WL-term dependence of k11.
lk1sat1	0	Length dependence of k1sat1.
nk1sat1	0	NFIN dependence of k1sat1.
pk1sat1	0	Cross-term dependence of k1sat1.
la11	0	Length dependence of a11.
na11	0	NFIN dependence of a11.
pa11	0	Cross-term dependence of a11.
wa11	0	W-term dependence of a11.
p2a11	0	WL-term dependence of a11.
la21	0	Length dependence of a21.
na21	0	NFIN dependence of a21.
pa21	0	Cross-term dependence of a21.
wa21	0	W-term dependence of a21.
p2a21	0	WL-term dependence of a21.
laigbinv1	0	Length dependence of aigbinv1.

© 2023 Cadence Design Systems, Inc.

naigbinv1	0	NFIN dependence of aigbinv1.
paigbinv1	0	Cross-term dependence of aigbinv1.
waigbinv1	0	W-term dependence of aigbinv1.
p2aigbinv1	0	WL-term dependence of aigbinv1.
laigbacc1	0	Length dependence of aigbacc1.
naigbacc1	0	NFIN dependence of aigbacc1.
paigbacc1	0	Cross-term dependence of aigbacc1.
waigbacc1	0	W-term dependence of aigbacc1.
p2aigbacc1	0	WL-term dependence of aigbacc1.
laigd1	0.0	Length dependence of aigd1.
naigd1	0.0	NFIN dependence of aigd1.
paigd1	0.0	Cross-term dependence of aigd1.
waigd1	0.0	W-term dependence of aigd1.
p2aigd1	0.0	WL-term dependence of aigd1.
lalphaii0	0.0	Length dependence of alphaii0.
nalphaii0	0.0	NFIN dependence of alphaii0.
palphaii0	0.0	Cross-term dependence of alphaii0.
walphaii0	0.0	W-term dependence of alphaii0.
p2alphaii0	0.0	WL-term dependence of alphaii0.

© 2023 Cadence Design Systems, Inc.

lalphaii1	0.0	Length dependence of alphaii1.
nalphaii1	0.0	NFIN dependence of alphaii1.
palphaii1	0.0	Cross-term dependence of alphaii1.
walphaii1	0.0	W-term dependence of alphaii1.
p2alphaii1	0.0	WL-term dependence of alphaii1.
lpsatcv	0	Length dependence of psatcv.
npsatcv	0	NFIN dependence of psatcv.
ppsatcv	0	Cross-term dependence of psatcv.
wpsatcv	0	W-term dependence of psatcv.
p2psatcv	0	WL-term dependence of psatcv.
ldeltavsatcv	0	Length dependence of deltavsatcv.
ndeltavsatcv	0	NFIN dependence of deltavsatcv.
pdeltavsatcv	0	Cross-term dependence of deltavsatcv.
wdeltavsatcv	0	W-term dependence of deltavsatcv.
p2deltavsatcv	0	WL-term dependence of deltavsatcv.
la0cv	0.0	Length dependence of psatcv.
na0cv	0.0	NFIN dependence of psatcv.
pa0cv	0.0	Cross-term dependence of psatcv.
lagscv	0.0	Length dependence of psatcv.

© 2023 Cadence Design Systems, Inc.

nagscv	0.0	NFIN dependence of psatcv.
pagscv	0.0	Cross-term dependence of psatcv.
lmexpcv	0.0	Length dependence of psatcv.
nmexpcv	0.0	NFIN dependence of psatcv.
pmexpcv	0.0	Cross-term dependence of psatcv.
lk1sisat	0.0	Length dependence of psatcv.
nk1sisat	0.0	NFIN dependence of psatcv.
pk1sisat	0.0	Cross-term dependence of psatcv.
lk1sisat1	0.0	Length dependence of psatcv.
nk1sisat1	0.0	NFIN dependence of psatcv.
pk1sisat1	0.0	Cross-term dependence of psatcv.
lkgisl	0.0	L-term of kgisl.
nkgisl	0.0	N-term of kgisl.
pkgisl	0.0	P-term of kgisl.
lkgidl	0.0	L-term of kgidl.
nkgidl	0.0	N-term of kgidl.
pkgidl	0.0	P-term of kgidl.
lmgisl	0.0	L-term of mgisl.
nmgisl	0.0	N-term of mgisl.

© 2023 Cadence Design Systems, Inc.

pmgisl	0.0	P-term of mgisl.
lmgidl	0.0	L-term of mgidl.
nmgidl	0.0	N-term of mgidl.
pmgidl	0.0	P-term of mgidl.
lgislfactor	0.0	L-term of gislfactor.
ngislfactor	0.0	N-term of gislfactor.
pgislfactor	0.0	P-term of gislfactor.
lgidlfactor	0.0	L-term of gidlfactor.
ngidlfactor	0.0	N-term of gidlfactor.
pgidlfactor	0.0	P-term of gidlfactor.
lcitr	0	L-term of CITR.
ncitr	0	N-term of CITR.
pcitr	0	P-term of CITR.
wcitr	0	W-term of CITR.
p2citr	0	WL-term of CITR.
ldvtshiftr	0	LDVTSHIFT in reverse mode.
ndvtshiftr	0	NDVTSHIFT in reverse mode.
pdvtshiftr	0	PDVTSHIFT in reverse mode.
wdvtshiftr	0	WDVTSHIFT in reverse mode.

© 2023 Cadence Design Systems, Inc.

p2dvtshiftr	0	P2DVTSHIFT in reverse mode.
lvsatr	0	LVSAT in reverse mode.
nvsatr	0	NVSAT in reverse mode.
pvsatr	0	PVSAT in reverse mode.
wvsatr	0 m^2/s	W-term of VSATR.
p2vsatr	0 m^3/s	WL-term of VSATR.
lksativr	0	LKSATIV in reverse mode.
nksativr	0	NKSATIV in reverse mode.
pksativr	0	PKSATIV in reverse mode.
wksativr	0	WKSATIV in reverse mode.
p2ksativr	0	P2KSATIV in reverse mode.
lu0r	0	LU0 in reverse mode.
nu0r	0	NU0 in reverse mode.
pu0r	0	PU0 in reverse mode.
wu0r	0	WU0 in reverse mode.
p2u0r	0	P2U0 in reverse mode.
luar	0	LUA in reverse mode.
nuar	0	NUA in reverse mode.
puar	0	PUA in reverse mode.

© 2023 Cadence Design Systems, Inc.

wuar	0	WUA in reverse mode.
p2uar	0	P2UA in reverse mode.
lucr	0	LUC in reverse mode.
nucr	0	NUC in reverse mode.
pucr	0	PUC in reverse mode.
wucr	0	LUC in reverse mode.
p2ucr	0	P2UC in reverse mode.
leur	0	LEU in reverse mode.
neur	0	NEU in reverse mode.
peur	0	PEU in reverse mode.
weur	0	WEU in reverse mode.
p2eur	0	P2EU in reverse mode.
ludr	0	LUD in reverse mode.
nudr	0	NUD in reverse mode.
pudr	0	PUD in reverse mode.
wudr	0	WUD in reverse mode.
p2udr	0	P2UD in reverse mode.
lpclmr	0	LPCLM in reverse mode.
npclmr	0	NPCLM in reverse mode.

© 2023 Cadence Design Systems, Inc.

ppclmr	0	PPCLM in reverse mode.
wpclmr	0	WPCLM in reverse mode.
p2pclmr	0	P2PCLM in reverse mode.
lpdibl2r	0	LPDIBL2 in reverse mode.
npdibl2r	0	NPDIBL2 in reverse mode.
ppdibl2r	0	PPDIBL2 in reverse mode.
wpdibl2r	0	WPDIBL2 in reverse mode.
p2pdibl2r	0	P2PDIBL2 in reverse mode.
luter	0.0	LUTE in reverse mode.
nuter	0.0	NUTE in reverse mode.
puter	0.0	PUTE in reverse mode.
wuter	0.0	WUTE in reverse mode.
p2uter	0.0	P2UTE in reverse mode.
lutlr	0.0	LUTL in reverse mode.
nutlr	0.0	NUTL in reverse mode.
putlr	0.0	PUTL in reverse mode.
wutlr	0.0	WUTL in reverse mode.
p2utlr	0.0	P2UTL in reverse mode.
lua1r	0.0	LUA1 in reverse mode.

© 2023 Cadence Design Systems, Inc.

nua1r	0.0	NUA1 in reverse mode.
pua1r	0.0	PUA1 in reverse mode.
wua1r	0.0	WUA1 in reverse mode.
p2ua1r	0.0	P2UA1 in reverse mode.
luc1r	0.0	LUC1 in reverse mode.
nuc1r	0.0	NUC1 in reverse mode.
puc1r	0.0	PUC1 in reverse mode.
wuc1r	0.0	WUC1 in reverse mode.
p2uc1r	0.0	P2UC1 in reverse mode.
lud1r	0.0	LUD1 in reverse mode.
nud1r	0.0	NUD1 in reverse mode.
pud1r	0.0	PUD1 in reverse mode.
wud1r	0.0	WUD1 in reverse mode.
p2ud1r	0.0	P2UD1 in reverse mode.
latr	0	LAT in reverse mode.
natr	0	NAT in reverse mode.
patr	0	PAT in reverse mode.
watr	0	WAT in reverse mode.
p2atr	0	P2AT in reverse mode.

© 2023 Cadence Design Systems, Inc.

latcv	0	Length dependence of atcv.
natcv	0	NFIN dependence of atcv.
patcv	0	Cross-term dependence of atcv.
watcv	0	W-term dependence of atcv.
p2atcv	0	WL-term dependence of atcv.
lk2si	0.0	Length dependence of k2si.
nk2si	0.0	NFIN dependence of k2si.
pk2si	0.0	Cross-term dependence of k2si.
wk2si	0.0	W-term dependence of k2si.
p2k2si	0.0	WL-term dependence of k2si.
lk2si1	0.0	Length dependence of k2si1.
nk2si1	0.0	NFIN dependence of k2si1.
pk2si1	0.0	Cross-term dependence of k2si1.
wk2si1	0.0	W-term dependence of k2si1.
p2k2si1	0.0	WL-term dependence of k2si1.
lk0sisat	0.0	Length dependence of k0sisat.
nk0sisat	0.0	NFIN dependence of k0sisat.
pk0sisat	0.0	Cross-term dependence of k0sisat.
wk0sisat	0.0	W-term dependence of k0sisat.

© 2023 Cadence Design Systems, Inc.

p2k0sisat	0.0	WL-term dependence of k0sisat.
lk0sisat1	0.0	Length dependence of k0sisat1.
nk0sisat1	0.0	NFIN dependence of k0sisat1.
pk0sisat1	0.0	Cross-term dependence of k0sisat1.
wk0sisat1	0.0	W-term dependence of k0sisat1.
p2k0sisat1	0.0	WL-term dependence of k0sisat1.
lk2sisat	0.0	Length dependence of k2sisat.
nk2sisat	0.0	NFIN dependence of k2sisat.
pk2sisat	0.0	Cross-term dependence of k2sisat.
wk2sisat	0.0	W-term dependence of k2sisat.
p2k2sisat	0.0	WL-term dependence of k2sisat.
lk2sisat1	0.0	Length dependence of k2sisat1.
nk2sisat1	0.0	NFIN dependence of k2sisat1.
pk2sisat1	0.0	Cross-term dependence of k2sisat1.
wk2sisat1	0.0	W-term dependence of k2sisat1.
p2k2sisat1	0.0	WL-term dependence of k2sisat1.
lk2sat	0.0	Length dependence of k2sat.
nk2sat	0.0	NFIN dependence of k2sat.
pk2sat	0.0	Cross-term dependence of k2sat.

© 2023 Cadence Design Systems, Inc.

wk2sat	0.0	W-term dependence of k2sat.
p2k2sat	0.0	WL-term dependence of k2sat.
lk2sat1	0.0	Length dependence of k2sat1.
nk2sat1	0.0	NFIN dependence of k2sat1.
pk2sat1	0.0	Cross-term dependence of k2sat1.
wk2sat1	0.0	W-term dependence of k2sat1.
p2k2sat1	0.0	WL-term dependence of k2sat1.
lk2	0.0	Length dependence of k2.
nk2	0.0	NFIN dependence of k2.
pk2	0.0	Cross-term dependence of k2.
wk2	0.0	W-term dependence of k2.
p2k2	0.0	WL-term dependence of k2.
lk21	0.0	Length dependence of k21.
nk21	0.0	NFIN dependence of k21.
pk21	0.0	Cross-term dependence of k21.
wk21	0.0	W-term dependence of k21.
p2k21	0.0	WL-term dependence of k21.
lupr	0.0	Length dependence of upr.
nupr	0.0	NFIN dependence of upr.

© 2023 Cadence Design Systems, Inc.

pupr	0.0	Cross-term dependence of upr.
wupr	0.0	W-term dependence of upr.
p2upr	0.0	WL-term dependence of upr.
dim1h	3	Max dimension for 1st subband (real number enables optimization).
dimension1	2	Dimension for 1st subband (real number enables optimization).
ldimension1	0.0 m	L-term of DIMENSION1.
ndimension1	0.0	N-term of DIMENSION1.
pdimension1	0.0 m	P-term of DIMENSION1.
wdimension1	0.0 m	W-term of DIMENSION1.
p2dimension1	0.0 m^2	WL-term of DIMENSION1.
dim2h	3	Max dimension for 2nd subband (real number enables optimization).
dimension2	2.6	Dimension for 2nd subband (real number enables optimization).
ldimension2	0.0 m	L-term of DIMENSION2.
ndimension2	0.0	N-term of DIMENSION2.
pdimension2	0.0 m	P-term of DIMENSION2.
wdimension2	0.0 m	W-term of DIMENSION2.
p2dimension2	0.0 m^2	WL-term of DIMENSION2.

© 2023 Cadence Design Systems, Inc.

dim3h	3	Max dimension for 3rd subband (real number enables optimization).
dimension3	2.6	Dimension for 3rd subband (real number enables optimization).
ldimension3	0.0 m	L-term of DIMENSION3.
ndimension3	0.0	N-term of DIMENSION3.
pdimension3	0.0 m	P-term of DIMENSION3.
wdimension3	0.0 m	W-term of DIMENSION3.
p2dimension3	0.0 m^2	WL-term of DIMENSION3.
wdim0	9.5e-9 m	WGAA at which dimension change happens.
wdimr	0.1 nm	Rate of dimension change with WGAA scaling.
ssp1	14	Subband smoothing parameter for 1st subband (WGAA<WSSP0).
lssp1	0.0 m	L-term of SSP1.
nssp1	0.0	N-term of SSP1.
pssp1	0.0 m	P-term of SSP1.
wssp1	0.0 m	W-term of SSP1.
p2ssp1	0.0 m^2	WL-term of SSP1.
ssp2	24	Subband smoothing parameter for 2nd subband (WGAA<WSSP0).
lssp2	0.0 m	L-term of SSP2.
nssp2	0.0	N-term of SSP2.

© 2023 Cadence Design Systems, Inc.

pssp2	0.0 m	P-term of SSP2.
wssp2	0.0 m	W-term of SSP2.
p2ssp2	0.0 m^2	WL-term of SSP2.
ssp3	24	Subband smoothing parameter for 3rd subband (WGAA<WSSP0).
lssp3	0.0 m	L-term of SSP3.
nssp3	0.0	N-term of SSP3.
pssp3	0.0 m	P-term of SSP3.
wssp3	0.0 m	W-term of SSP3.
p2ssp3	0.0 m^2	WL-term of SSP3.
dssp1	2	Change in SSP1 with WGAA scaling for large WGAA>WSSP0.
dssp2	0 m	Change in SSP2 with WGAA scaling for large WGAA>WSSP0.
dssp3	0	Change in SPP3 with WGAA scaling for large WGAA>WSSP0.
wssp0	9.5e-9 m	WGAA around which SSP change happens.
wsspr	0.1 nm	Rate of SSP change with WGAA scaling.
wgaanom	8e-9 m^2	Nominal WGAA.
e2nom	0.139 eV	2nd subband energy for nominal WGAA.
le2nom	0.0 m eV	L-term of E2NOM.
ne2nom	0.0 eV	N-term of E2NOM.

© 2023 Cadence Design Systems, Inc.

pe2nom	0.0 m eV	P-term of E2NOM.
we2nom	0.0 m eV	W-term of E2NOM.
p2e2nom	0.0 (m^2) eV	WL-term of E2NOM.
e3nom	2 eV	3rd subband energy for nominal WGAA.
le3nom	0.0 m eV	L-term of E3NOM.
ne3nom	0.0 ev	N-term of E3NOM.
pe3nom	0.0 m eV	P-term of E3NOM.
we3nom	0.0 m eV	W-term of E3NOM.
p2e3nom	0.0 (m^2) eV	WL-term of E3NOM.
mfe2	1	Rate of change in 2nd subband energy with WGAA and TGAA scaling.
mfe3	1	Rate of change in 3rd subband energy with WGAA and TGAA scaling.
wsfe2	1	WGAA scaling factor for 2nd subband energy.
wsfe3	1	WGAA scaling factor for 3rd subband energy.
mfq1nom	11.2	Scaling factor for 1st subband charge for nominal WGAA.
lmfq1nom	0.0 m	L-term of MFQ1NOM.
nmfq1nom	0.0	N-term of MFQ1NOM.
pmfq1nom	0.0 m	P-term of MFQ1NOM.

© 2023 Cadence Design Systems, Inc.

wmfq1nom	0.0 m	W-term of MFQ1NOM.
p2mfq1nom	0.0 m^2	WL-term of MFQ1NOM.
mfq2nom	8.02	Scaling factor for 2nd subband charge for nominal WGAA.
lmfq2nom	0.0 m	L-term of MFQ2NOM.
nmfq2nom	0.0	N-term of MFQ2NOM.
pmfq2nom	0.0 m	P-term of MFQ2NOM.
wmfq2nom	0.0 m	W-term of MFQ2NOM.
p2mfq2nom	0.0 m^2	WL-term of MFQ2NOM.
mfq3nom	6.18	Scaling factor for 3rd subband charge for nominal WHSEET.
lmfq3nom	0.0 m	L-term of MFQ3NOM.
nmfq3nom	0.0	N-term of MFQ3NOM.
pmfq3nom	0.0 m	P-term of MFQ3NOM.
wmfq3nom	0.0 m	W-term of MFQ3NOM.
p2mfq3nom	0.0 m^2	WL-term of MFQ3NOM.
mfq1	1	Rate of change in 1st subband charge with WGAA and TGAA scaling.
mfq2	1	Rate of change in 2nd subband charge with WGAA and TGAA scaling.
mfq3	1	Rate of change in 3rd subband charge with WGAA and TGAA scaling.

© 2023 Cadence Design Systems, Inc.

wsfq1	1	WGAA scaling factor for 1st subband charge.
wsfq2	1	WGAA scaling factor for 2nd subband charge.
wsfq3	1	WGAA scaling factor for 3rd subband charge.
tsre2	1.8	TGAA scaling for 2nd subband energy.
tdwse2	1.0	TGAA dependence of WGAA scaling for 2nd subband energy.
tsre3	0.67	TGAA scaling for 3rd subband energy .
tdwse3	0.23	TGAA dependence of WGAA scaling for 3rd subband energy.
tsrq1	1.1	TGAA scaling for 1st subband charge.
tdwsq1	2.4	TGAA dependence of WGAA scaling for 1st subband charge.
tsrq2	2.0	TGAA scaling for 2nd subband charge.
tdwsq2	2.0	TGAA dependence of WGAA scaling for 2nd subband charge.
tsrq3	6.0	TGAA scaling for 3rd subband charge.
tdwsq3	2.4	TGAA dependence of WGAA scaling for 3rd subband charge.
vds_max	infinity V	Maximum allowed voltage across source and drain.
vgd_max	infinity V	Maximum allowed voltage across drain and gate.
vgs_max	infinity V	Maximum allowed voltage across source/bulk and gate.

© 2023 Cadence Design Systems, Inc.

vbd_max	infinity V	Maximum allowed voltage across drain/source and bulk.
vbs_max	vbd_max V	Maximum allowed voltage across source and bulk.
vgb_max	infinity V	Maximum allowed voltage across gate and bulk.
vgdr_max	vgd_max V	Maximum allowed reverse voltage across gate and drain.
vgsr_max	vgs_max V	Maximum allowed reverse voltage across gate and source.
vgbr_max	vgb_max V	Maximum allowed reverse voltage across gate and bulk.
vbsr_max	vbs_max V	Maximum allowed reverse voltage across bulk and source.
vbdr_max	vbd_max V	Maximum allowed reverse voltage across bulk and drain.
mvtwl	0.0 V m	Threshold mismatch area dependence.
mvtwl2	0.0 V m^1.5	Threshold mismatch area square dependence.
mvt0	0.0 V	Threshold mismatch intercept.
mbewl	0.0 m	Beta mismatch area dependence.
mbe0	0.0	Beta mismatch intercept.
mismatchmod	0	Select mismatch mode. The available modes are 0, 1, 2 and 3.
mismatchdist	0.0	Mismatch distance.

© 2023 Cadence Design Systems, Inc.

trise	0 C	Temperature rise from ambient, alias of dtemp. It served as the default value of instance trise.
lmin	0.0 m	Minimum channel length for which the model is valid.
lmax	1.0 m	Maximum channel length for which the model is valid.
wmin	0.0 m	Minimum channel width for which the model is valid.
wmax	1.0 m	Maximum channel width for which the model is valid.
nfinmin	1	Minimum number of fins per finger.
nfinmax	100000	Maximum number of fins per finger.
cvmod	0	0: Consistent I-V & C-V, 1: Decoupled I-V & C-V.
cryomod	0	0: Turn off cryogenic temperature model; 1: Most physical cryogenic temperature models; 2: Cryogenic models converge to BSIM-CMG 111.1.0 temperature models for T > 210 K.
dwcacc	0	GAA delta W for C-V model in accumulation region (CAPMOD=1, BULKMOD=1 or 2).
dwbin	0	GAA Delta W for binning.
lxw	0.0 m^2	L-term of XW.
nxw	0.0 m	N-term of XW.
pxw	0.0 m^2	P-term of XW.
wxw	0.0 m^2	W-term of XW.
p2xw	0.0 m^3	WL-term of XW.

© 2023 Cadence Design Systems, Inc.

ldwbin	0.0 m^2	L-term of DWBIN.
ndwbin	0.0 m	N-term of DWBIN.
pdwbin	0.0 m^2	P-term of DWBIN.
wdwbin	0.0 m^2	W-term of DWBIN.
p2dwbin	0.0 m^3	WL-term of DWBIN.
eta0cv	0.60	CVMOD = 1 DIBL coefficient.
uds	2.0e-5	CRYOMOD != 0 weight factor correction for source side inversion charge density in Coulomb scattering model.
uds1	(-10.0)	CRYOMOD != 0 temperature coefficient for UDS.
udd	(-2.0e-5)	CRYOMOD != 0 weight factor correction for drain side inversion charge density in Coulomb scattering model.
udd1	(-10.0)	CRYOMOD != 0 temperature coefficient for UDD.
pclmt	(-2.0e-5)	CRYOMOD != 0 temperature coefficient for PCLM.
cgbw	0.0	GAA gate-to-substrate overlap capacitance per unit area per fin per finger.
kt11	0.01 V	CRYOMOD != 0 Vth temperature coefficient.
kt12	0.1 1/K	CRYOMOD != 0 Vth temperature coefficient.
tvth	40.0 K	CRYOMOD != 0 transition temperature for Vth temperature model.
ute1	(-0.4)	CRYOMOD != 0 mobility temperature coefficient.

© 2023 Cadence Design Systems, Inc.

ua2	(-0.04)	CRYOMOD != 0 mobility temperature coefficient for UA.
eu1	(-1.0e-3)	CRYOMOD != 0 mobility temperature coefficient for EU.
ud2	(-0.04)	CRYOMOD != 0 mobility temperature coefficient for UD.
ucste1	(-0.04)	CRYOMOD != 0 mobility temperature coefficient for UCS.
at2	2.0e-6 $1/K^2$	CRYOMOD != 0 saturation velocity temperature coefficient.
tmexp2	(-4.0e-6) $1/K^2$	CRYOMOD != 0 Temperature coefficient for Vdseff smoothing.
prt1	4.0e-4	CRYOMOD != 0 series resistance temperature coefficient at low temperatures.
tr0	170.0	CRYOMOD != 0 corner temperature in dual-slope temperature model of series resistance.
sprt	1.0e-2	CRYOMOD != 0 parameter for corner temperature smoothing in dual-slope temperature model of series resistance.
eta0n1cv	0	NFIN dependence of ETA0CV.
eta0n2cv	1.0e5	NFIN dependence of ETA0CV.
teta0cv	0.0 1/K	CVMOD = 1 temperature dependence of DIBL coefficient.
u0n1cv	0	CVMOD = 1 NFIN dependence of U0CV.
u0n2cv	1.0e5	CVMOD = 1 NFIN dependence of U0CV.

© 2023 Cadence Design Systems, Inc.

at2cv	2.0e-6	CRYOMOD != 0 saturation velocity temperature coefficient for CV.
u0cv	0.03	CVMOD = 1 low-field mobility.
uacv	0.3	CVMOD = 1 phonon/surface roughness scattering parameter.
uccv	0.0	CVMOD = 1 body effect for mobility degradation parameter (BULKMOD = 1 or 2).
udcv	0.0	CVMOD = 1 coulomb scattering parameter.
utecv	0.0	CVMOD = 1 mobility temperature coefficient.
ute1cv	(-0.4)	CRYOMOD != 0 and CVMOD = 1 mobility temperature coefficient.
utlcv	(-1.5e-3)	CVMOD = 1 mobility temperature coefficient.
ua1cv	1.032e-3	CVMOD = 1 mobility temperature coefficient for UA.
ua2cv	(-0.04)	CRYOMOD != 0 and CVMOD = 1 mobility temperature coefficient for UA.
uc1cv	0.056e-9	CVMOD = 1 mobility temperature coefficient for UC.
ud1cv	0.0	CVMOD = 1 mobility temperature coefficient for UD.
ud2cv	(-0.04)	CRYOMOD != 0 and CVMOD = 1 mobility temperature coefficient for UD.
eta0ltcv	0.0 1/m	Coupled NFIN and length dependence of ETA0CV.
u0ltcv	0.0 1/m	Coupled NFIN and length dependence of U0CV.
leta0cv	0	Length dependence of eta0cv.

© 2023 Cadence Design Systems, Inc.

neta0cv	0	NFIN dependence of eta0cv.
peta0cv	0	Cross-term dependence of eta0cv.
weta0cv	0	W-term dependence of eta0cv.
p2eta0cv	0	WL-term dependence of eta0cv.
ksativt1	(-2.0e-4) 1/K	CRYOMOD != 0 temperature coefficient for KSATIV.
ksativt2	(-2.0e-4) $1/K^2$	CRYOMOD != 0 temperature coefficient for KSATIV.
luds	0	L-term of UDS.
nuds	0	N-term of UDS.
puds	0	P-term of UDS.
wuds	0	W-term of UDS.
p2uds	0	WL-term of UDS.
luds1	0	L-term of UDS1.
nuds1	0	N-term of UDS1.
puds1	0	P-term of UDS1.
wuds1	0	W-term of UDS1.
p2uds1	0	WL-term of UDS1.
ludd	0	L-term of UDD.
nudd	0	N-term of UDD.

© 2023 Cadence Design Systems, Inc.

pudd	0	P-term of UDD.
wudd	0	W-term of UDD.
p2udd	0	WL-term of UDD.
ludd1	0	L-term of UDD1.
nudd1	0	N-term of UDD1.
pudd1	0	P-term of UDD1.
wudd1	0	W-term of UDD1.
p2udd1	0	WL-term of UDD1.
lucste1	0.0	Length dependence of ucste1.
nucste1	0.0	NFIN dependence of ucste1.
pucste1	0.0	Cross-term dependence of ucste1.
wucste1	0.0	W-term dependence of ucste1.
p2ucste1	0.0	WL-term dependence of ucste1.
lprt1	0	Length dependence of prt1.
nprt1	0	NFIN dependence of prt1.
pprt1	0	Cross-term dependence of prt1.
wprt1	0	W-term dependence of prt1.
p2prt1	0	WL-term dependence of prt1.
ltr0	0	Length dependence of tr0.

© 2023 Cadence Design Systems, Inc.

ntr0	0	NFIN dependence of tr0.
ptr0	0	Cross-term dependence of tr0.
wtr0	0	W-term dependence of tr0.
p2tr0	0	WL-term dependence of tr0.
lsprt	0	Length dependence of sprt.
nsprt	0	NFIN dependence of sprt.
psprt	0	Cross-term dependence of sprt.
wsprt	0	W-term dependence of sprt.
p2sprt	0	WL-term dependence of sprt.
lu0cv	0	L-term of U0CV.
nu0cv	0	N-term of U0CV.
pu0cv	0	P-term of U0CV.
wu0cv	0	W-term of U0CV.
p2u0cv	0	WL-term of U0CV.
luacv	0	L-term of UACV.
nuacv	0	N-term of UACV.
puacv	0	P-term of UACV.
wuacv	0	W-term of UACV.
p2uacv	0	WL-term of UACV.

© 2023 Cadence Design Systems, Inc.

luccv	0	L-term of UCCV.
nuccv	0	N-term of UCCV.
puccv	0	P-term of UCCV.
wuccv	0	W-term of UCCV.
p2uccv	0	WL-term of UCCV.
ludcv	0	L-term of UDCV.
nudcv	0	N-term of UDCV.
pudcv	0	P-term of UDCV.
wudcv	0	W-term of UDCV.
p2udcv	0	WL-term of UDCV.
lutecv	0.0	L-term of UTECV.
nutecv	0.0	N-term of UTECV.
putecv	0.0	P-term of UTECV.
wutecv	0.0	W-term of UTECV.
p2utecv	0.0	WL-term of UTECV.
lute1	0.0	L-term of UTE1.
nute1	0.0	N-term of UTE1.
pute1	0.0	P-term of UTE1.
wute1	0.0	W-term of UTE1.

© 2023 Cadence Design Systems, Inc.

p2ute1	0.0	WL-term of UTE1.
lute1cv	0.0	L-term of UTE1CV.
nute1cv	0.0	N-term of UTE1CV.
pute1cv	0.0	P-term of UTE1CV.
wute1cv	0.0	W-term of UTE1CV.
p2ute1cv	0.0	WL-term of UTE1CV.
lutlcv	0.0	L-term of UTLCV.
nutlcv	0.0	N-term of UTLCV.
putlcv	0.0	P-term of UTLCV.
wutlcv	0.0	W-term of UTLCV.
p2utlcv	0.0	WL-term of UTLCV.
lua1cv	0.0	L-term of UA1CV.
nua1cv	0.0	N-term of UA1CV.
pua1cv	0.0	P-term of UA1CV.
wua1cv	0.0	W-term of UA1CV.
p2ua1cv	0.0	WL-term of UA1CV.
lua2	0.0	L-term of UA2.
nua2	0.0	N-term of UA2.
pua2	0.0	P-term of UA2.

© 2023 Cadence Design Systems, Inc.

wua2	0.0	W-term of UA2.
p2ua2	0.0	WL-term of UA2.
lua2cv	0.0	L-term of UA2CV.
nua2cv	0.0	N-term of UA2CV.
pua2cv	0.0	P-term of UA2CV.
wua2cv	0.0	W-term of UA2CV.
p2ua2cv	0.0	WL-term of UA2CV.
leu1	0.0	L-term of EU1.
neu1	0.0	N-term of EU1.
peu1	0.0	P-term of EU1.
weu1	0.0	W-term of EU1.
p2eu1	0.0	WL-term of EU1.
luc1cv	0.0	L-term of UC1CV.
nuc1cv	0.0	N-term of UC1CV.
puc1cv	0.0	P-term of UC1CV.
wuc1cv	0.0	W-term of UC1CV.
p2uc1cv	0.0	WL-term of UC1CV.
lud1cv	0.0	L-term of UD1CV.
nud1cv	0.0	N-term of UD1CV.

© 2023 Cadence Design Systems, Inc.

pud1cv	0.0	P-term of UD1CV.
wud1cv	0.0	W-term of UD1CV.
p2ud1cv	0.0	WL-term of UD1CV.
lud2	0.0	L-term of UD2.
nud2	0.0	N-term of UD2.
pud2	0.0	P-term of UD2.
wud2	0.0	W-term of UD2.
p2ud2	0.0	WL-term of UD2.
lud2cv	0.0	L-term of UD2CV.
nud2cv	0.0	N-term of UD2CV.
pud2cv	0.0	P-term of UD2CV.
wud2cv	0.0	W-term of UD2CV.
p2ud2cv	0.0	WL-term of UD2CV.
agidlb	6.055e-12 1/ohm	Pre-exponential coefficient for parasitic substrate GIDL.
bgidlb	3.0e8 V/m	Exponential coefficient for parasitic substrate GIDL.
cgidlb	0.5 V^3	Parameter for body-effect of parasitic substrate GIDL.
egidlb	0.2 V	Band bending parameter for parasitic substrate GIDL.

© 2023 Cadence Design Systems, Inc.

pgidlb	1.0	Parameter for body-bias effect on parasitic substrate GIDL.
agislb	6.055e-12 1/ohm	Pre-exponential coefficient for parasitic substrate GISL.
bgislb	3.0e8 V/m	Exponential coefficient for parasitic substrate GISL.
cgislb	0.5 V^3	Parameter for body-effect of parasitic substrate GISL.
egislb	0.2 V	Band bending parameter for parasitic substrate GISL.
pgislb	1.0	Parameter for body-bias effect on parasitic substrate GISL.
lagidlb	0.0	L-term of AGIDLB.
nagidlb	0.0	N-term of AGIDLB.
pagidlb	0.0	P-term of AGIDLB.
wagidlb	0.0	W-term of AGIDLB.
p2agidlb	0.0	WL-term of AGIDLB.
lbgidlb	0.0	L-term of BGIDLB.
nbgidlb	0.0	N-term of BGIDLB.
pbgidlb	0.0	P-term of BGIDLB.
wbgidlb	0.0	W-term of BGIDLB.
p2bgidlb	0.0	WL-term of BGIDLB.
lcgidlb	0.0	L-term of CGIDLB.

© 2023 Cadence Design Systems, Inc.

ncgidlb	0.0	N-term of CGIDLB.
pcgidlb	0.0	P-term of CGIDLB.
wcgidlb	0.0	W-term of CGIDLB.
p2cgidlb	0.0	WL-term of CGIDLB.
legidlb	0.0	L-term of EGIDLB.
negidlb	0.0	N-term of EGIDLB.
pegidlb	0.0	P-term of EGIDLB.
wegidlb	0.0	W-term of EGIDLB.
p2egidlb	0.0	WL-term of EGIDLB.
lpgidlb	0.0	L-term of PGIDLB.
npgidlb	0.0	N-term of PGIDLB.
ppgidlb	0.0	P-term of PGIDLB.
wpgidlb	0.0	W-term of PGIDLB.
p2pgidlb	0.0	WL-term of PGIDLB.
lagislb	0.0	L-term of AGISLB.
nagislb	0.0	N-term of AGISLB.
pagislb	0.0	P-term of AGISLB.
wagislb	0.0	W-term of AGISLB.
p2agislb	0.0	WL-term of AGISLB.

© 2023 Cadence Design Systems, Inc.

lbgislb	0.0	L-term of BGISLB.
nbgislb	0.0	N-term of BGISLB.
pbgislb	0.0	P-term of BGISLB.
wbgislb	0.0	W-term of BGISLB.
p2bgislb	0.0	WL-term of BGISLB.
lcgislb	0.0	L-term of CGISLB.
ncgislb	0.0	N-term of CGISLB.
pcgislb	0.0	P-term of CGISLB.
wcgislb	0.0	W-term of CGISLB.
p2cgislb	0.0	WL-term of CGISLB.
legislb	0.0	L-term of EGISLB.
negislb	0.0	N-term of EGISLB.
pegislb	0.0	P-term of EGISLB.
wegislb	0.0	W-term of EGISLB.
p2egislb	0.0	WL-term of EGISLB.
lpgislb	0.0	L-term of PGISLB.
npgislb	0.0	N-term of PGISLB.
ppgislb	0.0	P-term of PGISLB.
wpgislb	0.0	W-term of PGISLB.

© 2023 Cadence Design Systems, Inc.

p2pgislb	0.0	WL-term of PGISLB.
tlow	50.0	CRYOMOD != 0 transition temperature of subthreshold swing at low temperatures.
tlow1	0.0	CRYOMOD != 0 transition temperature of subthreshold swing at low temperatures.
dtlow	1.0	CRYOMOD != 0 smoothing parameter for TLOW.
dtlow1	1e-3	CRYOMOD != 0 smoothing parameter for TLOW1.
klow1	0.0	CRYOMOD != 0 slope magnitude of effective temperature below TLOW1.
nvsrd	5.0e16 $1/m^2$	Charge density in the drain region.
vsatrsd	1.0e5 m/sec	Saturation velocity in S/D region.
ptwgvsrsd	0.0 1/V	VSATRSD variation with gate bias.
ptwg1vsrsd	0.0 V	VSATRSD variation with gate bias.
psatxvsrsd	60.0 V	Fine tuning of PTWGVSRSD effect.
mvsrsd	1.0	Non-linear resistance parameter.
nvsrs	5.0e16 $1/m^2$	Charge density in the source region.
rdlcw	0.0 Ω µm^WR	'R'esistance of the 'D'rain region at 'L'ow 'C'urrent.
rslcw	0.0 Ω µm^WR	'R'esistance of the 'S'ource region at 'L'ow 'C'urrent.

© 2023 Cadence Design Systems, Inc.

prtvsrsd	0.0	Temperature coefficient of resistance in S/D velocity saturation model.
atvsrsd	0.0 m/s	Temperature coefficient for S/D region saturation velocity.
vsrdfactor	1.0e-3	Parameter for delta_vsrd tuning.
vsrsfactor	1.0e-3	Parameter for delta_vsrs tuning.
rdvds	8.0 V	Parameter for Isat_rd variation with drain voltage.
gavsrd	0.0 1/V	Parameter for Isat_rd variation with drain voltage.

© 2023 Cadence Design Systems, Inc.

Output Parameters

weff	(m)	Effective channel width.
leff	(m)	Effective channel length.
weffcv	(m)	Effective channel width for C-V.
leffcv	(m)	Effective channel length for C-V.
rsgeo	(Ω)	External bias-independent source resistance.
rdgeo	(Ω)	External bias-independent drain resistance.
cfgeo	(F)	Geometric parasitic capacitance for cgeomod=1.
tempeff	(C)	Effective temperature without selfheating temperature.
meff		Effective multiplicity factor (m-factor).

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

a0cv M-430 lcigs M-1089 nutl M-1315 pxrcrg1 M-1301
a1 M-163 lcit M-688 nutlr M-1567 pxrcrg2 M-1306
a11 M-484 lcitr M-1506 nvasat M-926 qb OP-44
a2 M-164 lckappab M-1279 nvsat M-812 qbi OP-40

© 2023 Cadence Design Systems, Inc.

a21 M-485
abulkcon M-428
abulkmod M-427
ach_ufcm M-624
acs M-153
adej I-14
adej M-14
adeo I-10
adeo M-10
advtp0 M-593
advtp1 M-595
aeu M-142
aeur M-569
af_hv M-390
afds M-386
afrd M-385
afrs M-384
agidl M-258
agisl M-253
lckappad M-1269
lckappas M-1264
lcovd M-1249
lcovs M-1244
lcs M-912
ldeltavsat M-831
ldeltavsatcv M-1468
ldg M-202
ldimension1 M-1653
ldimension2 M-1660
ldimension3 M-1667
ldlbin M-680
ldrout M-991
ldsub M-738
ldvt0 M-708
ldvt1 M-713
ldvt1ss M-718
ldvtb M-784
ldvtp0 M-438
nvsat1 M-817
nvsat1r M-822
nvsatcv M-842
nvsatr M-1517
nvtm M-553
nwr M-972
nxl M-675
nxrcrg1 M-1300
nxrcrg2 M-1305
p2a1 M-937
p2a11 M-1432
p2a2 M-942
p2a21 M-1437
p2agidl M-1123
p2agisl M-1148
p2aigbacc M-1030
p2aigbacc1 M-1447
p2aigbinv M-1005
p2aigbinv1 M-1442
qd OP-42
qdi OP-38
qg OP-41
qgi OP-37
qm0 M-103
qm0acc M-105
qmfactor M-96
qmfactorcv M-629
qmtcencv M-98
qmtcencva M-99
qmtcencvo M-608
qmtceniv M-97
qs OP-43
qsi OP-39
qsref M-397
rcvfac M-483
rdc I-25
rddr M-180
rddrr M-181

© 2023 Cadence Design Systems, Inc.

agscv M-431
aigbacc M-230
aigbacc1 M-487
aigbinv M-225
aigbinv1 M-486
aigc M-237
aigc1 M-488
aigd M-247
aigd1 M-490
aigen M-360
aigs M-243
aigs1 M-489
alpha0 M-263
alpha01 M-491
alpha1 M-264
alpha11 M-492
alpha_ufcm M-630
alphaii M-266
alphaii0 M-493
ldvtp1 M-443
ldvtshift M-753
ldvtshiftr M-1511
le2nom M-1699
le3nom M-1705
leff O-2
leffcv O-4
legidl M-1129
legisl M-1154
leigbinv M-1016
lemobt M-1319
lesatii M-1204
leta0 M-728
leta0r M-733
letamob M-874
leu M-894
leur M-1541
lgidlfactor M-1503
lgislfactor M-1500
p2aigc M-1050
p2aigc1 M-1055
p2aigd M-1098
p2aigd1 M-1452
p2aigen M-1293
p2aigs M-1078
p2aigs1 M-1083
p2alpha0 M-1173
p2alpha1 M-1178
p2alphaii M-1188
p2alphaii0 M-1457
p2alphaii1 M-1462
p2at M-1353
p2atcv M-1595
p2atr M-1590
p2beta0 M-1183
p2betaii0 M-1193
p2betaii1 M-1198
p2betaii2 M-1203
rdgeo O-6
rdsmod M-35
rdsw M-166
rdswmin M-165
rdw M-174
rdwmin M-173
region I-42
region OP-1
reversed OP-95
rgatemod M-43
rgeoa M-210
rgeob M-211
rgeoc M-212
rgeod M-213
rgeoe M-214
rgeomod M-44
rgext M-189
rgfin M-190
rhoc M-195

© 2023 Cadence Design Systems, Inc.

alphaii01 M-494
alphaii1 M-495
alphaii11 M-496
alphaqm M-107
amexp M-124
amexpcv M-433
amexpr M-528
apclm M-156
apclmr M-575
apsat M-117
apsatcv M-500
aptwg M-128
aqmtcen M-100
ardsw M-167
ardw M-175
arsdend M-207
arsw M-171
asej I-13
asej M-13
aseo I-9
aseo M-9
ligt M-1387
lii M-271
liit M-1372
lint M-50
lintigen M-358
lintnoi M-392
lk0 M-763
lk01 M-1407
lk0si M-768
lk0si1 M-1412
lk0sisat M-1606
lk0sisat1 M-1611
lk1 M-773
lk11 M-1420
lk1rsce M-743
lk1sat M-781
lk1sat1 M-1425
lk1si M-778
lk1si1 M-1417
lk1sisat M-1482
lk1sisat1 M-1485
p2bgidl M-1128
p2bgisl M-1153
p2bigbacc M-1035
p2bigbinv M-1010
p2bigc M-1060
p2bigd M-1103
p2bigen M-1298
p2bigs M-1088
p2cdsc M-697
p2cdscd M-702
p2cdscdr M-707
p2cfd M-1243
p2cfs M-1238
p2cgbl M-1278
p2cgdl M-1263
p2cgidl M-1138
p2cgisl M-1163
p2cgsl M-1258
p2cigbacc M-1040
p2cigbinv M-1015
p2cigc M-1065
rhoext M-197
rhorsd M-196
rnoia M-403
rnoib M-404
rnoic M-587
rnoik M-589
rout OP-7
rsc I-24
rsdr M-178
rsdrr M-179
rsgeo O-5
rshd M-192
rshs M-191
rsw M-170
rswmin M-169
rth0 M-474
rtn_m I-33
rtn_mc M-374
rtnamp M-376
rtnampmc M-379
rtnfc M-375

© 2023 Cadence Design Systems, Inc.

ashexp M-622
asiliend M-206
asymmod M-36
at M-422
atcv M-554
athetamu M-150
athetasat M-131
atr M-583
aua M-138
auar M-565
aud M-145
audr M-572
avsat M-109
avsat1 M-113
avsatcv M-121
bcs M-154
bdvtp0 M-594
bdvtp1 M-596
beta OP-15
lk2 M-1636
lk21 M-1641
lk2sat M-1626
lk2sat1 M-1631
lk2si M-1596
lk2si1 M-1601
lk2sisat M-1616
lk2sisat1 M-1621
lkgidl M-1491
lkgisl M-1488
lksativ M-836
lksativr M-1521
lkt1 M-1362
ll M-51
llc M-56
llii M-1209
llint M-677
lln M-52
llpe0 M-748
p2cigd M-1108
p2cigs M-1093
p2cit M-692
p2citr M-1510
p2ckappab M-1283
p2ckappad M-1273
p2ckappas M-1268
p2covd M-1253
p2covs M-1248
p2deltavsat M-835
p2deltavsatcv M-1472
p2dimension1 M-1657
p2dimension2 M-1664
p2dimension3 M-1671
p2drout M-995
p2dsub M-742
p2dvt0 M-712
p2dvt1 M-717
p2dvt1ss M-722
rtnfcmc M-378
rtnfmod M-371
rtnmcloop M-373
rtnmcmod M-372
rtnmod M-370
rtnpr M-377
sdterm M-200
sft OP-102
sh_warn M-47
shmod M-42
sii0 M-272
sii1 M-273
sii2 M-274
siid M-275
sjd M-312
sjs M-311
sjswd M-314
sjswgd M-316
sjswgs M-315

© 2023 Cadence Design Systems, Inc.

beta0 M-265
betaii0 M-267
betaii1 M-268
betaii2 M-269
beu M-143
beur M-570
bg0sub M-72
bgidl M-259
bgisl M-254
bigbacc M-231
bigbinv M-226
bigc M-238
bigd M-248
bigen M-361
bigs M-244
binunit M-2
bmexp M-125
bmexpcv M-434
bmexpr M-529
bpclm M-157
llpeb M-787
lmax M-1768
lmexp M-846
lmexpcv M-1479
lmexpr M-851
lmfq1nom M-1715
lmfq2nom M-1721
lmfq3nom M-1727
lmgidl M-1497
lmgisl M-1494
lmin M-1767
lmpower M-1397
lmue M-909
lnbody M-666
lngate M-683
lnigbacc M-1041
lnigbinv M-1021
lnigc M-1066
lnoia2 M-1392
lntgen M-1284
p2dvtp0 M-442
p2dvtp1 M-447
p2dvtshift M-757
p2dvtshiftr M-1515
p2e2nom M-1703
p2e3nom M-1709
p2egidl M-1133
p2egisl M-1158
p2eigbinv M-1020
p2emobt M-1323
p2esatii M-1208
p2eta0 M-732
p2eta0r M-737
p2etamob M-878
p2eu M-898
p2eur M-1545
p2igt M-1391
p2iit M-1376
p2k0 M-767
p2k01 M-1411
sjsws M-313
smooth M-394
ssp1 M-1674
ssp2 M-1680
ssp3 M-1686
stcs M-421
stmue M-420
stthetamu M-419
stthetasat M-448
subbandmod I-54
subbandmod M-645
t_delta_sh OP-107
t_total_c OP-106
t_total_k OP-105
tbgasub M-407
tbgbsub M-408
tcj M-454
tcjsw M-455
tcjswg M-456
tdevice OP-104

© 2023 Cadence Design Systems, Inc.

bpclmr M-576
bpsat M-118
bpsatcv M-501
bptwg M-129
bqmtcen M-101
brdsw M-168
brdw M-176
brsw M-172
bshexp M-623
bthetamu M-151
bthetasat M-132
bua M-139
buar M-566
bud M-146
budr M-573
bulkmod M-29
bvd M-336
bvs M-335
bvsat M-110
bvsat1 M-114
lntox M-1109
lpa M-136
lpar M-563
lpclm M-915
lpclmcv M-928
lpclmg M-920
lpclmr M-1551
lpdibl1 M-976
lpdibl1r M-981
lpdibl2 M-986
lpdibl2r M-1556
lpe0 M-86
lpeb M-95
lpgidl M-1139
lpgisl M-1164
lphibe M-758
lphig M-669
lphin M-723
lpigcd M-1069
lpoly OP-94
p2k0si M-772
p2k0si1 M-1416
p2k0sisat M-1610
p2k0sisat1 M-1615
p2k1 M-777
p2k11 M-1424
p2k1rsce M-747
p2k2 M-1640
p2k21 M-1645
p2k2sat M-1630
p2k2sat1 M-1635
p2k2si M-1600
p2k2si1 M-1605
p2k2sisat M-1620
p2k2sisat1 M-1625
p2ksativ M-840
p2ksativr M-1525
p2kt1 M-1366
p2lii M-1213
p2lpe0 M-752
tdwse2 M-1739
tdwse3 M-1741
tdwsq1 M-1743
tdwsq2 M-1745
tdwsq3 M-1747
temp_sh OP-103
tempeff O-8
tempmod M-549
teta0 M-517
teta0r M-518
tfin I-4
tfin M-5
tfin_base M-628
tfin_top M-627
tfindrw M-545
tgaa I-43
tgaa M-634
tgate M-204
tgidl M-452
thetadibl M-551

© 2023 Cadence Design Systems, Inc.

bvsatcv M-122
capmod M-46
cdd OP-66
cddi OP-50
cde OP-68
cdei OP-52
cdg OP-65
cdgi OP-49
cds OP-67
cdsc M-76
cdscd M-77
cdscdn1 M-510
cdscdn2 M-511
cdscdr M-78
cdscdrn1 M-512
cdscdrn2 M-513
cdscn1 M-508
cdscn2 M-509
cdsi OP-51
cdsp I-19
cdsp M-19
lpoxedge M-1114
lprt M-1357
lprwg M-958
lprwgd M-966
lprwgs M-961
lpsat M-826
lpsatcv M-1463
lptwg M-856
lptwgr M-861
lptwgt M-1344
lpvag M-996
lqmfactor M-790
lqmtcencv M-798
lqmtcencva M-806
lqmtcencvo M-802
lqmtceniv M-795
lqsref M-1402
lrdsw M-943
lrdw M-953
lrsd I-22
lrsd M-22
p2mexp M-850
p2mexpr M-855
p2mfq1nom M-1719
p2mfq2nom M-1725
p2mfq3nom M-1731
p2mpower M-1401
p2ngate M-687
p2nigbacc M-1045
p2nigbinv M-1025
p2noia2 M-1396
p2ntgen M-1288
p2ntox M-1113
p2pclm M-919
p2pclmcv M-932
p2pclmg M-924
p2pclmr M-1555
p2pdibl1 M-980
p2pdibl1r M-985
p2pdibl2 M-990
p2pdibl2r M-1560
p2pgidl M-1143
thetamu M-149
thetasat M-130
thetasce M-550
thetasw M-552
tii M-451
tmask M-205
tmexp M-423
tmexpcv M-435
tmexpr M-530
tnjts M-468
tnjtsd M-469
tnjtssw M-470
tnjtsswd M-471
tnjtsswg M-472
tnjtsswgd M-473
tnoia M-401
tnoib M-402
tnoic M-586
tnoik M-590
tnoik2 M-588
tnoimod M-399

© 2023 Cadence Design Systems, Inc.

ced OP-74
cedi OP-58
cee OP-76
ceei OP-60
ceg OP-73
cegi OP-57
ces OP-75
cesi OP-59
cfd M-279
cfgeo O-7
cfs M-278
cgbl M-290
cgbn M-289
cgbo M-288
cgbov OP-79
cgd OP-63
cgdext OP-78
cgdi OP-47
cgdl M-285
cgdo M-283
lrsw M-948
lsii0 M-1214
lsii1 M-1219
lsii2 M-1224
lsiid M-1229
lsp M-201
lssp1 M-1675
lssp2 M-1681
lssp3 M-1687
lstthetasat M-1354
ltgidl M-1382
lthetasat M-866
ltii M-1377
ltss M-1367
lu0 M-869
lu0r M-1526
lua M-884
lua1 M-1324
lua1r M-1571
luar M-1531
p2pgisl M-1168
p2phibe M-762
p2phig M-673
p2phin M-727
p2pigcd M-1073
p2poxedge M-1118
p2prt M-1361
p2prwgd M-970
p2prwgs M-965
p2psat M-830
p2psatcv M-1467
p2ptwg M-860
p2ptwgr M-865
p2ptwgt M-1348
p2pvag M-1000
p2qmfactor M-794
p2qmtcencv M-805
p2qmtcencva M-810
p2qsref M-1406
p2rdsw M-947
tnom M-406
toxg M-477
toxp M-58
toxref M-250
tpb M-457
tpbsw M-458
tpbswg M-459
trddr M-188
trise I-28
trise M-1766
trsdr M-187
tsili M-194
tsre2 M-1738
tsre3 M-1740
tsrq1 M-1742
tsrq2 M-1744
tsrq3 M-1746
tss M-411
tsus I-44
tsus M-635

© 2023 Cadence Design Systems, Inc.

cgdp I-18
cgdp M-18
cge OP-64
cgei OP-48
cgeo1sw M-502
cgeoa M-215
cgeob M-216
cgeoc M-217
cgeod M-218
cgeoe M-219
cgeomod M-45
cgg OP-61
cggi OP-45
cgidl M-260
cgisl M-255
cgs OP-62
cgsext OP-77
cgsi OP-46
cgsl M-284
cgso M-282
cgsp I-17
luc M-889
luc1 M-1329
luc1r M-1576
lucr M-1536
lucs M-904
lucste M-1339
lud M-899
lud1 M-1334
lud1r M-1581
ludr M-1546
lup M-879
lupr M-1646
lute M-1309
luter M-1561
lutl M-1314
lutlr M-1566
lvasat M-925
lvsat M-811
lvsat1 M-816
lvsat1r M-821
lvsatcv M-841
p2rdw M-957
p2rsw M-952
p2sii0 M-1218
p2sii1 M-1223
p2sii2 M-1228
p2siid M-1233
p2ssp1 M-1679
p2ssp2 M-1685
p2ssp3 M-1691
p2tgidl M-1386
p2tii M-1381
p2tss M-1371
p2u0 M-873
p2u0r M-1530
p2ua M-888
p2ua1 M-1328
p2ua1r M-1575
p2uar M-1535
p2uc M-893
p2uc1 M-1333
p2uc1r M-1580
type M-27
u0 M-133
u0emsm1 M-664
u0emsm2 M-665
u0etawsc M-662
u0lt M-619
u0mult I-30
u0mult M-24
u0n1 M-531
u0n1r M-584
u0n2 M-532
u0n2r M-585
u0r M-561
ua M-137
ua1 M-415
ua1r M-580
uair M-654
uar M-564
uartsc M-652
uathin M-650
uatni M-653

© 2023 Cadence Design Systems, Inc.

cgsp M-17
chargewf M-533
cigbacc M-232
cigbinv M-227
cigc M-239
cigd M-249
cigs M-245
cins_ufcm M-625
cit M-75
citr M-555
cjd M-294
cjdt OP-81
cjs M-293
cjst OP-80
cjswd M-296
cjswgd M-298
cjswgs M-297
cjsws M-295
ckappab M-291
ckappad M-287
ckappas M-286
lvsatr M-1516
lwr M-971
lxl M-674
lxrcrg1 M-1299
lxrcrg2 M-1304
m I-1
mbe0 M-1763
mbewl M-1762
meff O-9
mexp M-123
mexpcv M-432
mexpr M-527
mfe2 M-1710
mfe3 M-1711
mfq1 M-1732
mfq1nom M-1714
mfq2 M-1733
mfq2nom M-1720
mfq3 M-1734
mfq3nom M-1726
mgidl M-604
p2ucr M-1540
p2ucs M-908
p2ucste M-1343
p2ud M-903
p2ud1 M-1338
p2ud1r M-1585
p2udr M-1550
p2up M-883
p2upr M-1650
p2ute M-1313
p2uter M-1565
p2utl M-1318
p2utlr M-1570
p2vsat M-815
p2vsat1 M-820
p2vsat1r M-825
p2vsatcv M-845
p2vsatr M-1520
p2wr M-975
p2xrcrg1 M-1303
p2xrcrg2 M-1308
uatsat M-651
uc M-140
uc1 M-416
uc1r M-581
ucr M-567
ucs M-147
ucste M-418
ud M-144
ud1 M-417
ud1r M-582
udptsc M-661
udr M-571
udthin M-659
udtsat M-660
up M-135
upr M-562
ute M-412
uter M-578
utl M-413
utlr M-579
vasat M-159

© 2023 Cadence Design Systems, Inc.

compatible M-535
coremod M-32
covd I-39
covd M-281
covmod M-607
covs I-38
covs M-280
cratio M-198
cs M-152
csd OP-70
csdesw M-292
csdi OP-54
cse OP-72
csei OP-56
csg OP-69
csgi OP-53
css OP-71
cssi OP-55
cth0 M-475
d I-3
mgisl M-603
minr M-534
mismatchdist M-1765
mismatchmod M-1764
mjd M-306
mjd2 M-318
mjs M-305
mjs2 M-317
mjswd M-308
mjswd2 M-320
mjswgd M-310
mjswgd2 M-322
mjswgs M-309
mjswgs2 M-321
mjsws M-307
mjsws2 M-319
mobmod M-34
mobscmod I-55
mobscmod M-646
mpower M-395
pa0cv M-1475
pa1 M-935
pa11 M-1430
pa2 M-940
pa21 M-1435
pagidl M-1121
pagisl M-1146
pagscv M-1478
paigbacc M-1028
paigbacc1 M-1445
paigbinv M-1003
paigbinv1 M-1440
paigc M-1048
paigc1 M-1053
paigd M-1096
paigd1 M-1450
paigen M-1291
paigs M-1076
paigs1 M-1081
palpha0 M-1171
vasatcv M-162
vbd_max M-1751
vbdr_max M-1758
vbs_max M-1752
vbsr_max M-1757
vdet OP-98
vds OP-10
vds_max M-1748
vdsat_c M-542
vdsat_vadj M-544
vdsat_vdl M-543
vdsatmod M-541
vdseff OP-17
vdssat OP-16
vdst OP-100
version M-1
ves OP-11
vest OP-101
vfb OP-14
vfbsd M-620

© 2023 Cadence Design Systems, Inc.

d M-4
dach1 I-48
dach1 M-639
dach2 I-50
dach2 M-641
dach3 I-52
dach3 M-643
deltaprsd M-199
deltavsat M-115
deltavsatcv M-498
deltaw M-62
deltawcv M-64
delvfb I-34
delvfbacc M-277
delvtrand I-29
delvtrand M-23
devmod M-598
devtype M-28
dim1h M-1651
mue M-148
mulbeta I-36
mulid0 I-32
mulmu0 I-35
mvt0 M-1761
mvtwl M-1759
mvtwl2 M-1760
na0cv M-1474
na1 M-934
na11 M-1429
na2 M-939
na21 M-1434
nagidl M-1120
nagisl M-1145
nagscv M-1477
naigbacc M-1027
naigbacc1 M-1444
naigbinv M-1002
naigbinv1 M-1439
palpha1 M-1176
palphaii M-1186
palphaii0 M-1455
palphaii1 M-1460
para_cdbox OP-86
para_cgbox OP-87
para_csbox OP-85
para_qds_fr OP-92
para_qgd_fr OP-91
para_qgd_ov OP-89
para_qgs_fr OP-90
para_qgs_ov OP-88
para_rd OP-83
para_rg OP-84
para_rs OP-82
pat M-1351
patcv M-1593
patr M-1588
pbd M-300
vfbsdcv M-621
vgb_max M-1753
vgbr_max M-1756
vgd OP-9
vgd_max M-1749
vgdr_max M-1754
vgdt OP-97
vget OP-99
vgs OP-8
vgs_max M-1750
vgsr_max M-1755
vgst OP-96
vgt OP-13
voffmod M-429
vsat M-108
vsat1 M-111
vsat1n1 M-523
vsat1n2 M-524
vsat1r M-112

© 2023 Cadence Design Systems, Inc.

dim2h M-1658
dim3h M-1665
dimension1 M-1652
dimension2 M-1659
dimension3 M-1666
dlbin M-55
dlc M-53
dlcacc M-54
dlcigd M-246
dlcigs M-242
dlthx M-548
dmobclamp M-425
drout M-223
dssp1 M-1692
dssp2 M-1693
dssp3 M-1694
dsub M-84
dtemp I-27
dvsatclamp M-424
dvt0 M-79
naigc M-1047
naigc1 M-1052
naigd M-1095
naigd1 M-1449
naigen M-1290
naigs M-1075
naigs1 M-1080
nalpha0 M-1170
nalpha1 M-1175
nalphaii M-1185
nalphaii0 M-1454
nalphaii1 M-1459
nat M-1350
natcv M-1592
natr M-1587
nbeta0 M-1180
nbetaii0 M-1190
nbetaii1 M-1195
nbetaii2 M-1200
nbgidl M-1125
pbeta0 M-1181
pbetaii0 M-1191
pbetaii1 M-1196
pbetaii2 M-1201
pbgidl M-1126
pbgisl M-1151
pbigbacc M-1033
pbigbinv M-1008
pbigc M-1058
pbigd M-1101
pbigen M-1296
pbigs M-1086
pbs M-299
pbswd M-302
pbswgd M-304
pbswgs M-303
pbsws M-301
pcdsc M-695
pcdscd M-700
pcdscdr M-705
vsat1rn1 M-525
vsat1rn2 M-526
vsatcv M-120
vsatn1 M-521
vsatn2 M-522
vsatr M-557
vsatrn1 M-558
vsatrn2 M-559
vth OP-12
vthmod M-536
vtsd M-353
vtss M-352
vtsswd M-355
vtsswgd M-357
vtsswgs M-356
vtssws M-354
w_ufcm M-626
wa1 M-936
wa11 M-1431
wa2 M-941

© 2023 Cadence Design Systems, Inc.

dvt1 M-80
dvt1ss M-514
dvtb M-94
dvtp0 M-519
dvtp1 M-520
dvtp2 M-597
dvtshift M-87
dvtshiftr M-556
dws1 I-47
dws1 M-638
dws2 I-49
dws2 M-640
dws3 I-51
dws3 M-642
e2nom M-1698
e3nom M-1704
easub M-70
ef M-365
efds M-389
efrd M-388
efrs M-387
nbgisl M-1150
nbigbacc M-1032
nbigbinv M-1007
nbigc M-1057
nbigd M-1100
nbigen M-1295
nbigs M-1085
nbody M-65
nbodyn1 M-503
nbodyn2 M-504
nc0sub M-73
ncdsc M-694
ncdscd M-699
ncdscdr M-704
ncfd M-1240
ncfs M-1235
ncgbl M-1275
ncgdl M-1260
ncgidl M-1135
ncgisl M-1160
ncgsl M-1255
pcfd M-1241
pcfs M-1236
pcgbl M-1276
pcgdl M-1261
pcgidl M-1136
pcgisl M-1161
pcgsl M-1256
pcigbacc M-1038
pcigbinv M-1013
pcigc M-1063
pcigd M-1106
pcigs M-1091
pcit M-690
pcitr M-1508
pckappab M-1281
pckappad M-1271
pckappas M-1266
pclm M-155
pclmcv M-160
pclmg M-158
pclmgcv M-161
wa21 M-1436
wagidl M-1122
wagisl M-1147
waigbacc M-1029
waigbacc1 M-1446
waigbinv M-1004
waigbinv1 M-1441
waigc M-1049
waigc1 M-1054
waigd M-1097
waigd1 M-1451
waigen M-1292
waigs M-1077
waigs1 M-1082
walpha0 M-1172
walpha1 M-1177
walphaii M-1187
walphaii0 M-1456
walphaii1 M-1461
wat M-1352
watcv M-1594

© 2023 Cadence Design Systems, Inc.

egbulk M-663
egidl M-261
egisl M-256
eigbinv M-228
em M-366
emobt M-414
eot M-57
eotacc M-276
eotbox M-59
epsrox M-68
epsrsp M-203
epsrsub M-69
esatii M-270
eta0 M-82
eta0lt M-592
eta0n1 M-515
eta0n2 M-516
eta0r M-83
etamob M-134
ncigbacc M-1037
ncigbinv M-1012
ncigc M-1062
ncigd M-1105
ncigs M-1090
ncit M-689
ncitr M-1507
nckappab M-1280
nckappad M-1270
nckappas M-1265
ncovd M-1250
ncovs M-1245
ncs M-913
ndeltavsat M-832
ndeltavsatcv M-1469
ndimension1 M-1654
ndimension2 M-1661
ndimension3 M-1668
ndlbin M-681
pclmr M-574
pcovd M-1251
pcovs M-1246
pcs M-914
pdej I-16
pdej M-16
pdeltavsat M-833
pdeltavsatcv M-1470
pdeo I-12
pdeo M-12
pdibl1 M-220
pdibl1r M-221
pdibl2 M-222
pdibl2r M-577
pdimension1 M-1655
pdimension2 M-1662
pdimension3 M-1669
pdlbin M-682
pdrout M-993
watr M-1589
wbeta0 M-1182
wbetaii0 M-1192
wbetaii1 M-1197
wbetaii2 M-1202
wbgidl M-1127
wbgisl M-1152
wbigbacc M-1034
wbigbinv M-1009
wbigc M-1059
wbigd M-1102
wbigen M-1297
wbigs M-1087
wcdsc M-696
wcdscd M-701
wcdscdr M-706
wcfd M-1242
wcfs M-1237
wcgbl M-1277

© 2023 Cadence Design Systems, Inc.

etamobir M-649
etamobthin M-647
etamobtni M-648
etaqm M-102
eu M-141
euir M-658
euptsc M-656
eur M-568
euthin M-655
eutni M-657
fech M-61
fechcv M-63
fnmod M-49
fnoik M-380
fnoimod M-400
fpitch I-5
fpitch M-6
gds OP-5
geomod M-33
ndrout M-992
ndsub M-739
ndvt0 M-709
ndvt1 M-714
ndvt1ss M-719
ndvtb M-785
ndvtp0 M-439
ndvtp1 M-444
ndvtshift M-754
ndvtshiftr M-1512
ne2nom M-1700
ne3nom M-1706
negidl M-1130
negisl M-1155
neigbinv M-1017
nemobt M-1320
nesatii M-1205
neta0 M-729
neta0r M-734
pdsub M-740
pdvt0 M-710
pdvt1 M-715
pdvt1ss M-720
pdvtb M-786
pdvtp0 M-440
pdvtp1 M-445
pdvtshift M-755
pdvtshiftr M-1513
pe2nom M-1701
pe3nom M-1707
pegidl M-1131
pegisl M-1156
peigbinv M-1018
pemobt M-1321
pesatii M-1206
peta0 M-730
peta0r M-735
petamob M-876
wcgdl M-1262
wcgidl M-1137
wcgisl M-1162
wcgsl M-1257
wcigbacc M-1039
wcigbinv M-1014
wcigc M-1064
wcigd M-1107
wcigs M-1092
wcit M-691
wcitr M-1509
wckappab M-1282
wckappad M-1272
wckappas M-1267
wcovd M-1252
wcovs M-1247
wdeltavsat M-834
wdeltavsatcv M-1471
wdim0 M-1672

© 2023 Cadence Design Systems, Inc.

gidlfactor M-600
gidlmod M-39
gislfactor M-599
gm OP-4
gmbs OP-6
hepi M-193
hfin M-60
hpff I-45
hpff M-636
id OP-2
ideff OP-19
ids OP-3
ids0mult I-31
ids0mult M-25
idsgen OP-23
igb0mult I-41
igb0mult M-31
igbacc OP-35
netamob M-875
neu M-895
neur M-1542
nf I-6
nfin I-7
nfin M-7
nfinmax M-1772
nfinmin M-1771
nfinnom I-23
ngaa I-53
ngaa M-644
ngate M-74
ngcon I-8
ngcon M-8
ngidlfactor M-1504
ngislfactor M-1501
ni0sub M-71
nidsmin M-405
peu M-896
peur M-1543
pgidl M-262
pgidlfactor M-1505
pgisl M-257
pgislfactor M-1502
phibe M-90
phig M-67
phigl M-505
phiglt M-591
phign1 M-506
phign2 M-507
phin M-81
pigcd M-241
pigt M-1389
piit M-1374
pk0 M-765
pk01 M-1409
wdimension1 M-1656
wdimension2 M-1663
wdimension3 M-1670
wdimr M-1673
wdrout M-994
wdsub M-741
wdvt0 M-711
wdvt1 M-716
wdvt1ss M-721
wdvtp0 M-441
wdvtp1 M-446
wdvtshift M-756
wdvtshiftr M-1514
we2nom M-1702
we3nom M-1708
weff O-1
weffcv O-3
wegidl M-1132

© 2023 Cadence Design Systems, Inc.

igbaccclamp M-235
igbd OP-34
igbinv OP-36
igbinvclamp M-234
igbmod M-38
igbratio M-606
igbs OP-33
igc0mult I-40
igc0mult M-30
igcd OP-32
igcinvclamp M-236
igclamp M-48
igcmod M-37
igcs OP-31
igd OP-30
igidl OP-25
igisl OP-26
igs OP-29
igt M-453
igtot OP-21
nigbacc M-233
nigbinv M-229
nigc M-240
nigt M-1388
niit M-1373
njd M-330
njs M-329
njts M-346
njtsd M-347
njtssw M-348
njtsswd M-349
njtsswg M-350
njtsswgd M-351
nk0 M-764
nk01 M-1408
nk0si M-769
nk0si1 M-1413
nk0sisat M-1607
nk0sisat1 M-1612
nk1 M-774
pk0si M-770
pk0si1 M-1414
pk0sisat M-1608
pk0sisat1 M-1613
pk1 M-775
pk11 M-1422
pk1rsce M-745
pk1sat M-783
pk1sat1 M-1427
pk1si M-780
pk1si1 M-1419
pk1sisat M-1484
pk1sisat1 M-1487
pk2 M-1638
pk21 M-1643
pk2sat M-1628
pk2sat1 M-1633
pk2si M-1598
pk2si1 M-1603
pk2sisat M-1618
wegisl M-1157
weigbinv M-1019
wemobt M-1322
wesatii M-1207
weta0 M-731
weta0r M-736
wetamob M-877
weu M-897
weur M-1544
wgaa I-46
wgaa M-637
wgaanom M-1697
wigt M-1390
wiit M-1375
wk0 M-766
wk01 M-1410
wk0si M-771
wk0si1 M-1415
wk0sisat M-1609
wk0sisat1 M-1614

© 2023 Cadence Design Systems, Inc.

iii OP-24
iimod M-40
iimod2clamp1 M-631
iimod2clamp2 M-632
iimod2clamp3 M-633
iiratio M-605
iit M-450
ijdb OP-28
ijsb OP-27
ijthdfwd M-332
ijthdrev M-334
ijthsfwd M-331
ijthsrev M-333
im M-547
imin M-497
iseff OP-20
isnoisy I-37
isub OP-22
ith OP-93
ithx M-546
nk11 M-1421
nk1rsce M-744
nk1sat M-782
nk1sat1 M-1426
nk1si M-779
nk1si1 M-1418
nk1sisat M-1483
nk1sisat1 M-1486
nk2 M-1637
nk21 M-1642
nk2sat M-1627
nk2sat1 M-1632
nk2si M-1597
nk2si1 M-1602
nk2sisat M-1617
nk2sisat1 M-1622
nkgidl M-1492
nkgisl M-1489
nksativ M-837
nksativr M-1522
pk2sisat1 M-1623
pkgidl M-1493
pkgisl M-1490
pksativ M-838
pksativr M-1523
pkt1 M-1364
plii M-1211
plint M-679
plpe0 M-750
plpeb M-789
pmexp M-848
pmexpcv M-1481
pmexpr M-853
pmfq1nom M-1717
pmfq2nom M-1723
pmfq3nom M-1729
pmgidl M-1499
pmgisl M-1496
pmpower M-1399
pmue M-911
wk1 M-776
wk11 M-1423
wk1rsce M-746
wk2 M-1639
wk21 M-1644
wk2sat M-1629
wk2sat1 M-1634
wk2si M-1599
wk2si1 M-1604
wk2sisat M-1619
wk2sisat1 M-1624
wksativ M-839
wksativr M-1524
wkt1 M-1365
wlii M-1212
wlpe0 M-751
wmax M-1770
wmexp M-849
wmexpr M-854
wmfq1nom M-1718

© 2023 Cadence Design Systems, Inc.

ivth M-537
ivth_vdsmin M-540
ivthl M-539
ivthw M-538
jsd M-324
jss M-323
jswd M-326
jswgd M-328
jswgs M-327
jsws M-325
jtsd M-340
jtss M-339
jtsswd M-342
jtsswgd M-344
jtsswgs M-343
jtssws M-341
jtweff M-345
k0 M-88
k01 M-478
k0si M-89
nkt1 M-1363
nlii M-1210
nlint M-678
nlpe0 M-749
nlpeb M-788
nmexp M-847
nmexpcv M-1480
nmexpr M-852
nmfq1nom M-1716
nmfq2nom M-1722
nmfq3nom M-1728
nmgidl M-1498
nmgisl M-1495
nmpower M-1398
nmue M-910
nnbody M-667
nngate M-684
nnigbacc M-1042
nnigbinv M-1022
nnigc M-1067
pnbody M-668
pngate M-685
pnigbacc M-1043
pnigbinv M-1023
pnigc M-1068
pnoia2 M-1394
pntgen M-1286
pntox M-1111
poxedge M-252
ppclm M-917
ppclmcv M-930
ppclmg M-922
ppclmr M-1553
ppdibl1 M-978
ppdibl1r M-983
ppdibl2 M-988
ppdibl2r M-1558
ppgidl M-1141
ppgisl M-1166
pphibe M-760
wmfq2nom M-1724
wmfq3nom M-1730
wmin M-1769
wmpower M-1400
wngate M-686
wnigbacc M-1044
wnigbinv M-1024
wnoia2 M-1395
wntgen M-1287
wntox M-1112
wpclm M-918
wpclmcv M-931
wpclmg M-923
wpclmr M-1554
wpdibl1 M-979
wpdibl1r M-984
wpdibl2 M-989
wpdibl2r M-1559
wpgidl M-1142
wpgisl M-1167

© 2023 Cadence Design Systems, Inc.

k0si1 M-479
k0sisat M-611
k0sisat1 M-612
k1 M-91
k11 M-481
k1rsce M-85
k1sat M-93
k1sat1 M-482
k1si M-92
k1si1 M-480
k1sisat M-436
k1sisat1 M-437
k2 M-617
k21 M-618
k2sat M-615
k2sat1 M-616
k2si M-609
k2si1 M-610
k2sisat M-613
k2sisat1 M-614
kf_hv M-391
nnoia2 M-1393
nntgen M-1285
nntox M-1110
noia M-367
noia2 M-393
noib M-368
noic M-369
noiua M-396
npclm M-916
npclmcv M-929
npclmg M-921
npclmr M-1552
npdibl1 M-977
npdibl1r M-982
npdibl2 M-987
npdibl2r M-1557
npgidl M-1140
npgisl M-1165
nphibe M-759
nphig M-670
nphin M-724
pphig M-671
pphin M-725
ppigcd M-1071
ppoxedge M-1116
pprt M-1359
pprwg M-960
pprwgd M-968
pprwgs M-963
ppsat M-828
ppsatcv M-1465
pptwg M-858
pptwgr M-863
pptwgt M-1346
ppvag M-998
pqm M-104
pqmacc M-106
pqmfactor M-792
pqmtcencv M-800
pqmtcencva M-808
pqmtcencvo M-804
pqmtceniv M-797
wphibe M-761
wphig M-672
wphin M-726
wpigcd M-1072
wpoxedge M-1117
wprt M-1360
wprwgd M-969
wprwgs M-964
wpsat M-829
wpsatcv M-1466
wptwg M-859
wptwgr M-864
wptwgt M-1347
wpvag M-999
wqmfactor M-793
wqmtcencv M-801
wqmtcencva M-809
wqsref M-1405
wr M-186
wrdsw M-946
wrdw M-956

© 2023 Cadence Design Systems, Inc.

kfds M-383
kfrd M-382
kfrs M-381
kgidl M-602
kgisl M-601
ksativ M-119
ksativr M-560
kt1 M-409
kt1l M-410
l I-2
l M-3
la0cv M-1473
la1 M-933
la11 M-1428
la2 M-938
la21 M-1433
lagidl M-1119
lagisl M-1144
lagscv M-1476
laigbacc M-1026
laigbacc1 M-1443
npigcd M-1070
npoxedge M-1115
nprt M-1358
nprwg M-959
nprwgd M-967
nprwgs M-962
npsat M-827
npsatcv M-1464
nptwg M-857
nptwgr M-862
nptwgt M-1345
npvag M-997
nqmfactor M-791
nqmtcencv M-799
nqmtcencva M-807
nqmtcencvo M-803
nqmtceniv M-796
nqsmod M-41
nqsref M-1403
nrd I-21
nrd M-21
pqsref M-1404
prddr M-183
prdsw M-945
prdw M-955
prsdend M-208
prsdr M-182
prsw M-950
prt M-449
prwg M-177
prwgd M-185
prwgs M-184
psat M-116
psatcv M-499
psej I-15
psej M-15
pseo I-11
pseo M-11
psii0 M-1216
psii1 M-1221
psii2 M-1226
psiid M-1231
wrsw M-951
wsfe2 M-1712
wsfe3 M-1713
wsfq1 M-1735
wsfq2 M-1736
wsfq3 M-1737
wsii0 M-1217
wsii1 M-1222
wsii2 M-1227
wsiid M-1232
wssp0 M-1695
wssp1 M-1678
wssp2 M-1684
wssp3 M-1690
wsspr M-1696
wtgidl M-1385
wth0 M-476
wtii M-1380
wtss M-1370
wu0 M-872
wu0r M-1529

© 2023 Cadence Design Systems, Inc.

laigbinv M-1001
laigbinv1 M-1438
laigc M-1046
laigc1 M-1051
laigd M-1094
laigd1 M-1448
laigen M-1289
laigs M-1074
laigs1 M-1079
lalpha0 M-1169
lalpha1 M-1174
lalphaii M-1184
lalphaii0 M-1453
lalphaii1 M-1458
lat M-1349
latcv M-1591
latr M-1586
lbeta0 M-1179
lbetaii0 M-1189
lbetaii1 M-1194
nrdsw M-944
nrdw M-954
nrs I-20
nrs M-20
nrsw M-949
nsd M-66
nsde M-209
nseg M-364
nsii0 M-1215
nsii1 M-1220
nsii2 M-1225
nsiid M-1230
nssp1 M-1676
nssp2 M-1682
nssp3 M-1688
nstthetasat M-1355
ntgen M-359
ntgidl M-1383
nthetasat M-867
ntii M-1378
pssp1 M-1677
pssp2 M-1683
pssp3 M-1689
pstthetasat M-1356
ptgidl M-1384
pthetasat M-868
ptii M-1379
ptss M-1369
ptwg M-126
ptwgr M-127
ptwgt M-426
pu0 M-871
pu0r M-1528
pua M-886
pua1 M-1326
pua1r M-1573
puar M-1533
puc M-891
puc1 M-1331
puc1r M-1578
wua M-887
wua1 M-1327
wua1r M-1574
wuar M-1534
wuc M-892
wuc1 M-1332
wuc1r M-1579
wucr M-1539
wucs M-907
wucste M-1342
wud M-902
wud1 M-1337
wud1r M-1584
wudr M-1549
wup M-882
wupr M-1649
wute M-1312
wuter M-1564
wutl M-1317
wutlr M-1569

© 2023 Cadence Design Systems, Inc.

lbetaii2 M-1199
lbgidl M-1124
lbgisl M-1149
lbigbacc M-1031
lbigbinv M-1006
lbigc M-1056
lbigd M-1099
lbigen M-1294
lbigs M-1084
lcdsc M-693
lcdscd M-698
lcdscdr M-703
lcfd M-1239
lcfs M-1234
lcgbl M-1274
lcgdl M-1259
lcgidl M-1134
lcgisl M-1159
lcgsl M-1254
lcigbacc M-1036
lcigbinv M-1011
ntnoi M-398
ntox M-251
ntss M-1368
nu0 M-870
nu0r M-1527
nua M-885
nua1 M-1325
nua1r M-1572
nuar M-1532
nuc M-890
nuc1 M-1330
nuc1r M-1577
nucr M-1537
nucs M-905
nucste M-1340
nud M-900
nud1 M-1335
nud1r M-1582
nudr M-1547
nup M-880
nupr M-1647
pucr M-1538
pucs M-906
pucste M-1341
pud M-901
pud1 M-1336
pud1r M-1583
pudr M-1548
pup M-881
pupr M-1648
pute M-1311
puter M-1563
putl M-1316
putlr M-1568
pvag M-224
pvasat M-927
pvsat M-813
pvsat1 M-818
pvsat1r M-823
pvsatcv M-843
pvsatr M-1518
pwr M-973
wvsat M-814
wvsat1 M-819
wvsat1r M-824
wvsatcv M-844
wvsatr M-1519
wwr M-974
wxrcrg1 M-1302
wxrcrg2 M-1307
xjbvd M-338
xjbvs M-337
xl I-26
xl M-26
xrcrg1 M-362
xrcrg2 M-363
xtid M-461
xtis M-460
xtsd M-463
xtss M-462
xtsswd M-465
xtsswgd M-467
xtsswgs M-466

© 2023 Cadence Design Systems, Inc.

lcigc M-1061 nute M-1310 pwr OP-18 xtssws M-464

lcigd M-1104 nuter M-1562 pxl M-676

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

46

BSIMSOI_S Model

Bsimsoi_s model (symmetric BSIM-SOI) is an international standard model for SOI (Silicon-On-Insulator) circuit design. This model offers two different mode of operations: SOIMOD=1 is dedicated to the dynamic depletion devices, and it has surface potential based core IV and CV formulation; SOIMOD=0 is developed for only partial depletion devices, and it is formulated on top of the BSIM-BULK framework.

This device is supported within altergroups.

Synopsis

```
Name ( d g s e [b] [t] ) ModelName <parameter=value> ...
```

Instance Parameters

m	1.0	Number of devices in parallel.
l	1.0e-5 m	Length.
w	1.0e-5 m	Total width including fingers.
nf	1	Number of fingers.
nrs	1.0	Number of squares in source.
nrd	1.0	Number of squares in drain.
vfbsdoff	0.0 V	Flatband voltage offset parameter.
minz	0	Minimize either drain or source.
rgatemod	0	Gate resistance model selector.

© 2023 Cadence Design Systems, Inc.

geomod	0	Geometry-dependent parasitics model.
rgeomod	0	Geometry-dependent source/drain resistance, 0: RSH-based, 1: Holistic.
sa	0.0 m	Distance between OD edge from poly from one side.
sb	0.0 m	Distance between OD edge from poly from other side.
sd	0.0 m	Distance between neighboring fingers.
sca	0.0	Integral of the first distribution function for scattered well dopants.
scb	0.0	Integral of second distribution function for scattered well dopants.
scc	0.0	Integral of third distribution function for scattered well dopants.
sc	0.0 m	Distance to a single well edge; if <= 0.0, turn off WPE.
as	0.0 m^2	Source-to-substrate junction area.
ad	0.0 m^2	Drain-to-substrate junction area.
ps	0.0 m	Source-to-substrate junction perimeter.
pd	0.0 m	Drain-to-substrate junction perimeter.
tnodeout	0	If it appears on instance parameter list and the device has 5 terminals, then 5th terminal is t-node, otherwise, 5th terminal is bulk node.
xgw	0.0 m	Distance from gate contact center to device edge.
ngcon	1	Number of gate contacts.

© 2023 Cadence Design Systems, Inc.

dtemp	0.0 K	Offset of device temperature.
trise	0.0 K	Offset of device temperature.
mulu0	1.0 m^2/(V s)	Multiplication factor for low field mobility.
delvto	0.0 V	Zero bias threshold voltage variation.
ids0mult	1.0	Variability in drain current for miscellaneous reasons.
edgefet	0	0: Edge FET Model OFF, 1: Edge FET Model ON.
sslmod	0	Sub-surface leakage drain current, 0: Turn off 1: Turn on.
bjtoff	0.0	BJT on/off flag.
frbody	1.0	layout dependent body-resistance coefficient.
nrb	1.0	Number of squares in body.
nseg	1	Number segments for width partitioning.
nbc	0.0	Number of body contact isolation edge 1 = TBODY, 2 = HBODY.
pdbcp	0.0 m	Perimeter length for bc parasitics at drain side.
psbcp	0.0 m	Perimeter length for bc parasitics at source side.
agbcp	0.0 m^2	Gate to body overlap area for bc parasitics.
agbcp2	2e-12 m^2	Parasitic Gate to body overlap area for bc parasitics /* v4.1 improvement on BC .
agbcpd	0.0 m^2	Gate to body overlap area for bc parasitics in DC.

© 2023 Cadence Design Systems, Inc.

aebcp	0.0 m^2	Substrate to body overlap area for bc parasitics.

Model Synopsis

```
model ModelName bsimsoi_s <parameter=value> ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

xgw	0.0 m	Distance from gate contact center to device edge.
ngcon	1	Number of gate contacts.
dtemp	0.0 K	Offset of device temperature.
mulu0	1.0 m^2/(V s)	Multiplication factor for low field mobility.
delvto	0.0 V	Zero bias threshold voltage variation.
ids0mult	1.0	Variability in drain current for miscellaneous reasons.
edgefet	0	0: Edge FET Model OFF, 1: Edge FET Model ON.
sslmod	0	Sub-surface leakage drain current, 0: Turn off 1: Turn on.
soimod	0	0: PDSOI mode, 1: DDSOI mode.
type	n	N-type = n, P-type = p.Possible values are p and n.
cvmod	0	0: Consistent I-V/C-V, 1: Different I-V/C-V.
covmod	0	0: Use bias-independent overlap capacitances, 1: Use bias-dependent overlap capacitances.
rdsmod	0	0: Internal bias dependent and external bias independent S/D resistance model, 1: External S/D resistance model, 2: Internal S/D resistance model.
wpemod	0	Model flag.
asymmod	0	0: Asymmetry model turned off - forward mode parameters used, 1: Asymmetry model turned on.
gidlmod	0	0: Turn off GIDL current, 1: Turn on GIDL current.

© 2023 Cadence Design Systems, Inc.

igcmod	0	0: Turn off Igc, Igs and Igd, 1: Turn on Igc, Igs and Igd.
igbmod	0	0: Turn off Igb, 1: Turn on Igb.
tnoimod	0	Thermal noise model selector.
shmod	0	0: Self heating model OFF, 1: Self heating model ON.
mobscale	0	Mobility scaling model, 0: Old Model, 1: New Model.
bodymod	0	Flag for body contact mode 0: Floating body, 1: linear 2: non-linear (bias-dependent RB) .
iiimod	0	Flag for III selector.
modagbcp2	0	0: AGBCP2 OFF, 1: AGBCP2 ON.
pdemod	0	0: PDE OFF, 1: PDE ON - for DD model.
fbody1	0	0: Extrinsic S/D substrate charge ON, 1: PExtrinsic S/D substrate charge OFF.
llong	1.0e-5 m	L of extracted long channel device.
lmlt	1.0	Length shrinking parameter.
wmlt	1.0	Width shrinking parameter.
xl	0.0 m	L offset for channel length due to mask/etch effect.
wwide	1.0e-5 m	W of extracted wide channel device.
xw	0.0 m	W offset for channel width due to mask/etch effect.
lint	0.0 m	Delta L for I-V.

© 2023 Cadence Design Systems, Inc.

ll	0.0 m^(1+LLN)	Length reduction parameter.
lw	0.0 m^(1+LWN)	Length reduction parameter.
lwl	0.0 m^(1+LLN +LWN)	Length reduction parameter.
lln	1.0	Length reduction parameter.
lwn	1.0	Length reduction parameter.
wint	0.0 m	Delta W for I-V.
wl	0.0 m^(1+WLN)	Width reduction parameter.
ww	0.0 m^(1+WWN)	Width reduction parameter.
wwl	0.0 m^(1+WWN +WLN)	Width reduction parameter.
wln	1.0	Width reduction parameter.
wwn	1.0	Width reduction parameter.
dlc	0.0 m	Delta L for C-V.
llc	0.0 m^(1+LLN)	Length reduction parameter.

© 2023 Cadence Design Systems, Inc.

lwc	0.0 m^(1+LWN)	Length reduction parameter.
lwlc	0.0 m^(1+LWN+LLN)	Length reduction parameter.
dwc	0.0 m	Delta W for C-V.
wlc	0.0 m^(1+WLN)	Width reduction parameter.
wwc	0.0 m^(1+WWN)	Width reduction parameter.
wwlc	0.0 m^(1+WWN+WLN)	Width reduction parameter.
tsi	40e-9 m	Silicon-on-insulator thickness.
tbox	200e-9 m	Back gate oxide thickness in meters.
toxe	3.0e-9 m	Effective gate dielectric thickness relative to SiO2.
toxp	3.0e-9 m	Physical gate dielectric thickness. If not given, TOXP is calculated from TOXE and DTOX.
dtox	0.0 m	Difference between effective dielectric thickness.
ndep	1e24 1/m^3	Channel doping concentration for I-V.
ndepl1	0.0 m	Length dependence coefficient of NDEP.
ndeplexp1	1.0	Length dependence exponent coefficient of NDEP.

© 2023 Cadence Design Systems, Inc.

ndepl2	0.0 m	Length dependence of NDEP - For Short Channel Devices.
ndeplexp2	2.0	Length dependence exponent coefficient of NDEP.
ndepw	0.0 m	Width dependence coefficient of NDEP.
ndepwexp	1.0	Width dependence exponent coefficient of NDEP.
ndepwl	0.0 m^2	Width-length dependence coefficient of NDEP.
ndepwlexp	1.0	Width-length dependence exponent coefficient of NDEP.
lndep	0.0 $1/m^2$	Length dependence of NDEP.
wndep	0.0 $1/m^2$	Width dependence of NDEP.
pndep	0.0 1/m	Area dependence of NDEP .
ndepcv	1e24 $1/m^3$	Channel doping concentration for C-V.
ndepcvl1	0.0 m	Length dependence coefficient of NDEPCV.
ndepcvlexp1	1.0	Length dependence exponent coefficient of NDEPCV.
ndepcvl2	0.0 m	Length dependence coefficient of NDEPCV - For Short Channel Devices.
ndepcvlexp2	2.0	Length dependence exponent coefficient of NDEPCV.
ndepcvw	0.0 m	Width dependence coefficient of NDEPCV.
ndepcvwexp	1.0	Width dependence exponent coefficient of NDEPCV.

© 2023 Cadence Design Systems, Inc.

ndepcvwl	0.0 m^2	Width-length dependence coefficient of NDEPCV.
ndepcvwlexp	1.0	Width-length dependence exponent coefficient of NDEPCV.
lndepcv	0.0 $1/m^2$	Length dependence of NDEP for C-V.
wndepcv	0.0 $1/m^2$	Width dependence of NDEP for C-V.
pndepcv	0.0 1/m	Area dependence of NDEP for C-V.
ngate	5e25 $1/m^3$	Gate doping concentration.
lngate	0.0 $1/m^2$	Length dependence of NGATE.
wngate	0.0 $1/m^2$	Width dependence of NGATE.
pngate	0.0 1/m	Area dependence of NGATE.
ni0sub	1.1e16 $1/m^3$	Intrinsic carrier concentration of the substrate at 300.15K.
bg0sub	1.17 eV	Bandgap of substrate at 300.15K.
epsrsub	11.9	Relative dielectric constant of the channel material.
epsrox	3.9	Relative dielectric constant of the gate dielectric.
xj	1.5e-7 m	S/D junction depth.
lxj	0.0 m^2	Length dependence of XJ.
wxj	0.0 m^2	Width dependence of XJ.
pxj	0.0 m^3	Area dependence of XJ.
vfb	(-0.5) V	Flatband voltage.

© 2023 Cadence Design Systems, Inc.

lvfb	0.0 V m	Length dependence of VFB.
wvfb	0.0 V m	Width dependence of VFB.
pvfb	0.0 V m^2	Area dependence of VFB.
vfbb	0.0 V	Flatband voltage.
lvfbb	0.0 V m	Length dependence of VFBB.
wvfbb	0.0 V m	Width dependence of VFBB.
pvfbb	0.0 V m^2	Area dependence of VFBB.
vfbl	0.0 m	Length dependence coefficient of VFBCV.
vfblexp	1.0	Length dependence exponent coefficient of VFBCV.
vfbw	0.0 m	Width dependence coefficient of VFBCV.
vfbwexp	1.0	Width dependence exponent coefficient of VFBCV.
vfbwl	0.0 m^2	Width-length dependence coefficient of VFBCV.
vfbwlexp	1.0	Width-length dependence coefficient of VFBCV.
vfbcv	(-0.5) V	Flatband voltage for C-V.
lvfbcv	0.0 V m	Length dependence of VFBCV.
wvfbcv	0.0 V m	Width dependence of VFBCV.
pvfbcv	0.0 V m^2	Area dependence of VFBCV.
vfbcvl	0.0 m	Length dependence coefficient of VFBCV.
vfbcvlexp	1.0	Length dependence exponent coefficient of VFBCV.

© 2023 Cadence Design Systems, Inc.

vfbcvw	0.0 m	Width dependence coefficient of VFBCV.
vfbcvwexp	1.0	Width dependence exponent coefficient of VFBCV.
vfbcvwl	0.0 m^2	Width-length dependence coefficient of VFBCV.
vfbcvwlexp	1.0	Width-length dependence coefficient of VFBCV.
delvfbacc	0.0	VFB shift in the accumulation region, valid for CVMOD = 1 only.
vfbagbcp2	(-0.5) V	Flatband voltage for AGBCP2 C-V.
ndepagbcp2	1e24 1/m^3	Channel doping concentration for AGBCP2.
nsd	1e26 1/m^3	S/D doping concentration.
lnsd	0.0 1/m^2	Length dependence of NSD.
wnsd	0.0 1/m^2	Width dependence of NSD.
pnsd	0.0 1/m	Area dependence of NSD.
dvtp0	0.0 m	DITS.
ldvtp0	0.0 m^2	Length dependence of DVTP0.
wdvtp0	0.0 m^2	Width dependence of DVTP0.
pdvtp0	0.0 m^3	Area dependence of DVTP0.
dvtp1	0.0 1/V	DITS.
ldvtp1	0.0 m/V	Length dependence of DVTP1.
wdvtp1	0.0 m/V	Width dependence of DVTP1.

© 2023 Cadence Design Systems, Inc.

pdvtp1	0.0 m^2/V	Area dependence of DVTP1.
dvtp2	0.0 m V	DITS.
ldvtp2	0.0 m^2/V	Length dependence of DVTP2.
wdvtp2	0.0 m^2/V	Width dependence of DVTP2.
pdvtp2	0.0 m^3/V	Area dependence of DVTP2.
dvtp3	0.0	DITS.
ldvtp3	0.0 m	Length dependence of DVTP3.
wdvtp3	0.0 m	Width dependence of DVTP3.
pdvtp3	0.0 m^2	Area dependence of DVTP3.
dvtp4	0.0 1/V	DITS.
ldvtp4	0.0 m/V	Length dependence of DVTP4.
wdvtp4	0.0 m/V	Width dependence of DVTP4.
pdvtp4	0.0 m^2/V	Area dependence of DVTP4.
dvtp5	0.0 V	DITS.
ldvtp5	0.0 m V	Length dependence of DVTP5.
wdvtp5	0.0 m V	Width dependence of DVTP5.
pdvtp5	0.0 m^2 V	Area dependence of DVTP5.
dvbd0	0.0	coupling from Vd to Vbs for improved dVbi model.
ldvbd0	0.0	Length dependence of DVBD0.

© 2023 Cadence Design Systems, Inc.

wdvbd0	0.0	Width dependence of DVBD0.
pdvbd0	0.0	Area dependence of DVBD0.
dvbd1	0.0	coupling from Vd to Vbs for improved dVbi model.
ldvbd1	0.0	Length dependence of DVBD1.
wdvbd1	0.0	Width dependence of DVBD1.
pdvbd1	0.0	Area dependence of DVBD1.
vsce	0.0	coupling from Vd to Vbs for improved dVbi model.
lvsce	0.0	Length dependence of DVBD1.
wvsce	0.0	Width dependence of DVBD1.
pvsce	0.0	Area dependence of DVBD1.
cdsbs1	1.0	coupling from Vd to Vbs for improved dVbi model.
lcdsbs1	0.0	Length dependence of CDSBS.
wcdsbs1	0.0	Width dependence of CDSBS.
pcdsbs1	0.0	Area dependence of CDSBS.
cdsbs	0.0	coupling from Vd to Vbs for improved dVbi model.
lcdsbs	0.0	Length dependence of CDSBS.
wcdsbs	0.0	Width dependence of CDSBS.
pcdsbs	0.0	Area dependence of CDSBS.
phin	0.045 V	Non-uniform vertical doping effect on surface potential.

© 2023 Cadence Design Systems, Inc.

lphin	0.0 m V	Length dependence of PHIN.
wphin	0.0 m V	Width dependence of PHIN.
pphin	0.0 m^2 V	Area dependence of PHIN.
eta0	0.08	DIBL coefficient.
leta0	0.0 m	Length dependence of ETA0.
weta0	0.0 m	Width dependence of ETA0.
peta0	0.0 m^2	Area dependence of ETA0.
eta0r	0.08	DIBL coefficient.
leta0r	0.0 m	Length dependence of ETA0R.
weta0r	0.0 m	Width dependence of ETA0R.
peta0r	0.0 m^2	Area dependence of ETA0R.
dsub	1.0	Length scaling exponent for DIBL.
etab	(-0.07) 1/V	Body bias coefficient for subthreshold DIBL effect.
etabexp	1.0	Exponent coefficient of ETAB.
letab	0.0 m/V	Length dependence of ETAB.
wetab	0.0 m/V	Width dependence of ETAB.
petab	0.0 m^2/V	Area dependence of ETAB.
etae	0.0 1/V	Body bias coefficient for subthreshold DIBL effect.
etaeexp	1.0	Exponent coefficient of ETAE.

© 2023 Cadence Design Systems, Inc.

letae	0.0 m/V	Length dependence of ETAE.
wetae	0.0 m/V	Width dependence of ETAE.
petae	0.0 m^2/V	Area dependence of ETAE.
eta1	0.0 1/V	Body bias coefficient for subthreshold DIBL effect.
eta1exp	1.0	Exponent coefficient of ETAE.
leta1	0.0 m/V	Length dependence of ETA1.
weta1	0.0 m/V	Width dependence of ETA1.
peta1	0.0 m^2/V	Area dependence of ETA1.
k1	0.0 V^0.5	First-order body-bias Vth shift due to vertical non-uniform doping.
k1l	0.0	length dependence coefficient of K1.
k1lexp	1.0	Length dependence exponent coefficient of K1.
k1w	0.0	Width dependence coefficient of K1.
k1wexp	1.0	Width dependence exponent coefficient of K1.
k1wl	0.0	Width-length dependence coefficient of K1.
k1wlexp	1.0	Width-length dependence exponent coefficient of K1.
lk1	0.0 m V^0.5	Length dependence of K1.
wk1	0.0 m V^0.5	Width dependence of K1.

© 2023 Cadence Design Systems, Inc.

pk1	0.0 m^2 V^0.5	Area dependence of K1.
k2	0.0 V	Vth shift due to vertical non-uniform doping.
k2l	0.0 m^K2LEXP	Length dependence coefficient of K2.
k2lexp	1.0	Length dependence exponent coefficient of K2.
k2w	0.0 m^K2WEXP	Width dependence coefficient of K2.
k2wexp	1.0	Width dependence exponent coefficient of K2.
k2wl	0.0 m^(2 K2WLEXP)	Width-length dependence coefficient of K2.
k2wlexp	1.0	Width-length dependence exponent coefficient of K2.
lk2	0.0 m	Length dependence of K2.
wk2	0.0 m	Width dependence of K2.
pk2	0.0 m^2	Area dependence of K2.
ados	0.0	Quantum mechanical effect pre-factor switch in inversion.
bdos	1.0	Charge centroid parameter - slope of C-V curve under QME in inversion.
qm0	1.0e-3	Charge centroid parameter - starting point for QME in inversion.
etaqm	0.54	Bulk charge coefficient for charge centroid in inversion.

© 2023 Cadence Design Systems, Inc.

cit	0.0 F/m^2	Parameter for interface traps.
lcit	0.0 F/m	Length dependence of CIT.
wcit	0.0 F/m	Width dependence of CIT.
pcit	0.0 F	Area dependence of CIT.
nfactor	0.0	Subthreshold slope factor.
nfactorl	0.0 m^NFACTORLEXP	Length dependence coefficient of NFACTOR.
nfactorlexp	1.0	Length dependence exponent coefficient of NFACTOR.
nfactorw	0.0 m^NFACTORWEXP	Width dependence coefficient of NFACTOR.
nfactorwexp	1.0	Width dependence exponent coefficient of NFACTOR.
nfactorwl	0.0 m^(2 NFACTORWLEXP)	Width-length dependence coefficient of NFACTOR.
nfactorwlexp	1.0	Width-length dependence exponent coefficient of NFACTOR.
lnfactor	0.0 m	Length dependence of NFACTOR.
wnfactor	0.0 m	Width dependence of NFACTOR.
pnfactor	0.0 m^2	Area dependence of NFACTOR.
ascl	0.0	Parameter for back-gate dependent scale length.

© 2023 Cadence Design Systems, Inc.

lascl	0.0	L-term of ASCL.
wascl	0.0	W-term of ASCL.
pascl	0.0	P-term of ASCL.
bscl	0.0	Parameter for back-gate dependent scale length.
lbscl	0.0	L-term of BSCL.
wbscl	0.0	W-term of BSCL.
pbscl	0.0	P-term of BSCL.
dvt1	1.0	SCE coefficient.
ldvt1	0.0	L-term of DVT1.
wdvt1	0.0	W-term of DVT1.
pdvt1	0.0	P-term of DVT1.
cdscd	0.0 F/m^2/V	Drain bias sensitivity of subthreshold slope.
lcdscd	0.0 F/m/V	Length dependence of CDSCD.
wcdscd	0.0 F/m/V	Width dependence of CDSCD.
pcdscd	0.0 F/V	Area dependence of CDSCD.
cdsc	1e-9 F/m^2/V	Coupling capacitance between S/D and channel.
lcdsc	0.0 F/m/V	Length dependence of CDSCD.

© 2023 Cadence Design Systems, Inc.

wcdsc	0.0 F/m/V	Width dependence of CDSCD.
pcdsc	0.0 F/V	Area dependence of CDSCD.
csecsed	0.0 F/(m^2 V^2)	Substrate-bias sensitivity of CDSCD.
cbcbd	0.0 F/(m^2 V^2)	Body bias sensitivity of CDSCD.
csecse0	0.0 F/(m^2 V)	Substrate-bias sensitivity of SS for long channel.
csecse0p	0.0 F/(m^2 V^2)	Substrate-bias sensitivity of SS for long channel.
csecse	0.0 F/(m^2 V)	Substrate-bias sensitivity of SS for long channel.
lcsecse	0.0 F/m/V	Length dependence of CDSCD.
wcsecse	0.0 F/m/V	Width dependence of CDSCD.
pcsecse	0.0 F/V	Area dependence of CDSCD.
csecsep	0.0 F/(m^2 V)	Substrate-bias sensitivity of SS for long channel.
cbcb	0.0 F/(m^2 V)	Substrate-bias sensitivity of SS for long channel.
lcbcb	0.0 F/m/V	Length dependence of CDSCD.
wcbcb	0.0 F/m/V	Width dependence of CDSCD.

© 2023 Cadence Design Systems, Inc.

pcbcb	0.0 F/V	Area dependence of CDSCD.
cbcbp	0.0 F/(m^2 V)	Substrate-bias sensitivity of SS for long channel.
cbcb0	0.0 F/(m^2 V)	Body-bias sensitivity of SS for long channel.
cbcb0p	0.0 F/(m^2 V^2)	Body-bias sensitivity of SS for long channel.
cdscdl	0.0 m^CDSCDL EXP	Length dependence coefficient of CDSCD.
cdscdlexp	1.0	Length dependence exponent coefficient of CDSCD.
cdscdr	0.0 F/m^2/V	Drain bias sensitivity of subthreshold slope.
lcdscdr	0.0 F/m/V	Length dependence of CDSCDR.
wcdscdr	0.0 F/m/V	Width dependence of CDSCDR.
pcdscdr	0.0 F/V	Area dependence of CDSCDR.
cdscb	0.0 F/m^2/V	Body-bias sensitivity of subthreshold slope.
cdscbl	0.0 m^CDSCBL EXP	Length dependence coefficient of CDSCB.
cdscblexp	1.0	Length dependence exponent coefficient of CDSCB.
lcdscb	0.0 F/m/V	Length dependence of CDSCB.

© 2023 Cadence Design Systems, Inc.

wcdscb	0.0 F/m/V	Width dependence of CDSCB.
pcdscb	0.0 F/V	Area dependence of CDSCB.
vbsa	0.0 V	vbsa offset voltage.
vsat	1e5 m/s	Saturation velocity.
lvsat	0.0 m^2/s	Length dependence of VSAT.
wvsat	0.0 m^2/s	Width dependence of VSAT.
pvsat	0.0 m^3/s	Area dependence of VSAT.
vsatl	0.0 m^VSATLEXP	Length dependence coefficient of VSAT.
vsatlexp	1.0	Length dependence exponent coefficient of VSAT.
vsatw	0.0 m^VSATWEXP	Width dependence coefficient of VSAT.
vsatwexp	1.0	Width dependence exponent coefficient of VSAT.
vsatwl	0.0 m^(2 VSATWLEXP)	Width-length dependence coefficient of VSAT.
vsatwlexp	1.0	Width-length dependence exponent coefficient of of VSAT.
vsatr	1e5 m/s	Saturation velocity.
lvsatr	0.0 m^2/s	Length dependence of VSATR.
wvsatr	0.0 m^2/s	Width dependence of VSATR.

© 2023 Cadence Design Systems, Inc.

pvsatr	0.0 m^3/s	Area dependence of VSATR.
delta	0.125	Smoothing function factor for Vdsat.
ldelta	0.0 m	Length dependence of DELTA.
wdelta	0.0 m	Width dependence of DELTA.
pdelta	0.0 m^2	Area dependence of DELTA.
deltal	0.0 m^DELTALEXP	Length dependence coefficient of DELTA.
deltalexp	1.0	Length dependence exponent coefficient of DELTA.
vsatcv	1e5 m/s	VSAT parameter for C-V.
lvsatcv	0.0 m^2/s	Length dependence of VSATCV.
wvsatcv	0.0 m^2/s	Width dependence of VSATCV.
pvsatcv	0.0 m^3/s	Area dependence of VSATCV.
vsatcvl	0.0 m^VSATLEXP	Length dependence coefficient of VSATCV.
vsatcvlexp	1.0	Length dependence exponent coefficient of VSATCV.
vsatcvw	0.0 m^VSATWEXP	Width dependence coefficient of VSATCV.
vsatcvwexp	1.0	Width dependence exponent coefficient of VSATCV.

© 2023 Cadence Design Systems, Inc.

vsatcvwl	0.0 m^(2 VSATWLEXP)	Width-length dependence coefficient of VSATCV.
vsatcvwlexp	1.0	Width-length dependence exponent coefficient of VSATCV.
thesat	0.3	Saturation velocity dependent parameter.
lthesat	0.0 m^2/s	Length dependence of THESAT.
wthesat	0.0 m^2/s	Width dependence of THESAT.
pthesat	0.0 m^3/s	Area dependence of THESAT.
lpe1	0.0	Equivalent length of pocket region at zero bias.
llpe1	0.0 m^2/s	Length dependence of LPE0.
wlpe1	0.0 m^2/s	Width dependence of LPE0.
plpe1	0.0 m^3/s	Area dependence of LPE0.
up1	0.0	Mobility channel length coefficient.
lp1	1.0e-8 m	Mobility channel length exponential coefficient.
up2	0.0	Mobility channel length coefficient.
lp2	1.0e-8 m	Mobility channel length exponential coefficient.
u0	67.0e-3 $m^2/V/s$	Low Field mobility..
u0l	0.0 m^U0LEXP	Length dependence coefficient of U0L.
u0lexp	1.0	Length dependence exponent coefficient of U0L.

© 2023 Cadence Design Systems, Inc.

lu0	0.0 m^3/V/s	Length dependence of U0.
wu0	0.0 m^3/V/s	Width dependence of U0.
pu0	0.0 m^4/V/s	Area dependence of U0.
u0r	67.0e-3 m^2/V/s	Reverse-mode Low Field mobility..
lu0r	0.0 m^3/V/s	Length dependence of U0R.
wu0r	0.0 m^3/V/s	Width dependence of U0R.
pu0r	0.0 m^4/V/s	Area dependence of U0R.
etamob	1.0	Effective field parameter (should be kept close to 1).
ua	0.001 (m/V)^EU	Mobility reduction coefficient.
ual	0.0 m^UALEXP	Length dependence coefficient of UA.
ualexp	1.0	Length dependence exponent coefficient of UA.
uaw	0.0 m^UAWEXP	Width dependence coefficient of UA.
uawexp	1.0	Width dependence exponent coefficient of UA.
uawl	0.0 m^UAWLEXP	Width-length dependence coefficient of UA.

© 2023 Cadence Design Systems, Inc.

uawlexp	1.0	Width-length dependence coefficient of UA.
lua	0.0 m (m/V)^EU	Length dependence of UA.
wua	0.0 m (m/V)^EU	Width dependence of UA.
pua	0.0 m^2 (m/V)^EU	Area dependence of UA.
uar	0.001 (m/V)^EU	Reverse-mode mobility reduction coefficient.
luar	0.0 m (m/V)^EU	Length dependence of UAR.
wuar	0.0 m (m/V)^EU	Width dependence of UAR.
puar	0.0 m^2 (m/V)^EU	Area dependence of UAR.
eu	1.5	Mobility reduction exponent.
leu	0.0 m	Length dependence of EU.
weu	0.0 m	Width dependence of EU.
peu	0.0 m^2	Area dependence of EU.
eul	0.0 m^EULEXP	Length dependence coefficient of EU.
eulexp	1.0	Length dependence exponent coefficient of EU.
euw	0.0 m^EUWEXP	Width dependence coefficient of EU.

© 2023 Cadence Design Systems, Inc.

euwexp	1.0	Width dependence exponent coefficient of EU.
euwl	0.0 m^EUWLEXP	Width-length dependence coefficient of EU.
euwlexp	1.0	Width-length dependence coefficient of EU.
ud	0.001	Coulomb scattering parameter.
udl	0.0 m^UDLEXP	Length dependence coefficient of UD.
udlexp	1.0	Length dependence exponent coefficient of UD.
lud	0.0 m	Length dependence of UD.
wud	0.0 m	Width dependence of UD.
pud	0.0 m^2	Area dependence of UD.
udr	0.001	Reverse-mode Coulomb scattering parameter.
ludr	0.0 m	Length dependence of UDR.
wudr	0.0 m	Width dependence of UDR.
pudr	0.0 m^2	Area dependence of UDR.
ucs	2.0	Coulomb scattering parameter.
lucs	0.0 m	Length dependence of UCS.
wucs	0.0 m	Width dependence of UCS.
pucs	0.0 m^2	Area dependence of UCS.
ucsr	2.0	Reverse-mode Coulomb scattering parameter.

© 2023 Cadence Design Systems, Inc.

lucsr	0.0 m	Length dependence of UCSR.
wucsr	0.0 m	Width dependence of UCSR.
pucsr	0.0 m^2	Area dependence of UCSR.
uc	0.0 (m/V)^EU/V	Mobility reduction with body bias.
ucl	0.0 m^UCLEXP	Length dependence coefficient of UC.
uclexp	1.0	Length dependence exponent coefficient of UC.
ucw	0.0 m^UCWEXP	Width dependence coefficient of UC.
ucwexp	1.0	Width dependence exponent coefficient of UC.
ucwl	0.0 m^(2 UCWLEXP)	Width-length dependence coefficient of UC.
ucwlexp	1.0	Width-length dependence exponent coefficient of UC.
luc	0.0 m (m/V)^EU/V	Length dependence of UC.
wuc	0.0 m (m/V)^EU/V	Width dependence of UC.
puc	0.0 m^2 (m/V)^EU/V	Area dependence of UC.
ucr	0.0 (m/V)^EU/V	Reverse-mode mobility reduction with body bias.

© 2023 Cadence Design Systems, Inc.

lucr	0.0 m (m/V)^EU/V	Length dependence of UCR.
wucr	0.0 m (m/V)^EU/V	Width dependence of UCR.
pucr	0.0 m^2 (m/V)^EU/V	Area dependence of UCR.
pclm	0.003	CLM pre-factor.
pclml	0.0 m^PCLMLEXP	Length dependence coefficient of PCLM.
pclmlexp	1.0	Length dependence exponent coefficient of PCLM.
lpclm	0.0 m	Length dependence of PCLM.
wpclm	0.0 m	Width dependence of PCLM.
ppclm	0.0 m^2	Area dependence of PCLM.
pclmr	0.003	Reverse-mode CLM pre-factor.
lpclmr	0.0 m	Length dependence of PCLMR.
wpclmr	0.0 m	Width dependence of PCLMR.
ppclmr	0.0 m^2	Area dependence of PCLMR.
pclmg	0.0 V	CLM pre-factor gate voltage dependence.
pclmcv	0.003	CLM parameter for C-V.

© 2023 Cadence Design Systems, Inc.

pclmcvl	0.0 m^PCLMLEXP	Length dependence coefficient of PCLMCV.
pclmcvlexp	1.0	Length dependence exponent coefficient of PCLMCV.
lpclmcv	0.0 m	Length dependence of PCLMCV.
wpclmcv	0.0 m	Width dependence of PCLMCV.
ppclmcv	0.0 m^2	Area dependence of PCLMCV.
pscbe1	4.24e8 V/m	Substrate current body-effect coefficient.
lpscbe1	0.0 V	Length dependence of PSCBE1.
wpscbe1	0.0 V	Width dependence of PSCBE1.
ppscbe1	0.0 V m	Area dependence of PSCBE1.
pscbe2	1.0e-8 m/V	Substrate current body-effect coefficient.
lpscbe2	0.0 m^2/V	Length dependence of PSCBE2.
wpscbe2	0.0 m^2/V	Width dependence of PSCBE2.
ppscbe2	0.0 m^3/V	Area dependence of PSCBE2.
pdits	0.0 1/V	Coefficient for drain-induced Vth shift.
lpdits	0.0 m/V	Length dependence of PDITS.
wpdits	0.0 m/V	Width dependence of PDITS.
ppdits	0.0 m^2/V	Area dependence of PDITS.

© 2023 Cadence Design Systems, Inc.

pditsl	0.0 1/m	L dependence of drain-induced Vth shift.
pditsd	0.0 1/V	Vds dependence of drain-induced Vth shift.
lpditsd	0.0 m/V	Length dependence of PDITSD.
wpditsd	0.0 m/V	Width dependence of PDITSD.
ppditsd	0.0 m^2/V	Area dependence of PDITSD.
rsh	0.0 ohm/ square	Source-drain sheet resistances.
prwg	1.0 1/V	Gate bias dependence of S/D extension resistances.
lprwg	0.0 m/V	Length dependence of PRWG.
wprwg	0.0 m/V	Width dependence of PRWG.
pprwg	0.0 m^2/V	Area dependence of PRWG.
prwb	0.0 1/V	Body bias dependence of resistances.
lprwb	0.0 m/V	Length dependence of PRWB.
wprwb	0.0 m/V	Width dependence of PRWB.
pprwb	0.0 m^2/V	Area dependence of PRWB.
prwbl	0.0 m^PRWBLE XP	Length dependence coefficient of PPRWB.
prwblexp	1.0	Length dependence exponent coefficient of PPRWB.
wr	1.0	W dependence parameter of S/D extension resistances.

© 2023 Cadence Design Systems, Inc.

lwr	0.0 m	Length dependence of WR.
wwr	0.0 m	Width dependence of WR.
pwr	0.0 m^2	Area dependence of WR.
rswmin	0.0 ohm µm^WR	Source resistance per unit width at high Vgs (RDSMOD = 1).
lrswmin	0.0 ohm µm^(2 WR)	Length dependence of RSWMIN.
wrswmin	0.0 ohm µm^(2 WR)	Width dependence of RSWMIN.
prswmin	0.0 ohm µm^(3 WR)	Area dependence of RSWMIN.
rsw	10.0 ohm µm^WR	Zero bias source resistance (RDSMOD = 1).
lrsw	0.0 ohm µm^(2 WR)	Length dependence of RSW.
wrsw	0.0 ohm µm^(2 WR)	Width dependence of RSW.
prsw	0.0 ohm µm^(3 WR)	Area dependence of RSW.
rswl	0.0 m^RSWLEXP	Geometrical scaling of RSW (RDSMOD = 1).

© 2023 Cadence Design Systems, Inc.

rswlexp	1.0	Geometrical scaling of RSW (RDSMOD = 1).
rdwmin	0.0 ohm µm^WR	Drain resistance per unit width at high Vgs (RDSMOD = 1).
lrdwmin	0.0 ohm µm^(2 WR)	Length dependence of RDWMIN.
wrdwmin	0.0 ohm µm^(2 WR)	Width dependence of RDWMIN.
prdwmin	0.0 ohm µm^(3 WR)	Area dependence of RDWMIN.
rdw	10.0 ohm µm^WR	Zero bias drain resistance (RDSMOD = 1).
lrdw	0.0 ohm µm^(2 WR)	Length dependence of RDW.
wrdw	0.0 ohm µm^(2 WR)	Width dependence of RDW.
prdw	0.0 ohm µm^(3 WR)	Area dependence of RDW.
rdwl	0.0 m^RDWLEXP	Geometrical scaling of RDW (RDSMOD = 1).
rdwlexp	1.0	Geometrical scaling of RDW (RDSMOD = 1).

© 2023 Cadence Design Systems, Inc.

rdswmin	0.0 ohm µm^WR	S/D Resistance per unit width at high Vgs (RDSMOD = 0 and RDSMOD = 2).
lrdswmin	0.0 ohm µm^(2 WR)	Length dependence of RDSWMIN.
wrdswmin	0.0 ohm µm^(2 WR)	Width dependence of RDSWMIN.
prdswmin	0.0 ohm µm^(3 WR)	Area dependence of RDSWMIN.
rdsw	20.0 ohm µm^WR	Zero bias resistance (RDSMOD = 0 and RDSMOD = 2).
rdswl	0.0 m^RDSWLEXP	Geometrical scaling of RDSW (RDSMOD = 0 and RDSMOD = 2).
rdswlexp	1.0	Geometrical scaling of RDSW (RDSMOD = 0 and RDSMOD = 2).
lrdsw	0.0 ohm µm^(2 WR)	Length dependence of RDSW.
wrdsw	0.0 ohm µm^(2 WR)	Width dependence of RDSW.
prdsw	0.0 ohm µm^(3 WR)	Area dependence of RDSW.
psat	1.0	Gmsat variation with gate bias.

© 2023 Cadence Design Systems, Inc.

lpsat	0.0 m	Length dependence of PSAT.
wpsat	0.0 m	Width dependence of PSAT.
ppsat	0.0 m^2	Area dependence of PSAT.
psatl	0.0 m^PSATLEXP	Length dependence coefficient of PSATL.
psatlexp	1.0	Length dependence exponent coefficient of PSATLEXP.
psatb	0.0 1/V	Body bias effect on Idsat.
psatr	1.0	Reverse-mode Gmsat variation with gate bias.
lpsatr	0.0 m	Length dependence of PSATR.
wpsatr	0.0 m	Width dependence of PSATR.
ppsatr	0.0 m^2	Area dependence of PSATR.
lpsatb	0.0 m/V	Length dependence of PSATB.
wpsatb	0.0 m/V	Width dependence of PSATB.
ppsatb	0.0 m^2/V	Area dependence of PSATB.
psatx	1.0	Fine tuning of PTWG effect.
ptwg	0.0	Idsat variation with gate bias.
lptwg	0.0 m	Length dependence of PTWG.
wptwg	0.0 m	Width dependence of PTWG.
pptwg	0.0 m^2	Area dependence of PTWG.

© 2023 Cadence Design Systems, Inc.

ptwgl	0.0 m^PTWGLEXP	Length dependence coefficient of PTWG.
vp	0.05	parameter for CLM dependence on VSAT, DD Model.
alp	0.01	parameter for CLM dependence on VSAT, DD Model.
ptwglexp	1.0	Length dependence exponent coefficient of PTWG.
ptwgr	0.0	Reverse-mode Idsat variation with gate bias.
lptwgr	0.0 m	Length dependence of PTWGR.
wptwgr	0.0 m	Width dependence of PTWGR.
pptwgr	0.0 m^2	Area dependence of PTWGR.
ksativ	1.0	Parameter for Vdsat.
lksativ	0.0	Length dependence of KVSATIV.
wksativ	0.0	Width dependence of KVSATIV.
pksativ	0.0	Area dependence of KVSATIV.
a1	0.0 $1/V^2$	Non-saturation effect parameter for strong inversion region.
la1	0.0 m/V^2	Length dependence of A1.
wa1	0.0 m/V^2	Width dependence of A1.
pa1	0.0 m^2/V^2	Area dependence of A1.
a11	0.0	Temperature dependence of A1.

© 2023 Cadence Design Systems, Inc.

la11	0.0 m	Length dependence of A11.
wa11	0.0 m	Width dependence of A11.
pa11	0.0 m^2	Area dependence of A11.
a2	0.0 1/V	Non-saturation effect parameter for moderate inversion region.
la2	0.0 m/V	Length dependence of A2.
wa2	0.0 m/V	Width dependence of A2.
pa2	0.0 m^2/V	Area dependence of A2.
a21	0.0	Temperature dependence of A2.
la21	0.0 m	Length dependence of A21.
wa21	0.0 m	Width dependence of A21.
pa21	0.0 m^2	Area dependence of A21.
pdiblc	0.0	Parameter for DIBL effect on Rout.
pdiblc1	0.0 m^PDIBLCLEXP	Length dependence coefficient of PDIBLC.
pdiblclexp	1.0	Length dependence exponent coefficient of PDIBLC.
lpdiblc	0.0 m	Length dependence of PDIBLC.
wpdiblc	0.0 m	Width dependence of PDIBLC.
ppdiblc	0.0 m^2	Area dependence of PDIBLC.
pdiblcr	0.0	Reverse-mode parameter for DIBL effect on Rout.

© 2023 Cadence Design Systems, Inc.

lpdiblcr	0.0 m	Length dependence of PDIBLCR.
wpdiblcr	0.0 m	Width dependence of PDIBLCR.
ppdiblcr	0.0 m^2	Area dependence of PDIBLCR.
pdiblcb	0.0 1/V	Parameter for DIBL effect on Rout.
lpdiblcb	0.0 m/V	Length dependence of PDIBLCB.
wpdiblcb	0.0 m/V	Width dependence of PDIBLCB.
ppdiblcb	0.0 m^2/V	Area dependence of PDIBLCB.
pvag	1.0	Vg dependence of early voltage.
lpvag	0.0 m	Length dependence of PVAG.
wpvag	0.0 m	Width dependence of PVAG.
ppvag	0.0 m^2	Area dependence of PVAG.
fprout	0.0 V/ m^0.5	Gds degradation factor due to pocket implants.
fproutl	0.0 m^FPROUT LEXP	Length dependence coefficient of FPROUT.
fproutlexp	1.0	Length dependence exponent coefficient of FPROUT.
lfprout	0.0 V m^0.5	Length dependence of FPROUT.
wfprout	0.0 V m^0.5	Width dependence of FPROUT.

© 2023 Cadence Design Systems, Inc.

pfprout	0.0 V m^1.5	Area dependence of FPROUT.
vabjt	10.0 V	Early voltage for bipolar current.
lvabjt	0.0	Length dependence of vabjt.
wvabjt	0.0	Width dependence of vabjt.
pvabjt	0.0	Cross-term dependence of vabjt.
aely	0.0 V/m	Channel length dependency of early voltage for bipolar current.
laely	0.0	Length dependence of aely.
waely	0.0	Width dependence of aely.
paely	0.0	Cross-term dependence of aely.
ahli	0.0	High level injection parameter for bipolar current /* v4.0 .
ahlid	0.0	High level injection parameter for bipolar current /* v4.0 .
lahli	0.0	Length dependence of ahli /*v4.0.
lahlid	0.0	Length dependence of ahlid /*v4.0.
wahli	0.0	Width dependence of ahli /* v4.0 .
wahlid	0.0	Width dependence of ahlid /* v4.0 .
pahli	0.0	X-term dependence of ahli /* v4.0 .
pahlid	0.0	X-term dependence of ahlid /* v4.0 .
xbjt	1.0	Temperature coefficient for Isbjt.

© 2023 Cadence Design Systems, Inc.

lxbjt	0.0		Length dependence of xbjt.
wxbjt	0.0		Width dependence of xbjt.
pxbjt	0.0		Cross-term dependence of xbjt.
ndiode	1.0		Diode non-ideality factor /*v4.0.
lndiode	0.0		Length dependence of ndiode.
wndiode	0.0		Width dependence of ndiode.
pndiode	0.0		Cross-term dependence of ndiode.
isbjt	0.0	A/m^2	BJT injection saturation current.
pisbjt	0.0		Cross-term dependence of isbjt.
wisbjt	0.0		Width dependence of isbjt.
lisbjt	0.0		Length dependence of isbjt.
idbjt	0.0	A/m^2	BJT injection saturation current.
lidbjt	0.0		Length dependence of idbjt.
widbjt	0.0		Width dependence of idbjt.
pidbjt	0.0		Cross-term dependence of idbjt.
nbjt	1.0		Power coefficient of channel length dependency for bipolar current.
lnbjt	0.0		Length dependence of nbjt.
llbjt0	0.0		Length dependence of lbjt0.
wnbjt	0.0		Width dependence of nbjt.

© 2023 Cadence Design Systems, Inc.

wlbjt0	0.0	Width dependence of lbjt0.
pnbjt	0.0	Cross-term dependence of nbjt.
plbjt0	0.0	Cross-term dependence of lbjt0.
lbjt0	0.20e-6 m	Reference channel length for bipolar current.
ln	2e-6 m	Electron/hole diffusion length.
vdsatii0	0.9	Nominal drain saturation voltage at threshold for impact ionization current.
lvdsatii0	0.0	Length dependence of vdsatii0.
wvdsatii0	0.0	Width dependence of vdsatii0.
pvdsatii0	0.0	Cross-term dependence of vdsatii0.
tii	0.0	Temperature dependent parameter for impact ionization.
alpha0	0.0 m/V	substrate current model parameter.
alpha0l	0.0 m^ALPHA0LEXP	Length dependence coefficient of ALPHA0.
alpha0lexp	1.0	Length dependence exponent coefficient of ALPHA0.
lalpha0	0.0 m^2/V	Length dependence of ALPHA0.
walpha0	0.0 m^2/V	Width dependence of ALPHA0.
palpha0	0.0 m^3/V	Area dependence of ALPHA0.

© 2023 Cadence Design Systems, Inc.

beta0	0.0 1/V	First Vds dependent parameter of impact ionization current.
lbeta0	0.0 m/V	Length dependence of BETA0.
wbeta0	0.0 m/V	Width dependence of BETA0.
pbeta0	0.0 m^2/V	Area dependence of BETA0.
beta1	0.0	Second Vds dependent parameter of impact ionization current.
lbeta1	0.0 m/V	Length dependence of BETA0.
wbeta1	0.0 m/V	Width dependence of BETA0.
pbeta1	0.0 m^2/V	Area dependence of BETA0.
beta2	0.1 V	Third Vds dependent parameter of impact ionization current.
lbeta2	0.0 m/V	Length dependence of BETA0.
wbeta2	0.0 m/V	Width dependence of BETA0.
pbeta2	0.0 m^2/V	Area dependence of BETA0.
lii	0.0	Channel length dependent parameter at threshold for impact ionization current.
llii	0.0 m/V	Length dependence of LII.
wlii	0.0 m/V	Width dependence of LII.
plii	0.0 m^2/V	Area dependence of LII.
sii0	0.5	First Vgs dependent parameter for impact ionization current.

© 2023 Cadence Design Systems, Inc.

lsii0	0.0 m/V	Length dependence of SII0.
wsii0	0.0 m/V	Width dependence of SII0.
psii0	0.0 m^2/V	Area dependence of SII0.
sii1	0.1	Second Vgs dependent parameter for impact ionization current.
lsii1	0.0 m/V	Length dependence of SII1.
wsii1	0.0 m/V	Width dependence of SII1.
psii1	0.0 m^2/V	Area dependence of SII1.
sii2	0.0	Third Vgs dependent parameter for impact ionization current.
lsii2	0.0 m/V	Length dependence of SII2.
wsii2	0.0 m/V	Width dependence of SII2.
psii2	0.0 m^2/V	Area dependence of SII2.
siid	0.0	Vds dependent parameter of drain saturation voltage for impact ionization current.
lsiid	0.0 m/V	Length dependence of SIID.
wsiid	0.0 m/V	Width dependence of SIID.
psiid	0.0 m^2/V	Area dependence of SIID.
esatii	1e7 V/m	Saturation electric field for impact ionization.
lesatii	0.0 m/V	Length dependence of ESATII.
wesatii	0.0 m/V	Width dependence of ESATII.

© 2023 Cadence Design Systems, Inc.

pesatii	0.0 m^2/V	Area dependence of SESATII.
iimod2clamp1	0.1 V	Clamp1 of SII1 * Vg term in IIMOD = 2.
iimod2clamp2	0.1 V	Clamp2 of SII0 * Vg term in IIMOD = 2.
iimod2clamp3	0.1 V	Clamp3 of ratio term in IIMOD = 2.
fbjtii	0.0	Fraction of bipolar current affecting the impact ionization.
lfbjtii	0.0	Length dependence of fbjtii.
wfbjtii	0.0	Width dependence of fbjtii.
pfbjtii	0.0	Cross-term dependence of fbjtii.
ebjtii	0.0	Impact ionization parameter for BJT part.
cbjtii	0.0 m	Length scaling parameter for II BJT part.
abjtii	0.0 1/V	Exponent factor for avalanche current.
labjtii	0.0	Length dependence of abjtii.
lcbjtii	0.0	Length dependence of cbjtii.
lebjtii	0.0	Length dependence of ebjtii.
wabjtii	0.0	Width dependence of abjtii.
wcbjtii	0.0	Width dependence of cbjtii.
webjtii	0.0	Width dependence of ebjtii.
pabjtii	0.0	Cross-term dependence of abjtii.
pcbjtii	0.0	Cross-term dependence of cbjtii.

© 2023 Cadence Design Systems, Inc.

pebjtii	0.0	Cross-term dependence of ebjtii.
vbci	0.0 V	Internal B-C built-in potential.
lvbci	0.0	Length dependence of vbci.
wvbci	0.0	Width dependence of vbci.
pvbci	0.0	Cross-term dependence of vbci.
tvbci	0.0	Temperature coefficient for VBCI.
mbjtii	0.4	Internal B-C grading coefficient.
lmbjtii	0.0	Length dependence of mbjtii.
wmbjtii	0.0	Width dependence of mbjtii.
pmbjtii	0.0	Cross-term dependence of mbjtii.
vecb	0.026	Vaux parameter for conduction-band electron tunneling.
alphagb1	0.35 1/V	First Vox dependent parameter for gate current in inversion.
lalphagb1	0.0	Length dependence of alphagb1.
walphagb1	0.0	Width dependence of alphagb1.
palphagb1	0.0	Cross-term dependence of alphagb1.
alphagb1_t	0.0	Temperature coefficient of ALPHAGB1.
lalphagb1_t	0.0	Length dependence of ALPHAGB1_T.
walphagb1_t	0.0	Width dependence of ALPHAGB1_T.

© 2023 Cadence Design Systems, Inc.

palphagb1_t	0.0	Cross-term dependence of ALPHAGB1_T.
betagb1	0.03 1/V^2	Second Vox dependent parameter for gate current in inversion.
lbetagb1	0.0	Length dependence of betagb1.
wbetagb1	0.0	Width dependence of betagb1.
pbetagb1	0.0	Cross-term dependence of betagb1.
alphagb2	0.43 1/V	First Vox dependent parameter for gate current in accumulation.
lalphagb2	0.0	Length dependence of aigbcp2.
walphagb2	0.0	Width dependence of alphagb2.
palphagb2	0.0	Cross-term dependence of alphagb2.
alphagb2_t	0.0	Temperature coefficient of ALPHAGB2.
lalphagb2_t	0.0	Length dependence of ALPHAGB2_T.
walphagb2_t	0.0	Width dependence of ALPHAGB2_T.
palphagb2_t	0.0	Cross-term dependence of alphagb2_t.
betagb2	0.05 1/V^2	Second Vox dependent parameter for gate current in accumulation.
lbetagb2	0.0	Length dependence of betagb2.
wbetagb2	0.0	Width dependence of betagb2.
pbetagb2	0.0	Cross-term dependence of betagb2.
vgb2	17 V	Third Vox dependent parameter for gate current in accumulation.

© 2023 Cadence Design Systems, Inc.

vgb1	300 V	Third Vox dependent parameter for gate current in inversion.
agb1	3.7622e-7	'A' for Igb1 Tunneling current model.
bgb1	(-3.1051e10)	'B' for Igb1 Tunneling current model.
agb2	4.9758e-7	'A' for Igb2 Tunneling current model.
bgb2	(-2.357e10)	'B' for Igb2 Tunneling current model.
agbc2n	3.4254e-7	NMOS 'A' for tunneling current model.
agbc2p	4.9723e-7	PMOS 'A' for tunneling current model.
bgbc2n	1.1665e12	NMOS 'B' for tunneling current model.
bgbc2p	7.4567e11	PMOS 'B' for tunneling current model.
eigbinv	1.1 V	Parameter for the Si bandgap for Igbinv.
aigc	1.36e-2 (F s^2/g)^0.5/m	Parameter for Igc.
bigc	1.71e-3 (F s^2/g)^0.5/m/V	Parameter for Igc.

© 2023 Cadence Design Systems, Inc.

cigc	0.075 1/V	Parameter for Igc.
aigs	1.36e-2 (F s^2/g)^0.5/m	Parameter for Igs.
aigs1	0.0	Temperature coefficient of AIGD.
bigs	1.71e-3 (F s^2/g)^0.5/m/V	Parameter for Igs.
cigs	0.075 1/V	Parameter for Igs.
aigd	1.36e-2 (F s^2/g)^0.5/m	Parameter for Igd.
aigd1	0.0	Temperature coefficient of AIGD.
bigd	1.71e-3 (F s^2/g)^0.5/m/V	Parameter for Igd.
cigd	0.075 1/V	Parameter for Igd.
dlcig	0.0 m	Delta L for Ig model.
dlcigd	0.0 m	Delta L for Ig model.
poxedge	1.0	Factor for the gate edge Tox.
ntox	1.0	Exponent for Tox ratio.

© 2023 Cadence Design Systems, Inc.

toxref	3.0e-9 m	Target tox value.
pigcd	1.0	Igc, S/D partition parameter.
aigcl	0.0 m	Length dependence coefficient of AIGC.
aigcw	0.0 m	Width dependence coefficient of AIGC.
aigc1	0.0	Temperature coefficient of AIGC.
aigsl	0.0 m	Length dependence coefficient of AIGS.
aigsw	0.0 m	Width dependence coefficient of AIGS.
aigdl	0.0 m	Length dependence coefficient of AIGD.
aigdw	0.0 m	Width dependence coefficient of AIGD.
pigcdl	0.0 m	Length dependence coefficient of PIGCD.
leigbinv	0.0 m V	Length dependence of EIGBINV.
weigbinv	0.0 m V	Width dependence of EIGBINV.
peigbinv	0.0 m^2 V	Area dependence of EIGBINV.
laigc	0.0 (F s^2/ g)^0.5	Length dependence of AIGC.
laigc1	0.0	Length dependence of AIGC1.
waigc	0.0 (F s^2/ g)^0.5	Width dependence of AIGC.
waigc1	0.0	Width dependence of AIGC1.

© 2023 Cadence Design Systems, Inc.

paigc	0.0 m ($F s^2/g$)^0.5	Area dependence of AIGC.
paigc1	0.0	Cross-term dependence of AIGC1.
lbigc	0.0 ($F s^2/g$)^0.5/V	Length dependence of BIGC.
wbigc	0.0 ($F s^2/g$)^0.5/V	Width dependence of BIGC.
pbigc	0.0 m ($F s^2/g$)^0.5/V	Area dependence of BIGC.
lcigc	0.0 m/V	Length dependence of CIGC.
wcigc	0.0 m/V	Width dependence of CIGC.
pcigc	0.0 m^2/V	Area dependence of CIGC.
laigs	0.0 ($F s^2/g$)^0.5	Length dependence of AIGS.
laigs1	0.0	Length dependence of AIGS1.
waigs	0.0 ($F s^2/g$)^0.5	Width dependence of AIGS.
waigs1	0.0	Width dependence of AIGS1.
paigs	0.0 m ($F s^2/g$)^0.5	Area dependence of AIGS.

© 2023 Cadence Design Systems, Inc.

paigs1	0.0	Cross-term dependence of AIGS1.
lbigs	0.0 (F s^2/ g)^0.5/V	Length dependence of BIGS.
wbigs	0.0 (F s^2/ g)^0.5/V	Width dependence of BIGS.
pbigs	0.0 m (F s^2/ g)^0.5/V	Area dependence of BIGS.
lcigs	0.0 m/V	Length dependence of CIGS.
wcigs	0.0 m/V	Width dependence of CIGS.
pcigs	0.0 m^2/V	Area dependence of CIGS.
laigd	0.0 (F s^2/ g)^0.5	Length dependence of AIGD.
laigd1	0.0	Length dependence of AIGD1.
waigd	0.0 (F s^2/ g)^0.5	Width dependence of AIGD.
waigd1	0.0	Width dependence of AIGD1.
paigd	0.0 m (F s^2/ g)^0.5	Area dependence of AIGD.
paigd1	0.0	Cross-term dependence of AIGD1.

© 2023 Cadence Design Systems, Inc.

lbigd	0.0 (F s^2/ g)^0.5/V	Length dependence of BIGD.
wbigd	0.0 (F s^2/ g)^0.5/V	Width dependence of BIGD.
pbigd	0.0 m (F s^2/ g)^0.5/V	Area dependence of BIGD.
lcigd	0.0 m/V	Length dependence of CIGD.
wcigd	0.0 m/V	Width dependence of CIGD.
pcigd	0.0 m^2/V	Area dependence of CIGD.
lpoxedge	0.0 m	Length dependence of POXEDGE.
wpoxedge	0.0 m	Width dependence of POXEDGE.
ppoxedge	0.0 m^2	Area dependence of POXEDGE.
ldlcig	0.0 m^2	Length dependence of DLCIG.
wdlcig	0.0 m^2	Width dependence of DLCIG.
pdlcig	0.0 m^3	Area dependence of DLCIG.
ldlcigd	0.0 m^2	Length dependence of DLCIGD.
wdlcigd	0.0 m^2	Width dependence of DLCIGD.
pdlcigd	0.0 m^3	Area dependence of DLCIGD.
lntox	0.0 m	Length dependence of NTOX.
wntox	0.0 m	Width dependence of NTOX.

© 2023 Cadence Design Systems, Inc.

pntox	0.0 m^2	Area dependence of NTOX.
aigbcp2	0.043 $1/V^2$	First Vgp dependent parameter for gate current in accumulation in AGBCP2 region.
aigbcp2_t	0.0	Temperature coefficient of AIGBCP2.
bigbcp2	0.0054 $1/V^2$	Second Vgp dependent parameter for gate current in accumulation in AGBCP2 region.
cigbcp2	0.0075 $1/V^2$	Third Vgp dependent parameter for gate current in accumulation in AGBCP2 region.
laigbcp2	0.0	Length dependence of aigbcp2.
laigbcp2_t	0.0	Length dependence of AIGBCP2_T.
lbigbcp2	0.0	Length dependence of bigbcp2.
lcigbcp2	0.0	Length dependence of cigbcp2.
waigbcp2	0.0	Width dependence of aigbcp2.
waigbcp2_t	0.0	Width dependence of AIGBCP2_T.
wbigbcp2	0.0	Width dependence of bigbcp2.
wcigbcp2	0.0	Width dependence of cigbcp2.
paigbcp2	0.0	Cross-term dependence of aigbcp2.
paigbcp2_t	0.0	Cross-term dependence of AIGBCP2_T.
pbigbcp2	0.0	Cross-term dependence of bigbcp2.
pcigbcp2	0.0	Cross-term dependence of cigbcp2.
agidl	0.0 V/m	Pre-exponential coefficient for GIDL.

© 2023 Cadence Design Systems, Inc.

agidll	0.0 m	Length dependence coefficient of AGIDL.
agidlw	0.0 m	Width dependence coefficient of AGIDL.
lagidl	0.0 m^2	Length dependence of AGIDL.
wagidl	0.0 m^2	Width dependence of AGIDL.
pagidl	0.0 m^3	Area dependence of AGIDL.
bgidl	2.3e9 V/m	Exponential coefficient for GIDL.
bgidl1	0.0 V/m	Temperature coefficient of BGIDL.
lbgidl	0.0 V	Length dependence of BGIDL.
wbgidl	0.0 V	Width dependence of BGIDL.
pbgidl	0.0 V m	Area dependence of BGIDL.
lbgidl1	0.0	Length dependence of bgidl1.
wbgidl1	0.0	Width dependence of bgidl1.
pbgidl1	0.0	Cross-term dependence of bgidl1.
cgidl	0.5 V/m	Exponential coefficient for GIDL.
lcgidl	0.0 V	Length dependence of CGIDL.
wcgidl	0.0 V	Width dependence of CGIDL.
pcgidl	0.0 V m	Area dependence of CGIDL.
egidl	0.8 V	Band bending parameter for GIDL.
legidl	0.0 V m	Length dependence of EGIDL.

© 2023 Cadence Design Systems, Inc.

wegidl	0.0 V m	Width dependence of EGIDL.
pegidl	0.0 V m^2	Area dependence of EGIDL.
agisl	0.0 V/m	Pre-exponential coefficient for GISL.
agisll	0.0 m	Length dependence coefficient of AGISL.
agislw	0.0 m	Width dependence coefficient of AGISL.
lagisl	0.0 m^2	Length dependence of AGISL.
wagisl	0.0 m^2	Width dependence of AGISL.
pagisl	0.0 m^3	Area dependence of AGISL.
bgisl	2.3e9 V/m	Exponential coefficient for GISL.
bgisl1	0.0 V/m	Temperature coefficient of BGISL.
lbgisl	0.0 V	Length dependence of BGISL.
wbgisl	0.0 V	Width dependence of BGISL.
pbgisl	0.0 V m	Area dependence of BGISL.
lbgisl1	0.0	Length dependence of bgisl1.
wbgisl1	0.0	Width dependence of bgisl.
pbgisl1	0.0	Cross-term dependence of bgisl1.
cgisl	0.5 V/m	Exponential coefficient for GISL.
lcgisl	0.0 V	Length dependence of CGISL.
wcgisl	0.0 V	Width dependence of CGISL.

© 2023 Cadence Design Systems, Inc.

pcgisl	0.0 V m	Area dependence of CGISL.
egisl	0.8 V	Band bending parameter for GISL.
legisl	0.0 V m	Length dependence of EGISL.
wegisl	0.0 V m	Width dependence of EGISL.
pegisl	0.0 V m^2	Area dependence of EGISL.
rgidl	1.0	GIDL vg parameter.
lrgidl	0.0	Length dependence of rgidl.
wrgidl	0.0	Width dependence of rgidl.
prgidl	0.0	Cross-term dependence of rgidl.
kgidl	0.0 V	GIDL vb parameter.
lkgidl	0.0	Length dependence of kgidl.
wfgidl	0.0	Width dependence of fgidl.
pfgidl	0.0	Cross-term dependence of fgidl.
fgidl	0.0	GIDL vb parameter.
lfgidl	0.0	Length dependence of fgidl.
wkgidl	0.0	Width dependence of kgidl.
pkgidl	0.0	Cross-term dependence of kgidl.
rgisl	1.0	GISL vg parameter.
lrgisl	0.0	Length dependence of rgisl.

© 2023 Cadence Design Systems, Inc.

wrgisl	0.0	Width dependence of rgisl.
prgisl	0.0	Cross-term dependence of rgisl.
kgisl	0.0 V	GISL vb parameter.
lkgisl	0.0	Length dependence of kgisl.
wkgisl	0.0	Width dependence of kgisl.
pkgisl	0.0	Cross-term dependence of kgisl.
fgisl	0.0	GISL vb parameter.
lfgisl	0.0	Length dependence of fgisl.
wfgisl	0.0	Width dependence of fgisl.
pfgisl	0.0	Cross-term dependence of fgisl.
cf	0.0 F/m	Outer fringe capacitance.
lcf	0.0 F	Length dependence of CF.
wcf	0.0 F	Width dependence of CF.
pcf	0.0 F m	Area dependence of CF.
cfrcoeff	1.0 F/m	Coefficient for outer fringe capacitance.
cgso	0.0 F/m	Gate-to-source overlap capacitance.
cgdo	0.0 F/m	Gate-to-drain overlap capacitance.
cgbo	0.0 F/m	Gate-to-body overlap capacitance.
cgsl	0.0 F/m	Overlap capacitance between gate and lightly-doped source region.

© 2023 Cadence Design Systems, Inc.

lcgsl	0.0	Length dependence of CGSL.
wcgsl	0.0	Width dependence of CGSL.
pcgsl	0.0	Area dependence of CGSL.
cgdl	0.0 F/m	Overlap capacitance between gate and lightly-doped drain region.
lcgdl	0.0 F	Length dependence of CGDL.
wcgdl	0.0 F	Width dependence of CGDL.
pcgdl	0.0 F m	Area dependence of CGDL.
ckappas	0.6 V	Coefficient of bias-dependent overlap capacitance for the source side.
lckappas	0.0 m V	Length dependence of CKAPPAS.
wckappas	0.0 m V	Width dependence of CKAPPAS.
pckappas	0.0 m^2 V	Area dependence of CKAPPAS.
ckappad	0.6 V	Coefficient of bias-dependent overlap capacitance for the drain side.
lckappad	0.0 m V	Length dependence of CKAPPAD.
wckappad	0.0 m V	Width dependence of CKAPPAD.
pckappad	0.0 m^2 V	Area dependence of CKAPPAD.
ckappad1	1.0e6	Parameter for tuning CGD.
ckappad2	1.0	Parameter for tuning CGD.
ckappas1	1.0e6	Parameter for tuning CGD.

© 2023 Cadence Design Systems, Inc.

ckappas2	1.0	Parameter for tuning CGD.
dmcg	0.0 m	Distance of mid-contact to gate edge.
dmci	0.0 m	Distance of mid-contact to isolation.
dmdg	0.0 m	Distance of mid-diffusion to gate edge.
dmcgt	0.0 m	Distance of mid-contact to gate edge in test.
xgl	0.0 m	Variation in Ldrawn.
rshg	0.1 ohm	Gate sheet resistance.
cjs	5.0e-4 F/m^2	Unit area source-side junction capacitance at zero bias.
cjd	5.0e-4 F/m^2	Unit area drain-side junction capacitance at zero bias.
cjsws	5.0e-10 F/m	Unit length source-side side-wall junction capacitance at zero bias.
cjswd	5.0e-10 F/m	Unit length drain-side side-wall junction capacitance at zero bias.
cjswgs	0.0 F/m	Unit length source-side gate side-wall junction capacitance at zero bias.
cjswgd	0.0 F/m	Unit length drain-side gate side-wall junction capacitance at zero bias.
pbs	1.0 V	Source-side bulk junction built-in potential.
pbd	1.0 V	Drain-side bulk junction built-in potential.
pbsws	1.0 V	Built-in potential for Source-side side-wall junction capacitance.

© 2023 Cadence Design Systems, Inc.

pbswd	1.0 V	Built-in potential for Drain-side side-wall junction capacitance.
pbswgs	1.0 V	Built-in potential for Source-side gate side-wall junction capacitance.
pbswgd	1.0 V	Built-in potential for Drain-side gate side-wall junction capacitance.
mjs	0.5	Source bottom junction capacitance grading coefficient.
mjd	0.5	Drain bottom junction capacitance grading coefficient.
mjsws	0.33	Source side-wall junction capacitance grading coefficient.
mjswd	0.33	Drain side-wall junction capacitance grading coefficient.
mjswgs	0.33	Source-side gate side-wall junction capacitance grading coefficient.
mjswgd	0.33	Drain-side gate side-wall junction capacitance grading coefficient.
tt	1e-12 s	Diffusion capacitance transit time coefficient.
ldif0	1.0	Channel-length dependency coefficient of diffusion cap.
ndif	(-1.0)	Power coefficient of channel length dependency for diffusion capacitance.
lndif	0.0	Length dependence of ndif.
wndif	0.0	Width dependence of ndif.

© 2023 Cadence Design Systems, Inc.

pndif	0.0	Cross-term dependence of ndif.
vtm00	0.026 V	Hard coded 25 degC thermal voltage.
permod	1	Whether PS/PD (when given) include gate-edge perimeter.
dwj	0.0 m	Delta W for S/D junctions.
xdif	1.0	Temperature coefficient for Isdif.
lxdif	0.0	Length dependence of xdif.
wxdif	0.0	Width dependence of xdif.
pxdif	0.0	Crss-term dependence of xdif.
isdif	1e-7 A/m^2	Body to source/drain injection saturation current.
iddif	1e-7 A/m^2	Body to source/drain injection saturation current /* v4.0 .
lisdif	0.0	Length dependence of isdif.
liddif	0.0	Length dependence of iddif.
wisdif	0.0	Width dependence of isdif.
widdif	0.0	Width dependence of iddif.
pisdif	0.0	Cross-term dependence of isdif.
piddif	0.0	Cross-term dependence of iddif.
nrecf0	2.0	Recombination non-ideality factor at forward bias.
lnrecf0	0.0	Length dependence of nrecf0.

© 2023 Cadence Design Systems, Inc.

wnrecf0	0.0	Width dependence of nrecf0.
pnrecf0	0.0	Cross-term dependence of nrecf0.
nrecr0	10.0	Recombination non-ideality factor at reversed bias.
lnrecr0	0.0	Length dependence of nrecr0.
wnrecr0	0.0	Width dependence of nrecr0.
pnrecr0	0.0	Cross-term dependence of nrecr0.
xrec	1.0	Temperature coefficient for Isrec.
lxrec	0.0	Length dependence of xrec.
wxrec	0.0	Width dependence of xrec.
pxrec	0.0	cross-section dependence of xrec.
isrec	1e-5 A/m^2	Recombination in depletion saturation current.
idrec	1e-5 A/m^2	Recombination in depletion saturation current.
lisrec	0.0	Length dependence of isrec.
lidrec	0.0	Length dependence of idrec.
wisrec	0.0	Width dependence of isrec.
widrec	0.0	Width dependence of idrec.
pisrec	0.0	Cross-term dependence of isrec.
pidrec	0.0	Cross-term dependence of idrec.

© 2023 Cadence Design Systems, Inc.

ntrecf	0.0	Temperature coefficient for Nrecf.
ntrecr	0.0	Temperature coefficient for Nrecr.
lntrecf	0.0	Length dependence of ntrecf.
lntrecr	0.0	Length dependence of ntrecr.
wntrecf	0.0	Width dependence of ntrecf.
wntrecr	0.0	Width dependence of ntrecr.
pntrecf	0.0	Cross-term dependence of ntrecf.
pntrecr	0.0	Cross-term dependence of ntrecr.
istun	1e-8 A/m^2	Reverse tunneling saturation current.
idtun	1e-8 A/m^2	Reverse tunneling saturation current.
listun	0.0	Length dependence of istun.
lidtun	0.0	Length dependence of idtun.
wistun	0.0	Width dependence of istun.
widtun	0.0	Width dependence of idtun.
pistun	0.0	Cross-term dependence of istun.
pidtun	0.0	Cross-term dependence of idtun.
xtun	0.0	Temperature coefficient for Istun.
xtund	0.0	Temperature coefficient for Idtun.

© 2023 Cadence Design Systems, Inc.

lxtun	0.0	Length dependence of xtun.
lxtund	0.0	Length dependence of xtund.
wxtun	0.0	Width dependence of xtun.
wxtund	0.0	Width dependence of xtund.
pxtun	0.0	Cross-term dependence of xtun.
pxtund	0.0	Cross-term dependence of xtund.
ntun	10.0	Reverse tunneling non-ideality factor.
ntund	10.0	Reverse tunneling non-ideality factor.
lntun	0.0	Length dependence of ntun.
lntund	0.0	Length dependence of ntund.
wntun	0.0	Width dependence of ntun.
wntund	0.0	Width dependence of ntund.
pntun	0.0	Cross-term dependence of ntun.
pntund	0.0	Cross-term dependence of ntund.
vtun0	0.0 V	Voltage dependent parameter for tunneling current.
vtun0d	0.0 V	Voltage dependent parameter for tunneling current.
lvtun0	0.0	Length dependence of vtun0.
lvtun0d	0.0	Length dependence of vtun0d.
wvtun0	0.0	Width dependence of vtun0.

© 2023 Cadence Design Systems, Inc.

wvtun0d	0.0	Width dependence of vtun0d.
pvtun0	0.0	Cross-term dependence of vtun0.
pvtun0d	0.0	Cross-term dependence of vtun0d.
vrec0	0.0 V	Voltage dependent parameter for recombination current.
vrec0d	0.0 V	Voltage dependent parameter for recombination current.
lvrec0	0.0	Length dependence of vrec0.
lvrec0d	0.0	Length dependence of vrec0d.
wvrec0	0.0	Width dependence of vrec0.
wvrec0d	0.0	Width dependence of vrec0d.
pvrec0	0.0	Cross-term dependence of vrec0.
pvrec0d	0.0	Cross-term dependence of vrec0d.
xrcrg1	12.0	1st fitting parameter the bias-dependent Rg .
xrcrg2	1.0	2nd fitting parameter the bias-dependent Rg .
ef	1.0	Flicker noise frequency exponent.
em	4.1e7 V/m	Saturation field.
noia	6.250e40 s^(1-EF)/(eV)^1/m^3	Flicker noise parameter A.

© 2023 Cadence Design Systems, Inc.

noib	3.125e25 s^(1-EF)/(eV)^1/m	Flicker noise parameter B.
noic	8.750e8 s^(1-EF) m/(eV)^1	Flicker noise parameter C.
lintnoi	0.0 m	Length reduction parameter offset.
noia1	0.0	Flicker noise fitting parameter in strong inversion.
noiax	1.0	Flicker noise fitting parameter in strong inversion for high VDS.
ntnoi	1.0	Noise factor for short-channel devices for TNOIMOD = 0 only.
rnoia	0.577	Noise parameter for TNOIMOD = 1.
rnoib	0.5164	Noise parameter for TNOIMOD = 1.
rnoic	0.395	Noise parameter for TNOIMOD = 1.
tnoia	1.5	Noise parameter for TNOIMOD = 1.
tnoib	3.5	Noise parameter for TNOIMOD = 1.
tnoic	0.0	Noise correlation coefficient for TNOIMOD = 1.
binunit	1	Unit of L and W for Binning, 1: micro-meter, 0: default.
dlbin	0.0	Length reduction parameter for binning.
dwbin	0.0	Width reduction parameter for binning.

© 2023 Cadence Design Systems, Inc.

tnom	27.0 degC	Temperature at which the model was extracted.
tbgasub	4.73e-4 eV/K	Bandgap temperature coefficient.
tbgbsub	636.0 K	Bandgap temperature coefficient.
tnfactor	0.0	Temperature exponent for NFACTOR.
ute	(-1.5)	Mobility temperature exponent.
lute	0.0 m	Length dependence of UTE.
wute	0.0 m	Width dependence of UTE.
pute	0.0 m^2	Area dependence of UTE.
utel	0.0 m	Length scaling parameter for UTE.
ua1	1.0e-3 m/V	Temperature coefficient for UA.
lua1	0.0 m^2/V	Length dependence of UA1.
wua1	0.0 m^2/V	Width dependence of UA1.
pua1	0.0 m^3/V	Area dependence of UA1.
ua1l	0.0 m	Length scaling parameter for UA1.
uc1	0.056e-9 1.0/K	Temperature coefficient for UC.
luc1	0.0 m/K	Length dependence of UC1.
wuc1	0.0 m/K	Width dependence of UC1.
puc1	0.0 m^2/K	Area dependence of UC1.

© 2023 Cadence Design Systems, Inc.

ud1	0.0 $1/m^2$	Temperature coefficient for UD.
lud1	0.0 1/m	Length dependence of UD1.
wud1	0.0 1/m	Width dependence of UD1.
pud1	0.0	Area dependence of UD1.
ud1l	0.0 m	Length scaling parameter for UD1.
eu1	0.0	Temperature coefficient for EU.
leu1	0.0 m	Length dependence of EU1.
weu1	0.0 m	Width dependence of EU1.
peu1	0.0 m^2	Area dependence of EU1.
ucste	(-4.775e-3)	Temperature coefficient for UCS.
lucste	0.0 m	Length dependence of UCSTE.
wucste	0.0 m	Width dependence of UCSTE.
pucste	0.0 m^2	Area dependence of UCSTE.
teta0	0.0	Temperature coefficient for ETA0.
prt	0.0	Temperature coefficient for resistance.
lprt	0.0 m	Length dependence of PRT.
wprt	0.0 m	Width dependence of PRT.
pprt	0.0 m^2	Area dependence of PRT.

© 2023 Cadence Design Systems, Inc.

at	(-1.56e-3) m/s	Temperature coefficient for saturation velocity.
lat	0.0 m^2/s	Length dependence of AT.
wat	0.0 m^2/s	Width dependence of AT.
pat	0.0 m^3/s	Area dependence of AT.
atl	0.0 m	Length Scaling parameter for AT.
tdelta	0.0 1/K	Temperature coefficient for DELTA.
ptwgt	0.0 1/K	Temperature coefficient for PTWG.
lptwgt	0.0 m/K	Length dependence of PTWGT.
wptwgt	0.0 m/K	Width dependence of PTWGT.
pptwgt	0.0 m^2/K	Area dependence of PTWGT.
ptwgtl	0.0 m	Length sacaling parameter for PTWGT.
kt1	(-0.11) V	Temperature coefficient for Vth.
kt1exp	1.0	Temperature coefficient for Vth.
kt11	0.0 V m	Temperature coefficient for Vth.
lkt1	0.0 V m	Length dependence of KT1.
wkt1	0.0 V m	Width dependence of KT1.
pkt1	0.0 V m^2	Area dependence of KT1.
kt2	0.022	Temperature coefficient for Vth.

© 2023 Cadence Design Systems, Inc.

lkt2	0.0 m	Length dependence of KT2.
wkt2	0.0 m	Width dependence of KT2.
pkt2	0.0 m^2	Area dependence of KT2.
iit	0.0	Temperature coefficient for BETA0.
liit	0.0 m	Length dependence of IIT.
wiit	0.0 m	Width dependence of IIT.
piit	0.0 m^2	Area dependence of IIT.
igt	2.5	Gate current temperature dependence.
ligt	0.0 m	Length dependence of IGT.
wigt	0.0 m	Width dependence of IGT.
pigt	0.0 m^2	Area dependence of IGT.
tcj	0.0 1/K	Temperature coefficient for CJS/CJD.
tcjsw	0.0 1/K	Temperature coefficient for CJSWS/CJSWD.
tcjswg	0.0 1/K	Temperature coefficient for CJSWGS/CJSWGD.
tpb	0.0 V/K	Temperature coefficient for PBS/PBD.
tpbsw	0.0 V/K	Temperature coefficient for PBSWS/PBSWD.
tpbswg	0.0 V/K	Temperature coefficient for PBSWGS/PBSWGD.
rth0	0.0 m K/W	Thermal resistance.

© 2023 Cadence Design Systems, Inc.

cth0	1.0e-5 s W/(m K)	Thermal capacitance.
wth0	0.0 m	Width dependence coefficient for Rth and Cth.
saref	1.0e-6 m	Reference distance between OD edge from Poly from one side.
sbref	1.0e-6 m	Reference distance between OD edge from Poly from other side.
wlod	0.0 m	Width parameter for stress effect.
ku0	0.0 m	Mobility degradation/enhancement parameter for stress effect.
kvsat	0.0 m	Saturation velocity degradation/enhancement parameter for stress effect.
tku0	0.0	Temperature coefficient for KU0.
lku0	0.0 m^LLODKU0	Length dependence of KU0.
wku0	0.0 m^WLODKU0	Width dependence of KU0.
pku0	0.0 m^(LLODKU0+WLODKU0)	Cross-term dependence of KU0.
llodku0	0.0	Length parameter for U0 stress effect.
wlodku0	0.0	Width parameter for U0 stress effect.
kvth0	0.0 V m	Threshold shift parameter for stress effect.

© 2023 Cadence Design Systems, Inc.

lkvth0	0.0 m^LLODKU0	Length dependence of KVTH0.
wkvth0	0.0 m^WLODKU0	Width dependence of KVTH0.
pkvth0	0.0 m^(LLODKU0+WLODKU0)	Cross-term dependence of KVTH0.
llodvth	0.0	Length parameter for Vth stress effect.
wlodvth	0.0	Width parameter for Vth stress effect.
stk2	0.0 m	K2 shift factor related to Vth change.
lodk2	0.0	K2 shift modification factor for stress effect.
steta0	0.0 m	ETA0 shift related to Vth0 change.
lodeta0	0.0	ETA0 modification factor for stress effect.
web	0.0	Coefficient for SCB (> 0).
wec	0.0	Coefficient for SCC (> 0).
kvth0we	0.0	Threshold shift factor for well proximity effect.
lkvth0we	0.0 m	Length dependence of KVTH0WE.
wkvth0we	0.0 m	Width dependence of KVTH0WE.
pkvth0we	0.0 m^2	Area dependence of KVTH0WE.
k2we	0.0	K2 shift factor for well proximity effect.

© 2023 Cadence Design Systems, Inc.

lk2we	0.0 m	Length dependence of K2WE.
wk2we	0.0 m	Width dependence of K2WE.
pk2we	0.0 m^2	Area dependence of K2WE.
ku0we	0.0	Mobility degradation factor for well proximity effect.
lku0we	0.0 m	Length dependence of KU0WE.
wku0we	0.0 m	Width dependence of KU0WE.
pku0we	0.0 m^2	Area dependence of KU0WE.
scref	1.0e-6 m	Reference distance to calculate SCA,SCB and SCC (< 0).
ssl0	4.0e2 A/m	Temperature- and doping-independent parameter for sub-surface leakage drain current.
ssl1	3.36e8 1/m	Temperature- and doping-independent parameter for gate length for sub-surface leakage drain current.
ssl2	0.185	Fitting parameter for sub-surface leakage drain current: barrier height.
ssl3	0.3 V	Fitting parameter for sub-surface leakage drain current: gate voltage effect.
ssl4	1.4 1/V	Fitting parameter for sub-surface leakage drain current: gate voltage effect.
ssl5	0 1/V	Fitting parameter for sub-surface leakage drain current: gate voltage effect.
sslexp1	0.490	Fitting exponent for SSL doping effect.
sslexp2	1.42	Fitting exponent for SSL temperature.

© 2023 Cadence Design Systems, Inc.

avdsx	20.0	Smoothing parameter in Vdsx in Vbsx.
wedge	10.0e-9 m	Edge FET width.
dgammaedge	0.0	Different in body-bias coefficient between Edge-FET and Main-FET.
dgammaedgel	0.0	L dependence parameter for DGAMMA.
dgammaedgelexp	1.0	Exponent of L dependence parameter for DGAMMA.
dvtedge	0.0	Vth shift for Edge FET.
ndepedge	1e24 $1/m^3$	Channel doping concentration for EDGEFET.
lndepedge	0.0 $1/m^2$	Length dependence of NDEPEDGE.
wndepedge	0.0 $1/m^2$	Width dependence of NDEPEDGE.
pndepedge	0.0 1/m	Area dependence of NDEPEDGE.
nfactoredge	0.0	NFACTOR for Edge FET.
lnfactoredge	0.0 m	Length dependence of NFACTOREDGE.
wnfactoredge	0.0 m	Width dependence of NFACTOREDGE.
pnfactoredge	0.0 m^2	Area dependence of NFACTOREDGE.
citedge	0.0 F/m^2	CIT for Edge FET.
lcitedge	0.0 F/m	Length dependence of CITEDGE.
wcitedge	0.0 F/m	Width dependence of CITEDGE.
pcitedge	0.0 F	Area dependence of CITEDGE.

© 2023 Cadence Design Systems, Inc.

cdscdedge	1e-9 F/m^2/V	CDSCD for edge FET.
lcdscdedge	0.0 F/m/V	Length dependence of CDSCDEDGE.
wcdscdedge	0.0 F/m/V	Width dependence of CDSCDEDGE.
pcdscdedge	0.0 F/V	Area dependence of CDSCDEDGE.
cdscbedge	0.0 F/m^2/V	CDSCB for edge FET.
lcdscbedge	0.0 F/m/V	Length dependence of CDSCBEDGE.
wcdscbedge	0.0 F/m/V	Width dependence of CDSCBEDGE.
pcdscbedge	0.0 F/V	Area dependence of CDSCBEDGE.
eta0edge	0.08	DIBL parameter for edge FET.
leta0edge	0.0 m	Length dependence of ETA0EDGE.
weta0edge	0.0 m	Width dependence of ETA0EDGE.
peta0edge	0.0 m^2	Area dependence of ETA0EDGE.
etabedge	(-0.07) 1/V	ETAB for edge FET.
letabedge	0.0 m/V	Length dependence of ETABEDGE.
wetabedge	0.0 m/V	Width dependence of ETABEDGE.
petabedge	0.0 m^2/V	Area dependence of ETABEDGE.

© 2023 Cadence Design Systems, Inc.

kt1edge	(-0.11) V	Temperature dependence parameter of threshold voltage for edge FET.
lkt1edge	0.0 V m	Length dependence of KT1EDGE.
wkt1edge	0.0 V m	Width dependence of KT1EDGE.
pkt1edge	0.0 V m^2	Area dependence of KT1EDGE.
kt1ledge	0.0 V m	Temperature dependence parameter of threshold voltage for edge FET.
lkt1ledge	0.0 V m^2	Length dependence of KT1LEDGE.
wkt1ledge	0.0 V m^2	Width dependence of KT1LEDGE.
pkt1ledge	0.0 V m^3	Area dependence of KT1LEDGE.
kt2edge	0.022	Temperature dependence parameter of threshold voltage for edge FET.
lkt2edge	0.0 m	Length dependence of KT2EDGE.
wkt2edge	0.0 m	Width dependence of KT2EDGE.
pkt2edge	0.0 m^2	Area dependence of KT2EDGE.
kt1expedge	1.0	Temperature dependence parameter of threshold voltage for edge device.
lkt1expedge	0.0 m	Length dependence of KT1EXPEDGE.
wkt1expedge	0.0 m	Width dependence of KT1EXPEDGE.
pkt1expedge	0.0 m^2	Area dependence of KT1EXPEDGE.
tnfactoredge	0.0	Temperature dependence parameter of subthreshold slope factor for edge.

© 2023 Cadence Design Systems, Inc.

ltnfactoredge	0.0 m	Length dependence of TNFACTOREDGE.
wtnfactoredge	0.0 m	Width dependence of TNFACTOREDGE.
ptnfactoredge	0.0 m^2	Area dependence of TNFACTOREDGE.
teta0edge	0.0	Temperature dependence parameter of DIBL parameter for edge FET.
lteta0edge	0.0 m	Length dependence of TETA0EDGE.
wteta0edge	0.0 m	Width dependence of TETA0EDGE.
pteta0edge	0.0 m^2	Area dependence of TETA0EDGE.
dvt0edge	2.2	First coefficient of SCE effect on Vth for Edge FET.
dvt1edge	0.53	Second coefficient of SCE effect on Vth for Edge FET.
dvt2edge	0.0 1/V	Body-bias coefficient for SCE effect for Edge FET.
k2edge	0.0 V	Vth shift due to Vertical Non-uniform doping.
lk2edge	0.0 m	Length dependence of K2EDGE.
wk2edge	0.0 m	Width dependence of K2EDGE.
pk2edge	0.0 m^2	Area dependence of K2EDGE.
kvth0edge	0.0 V m	Threshold Shift parameter for stress effect.
lkvth0edge	0.0 m^LLODKU0	Length dependence of KVTH0EDGE.
wkvth0edge	0.0 m^WLODKU0	Width dependence of KVTH0EDGE.

© 2023 Cadence Design Systems, Inc.

pkvth0edge	0.0 m^(LLODKU0+WLODKU0)	Area dependence of KVTH0EDGE.
kvth0edgewe	0.0	Threshold Shift parameter due to Well proximity in EDGEFET.
lkvth0edgewe	0.0	Length dependence of KVTHOWEEDGE.
wkvth0edgewe	0.0	Width dependence of KVTHOWEEDGE.
pkvth0edgewe	0.0	Area dependence of KVTHOWEEDGE.
k2edgewe	0.0	Vth shift due to Vertical Non-uniform doping due to Well proximity in EDGEFET.
lk2edgewe	0.0	Length dependence of K2WEEDGE.
wk2edgewe	0.0	Width dependence of K2WEEDGE.
pk2edgewe	0.0	Area dependence of K2WEEDGE.
stk2edge	0.0 m	K2 shift factor related to Vth change.
lstk2edge	0.0 m^2	Length dependence of STK2EDGE.
wstk2edge	0.0 m^2	Width dependence of STK2EDGE.
pstk2edge	0.0 m^3	Area dependence of STK2EDGE.
steta0edge	0.0 m	ETA0 shift related to Vth0 change.
lsteta0edge	0.0 m^2	Length dependence of STETA0EDGE.
wsteta0edge	0.0 m^2	Width dependence of STETA0EDGE.
psteta0edge	0.0 m^3	Area dependence of STETA0EDGE.

© 2023 Cadence Design Systems, Inc.

igclamp	1	Model flag for Ig clamping.
lp	1.0e-5 m	Length scaling parameter for thermal noise.
rnoik	0.0	Exponential coefficient for enhanced correlated thermal noise.
tnoik	0.0 1/m	Empirical parameter for Leff trend of Sid at low Ids.
tnoik2	0.1 1/m	Empirical parameter for sensitivity of RNOIK.
k0	0.0	Non-saturation effect parameter for strong inversion region.
lk0	0.0 m	Length dependence of K0.
wk0	0.0 m	Width dependence of K0.
pk0	0.0 m^2	Area dependence of K0.
k01	0.0 1/K	Temperature coefficient for K0.
lk01	0.0 m/K	Length dependence of K0.
wk01	0.0 m/K	Width dependence of K0.
pk01	0.0 m^2/K	Area dependence of K0.
m0	1.0	offset of non-saturation effect parameter for strong inversion region.
lm0	0.0 m	Length dependence of M0.
wm0	0.0 m	Width dependence of M0.
pm0	0.0 m^2	Area dependence of M0.
m01	0.0 1/K	Temperature coefficient for M0.

© 2023 Cadence Design Systems, Inc.

lm01	0.0 m/K	Length dependence of M01.
wm01	0.0 m/K	Width dependence of M01.
pm01	0.0 m^2/K	Area dependence of M01.
nedge	1	Flicker noise parameter for edge fet transistor.
noia1_edge	0.0	Flicker noise fitting parameter in strong inversion for edge fet transistor.
noiax_edge	1.0	Flicker noise fitting parameter in strong inversion for edge fet transistor.
fnoimod	0	Flicker noise model selector.
lh	1.0e-8 m	Length of halo transistor.
noia2	6.250e40 s^(1-EF)/(eV)^1/m^3	Flicker noise parameter A for Halo.
hndep	1e24 1/m^3	Halo doping concentration for I-V.
c0	0.0 V	Lateral NUD1 voltage parameter.
lc0	0.0 V m	Length dependence of C0.
wc0	0.0 V m	Width dependence of C0.
pc0	0.0 V m^2	Area dependence of C0.
c01	0.0 1/K	Temperature dependence of lateral NUD1 voltage parameter.
lc01	0.0 m/K	Length dependence of C01.

© 2023 Cadence Design Systems, Inc.

wc01	0.0 m/K	Width dependence of C01.
pc01	0.0 m^2/K	Area dependence of C01.
c0si	1.0 V	Correction factor for strong inversion used in Mnud1. After binning it should be within (0 : inf).
lc0si	0.0 V m	Length dependence of C0SI.
wc0si	0.0 V m	Width dependence of C0SI.
pc0si	0.0 V m^2	Area dependence of C0SI.
c0si1	0.0 1/K	Temperature dependence of C0SI1.
lc0si1	0.0 m/K	Length dependence of C0SI1.
wc0si1	0.0 m/K	Width dependence of C0SI1.
pc0si1	0.0 m^2/K	Area dependence of C0SI1.
c0sisat	0.0 V	Correction factor for strong inversion used in Mnud1.
lc0sisat	0.0 V m	Length dependence of C0SISAT.
wc0sisat	0.0 V m	Width dependence of C0SISAT.
pc0sisat	0.0 V m^2	Area dependence of C0SISAT.
c0sisat1	0.0 1/K	Temperature dependence of C0SISAT1.
lc0sisat1	0.0 m/K	Length dependence of C0SISAT1.
wc0sisat1	0.0 m/K	Width dependence of C0SISAT1.
pc0sisat1	0.0 m^2/K	Area dependence of C0SISAT1.

© 2023 Cadence Design Systems, Inc.

minr	0.001 Ω	minr is the value below which the simulator expects elimination of source/drain resistance and it will improve simulation efficiency without significantly altering the results..
abulk	1.0	For flexibility of tuning Cgg in strong inversion.
a0	0.0	Coefficient of depletion width dependence in AbulkIV for Id-Vd flexibility.
ags	0.0	Coefficient of Source Charge dependence in AbulkIV for Id-Vd flexibility.
ags1	1.0	qs nonlinear term for Id-Vd flexibility.
keta	0.0	Coefficient of back-bias dependence in AbulkIV for Id-Vd flexibility.
a0cv	0.0	Coefficient of depletion width dependence in AbulkCV for Capacitance flexibility.
agscv	0.0	Coefficient of Source Charge dependence in AbulkCV for Capacitance flexibility.
ketacv	0.0	Coefficient of back-bias dependence in AbulkCV for Capacitance flexibility.
rbody	0.0 ohm/ square	Intrinsic body contact sheet resistance.
rbsh	0.0 ohm/ square	Extrinsic body contact sheet resistance.
rhalo	1e15 ohm/m	body halo sheet resistance.
ub	67.0e-3 $m^2/V/s$	Mobility of majority carriers in body..

© 2023 Cadence Design Systems, Inc.

lub	0.0 $m^3/V/s$	Length dependence of UB.
wub	0.0 $m^3/V/s$	Width dependence of UB.
pub	0.0 $m^4/V/s$	Area dependence of UB.
ubte	1.0	Mobility temperature exponent.
lubte	0.0 m	Length dependence of UBTE.
wubte	0.0 m	Width dependence of UBTE.
pubte	0.0 m^2	Area dependence of UBTE.
neff	5e24 $1/m^3$	Effective substrate doping.
lneff	0.0 $1/m^2$	Length dependence of NEFF.
wneff	0.0 $1/m^2$	Width dependence of NEFF.
pneff	0.0 1/m	Area dependence of NEFF.
dwbc	0.0 m	Width offset for body contact isolation edge.
eggbcp2	1.12 eV	Bandgap in Agbcp2 region.
nsub	6.0e16 cm^{-3}	Substrate doping concentration with polarity.
lnsub	0.0	Length dependence of nsub.
wnsub	0.0	Width dependence of nsub.
pnsub	0.0	Cross-term dependence of nsub.

© 2023 Cadence Design Systems, Inc.

fbody	1.0	Scaling factor for body charge.
kb1	1.0	Scaling factor for backgate charge.
lkb1	0.0	Length dependence of kb1.
wkb1	0.0	Width dependence of kb1.
pkb1	0.0	Cross-term dependence of kb1.
dlbg	0.0 m	Length offset fitting parameter for backgate charge.
dlcb	0.0 m	Length offset fitting parameter for body charge.
csdesw	0.0 F/m	Source/drain sidewall fringing capacitance per unit length.
csdmin	0.0 V	Source/drain bottom diffusion minimum capacitance.
acesb	2.0	First fitting parameter for drain to bottom capacitance.
bcesb	0.0 V	Second fitting parameter for drain to bottom capacitance.
acedb	2.0	First fitting parameter for drain to bottom capacitance.
bcedb	0.0 V	Second fitting parameter for drain to bottom capacitance.
lmin	0.0 m	Minimum channel length for which the model is valid.
lmax	1.0 m	Maximum channel length for which the model is valid.
wmin	0.0 m	Minimum channel width for which the model is valid.

© 2023 Cadence Design Systems, Inc.

wmax	1.0 m	Maximum channel width for which the model is valid.
l	1.0e-5 m	NULL.
w	1.0e-5 m	
nf	1	

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

47

BSIM-IMG

BSIM-IMG is a SPICE compact model for modeling the electrical characteristics of common gate MG structures, developed by UC Berkeley. The latest version is 102.80.

The BSIM-IMG models the independent double-gate structure as a four terminal device, containing the source(s), drain(d), front gate(fg), and back gate(bg) terminals. The two gates (fg, bg) are allowed to have different workfunctions ($\Delta\varphi 1, \Delta\varphi 2$) and dielectric thicknesses (T_{ox1}, T_{ox2}). They can also be biased separately at different voltages.

This chapter contains the following information about the BSIM-IMG model:

- Model Overview on page 3151
- BSIM-IMG Model Equations on page 3152
  - Bias Independent Calculations on page 3152
  - Terminal Voltages and Pre-Conditioning on page 3155
  - Short Channel Effects on page 3156
  - Body Doping Effects on page 3157
  - Surface Potential Calculation on page 3157
  - Drain Saturation Voltage on page 3159
  - Calculate Average Field, Potential, and Charge on page 3162
  - Mobility Degradation on page 3163
  - Output Conductance on page 3164
  - Veolocity Saturation on page 3165
  - Drain Current Model on page 3165
  - C-V Model on page 3166
  - Parasitic Resistance and Capacitance Models on page 3166

© 2023 Cadence Design Systems, Inc.

- Impact Ionization and GIDL/GISL Model on page 3169
- Gate-Induced-Drain/Source-Leakage Current on page 3170
- Gate Tunneling Current on page 3171
- Self Heating Model on page 3172

■ Model Version Update on page 3176

■ Component Statements on page 3178

© 2023 Cadence Design Systems, Inc.

Model Overview

Physical surface-potential-based formulations are derived in both intrinsic and extrinsic models of BSIM-IMG. Surface potentials and integrated charge densities at the source and drain ends are obtained by solving the Poisson's equation in a fully-depleted, lightly doped body and calculating with efficient analytical approximations. Since the surface potential equation is derived based on Poisson's equation, the model captures volume inversion effects adequately and shows excellent scalability compared with 2D device simulation.

To meet the requirements of future devices, new parameters have been included to model devices consisting of novel materials. This includes parameters for non-silicon channel devices and High-K gate insulators.

The back-gate of a planar double-gate SOI FET is often used for tuning device threshold voltage (V_{TH}). Therefore, the effect of back-gate on V_{TH} must also be addressed by the model. V_{TH} varies with back-gate voltage. When V_{bg} is low, they follow a linear relationship. At large V_{bg}, however, the back-gate effect slows down as a result of back surface accumulation.

Other important effects, such as short channel effects, mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance are also incorporated in the model.

The model is continuous and symmetric at `Vds=0`. This physics-based model is scalable and predictive over a wide range of device parameters.

© 2023 Cadence Design Systems, Inc.

BSIM-IMG Model Equations

Bias Independent Calculations

Physical Constants

Physical quantities in BSIM-IMG are in M.K.S units, unless specified otherwise.

$$q = 1.6 \times 10^{-19}$$

$$\varepsilon_0 = 8.8542 \times 10^{-12}$$

$$k = 1.3787 \times 10^{-23}$$

$$\varepsilon_{si} = EPSRSUB \cdot \varepsilon_0$$

$$\varepsilon_{ox1} = EPSROX1 \cdot \varepsilon_0$$

$$\varepsilon_{ox2} = EPSROX2 \cdot \varepsilon_0$$

$$C_{ox1} = \frac{39 \cdot \varepsilon_0}{EOT1}$$

$$C_{ox2} = \frac{39 \cdot \varepsilon_0}{EOT2}$$

$$C_{si} = \frac{\varepsilon_{si}}{TSI}$$

$$\varepsilon_{ratio} = \frac{EPSRSUB}{3.9}$$

$$V_{tm} = \frac{kT}{q}$$

© 2023 Cadence Design Systems, Inc.

$$V_{gfb2n} = -1.2$$

Effective Channel Width, Channel Length

$$Lnew = L + XL$$

$$L_{LLN} = Lnew^{-LLN}$$

$$L_{WLN} = Lnew^{-WLN}$$

$$LW_{LLN-LWN} = L_{LLN} \cdot L_{LWN}$$

$$\Delta LIV = LINT + LL \cdot L_{LLN} + LW \cdot L_{LWN} + LWL \cdot LW_{L_{LLN-LWN}}$$

$$L_{eff} = Lnew - 2.0 \cdot \Delta LIV$$

$$\Delta LCV = DLC + LLC \cdot L_{LLN} + LWC \cdot L_{LWN} + LWLC \cdot LW_{L_{LLN-LWN}}$$

$$L_{eff,\,CV} = Lnew - 2.0 \cdot \Delta LCV$$

$$Wnew = \begin{cases} \frac{W}{NF} & NFMOD = 0 \\ W & NFMOD = 1 \end{cases}$$

$$Wnew = W + XW$$

$$W_{LWN} = W_{new}^{-LWN}$$

$$W_{WWN} = W_{new}^{-WWN}$$

$$LW_{WLN-WWN} = L_{WLN} \cdot W_{WWN}$$

© 2023 Cadence Design Systems, Inc.

$$\Delta WIV = WINT + WL \cdot L_{WLN} + WW \cdot W_{WWN} + WWL \cdot LW_{L_{WLN-WWN}}$$

$$W_{eff} = Wnew - 2.0 \cdot \Delta WIV$$

$$\Delta WCV = DWC + WLC \cdot L_{WLN} + WWC \cdot L_{WWN} + WWLC \cdot LW_{L_{WLN-WWN}}$$

$$W_{eff,\,CV} = Wnew - 2.0 \cdot \Delta WCV$$

Binning Calculations

$$PARAM_i = PARAM + \frac{1}{L_{eff}} \cdot LPARAM + \frac{1}{W_{eff}} \cdot WPARAM + \frac{1}{L_{eff} \cdot W_{eff}} \cdot PPARAM$$

Front and Back Gate Workfunction Calculation

$$\Phi_{ref} = \begin{cases} EASUB & for \quad NMOS \\ EASUB + E_g & for \quad PMOS \end{cases}$$

$$\Delta\Phi_1 = devsign \cdot (PHIG1_i - \Phi_{ref})$$

$$\Delta\Phi_2 = devsign \cdot (PHIG2_i - \Phi_{ref})$$

$$\Phi_{sd} = EASUB + \frac{E_g}{2} - devsign \cdot min[\frac{E_g}{2}, \frac{kT}{q} \cdot In\left(\frac{NSD}{ni}\right)]$$

$$V_{fbsd} = devsign \cdot (PHIG1_i - \Phi_{sd})$$

© 2023 Cadence Design Systems, Inc.

Terminal Voltages and Pre-Conditioning

Terminal Voltages and V_{dsx} Calculation

$$V_{fgs} = V_{fg} - V_s$$

$$V_{fgd} = V_{fg} - V_d$$

$$V_{bgs} = V_{bg} - V_s$$

$$V_{bgd} = V_{bg} - V_d$$

$$V_{ds} = V_d - V_s$$

$$V_{gfb1} = V_{fgs} - \Delta\Phi 1$$

$$V_{gfb2} = V_{bgs} - \Delta\Phi 2$$

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.0004} - 0.02$$

© 2023 Cadence Design Systems, Inc.

Back Gate Biasing Effect

$$Kvbg = KBG0 - \frac{0.5 \cdot KBG1}{\cosh\left(DBG \cdot \frac{Leff}{\lambda}\right)}$$

$$K^{*}_{vbg} = KBG2 + \frac{1}{2}\left[K_{vbg} - KBG2 + \sqrt{(K_{vbg} - KBG2)^2 + 0.0001}\right]$$

$$V_{gfb2eff} = V_{gfb2n} - symmetryfactor$$

$$\gamma_0 = -\frac{C_{ox2} \cdot C_{si}}{(C_{ox2} + C_{si}) \cdot C_{ox1}}$$

$$\Delta V_{th,\,vbg} = \gamma_0 \cdot K^{*}_{vbg} \cdot (V_{gfb2} - V_{gfb2eff})$$

Short Channel Effects

Vt Roll-off

$$\Delta V_{th,SCE} = -\frac{0.5 \cdot DVT0_i}{\cosh\left(DVT1 \cdot \frac{Leff}{\lambda}\right) - 1} \cdot (V_{bi} - \Phi_{st})$$

Drain Induced Barrier Lowering (DIBL)

$$\Delta V_{th,DIBL} = -\frac{0.5 \cdot ETA0_i}{\cosh\left(DSUB \cdot \frac{Leff}{\lambda}\right) - 1} \cdot V_{dsx}$$

© 2023 Cadence Design Systems, Inc.

Vt Roll on/off at moderate channel lengths

$$V_{th,RSCE} = K1RSCE\left[\sqrt{1+\frac{LPE0}{Leff}}-1\right]\cdot\sqrt{\Psi_{st}}$$

Vt Roll on/off at moderate channel lengths and high V_{ds}

$$\Delta V_{th,DSC} = -\frac{DSC0}{DSC1+L_{eff}}\cdot V_{dsx}$$

Body Doping Effects

Body Doping Effect

$$\Delta V_{TH,NBODY} = -\frac{q\cdot NBODY\cdot TS1}{C_{ox1}}\left[1-\frac{0.5\cdot TSI}{TSI+\varepsilon_{ratio}\cdot EOT2}\right]$$

Surface Potential Calculation

Surface Potential is computed solving the Poisson's equation in silicon body:

$$E_{S1}^{\ 2}-E_{S2}^{\ 2} = \frac{2N_{DOS}kT}{\varepsilon_{Si}}\left(e^{\frac{\Psi_{S1}-V_{ch}}{\nu_{tm}}}-e^{\frac{\Psi_{S2}-V_{ch}}{\nu_{tm}}}\right)$$

where

$$E_{S1} = \frac{C_{ox1}(V_{gfb1eff}-\Psi_{S1})}{\varepsilon_{Si}}$$

$$E_{S2} = \frac{C_{ox2}(V_{gfb2eff}-\Psi_{S2})}{\varepsilon_{Si}}$$

and

© 2023 Cadence Design Systems, Inc.

$$V_{gfb1eff} = V_{gfb1} - \Delta V_{th,all}$$
$$V_{gfb2eff} = V_{gfb2n}$$

The first equation above is simplified, replacing `vtm` by `nvtm` and neglecting the second exponential term on right side. Further approximating Ψ s2 to be

$$\Psi_{S2} = \frac{C_{Si}}{C_{Si}+C_{ox2}}\Psi_{S1} + \frac{C_{ox2}}{C_{Si}+C_{ox2}}V_{gfb2eff}$$

The simplified Poisson's equation obtained is:

$$\left(C_{ox1}\frac{V_{gfb1eff}-\psi_{s1}}{\epsilon_{Si}}\right)^2 - \left(\frac{V_{gfb2eff}-\psi_{s1}}{TSI+\frac{\epsilon_{si}}{\epsilon_{ox}}EOT2}\right)^2 = \frac{2N_{DOS}kT}{\epsilon_{Si}}\left(e^{\frac{\psi_{s1}-V_{ch}}{nv_{tm}}}\right)$$

This can rewritten as:

$$f(x) \equiv \left(\frac{\nu_{gfb1}-x}{G}\right)^2 - B_{sq}\left(\nu_{gfb2}-x\right)^2 - e^{(x-\nu_{ch})} = 0$$

where

$$\nu_{gfb1} = \frac{V_{gfb1eff}}{nv_{tm}}$$
$$\nu_{gfb2} = \frac{V_{gfb2eff}}{nv_{tm}}$$
$$\nu_{ch} = \frac{V_{ch}}{nv_{tm}}$$
$$x = \frac{\psi_{s1}}{nv_{tm}}$$
$$G = \frac{EOT1}{\epsilon_{ox}}\sqrt{\frac{2qN_{DOS}\epsilon_{si}}{nv_{tm}}}$$
$$B_{sq} = \left(\frac{1}{TSI}+\frac{\epsilon_{si}}{\epsilon_{ox}}EOT2\sqrt{\frac{\epsilon_{si}nv_{tm}}{2qN_C}}\right)^2$$

© 2023 Cadence Design Systems, Inc.

Solving the above equation using an iterative Halley's algorithm for a maximum of four iterations stopping when the error in surface potential solution is below 1 nV. Halley's algorithm is a second order Householder's method and can be written as:

$$x_{n+1} = x_n - \frac{2f(x)f'(x)}{2[f'(x)]^2 - f(x)f''(x)}$$

Simplifying the first equation assuming the back-gate to remain always in weak inversion, reducing it to become a function of only the front-gate parameters:

$$\left(C_{ox1}\frac{V_{gfb1eff} - \psi^0_{s1}}{\epsilon_{Si}}\right)^2 = \frac{2N_{DOS}kT}{\epsilon_{Si}}\left(e^{\frac{\psi^0_{s1} - V_{ch}}{nv_{tm}}}\right)$$

The above equation is solved using two iterations of Halley's algorithm and can be written as:

$$\tilde{\psi}^0_{s1} = \begin{cases} V_{gfb1eff} \\ min\left[V_{gfb1eff}, \left(V_{ch} + 2nv_{tm}\ln[\frac{V_{gfb1eff}C_{ox1}}{\sqrt{2qN_c n v_{tm}\epsilon_{si}}}]\right)\right] \end{cases}$$

Once x satisfying is known, Ψ s1 is obtained from x using:

$$\Psi_{s1} = x \cdot nv_{tm}$$

The equation is solved once at the source side, with `Vch = 0`, and once at drain side, with `Vch = Vds`, to obtain the surface potentials at the two ends of the channel.

Drain Saturation Voltage

The drain saturation voltage model is calculated after the source-side surface po-tential (φ_s) has been calculated. Vdseff is subsequently used to compute the drain-sidesurface potential (φ_d).

© 2023 Cadence Design Systems, Inc.

Electric Field Calculations

$$q_{is} = \frac{Q_{tots}}{C_{ox1}}$$

$$q_{bs} = \frac{q \cdot NBODY \cdot TSI}{C_{ox1}}$$

$$T_2 = \eta_\mu q_{is} + q_{bs} + E_{bs} \cdot \frac{\varepsilon_{si}}{C_{ox1}}$$

$$T_3 = \frac{1}{2}\left(T_2 + \sqrt{T_2^{\,2} + 0.001}\right)$$

$$E_{effs} = 10^{-8} \cdot \frac{C_{ox1}}{\varepsilon_{si}} \cdot T_3$$

Calculate the Drain Saturation Voltage

$$D_{mobs} = 1 + (UA(T) + UC(T) \cdot V_{bgs}) \cdot (E_{effs})^{EU} + \frac{UD(T)}{\left(\frac{1}{2}\left(1 + \frac{q_{is}}{q_{ia,\,th}}\right)\right)^{UCS(T)}}$$

$$E_{sat} = \frac{2 \cdot VSAT}{\mu_o D_{mobs}}$$

If D_{rs}=0, then

$$V_{dsat} = \frac{E_{sat}L_{eff} \cdot \left(\frac{Q_{tots}}{C_{ox1} + C_{ox2}}\right)}{E_{sat}L_{eff} + \frac{Q_{tots}}{C_{ox1} + C_{ox2}}}$$

© 2023 Cadence Design Systems, Inc.

If D_{rs} is not equal to 0, then

$$T6 = KSATIV \cdot \left(\frac{Q_{tots}}{C_{ox1} + C_{ox2}} + 2V_t \right)$$

$$a = 2W \cdot V_{SAT} \cdot C_{ox1} \cdot G_{rs}$$

$$b = T_6 + E_{sat} L_{eff} + 3T_6 W_{eff} \cdot V_{SAT} \cdot C_{ox1} \cdot G_{rs}$$

$$c = T_6 \cdot [E_{sat} L_{eff} + T_6 \cdot a]$$

$$V_{dsat} = \frac{b - \sqrt{b^2 - 2ac}}{a}$$

© 2023 Cadence Design Systems, Inc.

Calculate Average Field, Potential, and Charge

Average Field, Potential, and Charge

$$\varphi_m = \frac{\varphi_{fs} + \varphi_{fd}}{2}$$

$$q_{ia} = \frac{Q_{tots} + Q_{totd}}{2C_{ox1}}$$

$$q_{ba} = \frac{qN_A \cdot TSI}{C_{ox1}}$$

$$E_{ba} = \frac{E_{bs} + E_{bd}}{2}$$

$$\Delta\varphi = \varphi_{fd} - \varphi_{fs}$$

$$\Delta q_i = \frac{Q_{tots} - Q_{totd}}{C_{ox1}}$$

© 2023 Cadence Design Systems, Inc.

Mobility Degradation

The mobility model is based on the BSIM4 model.

$$\eta = \begin{cases} \frac{1}{2} \cdot ETAMOB & for \quad NMOS \\ \frac{1}{2} \cdot ETAMOB & for \quad PMOS \end{cases}$$

$$T_2 = \eta_\mu q_{ia} + q_{ba} + E_{ba} \cdot \frac{\varepsilon_{si}}{C_{ox1}}$$

$$T_3 = \frac{1}{2}\left(T_2 + \sqrt{T_2^{\,2} + 0.001}\right)$$

$$E_{effm} = 10^{-8} \cdot \frac{C_{ox1}}{\varepsilon_{si}} \cdot T_3$$

$$D_{mob0} = 1 + (UA(T) + UC(T) \cdot V_{bgs}) \cdot (E_{effm})^{EU} + \frac{UD(T) + UDB \cdot V_{bgx}}{\left(\frac{1}{2}\left(1 + \frac{q_{ia}}{10^{-2}/C_{ox1}}\right)\right)^{UCS(T)}}$$

$$D_{mob} = \frac{D_{mob0}}{U0MULT}$$

© 2023 Cadence Design Systems, Inc.

Output Conductance

Channel Length Modulation

$$C_{clm} = \begin{cases} PCLM \cdot (1 + PCLMG \cdot q_{im}) & for \quad PCLMG > 0 \\ PCLM \div (1 - PCLMG \cdot q_{im}) & for \quad PCLMG < 0 \end{cases}$$

$$M_{clm} = 1 + \frac{1}{C_{clm}} ln\left[1 + \frac{V_{ds} - V_{dseff}}{VASAT}\right] \cdot C_{clm}$$

Output Conductance due to DIBL

$$PVAG_{factor} = \begin{cases} 1 + PVAG \cdot \dfrac{q_{ia}}{E_{sat} L_{eff}} & for \quad PVAG > 0 \\ \dfrac{1}{1 - PVAG \cdot \dfrac{q_{ia}}{E_{sat} L_{eff}}} & for \quad PVAG < 0 \end{cases}$$

$$\theta_{rout} = \frac{0.5 \cdot PDIBL1}{\cosh\left(DROUT \cdot \dfrac{L_{eff}}{\lambda}\right) - 1} + PDIBL2$$

$$V_{ADIBL} = \frac{q_{im} + 2kT/q}{\theta_{rout}} \cdot \left(1 - \frac{V_{dsat}}{V_{dsat} + q_{ia} + 2kT/q}\right) \cdot PVAG_{factor}$$

$$M_{oc} = \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \cdot M_{clm}$$

M_{oc} is multiplied to `Ids` in the `_nal` drain current expression.

© 2023 Cadence Design Systems, Inc.

Veolocity Saturation

Current Degradation Due to Velocity Saturation

The following formulation models the current degradation factor due to velocity saturation in the linear region. It is adopted from the BSIM5 model.

$$E_{sat1} = \frac{2 \cdot VSAT1(T)}{\mu_{eff}}$$

$$\delta_{vsat} = DELTAVSAT$$

$$T_0 = 0.8 + VSATB \cdot V_{bgx}$$

$$X_{sat} = 0.2 + \frac{\left[T_0 + \sqrt{T_0^{\,2} + 0.01}\right]}{2}$$

$$D_{vsat} = \frac{1 + \sqrt{\delta_{vsat} + \left(\frac{\Delta q_i}{E_{sat1} L_{eff}} \cdot X_{sat}\right)^2}}{1 + \sqrt{\delta_{vsat}}} + \frac{1}{2} \cdot PTWG(T) \cdot q_{ia} \cdot \Delta q_i^2$$

Drain Current Model

$$I_{ds0} = \mu_0 \cdot C_{ox1} \cdot \frac{W_{eff}}{L_{eff}} \cdot i_{ds0} \cdot \frac{M_{oc}}{D_{mob} \cdot D_r \cdot D_{vsat}}$$

© 2023 Cadence Design Systems, Inc.

C-V Model

Channel Length Modulation

$$C_{clm,\,CV} = \begin{cases} PCLMCV \cdot (1 + PCLMGCV \cdot q_{im}) & for PCLMGCV > 0 \\ \dfrac{PCLMCV}{1 - PCLMGCV \cdot q_{im}} & for PCLMGCV < 0 \end{cases}$$

$$M_{clm,\,CV} = 1 + \frac{1}{C_{clm,\,CV}} ln1 + \left[\frac{V_{ds} - V_{dseff}}{VASAT} \cdot C_{clm,\,CV}\right]$$

Assign Variables

$$Q_{fg} = \frac{1}{M_{clm,\,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot (q_{fg})$$

$$Q_{bg} = \frac{1}{M_{clm,\,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot (q_{bg})$$

$$Q_{d} = \frac{1}{M_{clm,\,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot (-q_{d1} - q_{d2})$$

Parasitic Resistance and Capacitance Models

BSIM-IMG models the parasitic source/drain resistance in two components, a bias dependent extension resistance, and a bias independent diffusion resistance.

The parasitic capacitance model in BSIM-MG includes a bias-independent outer fringe capacitance, a bias-dependent inner fringe capacitance, a bias-dependent overlap capacitance, and substrate capacitances.

© 2023 Cadence Design Systems, Inc.

Bias-dependent Extension Resistance

RDSMOD=0 (Internal)

$$R_{ds} = \frac{1}{NF \cdot W_{eff}^{WR}} \cdot \left(RDSWMIN(T) + \frac{RDSW(T)}{1 + PRWG_i \cdot q_{ia}} \right)$$

RDSMOD=1 (External)

$$R_{source} = \frac{1}{W_{eff0}^{WR} \cdot NF} \cdot \left(RSWMIN(T) + \frac{RSW(T)}{1 + PRWG_i \cdot V_{gs,\,eff}} \right) + R_{s,\,geo}$$

$$R_{drain} = \frac{1}{W_{eff0}^{WR} \cdot NF} \cdot \left(RDWMIN(T) + \frac{RDW(T)}{1 + PRWG_i \cdot V_{gd,\,eff}} \right) + R_{d,\,geo}$$

RDSMOD=2 (Internal and Geometry dependent)

$$R_{ds}(V) = \frac{1}{NF \cdot W_{eff}^{WR}} \cdot \left(R_{s,\,geo} + R_{d,\,geo} + RDSWMIN(T) + \frac{RDSW(T)}{1 + PRWG_i \cdot q_{ia}} \right)$$

Bias-independent Diffusion Resistance

$$R_{s,\,geo} = NRD \cdot RSHS$$

$$R_{d,\,geo} = NRD \cdot RSHD$$

© 2023 Cadence Design Systems, Inc.

Overlap Capacitance Model

$$Q_{fgs,\,ov} = W_{eff,\,CV} \cdot LOVS_i \cdot C_{ox1} \cdot C(ge,s) + W_{eff,\,CV} \cdot CGSL$$

$$\left\{V_{fgs,\,noswap} - V_{fbsd} - V_{fgs,\,ov} - \frac{1}{2} \cdot CKAPPAS \cdot \left[\left(\sqrt{1 - \frac{4V_{gs,\,overlap}}{CKAPPAS}} - 1\right)\right]\right\} \cdot devsign$$

$$Q_{fgd,\,ov} = W_{eff,\,CV} \cdot LOVD_i \cdot C_{ox1} \cdot V(ge,d) + W_{eff,\,CV} \cdot CGDL$$

$$\left\{V_{fgd,\,noswap} - V_{fbsd} - V_{fgd,\,ov} - \frac{1}{2} \cdot CKAPPAS \cdot \left[\left(\sqrt{1 - \frac{4V_{gd,\,overlap}}{CKAPPAD}} - 1\right)\right]\right\} \cdot devsign$$

Outer Fringe Capacitances

$$Q_{fgs,\,of} = W_{eff,\,CV} \cdot CFS \cdot V(ge,s)$$

$$Q_{fgd,\,of} = W_{eff,\,CV} \cdot CFD \cdot V(ge,d)$$

© 2023 Cadence Design Systems, Inc.

Inner Fringe Capacitance

$$C_{if,factor} = ETACIF \cdot W_{eff,CV} \cdot \frac{2\varepsilon_{si}}{\pi}$$

$$1n\left[\frac{\varepsilon_{ratio} \cdot EOT1 + TSI + \sqrt{L_{un}{}^2 + TSI^2 + 2\varepsilon_{ratio} \cdot EOT1 \cdot TSI}}{L_{un} + \varepsilon_{ratio} \cdot EOT1}\right]$$

$$Q_{fgs,if} = devsign \cdot C_{if,factor} \cdot \left(\psi_{fs} - 0.0 - \frac{1}{2}E_g\right)$$

$$Q_{fgd,if} = devsign \cdot C_{if,factor} \cdot \left(\psi_{fd} - V_{ds} - \frac{1}{2}E_g\right)$$

Source/drain to Substrate Capacitances

$$C_{sdbgsw0} = CSDBGSW \cdot 1n\left(1 + \frac{TSI}{EOT2}\right)$$

$$Q_{sbg} = [C_{ox2} \cdot AS + (PS - W) \cdot C_{sdbgsw0}] \cdot V(s,bg)$$

$$Q_{dbg} = [C_{ox2} \cdot AD + (PD - W) \cdot C_{sdbgsw0}] \cdot V(d,bg)$$

Impact Ionization and GIDL/GISL Model

Impact Ionization Current

$$Iii = \frac{ALPHA0_i + ALPHA1_i \cdot L_{eff}}{L_{eff}}(V_{ds} - V_{dseff}) \cdot e^{\frac{-BETA0}{V_{ds} - V_{dseff}}} \cdot Ids$$

© 2023 Cadence Design Systems, Inc.

Gate-Induced-Drain/Source-Leakage Current

$$I_{gidl} = AGIDL \cdot W_{eff} \cdot \frac{V_{ds} - V_{fgs} - EGIDL + V_{fbsd}}{\varepsilon_{ratio} \cdot EOT1} \times \exp\left(-\frac{\varepsilon_{ratio} \cdot EOT1 \cdot BGIDL(T)}{V_{ds} - V_{fgs} - EGIDL + V_{fbsd}}\right)$$

$$I_{gisl} = AGIDL \cdot W_{eff} \cdot \frac{-V_{ds} - V_{fgd} - EGIDL + V_{fbsd}}{\varepsilon_{ratio} \cdot EOT1} \times \exp\left(-\frac{\varepsilon_{ratio} \cdot EOT1 \cdot BGIDL(T)}{-V_{ds} - V_{fgd} - EGIDL + V_{fbsd}}\right)$$

© 2023 Cadence Design Systems, Inc.

Gate Tunneling Current

Gate to channel current (I_{gc})

$$I_{gcs} = \frac{W_{eff} \cdot L_{eff} \cdot A}{\left(\frac{EOT1 \cdot EPSROX}{3.9}\right)^2} \cdot V'_{fgs} \cdot V_{auxs}$$

$$\cdot \exp\left(-B \cdot \frac{EOT1 \cdot EPSROX}{3.9} \cdot (AIGC - BIGC \cdot V_{oxm})\right) \cdot (1 + CIGC \cdot V_{oxm})$$

$$I_{gcd} = \frac{W_{eff} \cdot L_{eff} \cdot A}{\left(\frac{EOT1 \cdot EPSROX}{3.9}\right)^2} \cdot V'_{fgd} \cdot V_{auxd}$$

$$\cdot \exp\left(-B \cdot \frac{EOT1 \cdot EPSROX}{3.9} \cdot (AIGC - BIGC \cdot V_{oxm})\right) \cdot (1 + CIGC \cdot V_{oxm})$$

$$I_{gc} = I_{gcs} + I_{gcd}$$

© 2023 Cadence Design Systems, Inc.

Gate to source/drain current (`Igs`, `Igd`)

$$I_{gs} = \frac{W_{eff} \cdot DLCIG \cdot A}{\left(EOT \cdot \frac{EPSROX}{3.9} \cdot POXEDGE_i\right)^2} \cdot V_{fgs} \cdot V'_{fgs}$$

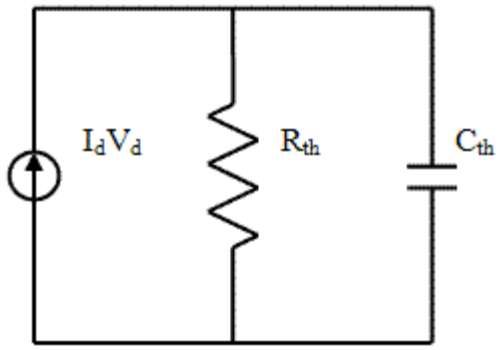
$$\cdot \exp\left(-B \cdot EOT \cdot \frac{EPSROX}{3.9} \cdot POXEDGE_i \cdot (AIGS_i - BIGS_i \cdot V'_{fgs}) \cdot (1 + CIGS_i \cdot V'_{fgs})\right)$$

$$I_{gd} = \frac{W_{eff} \cdot DLCIG \cdot A}{\left(EOT \cdot \frac{EPSROX}{3.9} \cdot POXEDGE_i\right)^2} \cdot V_{fgd} \cdot V'_{fgd}$$

$$\cdot \exp\left(-B \cdot EOT \cdot \frac{EPSROX}{3.9} \cdot POXEDGE_i \cdot (AIGS_i - BIGS_i \cdot V'_{fgd}) \cdot (1 + CIGS_i \cdot V'_{fgd})\right)$$

Self Heating Model

Figure 47-1 R-C network for self-heating calculation



© 2023 Cadence Design Systems, Inc.

Thermal resistance and capacitance calculations

$$\frac{1}{R_{th}} = G_{th} = \frac{WTH0 + W_{eff} \cdot NF}{RTH0}$$

$$C_{th} = CTH0 \cdot (WTH0 + W_{eff} \cdot NF)$$

Noise Modeling

Following noise models are available in BSIMIMG 102.6.1:

Flicker Noise Model

In BSIMIMG102.6.1, the flicker noise model is same as FNOIMOD=1 in BSIM4. The unified physical ficker noise model is smooth over all bias regions. The physical mechanism for the ficker noise is trapping/detrapping-related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobilities in the channel. The unified flicker noise model captures this physical process. In the inversion region, the noise density is expressed as:

$$E_{sat,noi} = \frac{2 \cdot VSAT(T)}{\mu_0(T) D_{mobs}}$$

$$L_{eff,noi} = L_{eff} - 2 \cdot LINTNOI$$

The channel length reduction due to channel length modulation and given by:

$$\Delta L_{clm} = l \cdot \ln \left[\frac{1}{E_{sat,noi}} \cdot \left(\frac{V_{ds} - V_{dseff}}{l} + EM \right) \right]$$

Charge density at the source side is given by:

$$N0 = \frac{C_{ox1} \cdot q_{is}}{q}$$

© 2023 Cadence Design Systems, Inc.

Charge density at the drain side is given by:

$$Nl = \frac{C_{ox1} \cdot q_{id}}{q}$$

and N* is given by:

$$N^{*} = \frac{kT}{q}(C_{ox1} + CIT)$$

where CIT is a model parameter from DC IV.

$$FN1 = NOIA \cdot \ln\left(\frac{N_0 + N^{*}}{N_l + N^{*}}\right) + NOIB \cdot (N_0 - N_l) + \frac{NOIC}{2}(N_0^2 - N_l^2)$$

$$FN2 = \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + N^{*})^2}$$

In the strong inversion region, the noise density is written as:

$$S_{si} = \frac{kTq^2\mu_0(T)I_{ds}}{C_{ox1}L_{eff,noi}^2 \cdot 10^{10}} \cdot FN1 + \frac{kTI_{ds}^2\Delta L_{clm}}{W_{eff} \cdot NF \cdot L_{eff,noi}^2 \cdot 10^{10}} \cdot FN2$$

In the subthresold region, the noise density is given as:

$$S_{wi} = \frac{NOIA \cdot kT \cdot I_{ds}^2}{W_{eff} \cdot NF \cdot L_{eff,noi} \cdot 10^{10} \cdot N^{*2}}$$

The total flicker noise density is given by:

$$S_{id,flicker} = \frac{S_{wi}S_{si}}{S_{wi} + S_{si}}$$

© 2023 Cadence Design Systems, Inc.

Thermal Noise Model

For TNOIMOD=0 (Charge-based model), the noise current is given by:

$$Q_{inv} = |Q_{s,intrinsic} + Q_{d,intrinsic}|$$

$$\overline{i_d^2} = \begin{cases} NTNOI \cdot \frac{4kT\Delta f}{R_{ds}(V)+\frac{L_{eff}^2}{\mu_0(T)Q_{inv}}} & \text{if RDSMOD} = 0 \text{ or } 2 \\ NTNOI \cdot \frac{4kT\Delta f}{L_{eff}^2} \cdot \mu_0(T)Q_{inv} & \text{if RDSMOD} = 1 \end{cases}$$

where $R_{ds}(V)$ is the bias-dependent LDD source/drain resistance, and the parameter NTNOI is introduced for more accurate fitting of short-channel devices. Q_{inv} is the total inversion charge in the channel. $Q_{s,intrinsic}$, $Q_{d,intrinsic}$ are intrinsic charges at source/drain ends.

Gate Current Shot Noise

$$\overline{i_{gs}^2} = 2q(I_{gcs} + I_{gs} + I_{gbs})$$
$$\overline{i_{gd}^2} = 2q(I_{gcd} + I_{gd} + I_{gbd})$$

Resistor Noise Model

If RDSMOD=1, then

$$\frac{\overline{i_{RS}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{source}}$$
$$\frac{\overline{i_{RD}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{drain}}$$

If RGATEMOD=1, then

$$\frac{\overline{i_{RG}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{geltd}}$$

© 2023 Cadence Design Systems, Inc.

Model Version Update

Version 102.94

- Sign of S/D resistance power in self heating model was corrected.

Version 102.92

- Some bugs have been fixed.
- Following enhancements have been made in this release:
  - Self-heating temperature is clamped to a maximum device temperature.
  - Added binning equations to QME parameters.
  - Implemented Drain-Induced-Vth Shift (DITS) module.

Version 102.90

- Added `Vbg` dependence in the gate current module.
- Added external thermal node, `t`.
- Added descriptions for the binning parameters.
- The `ifdef` statements are removed.
- Typo corrected in the technical manual and Bin term default values.
- Improved `gds` fitting in low gate overdrive.
- Added numerical protection for `sqrt(phist)` term
- Alignment of contribution (<+) lines is fixed.
- The pattern for no unit expression is now used for the binning parameters also.
- `$strobe` for `EF` and `NTNOI` are removed.
- `gth` and `cth` in the else case are initialized.
- `CONSTCtoK` is replaced with `P_CELSIUS0`.
- The strobe commands used for diagnostic purpose are removed.

© 2023 Cadence Design Systems, Inc.

Version 102.80

- Expressions of output variables `CGG`, `CSG`, and `CDG` have been fixed.
- Back-gate dependence of `GIDL`/`GISL` currents has been added
- Some additional binning parameters have been made binnable
- Range of several parameters has been adjusted
- `NQSMOD` (intrinsic-input impedance) has been added similar to BSIM-CMG. Two binnable model parameters `XRCRG1` and `XRCRG2` used to adjust the bias-dependent intrinsic-input resistance have also been added.
- First order NR solution in surface potential calculation has been removed to avoid convergence issues
- Output variables `t_total_k`, `t_total_c`, and `t_delta_sh` have been added for self-heating temperature

Version 102.70

- Some bugs have been fixed.
- Following enhancements have been made in this release:
  - A new smoothing function `smoothminx` has been introduced to clamp the minimum value of dmob/dmobs/dvsat at 1 (no degradation) with deltax being the smoothing factor.
  - Two new model parameters DMOBCLAMP and DVSATCLAMP with default values of 0.01have been added.
  - A new operating point parameter VTH has been added.

Version 102.61

Following enhacements have been made in this release:

- The description of `chargemod` parameter has been changed
- Minimum clamp has been updated in rgate for better convergence
- New operating point parameters have been added
- RDSMOD =2 has been introduced to enable source/drain node collapse

© 2023 Cadence Design Systems, Inc.

Component Statements

Sample Model Statement

```
Model nch bsimimg devtype=1 gidlmod=1 igmod=1 rdsmod=1 nobody=1e22
```

Sample Instance Statement

```
m1 (d fg s bg) nch1=30n w=1u nf=4
```

Instance Definition

```
Name  d  fg  s  bg ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

m	1	Multiplicity factor, number of devices in parallel.
l	(30e-9) m	Designed Gate Length.
w	(1e-6) m	Designed Gate Width.
nf	1	Number of fingers.
as	0.0 m^2	Source area.
ad	0.0 m^2	Drain area.
ps	0.0 m	Source perimeter.
pd	0.0 m	Drain perimeter.
nrs	0.0	Number of source diffusion squares.
nrd	0.0	Number of drain diffusion squares.
xl	0 m	L offset for channel length due to mask/etch effect.
dtemp	0 Celsius	Variability in Device Temperature.
trise	0	Variability in Device Temperature.
delvtrand	0 V	Variability in Vth.
u0mult	1	Variability in carrier mobility.
ids0mult	1.0	Variability in drain current and source/drain resistance for local layout effects.

© 2023 Cadence Design Systems, Inc.

ids0multmod	0	0: Multiply IDS0MULT with core current, 1: Multiply IDS0MULT with core current and divide S/D resistances by IDS0MULT, 2: Same as IDS0MULTMOD=1, except that scaling by IDS0MULT is not considered in self-heating power computation.
rdc	0 ohm	Drain contact resistance.
rsc	0 ohm	Source contact resistance.
isnoisy	yes	Should device generate noise.Possible values are no and yes.

Model Definition‘

```
model modelName bsimimg parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Model Parameters

Model Parameters

`l`	`30e-9 m`	Default channel length.
`w`	`1e-6 m`	Default total width including fingers.
`nf`	`1`	Number of fingers. It serves as the default value of instance nf.
`lmin`	`0.0 m`	Minimum channel length for which the model is valid.
`lmax`	`1.0 m`	Maximum channel length for which the model is valid.
`wmin`	`0.0 m`	Minimum channel width for which the model is valid.
`wmax`	`1.0 m`	Maximum channel width for which the model is valid.
`type`	`n`	Transistor type. For NMOS, type=n, for PMOS, type=p.Possible values are p and n.
`version`	`102.60`	The model parameter "version" only accepts a real number value, like 102.60 for version=102.6.0. The available versions now are 102.60, 102.61, 102.70, 102.80, 102.81, 102.90, 102.91, 102.92 and 102.94.
`welltype`	`(-1)`	Well (substrate) type. For N-well, default welltype=1; for P-well, default welltype=-1.
`chargemod`	`0`	0: Computationally efficient charge density model, 1: Accurate inversion charge density model.
`rdsmod`	`0`	0: Internal s/d resistance model, 1: External s/d resistance model, 2: Both bias dependent and independent part of source/drain resistance internal.

© 2023 Cadence Design Systems, Inc.

gidlmod	0	0: Turn off GIDL/GISL current, 1: Turn on GIDL/GISL current.
igcmod	0	0: Turn off Igc, Igs and Igd, 1: Turn on Igc, Igs and Igd. In V102.7.0, the Default vaule is 0; In Version before 102.7.0, the defaule vaule is 1.
igbmod	0	0: Turn off Igb.
shmod	0	0: No self-heating.
cryomod	0	0: Turn off cryogenic temperature model; 1: Turn on cryogenic temperature model; 2: Turn on cryogenic model and merge smoothly to CRYOMOD=0 for T > 210 K.
rgatemod	0	Gate resistance model selector.
nqsmod	0	0: Turn off NQS model, 1: NQS gate resistance (with gi node).
nfmod	0	0: W taken as total width like BSIM4, 1: W taken as single finger width .
xw	0.0 m	W offset for channel width due to mask/etch effect.
lint	0.0 m	Delta L for IV.
ll	0.0 m^(1+LLN)	Length reduction parameter (dopant diffusion effect).
lw	0.0 m^(1+LWN)	Length scaling parameter.
lwl	0.0 m^(LWN+LLN+1)	Length scaling parameter.

© 2023 Cadence Design Systems, Inc.

lln	1.0	Length reduction parameter (dopant diffusion effect).
lwn	1.0	Length scaling parameter.
wint	0.0 m	Delta W for IV.
wl	0.0 m^(1+WLN)	Width reduction parameter (dopant diffusion effect).
ww	0.0 m^(1+WWN)	Width scaling parameter.
wwl	0.0 m^(WLN+WWN+1)	Width scaling parameter.
wln	1.0	Width reduction parameter (dopant diffusion effect).
wwn	1.0	Width scaling parameter.
dlc	0.0 m	Delta L for CV.
llc	0.0 m	Length scaling parameter.
lwc	0.0 m	Length scaling parameter.
lwlc	0.0 m	Length scaling parameter.
dwc	0.0 m	Delta W for CV.
wlc	0.0 m	Width scaling parameter.
wwc	0.0 m	Width scaling parameter.
wwlc	0.0 m	Width scaling parameter.

© 2023 Cadence Design Systems, Inc.

eot1	(1.0e-9) m	Equivalent front gate dielectric thickness relative to SiO2.
eot2	(10e-9) m	Equivalent back gate dielectric thickness relative to SiO2.
eot1p	(1.0e-9) m	Equivalent physical front gate dielectric thickness relative to SiO2.
dtox1	0.0 m	Difference between effective dielectric thickness and physical thickness.
tsi	(8.0e-9) m	Body thickness.
nbody	1e22 m^{-3}	channel (body) doping.
nsd	2e26 m^{-3}	Source/drain active doping concentration.
nbg	5.0e23 m^{-3}	Well/substrate (or also called back-gate) doping, zero for metal.
xl	0 m	L offset for channel length due to mask/etch effect.
easub	4.05 eV	Electron affinity of well/substrate.
ni0sub	1.1e16 m^{-3}	Intrinsic carrier constant at 300.15K.
bg0sub	1.12 eV	Band gap of well/substrate at 300.15K.
nc0sub	2.86e25	Conduction band density of states.
phig1	4.61 eV	Front Gate Workfunction.
phig2	(4.05+1.12) eV	Back gate workfunction, will be modified according to NBG later in the code.
epsrsub	11.9	Relative dielectric constant of the channel material.

© 2023 Cadence Design Systems, Inc.

epsrox1	3.9	Relative dielectric constant of the front gate dielectric.
ascl	0.0	Parameter for back-gate dependent scale length.
bscl	0.0 V^-1	Parameter for back-gate dependent scale length.
cit	0.0 F/(m^2)	Parameter for interface trap.
cdsc	0.14 F/(m^2)	Coupling capacitance between S/D and channel.
cdscd	0.14 F/(m^2 V)	Drain-bias sensitivity of CDSC.
cbgcbg0	0.0 F/(m^2 V)	Backgate-bias sensitivity of SS for long channel.
cbgcbg0p	0.0 F/(m^2 V^2)	Backgate-bias sensitivity of SS for long channel.
cbgcbg	0.0 F/(m^2 V)	Backgate-bias sensitivity of CDSC.
cbgcbgp	0.0 F/(m^2 V^2)	Nonlinear backgate-bias sensitivity of SS.
cbgcbgd	0.0 F/(m^2 V^2)	backgate-bias sensitivity of CDSCD.
dvt0	19.20	SCE coefficient.
dvt1	0.45	SCE exponent coefficient.
phin	0.045 V	Nonuniform vertical doping effect on surface potential.
eta0	2.00	DIBL coefficient 1.

© 2023 Cadence Design Systems, Inc.

dsub	0.375	DIBL coefficient 2 (exponent coefficient).
dvtp0	0	Coefficient for Drain-Induced Vth Shift (DITS).
dvtp1	0	DITS exponent coefficient.
advtp0	0.0	Pre-exponential Coefficient for DITS.
bdvtp0	100.0e-9	Exponential coefficient for DITS.
advtp1	0.0	Pre-exponential coefficient for DVTP1.
bdvtp1	100.0e-9	Exponential coefficient for DVTP1.
dvtp2	0.0	DITS model parameter.
etab	0.00	DIBL coefficient - back gate dependence.
k1rsce	(-0.32)	Vt Roll-off at moderate Lg.
lpe0	8.2e-9 m	Equivalent length of pocket region at zero bias.
dsc0	0.0	Parameter for short channel effect at moderate L and high drain bias.
dsc1	1.00e-9	Parameter for short channel effect at moderate L and high drain bias.
k0	0.0 V	Lateral NUD voltage parameter.
k01	0.0 V/K	Temperature dependence of lateral NUD voltage parameter.
k0si	1.0	Correction factor for strong inversion, used in Mnud, after binning should be from (0:inf).
k0si1	0.0 K^-1	Temperature dependence of K0SI.

© 2023 Cadence Design Systems, Inc.

qmtcencv	0.0	Prefactor + switch for QM Width and Toxeff correction for CV.
etaqm	0.54	Bulk charge coefficient for Tcen.
qm0	1.00e-3	Knee-Point for Tcen in inversion (Charge normalized to Cox).
pqm	0.66	Slope of normalized Tcen in inversion.
toxp	(1.0e-9) m	physical oxide thickness.
vsat	85000 m/s	Saturation Velocity.
avsat	0.0 m/s	Saturation velocity in the saturation region for short channel devices.
bvsat	100.0e-9 m	Saturation velocity coefficient in the saturation region for short channel devices.
vsat1	85000 m/s	Saturation velocity in the linear region.
avsat1	0.0 m/s	Saturation velocity in the linear region for short channel devices.
bvsat1	100.0e-9 m	Saturation velocity coefficient in the linear region for short channel devices.
vsatcv	85000 m/s	Velocity Saturation parameter for CV.
avsatcv	0.0 m/s	Saturation velocity in the saturation region for short channel C-V.
bvsatcv	100.0e-9 m	Saturation velocity coefficient in the saturation region for short channel C-V.

© 2023 Cadence Design Systems, Inc.

deltavsat	1.0 m/s	Velocity saturation parameter.
ksativ	1.0	Parameter for strong inversion regime for long channel Vdsat.
ksubiv	1.0	Parameter for weak inversion regime for long channel Vdsat.
mexp	4.0	Smoothing function factor for Vdsat.
amexp	0.0	Smoothing function factor for Vdsat in short channel devices.
bmexp	1.0	Smoothing function coefficient for Vdsat in short channel devices.
ptwg	0.0 V^{-2}	Correction factor for velocity saturation.
aptwg	0.0 V^{-2}	Correction factor for velocity saturation in short channel devices.
bptwg	100.0e-9 m	Coefficient for correction factor for velocity saturation in short channel devices.
at	(-1.56e-3) /K	Saturation Velocity Temperature Coefficient.
at2	2.0e-6 / K^2	CRYOMOD != 0 saturation velocity temperature coefficient.
atl	0.0	Length scaling for AT.
tmexp	0.0	Temperature Coefficient for smoothing function factor for Vdsat.
tmexp2	(-4.0e-6) /K^2	CRYOMOD != 0 temperature coefficient for Vdseff smoothing.

© 2023 Cadence Design Systems, Inc.

ksativt1	(-2.0e-4) /K	CRYOMOD != 0 temperature coefficient for KSATIV.
ksativt2	(-2.0e-7) /K^2	CRYOMOD != 0 temperature coefficient for KSATIV.
ptwgt	0.004 /K	PTWG Temperature Coefficient.
ptwgb	0.0 V^{-3}	Parameter for back gate bias sensitivity.
ptwgb2	0.0 V^{-3}	Parameter for back gate bias sensitivity.
aptwgb	0.0 V^{-3}	Parameter for back gate bias sensitivity.
bptwgb	100.0e-9 m	Parameter for back gate bias sensitivity for short channel devices.
aptwgb2	0.0 V^{-3}	Parameter for back gate bias sensitivity for short channel devices.
bptwgb2	100.0e-9 m	Parameter for back gate bias sensitivity for short channel devices.
vsatb	0.0 V^-1	Saturation velocity parameter for Back Gate Bais dependence on mobility at high Vds.
atb	0.0 /K	Back bias sensitivity parameter for saturation velocity temperature coefficient.
atbl	0.0 m	Length scaling for ATB.
avsatb	0.0 V^-1	Saturation velocity parameter for back gate bias dependence on mobility at high Vds for short channel devices.
bvsatb	100.0e-9 m	Saturation velocity parameter for back gate bias dependence on mobility at high Vds for short channel devices.

© 2023 Cadence Design Systems, Inc.

dvsatclamp	0.01 m	Minimum clamp on Dvsat.
u0	0.03 m^2/(V s)	Low Field Mobility.
etamob	2.0	Effective field parameter.
up	0.0 (μm)^LPA	Mobility L coefficient.
lpa	1.0	Mobility L power coefficient.
ua	0.3 (MV/cm)^(-EU)	Phonon / surface roughness scattering.
aua	0.0 (MV/cm)^(-EU)	Phonon / surface roughness scattering for short channel devices.
bua	100.0e-9 m	Phonon / surface roughness scattering for short channel devices.
eu	2.5 cm/MV	Phonon / surface roughness scattering.
aeu	0.0 cm/MV	Phonon / surface roughness scattering for short channel devices.
beu	100.0e-9 m	Phonon / surface roughness scattering for short channel devices.
uc	0.0 (1/V) (MV/cm)^(-EU)	Parameter for Back Gate Bais dependence on mobility at low Vds.

© 2023 Cadence Design Systems, Inc.

auc	0.0 (1/V) (MV/cm)^(-EU)	Parameter for Back Gate Bais dependence on mobility at low Vds for short channel devices.
buc	100.0e-9 m	Parameter for Back Gate Bais dependence on mobility at low Vds for short channel devices.
ud	0.0	Columbic scattering (experimental).
aud	0.0	Columbic scattering (experimental) for short channel devices.
bud	50.0e-9 m	Columbic scattering (experimental) for short channel devices.
udb	0.0 V^-1	Back bias sensitivity on columbic scattering (experimental).
audb	0.0 V^-1	Back bias sensitivity on columbic scattering (experimental) for short channel devices.
budb	50.0e-9 m	Back bias sensitivity on columbic scattering (experimental) for short channel devices.
dmobclamp	0.01 m	Minimum clamp on Dmob.
ucs	1.0	Columbic scattering (experimental).
uds	2.0e-5	CRYOMOD != 0 weight factor correction for source side inversion charge density in Coulomb scattering model.
udd	(-2.0e-5)	CRYOMOD != 0 weight factor correction for drain side inversion charge density in Coulomb scattering model.
ute	0.0	Mobility temperature coefficient.

© 2023 Cadence Design Systems, Inc.

ute1	(-0.4)	CRYOMOD != 0 temperature coefficient for U0.
utl	(-1.5e-3)	Mobility temperature coefficient.
ua1	1.032e-3	Mobility temperature coefficient for UA.
ua2	(-0.04)	CRYOMOD != 0 mobility temperature coefficient for UA.
uc1	0.0	Mobility temperature coefficient for UC.
eu1	(-2.0e-4)	CRYOMOD != 0 mobility temperature coefficient for EU.
ud1	0.0	Mobility Temperature Coefficient.
ud2	(-0.04)	CRYOMOD != 0 mobility temperature coefficient for UD.
ucste	(-4.775e-3)	Mobility temperature coefficient.
ucste1	(-0.04)	CRYOMOD != 0 mobility temperature coefficient for UCS.
uds1	(-10.0)	CRYOMOD != 0 temperature coefficient for UDS.
udd1	(-10.0)	CRYOMOD != 0 temperature coefficient for UDD.
chargewf	0	Average channel charge weighting factor, +1:source-side, 0:middle, -1:drain-side.
rdswmin	0.0 ohm µm^WR	S/D extension resistance per unit width at high Vgs for RDSMOD = 0.

© 2023 Cadence Design Systems, Inc.

rdsw	100.0 ohm µm^WR	Zero bias S/D extension resistance per unit width for RDSMOD = 0.
ardsw	0.0 ohm µm^WR	RDSMOD = 0 zero bias S/D extension resistance per unit width for short channel devices.
brdsw	100.0e-9 m	RDSMOD = 0 zero bias S/D extension resistance per unit width for short channel devices.
rswmin	0.0 ohm µm^WR	Source extension resistance per unit width at high Vgs for RDSMOD = 1.
rsw	50.0 ohm µm^WR	Zero bias source extension resistance per unit width for RDSMOD = 1.
arsw	0.0 ohm µm^WR	pre-exponential coefficient for RSW.
brsw	100.0e-9 m	Zero bias source extension resistance per unit width for short channel devices for RDSMOD = 1.
rdwmin	0.0 ohm µm^WR	Drain extension resistance per unit width at high Vgs for RDSMOD = 1.
rdw	50.0 ohm µm^WR	Zero bias drain extension resistance per unit width for RDSMOD = 1.
ardw	0.0 ohm µm^WR	RDSMOD = 1 zero bias drain extension resistance per unit width for short channel devices.
brdw	100.0e-9 m	RDSMOD = 1 zero bias drain extension resistance per unit width for short channel devices.
prwg	0 V^-1	Gate bias dependence of source/drain extension resistance.
prwb	0 V^-1	Back gate bias dependence of source/drain extension resistance.

© 2023 Cadence Design Systems, Inc.

wr	1.0 V^-1	W dependence parameter of S/D extension resistance.
prt	0.001 K^-1	Series Resistance Temperature coefficient.
prt1	4.0e-4 K^-1	CRYOMOD != 0 series resistance temperature coefficient at low temperatures.
tr0	170.0 K	CRYOMOD != 0 corner temperature in dual-slope temperature model of series resistance.
sprt	1.0e-2	CRYOMOD != 0 parameter for corner temperature smoothing in dual-slope temperature model of series resistance.
pdibl1	1.30	DIBL Output Conductance parameter.
pdibl2	2.0e-4	DIBL Output Conductance parameter.
drout	1.06	L dependence of DIBL effect on Rout.
pvag	1.0	Vgs dependence on early voltage.
pclm	0.013	Channel Length Modulation (CLM) parameter.
apclm	0.0	Channel Length Modulation (CLM) parameter for short channel devices.
bpclm	100.0e-9 m	Channel Length Modulation (CLM) parameter for short channel devices.
pclmg	0.0	Gate bias dependent parameter for channel Length Modulation (CLM).
pclmcv	0.013	Channel Length Modulation (CLM) parameter for C-V.

© 2023 Cadence Design Systems, Inc.

pclmt	(-2.0e-5) /K	CRYOMOD != 0 temperature coefficient for PCLM.
rshs	0.0 ohm	Source-side sheet resistance.
rshd	0.0 ohm	Drain-side sheet resistance.
aigbinv	1.11e-2 ((F s^2/g)^0.5) m^-1	parameter for Igb in inversion.
bigbinv	9.49e-4 ((F s^2/g)^0.5) (m V)^-1	parameter for Igb in inversion.
cigbinv	6.00e-3 V^-1	parameter for Igb in inversion.
eigbinv	1.1 V	parameter for Igb in inversion.
nigbinv	3.0	parameter for Igb in inversion.
aigbacc	1.36e-2 ((F s^2/g)^0.5) m^-1	parameter for Igb in accumulation.
bigbacc	1.71e-3 ((F s^2/g)^0.5) (m V)^-1	parameter for Igb in accumulation.
cigbacc	7.5e-2 V^-1	parameter for Igb in accumulation.
nigbacc	1.0	parameter for Igb in accumulation.

© 2023 Cadence Design Systems, Inc.

aigc	1.36e-2 ((F s^2/ g)^0.5) m^-1	Parameter for Igc in inversion.
bigc	1.71e-3 ((F s^2/ g)^0.5) (m V)^-1	Parameter for Igc in inversion.
cigc	0.075 V^-1	Parameter for Igc in inversion.
pigcd	1.0	Parameter for Igc partition.
aigs	1.36e-2 ((F s^2/ g)^0.5) m^-1	Parameter for Igs, Igd.
bigs	1.71e-3 ((F s^2/ g)^0.5) (m V)^-1	Parameter for Igs, Igd.
cigs	0.075 V^-1	Parameter for Igs, Igd.
dlcigs	0	Delta L for Igs model.
dlcigd	0	Delta L for Igd model.
aigd	1.36e-2 ((F s^2/ g)^0.5) m^-1	Parameter for Igd in inversion.

© 2023 Cadence Design Systems, Inc.

bigd	1.71e-3 ((F s^2/ g)^0.5) (m V)^-1	Parameter for Igd in inversion.
cigd	0.075 V^-1	Parameter for Igs, Igd.
toxref	(1.2e-9) m	Target tox value.
ntox	1.0	Exponent for Tox ratio.
poxedge	1.0	Factor for the gate edge Tox.
agisl	(6.055e-12) mho	pre-exponential coeff. for GISL.
bgisl	0.3e9 V/ m	exponential coeff. for GISL.
egisl	0.2 V	Band bending parameter for GISL.
pgisl	1.0	Parameter for body-bias effect on GISL.
agidl	(6.055e-12) mho	Pre-exponential coeff. for GIDL.
bgidl	0.3e9 V/ m	Exponential coeff. for GIDL.
egidl	0.2 V	Band bending parameter for GIDL.
pgidl	1.0	Parameter for body-bias effect on GIDL.
vbgisl	1.0	Back gate correction factor for GISL.
vbegisl	0.5 V	Back band bending parameter for GISL.

© 2023 Cadence Design Systems, Inc.

vbgidl	1.0	Back gate correction factor for GIDL.
vbegidl	0.5 V	Back band bending parameter for GIDL.
alpha0	0.0 m/V	First parameter of Iii.
alpha1	0.0 V^-1	L scaling parameter of Iii.
beta0	0.0 V^-1	Vds dependent parameter of Iii.
lovs	0.0 m	Overlap length for fg/s fg/d overlap.
lovd	0.0 m	Overlap length for fg/s fg/d overlap.
cfs	0.0 F/m	Outer Fringe Cap.
cfd	0.0 F/m	Outer Fringe Cap.
cgsl	0.0 F/m	Overlap capacitance between gate and lightly-doped source region.
cgdl	0.0 F/m	Overlap capacitance between gate and lightly-doped drain region.
ckappas	0.6 V	Coefficient of bias-dependent overlap capacitance for the source side.
ckappad	0.6 V	Coefficient of bias-dependent overlap capacitance for the drain side.
csdbgsw	0.0 F/m	Source/drain sidewall fringing capacitance per unit length.
pcovbs0	0.0 V	Back-gate dependent overlap capacitance clamping shift voltage for the source side.
pcovbs1	0.0	Parameter of back-gate dependent overlap capacitance for the source side.

© 2023 Cadence Design Systems, Inc.

pcovbd0	0 V	Back-gate dependent overlap capacitance clamping shift voltage for the drain side.
pcovbd1	0	Parameter of back-gate dependent overlap capacitance for the drain side.
kbg0pw	1.0	Length dependence of substrate factor.
kbg1pw	0.0	Length dependence of substrate factor.
kbg2pw	(-1.0)	Length dependence of substrate factor.
dbgpw	0.12	Length dependence of substrate factor.
bpfactorpw	0.0	Back-plane (BP) effect, 1 means no BP.
vknee1pw	0.0 V	Back gate voltage at which the substrate depletion below the BOX starts.
vknee2pw	1.0 V	Maximum potential drop below the BOX.
kbg0nw	1.0	Length dependence of body factor.
kbg1nw	0.0	Length dependence of body factor.
kbg2nw	(-1.0)	Length dependence of body factor.
dbgnw	0.12	Length dependence of body factor.
bpfactornw	0.0	Back-plane (BP) effect, 1 means no BP.
vknee1nw	0.0 V	Back gate voltage at which the substrate depletion below the BOX starts.
vknee2nw	1.0 V	Maximum potential drop below the BOX.
ef	1.0	Flicker noise frequency exponent.

© 2023 Cadence Design Systems, Inc.

em	4.1e7 V/m	Flicker noise parameter.
noia	6.250e+39 eV^-1 s^1-EF m^{-3}	Flicker noise parameter.
noib	3.125e+24 eV^-1 s^1-EF m^-1	Flicker noise parameter.
noic	8.750e+07 eV^-1 s^1-EF m	Flicker noise parameter.
ntnoi	1.0	Thermal noise parameter.
lintnoi	0.0 m	Lint offset for flicker noise calculation.
tnoimod	0	0: Charge-based, 1: Correlated thermal noise model.
rnoia	0.5774	Empirical parameter for Sid level.
tnoia	0.0 /m	Empirical parameter for Leff trend of Sid.
rnoib	0.3652	Empirical parameter for Sig level.
tnoib	0.0 /m	Empirical parameter for Leff trend of Sig.
rnoic	0.3953	Empirical parameter for correlation coefficient.
tnoic	0.0 /m	Empirical parameter for Leff trend of correlation coefficient.
rnoik	0.0	Empirical parameter for Sid level at low Ids.

© 2023 Cadence Design Systems, Inc.

tnoik	0.0 /m	Empirical parameter for Leff trend of Sid at low Ids.
tnoik2	0.1	Empirical parameter for sensitivity of RNOIK.
tnom	27.0 Celsius	Temperature at which the model is extracted.
tmaxc	400.0 Celsius	Maximum device temperature.
tbgasub	7.02e-4 eV/K	Bandgap temperature coefficient.
tbgbsub	1108.0 K	Bandgap temperature coefficient.
kt1	0.0 V	Vth temperature coefficient.
kt1l	0.0 V m	Vth temperature length coefficient.
kt2	0.0	Vth temperature vbg coefficient.
kt2l	0.0 m	Vbg temperature length coefficient.
kt11	0.01 V	CRYOMOD != 0 Vth temperature coefficient.
kt12	0.1 /K	CRYOMOD != 0 Vth temperature coefficient.
tvth	50.0 K	CRYOMOD != 0 transition temperature for Vth temperature model.
iit	(-0.5)	Impact ionization temperature dependence.
tgidl	(-0.003) K^-1	GIDL temperature dependence.
tgisl	(-0.003) K^-1	GISL temperature dependence.
igt	2.5	Gate current temperature dependence.

© 2023 Cadence Design Systems, Inc.

teta0	0.0 K^-1	Temperature dependence for DIBL effects.
tlow	50.0 K	CRYOMOD != 0 transition temperature of subthreshold swing at low temperature.
dtlow	1.0 K	CRYOMOD != 0 smoothing parameter for TLOW.
tlow1	0.0 K	CRYOMOD != 0 transition temperature of subthreshold swing at low temperatures.
dtlow1	0.0 K	CRYOMOD != 0 smoothing parameter for TLOW1.
klow1	0.0	CRYOMOD != 0 magnitude of slope of effective temperature vs temperature below TLOW1.
rth0	0.01 ohm m K/W	Thermal resistance.
cth0	1.0E-05 W s/m/K	Thermal capacitance.
wth0	0.0 m	Width dependence coefficient for Rth and Cth.
minr	0.001 ohm	Minimum resistance.
compatible	spectre	Compatible parameter.Possible values are spectre, spice2, spice3, cdsspice, hspice, spiceplus, eldo, sspice and mica.
vthmod		Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'.Possible values are std and vthcc.
ivth	(A)	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.

© 2023 Cadence Design Systems, Inc.

ivthw	(m)	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
ivthl	(m)	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
ivth_vdsmin	(V)	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
vdsatmod	0	Vdsat output selector. Possible values are std, gds, and slow_gds.Possible values are std, gds and slow_gds.
vdsat_c	0.0	Coefficient for Gds based Vdsat.
vdsat_vdl	0.0	Coefficient for Gds based Vdsat.
vdsat_vadj	0.0	Coefficient for Gds based Vdsat.
xgw	0.0 m	Dist from gate contact center to dev edge.
xgl	0.0 m	Variation in Ldrawn.
ngcon	1	Number of gate contacts.
rshg	0.1 ohm	Gate sheet resistance.
xrcrg1	12.0	Parameter for Rg in NQSMOD = 1.
xrcrg2	1.0	Parameter for Rg in NQSMOD = 1.
delhci	0.0	HCI degradation parameter. 0: turns off HCI aging model.
hcidb0	0.0	HCI parameter for Vdbg dependence.
hcidb1	0.0 V^-1	HCI parameter for Vdbg dependence.

© 2023 Cadence Design Systems, Inc.

hciu0	0.0 m^2/(Vs)	HCI aging parameter for U0.
hcidu0	0.0 m^2/(Vs)	HCI aging parameter for U0.
hciud	0.0	HCI aging parameter for UD.
hcidud	0.0	HCI aging parameter for UD.
hciucs	0.0	HCI aging parameter for UCS.
hciducs	0.0	HCI aging parameter for UCS.
hcivsat	0.0 m/s	HCI aging parameter for VSAT.
hcidvsat	0.0 m/s	HCI aging parameter for VSAT.
hcicit	0.0 F/m^2	HCI aging parameter for CIT.
hcidcit	0.0 F/m^2	HCI aging parameter for CIT.
hcivth	0.0 V	HCI aging parameter for threshold voltage.
hcidvth	0.0 V	HCI aging parameter for threshold voltage.
gdsmin	1.0e-15 mho	Minimum Conductance.
lrdsw	0.0 ohm µm^WR m	Length scaling parameter for rdsw.
wrdsw	0.0 ohm µm^WR m	Width scaling parameter for rdsw.
prdsw	0.0 ohm µm^WR m^2	Cross-term scaling parameter for rdsw.

© 2023 Cadence Design Systems, Inc.

lrdw	0.0 ohm µm^WR m	Length scaling parameter for rdw.
wrdw	0.0 ohm µm^WR m	Width scaling parameter for rdw.
prdw	0.0 ohm µm^WR m^2	Cross-term scaling parameter for rdw.
lrsw	0.0 ohm µm^WR m	Length scaling parameter for rsw.
wrsw	0.0 ohm µm^WR m	Width scaling parameter for rsw.
prsw	0.0 ohm µm^WR m^2	Cross-term scaling parameter for rsw.
lprwg	0.0 m/V	Length scaling parameter for prwg.
wprwg	0.0 m/V	Width scaling parameter for prwg.
pprwg	0.0 (m^2)/V	Cross-term scaling parameter for prwg.
lprwb	0.0 m	Length scaling parameter for prwb.
wprwb	0.0 m	Width scaling parameter for prwb.
pprwb	0.0 m^2	Cross-term scaling parameter for prwb.
lwr	0.0 m	Length scaling parameter for wr.
wwr	0.0 m	Width scaling parameter for wr.
pwr	0.0 m^2	Cross-term scaling parameter for wr.
lphig1	0.0 V m	Length scaling parameter for phig1.

© 2023 Cadence Design Systems, Inc.

wphig1	0.0 V m	Width scaling parameter for phig1.
pphig1	0.0 V (m^2)	Cross-term scaling parameter for phig1.
lphig2	0.0 V m	Length scaling parameter for phig2.
wphig2	0.0 V m	Width scaling parameter for phig2.
pphig2	0.0 V (m^2)	Cross-term scaling parameter for phig2.
lnsd	0.0 m^{-2}	Length scaling parameter for nsd.
wnsd	0.0 m^{-2}	Width scaling parameter for nsd.
pnsd	0.0 m^-1	Cross-term scaling parameter for nsd.
lnbody	0.0 m^{-2}	Length scaling parameter for nbody.
wnbody	0.0 m^{-2}	Width scaling parameter for nbody.
pnbody	0.0 m^-1	Cross-term scaling parameter for nbody.
lcit	0.0 F/m	Length scaling parameter for cit.
wcit	0.0 F/m	Width scaling parameter for cit.
pcit	0.0 F	Cross-term scaling parameter for cit.
lcdsc	0.0 F/m	Length scaling parameter for cdsc.
wcdsc	0.0 F/m	Width scaling parameter for cdsc.
pcdsc	0.0 F	Cross-term scaling parameter for cdsc.
lcdscd	0.0 F/(m V)	Length scaling parameter for cdscd.

© 2023 Cadence Design Systems, Inc.

wcdscd	0.0 F/(m V)	Width scaling parameter for cdscd.
pcdscd	0.0 F/V	Cross-term scaling parameter for cdscd.
lcbgcbg	0.0 F/(m V)	Length scaling parameter for cbgcbg.
wcbgcbg	0.0 F/(m V)	Width scaling parameter for cbgcbg.
pcbgcbg	0.0 F/m	Cross-term scaling parameter for cbgcbg.
ldvt0	0.0 m	Length scaling parameter for dvt0.
wdvt0	0.0 m	Width scaling parameter for dvt0.
pdvt0	0.0 m^2	Cross-term scaling parameter for dvt0.
ldvt1	0.0 m	Length scaling parameter for dvt1.
wdvt1	0.0 m	Width scaling parameter for dvt1.
pdvt1	0.0 m^2	Cross-term scaling parameter for dvt1.
lphin	0.0 V m	Length scaling parameter for phin.
wphin	0.0 V m	Width scaling parameter for phin.
pphin	0.0 V (m^2)	Cross-term scaling parameter for phin.
leta0	0.0 m	Length scaling parameter for eta0.
weta0	0.0 m	Width scaling parameter for eta0.
peta0	0.0 m	Cross-term scaling parameter for eta0.
letab	0.0 m/V	Length scaling parameter for etab.

© 2023 Cadence Design Systems, Inc.

wetab	0.0 m/V	Width scaling parameter for etab.
petab	0.0 $(m^2)/V$	Cross-term scaling parameter for etab.
ldsub	0.0 m	Length scaling parameter for dsub.
wdsub	0.0 m	Width scaling parameter for dsub.
pdsub	0.0 m^2	Cross-term scaling parameter for dsub.
lk1rsce	0.0 m V^(-1/2)	Length scaling parameter for k1rsce.
wk1rsce	0.0 m V^(-1/2)	Width scaling parameter for k1rsce.
pk1rsce	0.0 (m^2) V^(-1/2)	Cross-term scaling parameter for k1rsce.
llpe0	0.0 m^2	Length scaling parameter for lpe0.
wlpe0	0.0 m^2	Width scaling parameter for lpe0.
plpe0	0.0 m^3	Cross-term scaling parameter for lpe0.
lk0	0.0 m	Length scaling parameter for k0.
wk0	0.0 m	Width scaling parameter for k0.
pk0	0.0 m^2	Cross-term scaling parameter for k0.
lk01	0.0 Vm/K	Length scaling parameter for k01.
wk01	0.0 Vm/K	Width scaling parameter for k01.
pk01	0.0 $V(m^2)/K$	Cross-term scaling parameter for k01.

© 2023 Cadence Design Systems, Inc.

lk0si	0.0 m/K	Length scaling parameter for k0si.
wk0si	0.0 m/K	Width scaling parameter for k0si.
pk0si	0.0 $(m^2)/K$	Cross-term scaling parameter for k0si.
lk0si1	0.0 m	Length scaling parameter for k0si1.
wk0si1	0.0 m	Width scaling parameter for k0si1.
pk0si1	0.0 m^2	Cross-term scaling parameter for k0si1.
lmexp	0.0 m	Length scaling parameter for mexp.
wmexp	0.0 m	Width scaling parameter for mexp.
pmexp	0.0 m^2	Cross-term scaling parameter for mexp.
lptwg	0.0 $m/(V^2)$	Length scaling parameter for ptwg.
wptwg	0.0 $m/(V^2)$	Width scaling parameter for ptwg.
pptwg	0.0 $(m^2)/(V^2)$	Cross-term scaling parameter for ptwg.
lptwgb	0.0 $m/(V^3)$	Length scaling parameter for ptwgb.
wptwgb	0.0 $m/(V^3)$	Width scaling parameter for ptwgb.
pptwgb	0.0 $(m^2)/(V^3)$	Cross-term scaling parameter for ptwgb.

© 2023 Cadence Design Systems, Inc.

lptwgb2	0.0 m/(V^3)	Length scaling parameter for ptwgb2.
wptwgb2	0.0 m/(V^3)	Width scaling parameter for ptwgb2.
pptwgb2	0.0 (m^2)/(V^3)	Cross-term scaling parameter for ptwgb2.
lptwgt	0.0 m/K	Length scaling parameter for ptwgt.
wptwgt	0.0 m/K	Width scaling parameter for ptwgt.
pptwgt	0.0 (m^2)/K	Cross-term scaling parameter for ptwgt.
lu0	0.0 (m^3)/V s	Length scaling parameter for u0.
wu0	0.0 (m^3)/V s	Width scaling parameter for u0.
pu0	0.0 (m^4)/V s	Cross-term scaling parameter for u0.
lua	0.0 m (MV/cm)^(-EU)	Length scaling parameter for ua.
wua	0.0 m (MV/cm)^(-EU)	Width scaling parameter for ua.

© 2023 Cadence Design Systems, Inc.

pua	0.0 m^2 (MV/cm)^(-EU)	Cross-term scaling parameter for ua.
luc	0.0 (m/V) (MV/cm)^(-EU)	Length scaling parameter for uc.
wuc	0.0 (m/V) (MV/cm)^(-EU)	Width scaling parameter for uc.
puc	0.0 (m^2/V) (MV/cm)^(-EU)	Cross-term scaling parameter for uc.
lud	0.0 m	Length scaling parameter for ud.
wud	0.0 m	Width scaling parameter for ud.
pud	0.0 m^2	Cross-term scaling parameter for ud.
lucs	0.0 m	Length scaling parameter for ucs.
wucs	0.0 m	Width scaling parameter for ucs.
pucs	0.0 m^2	Cross-term scaling parameter for ucs.
luds	0.0 m	L-term of UDS.
wuds	0.0 m	W-term of UDS.
puds	0.0 m^2	P-term of UDS.
luds1	0.0 m	L-term of UDS1.

© 2023 Cadence Design Systems, Inc.

wuds1	0.0 m	W-term of UDS1.
puds1	0.0 m^2	P-term of UDS1.
ludd	0.0 m	L-term of UDD.
wudd	0.0 m	W-term of UDD.
pudd	0.0 m^2	P-term of UDD.
ludd1	0.0 m	L-term of UDD1.
wudd1	0.0 m	W-term of UDD1.
pudd1	0.0 m^2	P-term of UDD1.
leu	0.0 m^2/MV	Length scaling parameter for eu.
weu	0.0 m^2/MV	Width scaling parameter for eu.
peu	0.0 m^3/MV	Cross-term scaling parameter for eu.
lutl	0.0 m	Length scaling parameter for utl.
wutl	0.0 m	Width scaling parameter for utl.
putl	0.0 m^2	Cross-term scaling parameter for utl.
lute	0.0 m	Length scaling parameter for ute.
wute	0.0 m	Width scaling parameter for ute.
pute	0.0 m^2	Cross-term scaling parameter for ute.
lute1	0.0 m	L-term of UTE1.

© 2023 Cadence Design Systems, Inc.

wute1	0.0 m	W-term of UTE1.
pute1	0.0 m^2	P-term of UTE1.
lua1	0.0 m	Length scaling parameter for ua1.
wua1	0.0 m	Width scaling parameter for ua1.
pua1	0.0 m^2	Cross-term scaling parameter for ua1.
lua2	0.0 m	L-term of UA2.
wua2	0.0 m	W-term of UA2.
pua2	0.0 m^2	P-term of UA2.
lud1	0.0 m	Length scaling parameter for ud1.
wud1	0.0 m	Width scaling parameter for ud1.
pud1	0.0 m^2	Cross-term scaling parameter for ud1.
lud2	0.0 m	L-term of UD2.
wud2	0.0 m	W-term of UD2.
pud2	0.0 m^2	P-term of UD2.
lucste	0.0 m	Length scaling parameter for ucste.
wucste	0.0 m	Width scaling parameter for ucste.
pucste	0.0 m^2	Cross-term scaling parameter for ucste.
lucste1	0.0 m	L-term of UCSTE1.
wucste1	0.0 m	W-term of UCSTE1.

© 2023 Cadence Design Systems, Inc.

pucste1	0.0 m^2	P-term of UCSTE1.
lat	0.0 m/K	Length scaling parameter for at.
wat	0.0 m/K	Width scaling parameter for at.
pat	0.0 (m^2)/K	Cross-term scaling parameter for at.
leu1	0.0 m^2/MV	L-term of EU1.
weu1	0.0 m^2/MV	W-term of EU1.
peu1	0.0 m^3/MV	P-term of EU1.
latb	0.0 m/K	Length scaling parameter for atb.
watb	0.0 m/K	Width scaling parameter for atb.
patb	0.0 (m^2)/K	Cross-term scaling parameter for atb.
lprt	0.0 m/K	Length scaling parameter for prt.
wprt	0.0 m/K	Width scaling parameter for prt.
pprt	0.0 (m^2)/K	Cross-term scaling parameter for prt.
lprt1	0.0 m/K	L-term of PRT1.
wprt1	0.0 m/K	W-term of PRT1.
pprt1	0.0 (m^2)/K	P-term of PRT1.

© 2023 Cadence Design Systems, Inc.

ltr0	0.0 m K	L-term of TR0.
wtr0	0.0 m K	W-term of TR0.
ptr0	0.0 (m^2) K	P-term of TR0.
lsprt	0.0 m/K	L-term of SPRT.
wsprt	0.0 m/K	W-term of SPRT.
psprt	0.0 (m^2)/K	P-term of SPRT.
liit	0.0 m	Length scaling parameter for iit.
wiit	0.0 m	Width scaling parameter for iit.
piit	0.0 m^2	Cross-term scaling parameter for iit.
ltgidl	0.0 m/K	Length scaling parameter for tgidl.
wtgidl	0.0 m/K	Width scaling parameter for tgidl.
ptgidl	0.0 (m^2)/K	Cross-term scaling parameter for tgidl.
ltgisl	0.0 m/K	Length scaling parameter for tgisl.
wtgisl	0.0 m/K	Width scaling parameter for tgisl.
ptgisl	0.0 (m^2)/K	Cross-term scaling parameter for tgisl.
ligt	0.0 m	Length scaling parameter for igt.
wigt	0.0 m	Width scaling parameter for igt.
pigt	0.0 m^2	Cross-term scaling parameter for igt.

© 2023 Cadence Design Systems, Inc.

lpclm	0.0 m	Length scaling parameter for pclm.
wpclm	0.0 m	Width scaling parameter for pclm.
ppclm	0.0 m^2	Cross-term scaling parameter for pclm.
lpclmcv	0.0 m	Length scaling parameter for pclmcv.
wpclmcv	0.0 m	Width scaling parameter for pclmcv.
ppclmcv	0.0 m^2	Cross-term scaling parameter for pclmcv.
ldrout	0.0 m	Length scaling parameter for drout.
wdrout	0.0 m	Width scaling parameter for drout.
pdrout	0.0 m^2	Cross-term scaling parameter for drout.
lpdibl1	0.0 m	Length scaling parameter for pdibl1.
wpdibl1	0.0 m	Width scaling parameter for pdibl1.
ppdibl1	0.0 m^2	Cross-term scaling parameter for pdibl1.
lpdibl2	0.0 m	Length scaling parameter for pdibl2.
wpdibl2	0.0 m	Width scaling parameter for pdibl2.
ppdibl2	0.0 m^2	Cross-term scaling parameter for pdibl2.
lpvag	0.0 m	Length scaling parameter for pvag.
wpvag	0.0 m	Width scaling parameter for pvag.
ppvag	0.0 m^2	Cross-term scaling parameter for pvag.
lalpha0	0.0 m^2/V	Length scaling parameter for alpha0.

© 2023 Cadence Design Systems, Inc.

walpha0	0.0 m^2/V	Width scaling parameter for alpha0.
palpha0	0.0 m^3/V	Cross-term scaling parameter for alpha0.
lalpha1	0.0 m/V	Length scaling parameter for alpha1.
walpha1	0.0 m/V	Width scaling parameter for alpha1.
palpha1	0.0 m^2/V	Cross-term scaling parameter for alpha1.
lbeta0	0.0 m/V	Length scaling parameter for beta0.
wbeta0	0.0 m/V	Width scaling parameter for beta0.
pbeta0	0.0 m^2/V	Cross-term scaling parameter for beta0.
laigc	0.0 (F s^2/ g)^0.5	Length scaling parameter for aigc.
waigc	0.0 (F s^2/ g)^0.5	Width scaling parameter for aigc.
paigc	0.0 m (F s^2/ g)^0.5	Cross-term scaling parameter for aigc.
lbigc	0.0 V (F s^2/ g)^0.5	Length scaling parameter for bigc.
wbigc	0.0 V (F s^2/ g)^0.5	Width scaling parameter for bigc.
pbigc	0.0 m V (F s^2/ g)^0.5	Cross-term scaling parameter for bigc.

© 2023 Cadence Design Systems, Inc.

lcigc	0.0 m/V	Length scaling parameter for cigc.
wcigc	0.0 m/V	Width scaling parameter for cigc.
pcigc	0.0 (m^2)/V	Cross-term scaling parameter for cigc.
lpigcd	0.0 m	Length scaling parameter for pigcd.
wpigcd	0.0 m	Width scaling parameter for pigcd.
ppigcd	0.0 m^2	Cross-term scaling parameter for pigcd.
lagidl	0.0 m/ohm	Length scaling parameter for agidl.
wagidl	0.0 m/ohm	Width scaling parameter for agidl.
pagidl	0.0 (m^2)/ohm	Cross-term scaling parameter for agidl.
lbgidl	0.0 V	Length scaling parameter for bgidl.
wbgidl	0.0 V	Width scaling parameter for bgidl.
pbgidl	0.0 m V	Cross-term scaling parameter for bgidl.
legidl	0.0 m V	Length scaling parameter for egidl.
wegidl	0.0 m V	Width scaling parameter for egidl.
pegidl	0.0 (m^2) V	Cross-term scaling parameter for egidl.
lpgidl	0.0 m	Length scaling parameter for pgidl.
wpgidl	0.0 m	Width scaling parameter for pgidl.

© 2023 Cadence Design Systems, Inc.

ppgidl	0.0 m^2	Cross-term scaling parameter for pgidl.
lagisl	0.0 m/ ohm	Length scaling parameter for agisl.
wagisl	0.0 m/ ohm	Width scaling parameter for agisl.
pagisl	0.0 (m^2)/ohm	Cross-term scaling parameter for agisl.
lbgisl	0.0 V	Length scaling parameter for bgisl.
wbgisl	0.0 V	Width scaling parameter for bgisl.
pbgisl	0.0 m V	Cross-term scaling parameter for bgisl.
legisl	0.0 m V	Length scaling parameter for egisl.
wegisl	0.0 m V	Width scaling parameter for egisl.
pegisl	0.0 (m^2) V	Cross-term scaling parameter for egisl.
lpgisl	0.0 m	Length scaling parameter for pgisl.
wpgisl	0.0 m	Width scaling parameter for pgisl.
ppgisl	0.0 m^2	Cross-term scaling parameter for pgisl.
laigs	0.0 (F s^2/ g)^0.5	Length scaling parameter for aigs.
waigs	0.0 (F s^2/ g)^0.5	Width scaling parameter for aigs.

© 2023 Cadence Design Systems, Inc.

paigs	0.0 m (F s^2/ g)^0.5	Cross-term scaling parameter for aigs.
laigd	0.0 (F s^2/ g)^0.5	Length scaling parameter for aigd.
waigd	0.0 (F s^2/ g)^0.5	Width scaling parameter for aigd.
paigd	0.0 m (F s^2/ g)^0.5	Cross-term scaling parameter for aigd.
lbigs	0.0 ((F s^2/ g)^0.5)/ V	Length scaling parameter for bigs.
wbigs	0.0 ((F s^2/ g)^0.5)/ V	Width scaling parameter for bigs.
pbigs	0.0 (m (F s^2/ g)^0.5)/ V	Cross-term scaling parameter for bigs.
lbigd	0.0 ((F s^2/ g)^0.5)/ V	Length scaling parameter for bigd.
wbigd	0.0 ((F s^2/ g)^0.5)/ V	Width scaling parameter for bigd.

© 2023 Cadence Design Systems, Inc.

pbigd	0.0 (m (F s^2/ g)^0.5)/ V	Cross-term scaling parameter for bigd.
lcigs	0.0 m/V	Length scaling parameter for cigs.
wcigs	0.0 m/V	Width scaling parameter for cigs.
pcigs	0.0 (m^2)/V	Cross-term scaling parameter for cigs.
lcigd	0.0 m/V	Length scaling parameter for cigd.
wcigd	0.0 m/V	Width scaling parameter for cigd.
pcigd	0.0 m/V	Cross-term scaling parameter for cigd.
lntox	0.0 m	Length scaling parameter for ntox.
wntox	0.0 m	Width scaling parameter for ntox.
pntox	0.0 m^2	Cross-term scaling parameter for ntox.
lpoxedge	0.0 m	Length scaling parameter for poxedge.
wpoxedge	0.0 m	Width scaling parameter for poxedge.
ppoxedge	0.0 m	Cross-term scaling parameter for poxedge.
llovs	0.0 m^2	Length scaling parameter for lovs.
wlovs	0.0 m^2	Width scaling parameter for lovs.
plovs	0.0 m^3	Cross-term scaling parameter for lovs.
llovd	0.0 m^2	Length scaling parameter for lovd.
wlovd	0.0 m^2	Width scaling parameter for lovd.

© 2023 Cadence Design Systems, Inc.

plovd	0.0 m^3	Cross-term scaling parameter for lovd.
lcfs	0.0 F	Length scaling parameter for cfs.
wcfs	0.0 F	Width scaling parameter for cfs.
pcfs	0.0 F m	Cross-term scaling parameter for cfs.
lcfd	0.0 F	Length scaling parameter for cfd.
wcfd	0.0 F	Width scaling parameter for cfd.
pcfd	0.0 F m	Cross-term scaling parameter for cfd.
lvsat	0.0 $(m^2)/s$	Length scaling parameter for vsat.
wvsat	0.0 $(m^2)/s$	Width scaling parameter for vsat.
pvsat	0.0 $(m^3)/s$	Cross-term scaling parameter for vsat.
lvsatb	0.0 m/V	Length scaling parameter for vsatb.
wvsatb	0.0 m/V	Width scaling parameter for vsatb.
pvsatb	0.0 $(m^2)/V$	Cross-term scaling parameter for vsatb.
lvsat1	0.0 $(m^2)/s$	Length scaling parameter for vsat1.
wvsat1	0.0 $(m^2)/s$	Width scaling parameter for vsat1.
pvsat1	0.0 $(m^3)/s$	Cross-term scaling parameter for vsat1.

© 2023 Cadence Design Systems, Inc.

lvsatcv	0.0 $(m^2)/s$	Length scaling parameter for vsatcv.
wvsatcv	0.0 $(m^2)/s$	Width scaling parameter for vsatcv.
pvsatcv	0.0 $(m^3)/s$	Cross-term scaling parameter for vsatcv.
lksativ	0.0 m	Length scaling parameter for ksativ.
wksativ	0.0 m	Width scaling parameter for ksativ.
pksativ	0.0 m^2	Cross-term scaling parameter for ksativ.
lksubiv	0.0 m	Length scaling parameter for ksubiv.
wksubiv	0.0 m	Width scaling parameter for ksubiv.
pksubiv	0.0 m^2	Cross-term scaling parameter for ksubiv.
lup	0.0 m^(LPA+1)	Length scaling parameter for up.
wup	0.0 m^(LPA+1)	Width scaling parameter for up.
pup	0.0 m^(LPA+2)	Cross-term scaling parameter for up.
laigbinv	0.0 (F s^2/ g)^0.5	Length scaling parameter for aigbinv.

© 2023 Cadence Design Systems, Inc.

waigbinv	0.0 (F s^2/ g)^0.5	Width scaling parameter for aigbinv.
paigbinv	0.0 m (F s^2/ g)^0.5	Cross-term scaling parameter for aigbinv.
lbigbinv	0.0 ((F s^2/ g)^0.5)V ^-1	Length scaling parameter for bigbinv.
wbigbinv	0.0 ((F s^2/ g)^0.5)V ^-1	Width scaling parameter for bigbinv.
pbigbinv	0.0 (m ((F s^2/ g)^0.5)V ^-1)	Cross-term scaling parameter for bigbinv.
lcigbinv	0.0 m/V	Length scaling parameter for cigbinv.
wcigbinv	0.0 m/V	Width scaling parameter for cigbinv.
pcigbinv	0.0 (m^2)/V	Cross-term scaling parameter for cigbinv.
leigbinv	0.0 m V	Length scaling parameter for eigbinv.
weigbinv	0.0 m V	Width scaling parameter for eigbinv.
peigbinv	0.0 (m^2) V	Cross-term scaling parameter for eigbinv.
lnigbinv	0.0 m	Length scaling parameter for nigbinv.

© 2023 Cadence Design Systems, Inc.

wnigbinv	0.0 m	Width scaling parameter for nigbinv.
pnigbinv	0.0 m^2	Cross-term scaling parameter for nigbinv.
laigbacc	0.0 (F s^2/ g)^0.5	Length scaling parameter for aigbacc.
waigbacc	0.0 (F s^2/ g)^0.5	Width scaling parameter for aigbacc.
paigbacc	0.0 m (F s^2/ g)^0.5	Cross-term scaling parameter for aigbacc.
lbigbacc	0.0 ((F s^2/ g)^0.5)V ^-1	Length scaling parameter for bigbacc.
wbigbacc	0.0 ((F s^2/ g)^0.5)V ^-1	Width scaling parameter for bigbacc.
pbigbacc	0.0 (m ((F s^2/ g)^0.5)V ^-1)	Cross-term scaling parameter for bigbacc.
lcigbacc	0.0 m/V	Length scaling parameter for cigbacc.
wcigbacc	0.0 m/V	Width scaling parameter for cigbacc.
pcigbacc	0.0 (m^2)/V	Cross-term scaling parameter for cigbacc.
lnigbacc	0.0 m	Length scaling parameter for nigbacc.

© 2023 Cadence Design Systems, Inc.

wnigbacc	0.0 m	Width scaling parameter for nigbacc.
pnigbacc	0.0 m^2	Cross-term scaling parameter for nigbacc.
lbpfactorpw	0.0	L-term of BPFACTORPW.
wbpfactorpw	0.0	W-term of BPFACTORPW.
pbpfactorpw	0.0	P-term of BPFACTORPW.
lvknee1pw	0.0 V	L-term of VKNEE1PW.
wvknee1pw	0.0 V	W-term of VKNEE1PW.
pvknee1pw	0.0 V	P-term of VKNEE1PW.
lvknee2pw	0.0 V	L-term of VKNEE2PW.
wvknee2pw	0.0 V	W-term of VKNEE2PW.
pvknee2pw	0.0 V	P-term of VKNEE2PW.
ldbgpw	0.0	L-term of DBGPW.
wdbgpw	0.0	W-term of DBGPW.
pdbgpw	0.0	P-term of DBGPW.
lkbg0pw	0.0	L-term of KBG0PW.
wkbg0pw	0.0	W-term of KBG0PW.
pkbg0pw	0.0	P-term of KBG0PW.
lkbg1pw	0.0	L-term of KBG1PW.
wkbg1pw	0.0	W-term of KBG1PW.

© 2023 Cadence Design Systems, Inc.

pkbg1pw	0.0	P-term of KBG1PW.
lkbg2pw	0.0	L-term of KBG2PW.
wkbg2pw	0.0	W-term of KBG2PW.
pkbg2pw	0.0	P-term of KBG2PW.
lbpfactornw	0.0	L-term of BPFACTORNW.
wbpfactornw	0.0	W-term of BPFACTORNW.
pbpfactornw	0.0	P-term of BPFACTORNW.
lvknee1nw	0.0 V	L-term of VKNEE1NW.
wvknee1nw	0.0 V	W-term of VKNEE1NW.
pvknee1nw	0.0 V	P-term of VKNEE1NW.
lvknee2nw	0.0 V	L-term of VKNEE2NW.
wvknee2nw	0.0 V	W-term of VKNEE2NW.
pvknee2nw	0.0 V	P-term of VKNEE2NW.
ldbgnw	0.0	L-term of DBGNW.
wdbgnw	0.0	W-term of DBGNW.
pdbgnw	0.0	P-term of DBGNW.
lkbg0nw	0.0	L-term of KBG0NW.
wkbg0nw	0.0	W-term of KBG0NW.
pkbg0nw	0.0	P-term of KBG0NW.

© 2023 Cadence Design Systems, Inc.

lkbg1nw	0.0	L-term of KBG1NW.
wkbg1nw	0.0	W-term of KBG1NW.
pkbg1nw	0.0	P-term of KBG1NW.
lkbg2nw	0.0	L-term of KBG2NW.
wkbg2nw	0.0	W-term of KBG2NW.
pkbg2nw	0.0	P-term of KBG2NW.
ldsc0	0.0	L-term of DSC0.
wdsc0	0.0	W-term of DSC0.
pdsc0	0.0	P-term of DSC0.
ldsc1	0.0	L-term of DSC1.
wdsc1	0.0	W-term of DSC1.
pdsc1	0.0	P-term of DSC1.
lascl	0.0	L-term of ASCL.
wascl	0.0	W-term of ASCL.
pascl	0.0	P-term of ASCL.
lbscl	0.0 V^-1	L-term of BSCL.
wbscl	0.0 V^-1	W-term of BSCL.
pbscl	0.0 V^-1	P-term of BSCL.
letamob	0.0	L-term of ETAMOB.

© 2023 Cadence Design Systems, Inc.

wetamob	0.0	W-term of ETAMOB.
petamob	0.0	P-term of ETAMOB.
lvbgidl	0.0 m	L-term of VBGIDL.
wvbgidl	0.0 m	W-term of VBGIDL.
pvbgidl	0.0 m^2	P-term of VBGIDL.
lvbegidl	0.0 m V	L-term of VBEGIDL.
wvbegidl	0.0 m V	W-term of VBEGIDL.
pvbegidl	0.0 (m^2) V	P-term of VBEGIDL.
lvbgisl	0.0 m	L-term of VBGISL.
wvbgisl	0.0 m	W-term of VBGISL.
pvbgisl	0.0 m^2	P-term of VBGISL.
lvbegisl	0.0 m V	L-term of VBEGISL.
wvbegisl	0.0 m V	W-term of VBEGISL.
pvbegisl	0.0 (m^2) V	P-term of VBEGISL.
lxrcrg1	0.0	L-term of XRCRG1.
wxrcrg1	0.0	W-term of XRCRG1.
pxrcrg1	0.0	P-term of XRCRG1.
lxrcrg2	0.0	L-term of XRCRG2.

© 2023 Cadence Design Systems, Inc.

wxrcrg2	0.0	W-term of XRCRG2.
pxrcrg2	0.0	P-term of XRCRG2.
eta1	0.00	DIBL coefficient for low gate overdrive.
digc	1.0	Parameter for Igc in inversion.
digs	1.0	Parameter for Igs, Igd.
digd	1.0	Parameter for Igs, Igd.
leta1	0.0 m	L-term of ETA1.
weta1	0.0 m	W-term of ETA1.
peta1	0.0 m	P-term of ETA1.
ldigc	0.0 m/V	L-term of DIGC.
wdigc	0.0 m/V	W-term of DIGC.
pdigc	0.0 $(m^2)/V$	P-term of DIGC.
ldigs	0.0 m/V	L-term of DIGS.
wdigs	0.0 m/V	W-term of DIGS.
pdigs	0.0 $(m^2)/V$	P-term of DIGS.
ldigd	0.0 m/V	L-term of DIGD.
wdigd	0.0 m/V	W-term of DIGD.
pdigd	0.0 $(m^2)/V$	P-term of DIGD.

© 2023 Cadence Design Systems, Inc.

lqmtcencv	0.0	L-term of QMTCENCV.
wqmtcencv	0.0	W-term of QMTCENCV.
pqmtcencv	0.0	P-term of QMTCENCV.
letaqm	0.0	L-term of ETAQM.
wetaqm	0.0	W-term of ETAQM.
petaqm	0.0	P-term of ETAQM.
lqm0	0.0	L-term of QM0.
wqm0	0.0	W-term of QM0.
pqm0	0.0	P-term of QM0.
lpqm	0.0	L-term of PQM.
wpqm	0.0	W-term of PQM.
ppqm	0.0	P-term of PQM.

© 2023 Cadence Design Systems, Inc.

Safe operating areas parameters

vds_max	infinity V	Maximum allowed voltage cross drain and source.
vgd_max	infinity V	Maximum allowed voltage cross front gate and drain.
vgs_max	infinity V	Maximum allowed voltage cross front gate and source.
vbd_max	infinity V	Maximum allowed voltage cross back gate and drain.
vbs_max	vbd_max V	Maximum allowed voltage cross back gate and source.
vgb_max	infinity V	Maximum allowed voltage cross front gate and back gate.
vgdr_max	vgd_max V	Maximum allowed reverse voltage cross front gate and drain.
vgsr_max	vgs_max V	Maximum allowed reverse voltage cross front gate and source.
vgbr_max	vgb_max V	Maximum allowed reverse voltage cross front gate and back gate.
vbsr_max	vbs_max V	Maximum allowed reverse voltage cross back gate and source.
vbdr_max	vbd_max V	Maximum allowed reverse voltage cross back gate and drain.
trise	0.0 C	Temperature rise from ambient, alias of dtemp. It served as the default value of instance trise.

© 2023 Cadence Design Systems, Inc.

igflag	0	Enable version 102.9.1 Igate model: 0 = OFF(backward compatible with version 102.8.0), 1 = ON.
fnmod	0	Flicker noise model 0: Old, 1: Improved.
convmod	1	Enable bug fixes related to non-convergence issues in version 102.9.2: 0 = OFF, 1 = ON.
rsc	0 ohm	Source contact resistance.
rdc	0 ohm	Drain contact resistance.
trs	0 K^-1	TEMP Dependence of Source contact resistance.
trd	0 K^-1	TEMP Dependence of Drain contact resistance.
noia2	6.250e+39 eV^-1 s^1-EF m^{-3}	Noise parameter for FNMOD=1.
smooth	2	Smoothing Parameter.
mpower	1.2	Sub-threshold to strong inversion transition slope Parameter.
qsref	50.0e-3 C m^{-2}	Charge at threshold condition.
lnoia2	0.0	L-term of NOIA2.
wnoia2	0.0	W-term of NOIA2.
pnoia2	0.0	P-term of NOIA2.
lmpower	0.0	L-term of MPOWER.
wmpower	0.0	W-term of MPOWER.

© 2023 Cadence Design Systems, Inc.

pmpower	0.0	P-term of MPOWER.
lqsref	0.0	L-term of QSREF.
wqsref	0.0	W-term of QSREF.
pqsref	0.0	P-term of QSREF.

Output Parameters

meff		Effective multiplicity factor (m-factor).
leff	(m)	Effective channel length.
weff	(m)	Effective channel width.
tempeff	(C)	Effective temperature without selfheating temperature.

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

ad	I-6	kt1l	M-260	pbpfactornw	M-606	ucs	M-147
advtp0	M-74	kt2	M-261	pbpfactorpw	M-585	ucste	M-153
advtp1	M-76	kt2l	M-262	pbscl	M-636	ud	M-140

© 2023 Cadence Design Systems, Inc.

aeu M-135
agidl M-210
agisl M-206
aigbacc M-187
aigbinv M-182
aigc M-191
aigd M-200
aigs M-195
alpha0 M-218
alpha1 M-219
amexp M-106
apclm M-176
aptwg M-109
aptwgb M-117
aptwgb2 M-119
ardsw M-157
ardw M-165
arsw M-161
as I-5
ascl M-57
at M-111
l I-2
l M-1
lagidl M-475
lagisl M-487
laigbacc M-571
laigbinv M-556
laigc M-463
laigd M-502
laigs M-499
lalpha0 M-454
lalpha1 M-457
lascl M-631
lat M-415
latb M-418
lbeta0 M-460
lbgidl M-478
lbgisl M-490
lbigbacc M-574
lbigbinv M-559
lbigc M-466
lbigd M-508
pcbgcbg M-330
pcdsc M-324
pcdscd M-327
pcfd M-534
pcfs M-531
pcigbacc M-579
pcigbinv M-564
pcigc M-471
pcigd M-516
pcigs M-513
pcit M-321
pclm M-175
pclmcv M-179
pclmg M-178
pcovbd0 M-232
pcovbd1 M-233
pcovbs0 M-230
pcovbs1 M-231
pd I-8
pdbgnw M-615
pdbgpw M-594
ud1 M-152
udb M-143
up M-129
ute M-148
utl M-149
vbd_max M-689
vbdr_max M-696
vbegidl M-217
vbegisl M-215
vbgidl M-216
vbgisl M-214
vbs_max M-690
vbsr_max M-695
vdb OP-15
vds OP-13
vds_max M-686
vdsat_c M-279
vdsat_vadj M-281
vdsat_vdl M-280
vdsatmod M-278
vdssat OP-7

© 2023 Cadence Design Systems, Inc.

atb M-122
atbl M-123
atl M-112
aua M-132
auc M-138
aud M-141
audb M-144
avsat M-94
avsat1 M-97
avsatb M-124
avsatcv M-100
bdvtp0 M-75
bdvtp1 M-77
beta0 M-220
beu M-136
bg0sub M-51
bgidl M-211
bgisl M-207
bigbacc M-188
bigbinv M-183
lbigs M-505
lbpfactornw M-604
lbpfactorpw M-583
lbscl M-634
lcbgcbg M-328
lcdsc M-322
lcdscd M-325
lcfd M-532
lcfs M-529
lcigbacc M-577
lcigbinv M-562
lcigc M-469
lcigd M-514
lcigs M-511
lcit M-319
ldbgnw M-613
ldbgpw M-592
ldigc M-665
ldigd M-671
ldigs M-668
pdibl1 M-171
pdibl2 M-172
pdigc M-667
pdigd M-673
pdigs M-670
pdrout M-444
pdsc0 M-627
pdsc1 M-630
pdsub M-348
pdvt0 M-333
pdvt1 M-336
pegidl M-483
pegisl M-495
peigbinv M-567
peta0 M-342
peta1 M-664
petab M-345
petamob M-639
petaqm M-679
peu M-399
version M-9
vgb_max M-691
vgbr_max M-694
vgd OP-12
vgd_max M-687
vgdr_max M-692
vgs OP-11
vgs_max M-688
vgsr_max M-693
vknee1nw M-246
vknee1pw M-239
vknee2nw M-247
vknee2pw M-240
vsat M-93
vsat1 M-96
vsatb M-121
vsatcv M-99
vsb OP-14
vth OP-58
vthmod M-273

© 2023 Cadence Design Systems, Inc.

bigc M-192
bigd M-201
bigs M-196
bmexp M-107
bpclm M-177
bpfactornw M-245
bpfactorpw M-238
bptwg M-110
bptwgb M-118
bptwgb2 M-120
brdsw M-158
brdw M-166
brsw M-162
bscl M-58
bua M-133
buc M-139
bud M-142
budb M-145
bvsat M-95
bvsat1 M-98
bvsatb M-125
ldrout M-442
ldsc0 M-625
ldsc1 M-628
ldsub M-346
ldvt0 M-331
ldvt1 M-334
legidl M-481
legisl M-493
leigbinv M-565
leta0 M-340
leta1 M-662
letab M-343
letamob M-637
letaqm M-677
leu M-397
ligt M-433
liit M-424
lint M-21
lintnoi M-254
lk0 M-355
lk01 M-358
pgidl M-213
pgisl M-209
phig1 M-53
phig2 M-54
phin M-69
pigcd M-194
pigt M-435
piit M-426
pk0 M-357
pk01 M-360
pk0si M-363
pk0si1 M-366
pk1rsce M-351
pkbg0nw M-618
pkbg0pw M-597
pkbg1nw M-621
pkbg1pw M-600
pkbg2nw M-624
pkbg2pw M-603
pksativ M-549
pksubiv M-552
w I-3
w M-2
wagidl M-476
wagisl M-488
waigbacc M-572
waigbinv M-557
waigc M-464
waigd M-503
waigs M-500
walpha0 M-455
walpha1 M-458
wascl M-632
wat M-416
watb M-419
wbeta0 M-461
wbgidl M-479
wbgisl M-491
wbigbacc M-575
wbigbinv M-560
wbigc M-467
wbigd M-509

© 2023 Cadence Design Systems, Inc.

bvsatcv M-101
cbb OP-28
cbbi OP-48
cbd OP-25
cbdi OP-45
cbg OP-26
cbgcbg M-64
cbgcbg0 M-62
cbgcbg0p M-63
cbgcbgd M-66
cbgcbgp M-65
cbgi OP-46
cbs OP-27
cbsi OP-47
cdb OP-32
cdbi OP-52
cdd OP-29
cddi OP-49
cdg OP-30
cdgi OP-50
lk0si M-361
lk0si1 M-364
lk1rsce M-349
lkbg0nw M-616
lkbg0pw M-595
lkbg1nw M-619
lkbg1pw M-598
lkbg2nw M-622
lkbg2pw M-601
lksativ M-547
lksubiv M-550
ll M-22
llc M-34
lln M-25
llovd M-526
llovs M-523
llpe0 M-352
lmax M-5
lmexp M-367
lmin M-4
plovd M-528
plovs M-525
plpe0 M-354
pmexp M-369
pmpower M-714
pnbody M-318
pnigbacc M-582
pnigbinv M-570
pnoia2 M-711
pnsd M-315
pntox M-519
poxedge M-205
ppclm M-438
ppclmcv M-441
ppdibl1 M-447
ppdibl2 M-450
ppgidl M-486
ppgisl M-498
pphig1 M-309
pphig2 M-312
wbigs M-506
wbpfactornw M-605
wbpfactorpw M-584
wbscl M-635
wcbgcbg M-329
wcdsc M-323
wcdscd M-326
wcfd M-533
wcfs M-530
wcigbacc M-578
wcigbinv M-563
wcigc M-470
wcigd M-515
wcigs M-512
wcit M-320
wdbgnw M-614
wdbgpw M-593
wdigc M-666
wdigd M-672
wdigs M-669

© 2023 Cadence Design Systems, Inc.

cds OP-31
cdsc M-60
cdscd M-61
cdsi OP-51
cfd M-224
cfs M-223
cgb OP-24
cgbi OP-44
cgd OP-21
cgdi OP-41
cgdl M-226
cgg OP-22
cggi OP-42
cgs OP-23
cgsi OP-43
cgsl M-225
chargemod M-11
chargewf M-154
cigbacc M-189
cigbinv M-184
cigc M-193
lmpower M-712
lnbody M-316
lnigbacc M-580
lnigbinv M-568
lnoia2 M-709
lnsd M-313
lntox M-517
lovd M-222
lovs M-221
lpa M-130
lpclm M-436
lpclmcv M-439
lpdibl1 M-445
lpdibl2 M-448
lpe0 M-81
lpgidl M-484
lpgisl M-496
lphig1 M-307
lphig2 M-310
lphin M-337
lpigcd M-472
pphin M-339
ppigcd M-474
ppoxedge M-522
ppqm M-685
pprt M-423
pprwb M-303
pprwg M-300
pptwg M-372
pptwgb M-375
pptwgb2 M-378
pptwgt M-381
ppvag M-453
pqm M-91
pqm0 M-682
pqmtcencv M-676
pqsref M-717
prdsw M-291
prdw M-294
prsw M-297
prt M-170
prwb M-168
wdrout M-443
wdsc0 M-626
wdsc1 M-629
wdsub M-347
wdvt0 M-332
wdvt1 M-335
wegidl M-482
wegisl M-494
weigbinv M-566
welltype M-10
weta0 M-341
weta1 M-663
wetab M-344
wetamob M-638
wetaqm M-678
weu M-398
wigt M-434
wiit M-425
wint M-27
wk0 M-356
wk01 M-359

© 2023 Cadence Design Systems, Inc.

cigd M-202
cigs M-197
cit M-59
ckappad M-228
ckappas M-227
compatible M-272
convmod M-700
csb OP-36
csbi OP-56
csd OP-33
csdbgsw M-229
csdi OP-53
csg OP-34
csgi OP-54
css OP-35
cssi OP-55
cth0 M-269
dbgnw M-244
dbgpw M-237
deltavsat M-102
delvtrand I-14
lpoxedge M-520
lpqm M-683
lprt M-421
lprwb M-301
lprwg M-298
lptwg M-370
lptwgb M-373
lptwgb2 M-376
lptwgt M-379
lpvag M-451
lqm0 M-680
lqmtcencv M-674
lqsref M-715
lrdsw M-289
lrdw M-292
lrsw M-295
ltgidl M-427
ltgisl M-430
lu0 M-382
lua M-385
lua1 M-406
prwg M-167
ps I-7
ptgidl M-429
ptgisl M-432
ptwg M-108
ptwgb M-115
ptwgb2 M-116
ptwgt M-114
pu0 M-384
pua M-387
pua1 M-408
puc M-390
pucs M-396
pucste M-414
pud M-393
pud1 M-411
pup M-555
pute M-405
putl M-402
pvag M-174
pvbegidl M-645
wk0si M-362
wk0si1 M-365
wk1rsce M-350
wkbg0nw M-617
wkbg0pw M-596
wkbg1nw M-620
wkbg1pw M-599
wkbg2nw M-623
wkbg2pw M-602
wksativ M-548
wksubiv M-551
wl M-28
wlc M-38
wln M-31
wlovd M-527
wlovs M-524
wlpe0 M-353
wmax M-7
wmexp M-368
wmin M-6
wmpower M-713

© 2023 Cadence Design Systems, Inc.

digc M-659
digd M-661
digs M-660
dlc M-33
dlcigd M-199
dlcigs M-198
dmobclamp M-146
drout M-173
dsc0 M-82
dsc1 M-83
dsub M-71
dtemp I-12
dtox1 M-44
dvsatclamp M-126
dvt0 M-67
dvt1 M-68
dvtp0 M-72
dvtp1 M-73
dvtp2 M-78
dwc M-37
easub M-49
luc M-388
lucs M-394
lucste M-412
lud M-391
lud1 M-409
lup M-553
lute M-403
lutl M-400
lvbegidl M-643
lvbegisl M-649
lvbgidl M-640
lvbgisl M-646
lvknee1nw M-607
lvknee1pw M-586
lvknee2nw M-610
lvknee2pw M-589
lvsat M-535
lvsat1 M-541
lvsatb M-538
lvsatcv M-544
lw M-23
pvbegisl M-651
pvbgidl M-642
pvbgisl M-648
pvknee1nw M-609
pvknee1pw M-588
pvknee2nw M-612
pvknee2pw M-591
pvsat M-537
pvsat1 M-543
pvsatb M-540
pvsatcv M-546
pwr M-306
pwr OP-59
pxrcrg1 M-654
pxrcrg2 M-657
qb OP-18
qbi OP-38
qd OP-19
qdi OP-39
qg OP-17
qgi OP-37
wnbody M-317
wnigbacc M-581
wnigbinv M-569
wnoia2 M-710
wnsd M-314
wntox M-518
wpclm M-437
wpclmcv M-440
wpdibl1 M-446
wpdibl2 M-449
wpgidl M-485
wpgisl M-497
wphig1 M-308
wphig2 M-311
wphin M-338
wpigcd M-473
wpoxedge M-521
wpqm M-684
wprt M-422
wprwb M-302
wprwg M-299

© 2023 Cadence Design Systems, Inc.

ef M-248
egidl M-212
egisl M-208
eigbinv M-185
em M-249
eot1 M-41
eot1p M-43
eot2 M-42
epsrox1 M-56
epsrsub M-55
eta0 M-70
eta1 M-658
etab M-79
etamob M-128
etaqm M-89
eu M-134
fnmod M-699
gds OP-9
gdsmin M-288
gidlmod M-13
gm OP-8
lwc M-35
lwl M-24
lwlc M-36
lwn M-26
lwr M-304
lx51 OP-63
lxrcrg1 M-652
lxrcrg2 M-655
m I-1
meff O-1
mexp M-105
minr M-271
mpower M-707
nbg M-48
nbody M-46
nc0sub M-52
nf I-4
nf M-3
nfmod M-19
ngcon M-284
ni0sub M-50
qm0 M-90
qmtcencv M-88
qs OP-20
qsi OP-40
qsref M-708
rdc I-16
rdc M-702
rdsmod M-12
rdsw M-156
rdswmin M-155
rdw M-164
rdwmin M-163
region OP-57
rgatemod M-17
ron OP-65
rout OP-66
rsc I-17
rsc M-701
rshd M-181
rshg M-285
rshs M-180
wptwg M-371
wptwgb M-374
wptwgb2 M-377
wptwgt M-380
wpvag M-452
wqm0 M-681
wqmtcencv M-675
wqsref M-716
wr M-169
wrdsw M-290
wrdw M-293
wrsw M-296
wtgidl M-428
wtgisl M-431
wth0 M-270
wu0 M-383
wua M-386
wua1 M-407
wuc M-389
wucs M-395
wucste M-413

© 2023 Cadence Design Systems, Inc.

gmbs OP-10
id OP-1
ids OP-16
ig OP-2
igbmod M-15
igcmod M-14
igflag M-698
igidl OP-5
igisl OP-6
igt M-266
iii OP-4
iit M-263
is OP-3
isnoisy I-18
ivth M-274
ivth_vdsmin M-277
ivthl M-276
ivthw M-275
k0 M-84
k01 M-85
nigbacc M-190
nigbinv M-186
noia M-250
noia2 M-705
noib M-251
noic M-252
nqsmod M-18
nrd I-10
nrs I-9
nsd M-47
ntnoi M-253
ntox M-204
pagidl M-477
pagisl M-489
paigbacc M-573
paigbinv M-558
paigc M-465
paigd M-504
paigs M-501
palpha0 M-456
rsw M-160
rswmin M-159
rth0 M-268
sft OP-62
shmod M-16
smooth M-706
t_delta_sh OP-64
t_total_c OP-61
t_total_k OP-60
tbgasub M-257
tbgbsub M-258
tempeff O-2
teta0 M-267
tgidl M-264
tgisl M-265
tmaxc M-256
tmexp M-113
tnom M-255
toxp M-92
toxref M-203
wud M-392
wud1 M-410
wup M-554
wute M-404
wutl M-401
wvbegidl M-644
wvbegisl M-650
wvbgidl M-641
wvbgisl M-647
wvknee1nw M-608
wvknee1pw M-587
wvknee2nw M-611
wvknee2pw M-590
wvsat M-536
wvsat1 M-542
wvsatb M-539
wvsatcv M-545
ww M-29
wwc M-39
wwl M-30

© 2023 Cadence Design Systems, Inc.

k0si M-86
k0si1 M-87
k1rsce M-80
kbg0nw M-241
kbg0pw M-234
kbg1nw M-242
kbg1pw M-235
kbg2nw M-243
kbg2pw M-236
ksativ M-103
ksubiv M-104
kt1 M-259
palpha1 M-459
pascl M-633
pat M-417
patb M-420
pbeta0 M-462
pbgidl M-480
pbgisl M-492
pbigbacc M-576
pbigbinv M-561
pbigc M-468
pbigd M-510
pbigs M-507
trd M-704
trise I-13
trise M-697
trs M-703
tsi M-45
type M-8
u0 M-127
u0mult I-15
ua M-131
ua1 M-150
uc M-137
uc1 M-151
wwlc M-40
wwn M-32
wwr M-305
wxrcrg1 M-653
wxrcrg2 M-656
xgl M-283
xgw M-282
xl I-11
xrcrg1 M-286
xrcrg2 M-287
xw M-20

© 2023 Cadence Design Systems, Inc.

48

Angelov Model

The Angelov model is an empirical equation-based large signal model that is used for III-V field effect transistors, such as HEMT and MESFET. This model can be used for GaAs and other HEMT devices. An enhancement version of Angelov model, which was developed by L.S. Liu, J.G. Ma, and G.I. Ng, is also integrated into this model, which improves both model accuracy and convergence. The enhancement version is called as MA (modified Angelov) model, which can be turned on with model parameter `ma_mod=1`.

Related Topics

Model Equations

Release History and Version

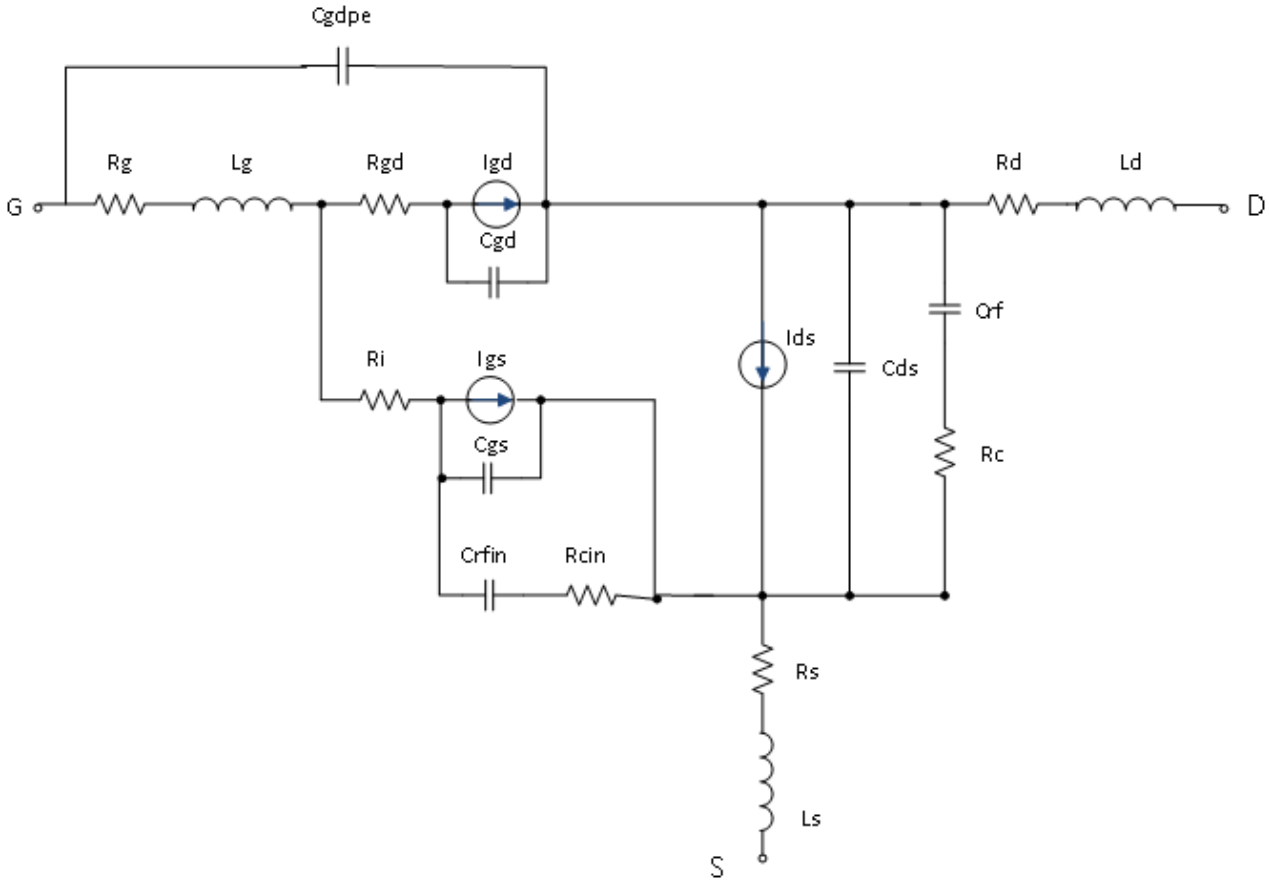
Model Usage

Model Usage

© 2023 Cadence Design Systems, Inc.

Model Equations

Equivalent Circuit



Ids Equations

(48-1)

$$P1m = P1 \cdot (1 + B1/(\cosh(B2 \cdot Vds) \cdot \cosh(B2 \cdot Vds)))$$

(48-2)

$$Vpkm = VPKS - DVPKS + DVPKS \cdot \tanh(ALPHA \cdot Vds) - VSB2 \cdot (Vdg - VTR)^2$$

© 2023 Cadence Design Systems, Inc.

(48-3)

$$\psi = P1m \cdot ((Vgs - Vpkm) + P2 \cdot (Vgs - Vpkm)^2 + P3 \cdot (Vgs - Vpkm)^3)$$

(48-4)

$$\alpha = ALPHAR + ALPHAS \cdot (1 + \tanh(\psi))$$

For original model (`idsmod=0`)

(48-5)

$$Ids = IPK0 \cdot (1 + \tanh(\psi)) \cdot \tanh(\alpha \cdot Vds) \cdot (1 + LAMBDA \cdot Vds + LSB0 \cdot \exp(Vdg - VTR))$$

For the symmetric model (`idsmod=1`)

(48-6)

$$\psi_n = P1m \cdot ((Vgd - Vpkm) + P2 \cdot (Vgd - Vpkm)^2 + P3 \cdot (Vgd - Vpkm)^3)$$

(48-7)

$$\alpha_n = ALPHAR + ALPHAS \cdot (1 + \tanh(\psi_n))$$

(48-8)

$$\lambda_n = LAMBDA + LVG \cdot (1 + \tanh(\psi_n))$$

(48-9)

$$\lambda_p = LAMBDA + LVG \cdot (1 + \tanh(\psi_p))$$

(48-10)

$$\lambda_{n1} = LAMBDA1 + LVG \cdot (1 + \tanh(\psi_n))$$

© 2023 Cadence Design Systems, Inc.

(48-11)

$$\lambda_{p1} = LAMBDA1 + LVG \cdot (1 + \tanh(\psi_p))$$

(48-12)

$$Idsp = IPK0 \times (1 + \tanh(\psi)) \times (1 + \tanh(\alpha \times Vds)) \times \left(1 + \lambda_p \times Vds + \lambda_{p1} \times \exp\left(\frac{Vds}{Vkn} - 1\right)\right)$$

(48-13)

$$Idsn = IPK0 \times (1 + \tanh(\psi_n)) \times (1 - \tanh(\alpha_n \times Vds)) \times \left(1 - \lambda_n \times Vds - \lambda_{n1} \times \exp\left(\frac{Vds}{Vkn} - 1\right)\right)$$

(48-14)

$$Ids = 0.5 \times (Idsp - Idsn)$$

MA Model

I*ds=Ids1*Ids2*

(48-15)

$$Ids2 = \tanh(\alpha_n \times Vds)(1 + \lambda_n \cdot Vds + LSB0 \cdot \exp(Vdg - VTR))$$

For idsmod=0

phi1=P1m((Vgs-Vpkm) + P2*(Veffp1)^2+P3*(Veffp1)^3+P2*(Veffp2)^2+P3(Veffp2)^3*

Ids1=IPK0(1+tanh(phi1))*

For idsmod=1

*ph1=P1m * Veffp1 + P2*(Veffp1)^2 + P3*(Veffp1)^3*

*ph2=P1m * Veffp2 + P2*(Veffp2)^2 + P3*(Veffp2)^3*

Ids1=IPK0(1+tanh(ph1) + tanh(ph2))*

© 2023 Cadence Design Systems, Inc.

Igs and Igd Equations

When `igmod=0`

(48-16)

$$Igs = IJ \times (\exp(PG \times \tanh(2 \times (Vgsc - VJG))) - \exp(PG \times \tanh(-2 \times VJG)))$$

(48-17)

$$Igd = IJ \times (\exp(PG \times \tanh(2 \times (Vgdc - VJG))) - \exp(PG \times \tanh(-2 \times VJG)))$$

When `igmod=1`

(48-18)

$$Igs = IJ \times (\exp(PG \times \tanh(Vgsc - VJG)) - \exp(-PG \times VJG))$$

(48-19)

$$Igd = IJ \times (\exp(PG \times \tanh(Vgdc - VJG)) - \exp(-PG \times VJG))$$

Temperature Equations

(48-20)

$$Ipk0 = IPK0 \times (1 + TCIPK0 \times (Temp - Tnom))$$

(48-21)

$$P1 = P1 \times (1 + TCP1 \times (Temp - Tnom))$$

(48-22)

$$Lsb0 = LSB0 \times (1 + TCLSB0 \times (Temp - Tnom))$$

(48-23)

$$Cgs0 = CGS0 \times (1 + TCGS0 \times (Temp - Tnom))$$

© 2023 Cadence Design Systems, Inc.

(48-24)

$$Cgd0 = CGD0 \times (1 + TCGD0 \times (Temp - Tnom))$$

(48-25)

$$Rc = RC \times (1 + TCRC \times (Temp - Tnom))$$

(48-26)

$$Crf = CRF \times (1 + TCCRF \times (Temp - Tnom))$$

Charge Equations

(48-27)

$$Phi1 = P10 + P11 \times Vgsc + P111 \times Vds$$

(48-28)

$$Phi2 = P20 + P21 \times Vds$$

(48-29)

$$Phi3 = P30 - P31 \times Vds$$

(48-30)

$$Phi4 = P40 + P41 \times Vgdc - P111 \times Vds$$

For `capmod=0`

```
Cgs = CGSP
Cgd = CGDP
Qgs = CGSP * Vgsc
Qgd = CGDP * Vgdc
```

For `capmod=1`

```
Cgs = CGSP+CGS0 x ( 1 + tanh(Phi1))( 1 + tanh(Phi2))
Cgd = CGDP + CGD0 x ((1 - P111 + tanh(Phi3)) (1 + tanh(Phi4)) + 2 x P111)
```


© 2023 Cadence Design Systems, Inc.

```
Qgs = CGSP x Vgsc
Qgd = CGDP x Vgdc
```

For `capmod=2`

```
Lc1 = 1n(cosh(Phi1))
Lc10 = ln(cosh(P10 + P11 X Vds))
Qgs = CGSP x Vgsc + CGS0 x ((Phi1 + Lc1 - Qgs0) x (1 + tanh(Phi2)) / P11 + 2 x P111
x Vgsc
Qgs0 = P10 + P111 x Vds + Lc10
Lc4 = 1n(cosh(Phi4))
Lc40 = 1n(cosh(P40 -P111 x Vds))
Qgd = CGDP x Vgdc + CGD0 x ((Phi4 + Lc4 - Qgd0) x (1 - P111 + tanh(Phi3)) / P41 +
2 x P111 x Vgdc
Qgd0 = P40 - P111 x Vds + Lc40
```

Excess Phase

In an actual device, the measured phase shift is often larger than the shift predicted by the lumped model. The excess-phase parameter `td` accounts for this extra phase shift at high frequencies. An all-pass, second-order Bessel function filter creates this extra phase shift. The frequency response of this filter is:

(48-31)

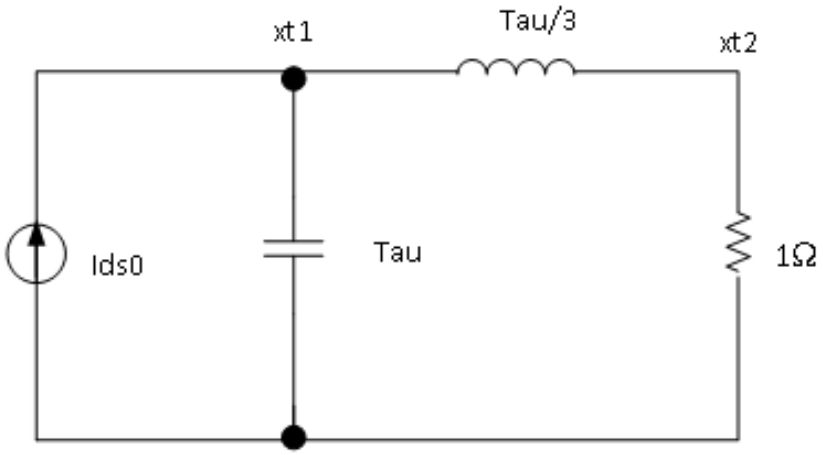
$$\varphi_s = \frac{3\omega_0^2}{s^2 + 3\omega_0 s + 3\omega_0^2}$$

(48-32)

$$\omega_0 = \frac{1}{\tau}$$

© 2023 Cadence Design Systems, Inc.

The Bessel filter is implemented with the excess phase network, as shown in the figure below.



Self Heating Model

The power used for the self-heating model is given by:

(48-33)

$$Pwr = abs(-Ids \cdot Vds + Igs \cdot Vgsc)$$

Noise Model

Broadband Noise:

Noimod=0:

(48-34)

$$I_{dtn} = \left|I_{DS}\right| + \left|I_{GD}\right|$$

(48-35)

$$T'_D = Td[1 + Tmn(1 + \tanh(\psi)) \cdot \left|\tanh(\alpha V_{DS})\right| \cdot (1 + Lambda \cdot V_{DS})]$$

© 2023 Cadence Design Systems, Inc.

(48-36)

$$\frac{\langle i_d^2 \rangle}{\Delta f} = 4kTLw\sqrt{\frac{T'_D}{Temp}}I_{dtn} + Td1 \cdot I^2_{dtn}$$

Noimod=1

Parameters `NoiseP`, `NoiseR`, and `NoiseC` model the drain and gate noise sources, and their correlation.

(48-37)

$$\frac{\langle i_d^2 \rangle}{\Delta f} = 4kT \cdot GM \cdot NoiseP$$

(48-38)

$$\frac{\langle i_g^2 \rangle}{\Delta f} = 4kT \cdot C^2_{gs} \cdot \omega^2 \cdot \frac{NoiseR}{gm}$$

(48-39)

$$\frac{\langle ig, id^* \rangle}{\Delta f} = j \cdot NoiseC \cdot 4kT \cdot C_{gs} \cdot \omega \cdot \sqrt{NoiseP \cdot NoiseR}$$

Igs, Igd Shot Noise and Flicker Noise

(48-40)

$$\frac{\langle i_{gs}^2 \rangle}{\Delta f} = 2 \cdot q \cdot I_{gs} + KF \cdot \frac{I_{gs}^{AF}}{freq^{Ffe}}$$

© 2023 Cadence Design Systems, Inc.

(48-41)

$$\frac{\langle i_{gd}^{2} \rangle}{\Delta f} = 2 \cdot q \cdot I_{gd} + KF \cdot \frac{I_{gd}^{AF}}{freq^{Ffe}}$$

Ids Flicker Noise

Noimod=0 (default value)

(48-42)

$$\frac{i_{df}^{2}}{\Delta f} = KLFD \cdot \frac{\langle i_{d}^{2} \rangle}{\Delta f}$$

where

(48-43)

$$KLFD \cong KLF \cdot \left(\frac{1}{freq^{NP}} + \frac{1}{\left(1 + \left(\frac{freq}{FGR}\right)^{2}\right)} \right)$$

Noimod=1

(48-44)

$$\frac{\langle i_{d}^{2} \rangle}{\Delta f} = \frac{KF \cdot I_{ds}^{AF}}{freq^{FFE}} + 4kT \cdot gm \cdot NoiseP \cdot \frac{Fnc}{freq}$$

Thermal Noise

Thermal noise of resistances Rgd, Rd, Rg, and Rs

© 2023 Cadence Design Systems, Inc.

(48-45)

$$\frac{\overline{i^2}}{\Delta f} = \frac{4kT}{R}$$

For Ri

(48-46)

$$\frac{\overline{i^2}}{\Delta f} = \frac{4kT_g}{R_i}$$

Related Topics

Angelov Model

Model Equations

Release History and Version

Model Usage

Model Usage

Release History and Version

Version 2.3 is the Verilog-A model released in June, 2015.

Related Topics

Angelov Model

Model Equations

Model Usage

Model Usage

© 2023 Cadence Design Systems, Inc.

Model Usage

Instance Syntax

An Angelov instance has three or four terminals. The model name has to be associated with Angelov model card.

```
InstanceName (d g s <t>) AngelovModelName <parameter=value>
```

Sample Instance Statement

```
m1 (v1 v2 v3) angelov_mod trise=20
```

Model Syntax

The following syntax specifies the Angelov model:

```
model modelName angelov parameter=value ...
```

The third parameter, `angelov`, is the master to indicate that this model card is an angelov model card.

Sample Model Statement

```
model pchmod angelov  +rd=50 rs=50 tau=1e-12
```

Related Topics

Angelov Model

Model Equations

Release History and Version

Model Usage

Component Statements

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.
`dtemp=0.0 C`	alias of trise.
`trise=0.0 C`	Difference sim. temp and device temp.
`temp=(-9.9999e-99) C`	Device temp (only used if Trise is zero.

Model Parameters

`type=n`	Channel type parameter, n=NFET p=PFET. Possible values are `n` and `p`.
`noise=1`	Globally disable noise.
`noimod=0`	Noise model (0=def, 1=PRC).
`selft=0`	Flag for self-heating.
`idsmod=0`	Ids Current Model [0:1].
`igmod=0`	Select gate diode model [0:1].
`capmod=2`	Select cap model [0:2].
`ipk0=0.05 A`	Current for max. transconductance Ipk.
`vpks=(-0.2) V`	Gate voltage Vpk for max transconductance.
`dvpks=0.2 V`	Delta gate voltage at peak gm.
`p1=1.0 1/V`	Polynomial coeff P1 for channel current.
`p2=0.0 1/V`^{2}	Polynomial coeff P2 for channel current.
`p3=0.0 1/V`^{3}	Polynomial coeff P3 for channel current.
`alphar=0.1 1/V`	Saturation parameter alpha_r.
`alphas=1.0 1/V`	Saturation parameter alpha.
`vkn=0.8 V`	Knee voltage.
`lambda=0.0`	Channel length modulation parameter.
`lambda1=0.0`	Channel length modulation parameter.

© 2023 Cadence Design Systems, Inc.

`lvg=0.0`	Coeff for channel length modulation parameter
`b1=0.0`	Unsaturated coeff B1 for P1.
`b2=3.0 1/V`	Saturated coeff B2 for P1.
`lsb0=0.0`	Soft breakdown model parameter.
`vtr=20.0 V`	Soft breakdown model parameter.
`vsb2=0.0 V`	Surface breakdown model parameter.
`cds=0 F`	Zero-bias D-S junction capacitance.
`cgspi=0.0 F`	Gate-source pinch-off capacitance.
`cgs0=0.0 F`	Gate-source capacitance parameter.
`cgdpi=0.0 F`	Gate-drain pinch-off capacitance.
`cgdpe=0 F`	External G-D Capacitor.
`cgd0=0.0 F`	Gate-drain capacitance parameter Cgdo.
`p10=0.0`	Polynomial coeff P10 for capacitance.
`p11=1.0`	Polynomial coeff P11 for capacitance.
`p20=0.0`	Polynomial coeff P20 for capacitance.
`p21=0.2`	Polynomial coeff P21 for capacitance.
`p30=0.0`	Polynomial coeff P30 for capacitance.
`p31=0.2`	Polynomial coeff P31 for capacitance.
`p40=0.0`	Polynomial coeff P40 for capacitance.
`p41=1.0`	Polynomial coeff P41 for capacitance.
`p111=0.0`	Polynomial coeff P400 for capacitance.
`ij=0.00005 A`	Gate fwd saturation current.
`pg=(-(-9.9999e-99)`	Gate current parameter.
`ne=(-(-9.9999e-99))`	Gate p-n emission coeff.
`vjg=0.7 V`	Gate current parm.
`rg=0.0 Ω`	Gate ohmic resistance.
`rd=0.0 Ω`	Drain ohmic resistance.
`ri=0.0 Ω`	Input resistance.
`rs=0.0 Ω`	Source ohmic resistance.

© 2023 Cadence Design Systems, Inc.

`rgd=0 Ω`	Gate resistance.
`ld=0 H`	Drain ohmic inductance.
`ls=0 H`	Source ohmic inductance.
`lg=0 H`	Gate ohmic inductance.
`tau=0 s`	Device delay.
`rcmin=1.0e3 Ω`	Minimum value of Rc.
`rc=10.0e3 Ω`	R for freq dep output cond.
`crf=0.0 F`	C for freq dep output cond.
`rcin=100.0e3 Ω`	R for freq dep input cond.
`crfin=0.0 F`	C for freq dep input cond.
`rtherm=0.0`	Alias of rth.
`rth=0.0 Ω`	Thermal resistance.
`ctherm=0.0`	Alias of cth.
`cth=0.0 F`	Thermal capacitance.
`tcipk0=0.0 A/K`	Linear temp coef TIpk for Ipk.
`tcp1=0.0 A/K`	Linear temp coef TIpk for Ipk.
`tccgs0=0.0`	Linear temp coef Cgs0 parm.
`tccgd0=0.0`	Linear temp coef Cgd0 parm.
`tclsb0=0.0`	Linear temp coef Lsb0 parm.
`tcrc=0.0`	Linear temp coef Rc parm.
`tccrf=0.0`	Linear temp coef Crf parm.
`noiser=0.5`	Gate noise coeff.
`noisep=1.0`	Gate noise coeff.
`noisec=0.9`	Gate-drain noise coeff.
`fnc=0.0 Hz`	Noise corner freq.
`kf=0.0`	Flicker noise coeff.
`af=1.0`	Flicker noise exponent.
`ffe=1.0`	Flicker noise parameter.
`tg=25.0 C`	Gate equiv temp.

© 2023 Cadence Design Systems, Inc.

`td=25.0 C`	Drain equiv temp.
`td1=0.1 C`	Drain equiv temp.
`tmn=1.0`	Noise fitting coeff.
`klf=1.0e14`	Flicker noise exponent.
`fgr=60.0e3 Hz`	G-R freq corner.
`np=0.3`	Flicker noise freq exp.
`lw=0.1 mm`	Effective gate noise width.
`tnom=(-9.9999e-99) C`	Parameters measurement temperature.
`version=2.3`	The available version is 2.30(2.3.0).
`ma_mod=0`	Flag to turn on Ma model.
`trise=0.0 C`	Temperature rise from ambient alias of dtemp. It serves as the default value of instance trise.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`ids (A)`	Drain current.
`igs (A)`	Gate-source current.
`igd (A)`	Gate-drain current.
`dTjunc (C)`	Delta T.
`Cgssim (F)`	Gate-source capacitance.
`Cgdsim (F)`	Gate-drain capacitance.
`pwr (W)`	Power at op point.

© 2023 Cadence Design Systems, Inc.

Related Topics

Angelov Model

Model Equations

Release History and Version

Model Usage

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

49

Angelov GaN Model

The Angelov model is an empirical equation-based large signal model that is used for III-V field effect transistors, such as HEMT and MESFET. This model can be used for GaN and other HEMT devices. It is developed by Chalmers University of Technology.

Related Topics

Model Equations

Release History and Version

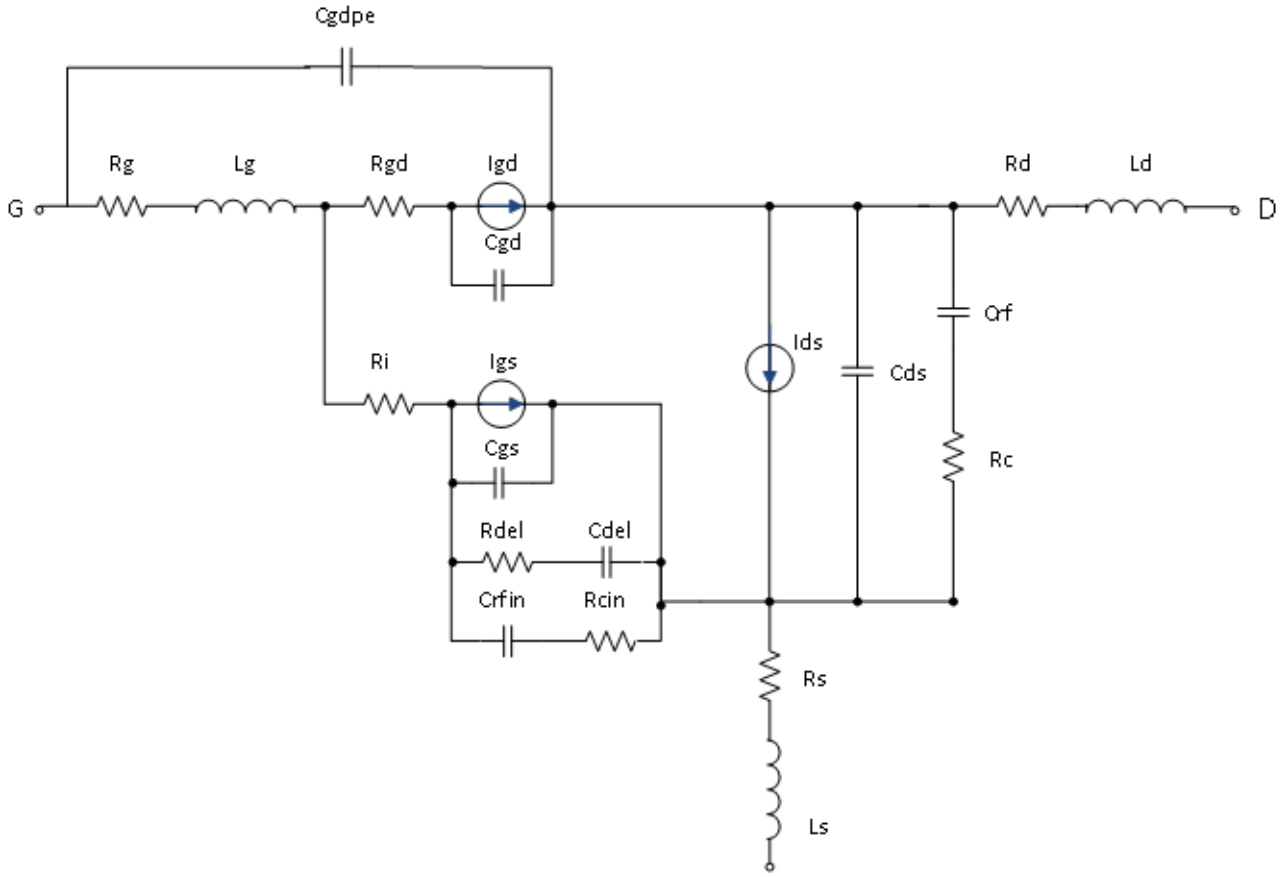
Component Statements

Model Usage

© 2023 Cadence Design Systems, Inc.

Model Equations

Equivalent Circuit



Ids Equations

(49-1)

$$P1m = P1 \cdot (1 + B1/(\cosh(B2 \cdot Vds) \cdot \cosh(B2 \cdot Vds)))$$

(49-2)

$$Vpkm = VPKS - DVPKS + DVPKS \cdot \tanh(ALPHA \cdot Vds) - VSB2 \cdot (Vdg - VTR)^2$$

© 2023 Cadence Design Systems, Inc.

(49-3)

$$\psi_p = P1m \cdot ((Vgs - Vpkm) + P2 \cdot (Vgs - Vpkm)^2 + P3 \cdot (Vgs - Vpkm)^3)$$

(49-4)

$$\alpha_p = ALPHAR + ALPHAS \cdot (1 + \tanh(\psi_p))$$

For original model (`idsmod=0`)

(49-5)

$$Ids = IPK0 \cdot (1 + \tanh(\psi_p)) \cdot \tanh(\alpha_p \cdot Vds) \cdot (1 + LAMBDA \cdot Vds + LSB0 \cdot \exp(Vdg - VTR))$$

For the symmetric model (`idsmod=1`)

(49-6)

$$\psi_n = P1m \cdot (Vgd - Vpkm) + P2 \cdot (Vgd - Vpkm)^2 + P3 \cdot (Vgd - Vpkm)^3$$

(49-7)

$$\alpha_n = ALPHAR + ALPHAS \cdot (1 + \tanh(\psi_n))$$

(49-8)

$$\lambda_n = LAMBDA + LVG \cdot (1 + \tanh(\psi_n))$$

(49-9)

$$\lambda_p = LAMBDA + LVG \cdot (1 + \tanh(\psi_p))$$

(49-10)

$$\lambda_{n1} = LAMBDA1 + LVG \cdot (1 + \tanh(\psi_n))$$

© 2023 Cadence Design Systems, Inc.

(49-11)

$$\lambda_{p1} = LAMBDA1 + LVG \cdot (1 + \tanh(\psi_p))$$

(49-12)

$$Idsp = IPK0 \times (1 + \tanh(\psi_p)) \times (1 + \tanh(\alpha_p \times Vds)) \times \left(1 + \lambda_p \times Vds + \lambda_{p1} \times \exp\left(\frac{Vds}{Vkn} - 1\right)\right)$$

(49-13)

$$Idsn = IPK0 \times (1 + \tanh(\psi_n)) \times (1 - \tanh(\alpha_n \times Vds)) \times \left(1 - \lambda_n \times Vds - \lambda_{n1} \times \exp\left(\frac{Vds}{Vkn} - 1\right)\right)$$

(49-14)

$$Ids = 0.5 \times (Idsp - Idsn)$$

idsmod=2

(49-15)

$$\psi_p = P1m \cdot ((Vgs - Vpkm) + P2 \cdot (Vgs - Vpkm)^2 + P3 \cdot (Vgs - Vpkm)^3)$$

(49-16)

$$\tan h(\psi_p) = 1 + \tanh(0.5 \cdot (\exp(\psi_p) - \exp(-\psi_p)))$$

(49-17)

$$\alpha_p = ALPHAR + ALPHAS \cdot \tanh(\psi_p)$$

(49-18)

$$Ids = IPK0 \cdot \tanh(\psi_p) \cdot \tanh(\alpha_p \cdot Vds) \cdot (1 + \lambda + LVG \cdot \tanh(\psi_p) \cdot Vds + LSB \cdot \exp(Vdg - Vtr))$$

idsmod=3

© 2023 Cadence Design Systems, Inc.

(49-19)

$$\psi_p = P1m \cdot ((Vgs - Vpkm) + P2 \cdot (Vgs - Vpkm)^2 + P3 \cdot (Vgs - Vpkm)^3)$$

(49-20)

$$\tan h(\psi_p) = 1 + \tanh(0.5 \cdot (\exp(\psi_p) - \exp(-\psi_p)))$$

(49-21)

$$\alpha_p = ALPHAR + ALPHAS \cdot \tanh(\psi_p)$$

(49-22)

$$Idsp = IPK0 \cdot \tanh(\psi_p) \cdot (1 + \tanh(\alpha_p \cdot Vds)) \cdot (1 + LAMBDA + LVG \cdot \tanh(\psi_p) \cdot VDS + LSB0 \cdot \exp(VDS - VTR))$$

(49-23)

$$\psi_n = P1m \cdot ((Vgd - Vpkm) + P2 \cdot (Vgd - Vpkm)^2 + P3 \cdot (Vgd - Vpkm)^3)$$

(49-24)

$$\tan h(\psi_n) = 1 + \tanh(0.5 \cdot (\exp(\psi_n) - \exp(-\psi_n)))$$

(49-25)

$$\alpha_n = ALPHAR + ALPHAS \cdot \tanh(\psi_n)$$

(49-26)

$$Idsn = IPK0 \cdot \tanh(\psi_n) \cdot (1 - \tanh(\alpha_p \cdot Vds)) \cdot (1 - (LAMBDA + LVG \cdot \tan h(\psi_n))) \cdot Vds$$

© 2023 Cadence Design Systems, Inc.

(49-27)

$$Ids = 0.5 \times (Idsp - Idsn)$$

Igs and Igd Equations

When `igmod=0`

(49-28)

$$Igs = IJ \cdot (\exp(PG \cdot (Vgsc - VJG) - 1e-6 \cdot Kbdgate \cdot (\exp(Pbdg \cdot (-Vgsc - Vbdgs))) - \exp(PG \cdot \tanh(-Vjg))))$$

(49-29)

$$Igd = IJ \cdot (\exp(PG \cdot (Vgdc - VJG) - 1e-6 \cdot Kbdgate \cdot (\exp(Pbdg \cdot (-Vgdc - Vbdgd))) - \exp(PG \cdot \tanh(-Vjg))))$$

When `igmod=1`

(49-30)

$$Igs = IJ \cdot (\exp(((PG \cdot \tanh(Vgsc - VJG)) - 1e-6 \cdot Kbdgate \cdot (\exp(Pbdg \cdot (-Vgsc - Vbdgs))) - \exp(-Pbdg \cdot Vbgd)) - \exp(-PG \cdot Vjg)))$$

(49-31)

$$Igd = IJ \cdot (\exp(((PG \cdot \tanh(Vgdc - VJG)) - 1e-6 \cdot Kbdgate \cdot (\exp(Pbdg \cdot (-Vgdc - Vbdgd))) - \exp(-Pbdg \cdot Vbgd)) - \exp(-PG \cdot Vjg)))$$

When `igmod=2`

(49-32)

$$Igs = IJ \cdot (\exp((PG \cdot (Vgsc - VJG) - 1e-6 \cdot Kbdgate \cdot (\exp(Pbdg \cdot (-Vgsc - Vbdgs))) - \exp(-Pbdg \cdot Vbdgs)) - \exp(-PG \cdot Vjg)))$$

(49-33)

$$Igd = IJ \cdot (\exp((PG \cdot (Vgdc - VJG) - 1e-6 \cdot Kbdgate \cdot (\exp(Pbdg \cdot (-Vgdc - Vbdgd))) - \exp(-Pbdg \cdot Vbdgd)) - \exp(-PG \cdot Vjg)))$$

© 2023 Cadence Design Systems, Inc.

Temperature Equations

(49-34)

$$Ipk0 = IPK0 \times (1 + TCIPK0 \times (Temp - Tnom))$$

(49-35)

$$P1 = P1 \times (1 + TCP1 \times (Temp - Tnom))$$

(49-36)

$$Lsb0 = LSB0 \times (1 + TCLSB0 \times (Temp - Tnom))$$

(49-37)

$$Cgs0 = CGS0 \times (1 + TCGS0 \times (Temp - Tnom))$$

(49-38)

$$Cgd0 = CGD0 \times (1 + TCGD0 \times (Temp - Tnom))$$

(49-39)

$$Rc = RC \times (1 + TCRC \times (Temp - Tnom))$$

(49-40)

$$Crf = CRF \times (1 + TCCRF \times (Temp - Tnom))$$

Charge Equations

(49-41)

$$Phi1 = P10 + P11 \times Vgsc + P111 \times Vds$$

© 2023 Cadence Design Systems, Inc.

(49-42)

$$Phi2 = P20 + P21 \times Vds$$

(49-43)

$$Phi3 = P30 - P31 \times Vds$$

(49-44)

$$Phi4 = P40 + P41 \times Vgdc - P111 \times Vds$$

For `capmod=0`

```
Cgs = CGSP
Cgd = CGDP
Qgs = CGSP * Vgsc
Qgd = CGDP * Vgdc
```

For `capmod=1`

```
Cgs = CGSP+CGS0 x ( 1 + tanh(Phi1))( 1 + tanh(Phi2))
Cgd = CGDP + CGD0 x ((1 - P111 + tanh(Phi3)) (1 + tanh(Phi4)) + 2 x P111)
Qgs = CGSP x Vgsc
Qgd = CGDP x Vgdc
```

For `capmod=2`

```
Lc1 = ln(cosh(Phi1))
Lc10 = ln(cosh(P10 + P11 X Vds))
Qgs = CGSP x Vgsc + CGS0 x ((Phi1 + Lc1 - Qgs0) x (1 + tanh(Phi2)) / P11 + 2 x P111
x Vgsc
Qgs0 = P10 + P111 x Vds + Lc10
Lc4 = 1n(cosh(Phi4))
Lc40 = 1n(cosh(P40 -P111 x Vds))
Qgd = CGDP x Vgdc + CGD0 x ((Phi4 + Lc4 - Qgd0) x (1 - P111 + tanh(Phi3)) / P41 +
2 x P111 x Vgdc
Qgd0 = P40 - P111 x Vds + Lc40
```

For `capmod=3`

```
y = (((Vgsc+2.0)/P10) - 1.0)
Cgsdep1 = pow((m + (y x y)), -1.5) x m
tanh1 = 1 + tanh(P10 + P11 x (Vgsc + P111 x Vds))
tanh2 = (1 + tanh(P20 + P21 x Vds))
```


© 2023 Cadence Design Systems, Inc.

```
tanh3 = 1 - P111 + tanh(P30 + P31 x Vds)
tanh4 = 1+ tanh(P40 + P41 x (Vgdc + Vds x (1 - P111)))
Cgs = CGS0 x (tanh1 + P222 x Cgsdep1) x tanh2 + CGSP
Cgd = CGD0 x (tanh3 x tanh4 + 2 x P111) + CGDP
Qgs = Cgs x Vgsc
Qgd = Cgd x Vgdc
```

For `capmod=4`

```
Lc1 = ln(cosh(Phi1))
LC10 = ln(cosh(P10 +P111 x Vds)
Qgsdepl = P222 x (P10 + Vgsc) x pow(m + pow(-1 + (Vgsc/P10),2), -0.5)
Qgsdep10 = P222 x P10 x pw((m+1), -0.5)
Qgs0 = P10 + P111xVds + Lc10
Qgs = CGS0 x ((Phi1 + Lc1 - Qgs0 + Qgsdep1 - Qgsdep10) x (1 - P111 + tanh(Phi2))/
P11 + 2 x P111 x Vgsc) + CGSP x Vgsc
Lc4 = ln(cosh(Phi4))
Lc40 = ln(cosh(P40 - P111 x Vds)
Qgd0 = P40 - p111 x Vds + Lc40
Qgd = Cgd0 x ((Phi4 + Lc4 - Qgd0) x (1 - P111 + tanh(Phi3))/P41 + 2 x P111 x Vgdc)
+ CGDP x Vgdc
```

Excess Phase

In an actual device, the measured phase shift is often larger than the shift predicted by the lumped model. The excess-phase parameter `td` accounts for this extra phase shift at high frequencies. An all-pass, second-order Bessel function filter creates this extra phase shift. The frequency response of this filter is:

(49-45)

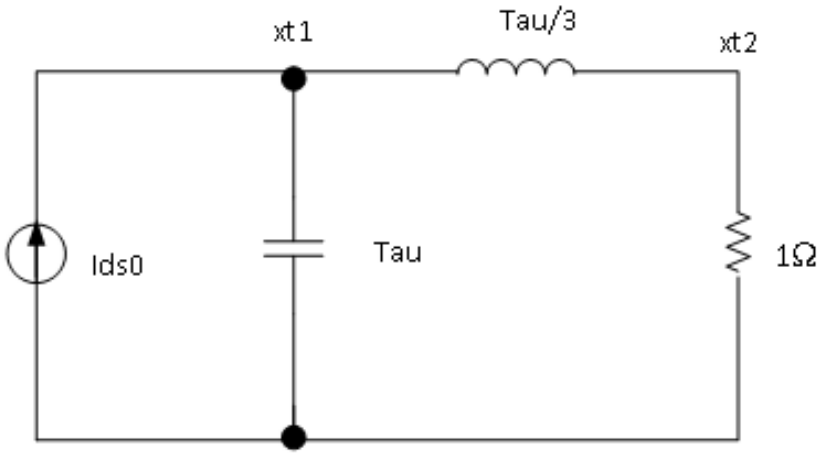
$$\varphi_s = \frac{3\omega_0^2}{s^2 + 3\omega_0 s + 3\omega_0^2}$$

(49-46)

$$\omega_0 = \frac{1}{\tau}$$

© 2023 Cadence Design Systems, Inc.

The Bessel filter is implemented with the excess phase network, as shown in the figure below.



Self Heating Model

The power used for the self-heating model is given by:

(49-47)

$$Pwr = abs(-Ids \cdot Vds + Igs \cdot Vgsc)$$

Noise Model

Broadband Noise:

Noimod=0:

(49-48)

$$I_{dtn} = \left|I_{DS}\right| + \left|I_{GD}\right|$$

(49-49)

$$T'_D = Td[1 + Tmn(1 + \tanh(\psi)) \cdot \left|\tanh(\alpha V_{DS})\right| \cdot (1 + Lambda \cdot V_{DS})]$$

© 2023 Cadence Design Systems, Inc.

(49-50)

$$\frac{\langle i_d^2 \rangle}{\Delta f} = 4kTLw\sqrt{\frac{T'_D}{Temp}}I_{dtn} + Td1 \cdot I^2_{dtn}$$

Noimod=1

Parameters `NoiseP`, `NoiseR`, and `NoiseC` model the drain and gate noise sources, and their correlation.

(49-51)

$$\frac{\langle i_d^2 \rangle}{\Delta f} = 4kT \cdot GM \cdot NoiseP$$

(49-52)

$$\frac{\langle i_g^2 \rangle}{\Delta f} = 4kT \cdot C^2_{gs} \cdot \omega^2 \cdot \frac{NoiseR}{gm}$$

(49-53)

$$\frac{\langle ig, id^* \rangle}{\Delta f} = j \cdot NoiseC \cdot 4kT \cdot C_{gs} \cdot \omega \cdot \sqrt{NoiseP \cdot NoiseR}$$

Igs, Igd Shot Noise and Flicker Noise

(49-54)

$$\frac{\langle i_{gs}^2 \rangle}{\Delta f} = 2 \cdot q \cdot I_{gs} + KF \cdot \frac{I_{gs}^{AF}}{freq^{Ffe}}$$

© 2023 Cadence Design Systems, Inc.

(49-55)

$$\frac{\langle i_{gd}^{\ 2} \rangle}{\Delta f} = 2 \cdot q \cdot I_{gd} + KF \cdot \frac{I_{gd}^{AF}}{freq^{Ffe}}$$

Ids Flicker Noise

Noimod=0 (default value)

(49-56)

$$\frac{i_{df}^{2}}{\Delta f} = KLFD \cdot \frac{\langle i_{d}^{\ 2} \rangle}{\Delta f}$$

where

(49-57)

$$KLFD \cong KLF \cdot \left(\frac{1}{freq^{NP}} + \frac{1}{\left(1 + \left(\frac{freq}{FGR}\right)^{2}\right)} \right)$$

Noimod=1

(49-58)

$$\frac{\langle i_{d}^{\ 2} \rangle}{\Delta f} = \frac{KF \cdot I_{ds}^{AF}}{freq^{FFE}} + 4kT \cdot gm \cdot NoiseP \cdot \frac{Fnc}{freq}$$

Thermal Noise

Thermal noise of resistances Rgd, Rd, Rg, and Rs

© 2023 Cadence Design Systems, Inc.

(49-59)

$$\frac{\overline{i^2}}{\Delta f} = \frac{4kT}{R}$$

For Ri

(49-60)

$$\frac{\overline{i^2}}{\Delta f} = \frac{4kT_g}{R_i}$$

Related Topics

Angelov GaN Model

Model Equations

Release History and Version

Model Usage

Component Statements

Release History and Version

Version 2.3 is the verilog-A model released in June, 2015.

Related Topics

Angelov GaN Model

Model Equations

Model Usage

Component Statements

© 2023 Cadence Design Systems, Inc.

Model Usage

Instance Syntax

An Angelov GaN instance has three or four terminals. The model name has to be associated with `angelov_gan` model card.

```
InstanceName (d g s <t>) Angelov_ganModelName <parameter=value>
```

Sample Instance Statement

```
m1 (v1 v2 v3) angelov_gan trise=20
```

Model Syntax

The following syntax specifies the Angelov model:

```
mode ModelName angelov_gan parameter=value ...
```

The third parameter, `angelov_gan`, is the master to indicate that this model card is an Angelov GaN model card.

Sample Model Statement

```
model pchmod angelov_gan +rd=50 rs=50 tau=1e-12
```

Related Topics

Angelov GaN Model

Model Equations

Release History and Version

Component Statements

Component Statements

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

Instance Parameters

`trise=0.0`	Difference sim. temp and device temp, [C deg].
`dtemp=0.0`	Alias of trise.
`temp=25.0`	Device temp (only used if Trise is zero) [C].
`m=1.0`	Multiplicity factor.
`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.

Model Parameters

`noise=1`	Globally disable noise.
`noimod=0`	Noise model (0=def, 1=PRC).
`selft=0`	Flag for self-heating.
`idsmod=0`	Ids Current Model [0:3].
`igmod=0`	Select gate diode model [0:1].
`capmod=2`	Select cap model [0:4].
`ipk0=0.05`	Current for max. transconductance Ipk [A].
`vpks=(-0.2)`	Gate voltage Vpk for max transconductance [V].
`dvpks=0.2`	Delta gate voltage at peak gm [V].
`p1=0.8`	Polynomial coeff P1 for channel current [1/V].
`p2=0.0`	Polynomial coeff P2 for channel current [1/V^2].
`p3=0.0`	Polynomial coeff P3 for channel current [1/V^3].
`alphar=0.1`	Saturation parameter alpha_r [1/V].
`alphas=1.0`	Saturation parameter alpha [1/V].
`vkn=4.0`	Knee voltage [V].
`lambda=0.001`	Channel length modulation parameter.
`lambda1=0.0`	Channel length modulation parameter.
`lvg=0.0`	Coeff for channel length modulation parameter.
`b1=0.1`	Unsaturated coeff B1 for P1.

© 2023 Cadence Design Systems, Inc.

`b2=4.0`	Saturated coeff B2 for P1 [1/V].
`lsb0=0.0`	Soft breakdown model parameter.
`vtr=50.0`	Soft breakdown model parameter [V].
`vsb2=0.0`	Surface breakdown model parameter [V].
`ebd=0.2`	Surface breakdown model parameter [1/V].
`cds=0`	Zero-bias D-S junction capacitance [F].
`cgspi=0.0`	Gate-source pinch-off capacitance [F].
`cgs0=0.0`	Gate-source capacitance parameter [F].
`cgdpi=0.0`	Gate-drain pinch-off capacitance [F].
`cgdpe=0`	External G-D Capacitor [F].
`cgd0=0.0`	Gate-drain capacitance parameter Cgdo [F].
`p10=0.0`	Polynomial coeff P10 for capacitance.
`p11=1.0`	Polynomial coeff P11 for capacitance.
`p20=0.0`	Polynomial coeff P20 for capacitance.
`p21=0.2`	Polynomial coeff P21 for capacitance.
`p30=0.0`	Polynomial coeff P30 for capacitance.
`p31=0.2`	Polynomial coeff P31 for capacitance.
`p40=0.0`	Polynomial coeff P40 for capacitance.
`p41=1.0`	Polynomial coeff P41 for capacitance.
`p111=0.0`	Polynomial coeff P111 for capacitance.
`p222=0.0`	Polynomial coeff P222 for capacitance.
`m=0.5`	Coefficient for capacitance .
`ij=0.00005`	Gate fwd saturation current [A].
`pg=15.0`	Gate current parameter.
`ne=1.0`	Gate p-n emission coeff.
`vjg=0.7`	Gate current parm [V].
`rg=0.05`	Gate ohmic resistance [Ohm].
`rd=0.05`	Drain ohmic resistance [Ohm].
`rd2=0.0`	Variable Drain ohmic resistance [Ohm].

© 2023 Cadence Design Systems, Inc.

`ri=0.05`	Input resistance [Ohm].
`rs=0.05`	Source ohmic resistance [Ohm].
`rgd=0.05`	Gate resistance [Ohm].
`ld=0`	Drain ohmic inductance [H].
`ls=0`	Source ohmic inductance [H].
`lg=0`	Gate ohmic inductance [H].
`tau=0`	Device delay [s].
`rcmin=1.0e3`	Min value of Rc [Ohm].
`rc=10.0e3`	R for freq dep output cond [Ohm].
`crf=0.0`	C for freq dep output cond [F].
`rcin=100.0e3`	R for freq dep input cond [Ohm].
`crfin=0.0`	C for freq dep input cond[F].
`rdel=1`	R for freq dep input cond [Ohm].
`cdel=0.0`	C for freq dep input cond[F].
`kbgate=0.00`	Polynomial coeff Kbgate for freq dep input cond [1/V].
`rtherm=0.001`	Thermal resistance [K/W].
`rth=0.001`	Thermal resistance [K/W].
`ctherm=0.0001`	Thermal capacitance [Ws/K].
`cth=0.0001`	Thermal capacitance [Ws/K].
`tcipk0=(-0.002)`	Linear temp coef TIpk for Ipk [1/K].
`tcp1=(-0.002)`	Linear temp coef TIpk for Ipk [1/K].
`tccgs0=0.002`	Linear temp coef for Cgs0 [1/K].
`tccgd0=0.002`	Linear temp coef for Cgd0 [1/K].
`tclsb0=0.0`	Linear temp coef for Lsb0 [1/K].
`tcrc=0.0`	Linear temp coef for Rc [1/K].
`tccrf=0.0`	Linear temp coef for Crf [1/K].
`tcrs=0.003`	Linear temp coef for Rs [1/K].
`tcrtherm=0.002`	Linear temp coef for Rth [1/K].
`kbdgate=1.0`	Gate breakdown parm [V].

© 2023 Cadence Design Systems, Inc.

`vbdgs=5.0`	Gate source breakdown voltage [V].
`vbdgd=20.0`	Gate drain breakdown voltage [V].
`pbdg=0.5`	Gate breakdown exponent [1/V].
`noiser=0.5`	Gate noise coeff.
`noisep=1.0`	Gate noise coeff.
`noisec=0.9`	Gate-drain noise coeff.
`fnc=0.0`	Noise corner freq [Hz].
`kf=0.0`	Flicker noise coeff.
`af=1.0`	Flicker noise exponent.
`ffe=1.0`	Flicker noise parameter.
`tg=25.0`	Equiv temp [C].
`td=25.0`	Equiv temp [C].
`td1=0.1`	Equiv temp [C].
`tmn=1.0`	noise fitting coeff.
`klf=1.0e14`	Flicker noise exponent.
`fgr=60.0e3`	G-R freq corner [Hz].
`np=0.3`	flicker noise freq exp.
`lw=0.1`	effective gate noise width [mm].
`tnom=25.0`	param meas T [C].
`version=2.3`	The available version is 2.30(2.3.0).
`p10pk=4`	Polynomial coeff P10pk for capacitance.
`krfdc=1.0001`	Coeff KRFDC will set division between Ids and Dispersion IdsRF current.
`tcvpk=0.001`	Linear temp coef for Vpk [1/K].
`tcvjg=(-0.001)`	Linear temp coef for Vjg [1/K].
`trise=0.0 C`	Temperature rise from ambient alias of dtemp. It serves as the default value of instance trise.

© 2023 Cadence Design Systems, Inc.

Output Parameters

`tempeff`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

`pwr (W)`	Power at op point.
`ids (A)`	Drain-source current.
`igs (A)`	Gate-source current.
`igd (A)`	Gate-drain current.
`dTjunc (C)`	Delta T.
`Cgssim (F)`	Gate-source capacitance.
`Cgdsim (F)`	Gate-drain capacitance.

Related Topics

Angelov GaN Model

Model Equations

Release History and Version

Model Usage

Component Statements

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

50

DIODE_CMC Model

The DIODE_CMC model is based on Juncap2 200.3.3 from NXP Semiconductors. It is mainly used to model those diodes that are formed with MOSFETs. Those MOSFETs have source, drain, or well-to-bulk junctions. Geometrically, DIODE_CMC has capacitances and currents of bottom, gate edge, and STI edge contributions.

Related Topics

Model Equations

Model Equations

Model Usage

Component Statements

Model Equations

Junction Charge

(50-1)

$$C_{jo} = CJOR \cdot \left(\frac{VBIR}{V_{bi}}\right)^{P}$$

(50-2)

$$V_j = hyp_5(V_{AK};V_{F,min}, V_{ch})$$

© 2023 Cadence Design Systems, Inc.

(50-3)

$$Q'_j = \left\{ \frac{C_{j0} \cdot V_{bi}}{1-P} \cdot \left[1 - \left(1 - \frac{V_j}{V_{bi}} \right)^{1-P} \right] + a \cdot C_{j0} \cdot (V_{AK} - V_j) \right\}$$

Ideal Current

(50-4)

$$M_{ID} = \left\{ \begin{array}{ll} \exp\left(\frac{V_{AK}}{n \cdot \phi_{TD}} \right) & if\ V_{AK} < V_{max} \\ \left(1 + \frac{V_{AK} - VMAX}{n \cdot \phi_{TD}} \right) \cdot \exp\left(\frac{VMAX}{\phi_{TD}} \right) & if\ V_{AK} \geq V_{max} \end{array} \right\}$$

$$I'_D = (M_{ID} - 1) \cdot I_{DSAT}$$

Ideal Current with High Injection

$$I'_D = (M_{\mathrm{ID}} - 1) \cdot I_{\mathrm{DSAT}}$$

$$M_{\mathrm{ID}} = \left\{ \begin{array}{ll} \exp\left[\frac{V_{\mathrm{AK}}}{n_{\mathrm{jA}}(V_{\mathrm{AK}}) \cdot \phi_{\mathrm{TD}}} + V_{\mathrm{HA}} \cdot \frac{n_{\mathrm{jA}}(V_{\mathrm{AK}}) - \mathbf{NFA}}{\mathbf{NFA \cdot NJH}} \right] & if\ V_{\mathrm{AK}} < VMAX \\ \left\{ 1 + \frac{V_{\mathrm{AK}} - VMAX}{\phi_{\mathrm{TD}}} \cdot dVMAX \right\} & \\ \cdot \exp\left[\frac{VMAX}{n_{\mathrm{jA}}(VMAX) \cdot \phi_{\mathrm{TD}}} + V_{\mathrm{HA}} \cdot \frac{n_{\mathrm{jA}}(VMAX) - \mathbf{NFA}}{\mathbf{NFA \cdot NJH}} \right] & if\ V_{\mathrm{AK}} \geq VMAX \end{array} \right.$$

$$dVMAX = \frac{n_{\mathrm{jA}}(VMAX) - VMAX \cdot \left[\frac{dn_{\mathrm{jA}}}{dV_{\mathrm{AK}}} \right]_{VMAX}}{n_{\mathrm{jA}}(VMAX)^2} + V_{\mathrm{HA}} \cdot \frac{\left[\frac{dn_{\mathrm{jA}}}{dV_{\mathrm{AK}}} \right]_{VMAX}}{\mathbf{NFA \cdot NJH}}$$

© 2023 Cadence Design Systems, Inc.

Shockley-Read-Hall current

(50-5)

$$Z_{inv} = \left\{ \begin{array}{ll} \sqrt{\exp\left(\frac{V_{AK}}{\phi_{TD}}\right)} & if \quad V_{AK} < V_{max} \\ \sqrt{\left(1 + \frac{V_{AK} - VMAX}{\phi_{TD}}\right) \cdot \exp\left(\frac{VMAX}{\phi_{TD}}\right)} & if \quad V_{AK} \geq V_{max} \end{array} \right\}$$

(50-6)

$$Z = \frac{1}{Z_{inv}}$$

(50-7)

$$\Psi^{*} = \left\{ \begin{array}{ll} \phi_{TD} \cdot \ln[z + 2 + \sqrt{(z+1) \cdot (z+3)}] & if \quad V_{AK} > 0 \\ -\frac{V_{AK}}{2} + \phi_{TD} \cdot \ln[1 + 2 \cdot z_{inv} + \sqrt{(1 + z_{inv}) \cdot (1 + 3 \cdot z_{inv})}] & if \quad V_{AK} \leq 0 \end{array} \right\}$$

(50-8)

$$V_{j,\,lim} = V_{bi,\,min} - 2 \cdot \Psi^{*}$$

(50-9)

$$V_{j,\,SRH} = hyp2(V_{AK}; V_{j,\,lim}, \phi_{TD})$$

(50-10)

$$\Delta w_{SRH} = \left(\frac{w_{SRH,\,step}^{2} \cdot \ln w_{SRH,\,step}}{1 - w_{SRH,\,step}} + w_{SRH,\,step} \right) \cdot (1 - 2 \cdot P)$$

© 2023 Cadence Design Systems, Inc.

(50-11)

$$w_{SRH} = w_{SRH,\,step} + \Delta w_{SRH}$$

(50-12)

$$W_{dep} = \frac{XJUN \cdot \varepsilon_{Si}}{CJOR} \cdot \left(\frac{V_{bi} - V_{j,\,SRH}}{VBIR}\right)^{P}$$

(50-13)

$$I_{SRH} = CSRH \cdot F_{TD} \cdot (z_{inv} - 1) \cdot w_{SRH} \cdot W_{dep}$$

Trap-Assisted Tunneling Current

(50-14)

$$F_{max} = \frac{V_{bi} - V_{j,\,SRH}}{W_{dep} \cdot (1 - P)}$$

(50-15)

$$m_{eff} = MEFFTAT \cdot m_0$$

(50-16)

$$\Delta E = max\left(\frac{\phi_{GD}}{2}, \phi_{TD}\right)$$

(50-17)

$$a_{TAT} = \frac{\Delta E}{\phi_{TD}}$$

© 2023 Cadence Design Systems, Inc.

(50-18)

$$b_{TAT} = \sqrt{\frac{32 \cdot m_{eff} \cdot q \cdot \Delta E^3}{3 \cdot h \cdot F_{max}}}$$

(50-19)

$$u'_{max} = \left(\frac{2 \cdot a_{TAT}}{3 \cdot b_{TAT}}\right)^2$$

(50-20)

$$u_{max} = \sqrt{\frac{u'^2_{max}}{u'^2_{max} + 1}}$$

(50-21)

$$w_{\Gamma} = \left(1 + b_{TAT} \cdot u_{max}^{\frac{3}{2}}\right)^{\frac{P}{P-1}}$$

(50-22)

$$w_{TAT} = \frac{w_{SRH} \cdot w_{\Gamma}}{w_{SRH} + w_{\Gamma}}$$

(50-23)

$$k_{TAT} = \sqrt{\frac{3 \cdot b_{TAT}}{8 \cdot \sqrt{u_{max}}}}$$

© 2023 Cadence Design Systems, Inc.

(50-24)

$$l_{TAT} = \frac{4 \cdot a_{TAT}}{3 \cdot b_{TAT}} \cdot \sqrt{u_{max}} - u_{max}$$

(50-25)

$$m_{TAT} = \frac{2 \cdot a_{TAT}^{2}}{3 \cdot b_{TAT}} \cdot \sqrt{u_{max}} - a_{TAT} \cdot u_{max} + \frac{b_{TAT}}{2} u_{max}^{3/2}$$

(50-26)

$$erfcapprox(y) = \left\{ \begin{array}{l} terfc = \begin{array}{ll} \frac{1}{1 + p_{erfc} \cdot y} & if \quad y > 0 \\ \frac{1}{1 - p_{erfc} \cdot y} & if \quad y \le 0 \end{array} \\ erfcapprox^{+} = \left(a_{erfc} \cdot t_{erfc} + b_{erfc} \cdot t_{erfc}^{2} + c_{erfc} \cdot t_{erfc}^{3} \right) \cdot \exp(-y^{2}) \\ erfcapprox(y) = \left\{ \begin{array}{ll} erfcapprox^{+} & if \quad y > 0 \\ 2 - erfcapprox^{+} & if \quad y \le 0 \end{array} \right\} \end{array} \right\}$$

(50-27)

$$\Gamma_{max} = \frac{a_{TAT} \cdot \exp(m_{TAT}) \cdot erfcapprox[k_{TAT} \cdot (l_{TAT} - 1)] \cdot \sqrt{\pi}}{2 \cdot k_{TAT}}$$

© 2023 Cadence Design Systems, Inc.

(50-28)

$$I'_{TAT} = CTAT \cdot F_{TD} \cdot (z_{inv} - 1) \cdot \Gamma_{max} \cdot w_{TAT} \cdot W_{dep}$$

Band-to-band tunneling current

(50-29)

$$V_{BBT,\,lim} = min(VBIRBOT, VBIRSTI, VBIRGAT) - \Delta V_{bi}$$

(50-30)

$$V_{BBT} = hyp_2(V_{AK}, V_{BBT,\,lim}, \phi_{TR})$$

(50-31)

$$W_{dep,\,r} = \frac{XJUN \cdot \varepsilon_{Si}}{CJOR} \cdot \left(\frac{VBIR - V_{BBT}}{VBIR}\right)$$

(50-32)

$$F_{max,\,r} = \frac{VBIR - V_{BBT}}{W_{dep,\,r} \cdot (1 - P)}$$

(50-33)

$$F_{BBT} = FBBTR \cdot [1 + STFBBT \cdot (T_{KD} - T_{KR})]$$

(50-34)

$$I'_{BBT} = CBBT \cdot V_{AK} \cdot F^2_{max,\,r} \cdot \exp\left(-\frac{F_{BBT}}{F_{max,\,r}}\right)$$

© 2023 Cadence Design Systems, Inc.

Avalanche and Breakdown

(50-35)

$$V_{av} = hyp_2(V_{AK};0,\varepsilon_{av})$$

$$f_{stop} = \frac{1}{1-\alpha_{av}^{PBR}}$$

$$s_f = -f_{stop}^2 \cdot \alpha_{av}^{PBR-1} \cdot \frac{PBR}{VBR}$$

$$f_{breakdown} = \begin{cases} \dfrac{1}{1-\left|\dfrac{-V_{av}}{VBR}\right|^{PBR}} & if \quad V_{av} > -\alpha_{av} \cdot VBR \\ f_{stop} + (V_{av} + \alpha_{av} \cdot VBR) \cdot s_f & if \quad V_{av} \le -\alpha_{av} \cdot VBR \end{cases}$$

Total Current

(50-36)

$$I'_j = (I'_D + I'_{SRH} + I'_{TAT} + I'_{BBT}) \cdot f_{breakdown}$$

Thermal Voltage

(50-37)

$$T_{KR} = T_0 + TRJ$$

$$T_{KD} = max(T_0 + temp + subckt_\text{rise} + TRISE + DTA, T_0 + T_{min})$$

$$\phi_{TR} = \frac{k_B \cdot T_{KR}}{q}$$

$$\phi_{TD} = \frac{k_B \cdot T_{KD}}{q}$$

© 2023 Cadence Design Systems, Inc.

Band Gap

(50-38)

$$\Delta\phi_{GR} = -\frac{7.02e-4 \cdot T_{KR}^2}{1108.0 + T_{KR}}$$

$$\phi_{GR,\,bot} = PHIGBOT + \Delta\phi_{GR}$$

$$\phi_{GR,\,sti} = PHIGSTI + \Delta\phi_{GR}$$

$$\phi_{GR,\,gat} = PHIGGAT + \Delta\phi_{GR}$$

$$\Delta\phi_{GD} = -\frac{7.02e-4 \cdot T_{KD}^2}{1108.0 + T_{KD}}$$

$$\phi_{GD,\,bot} = PHIGBOT + \Delta\phi_{GD}$$

$$\phi_{GD,\,sti} = PHIGSTI + \Delta\phi_{GD}$$

$$\phi_{GD,\,gat} = PHIGGAT + \Delta\phi_{GD}$$

Intrinsic Carrier Concentration

(50-39)

$$F_{TD,\,bot} = \left(\frac{T_{KD}}{T_{KR}}\right)^{XTI/2.0} \cdot \exp\left(\frac{\phi_{GR,\,bot}}{2 \cdot \phi_{TR}} - \frac{\phi_{GD,\,bot}}{2 \cdot \phi_{TD}}\right)$$

$$F_{TD,\,sti} = \left(\frac{T_{KD}}{T_{KR}}\right)^{XTI/2.0} \cdot \exp\left(\frac{\phi_{GR,\,sti}}{2 \cdot \phi_{TR}} - \frac{\phi_{GD,\,sti}}{2 \cdot \phi_{TD}}\right)$$

$$F_{TD,\,gat} = \left(\frac{T_{KD}}{T_{KR}}\right)^{XTI/2.0} \cdot \exp\left(\frac{\phi_{GR,\,gat}}{2 \cdot \phi_{TR}} - \frac{\phi_{GD,\,gat}}{2 \cdot \phi_{TD}}\right)$$

© 2023 Cadence Design Systems, Inc.

Saturation Current Density

(50-40)

$$I_{DSAT,\,bot} = IDSATRBOT \cdot F_{TD,\,bot}^{2}$$

$$I_{DSAT,\,sti} = IDSATRSTI \cdot F_{TD,\,sti}^{2}$$

$$I_{DSAT,\,gat} = IDSATRGAT \cdot F_{TD,\,gat}^{2}$$

Determination of Vmax

(50-41)

$$V_{max,\,bot} = \begin{cases} V_{max,\,large} & if \quad I_{DSAT,\,bot} \cdot AB = 0 \\ \phi_{TD} \cdot \ln\left(\dfrac{IMAX}{I_{DSAT,\,bot} \cdot AB} + 1\right) & if \quad I_{DSAT,\,bot} \cdot AB \neq 0 \end{cases}$$

(50-42)

$$V_{max,\,sti} = \begin{cases} V_{max,\,large} & if \quad I_{DSAT,\,sti} \cdot LS = 0 \\ \phi_{TD} \cdot \ln\left(\dfrac{IMAX}{I_{DSAT,\,sti} \cdot LS} + 1\right) & if \quad I_{DSAT,\,sti} \cdot LS \neq 0 \end{cases}$$

(50-43)

$$V_{max,\,gat} = \begin{cases} V_{max,\,large} & if \quad I_{DSAT,\,gat} \cdot LG = 0 \\ \phi_{TD} \cdot \ln\left(\dfrac{IMAX}{I_{DSAT,\,gat} \cdot LG} + 1\right) & if \quad I_{DSAT,\,gat} \cdot LG \neq 0 \end{cases}$$

(50-44)

© 2023 Cadence Design Systems, Inc.

$$V_{max} = min(V_{max,bot}, V_{max,sti}, V_{max,gat})$$

Built-In Voltages

(50-45)

$$U_{bi,bot} = VBIRBOT \cdot \frac{T_{KD}}{T_{KR}} - 2 \cdot \phi_{TD} \cdot \ln F_{TD,bot}$$

(50-46)

$$V_{bi,bot} = U_{bi,bot} + \phi_{TD} \cdot \ln\left[1 + \exp\left(\frac{V_{bi,low} - U_{bi,bot}}{\phi_{TD}}\right)\right]$$

(50-47)

$$U_{bi,sti} = VBIRSTI \cdot \frac{T_{KD}}{T_{KR}} - 2 \cdot \phi_{TD} \cdot \ln F_{TD,sti}$$

(50-48)

$$V_{bi,sti} = U_{bi,sti} + \phi_{TD} \cdot \ln\left[1 + \exp\left(\frac{V_{bi,low} - U_{bi,sti}}{\phi_{TD}}\right)\right]$$

(50-49)

$$U_{bi,gat} = VBIRGAT \cdot \frac{T_{KD}}{T_{KR}} - 2 \cdot \phi_{TD} \cdot \ln F_{TD,gat}$$

(50-50)

© 2023 Cadence Design Systems, Inc.

$$V_{bi,\,gat} = U_{bi,\,gat} + \phi_{TD} \cdot \ln\left[1 + \exp\left(\frac{V_{bi,\,low} - U_{bi,\,gat}}{\phi_{TD}}\right)\right]$$

Determination of VF, min and Vch

(50-51)

$$V_{bi,\,min} = min(V_{bi,\,bot}, V_{bi,\,sti}, V_{bi,\,gat})$$

(50-52)

$$V_{F,\,min} = \begin{cases} V_{bi,\,min} \cdot (1 - a^{-1/(PBOT)}) & if \quad V_{bi,\,min} = V_{bi,\,bot} \\ V_{bi,\,min} \cdot (1 - a^{-1/(PSTI)}) & if \quad V_{bi,\,min} = V_{bi,\,sti} \\ V_{bi,\,min} \cdot (1 - a^{-1/(PGAT)}) & if \quad V_{bi,\,min} = V_{bi,\,gat} \end{cases}$$

(50-53)

$$V_{ch} = \varepsilon_{ch} \cdot V_{bi,\,min}$$

Voltage Difference VAK

(50-54)

$$V_{AK} = TYPE \cdot (V_A - V_K)$$

Final Junction Current

(50-55)

$$I_j = TYPE \cdot MULT \cdot (AB \cdot I'_{j,\,bot} + LS \cdot I'_{j,\,sti} + LG \cdot I'_{j,\,gat})$$

© 2023 Cadence Design Systems, Inc.

Auxiliary Equations

(50-56)

$$hyp_1(x;\varepsilon) = \frac{1}{2} \cdot \left(x + \sqrt{x^2 + 4 \cdot \varepsilon^2} \right)$$

(50-57)

$$hyp_2(x;x_0, \varepsilon) = x - hyp_1(x - x_0, \varepsilon)$$

(50-58)

$$hyp_5(x;x_0, \varepsilon) = x_0 - hyp_1\left(x_0 - x - \frac{\varepsilon^2}{x_0};\varepsilon \right)$$

Related Topics

DIODE_CMC Model

Model Equations

Model Usage

Component Statements

Model Version and Development

MMSIM supports `DIODE_CMC` model version 1.0.0 and 2.0.0. The current available version for `DIODE_CMC` is version 2.0.0.

Version Update and Enhancement

Version 2.0.0 Enhancement

Following enhancements have been made in version 2.0.0:

- Internal node AIK has been added

© 2023 Cadence Design Systems, Inc.

- NQS recovery mode has been added.
- Following parameters have been added for NQS recovery mode: `corecovery`, `njh`, `njdv`, `ndibot`, `ndigat`, `ndisti`, `inj1`, `inj2`, `nqs`, `tau`, `wi`, `depnqs`, `tnom`, `taut`, `injt`, and `qrr`.

Related Topics

DIODE_CMC Model

Model Equations

Model Usage

Component Statements

Model Usage

Instance Syntax

```
Name  a  k ModelName parameter=value ...
```

Sample Instance Statement

```
m1 (v1 v2 v3) angelov_gan trise=20
```

Model Syntax

```
model modelName diode_cmc parameter=value ...
```

Related Topics

DIODE_CMC Model

Model Equations

Model Version and Development

Component Statements

© 2023 Cadence Design Systems, Inc.

Component Statements

This device is supported within altergroups.

Instance Parameters

`ab=1E-12 m`^{2}	Junction area.
`area=1E-12`	Junction area.
`ls=1e-6 m`	STI-edge part of junction perimeter.
`pj=1e-6`	STI-edge part of junction perimeter.
`perim=1e-6`	STI-edge part of junction perimeter.
`lg=0 m`	Gate-edge part of junction perimeter.
`mult=1`	Number of devices in parallel.
`m=1`	Number of devices in parallel.
`trise=0.0`	Temperature rise from the ambient.
`region=on`	Estimated operating region. Spectre generates output number (0-2) in a rawfile. Possible values are `off`, `on`, and `breakdown`.
`isnoisy=yes`	Should the device generate noise. Possible values are `yes` and `no`.

Model Parameters

`level=1002`	Model level must be 1002.
`version=1`	Model version.
`subversion=0`	Model subversion.
`revision=0`	Model revision.
`type=n`	Type parameter, n reflects n-type, p reflects p-type. Possible values are `n` and `p`.
`dta=0 C`	Temperature offset with respect to ambient temperature.
`imax=1000 A`	Maximum current up to which forward current behaves exponentially.

© 2023 Cadence Design Systems, Inc.

`trj=21 C`	Reference temperature.
`cjorbot=1E-3 Fm`$^{-2}$	Zero-bias capacitance per unit-of-area of bottom component.
`cjorsti=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of STI-edge component.
`cjorgat=1E-9 Fm^-1`	Zero-bias capacitance per unit-of-length of gate-edge component.
`vbirbot=1 V`	Built-in voltage at the reference temperature of bottom component.
`vbirsti=1 V`	Built-in voltage at the reference temperature of STI-edge component.
`vbirgat=1 V`	Built-in voltage at the reference temperature of gate-edge component.
`pbot=0.5`	Grading coefficient of bottom component.
`psti=0.5`	Grading coefficient of STI-edge component.
`pgat=0.5`	Grading coefficient of gate-edge component.
`phigbot=1.16 V`	Zero-temperature bandgap voltage of bottom component.
`phigsti=1.16 V`	Zero-temperature bandgap voltage of STI-edge component.
`phiggat=1.16 V`	Zero-temperature bandgap voltage of gate-edge component.
`idsatrbot=1E-12 Am`$^{-2}$	Saturation current density at the reference temperature of bottom component.
`idsatrsti=1E-18 Am^-1`	Saturation current density at the reference temperature of STI-edge component.
`idsatrgat=1E-18 Am^-1`	

© 2023 Cadence Design Systems, Inc.

	Saturation current density at the reference temperature of gate-edge component.
csrhbot=1E2 Am^{-3}	Shockley-Read-Hall prefactor of bottom component.
csrhsti=1E-4 Am^{-2}	Shockley-Read-Hall prefactor of STI-edge component.
csrhgat=1E-4 Am^{-2}	Shockley-Read-Hall prefactor of gate-edge component.
xjunsti=100E-9 m	Junction depth of STI-edge component.
xjungat=100E-9 m	Junction depth of gate-edge component.
ctatbot=1E2 Am^{-3}	Trap-assisted tunneling prefactor of bottom component.
ctatsti=1E-4 Am^{-2}	Trap-assisted tunneling prefactor of STI-edge component.
ctatgat=1E-4 Am^{-2}	Trap-assisted tunneling prefactor of gate-edge component.
mefftatbot=0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component.
mefftatsti=0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component.
mefftatgat=0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component.
cbbtbot=1E-12 AV^{-3}	Band-to-band tunneling prefactor of bottom component.
cbbtsti=1E-18 $AV^{-3}m$	Band-to-band tunneling prefactor of STI-edge component.
cbbtgat=1E-18 $AV^{-3}m$	Band-to-band tunneling prefactor of gate-edge component.
fbbtrbot=1E9 Vm^-1	Normalization field at the reference temperature for band-to-band tunneling of bottom component.
fbbtrsti=1E9 Vm^-1	

© 2023 Cadence Design Systems, Inc.

	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component.
`fbbtrgat=1E9 Vm^-1`	
	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component.
`stfbbtbot=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of bottom component.
`stfbbtsti=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of STI-edge component.
`stfbbtgat=(-1E-3) K^-1`	
	Temperature scaling parameter for band-to-band tunneling of gate-edge component.
`vbrbot=10 V`	Breakdown voltage of bottom component.
`vbrsti=10 V`	Breakdown voltage of STI-edge component.
`vbrgat=10 V`	Breakdown voltage of gate-edge component.
`pbrbot=4 V`	Breakdown onset tuning parameter of bottom component.
`pbrsti=4 V`	Breakdown onset tuning parameter of STI-edge component.
`pbrgat=4 V`	Breakdown onset tuning parameter of gate-edge component.
`rsbot=0.0 VA^-1m`^{2}	
	Series resistance per unit-of-area of bottom component.
`rssti=0.0 VA^-1m`	Series resistance per unit-of-length of STI-edge component.
`rsgat=0.0 VA^-1m`	Series resistance per unit-of-length of gate-edge component.
`rscom=0.0 ohm`	Common series resistance, no scaling.
`strs=0`	Temperature scaling parameter for series resistance.
`kf=0`	KF parameter for flicker noise.
`af=1.0`	AF parameter for flicker noise.

© 2023 Cadence Design Systems, Inc.

`tt=0 s`	Transit time.
`stvbrbot1=0 1/K`	Temp. co of breakdown voltage bottom component.
`stvbrbot2=0 1/K`^{2}	Temp. co of breakdown voltage bottom component.
`stvbrsti1=0 1/K`	Temp. co of breakdown voltage STI-edge component.
`stvbrsti2=0 1/K`^{2}	Temp. co of breakdown voltage STI-edge component.
`stvbrgat1=0 1/K`	Temp. co of breakdown voltage gate-edge component.
`stvbrgat2=0 1/K`^{2}	Temp. co of breakdown voltage gate-edge component.
`nfabot=1.0`	ideality factor bottom component.
`nfasti=1.0`	ideality factor STI-edge component.
`nfagat=1.0`	ideality factor gate-edge component.
`abmin=0.0 m`^{2}	minimum allowed junction area.
`abmax=1.0 m`^{2}	maximum allowed junction area.
`lsmin=0.0 m`	minimum allowed junction STI-edge.
`lsmax=1.0 m`	maximum allowed junction STI-edge.
`lgmin=0.0 m`	minimum allowed junction gate-edge.
`lgmax=1.0 m`	maximum allowed junction gate-edge.
`tempmin=(-55) C`	minimum allowed junction temp.
`tempmax=155 C`	maximum allowed junction temp.
`vfmax=0.0 V`	maximum allowed forward junction bias.
`vrmax=0.0 V`	maximum allowed reverse junction bias.
`pt=3`	Temp. co of saturation current.
`xti=3`	Temp. co of saturation current.
`scalee=1.0`	Scale parameter.
`shrink=0`	Scale parameter.
`swjunexp=0.0`	Flag for JUNCAP-express; 0=full model, 1=express model.
`vjunref=2.5`	Typical maximum junction voltage; usually about 2*VSUP.
`fjunq=0.03`	Fraction below which junction capacitance components are considered negligible.
`corecovery`	Flag for recovery equations; 0=original and 1=hiroshima

© 2023 Cadence Design Systems, Inc.

`njh=1.0`	High-injection emission coefficient.
`njdv=0.1 1/V`	Transition slope of emission coefficient
`ndibot=1e16 cm^-3`	Doping concentration of drift region.
`ndigat=1e16 cm^-3`	Doping concentration of drift region.
`ndisti=1e16 cm^-3`	Doping concentration of drift region.
`inj1=1.0`	For carrier density.
`inj2=10.0`	For carrier density in high-density injection.
`nqs=5e-9 sec`	Carrier delay time.
`tau=2e-7 sec`	Carrier lifetime.
`wi=5e-6 m`	Length of drift region.
`depnqs=0.0 sec`	Depletion delay time.
`tnom=21 C`	Alias reference temperature.
`taut=0.0`	Temperature coefficient of carrier lifetime.
`injt=0.0`	Temperature coefficient of carrier density in high injection condition.

Output Parameters

`tempeff (C)`	Effective temperature for a single device.
`meff`	Effective multiplicity factor (m factor)

Operating-Point Parameters

`region=on`	Estimated operating region. Spectre generates output number (0-2) in a rawfile. Possible values are `off`, `on`, and `breakdown`.
`vak (V)`	Voltage between anode and cathode excluding the series resistor.
`cj (F)`	Total source junction capacitance.
`cjbot (F)`	Junction capacitance (bottom component).

© 2023 Cadence Design Systems, Inc.

`cjgat (F)`	Junction capacitance (gate-edge component).
`cjsti (F)`	Junction capacitance (STI-edge component).
`ij (A)`	Total source junction current.
`ijbot (A)`	Junction current (bottom component).
`ijgat (A)`	Junction current (gate-edge component).
`ijsti (A)`	Junction current (STI-edge component).
`si (A`^{2}`/Hz)`	Total junction current noise spectral density.
`vrs (V)`	Voltage across series resistor.
`sf (A`^{2}`/Hz)`	Total junction flicker noise spectral density.
`sr (A`^{2}`/Hz)`	Total series resistor thermal noise spectral density.
`rseries (V/A)`	Series resistor.
`qrr (C)`	Recovery charge.

Related Topics

DIODE_CMC Model

Model Equations

Model Equations

Model Usage

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

51

JFET100 Model

JFET100 is a new model developed by TSMC.

Instance Definition

```
Name  d  g  s  e ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

1	`l=1.0e-6`	Drawn Length.
2	`w=1.0e-6`	Drawn Width.
3	`nf=1.0`	Number of finger.
4	`as=1.0e-12`	Source diffusion area.
5	`ad=1.0e-12`	Drain diffusion area.
6	`ps=1.0e-6`	Source diffusion perimeter.
7	`pd=1.0e-6`	Drain diffusion perimeter.
8	`nrs=1.0`	Number of squares of drain diffusion for resistance calculations.
9	`nrd=1.0`	Number of squares of source diffusion for resistance calculations.
10	`lgs=1.0e-6`	Space of source to gate open.
11	`lgd=1.0e-6`	Space of drain to gate open.
12	`dtemp=0`	Temperature offset.
13	`ids0mult=1`	Variability in Drain current for misc. reasons.
14	`flk0mult=1`	Variability in Noise.
15	`q0mult=1`	Variability in AC.
16	`trise=0`	Alias of DTEMP.
17	`m=1.0`	Multiplicity factor (number of MOSFETs in parallel).
18	`isnoisy=yes`	Should the device enable noise calculation. Possible values are `yes and no`.

Model Definition

```
model modelName jfet100 parameter=value ...
```

Model Parameters

1	`level=100`	Level number of the JFET model.
2	`version=0.4`	Version number of the JFET model.

© 2023 Cadence Design Systems, Inc.

3	`type=1`	Device type: ntype(1), ptype(-1). Possible values are `p` and `n`.
4	`shmod=0`	Self-heating mode: off(0), on(1).
5	`capmod=1`	Capacitance mode: single depletion capacitor model(0), double depletion capacitor model(1).
6	`cdsmod=0`	Capacitance mode: constant cds capacitor model(0), single-step cds capacitor model(1).
7	`resmod=0`	Resistance mode: without internal drain resistance(0), with internal drain resistance(1).
8	`betatempmod=1`	Temperature dependence mode of BETA.
9	`tlevc=1`	Temperature dependence mode of capacitance.
10	`tlev=1`	Temperature dependence mode of bandgap evaluation.
11	`xl=0.0`	Length offset.
12	`dlc=0.0`	Length offset in CV evaluation.
13	`xw=0.0`	Width offset.
14	`dwc=0.0`	Width offset in CV evaluation.
15	`rg=0.0`	Gate resistance.
16	`rs=0.0`	Source resistance.
17	`rd=0.0`	Drain resistance.
18	`rdis=0.0`	The resistance in series with the gate-source diode.
19	`rdid=0.0`	The resistance in series with the gate-drain diode.
20	`tnom=25.0`	
21	`eg=1.16`	Energy bandgap for the gate-drain and gate-source diode for TLEV=2.
22	`gap1=7.02e-4`	First bandgap correction factor for TLEV=2.
23	`gap2=1108`	Second bandgap correction factor for TLEV=2.
24	`shconst=5.0`	Temperature smoothing constant.
25	`ifwdlimit=0.01`	Limiting current for the forward gate-drain and gate-source diode per Weff.

© 2023 Cadence Design Systems, Inc.

26	`iss=1.0e-14`	Saturation current of the gate-source diode per unit area.
27	`nsf=5.0`	Emission coefficient of the gate-source diode.
28	`its=1.0e-14`	Tunneling saturation current of the gate-source diode per unit area.
29	`nts=10.0`	Tunneling emission coefficient of the gate-source diode.
30	`vts=10.0`	Trap-assisted voltage dependent parameter of the gate-source diode.
31	`offsets=0.0`	Offset voltage in evaluating tunneling current of the gate-source diode.
32	`isd=1.0e-14`	Saturation current of the gate-drain diode per unit area.
33	`ndf=5.0`	Emission coefficient of the gate-drain diode.
34	`itd=1.0e-14`	Tunneling saturation current of the gate-drain diode per unit area.
35	`ntd=10.0`	Tunneling emission coefficient of the gate-drain diode.
36	`vtd=10.0`	Trap-assisted voltage dependent parameter of the gate-drain diode.
37	`offsetd=0.0`	Offset voltage in evaluating tunneling current of the gate-drain diode.
38	`alpha=2.0`	Saturation factor.
39	`beta=1.0e-4`	Transconductance parameter.
40	`delta=0.0`	Ids feedback parameter.
41	`gamds=0.0`	Drain induced threshold voltage lowering coefficient.
42	`lambda=0.0`	Channel length modulation parameter.
43	`k1=0.0`	Threshold voltage sensitivity to body bias.
44	`nd=0.0`	Drain subthreshold factor.
45	`ng=0.0`	Gate subthreshold factor.
46	`mstar=0.5`	Fitting factor for moderate inversion condition.
47	`subconst=100.0e-3`	

© 2023 Cadence Design Systems, Inc.

		Fitting factor for the subthreshold swing.
48	`ucrit=0.0`	Critical field for mobility degradation.
49	`vgexp=2.0`	Gate voltage exponent.
50	`vto=(-2.0)`	Threshold voltage.
51	`voff=0.0`	Offset voltage in subthreshold region.
52	`satexp=3.0`	Drain voltage exponent.
53	`gdsmin=0.0`	The leakage path from drain to source.
54	`cvto=0.0`	Threshold voltage for CV model.
55	`calpha=4.0e-2`	Saturation factor for CV model.
56	`cgamds=0.0`	Drain induced threshold voltage lowering coefficient for CV model.
57	`ck1=0.0`	Body bias dependence factor for CV model.
58	`cgs=0.0`	Zero-bias gate-source junction capacitance.
59	`cgd=0.0`	Zero-bias gate-drain junction capacitance.
60	`mjs=0.5`	Grading coefficient for gate-source diode.
61	`mjd=0.5`	Grading coefficient for gate-drain diode.
62	`cgd1=0.0`	Zero-bias gate-drain junction capacitance for the second depletion capacitance (only for CAPMOD=1).
63	`cgs1=0.0`	Zero-bias gate-source junction capacitance for the second depletion capacitance (only for CAPMOD=1).
64	`mjs1=0.2`	Grading coefficient for the second depletion gate-source diode (only for CAPMOD=1).
65	`mjd1=0.2`	Grading coefficient for the second depletion gate-drain diode (only for CAPMOD=1).
66	`pb=0.8`	Gate junction potential.
67	`fc=0.9`	Coefficient for forward-bias depletion capacitance formulas.
68	`cvtd=0.0`	Second threshold voltage for CV model.
69	`calphad=4.0e-2`	Second Saturation factor for CV model.
70	`covs=0.0`	Overlap capacitance between gate and source.
71	`covd=0.0`	Overlap capacitance between gate and drain.

© 2023 Cadence Design Systems, Inc.

72	`cvtds=0.0`	First switching voltage for the step like drain-source capacitance (only for CDSMOD=1).
73	`cvtds1=0.0`	Second switching voltage for the step like drain-source capacitance (only for CDSMOD=1).
74	`cvtds2=0.0`	Third switching voltage for the step like drain-source capacitance (only for CDSMOD=1).
75	`calphads=2.0`	First saturation factor for drain-source capacitance (only for CDSMOD=1).
76	`calphads1=2.0`	Second saturation factor for drain-source capacitance (only for CDSMOD=1).
77	`calphads2=2.0`	Third saturation factor for drain-source capacitance (only for CDSMOD=1).
78	`mjds=0.5`	Grading coefficient for the first drain-source capacitance (only for CDSMOD=1).
79	`mjds1=0.5`	Grading coefficient for the second drain-source capacitance (only for CDSMOD=1).
80	`mjds2=0.5`	Grading coefficient for the third drain-source capacitance (only for CDSMOD=1).
81	`mjds3=0.5`	Grading coefficient for the fourth drain-source capacitance (only for CDSMOD=1).
82	`capds=0.0`	Capacitance between drain and source.
83	`capds1=0.0`	Zero-bias drain-source capacitance for the second capacitance (only for CDSMOD=1).
84	`capds2=0.0`	Zero-bias drain-source capacitance for the third capacitance (only for CDSMOD=1).
85	`capds3=0.0`	Zero-bias drain-source capacitance for the fourth capacitance (only for CDSMOD=1).
86	`pbds=0.8`	First Drain-source junction potential (only for CDSMOD=1).
87	`pbds1=0.8`	Second Drain-source junction potential (only for CDSMOD=1).

© 2023 Cadence Design Systems, Inc.

88	`pbds2=0.8`	Third Drain-source junction potential (only for CDSMOD=1).
89	`fcds=0.9`	Coefficient for forward-bias drain-source capacitance formulas (only for CDSMOD=1).
90	`capsb=0.0`	Capacitance between source and body.
91	`capdb=0.0`	Capacitance between drain and body.
92	`capgb=0.0`	Capacitance between gate and body.
93	`xtis=0.0`	Junction current temperature exponent for gate-source diode.
94	`xtid=0.0`	Junction current temperature exponent for gate-drain diode.
95	`xts=0.0`	Power dependence of ITS.
96	`tnts=0.0`	Temperature coefficient of NTS.
97	`xtd=0.0`	Power dependence of ITD.
98	`tntd=0.0`	Temperature coefficient of NTD.
99	`tvto=0.0`	Temperature coefficient of VTO.
100	`tvoff=0.0`	Temperature coefficient of VOFF.
101	`tgamds=0.0`	Temperature coefficient of GAMDS.
102	`tdelta=0.0`	Temperature coefficient of DELTA.
103	`trg1=0.0`	First order temperature cofficient of RG.
104	`trs1=0.0`	First order temperature cofficient of RS.
105	`trd1=0.0`	First order temperature cofficient of RD.
106	`trg2=0.0`	Second order temperature cofficient of RG.
107	`trs2=0.0`	Second order temperature cofficient of RS.
108	`trd2=0.0`	Second order temperature cofficient of RD.
109	`trdis1=0.0`	First order temperature cofficient of RDIS.
110	`trdid1=0.0`	First order temperature cofficient of RDID.
111	`trdis2=0.0`	Second order temperature cofficient of RDIS.
112	`trdid2=0.0`	

© 2023 Cadence Design Systems, Inc.

		Second order temperature cofficient of RDIS.
113	`ctd=0.0`	Temperature coefficient of CGD (TLEVC=1).
114	`cts=0.0`	Temperature coefficient of CGS (TLEVC=1).
115	`tpb=0.0`	Temperature coefficient of PB (TLEVC=1, 2).
116	`tfbex=1.0`	Temperature factor for BEX.
117	`bex1=0.0`	First order temperature cofficient of mobility exponent.
118	`bex2=0.0`	Second order temperature cofficient of mobility exponent.
119	`tfvgexp=1.0`	Temperature factor for VGEXP.
120	`vgexpt1=0.0`	First order temperature cofficient of gate voltage exponent.
121	`vgexpt2=0.0`	Second order temperature cofficient of gate voltage exponent.
122	`tcvto=0.0`	Temperature coefficient of CVTO.
123	`tcgamds=0.0`	Temperature coefficient of CGAMDS.
124	`tcvtds=0.0`	Temperature coefficient of CVTDS (CDSMOD=1).
125	`ctds=0.0`	Temperature coefficient of CAPDS and CAPDS1 (CDSMOD=1).
126	`tcvtd=0.0`	
127	`tpbds=0.0`	Temperature coefficient of PBDS (CDSMOD=1)).
128	`trdv1=0.0`	First order temperature cofficient of RDV.
129	`trdv2=0.0`	Second order temperature cofficient of RDV.
130	`trdvg1=0.0`	First order temperature cofficient of RDVG.
131	`tvdeff1=0.0`	First order temperature cofficient of VDEFF.
132	`tvdmr1=0.0`	First order temperature cofficient of VDMR.
133	`kf=0.0`	Flicker noise coefficient.
134	`af=1.0`	Flicker noise exponent.
135	`ef=1.0`	Flicker noise frequency exponent.
136	`gdsnoi=1.0`	Channel noise coefficient.
137	`rth0=0.01`	Thermal resistance.

© 2023 Cadence Design Systems, Inc.

138	`cth0=1.0E-05`	Thermal capacitance.
139	`shlimit=(-1.0)`	Limit of temperature change due to self-heating; if it is negative, there is no limit.
140	`wth0=0.0`	Minimum width for thermal.
141	`ls=2.5e-6`	Length of ohmic open at source side.
142	`ld=2.5e-6`	Length of ohmic open at drain side.
143	`lfp=1.0e-6`	Source side field plate.
144	`pfp=1.0e-6`	Gate side field plate.
145	`rdv=0.0`	Voltage dependent RD coefficient.
146	`rdvg=0.2`	Gate-bias dependent RD parameter.
147	`vdeff=1.0`	Drain-bias exponent RD parameter.
148	`vdmr=500`	Drain-bias dependent RD parameter.
149	`liss=0.0`	Length dependence of iss.
150	`wiss=0.0`	Width dependence of iss.
151	`piss=0.0`	Cross-term dependence of iss.
152	`lnsf=0.0`	Length dependence of nsf.
153	`wnsf=0.0`	Width dependence of nsf.
154	`pnsf=0.0`	Cross-term dependence of nsf.
155	`lxtis=0.0`	Length dependence of xtis.
156	`wxtis=0.0`	Width dependence of xtis.
157	`pxtis=0.0`	Cross-term dependence of xtis.
158	`lits=0.0`	Length dependence of its.
159	`wits=0.0`	Width dependence of its.
160	`pits=0.0`	Cross-term dependence of its.
161	`lnts=0.0`	Length dependence of nts.
162	`wnts=0.0`	Width dependence of nts.
163	`pnts=0.0`	Cross-term dependence of nts.
164	`lxts=0.0`	Length dependence of xts.
165	`wxts=0.0`	Width dependence of xts.

© 2023 Cadence Design Systems, Inc.

166	`pxts=0.0`	Cross-term dependence of xts.
167	`lvts=0.0`	C dependence of vts.
168	`wvts=0.0`	Width dependence of vts.
169	`pvts=0.0`	Cross-term dependence of vts.
170	`ltnts=0.0`	Length dependence of tnts.
171	`wtnts=0.0`	Width dependence of tnts.
172	`ptnts=0.0`	Cross-term dependence of tnts.
173	`lisd=0.0`	Length dependence of isd.
174	`wisd=0.0`	Width dependence of isd.
175	`pisd=0.0`	Cross-term dependence of isd.
176	`lndf=0.0`	Length dependence of ndf.
177	`wndf=0.0`	Width dependence of ndf.
178	`pndf=0.0`	Cross-term dependence of ndf.
179	`lxtid=0.0`	Length dependence of xtid.
180	`wxtid=0.0`	Width dependence of xtid.
181	`pxtid=0.0`	Cross-term dependence of xtid.
182	`litd=0.0`	Length dependence of itd.
183	`witd=0.0`	Width dependence of itd.
184	`pitd=0.0`	Cross-term dependence of itd.
185	`lntd=0.0`	Length dependence of ntd.
186	`wntd=0.0`	Width dependence of ntd.
187	`pntd=0.0`	Cross-term dependence of ntd.
188	`lxtd=0.0`	Length dependence of xtd.
189	`wxtd=0.0`	Width dependence of xtd.
190	`pxtd=0.0`	Cross-term dependence of xtd.
191	`lvtd=0.0`	Length dependence of vtd.
192	`wvtd=0.0`	Width dependence of vtd.
193	`pvtd=0.0`	Cross-term dependence of vtd.
194	`ltntd=0.0`	Length dependence of tntd.

© 2023 Cadence Design Systems, Inc.

195	`wtntd=0.0`	Width dependence of tntd.
196	`ptntd=0.0`	Cross-term dependence of tntd.
197	`lalpha=0.0`	Length dependence of alpha.
198	`walpha=0.0`	Width dependence of alpha.
199	`palpha=0.0`	Cross-term dependence of alpha.
200	`lbeta=0.0`	Length dependence of beta.
201	`wbeta=0.0`	Width dependence of beta.
202	`pbeta=0.0`	Cross-term dependence of beta.
203	`ldelta=0.0`	Length dependence of delta.
204	`wdelta=0.0`	Width dependence of delta.
205	`pdelta=0.0`	Cross-term dependence of delta.
206	`lgamds=0.0`	Length dependence of gamds.
207	`wgamds=0.0`	Width dependence of gamds.
208	`pgamds=0.0`	Cross-term dependence of gamds.
209	`llambda=0.0`	Length dependence of lambda.
210	`wlambda=0.0`	Width dependence of lambda.
211	`plambda=0.0`	Cross-term dependence of lambda.
212	`lk1=0.0`	Length dependence of k1.
213	`wk1=0.0`	Width dependence of k1.
214	`pk1=0.0`	Cross-term dependence of k1.
215	`lnd=0.0`	Length dependence of nd.
216	`wnd=0.0`	Width dependence of nd.
217	`pnd=0.0`	Cross-term dependence of nd.
218	`lng=0.0`	Length dependence of ng.
219	`wng=0.0`	Width dependence of ng.
220	`png=0.0`	Cross-term dependence of ng.
221	`lmstar=0.0`	Length dependence of mstar.
222	`wmstar=0.0`	Width dependence of mstar.
223	`pmstar=0.0`	Cross-term dependence of mstar.

© 2023 Cadence Design Systems, Inc.

224	`lsatexp=0.0`	Length dependence of satexp.
225	`wsatexp=0.0`	Width dependence of satexp.
226	`psatexp=0.0`	Cross-term dependence of satexp.
227	`lucrit=0.0`	Length dependence of ucrit.
228	`wucrit=0.0`	Width dependence of ucrit.
229	`pucrit=0.0`	Cross-term dependence of ucrit.
230	`lvgexp=0.0`	Length dependence of vgexp.
231	`wvgexp=0.0`	Width dependence of vgexp.
232	`pvgexp=0.0`	Cross-term dependence of vgexp.
233	`lvto=0.0`	Length dependence of vto.
234	`wvto=0.0`	Width dependence of vto.
235	`pvto=0.0`	Cross-term dependence of vto.
236	`lvoff=0.0`	Length dependence of voff.
237	`wvoff=0.0`	Width dependence of voff.
238	`pvoff=0.0`	Cross-term dependence of voff.
239	`lrs=0.0`	Length dependence of rs.
240	`wrs=0.0`	Width dependence of rs.
241	`prs=0.0`	Cross-term dependence of rs.
242	`lrd=0.0`	Length dependence of rd.
243	`wrd=0.0`	Width dependence of rd.
244	`prd=0.0`	Cross-term dependence of rd.
245	`lrg=0.0`	Length dependence of rg.
246	`wrg=0.0`	Width dependence of rg.
247	`prg=0.0`	Cross-term dependence of rg.
248	`lrdis=0.0`	Length dependence of rdis.
249	`wrdis=0.0`	Width dependence of rdis.
250	`prdis=0.0`	Cross-term dependence of rdis.
251	`lrdid=0.0`	Length dependence of rdid.
252	`wrdid=0.0`	Width dependence of rdid.

© 2023 Cadence Design Systems, Inc.

253	`prdid=0.0`	Cross-term dependence of rdid.
254	`lrdv=0.0`	Length dependence of rdv.
255	`wrdv=0.0`	Width dependence of rdv.
256	`prdv=0.0`	Cross-term dependence of rdv.
257	`lrdvg=0.0`	Length dependence of rdvg.
258	`wrdvg=0.0`	Width dependence of rdvg.
259	`prdvg=0.0`	Cross-term dependence of rdvg.
260	`lvdeff=0.0`	Length dependence of vdeff.
261	`wvdeff=0.0`	Width dependence of vdeff.
262	`pvdeff=0.0`	Cross-term dependence of vdeff.
263	`lvdmr=0.0`	Length dependence of vdmr.
264	`wvdmr=0.0`	Width dependence of vdmr.
265	`pvdmr=0.0`	Cross-term dependence of vdmr.
266	`ltrdv1=0.0`	Length dependence of trdv1.
267	`wtrdv1=0.0`	Width dependence of trdv1.
268	`ptrdv1=0.0`	Cross-term dependence of trdv1.
269	`ltrdv2=0.0`	Length dependence of trdv2.
270	`wtrdv2=0.0`	Width dependence of trdv2.
271	`ptrdv2=0.0`	Cross-term dependence of trdv2.
272	`ltrdvg1=0.0`	Length dependence of trdvg1.
273	`wtrdvg1=0.0`	Width dependence of trdvg1.
274	`ptrdvg1=0.0`	Cross-term dependence of trdvg1.
275	`ltrdvg2=0.0`	Length dependence of trdvg2.
276	`wtrdvg2=0.0`	Width dependence of trdvg2.
277	`ptrdvg2=0.0`	Cross-term dependence of trdvg2.
278	`ltvdeff1=0.0`	Length dependence of tvdeff1.
279	`wtvdeff1=0.0`	Width dependence of tvdeff1.
280	`ptvdeff1=0.0`	Cross-term dependence of tvdeff1.
281	`ltvdeff2=0.0`	Length dependence of tvdeff2.

© 2023 Cadence Design Systems, Inc.

282	`wtvdeff2=0.0`	Width dependence of tvdeff2.
283	`ptvdeff2=0.0`	Cross-term dependence of tvdeff2.
284	`ltvdmr1=0.0`	Length dependence of tvdmr1.
285	`wtvdmr1=0.0`	Width dependence of tvdmr1.
286	`ptvdmr1=0.0`	Cross-term dependence of tvdmr1.
287	`ltvdmr2=0.0`	Length dependence of tvdmr2.
288	`wtvdmr2=0.0`	Width dependence of tvdmr2.
289	`ptvdmr2=0.0`	Cross-term dependence of tvdmr2.
290	`lcvto=0.0`	Length dependence of cvto.
291	`wcvto=0.0`	Width dependence of cvto.
292	`pcvto=0.0`	Cross-term dependence of cvto.
293	`lcalpha=0.0`	Length dependence of calpha.
294	`wcalpha=0.0`	Width dependence of calpha.
295	`pcalpha=0.0`	Cross-term dependence of calpha.
296	`lcgamds=0.0`	Length dependence of cgamds.
297	`wcgamds=0.0`	Width dependence of cgamds.
298	`pcgamds=0.0`	Cross-term dependence of cgamds.
299	`lcvtds=0.0`	Length dependence of cvtds.
300	`wcvtds=0.0`	Width dependence of cvtds.
301	`pcvtds=0.0`	Cross-term dependence of cvtds.
302	`lcvtds1=0.0`	Length dependence of cvtds1.
303	`wcvtds1=0.0`	Width dependence of cvtds1.
304	`pcvtds1=0.0`	Cross-term dependence of cvtds1.
305	`lcvtds2=0.0`	Length dependence of cvtds2.
306	`wcvtds2=0.0`	Width dependence of cvtds2.
307	`pcvtds2=0.0`	Cross-term dependence of cvtds2.
308	`lcalphads=0.0`	Length dependence of calphads.
309	`wcalphads=0.0`	Width dependence of calphads.
310	`pcalphads=0.0`	Cross-term dependence of calphads.

© 2023 Cadence Design Systems, Inc.

311	`lcalphads1=0.0`	Length dependence of calphads1.
312	`wcalphads1=0.0`	Width dependence of calphads1.
313	`pcalphads1=0.0`	Cross-term dependence of calphads1.
314	`lcalphads2=0.0`	Length dependence of calphads2.
315	`wcalphads2=0.0`	Width dependence of calphads2.
316	`pcalphads2=0.0`	Cross-term dependence of calphads2.
317	`lcalphad=0.0`	Length dependence of calphad.
318	`wcalphad=0.0`	Width dependence of calphad.
319	`pcalphad=0.0`	Cross-term dependence of calphad.
320	`ltgamds=0.0`	Length dependence of tgamds.
321	`wtgamds=0.0`	Width dependence of tgamds.
322	`ptgamds=0.0`	Cross-term dependence of tgamds.
323	`ltvto=0.0`	Length dependence of tvto.
324	`wtvto=0.0`	Width dependence of tvto.
325	`ptvto=0.0`	Cross-term dependence of tvto.
326	`ltvoff=0.0`	Length dependence of tvoff.
327	`wtvoff=0.0`	Width dependence of tvoff.
328	`ptvoff=0.0`	Cross-term dependence of tvoff.
329	`lck1=0.0`	Length dependence of ck1.
330	`wck1=0.0`	Width dependence of ck1.
331	`pck1=0.0`	Cross-term dependence of ck1.
332	`ltcgamds=0.0`	Length dependence of tcgamds.
333	`wtcgamds=0.0`	Width dependence of tcgamds.
334	`ptcgamds=0.0`	Cross-term dependence of tcgamds.
335	`ltcvto=0.0`	Length dependence of tcvto.
336	`wtcvto=0.0`	Width dependence of tcvto.
337	`ptcvto=0.0`	Cross-term dependence of tcvto.
338	`ltcvtd=0.0`	Length dependence of tcvtd.
339	`wtcvtd=0.0`	Width dependence of tcvtd.

© 2023 Cadence Design Systems, Inc.

340	`ptcvtd=0.0`	Cross-term dependence of tcvtd.
341	`ltcvtds=0.0`	Length dependence of tcvtds.
342	`wtcvtds=0.0`	Width dependence of tcvtds.
343	`ptcvtds=0.0`	Cross-term dependence of tcvtds.
344	`ltrg1=0.0`	Length dependence of trg1.
345	`wtrg1=0.0`	Width dependence of trg1.
346	`ptrg1=0.0`	Cross-term dependence of trg1.
347	`ltrg2=0.0`	Length dependence of trg2.
348	`wtrg2=0.0`	Width dependence of trg2.
349	`ptrg2=0.0`	Cross-term dependence of trg2.
350	`ltrs1=0.0`	Length dependence of trs1.
351	`wtrs1=0.0`	Width dependence of trs1.
352	`ptrs1=0.0`	Cross-term dependence of trs1.
353	`ltrs2=0.0`	Length dependence of trs2.
354	`wtrs2=0.0`	Width dependence of trs2.
355	`ptrs2=0.0`	Cross-term dependence of trs2.
356	`ltrd1=0.0`	Length dependence of trd1.
357	`wtrd1=0.0`	Width dependence of trd1.
358	`ptrd1=0.0`	Cross-term dependence of trd1.
359	`ltrd2=0.0`	Length dependence of trd2.
360	`wtrd2=0.0`	Width dependence of trd2.
361	`ptrd2=0.0`	Cross-term dependence of trd2.
362	`ltrdis1=0.0`	Length dependence of trdis1.
363	`wtrdis1=0.0`	Width dependence of trdis1.
364	`ptrdis1=0.0`	Cross-term dependence of trdis1.
365	`ltrdis2=0.0`	Length dependence of trdis2.
366	`wtrdis2=0.0`	Width dependence of trdis2.
367	`ptrdis2=0.0`	Cross-term dependence of trdis2.
368	`ltrdid1=0.0`	Length dependence of trdid1.

© 2023 Cadence Design Systems, Inc.

369	`wtrdid1=0.0`	Width dependence of trdid1.
370	`ptrdid1=0.0`	Cross-term dependence of trdid1.
371	`ltrdid2=0.0`	Length dependence of trdid2.
372	`wtrdid2=0.0`	Width dependence of trdid2.
373	`ptrdid2=0.0`	Cross-term dependence of trdid2.
374	`ltpb=0.0`	Length dependence of tpb.
375	`wtpb=0.0`	Width dependence of tpb.
376	`ptpb=0.0`	Cross-term dependence of tpb.
377	`ltpbds=0.0`	Length dependence of tpbds.
378	`wtpbds=0.0`	Width dependence of tpbds.
379	`ptpbds=0.0`	Cross-term dependence of tpbds.
380	`lbex1=0.0`	Length dependence of bex1.
381	`wbex1=0.0`	Width dependence of bex1.
382	`pbex1=0.0`	Cross-term dependence of bex1.
383	`lbex2=0.0`	Length dependence of bex2.
384	`wbex2=0.0`	Width dependence of bex2.
385	`pbex2=0.0`	Cross-term dependence of bex2.
386	`ltdelta=0.0`	Length dependence of tdelta.
387	`wtdelta=0.0`	Width dependence of tdelta.
388	`ptdelta=0.0`	Cross-term dependence of tdelta.
389	`lvgexpt1=0.0`	Length dependence of vgexpt1.
390	`wvgexpt1=0.0`	Width dependence of vgexpt1.
391	`pvgexpt1=0.0`	Cross-term dependence of vgexpt1.
392	`lvgexpt2=0.0`	Length dependence of vgexpt2.
393	`wvgexpt2=0.0`	Width dependence of vgexpt2.
394	`pvgexpt2=0.0`	Cross-term dependence of vgexpt2.
395	`lrth0=0.0`	Length dependence of rth0.
396	`wrth0=0.0`	Width dependence of rth0.
397	`prth0=0.0`	Cross-term dependence of rth0.

© 2023 Cadence Design Systems, Inc.

398	`lcth0=0.0`	Length dependence of cth0.
399	`wcth0=0.0`	Width dependence of cth0.
400	`pcth0=0.0`	Cross-term dependence of cth0.
401	`vds_max=infinity V`	Maximum allowed voltage cross source and drain.
402	`vgd_max=infinity V`	Maximum allowed voltage cross gate and drain.
403	`vgs_max=infinity V`	Maximum allowed voltage cross gate and source/bulk.
404	`vbd_max=infinity V`	Maximum allowed voltage cross source/drain and bulk.
405	`vbs_max=vbd_max V`	Maximum allowed voltage cross source and bulk.
406	`vgb_max=infinity V`	Maximum allowed voltage cross gate and bulk.
407	`vgdr_max=vgd_max V`	Maximum allowed reverse voltage cross gate and drain.
408	`vgsr_max=vgs_max V`	Maximum allowed reverse voltage cross gate and source.
409	`vgbr_max=vgb_max V`	Maximum allowed reverse voltage cross gate and bulk.
410	`vbsr_max=vbs_max V`	Maximum allowed reverse voltage cross source and bulk.
411	`vbdr_max=vbd_max V`	Maximum allowed reverse voltage cross source/drain and bulk.

© 2023 Cadence Design Systems, Inc.

412	`wmax=1.0 m`	Maximum channel width for which the model is valid.
413	`wmin=0.0 m`	Minimum channel width for which the model is valid.
414	`lmax=1.0 m`	Maximum channel length for which the model is valid.
415	`lmin=0.0 m`	Minimum channel length for which the model is valid.

Output Parameters

1	`weff`	Effective channel width.
2	`leff`	Effective channel length.
3	`weffcv`	Effective channel width for CV.
4	`leffcv`	Effective channel length for CV.
5	`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

1	`devtemper`	Device temperature.
2	`ids (A)`	Channel Current.
3	`igs (A)`	Gate-to-source Current.
4	`igd (A)`	Gate-to-drain Current.
5	`vgs (V)`	Voltage difference between the terminals of the gate-source diode for IV evaluation.
6	`vgd (V)`	Voltage difference between the terminals of the gate-drain diode for IV evaluation.
7	`vgscv (V)`	Voltage difference between the terminals of the gate-source diode for CV evaluation.
8	`vgdcv (V)`	Voltage difference between the terminals of the gate-drain diode for CV evaluation.
9	`vth (V)`	Threshold voltage.
10	`gm`	Transconductance.
11	`gds`	Conductance.

© 2023 Cadence Design Systems, Inc.

12	cgd (C)	Intrinsic gate-to-drain capacitance.
13	cgs (C)	Intrinsic gate-to-drain capacitance.
14	pwr (W)	Power dissipation.

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

ad I-5
af M-134
alpha M-38
as I-4
beta M-39
betatempmod M-8
bex1 M-117
bex2 M-118
calpha M-55
calphad M-69
calphads M-75
calphads1 M-76
calphads2 M-77
capdb M-91
lrdv M-254
lrdvg M-257
lrg M-245
lrs M-239
lrth0 M-395
ls M-141
lsatexp M-224
ltcgamds M-332
ltcvtd M-338
ltcvtds M-341
ltcvto M-335
ltdelta M-386
ltgamds M-320
ltntd M-194
prdv M-256
prdvg M-259
prg M-247
prs M-241
prth0 M-397
ps I-6
psatexp M-226
ptcgamds M-334
ptcvtd M-340
ptcvtds M-343
ptcvto M-337
ptdelta M-388
ptgamds M-322
ptntd M-196
vgdcv OP-8
vgdr_max M-407
vgexp M-49
vgexpt1 M-120
vgexpt2 M-121
vgs OP-5
vgs_max M-403
vgscv OP-7
vgsr_max M-408
voff M-51
vtd M-36
vth OP-9
vto M-50
vts M-30

© 2023 Cadence Design Systems, Inc.

capds M-82
capds1 M-83
capds2 M-84
capds3 M-85
capgb M-92
capmod M-5
capsb M-90
cdsmod M-6
cgamds M-56
cgd M-59
cgd OP-12
cgd1 M-62
cgs M-58
cgs OP-13
cgs1 M-63
ck1 M-57
covd M-71
covs M-70
ctd M-113
ctds M-125
cth0 M-138
ltnts M-170
ltpb M-374
ltpbds M-377
ltrd1 M-356
ltrd2 M-359
ltrdid1 M-368
ltrdid2 M-371
ltrdis1 M-362
ltrdis2 M-365
ltrdv1 M-266
ltrdv2 M-269
ltrdvg1 M-272
ltrdvg2 M-275
ltrg1 M-344
ltrg2 M-347
ltrs1 M-350
ltrs2 M-353
ltvdeff1 M-278
ltvdeff2 M-281
ltvdmr1 M-284
ltvdmr2 M-287
ptnts M-172
ptpb M-376
ptpbds M-379
ptrd1 M-358
ptrd2 M-361
ptrdid1 M-370
ptrdid2 M-373
ptrdis1 M-364
ptrdis2 M-367
ptrdv1 M-268
ptrdv2 M-271
ptrdvg1 M-274
ptrdvg2 M-277
ptrg1 M-346
ptrg2 M-349
ptrs1 M-352
ptrs2 M-355
ptvdeff1 M-280
ptvdeff2 M-283
ptvdmr1 M-286
ptvdmr2 M-289
w I-2
walpha M-198
wbeta M-201
wbex1 M-381
wbex2 M-384
wcalpha M-294
wcalphad M-318
wcalphads M-309
wcalphads1 M-312
wcalphads2 M-315
wcgamds M-297
wck1 M-330
wcth0 M-399
wcvtds M-300
wcvtds1 M-303
wcvtds2 M-306
wcvto M-291
wdelta M-204
weff O-1
weffcv O-3
wgamds M-207

© 2023 Cadence Design Systems, Inc.

cts M-114
cvtd M-68
cvtds M-72
cvtds1 M-73
cvtds2 M-74
cvto M-54
delta M-40
devtemper OP-1
dlc M-12
dtemp I-12
dwc M-14
ef M-135
eg M-21
fc M-67
fcds M-89
gamds M-41
gap1 M-22
gap2 M-23
gds OP-11
gdsmin M-53
gdsnoi M-136
ltvoff M-326
ltvto M-323
lucrit M-227
lvdeff M-260
lvdmr M-263
lvgexp M-230
lvgexpt1 M-389
lvgexpt2 M-392
lvoff M-236
lvtd M-191
lvto M-233
lvts M-167
lxtd M-188
lxtid M-179
lxtis M-155
lxts M-164
m I-14
meff O-5
mjd M-61
mjd1 M-65
mjds M-78
ptvoff M-328
ptvto M-325
pucrit M-229
pvdeff M-262
pvdmr M-265
pvgexp M-232
pvgexpt1 M-391
pvgexpt2 M-394
pvoff M-238
pvtd M-193
pvto M-235
pvts M-169
pwr OP-14
pxtd M-190
pxtid M-181
pxtis M-157
pxts M-166
rd M-17
rdid M-19
rdis M-18
rdv M-145
wisd M-174
wiss M-150
witd M-183
wits M-159
wk1 M-213
wlambda M-210
wmax M-412
wmin M-413
wmstar M-222
wnd M-216
wndf M-177
wng M-219
wnsf M-153
wntd M-186
wnts M-162
wrd M-243
wrdid M-252
wrdis M-249
wrdv M-255
wrdvg M-258
wrg M-246

© 2023 Cadence Design Systems, Inc.

gm OP-10
ids OP-2
ifwdlimit M-25
igd OP-4
igs OP-3
isd M-32
isnoisy I-15
iss M-26
itd M-34
its M-28
k1 M-43
kf M-133
l I-1
lalpha M-197
lambda M-42
lbeta M-200
lbex1 M-380
lbex2 M-383
lcalpha M-293
lcalphad M-317
lcalphads M-308
mjds1 M-79
mjds2 M-80
mjds3 M-81
mjs M-60
mjs1 M-64
mstar M-46
nd M-44
ndf M-33
nf I-3
ng M-45
nrd I-9
nrs I-8
nsf M-27
ntd M-35
nts M-29
offsetd M-37
offsets M-31
palpha M-199
pb M-66
pbds M-86
pbds1 M-87
rdvg M-146
resmod M-7
rg M-15
rs M-16
rth0 M-137
satexp M-52
shconst M-24
shlimit M-139
shmod M-4
subconst M-47
tcgamds M-123
tcvtd M-126
tcvtds M-124
tcvto M-122
tdelta M-102
tfbex M-116
tfvgexp M-119
tgamds M-101
tlev M-10
tlevc M-9
tnom M-20
wrs M-240
wrth0 M-396
wsatexp M-225
wtcgamds M-333
wtcvtd M-339
wtcvtds M-342
wtcvto M-336
wtdelta M-387
wtgamds M-321
wth0 M-140
wtntd M-195
wtnts M-171
wtpb M-375
wtpbds M-378
wtrd1 M-357
wtrd2 M-360
wtrdid1 M-369
wtrdid2 M-372
wtrdis1 M-363
wtrdis2 M-366
wtrdv1 M-267

© 2023 Cadence Design Systems, Inc.

lcalphads1 M-311
lcalphads2 M-314
lcgamds M-296
lck1 M-329
lcth0 M-398
lcvtds M-299
lcvtds1 M-302
lcvtds2 M-305
lcvto M-290
ld M-142
ldelta M-203
leff O-2
leffcv O-4
level M-1
lfp M-143
lgamds M-206
lgd I-11
lgs I-10
lisd M-173
liss M-149
litd M-182
pbds2 M-88
pbeta M-202
pbex1 M-382
pbex2 M-385
pcalpha M-295
pcalphad M-319
pcalphads M-310
pcalphads1 M-313
pcalphads2 M-316
pcgamds M-298
pck1 M-331
pcth0 M-400
pcvtds M-301
pcvtds1 M-304
pcvtds2 M-307
pcvto M-292
pd I-7
pdelta M-205
pfp M-144
pgamds M-208
pisd M-175
tntd M-98
tnts M-96
tpb M-115
tpbds M-127
trd1 M-105
trd2 M-108
trdid1 M-110
trdid2 M-112
trdis1 M-109
trdis2 M-111
trdv1 M-128
trdv2 M-129
trdvg1 M-130
trg1 M-103
trg2 M-106
trise I-13
trs1 M-104
trs2 M-107
tvdeff1 M-131
tvdmr1 M-132
tvoff M-100
wtrdv2 M-270
wtrdvg1 M-273
wtrdvg2 M-276
wtrg1 M-345
wtrg2 M-348
wtrs1 M-351
wtrs2 M-354
wtvdeff1 M-279
wtvdeff2 M-282
wtvdmr1 M-285
wtvdmr2 M-288
wtvoff M-327
wtvto M-324
wucrit M-228
wvdeff M-261
wvdmr M-264
wvgexp M-231
wvgexpt1 M-390
wvgexpt2 M-393
wvoff M-237
wvtd M-192

© 2023 Cadence Design Systems, Inc.

lits M-158
lk1 M-212
llambda M-209
lmax M-414
lmin M-415
lmstar M-221
lnd M-215
lndf M-176
lng M-218
lnsf M-152
lntd M-185
lnts M-161
lrd M-242
lrdid M-251
lrdis M-248
piss M-151
pitd M-184
pits M-160
pk1 M-214
plambda M-211
pmstar M-223
pnd M-217
pndf M-178
png M-220
pnsf M-154
pntd M-187
pnts M-163
prd M-244
prdid M-253
prdis M-250
tvto M-99
type M-3
ucrit M-48
vbd_max M-404
vbdr_max M-411
vbs_max M-405
vbsr_max M-410
vdeff M-147
vdmr M-148
vds_max M-401
version M-2
vgb_max M-406
vgbr_max M-409
vgd OP-6
vgd_max M-402
wvto M-234
wvts M-168
wxtd M-189
wxtid M-180
wxtis M-156
wxts M-165
xl M-11
xtd M-97
xtid M-94
xtis M-93
xts M-95
xw M-13

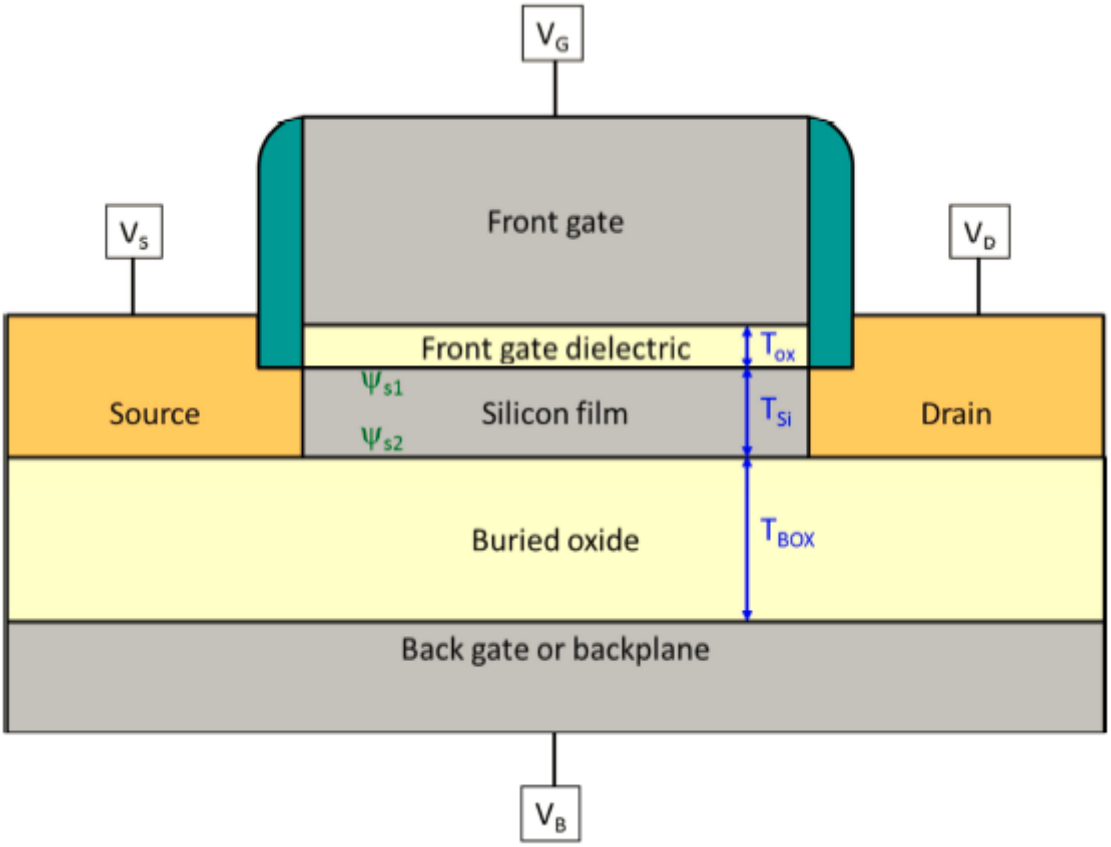
© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

52

UTSOI2 Model

UTSOI2 is the second version of the UTSOI model, compact model dedicated to Fully-Depleted on Silicon-On-Insulator (FDSOI) technologies with low-doped channel, developed at CEA-LETI. The device architecture described by this model is shown in the figure below.



This chapter contains the following information about the UTSOI2 model:

- Model Overview
  - Model Structure
- Version Update and Enhancement

© 2023 Cadence Design Systems, Inc.

- Geometrical dependences, stress effects and junction asymmetry
- Scaling Equations
- Stress Model
- Asymmetric Junctions
- Model Equations on page 3346
  - Internal Parameters Including Temperature Dependencies
  - Terminal Voltage Conditioning
  - Backplane Depletion
  - Channel Current
  - Gate Current, Intrinsic Charges and Overlap Related Variables
  - Gate Current
  - Gate Induced Drain/Source Leakage (GIDL/GISL)
  - Charge Model
  - Self-Heating
  - Noise Model
  - Total Current and Charges
- Operating Point Output
- Component Statements

© 2023 Cadence Design Systems, Inc.

Model Overview

UTSOI2 has been developed with the aim to describe device operations with a strongly inverted back interface. Therefore, an original analytical procedure has been developed to calculate the exact values of the surface potentials at front and back interfaces in all operating conditions. Besides this surface potential calculation, new drain current and intrinsic charge models have also been developed. Not that the new model core is valid not only for FDSOI technologies, but also for all Independent Double Gate device architectures.

In UTSOI2, the effect of backplane depletion, computed through a bulk MOSFET like surface potential calculation has been introduced. This effect can be activated through the value of the `SWSUBDEP` flag. If the flag is set to 0, the backplane is assumed metallic, as in UTSOI1.

UTSOI2 offers the possibility to define two different junctions at source and drain sides, as done in PSP. Junction related parameters are therefore duplicated, the drain related parameters having the same name as their source side counterparts plus a final “D”. This possible junction asymmetry can be activated using the `SWJUNASYM` flag. When it is de-activated, drain related parameters are ignored.

Starting with version 2.1.0, the temperature node of the transistor (`Tnode`), that gives channel temperature elevation induced by self-heating, is accessible from the circuit netlist (that is, declared as `inout`). Therefore, from version 2.1.0, transistor instantiation accepts five nodes: drain, gate, source, bulk, and internal temperature.

Model Structure

The model structure of utsoi2 model is the same as different versions of utsoi1 and similar to PSP3 and PSP4. It is based on the hierarchical construction featuring two levels of parameter set:

- A local mode, in which the knowledge of the device geometry (channel length and width) is not needed. In this mode, the local parameter values are directly obtained from the model cards.
- A global mode, in which the local parameters are computed from the global model card and the device geometry through scaling laws. The computed local parameters are then used to compute the model equations. In this mode, some local parameters can also be modified according to the stress model.

© 2023 Cadence Design Systems, Inc.

Version Update and Enhancement

Version 2.3.0 Enhancement

Bug fixes:

- Correction of an undesired W-scaling of Cbs and Cbd capacitances that was induced in UTSOI 2.2 for negative values of the narrow channel parameter `PNCEW`.
- Correction of a small undesired scaling of the flicker noise in the subthreshold regime as a function of gate length and back bias.

Accuracy and predictability improvements

- Implementation of the self-heating is simplified.
- Model introduced for the excess noise.
- Global scale parameters `AXL2` and `AXLEXP2` are added for more flexibility in AX scaling description.
- Global scale parameters `AGIDLO` and `DGIDLO` are added for more scaling flexibility of the GIDL model.

Changes in model inputs and outputs

- Warnings about clipping of instance, global and local parameters, and channel temperature elevation has been updated. Display is still controlled through the `SWCLIPCHK` flag.

© 2023 Cadence Design Systems, Inc.

Geometrical dependences, stress effects and junction asymmetry

Scaling Equations

Effective Dimension

Introduction of the number of fingers.

$$W_f = W/\mathbf{NF}$$
$$A_{source,f} = \mathbf{ASOURCE}/\mathbf{NF}$$
$$A_{drain,f} = \mathbf{ADRAIN}/\mathbf{NF}$$
$$P_{source,f} = \mathbf{PSOURCE}/\mathbf{NF}$$
$$P_{drain,f} = \mathbf{PDRAIN}/\mathbf{NF}$$
$$Mult_f = \mathbf{MULT}\times\mathbf{NF}$$

Effective length and width for current model.

$$L_{EN} = 10^{-6}$$
$$W_{EN} = 10^{-6}$$
$$\Delta L_{PS} = \mathbf{LVARO}\left(1+\mathbf{LVARL}\frac{L_{EN}}{L}\right)\left(1+\mathbf{LVARW}\frac{W_{EN}}{W_f}\right)$$
$$\Delta W_{OD} = \mathbf{WVARO}\left(1+\mathbf{WVARL}\frac{L_{EN}}{L}\right)\left(1+\mathbf{WVARW}\frac{W_{EN}}{W_f}\right)$$
$$L_E = L+\Delta L_{PS}-2\times\mathbf{LAP}$$
$$W_E = W_f+\Delta W_{OD}-2\times\mathbf{WOT}$$

© 2023 Cadence Design Systems, Inc.

Effective length and width of charge model.

$$L_{E,CV} = L + \Delta L_{PS} - 2\times \mathbf{LAP} + \mathbf{DLQ}$$
$$W_{E,CV} = W_f + \Delta W_{OD} - 2\times \mathbf{WOT} + \mathbf{DWQ}$$
$$L_{G,CV} = L + \Delta L_{PS} + \mathbf{DLQ}$$
$$W_{G,CV} = W_f + \Delta W_{OD} + \mathbf{DWQ}$$

Effective length and width for self heating.

$$L_{G,TH} = L + \Delta L_{PS}$$
$$W_{G,TH} = W_f + \Delta W_{OD}$$

Process Parameters

$$\mathbf{TOXE} = \mathbf{TOXEO}$$
$$\mathbf{TSI} = \mathbf{TSIO}$$
$$\mathbf{XGE} = \mathbf{XGEO}$$
$$\mathbf{TBOX} = \mathbf{TBOXO}$$
$$\mathbf{NSUB} = \mathbf{NSUBO}$$
$$\mathbf{CT} = \mathbf{CTO}$$
$$\mathbf{TOXP} = \mathbf{TOXPO}$$
$$\mathbf{NOV} = \mathbf{NOVO}$$
$$\mathbf{NOVD} = \mathbf{NOVDO}$$

$$\mathbf{VFB} = \mathbf{VFBO} + \mathbf{VFBL}\left(\frac{L_{EN}}{L_e}\right)^{\mathbf{VFBLEXP}} + \mathbf{VFBW}\frac{W_{EN}}{W_e} + \mathbf{VFBLW}\frac{L_{EN}}{L_e}\frac{W_{EN}}{W_e}$$

$$\mathbf{VFBB} = \mathbf{VFBBO} + \mathbf{VFBLBO}\times\frac{\mathbf{TBOX}}{\mathbf{TOXE}}\times\mathbf{VFBL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{VFBLEXP}}$$

$$\mathbf{STVFB} = \mathbf{STVFBO}\left(1 + \mathbf{STVFBL}\frac{L_{EN}}{L_E}\right)\left(1 + \mathbf{STVFBW}\frac{W_{EN}}{W_E}\right)\left(1 + \mathbf{STVFBLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

© 2023 Cadence Design Systems, Inc.

Gate-to-interface coupling parameters

$$\mathbf{CICF} = \mathbf{CICFO}$$

$$\mathbf{CIC} = \mathbf{CICO}$$

$$\lambda_{2D} = \sqrt{\frac{\varepsilon_{Si}(1-\mathbf{XGE}) + \varepsilon_{Ge}\mathbf{XGE}}{\varepsilon_{ox}} \times \mathbf{TSI} \times \left(\mathbf{TOXE} + 4\,10^{-10}\right)}$$

$$\mathbf{PSCE} = 2 \times \mathbf{PSCEL}\left(\frac{\lambda_{2D}}{L_E}\right)^{\mathbf{PSCELEXP}}\left(1 + \mathbf{PSCEW}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{PSCEB} = \mathbf{PSCEBO}$$

$$\mathbf{PSCEDL} = \mathbf{PSCEDLL}\frac{L_{EN}}{L_E}\Big/\max\left(1 + \mathbf{PSCEDLW}\frac{W_{EN}}{W_E}, 10^{-3}\right)$$

$$\mathbf{PNCE} = \mathbf{PNCEW}\frac{W_{EN}}{W_E}$$

Drain Induced Barrier Lowering Parameters

$$\mathbf{CF} = \mathbf{CFL}\left(\frac{\lambda_{2D}}{L_E}\right)^{\mathbf{CFLEXP}}\left(1 + \mathbf{CFW}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{CFB} = \mathbf{CFBO}$$

$$\mathbf{STCF} = \mathbf{STCFL}\left(\frac{\lambda_{2D}}{L_E}\right)^{\mathbf{CFLEXP}}\left(1 + \mathbf{CFW}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{CFD} = \mathbf{CFDO}$$

$$\mathbf{CFDL} = \mathbf{CFDLL}\frac{L_{EN}}{L_E}\Big/\max\left(1 + \mathbf{CFDLW}\frac{W_{EN}}{W_E}, 10^{-3}\right)$$

© 2023 Cadence Design Systems, Inc.

Mobility Parameters

$$L_{P1eff} = \mathbf{LP1} \times \max\left(1 + \mathbf{LP1W}\frac{W_{EN}}{W_E}, 10^{-3}\right)$$

$$G_{PE} = \max\left(1 + \mathbf{FBET1}\left(1 + \mathbf{FBET1W}\frac{W_{EN}}{W_E}\right)\frac{1 - \exp\left(-L_E/L_{P1eff}\right)}{L_E/L_{P1eff}} + \mathbf{FBET2}\frac{1 - \exp\left(-L_E/\mathbf{LP2}\right)}{L_E/\mathbf{LP2}}, 10^{-6}\right)$$

$$G_{WE} = \max\left(1 + \mathbf{BETW1}\frac{W_{EN}}{W_E} + \mathbf{BETW2}\frac{W_{EN}}{W_E}\ln\left(1 + \frac{W_E}{\mathbf{WBET}}\right), 10^{-6}\right)$$

$$G_E = \mathbf{UO}\frac{G_{WE}}{G_{PE}}$$

© 2023 Cadence Design Systems, Inc.

Note: Unlike in UTSOI1, `UO` is integrated into `GE`. This changes the signification of the `THESAT` related global parameters, as detailed in the Velocity Saturation Parameters section.

$$\mathbf{BETN} = G_E \frac{W_E}{L_E}$$

$$\mathbf{BETNB} = \mathbf{BETNBO}$$

$$\mathbf{STBET} = \mathbf{STBETO}\left(1+\mathbf{STBETL}\frac{L_{EN}}{L_E}\right)\left(1+\mathbf{STBETW}\frac{W_{EN}}{W_E}\right)\left(1+\mathbf{STBETLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{CS} = \left(\mathbf{CSO}+\mathbf{CSL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{CSLEXP}}\right)\left(1+\mathbf{CSW}\frac{W_{EN}}{W_E}\right)\left(1+\mathbf{CSLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{STCS} = \mathbf{STCSO}$$

$$\mathbf{THECS} = \mathbf{THECSO}$$

$$\mathbf{STTHECS} = \mathbf{STTHECSO}$$

$$\mathbf{CSTHR} = \mathbf{CSTHRO}$$

$$\mathbf{MUE} = \mathbf{MUEO}$$

$$\mathbf{STMUE} = \mathbf{STMUEO}$$

$$\mathbf{THEMU} = \mathbf{THEMUO}$$

$$\mathbf{STTHEMU} = \mathbf{STTHEMUO}$$

$$\mathbf{XCOR} = \mathbf{XCORO}\left(1+\mathbf{XCORL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{XCORLEXP}}\right)\left(1+\mathbf{XCORW}\frac{W_{EN}}{W_E}\right)\left(1+\mathbf{XCORLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{STXCOR} = \mathbf{STXCORO}$$

$$\mathbf{FETA} = \mathbf{FETAO}$$

Series Resistance Parameters

$$\mathbf{RS} = \mathbf{RSW1}\frac{W_{EN}}{W_E}\left(1+\mathbf{RSW2}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{STRS} = \mathbf{STRSO}$$

$$\mathbf{RSG} = \mathbf{RSGO}$$

$$\mathbf{THERSG} = \mathbf{THERSGO}$$

© 2023 Cadence Design Systems, Inc.

Velocity Saturation Parameters

$$\mathbf{THESAT} = \left(\mathbf{THESATO} + G_E \mathbf{THESATL} \left(\frac{L_{EN}}{L_E} \right)^{\mathbf{THESATLEXP}} \right) \left(1 + \mathbf{THESATW} \frac{W_{EN}}{W_E} \right) \left(1 + \mathbf{THESATLW} \frac{L_{EN}}{L_E} \frac{W_{EN}}{W_E} \right)$$

Since `UO` has been included in `GE` (see (Mobility Parameters), `THESATL`, in UTSOI2, is closely related to the saturation velocity itself.

$$\mathbf{STTHESAT} = \mathbf{STTHESATO} \left(1 + \mathbf{STTHESATL} \frac{L_{EN}}{L_E} \right) \left(1 + \mathbf{STTHESATW} \frac{W_{EN}}{W_E} \right) \left(1 + \mathbf{STTHESATLW} \frac{L_{EN}}{L_E} \frac{W_{EN}}{W_E} \right)$$

$$\mathbf{THESATG} = \mathbf{THESATGO}$$

$$\mathbf{THESATB} = \mathbf{THESATBO}$$

Saturation and Channel Length Modulation Parameters

$$\mathbf{AX} = \frac{\mathbf{AXO}}{1 + \mathbf{AXL} \left(\frac{L_{EN}}{L_E} \right)^{\mathbf{AXLEXP}}}$$

$$\mathbf{ALP} = \frac{\mathbf{ALPL1} \left(\frac{L_{EN}}{L_E} \right)^{\mathbf{ALPLEXP}}}{1 + \mathbf{ALPL2} \left(\frac{L_{EN}}{L_E} \right)^{\mathbf{ALPLEXP}+1}} \left(1 + \mathbf{ALPW} \frac{W_{EN}}{W_E} \right)$$

$$\mathbf{ALP1} = \frac{\mathbf{ALP1L1} \left(\frac{L_{EN}}{L_E} \right)^{\mathbf{ALP1LEXP}}}{1 + \mathbf{ALP1L2} \left(\frac{L_{EN}}{L_E} \right)^{\mathbf{ALP1LEXP}+1}} \left(1 + \mathbf{ALP1W} \frac{W_{EN}}{W_E} \right)$$

$$\mathbf{VP} = \mathbf{VPO}$$

© 2023 Cadence Design Systems, Inc.

Gate Current Parameters

$$\mathrm{GCO} = \mathrm{GCOO}$$

$$\mathrm{IGINV} = \mathrm{IGINVLW}\frac{L_E}{L_{EN}}\frac{W_E}{W_{EN}}$$

$$\mathrm{IGOVINV} = \mathrm{IGOVINVW}\frac{W_E}{W_{EN}}$$

$$\mathrm{IGOVINVD} = \mathrm{IGOVINVDW}\frac{W_E}{W_{EN}}$$

$$\mathrm{IGOVACC} = \mathrm{IGOVACCW}\frac{W_E}{W_{EN}}$$

$$\mathrm{IGOVACCD} = \mathrm{IGOVACCDW}\frac{W_E}{W_{EN}}$$

Unlike in UTSOI1, gate currents in overlap regions are not linked with `LOVO` in UTSOI2.

$$\mathrm{STIG} = \mathrm{STIGO}$$

$$\mathrm{GC2CH} = \mathrm{GC2CHO}$$

$$\mathrm{GC3CH} = \mathrm{GC3CHO}$$

$$\mathrm{GC2OVINV} = \mathrm{GC2OVINVO}$$

$$\mathrm{GC3OVINV} = \mathrm{GC3OVINVO}$$

$$\mathrm{GC2OVACC} = \mathrm{GC2OVACCO}$$

$$\mathrm{GC3OVACC} = \mathrm{GC3OVACCO}$$

$$\mathrm{CHIB} = \mathrm{CHIBO}$$

$$\mathrm{NIGINV} = \mathrm{NIGINVO}$$

Gate Induced Drain/Source Leakage (GIDL/GISL) Parameters

$$\mathrm{AGIDL} = \mathrm{AGIDLW}\frac{W_E}{W_{EN}}$$

$$\mathrm{AGIDLD} = \mathrm{AGIDLDW}\frac{W_E}{W_{EN}}$$

© 2023 Cadence Design Systems, Inc.

For gate currents, GIDL/GISL currents are not linked with `LOVO` in UTSOI2, as compared to UTSOI1.

$$\mathbf{BGIDL} = \mathbf{BGIDLO}$$

$$\mathbf{BGIDLD} = \mathbf{BGIDLDO}$$

$$\mathbf{STBGIDL} = \mathbf{STBGIDLO}$$

$$\mathbf{STBGIDLD} = \mathbf{STBGIDLDO}$$

$$\mathbf{CGIDL} = \mathbf{CGIDLO}$$

$$\mathbf{CGIDLD} = \mathbf{CGIDLDO}$$

Charge Model Parameters

$$\mathbf{AREAQ} = L_{E,CV} W_{E,CV}$$

$$\mathbf{CGBOV} = \mathbf{CGBOVL} \frac{L_{G,CV}}{L_{EN}}$$

$$\mathbf{COV} = \varepsilon_{ox} \frac{W_{E,CV}}{\mathbf{TOXE}} \mathbf{LOVO}$$

$$\mathbf{COVD} = \varepsilon_{ox} \frac{W_{E,CV}}{\mathbf{TOXE}} \mathbf{LOVDO}$$

$$\mathbf{COVDL} = \mathbf{COVDLO} \Big/ \max\left(1 + \mathbf{COVDLW} \frac{W_{EN}}{W_{E,CV}}, 10^{-3}\right)$$

$$\mathbf{DVFBOV} = \mathbf{DVFBOVO}$$

$$\mathbf{CFR} = \mathbf{CFRO} + \mathbf{CFRW} \frac{W_{G,CV}}{W_{EN}}$$

$$\mathbf{CFRD} = \mathbf{CFRDO} + \mathbf{CFRDW} \frac{W_{G,CV}}{W_{EN}}$$

$$\mathbf{CSD} = \mathbf{CSDO}\left(\varepsilon_{Si}(1 - \mathbf{XGE}) + \varepsilon_{Ge}\mathbf{XGE}\right)\mathbf{TSI} \frac{W_E}{L_E}$$

$$\mathbf{CSDBP} = \mathbf{CSDBPO}$$

© 2023 Cadence Design Systems, Inc.

Self-heating Parameters

$$\mathbf{RTH} = \frac{\mathbf{RTHO}}{1 + \mathbf{RTHL}\frac{L_{G,TH}}{L_{EN}} + \mathbf{RTHW}\frac{W_{G,TH}}{W_{EN}} + \mathbf{RTHLW}\frac{L_{G,TH}}{L_{EN}}\frac{W_{G,TH}}{W_{EN}}}$$

$$\mathbf{STRTH} = \mathbf{STRTHO}$$

$$\mathbf{CTH} = \mathbf{CTHO}\left(1 + \mathbf{RTHL}\frac{L_{G,TH}}{L_{EN}} + \mathbf{RTHW}\frac{W_{G,TH}}{W_{EN}} + \mathbf{RTHLW}\frac{L_{G,TH}}{L_{EN}}\frac{W_{G,TH}}{W_{EN}}\right)$$

Noise Model Parameters

$$\mathbf{FNT} = \mathbf{FNTO}$$

$$\mathbf{NFA} = \mathbf{NFALW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}$$

$$\mathbf{NFB} = \mathbf{NFBLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}$$

$$\mathbf{NFC} = \mathbf{NFCLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}$$

$$\mathbf{EF} = \mathbf{EFO}$$

$$\mathbf{NFE} = \mathbf{NFEO}$$

$$\mathbf{NFEB} = \mathbf{NFEBO}$$

© 2023 Cadence Design Systems, Inc.

Stress Model

Effective SA/SB-related Parameters

$$R_A = \frac{1}{\mathbf{NF}} \sum_{i=0}^{\mathbf{NF}-1} \frac{1}{\mathbf{SA} + L/2 + i(\mathbf{SD} + L)}$$

$$R_B = \frac{1}{\mathbf{NF}} \sum_{i=0}^{\mathbf{NF}-1} \frac{1}{\mathbf{SB} + L/2 + i(\mathbf{SD} + L)}$$

$$R_{A,ref} = \frac{1}{\mathbf{SAREF} + L/2}$$

$$R_{B,ref} = \frac{1}{\mathbf{SBREF} + L/2}$$

Modification of Mobility-related Parameters

$$K_{u0} = \left(1 + \frac{\mathbf{LKUO}}{(L + \Delta L_{PS})^{\mathbf{LLODKUO}}} + \frac{\mathbf{WKUO}}{(W_f + \Delta W_{OD} + \mathbf{WLOD})^{\mathbf{WLODKUO}}} + \frac{\mathbf{PKUO}}{(L + \Delta L_{PS})^{\mathbf{LLODKUO}} (W_f + \Delta W_{OD} + \mathbf{WLOD})^{\mathbf{WLODKUO}}} \right) \left(1 + \mathbf{TKUO} \left(\frac{T_{KD}}{T_{KR}} - 1 \right) \right)$$

$$\rho_\beta = \frac{\mathbf{KUO}}{K_{u0}} (R_A + R_B)$$

$$\rho_{\beta,ref} = \frac{\mathbf{KUO}}{K_{u0}} (R_{A,ref} + R_{B,ref})$$

$$\mathbf{BETN} = \frac{1 + \rho_\beta}{1 + \rho_{\beta,ref}} \mathbf{BETN}_{ref}$$

$$\mathbf{THESAT} = \frac{1 + \rho_\beta}{1 + \rho_{\beta,ref}} \frac{1 + \mathbf{KVSAT}\rho_{\beta,ref}}{1 + \mathbf{KVSAT}\rho_\beta} \mathbf{THESAT}_{ref}$$

© 2023 Cadence Design Systems, Inc.

Modification of Threshold Voltage-related Parameters

$$K_{vth0} = 1 + \frac{\mathbf{LKVTHO}}{\left(L + \Delta L_{PS}\right)^{\mathbf{LLODVTH}}} + \frac{\mathbf{WKVTHO}}{\left(W_f + \Delta W_{OD} + \mathbf{WLOD}\right)^{\mathbf{WLODVTH}}} + \frac{\mathbf{PKVTHO}}{\left(L + \Delta L_{PS}\right)^{\mathbf{LLODVTH}} \left(W_f + \Delta W_{OD} + \mathbf{WLOD}\right)^{\mathbf{WLODVTH}}}$$

$$\Delta R = R_A + R_B - R_{A,ref} - R_{B,ref}$$

$$\mathbf{VFB} = \mathbf{VFB}_{ref} + \frac{\mathbf{KVTHO}}{K_{vth0}} \Delta R$$

$$\mathbf{VFBB} = \mathbf{VFBB}_{ref} + \frac{\mathbf{KVTHO}}{K_{vth0}} \Delta R$$

$$\mathbf{CF} = \mathbf{CF}_{ref} + \frac{\mathbf{STETAO}}{K_{vth0}^{\mathbf{LODETAO}}} \Delta R$$

Asymmetric Junctions

After the calculations described Scaling Equations and Stress Model, local parameters are clipped according to the min/max values of the parameters.

Then, if the switch parameter SWJUNASYM is equal to 0, drain and source junctions are assumed symmetrical and all parameters related to the drain junction are overwritten by their source side counterparts.

If `SWJUNASYM=0`:

$$\mathbf{NOVD} = \mathbf{NOV}$$

$$\mathbf{IGOVINVD} = \mathbf{IGOVINV}$$

$$\mathbf{IGOVACCD} = \mathbf{IGOVACC}$$

$$\mathbf{AGIDLD} = \mathbf{AGIDL}$$

$$\mathbf{BGIDLD} = \mathbf{BGIDL}$$

$$\mathbf{STBGIDLD} = \mathbf{STBGIDL}$$

$$\mathbf{CGIDLD} = \mathbf{CGIDL}$$

$$\mathbf{COVD} = \mathbf{COV}$$

$$\mathbf{CFRD} = \mathbf{CFR}$$

© 2023 Cadence Design Systems, Inc.

If `SWJUNASYM = 1`, the parameters related to the drain side are kept unchanged.

Note: If some of the drain side parameters are not specified in the model card, they take their default value and not the value of their source side counterpart.

Model Equations

Internal Parameters Including Temperature Dependencies

Transistor Temperature

$$T_{KR} = 273.15 + \mathbf{TR}$$

$$T_{KD} = 273.15 + T_{Ambient}$$

As in UTSOI1, a temperature node is used to compute the elevation of the channel temperature with respect to the circuit temperature due to self-heating when the `SWSHE` flag is set to 1 (see paragraph 4.9 for details). This temperature elevation is given by DTC. The channel temperature TKC is given by:

$$\begin{cases} T_{KC} = T_{KD} + \Delta T_C & if\ \mathbf{SWSHE} = 1 \\ T_{KC} = T_{KD} & else \end{cases}$$

$$\Delta T = T_{KC} - T_{KR}$$

$$\phi_{T0} = \frac{k_B T_{KC}}{q}$$

© 2023 Cadence Design Systems, Inc.

Local Process Parameters

$$\varepsilon_{ch} = \varepsilon_{Si}(1-\mathbf{XGE}) + \varepsilon_{Ge}\mathbf{XGE}$$

$$E_{g,Si} = E_{g0,Si} - \frac{\alpha_{Si} T_{KC}^{\ 2}}{\beta_{Si} + T_{KC}}$$

$$E_{g,Ge} = E_{g0,Ge} - \frac{\alpha_{Ge} T_{KC}^{\ 2}}{\beta_{Ge} + T_{KC}}$$

$$\delta E_g = \left(E_{g,Ge} - E_{g,Si} + C_G(1-\mathbf{XGE})\right)\mathbf{XGE}$$

$$E_g = E_{g,Si} + \delta E_g$$

$$n_{eff} = \frac{n_{i,fact,300}}{1+\sqrt{10\mathbf{XGE}}}\left(\frac{T_{KC}}{300}\right)^{3/2} \exp\left(-\frac{E_g}{2\phi_{T0}}\right)$$

$$\delta V_{FB,ch} = 0.05\mathbf{XGE} - \delta E_g/2$$

© 2023 Cadence Design Systems, Inc.

Interface Coupling Internal Parameters

$$\begin{cases} C_{ox1}' = \dfrac{\varepsilon_{ox}}{\mathbf{TOXE}} & \text{if } \mathbf{PNCE} \le 0 \\ C_{ox1}' = \dfrac{\varepsilon_{ox}}{\mathbf{TOXE}}(1+\mathbf{PNCE}) & \text{else} \end{cases}$$

$$\begin{cases} C_{ox2}' = \dfrac{\varepsilon_{ox}}{\mathbf{TBOX}}(1-\mathbf{PNCE}) & \text{if } \mathbf{PNCE} \le 0 \\ C_{ox2}' = \dfrac{\varepsilon_{ox}}{\mathbf{TBOX}} & \text{else} \end{cases}$$

$$C_{Si0}' = \frac{\varepsilon_{ch}}{\mathbf{TSI}}$$

$$\phi_T = \phi_{T0}\left(1+\mathbf{CT}\frac{T_{KR}}{T_{KC}}\right)$$

$$r_{cap10} = \frac{C_{ox1}'}{C_{Si0}'}$$

$$r_{cap20} = \frac{C_{ox2}'}{C_{Si0}'}$$

$$PSCE_1 = \mathbf{PSCE}$$

$$PSCE_2 = \mathbf{PSCEB} \times \mathbf{PSCE} \times \mathbf{TBOX}/\mathbf{TOXE}$$

$$C_{eq0} = \frac{C_{Si0}'}{1 + 1/(1+PSCE_1)/r_{cap10} + 1/(1+PSCE_2)/r_{cap20}}$$

$$f_{A0} = \frac{2qn_{eff}\varepsilon_{ch}}{\phi_T}$$

Drain Induced Barrier Lowering Internal Parameters

$$CF_1 = \mathbf{CF} + \mathbf{STCF} \times \Delta T$$

$$CF_2 = \mathbf{CF} \times \mathbf{CFB} \times \frac{\mathbf{TBOX}}{\mathbf{TOXE}} + \mathbf{STCF} \times \Delta T$$

$$x_{d0} = \frac{\mathbf{CFD}}{\phi_T}$$

© 2023 Cadence Design Systems, Inc.

Backplane Internal Parameters

Since the backplane is located under the buried oxide of the device, it is assumed that its temperature is that of the environment. Therefore, the self-heating effect is not included for the corresponding parameters and temperature. TKD is considered.

$$n_{eff,sub} = n_{i,fact,300}\left(\frac{T_{KD}}{300}\right)^{3/2}\exp\left(-\frac{E_{g,Si}}{2(k_B T_{KD}/q)}\right)$$

$$NSUB_{eff} = \mathbf{NSUB}\left(1 + PSCE_2\right)$$

$$G_{f,sub} = \frac{\sqrt{2q\varepsilon_{Si}NSUB_{eff}}}{C_{eq0}\sqrt{k_B T_{KD}/q}}$$

$$\xi_{sub} = 1 + \frac{G_{f,sub}}{\sqrt{2}}$$

$$\xi_{mrg,sub} = 10^{-5}\xi_{sub}$$

$$x_{b,sub} = \ln\left(\frac{NSUB_{eff}}{n_{eff,sub}}\right)$$

$$x_{n,sub} = 2x_{b,sub}$$

$$\begin{cases} type_{sub} = 1 & if\ \mathbf{NSUB} \geq 0 \\ type_{sub} = -1 & else \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Quantum Mechanical Correction Internal Parameters

$$\begin{cases} \delta V_{FB,qm} = 0 & \text{if } \mathbf{QMC} = 0 \\ \delta V_{FB,qm} = \dfrac{0.409618895}{10^{18}\,\mathbf{TSI}^2} & \text{if } \mathbf{QMC} > 0 \text{ and } \mathbf{TYPE} = +1 \ (NMOS) \\ \delta V_{FB,qm} = \dfrac{0.723134895}{10^{18}\,\mathbf{TSI}^2} & \text{if } \mathbf{QMC} > 0 \text{ and } \mathbf{TYPE} = -1 \ (PMOS) \end{cases}$$

$$\begin{cases} qq = 0 & \text{if } \mathbf{QMC} = 0 \\ qq = \dfrac{0.4QM_N\mathbf{QMC}}{\left(10^{18}\,\mathbf{TSI}^2\phi_T\right)^{1/3}} & \text{if } \mathbf{QMC} > 0 \text{ and } \mathbf{TYPE} = +1 \ (NMOS) \\ qq = \dfrac{0.4QM_p\mathbf{QMC}}{\left(10^{18}\,\mathbf{TSI}^2\phi_T\right)^{1/3}} & \text{if } \mathbf{QMC} > 0 \text{ and } \mathbf{TYPE} = -1 \ (PMOS) \end{cases}$$

$$V_{FB1} = \mathbf{TYPE}\left(\mathbf{VFB} + \mathbf{STVFB} \times \Delta T + \delta V_{FB,ch}\right) + \delta V_{FB,qm} + \mathbf{DELVTO}$$

$$\begin{cases} V_{FB2} = \mathbf{TYPE}\left(\mathbf{VFBB} + \mathbf{STVFB} \times \Delta T + \delta V_{FB,ch}\right) + \delta V_{FB,qm} & \text{if } \mathbf{SWSUBDEP} = 0 \\ V_{FB2} = \mathbf{TYPE}\left(\mathbf{VFBB} + \mathbf{STVFB} \times \Delta T + \delta V_{FB,ch} + type_{sub} x_{b,sub}\left(k_B T_{KD}/q\right)\right) + \delta V_{FB,qm} & else \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Mobility Internal Parameters

$$\beta_{N1} = \mathbf{FACTUO} \times \mathbf{BETN} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STBET}}$$

$$\beta_{N2} = \mathbf{FACTUO} \times \mathbf{BETN} \times \mathbf{BETNB} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STBET}}$$

$$\mu_E = \mathbf{MUE} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STMUE}}$$

$$\theta_\mu = \mathbf{THEMU} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STTHEMU}}$$

$$C_S = \mathbf{CS} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STCS}}$$

$$\theta_{CS} = \mathbf{THECS} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STTHECS}}$$

$$X_{cor} = \mathbf{XCOR} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STXCOR}}$$

$$f_{\mu E} = 10^{-8} \frac{\phi_T}{\mathbf{TSI}} \mu_E$$

$$q_{ith,CS} = 0.5 \times \mathbf{CSTHR}$$

$$\begin{cases} \eta_\mu = 1/2 \times \mathbf{FETA} & \text{if } \mathbf{TYPE} = +1 \ (NMOS) \\ \eta_\mu = 1/3 \times \mathbf{FETA} & \text{if } \mathbf{TYPE} = -1 \ (PMOS) \end{cases}$$

Series Resistance Internal Parameters

$$R_S = \mathbf{RS} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STRS}}$$

$$f_{RS} = 2\phi_T R_S$$

© 2023 Cadence Design Systems, Inc.

Velocity Saturation Internal Parameters

$$\theta_{sat} = \mathbf{FACTUO} \times \mathbf{THESAT} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STTHESAT}+\mathbf{STBET}}$$

Note the presence of the `FACTUO` pre-factor and of `STBET` in the temperature exponent. This contributes to decouple velocity saturation parameters from low longitudinal field mobility ones, and makes in particular `STTHESAT` the temperature exponent of the saturation velocity itself.

$$f_{vsat} = \phi_T \theta_{sat}$$

Channel Length Modulation Internal Parameters

$$f_{alp1} = \frac{\mathbf{ALP1}}{\phi_T}$$

$$f_{vp} = \frac{\phi_T}{\mathbf{VP}}$$

© 2023 Cadence Design Systems, Inc.

Gate Current Internal Parameters

$$I_{G,inv} = \mathbf{IGINV} \times \left(\frac{T_{KC}}{T_{KR}} \right)^{\mathbf{STIG}}$$

$$I_{G,ovinv} = \mathbf{IGOVINV} \times \left(\frac{T_{KC}}{T_{KR}} \right)^{\mathbf{STIG}}$$

$$I_{G,ovinvD} = \mathbf{IGOVINVD} \times \left(\frac{T_{KC}}{T_{KR}} \right)^{\mathbf{STIG}}$$

$$I_{G,ovacc} = \mathbf{IGOVACC} \times \left(\frac{T_{KC}}{T_{KR}} \right)^{\mathbf{STIG}}$$

$$I_{G,ovaccD} = \mathbf{IGOVACCD} \times \left(\frac{T_{KC}}{T_{KR}} \right)^{\mathbf{STIG}}$$

$$B_{ch} = \frac{4}{3} \frac{\sqrt{2qm_0\mathbf{CHIB}}}{\hbar} \mathbf{TOXP}$$

$$B_{ov} = \frac{4}{3} \frac{\sqrt{2qm_0\mathbf{CHIB}}}{\hbar} \mathbf{TOXP}$$

© 2023 Cadence Design Systems, Inc.

Note: Contrary to UTSOI1, B_{ch} and B_{ov} are equal in UTSOI2, since the parameter TOXOV has been removed.

$$\begin{cases} G_{CQ,ch} = 0 & \text{if } \mathbf{GC3CH} \geq 0 \\ G_{CQ,ch} = -0.495\,\mathbf{GC2CH}/\mathbf{GC3CH} & \text{else} \end{cases}$$

$$\begin{cases} G_{CQ,ovinv} = 0 & \text{if } \mathbf{GC3OVINV} \geq 0 \\ G_{CQ,ovinv} = -0.495\,\mathbf{GC2OVINV}/\mathbf{GC3OVINV} & \text{else} \end{cases}$$

$$\begin{cases} G_{CQ,ovacc} = 0 & \text{if } \mathbf{GC3OVACC} \geq 0 \\ G_{CQ,ovacc} = -0.495\,\mathbf{GC2OVACC}/\mathbf{GC3OVACC} & \text{else} \end{cases}$$

$$\alpha_b = \frac{E_g}{2}$$

$$D_{ch} = \phi_T \mathbf{GCO}$$

$$D_{ov} = \phi_{T0} \mathbf{GCO}$$

$$n_{iginv} = \frac{1}{1 + \mathbf{NIGINV} \times E_g/(2\phi_T)}$$

Gate Induced Drain/Source Leakage (GIDL/GISL) Internal Parameters

$$A_{GIDL} = \frac{4.10^{-18}}{\mathbf{TOXP}^2}\mathbf{AGIDL}$$

$$A_{GIDLD} = \frac{4.10^{-18}}{\mathbf{TOXP}^2}\mathbf{AGIDLD}$$

$$B_{GIDL} = 5.10^8\,\mathbf{TOXP}(1+\mathbf{STBGIDL}\times\Delta T)\mathbf{BGIDL}$$

$$B_{GIDLD} = 5.10^8\,\mathbf{TOXP}(1+\mathbf{STBGIDLD}\times\Delta T)\mathbf{BGIDLD}$$

Charge Model Internal Parameters

$$f_{area} = \phi_T \mathbf{AREAQ}$$

© 2023 Cadence Design Systems, Inc.

Self-heating Internal Parameters

$$R_{th} = \mathbf{RTH} \times \left(\frac{T_{KR}}{T_{KC}} \right)^{\mathbf{STRTH}}$$

Noise Model Internal Parameters

$$n_T = 4 k_B T_{KC} \mathbf{FNT}$$

Terminal Voltage Conditioning

The input voltages used in the model are V_{GS}, V_{DS}, and V_{SB} in nMOSFET and positive VDS configuration (that is, sign of external voltages is reversed for pMOSFET, and source/drain are interchanged in case of negative V_{DS}), from which V_{SD}, V_{GD}, V_{DB}, and V_{GB} are computed. Then, dimensionless quantities are defined from these voltages.

© 2023 Cadence Design Systems, Inc.

Voltages for Channel Current and Intrinsic Charge Models

$$x_d = \frac{V_{DS}}{\phi_T}$$

$$x_{dsx} = \frac{\sqrt{V_{DS}^{\ 2} + 0.01} - 0.1}{\phi_T}$$

$$x_{g10} = \frac{V_{GS} - V_{FB1}}{\phi_T} - \frac{x_d - x_{dsx}}{2}$$

$$x_{g20} = \frac{-V_{SB} - V_{FB2}}{\phi_T} - \frac{x_d - x_{dsx}}{2}$$

$$\delta l_{eff} = -2 \times \text{MIN_FUNC}\left(\frac{r_{cap10} x_{g10} + r_{cap20} x_{g20}}{\left(r_{cap10} + r_{cap20}\right) E_g / \left(2\phi_T\right)}, 0, 0.3 \right)$$

$$c_{sce1} = \frac{1}{1 + PSCE_1 / \left(1 + \mathbf{PSCEDL} \times \delta l_{eff}\right)}$$

$$c_{sce2} = \frac{1}{1 + PSCE_2 / \left(1 + \mathbf{PSCEDL} \times \delta l_{eff}\right)}$$

$$\delta x_{g1,DIBL} = 2CF_1 x_{d0} \left(\sqrt{1 + x_{dsx}/x_{d0}} - 1\right)\left(1 + \mathbf{CFDL} \times \delta l_{eff}\right)$$

$$\delta x_{g2,DIBL} = 2CF_2 x_{d0} \left(\sqrt{1 + x_{dsx}/x_{d0}} - 1\right)\left(1 + \mathbf{CFDL} \times \delta l_{eff}\right)$$

$$x_{g1} = \left(x_{g10} - \frac{E_g}{2\phi_T} + \delta x_{g1,DIBL} \right) c_{sce1} + \frac{E_g}{2\phi_{T0}} + \frac{x_d - x_{dsx}}{2}$$

$$x_{g2} = \left(x_{g20} - \frac{E_g}{2\phi_T} + \delta x_{g2,DIBL} \right) c_{sce2} + \frac{E_g}{2\phi_{T0}} + \frac{x_d - x_{dsx}}{2}$$

$$x_{g1x} = \text{MIN_FUNC}\left(x_{g2} + \mathbf{CICF}\left(x_{g1} - x_{g2}\right), 600, 0.01\right)$$

$$x_{g2x} = \text{MIN_FUNC}\left(x_{g1} + \mathbf{CIC}\left(x_{g2} - x_{g1}\right), 600, 0.01\right)$$

© 2023 Cadence Design Systems, Inc.

Voltages for Overlap Currents and Charges

$$x_{gs,ov} = -\frac{V_{GS}}{\phi_{T0}}$$

$$x_{gd,ov} = -\frac{V_{GD}}{\phi_{T0}}$$

$$x_{gs,ovcv} = -\frac{V_{GS} - \mathbf{DVFBOV} - E_g/2}{\phi_{T0}}$$

$$x_{gd,ovcv} = -\frac{V_{GD} - \mathbf{DVFBOV} - E_g/2}{\phi_{T0}}$$

Backplane Depletion

Depletion of the backplane is accounted for through the calculation of an effective backplane bias x_{g2eff}. If backplane depletion is not activated (that is, `SWSUBDEP=0`), then x_{g2eff} is given by:

$$x_{g2eff} = x_{g2x}$$

If backplane depletion is activated (that is, `SWSUBDEP=1`), then the computation of x_{g2eff} uses a PSP-like surface potential calculation sequence. This computation is based on the following analogy: the backplane is considered as the channel of a bulk MOSFET, where gate electrode is the front gate and where gate oxide capacitance is equal to the front gate oxide

© 2023 Cadence Design Systems, Inc.

capacitance in series with the channel film capacitance and the buried oxide capacitance. The detailed calculation of x_{g2eff} is:

$$x_{g1int} = \mathbf{TYPE} \times type_{sub} \times x_{g1x}$$

$$x_{g2int} = \mathbf{TYPE} \times type_{sub} \times x_{g2x}$$

$$x_{gbint} = x_{g1int} - x_{g2int}$$

if $|x_{gbint}| \le \xi_{mrg,sub}$:

$$\delta x_{g2,sub} = \frac{x_{gbint}}{\xi_{sub}}\left(1 + \frac{x_{gbint} G_{f,sub}\left(1-\exp\left(-x_{n,sub}\right)\right)}{6\sqrt{2}\xi_{sub}^{\ 2}}\right)$$

else if $x_{gbint} < -\xi_{mrg,sub}$:

$$y_g = -x_{gbint}$$

$$y_{sub} = 1.25 y_g / \xi_{sub}$$

$$\eta = \left(y_{sub} + 10 - \sqrt{(y_{sub}-6)^2 + 64}\right)/2$$

$$a = (y_g - \eta)^2 + G_{f,sub}^{\ 2}(\eta + 1)$$

$$c = 2(y_g - \eta) - G_{f,sub}^{\ 2}$$

$$\tau = -\eta + \ln\left(a / G_{f,sub}^{\ 2}\right)$$

$$y_0 = \sigma_3(a, c, \tau, \eta)$$

$$\Delta_0 = \exp(y_0)$$

$$\chi_0 = y_0^{\ 2}/\left(2 + y_0^{\ 2}\right)$$

$$\chi_1 = 4y_0/\left(2 + y_0^{\ 2}\right)^2$$

$$\chi_2 = \left(8 - 12y_0^{\ 2}\right)/\left(2 + y_0^{\ 2}\right)^3$$

$$p_C = 2(y_g - y_0) + G_{f,sub}^{\ 2}\left(\Delta_0 - 1 + \exp\left(-x_{n,sub}\right)\left(1 - \chi_1 - 1/\Delta_0\right)\right)$$

$$q_C = (y_g - y_0)^2 + G_{f,sub}^{\ 2}\left(y_0 - \Delta_0 + 1 + \exp\left(-x_{n,sub}\right)\left(1 + \chi_0 - 1/\Delta_0 - y_0\right)\right)$$

$$\delta x_{g2,sub} = -y_0 - \frac{2q_C}{p_C + \sqrt{p_C^{\ 2} - 2q_C\left(2 - G_{f,sub}^{\ 2}\left(\Delta_0 + \exp\left(-x_{n,sub}\right)\left(1/\Delta_0 - \chi_2\right)\right)\right)}}$$

© 2023 Cadence Design Systems, Inc.

else

$$x_{g1} = 1.25 + 0.7324648775 G_{f,sub}$$

$$\frac{1}{\tilde{x}_{g1}} = \frac{1.25 \xi_{sub} / x_{g1} - 1}{x_{g1}}$$

$$\overline{x} = \frac{x_{gbint}}{\xi_{sub}} \left(1 + \frac{x_{gbint}}{\tilde{x}_{g1}} \right)$$

$$w = 1 - \exp(-\overline{x})$$

$$x_1 = x_{gbint} + G_{f,sub}{}^2 / 2 - G_{f,sub} \sqrt{x_{gbint} + G_{f,sub}{}^2 / 4 - w}$$

$$b_x = x_{n,sub} + 3$$

$$\eta = \text{MIN_FUNC}(x_1, b_x, 5) - \left(b_x - \sqrt{b_x{}^2 + 5} \right) / 2$$

$$\chi_0 = \eta^2 / (2 + \eta^2)$$

$$\chi_1 = 4\eta / (2 + \eta^2)^2$$

$$\chi_2 = (8 - 12\eta^2) / (2 + \eta^2)^3$$

$$a = (x_{gbint} - \eta)^2 - G_{f,sub}{}^2 (\exp(-\eta) + \eta - 1 - \exp(-x_{n,sub})(\eta + 1 + \chi_0))$$

$$b = 1 - G_{f,sub}{}^2 (\exp(-\eta) - \chi_2 \exp(-x_{n,sub}))/2$$

$$c = 2(x_{gbint} - \eta) + G_{f,sub}{}^2 (1 - \exp(-\eta) - \exp(-x_{n,sub})(1 + \chi_1))$$

$$\tau = x_{n,sub} - \eta + \ln(a / G_{f,sub}{}^2)$$

$$x_0 = \sigma_2(a, b, c, \tau, \eta)$$

$$\Delta_0 = \exp(x_0)$$

$$\chi_0' = x_0{}^2 / (2 + x_0{}^2)$$

$$\chi_1' = 4x_0 / (2 + x_0{}^2)^2$$

$$\chi_2' = (8 - 12x_0{}^2) / (2 + x_0{}^2)^3$$

$$p_C = 2(x_{gbint} - x_0) + G_{f,sub}{}^2 (1 - 1/\Delta_0 + \exp(-x_{n,sub})(\Delta_0 - 1 - \chi_1'))$$

$$q_C = (x_{gbint} - x_0)^2 - G_{f,sub}{}^2 (x_0 - 1 + 1/\Delta_0 + \exp(-x_{n,sub})(\Delta_0 - 1 - \chi_0' - x_0))$$

$$\delta x_{g2,sub} = x_0 + \frac{2q_C}{p_C + \sqrt{p_C{}^2 - 2q_C (2 - G_{f,sub}{}^2 (1/\Delta_0 + \exp(-x_{n,sub})(\Delta_0 - \chi_2')))}}$$

© 2023 Cadence Design Systems, Inc.

Finally:

$$x_{g2eff} = \mathbf{TYPE} \times type_{sub} \times \left(x_{g2\text{int}} + \delta x_{g2,sub} \right)$$

Channel Current

Since the calculation of the MOSFET channel current is completely symmetrical between front and back interfaces, it is valid not only for Ultra-Thin Body and Buried oxide FDSOI transistors, but also for Independent Double Gate MOSFETs.

Quantum Mechanical Correction in Subthreshold Regime

To account properly for quantum confinement when the effect is activated (`QMC>0`), the effective geometry of the device is modified. In the first correction detailed here, it is assumed that there is no charge in the channel. Therefore, this correction is valid only in the subthreshold regime. A second correction will be brought afterwards to account properly for quantum confinement also in the strong inversion regime.

$$k_{10} = r_{cap10} / c_{sce1}$$
$$k_{20} = r_{cap20} / c_{sce2}$$
$$k_{eq0} = \frac{1}{1 + 1/k_{10} + 1/k_{20}}$$

© 2023 Cadence Design Systems, Inc.

If QMC>0

$$e_1 = \mathrm{MAX_FUNC}\left(k_{eq0}\left(x_{g1x} - x_{g2eff}\right), 15, 225\right)$$
$$e_2 = \mathrm{MAX_FUNC}\left(-k_{eq0}\left(x_{g1x} - x_{g2eff}\right), 15, 225\right)$$
$$C_{Si}' = \frac{C_{Si0}'}{1 - qq\left(e_1^{-1/3} + e_2^{-1/3}\right)}$$
$$k_1 = k_{10}\frac{1 - qq\left(e_1^{-1/3} + e_2^{-1/3}\right)}{1 + k_{10}e_1^{-1/3}qq}$$
$$k_2 = k_{20}\frac{1 - qq\left(e_1^{-1/3} + e_2^{-1/3}\right)}{1 + k_{20}e_2^{-1/3}qq}$$
$$k_{eq} = \frac{1}{1 + 1/k_1 + 1/k_2}$$
$$t_{ox1fact} = 1 + k_1 e_1^{-1/3} qq$$
$$t_{ox2fact} = 1 + k_2 e_2^{-1/3} qq$$

else:

$$C_{Si}' = C_{Si0}'$$
$$k_1 = k_{10}$$
$$k_2 = k_{20}$$
$$k_{eq} = k_{eq0}$$
$$t_{ox1fact} = 1$$
$$t_{ox2fact} = 1$$

© 2023 Cadence Design Systems, Inc.

Interface Coupling in Subthreshold Regime

$$A_0 = \frac{f_{A0}}{C_{Si}'^2}$$

$$\delta x_{th} = \ln\left(\frac{1+k_1}{1+k_2}\right)$$

$$diff_{\min} = 2\delta x_{th}\frac{\exp(\delta x_{th})+1}{\exp(\delta x_{th})-1}$$

$$\delta x_{WI} = k_{eq}\left(x_{g1x} - x_{g2eff}\right)$$

$$x_{1,WI0} = x_{g1x} - \delta x_{WI}/k_1$$

$$x_{2,WI0} = x_{g2eff} + \delta x_{WI}/k_2$$

Inversion Charge and Related Quantities on Source Side

First, the gate charge density at the source side q1S, normalized to $k_1 C_{Si}'\phi_T$, is computed by a call to the `CHARGE_DENSITY` function.

$$q_{1S} = \text{CHARGE_DENSITY}\left(x_{g1x}, x_{g2eff}, 0\right)$$

Then, inversion and back gate charge densities, normalized to $C_{Si}'\phi_T$ and $k_2 C_{Si}'\phi_T$ respectively, are calculated:

$$A_{e1S} = A_0 \exp\left(x_{g1x} - q_{1S}\right)$$

$$f_{qsqS} = k_1^2 q_{1S}^2 - A_{e1S}$$

If $f_{qsqS} < -0.005$:

$$f_{qctS} = \sqrt{\left|f_{qsqS}\right|}\cot\left(\sqrt{\left|f_{qsqS}\right|}/2\right)$$

$$f_{shS} = -\frac{f_{qsqS}}{\sin\left(\sqrt{\left|f_{qsqS}\right|}/2\right)^2}$$

$$f_{lnS} = \ln\left(f_{shS}\right)$$

© 2023 Cadence Design Systems, Inc.

else if $f_{qsqS} > 0.005$:

$$\zeta_S = \exp\left(-\sqrt{|f_{qsqS}|}\right)$$
$$f_{qctS} = \sqrt{|f_{qsqS}|}\frac{1+\zeta_S}{1-\zeta_S}$$
$$f_{shS} = \frac{4f_{qsqS}}{1-\zeta_S(2-\zeta_S)}\zeta_S$$
$$f_{lnS} = \ln\left(\frac{4f_{qsqS}}{1-\zeta_S(2-\zeta_S)}\right) - \sqrt{|f_{qsqS}|}$$

else:

$$f_{qctS} = 2 + \frac{f_{qsqS}}{6}\left(1 - \frac{f_{qsqS}}{60}\left(1 - \frac{f_{qsqS}}{42}\right)\right)$$
$$f_{shS} = 4 - \frac{f_{qsqS}}{3}\left(1 - \frac{f_{qsqS}}{20}\left(1 - \frac{5f_{qsqS}}{126}\right)\right)$$
$$f_{lnS} = \ln(f_{shS})$$

If $1.01k_1q_{1s} + f_{qctS} \le 0$:

$$q_{iS} = \frac{k_1q_{1S} - f_{qctS}}{1 - f_{shS}/A_{e1S}}$$
$$q_{2S} = \frac{q_{iS} - k_1q_{1S}}{k_2}$$

else if $A_{e1S}k_1q_{1s} < 0.9k_1{}^2q_{1S}{}^2(k_1q_{1s} + f_{qctS})$

$$q_{iS} = \frac{A_{e1S}}{k_1q_{1S} + f_{qctS}}$$
$$q_{2S} = \frac{q_{iS} - k_1q_{1S}}{k_2}$$

© 2023 Cadence Design Systems, Inc.

else:

$$q_{2S} = x_{g2eff} - x_{g1x} + q_{1S} + 2\ln\left(k_1 q_{1S} + f_{qctS}\right) - f_{lnS}$$
$$q_{iS} = k_1 q_{1S} + k_2 q_{2S}$$

Finally, some required quantities, including the drift electrostatic potential, are computed:

$A_{e2S} = A_0 \exp(x_{g2eff} - q_{2s})$

If $qiS > 10^{-6}$

$$b_{1S} = A_{e1S}/k_1$$
$$b_{2S} = A_{e2S}/k_2$$
$$a_{1S} = b_{1S} + 2k_1 q_{1S}$$
$$a_{2S} = b_{2S} + 2k_2 q_{2S}$$
$$\Sigma_S = 2q_{iS} + b_{1S} + b_{2S}$$

$$\begin{cases} Z_S = \dfrac{-4 f_{qsqS} \Sigma_S}{q_{iS}\left(a_{1S}a_{2S} + 2a_{1S}\left(q_{2S}+2\right) + 2a_{2S}\left(q_{1S}+2\right)\right)} & if \ \left|f_{qsqS}\right| > 0.00 \\ Z_S = \dfrac{A_{e1S}A_{e2S}\Sigma_S}{q_{iS}\left(a_{1S}A_{e1S} + a_{2S}A_{e2S} + a_{1S}a_{2S}q_{iS}\left(1 + \dfrac{q_{iS}}{6}\left(1 - \dfrac{f_{qsqS}}{30}\left(1 - \dfrac{f_{qsqS}}{28}\left(1 - \dfrac{f_{qsqS}}{30}\right)\right)\right)\right)\right)} & else \end{cases}$$

Finally:

$$x_{driftS} = \ln\left(q_{iS}\right)$$

© 2023 Cadence Design Systems, Inc.

Mobility Attenuation and Series Resistance at Source Side

Front and back transverse effective fields, normalized to $C_{Si}'\phi_T/\varepsilon_{ch}$.

$$e_{surf1S} = 2\ln\left(1+\exp\left(k_1 q_{1S}/2\right)\right)$$
$$e_{surf2S} = 2\ln\left(1+\exp\left(k_2 q_{2S}/2\right)\right)$$
$$e_{eff1S} = \eta_\mu e_{surf1S} + \left(1-\eta_\mu\right)\left(e_{surf2S} - k_2 q_{2S}\right)$$
$$e_{eff2S} = \eta_\mu e_{surf2S} + \left(1-\eta_\mu\right)\left(e_{surf1S} - k_1 q_{1S}\right)$$

Non-universality correction factor:

$$f_{cor} = \frac{\text{MAX_FUNC}\left(1+V_{GB}X_{cor},0,0.01\right)}{\text{MAX_FUNC}\left(1+0.2V_{GB}X_{cor},0,0.01\right)}$$

Coulomb scattering term:

$$G_{CSS} = C_S\left(1+q_{iS}/q_{ith,CS}\right)^{-\theta_{CS}}$$

Series resistance term:

$$q_{i1S} = \frac{e_{surf1S}}{e_{surf1S}+e_{surf2S}}q_{iS}$$
$$q_{i2S} = \frac{e_{surf2S}}{e_{surf1S}+e_{surf2S}}q_{iS}$$
$$\begin{cases} G_{RSS} = f_{RS}C_{Si}'q_{iS}\left(1-\mathbf{RSG}\left(q_{i1S}{}^{\mathbf{THERSG}}+q_{i2S}{}^{\mathbf{THERSG}}\right)\right) & \text{if } \mathbf{RSG}<0 \\ G_{RSS} = f_{RS}C_{Si}'q_{iS}/\left(1+\mathbf{RSG}\left(q_{i1S}{}^{\mathbf{THERSG}}+q_{i2S}{}^{\mathbf{THERSG}}\right)\right) & \text{else} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Total mobility degradation term, including high field mobility effect:

$$G_{mob1S} = 1 + \left(f_{\mu E} e_{eff1S}\right)^{\theta_\mu} + G_{CSS} + \beta_{N1} G_{RSS}$$
$$G_{mob2S} = 1 + \left(f_{\mu E} e_{eff2S}\right)^{\theta_\mu} + G_{CSS} + \beta_{N2} G_{RSS}$$
$$c_{1S} = e_{surf1S} \beta_{N1}$$
$$c_{2S} = e_{surf2S} \beta_{N2}$$
$$G_{mobS} = f_{cor} \frac{c_{1S} + c_{2S}}{c_{1S}/G_{mob1S} + c_{2S}/G_{mob2S}}$$

Drain Saturation Voltage, Including Velocity Saturation Effect

Derivative of inversion charge versus drift potential at the onset of saturation:

if $\delta x_{WI} > 0.007$:

$$s_1 = \frac{\delta x_{WI}}{1 - \exp\left(-\delta x_{WI}\right)}$$
$$s_2 = \exp\left(-\delta x_{WI}\right) s_1$$
$$\delta x_\infty = \ln\left(\frac{A_0}{2 q_{iS} s_1}\right) + x_{1,WI0}$$
$$\hat{q}_{1\infty} = \frac{-\delta x_{WI}}{k_{eq}\left(1 - s_1 - \delta x_{WI}/k_2\right)}$$
$$\hat{q}_{2\infty} = \frac{\delta x_{WI}}{k_{eq}\left(1 - s_2 - \delta x_{WI}/k_1\right)}$$
$$d_\infty = \frac{\delta x_{WI}}{\left(s_2/k_2 + 1/2\right)/\hat{q}_{2\infty} - \left(s_1/k_1 + 1/2\right)/\hat{q}_{1\infty}}$$

© 2023 Cadence Design Systems, Inc.

else if $\delta x_{WI} < -0.007$:

$$s_2 = \frac{\delta x_{WI}}{\exp(\delta x_{WI}) - 1}$$
$$s_1 = \exp(\delta x_{WI}) s_2$$
$$\delta x_{\infty} = \ln\left(\frac{A_0}{2 q_{iS} s_2}\right) + x_{2,WI0}$$
$$\hat{q}_{1\infty} = \frac{-\delta x_{WI}}{k_{eq}(1 - s_1 - \delta x_{WI}/k_2)}$$
$$\hat{q}_{2\infty} = \frac{\delta x_{WI}}{k_{eq}(1 - s_2 - \delta x_{WI}/k_1)}$$
$$d_{\infty} = \frac{\delta x_{WI}}{(s_2/k_2 + 1/2)/\hat{q}_{2\infty} - (s_1/k_1 + 1/2)/\hat{q}_{1\infty}}$$

else:

$$s_1 = 1 + \frac{\delta x_{WI}}{2} + \frac{\delta x_{WI}^2}{12}$$
$$s_2 = 1 - \frac{\delta x_{WI}}{2} + \frac{\delta x_{WI}^2}{12}$$
$$\hat{q}_{1\infty} = \frac{1}{k_{eq}(1/2 + 1/k_2 + \delta x_{WI}/12)}$$
$$\hat{q}_{2\infty} = \frac{1}{k_{eq}(1/2 + 1/k_1 - \delta x_{WI}/12)}$$
$$\delta x_{\infty} = \ln\left(\frac{A_0}{2 q_{iS}(1 - \delta x_{WI}^2/24)}\right) + \frac{x_{1,WI0} + x_{2,WI0}}{2}$$
$$d_{\infty} = \frac{-12}{4 - 3k_{eq} + 12 k_{eq}/(k_1 k_2) + (k_{eq}/k_1 - k_{eq}/k_2)\delta x_{WI} + (1/15 - k_{eq}/12)\delta x_{WI}^2}$$

© 2023 Cadence Design Systems, Inc.

Calculation of δx_{sat} and q_{iDsat}

if $q_{iS} > 10^{-6}$:

$$w_{sat1S} = \frac{100 e_{surf1S}}{100 + e_{surf1S}}$$

$$\begin{cases} sat_{fact1S} = 1/(1 - w_{sat1S}\,\mathbf{THESATG}) & \textit{if } \mathbf{THESATG} < 0 \\ sat_{fact1S} = 1 + w_{sat1S}\,\mathbf{THESATG} & \textit{else} \end{cases}$$

$$w_{sat2S} = \frac{100 e_{surf2S}}{100 + e_{surf2S}}$$

$$\begin{cases} sat_{fact2S} = 1/(1 - w_{sat2S}\,\mathbf{THESATB}) & \textit{if } \mathbf{THESATB} < 0 \\ sat_{fact2S} = 1 + w_{sat2S}\,\mathbf{THESATB} & \textit{else} \end{cases}$$

$$Z_{iS} = \frac{Z_S \Sigma_S}{a_{1S} a_{2S}} - \frac{1}{q_{iS}} \left(\frac{A_{e1S}}{a_{1S}} + \frac{A_{e2S}}{a_{2S}} \right)$$

$$d_S = \frac{Z_{iS} q_{iS}}{Z_{iS} + 1}$$

$$\delta x_i = \mathrm{MAX_FUNC}\left(\frac{q_{iS} + d_\infty \delta x_\infty}{d_\infty - d_S}, 0, 10^{-6} \right)$$

$$\gamma_{sat} = \frac{f_{vsat}}{G_{mobS}} \frac{sat_{fact1S} + sat_{fact2S}}{2}$$

$$v_S = 1 - q_{iS}/d_S$$

$$v_D = 1 + \delta x_\infty$$

$$w_D = \left((2 d_S - q_{iS})/d_\infty - 2 - \delta x_\infty \right) \delta x_i$$

$$p_S = 2/\gamma_{sat}{}^2$$

$$q_S = p_S + v_S$$

$$p_D = p_S + w_D$$

$$q_D = p_S + v_D$$

$$r_{cS} = \sqrt{q_S{}^2 + 4 p_S{}^3/27}$$

$$r_{cD} = \sqrt{q_D{}^2 + 4 p_D{}^3/27}$$

© 2023 Cadence Design Systems, Inc.

$$\delta x_{satS} = \left(\frac{r_{cS} + q_S}{2}\right)^{1/3} - \left(\frac{r_{cS} - q_S}{2}\right)^{1/3}$$

$$\delta x_{satD} = \left(\frac{r_{cD} + q_D}{2}\right)^{1/3} - \left(\frac{r_{cD} - q_D}{2}\right)^{1/3}$$

$$\delta x_{sat} = 0.47\left(\delta x_{satS} + \delta x_{satD} + \sqrt{(\delta x_{satS} - \delta x_{satD})^2 + 2(d_S - d_\infty)^4}\right)$$

$$q_{iDsatS} = q_{iS} + d_S \delta x_{sat}$$

$$q_{iDsatD} = d_\infty (\delta x_{sat} - \delta x_\infty)$$

$$q_{iDsat} = \text{MAX_FUNC}\left(q_{iDsatS}, q_{iDsatD}, 36(d_S - d_\infty)^2\right)$$

else:

$$d_S = d_\infty$$

$$\delta x_{sat} = 2 \times 0.47 \times (1 + \delta x_\infty)$$

$$q_{iDsat} = q_{iS}/2 + d_\infty (\delta x_{sat} - \delta x_\infty/2)$$

Normalized saturation and effective drain voltages:

$$x_{nDS,0} = \delta x_{sat} + \ln\left(\frac{q_{iS}}{0.5 + \ln(1 + \exp(q_{iDsat} - 0.5))}\right)$$

$$x_{nDS,1} = 4 + \ln(1 + \exp(x_{nDS,0} - 4))$$

$$x_{nDS,sat} = 600 - \ln(1 + \exp(600 - x_{nDS,1}))$$

$$x_{Deff} = \frac{x_D}{\left(1 + (x_D / x_{nDS,sat})^{AX}\right)^{1/AX}}$$

Inversion charge and Related Quantities at Drain Side

Gate charge density at drain side:

$$q_{1D} = \text{CHARGE_DENSITY}(x_{g1x}, x_{g2eff}, x_{Deff})$$

© 2023 Cadence Design Systems, Inc.

Then, inversion and back gate charge densities, normalized to $C_{Si}'\phi_T$ and $k_2C_{Si}'\phi_T$ respectively, are calculated:

$$A_{e1D} = A_0 \exp\left(x_{g1x} - q_{1D} - x_{Deff}\right)$$
$$f_{qsqD} = k_1{}^2 q_{1D}{}^2 - A_{e1D}$$

if $f_{qsqD} < -0.005$

$$f_{qctD} = \sqrt{\left|f_{qsqD}\right|}\cot\left(\sqrt{\left|f_{qsqD}\right|}/2\right)$$
$$f_{shD} = -\frac{f_{qsqD}}{\sin\left(\sqrt{\left|f_{qsqD}\right|}/2\right)^2}$$
$$f_{lnD} = \ln\left(f_{shD}\right)$$

else if $f_{qsqD} > 0.005$

$$\zeta_D = \exp\left(-\sqrt{\left|f_{qsqD}\right|}\right)$$
$$f_{qctD} = \sqrt{\left|f_{qsqD}\right|}\frac{1+\zeta_D}{1-\zeta_D}$$
$$f_{shD} = \frac{4f_{qsqD}}{1-\zeta_D\left(2-\zeta_D\right)}\zeta_D$$
$$f_{lnD} = \ln\left(\frac{4f_{qsqD}}{1-\zeta_D\left(2-\zeta_D\right)}\right) - \sqrt{\left|f_{qsqD}\right|}$$

else:

$$f_{qctD} = 2 + \frac{f_{qsqD}}{6}\left(1 - \frac{f_{qsqD}}{60}\left(1 - \frac{f_{qsqD}}{42}\right)\right)$$
$$f_{shD} = 4 - \frac{f_{qsqD}}{3}\left(1 - \frac{f_{qsqD}}{20}\left(1 - \frac{5f_{qsqD}}{126}\right)\right)$$
$$f_{lnD} = \ln\left(f_{shD}\right)$$

© 2023 Cadence Design Systems, Inc.

else if $A_{e1D}k_1q_{1D} < 0.9k_1^2q_1D^2(k_1q_{1D}+f_{qctD})$:

$$q_{iD} = \frac{A_{e1D}}{k_1 q_{1D} + f_{qctD}}$$
$$q_{2D} = \frac{q_{iD} - k_1 q_{1D}}{k_2}$$

else:

$$q_{2D} = x_{g2eff} - x_{g1x} + q_{1D} + 2\ln\left(k_1 q_{1D} + f_{qctD}\right) - f_{lnD}$$
$$q_{iD} = k_1 q_{1D} + k_2 q_{2D}$$

Finally, some required quantities, including the drift electrostatic potential, are computed:

$$A_{e2D} = A_0 \exp\left(x_{g2eff} - q_{2D} - x_{Deff}\right)$$

if $q_{iS} > 10^{-6}$:

$$b_{1D} = A_{e1D}/k_1$$
$$b_{2D} = A_{e2D}/k_2$$
$$a_{1D} = b_{1D} + 2k_1 q_{1D}$$
$$a_{2D} = b_{2D} + 2k_2 q_{2D}$$
$$\Sigma_D = 2q_{iD} + b_{1D} + b_{2D}$$

$$\begin{cases} Z_D = \dfrac{-4 f_{qsqD}\Sigma_D}{q_{iD}\left(a_{1D}a_{2D} + 2a_{1D}\left(q_{2D}+2\right) + 2a_{2D}\left(q_{1D}+2\right)\right)} & \text{if } \left|f_{qsqD}\right| > 0.005 \\ Z_D = \dfrac{A_{e1D}A_{e2D}\Sigma_D}{q_{iD}\left(a_{1D}A_{e1D} + a_{2D}A_{e2D} + a_{1D}a_{2D}q_{iD}\left(1 + \dfrac{q_{iD}}{6}\left(1 - \dfrac{f_{qsqD}}{30}\left(1 - \dfrac{f_{qsqD}}{28}\left(1 - \dfrac{f_{qsqD}}{30}\right)\right)\right)\right)\right)} & \text{else} \end{cases}$$

Finally:

$$x_{driftD} = x_{Deff} + \ln\left(q_{iD}\right)$$

© 2023 Cadence Design Systems, Inc.

Mid-Point Inversion Charge

$$q_{im} = \frac{q_{iS} + q_{iD}}{2}$$

Mobility Attenuation and Series Resistance

Front and back transverse effective fields at drain side, normalized to $C_{Si}'\phi_T/\varepsilon_{ch}$.

$$e_{surf1S} = 2\ln\left(1+\exp\left(k_1 q_{1S}/2\right)\right)$$
$$e_{surf2S} = 2\ln\left(1+\exp\left(k_2 q_{2S}/2\right)\right)$$
$$e_{eff1S} = \eta_\mu e_{surf1S} + \left(1-\eta_\mu\right)\left(e_{surf2S} - k_2 q_{2S}\right)$$
$$e_{eff2S} = \eta_\mu e_{surf2S} + \left(1-\eta_\mu\right)\left(e_{surf1S} - k_1 q_{1S}\right)$$

Non-universality correction factor:

$$f_{cor} = \frac{\mathrm{MAX_FUNC}\left(1+V_{GB}X_{cor},0,0.01\right)}{\mathrm{MAX_FUNC}\left(1+0.2V_{GB}X_{cor},0,0.01\right)}$$

Coulomb scattering term:

$$G_{CSS} = C_S\left(1+q_{iS}/q_{ith,CS}\right)^{-\theta_{CS}}$$

Series resistance term:

$$q_{i1S} = \frac{e_{surf1S}}{e_{surf1S}+e_{surf2S}}q_{iS}$$
$$q_{i2S} = \frac{e_{surf2S}}{e_{surf1S}+e_{surf2S}}q_{iS}$$
$$\begin{cases} G_{RSS} = f_{RS}C_{Si}'q_{iS}\left(1-\mathbf{RSG}\left(q_{i1S}^{\ \mathbf{THERSG}}+q_{i2S}^{\ \mathbf{THERSG}}\right)\right) & \text{if } \mathbf{RSG}<0 \\ G_{RSS} = f_{RS}C_{Si}'q_{iS}/\left(1+\mathbf{RSG}\left(q_{i1S}^{\ \mathbf{THERSG}}+q_{i2S}^{\ \mathbf{THERSG}}\right)\right) & \text{else} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Total mobility degradation term, including high field mobility effect:

$$G_{mob1S} = 1 + \left(f_{\mu E} e_{eff1S}\right)^{\theta_\mu} + G_{CSS} + \beta_{N1} G_{RS}$$
$$G_{mob2S} = 1 + \left(f_{\mu E} e_{eff2S}\right)^{\theta_\mu} + G_{CSS} + \beta_{N2} G_{RS}$$
$$c_{1S} = e_{surf1S} \beta_{N1}$$
$$c_{2S} = e_{surf2S} \beta_{N2}$$
$$G_{mobS} = f_{cor} \frac{c_{1S} + c_{2S}}{c_{1S}/G_{mob1S} + c_{2S}/G_{mob2S}}$$

Drain Saturation Voltage, Including Velocity Saturation Effect

Derivative of inversion charge versus drift potential at the onset of saturation.

if $\delta x_{WI} > 0.007$:

$$s_1 = \frac{\delta x_{WI}}{1 - \exp(-\delta x_{WI})}$$
$$s_2 = \exp(-\delta x_{WI}) s_1$$
$$\delta x_\infty = \ln\left(\frac{A_0}{2 q_{iS} s_1}\right) + x_{1,WI0}$$
$$\hat{q}_{1\infty} = \frac{-\delta x_{WI}}{k_{eq}\left(1 - s_1 - \delta x_{WI}/k_2\right)}$$
$$\hat{q}_{2\infty} = \frac{\delta x_{WI}}{k_{eq}\left(1 - s_2 - \delta x_{WI}/k_1\right)}$$
$$d_\infty = \frac{\delta x_{WI}}{\left(s_2/k_2 + 1/2\right)/\hat{q}_{2\infty} - \left(s_1/k_1 + 1/2\right)/\hat{q}_{1\infty}}$$

© 2023 Cadence Design Systems, Inc.

else if $\delta x_{WI} < -0.007$:

$$s_2 = \frac{\delta x_{WI}}{\exp(\delta x_{WI}) - 1}$$
$$s_1 = \exp(\delta x_{WI}) s_2$$
$$\delta x_{\infty} = \ln\left(\frac{A_0}{2 q_{iS} s_2}\right) + x_{2,WI0}$$
$$\hat{q}_{1\infty} = \frac{-\delta x_{WI}}{k_{eq}(1 - s_1 - \delta x_{WI}/k_2)}$$
$$\hat{q}_{2\infty} = \frac{\delta x_{WI}}{k_{eq}(1 - s_2 - \delta x_{WI}/k_1)}$$
$$d_{\infty} = \frac{\delta x_{WI}}{(s_2/k_2 + 1/2)/\hat{q}_{2\infty} - (s_1/k_1 + 1/2)/\hat{q}_{1\infty}}$$

else

$$s_1 = 1 + \frac{\delta x_{WI}}{2} + \frac{\delta x_{WI}^2}{12}$$
$$s_2 = 1 - \frac{\delta x_{WI}}{2} + \frac{\delta x_{WI}^2}{12}$$
$$\hat{q}_{1\infty} = \frac{1}{k_{eq}(1/2 + 1/k_2 + \delta x_{WI}/12)}$$
$$\hat{q}_{2\infty} = \frac{1}{k_{eq}(1/2 + 1/k_1 - \delta x_{WI}/12)}$$
$$\delta x_{\infty} = \ln\left(\frac{A_0}{2 q_{ic}(1 - \delta x_{WI}^2/24)}\right) + \frac{x_{1,WI0} + x_{2,WI0}}{2}$$
$$d_{\infty} = \frac{-12}{4 - 3k_{eq} + 12 k_{eq}/(k_1 k_2) + (k_{eq}/k_1 - k_{eq}/k_2)\delta x_{WI} + (1/15 - k_{eq}/12)\delta x_{WI}^2}$$

Calculation of δx_{sat} and q_{iDsat}

© 2023 Cadence Design Systems, Inc.

if $q_{iS} > 10^{-6}$

$$w_{sat1S} = \frac{100 e_{surf1S}}{100 + e_{surf1S}}$$

$$\begin{cases} sat_{fact1S} = 1/(1 - w_{sat1S}\,\mathbf{THESATG}) & \textit{if } \mathbf{THESATG} < 0 \\ sat_{fact1S} = 1 + w_{sat1S}\,\mathbf{THESATG} & \textit{else} \end{cases}$$

$$w_{sat2S} = \frac{100 e_{surf2S}}{100 + e_{surf2S}}$$

$$\begin{cases} sat_{fact2S} = 1/(1 - w_{sat2S}\,\mathbf{THESATB}) & \textit{if } \mathbf{THESATB} < 0 \\ sat_{fact2S} = 1 + w_{sat2S}\,\mathbf{THESATB} & \textit{else} \end{cases}$$

$$Z_{iS} = \frac{Z_S \Sigma_S}{a_{1S} a_{2S}} - \frac{1}{q_{iS}} \left(\frac{A_{e1S}}{a_{1S}} + \frac{A_{e2S}}{a_{2S}} \right)$$

$$d_S = \frac{Z_{iS} q_{iS}}{Z_{iS} + 1}$$

$$\delta x_i = \mathrm{MAX_FUNC}\left(\frac{q_{iS} + d_\infty \delta x_\infty}{d_\infty - d_S}, 0, 10^{-6} \right)$$

$$\gamma_{sat} = \frac{f_{vsat}}{G_{mobS}} \frac{sat_{fact1S} + sat_{fact2S}}{2}$$

$$v_S = 1 - q_{iS}/d_S$$

$$v_D = 1 + \delta x_\infty$$

$$w_D = \left((2 d_S - q_{iS})/d_\infty - 2 - \delta x_\infty \right) \delta x_i$$

$$p_S = 2/\gamma_{sat}^{\,2}$$

$$q_S = p_S + v_S$$

$$p_D = p_S + w_D$$

$$q_D = p_S + v_D$$

$$r_{cS} = \sqrt{q_S^{\,2} + 4 p_S^{\,3}/27}$$

$$r_{cD} = \sqrt{q_D^{\,2} + 4 p_D^{\,3}/27}$$

$$\delta x_{satS} = \left(\frac{r_{cS} + q_S}{2} \right)^{1/3} - \left(\frac{r_{cS} - q_S}{2} \right)^{1/3}$$

© 2023 Cadence Design Systems, Inc.

$$\delta x_{satD} = \left(\frac{r_{cD} + q_D}{2}\right)^{1/3} - \left(\frac{r_{cD} - q_D}{2}\right)^{1/3}$$

$$\delta x_{sat} = 0.47\left(\delta x_{satS} + \delta x_{satD} + \sqrt{(\delta x_{satS} - \delta x_{satD})^2 + 2(d_S - d_\infty)^4}\right)$$

$$q_{iDsatS} = q_{iS} + d_S \delta x_{sat}$$

$$q_{iDsatD} = d_\infty(\delta x_{sat} - \delta x_\infty)$$

$$q_{iDsat} = \text{MAX_FUNC}\left(q_{iDsatS}, q_{iDsatD}, 36(d_S - d_\infty)^2\right)$$

else

$$d_S = d_\infty$$

$$\delta x_{sat} = 2 \times 0.47 \times (1 + \delta x_\infty)$$

$$q_{iDsat} = q_{iS}/2 + d_\infty(\delta x_{sat} - \delta x_\infty/2)$$

Normalized saturation and effective drain voltages

$$x_{nDS,0} = \delta x_{sat} + \ln\left(\frac{q_{iS}}{0.5 + \ln(1 + \exp(q_{iDsat} - 0.5))}\right)$$

$$x_{nDS,1} = 4 + \ln(1 + \exp(x_{nDS,0} - 4))$$

$$x_{nDS,sat} = 600 - \ln(1 + \exp(600 - x_{nDS,1}))$$

$$x_{Deff} = \frac{x_D}{\left(1 + (x_D / x_{nDS,sat})^{\mathbf{AX}}\right)^{1/\mathbf{AX}}}$$

Inversion Charge and Related Quantities on Drain Side

Gate charge density at drain side:

$$q_{1D} = \text{CHARGE_DENSITY}(x_{g1x}, x_{g2eff}, x_{Deff})$$

© 2023 Cadence Design Systems, Inc.

Then, inversion and back gate charge densities, normalized to $C_{Si}'\phi_T$ and $k_2C_{Si}'\phi_T$, respectively, are calculated:

$$A_{e1D} = A_0 \exp(x_{g1x} - q_{1D} - x_{Deff})$$
$$f_{qsqD} = k_1^2 q_{1D}^2 - A_{e1D}$$

if $f_{qsqD} < -0.005$:

$$f_{qctD} = \sqrt{|f_{qsqD}|}\cot\left(\sqrt{|f_{qsqD}|}/2\right)$$
$$f_{shD} = -\frac{f_{qsqD}}{\sin\left(\sqrt{|f_{qsqD}|}/2\right)^2}$$
$$f_{lnD} = \ln(f_{shD})$$

else if $f_{qsqD} > 0.005$:

$$\zeta_D = \exp\left(-\sqrt{|f_{qsqD}|}\right)$$
$$f_{qctD} = \sqrt{|f_{qsqD}|}\frac{1+\zeta_D}{1-\zeta_D}$$
$$f_{shD} = \frac{4f_{qsqD}}{1-\zeta_D(2-\zeta_D)}\zeta_D$$
$$f_{lnD} = \ln\left(\frac{4f_{qsqD}}{1-\zeta_D(2-\zeta_D)}\right) - \sqrt{|f_{qsqD}|}$$

else

$$f_{qctD} = 2 + \frac{f_{qsqD}}{6}\left(1 - \frac{f_{qsqD}}{60}\left(1 - \frac{f_{qsqD}}{42}\right)\right)$$
$$f_{shD} = 4 - \frac{f_{qsqD}}{3}\left(1 - \frac{f_{qsqD}}{20}\left(1 - \frac{5f_{qsqD}}{126}\right)\right)$$
$$f_{lnD} = \ln(f_{shD})$$

© 2023 Cadence Design Systems, Inc.

If $1.01k_1q_{1D} + f_{qctD} \le 0$:

$$q_{iD} = \frac{k_1 q_{1D} - f_{qctD}}{1 - f_{shD}/A_{e1D}}$$
$$q_{2D} = \frac{q_{iD} - k_1 q_{1D}}{k_2}$$

else if $A_{e1D}k_1q_{1D} < 0.9k_1^2q_{1D}^2(k_1q_{1D} + f_{qctD})$

$$q_{iD} = \frac{A_{e1D}}{k_1 q_{1D} + f_{qctD}}$$
$$q_{2D} = \frac{q_{iD} - k_1 q_{1D}}{k_2}$$

else

$$q_{2D} = x_{g2eff} - x_{g1x} + q_{1D} + 2\ln\left(k_1 q_{1D} + f_{qctD}\right) - f_{lnD}$$
$$q_{iD} = k_1 q_{1D} + k_2 q_{2D}$$

Next, some required quantities, including the drift electrostatic potential, are computed:

$$A_{e2D} = A_0 \exp\left(x_{g2eff} - q_{2D} - x_{Deff}\right)$$

© 2023 Cadence Design Systems, Inc.

if $q_{iS} > 10^{-6}$

$$
\left|
\begin{array}{l}
b_{1D} = A_{e1D}/k_1 \\
b_{2D} = A_{e2D}/k_2 \\
a_{1D} = b_{1D} + 2k_1 q_{1D} \\
a_{2D} = b_{2D} + 2k_2 q_{2D} \\
\Sigma_D = 2q_{iD} + b_{1D} + b_{2D} \\
\left\{
\begin{array}{ll}
Z_D = \dfrac{-4 f_{qsqD} \Sigma_D}{q_{iD}(a_{1D}a_{2D} + 2a_{1D}(q_{2D}+2) + 2a_{2D}(q_{1D}+2))} & if \ \left|f_{qsqD}\right| > 0.005 \\
Z_D = \dfrac{A_{e1D}A_{e2D}\Sigma_D}{q_{iD}\left(a_{1D}A_{e1D} + a_{2D}A_{e2D} + a_{1D}a_{2D}q_{iD}\left(1 + \dfrac{q_{iD}}{6}\left(1 - \dfrac{f_{qsqD}}{30}\left(1 - \dfrac{f_{qsqD}}{28}\left(1 - \dfrac{f_{qsqD}}{30}\right)\right)\right)\right)\right)} & else
\end{array}
\right.
\end{array}
\right.
$$

Finally:

$$x_{driftD} = x_{Deff} + \ln(q_{iD})$$

Mid-point Inversion Charge

$$q_{im} = \frac{q_{iS} + q_{iD}}{2}$$

Mobility Attenuation and Series Resistance

Front and back transverse effective fields at drain side, normalized to $C_{Si}'\phi_T/\varepsilon_{ch}$.

$$
\begin{aligned}
e_{surf1D} &= 2\ln(1 + \exp(k_1 q_{1D}/2)) \\
e_{surf2D} &= 2\ln(1 + \exp(k_2 q_{2D}/2)) \\
e_{eff1D} &= \eta_\mu e_{surf1D} + (1 - \eta_\mu)(e_{surf2D} - k_2 q_{2D}) \\
e_{eff2D} &= \eta_\mu e_{surf2D} + (1 - \eta_\mu)(e_{surf1D} - k_1 q_{1D})
\end{aligned}
$$

© 2023 Cadence Design Systems, Inc.

Mid-values of surface and effective fields:

$$e_{surf1} = \frac{e_{surf1S} + e_{surf1D}}{2}$$
$$e_{surf2} = \frac{e_{surf2S} + e_{surf2D}}{2}$$
$$e_{eff1} = \frac{e_{eff1S} + e_{eff1D}}{2}$$
$$e_{eff2} = \frac{e_{eff2S} + e_{eff2D}}{2}$$

Coulomb scattering term:

$$G_{CS} = C_S\left(1 + q_{im}/q_{ith,CS}\right)^{-\theta_{CS}}$$

Series resistance term:

$$q_{i1m} = \frac{e_{surf1}}{e_{surf1} + e_{surf2}} q_{im}$$
$$q_{i2m} = \frac{e_{surf2}}{e_{surf1} + e_{surf2}} q_{im}$$
$$\begin{cases} G_{RS} = f_{RS} C_{Si}' q_{im}\left(1 - \mathbf{RSG}\left(q_{i1m}{}^{\mathbf{THERSG}} + q_{i2m}{}^{\mathbf{THERSG}}\right)\right) & \text{if } \mathbf{RSG} < 0 \\ G_{RS} = f_{RS} C_{Si}' q_{im} / \left(1 + \mathbf{RSG}\left(q_{i1m}{}^{\mathbf{THERSG}} + q_{i2m}{}^{\mathbf{THERSG}}\right)\right) & \text{else} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Total mobility degradation term, including high field mobility effect:

$$G_{mob1} = 1 + \left(f_{\mu E} e_{eff1}\right)^{\theta_\mu} + G_{CS} + \beta_{N1} G_{RS}$$
$$G_{mob2} = 1 + \left(f_{\mu E} e_{eff2}\right)^{\theta_\mu} + G_{CS} + \beta_{N2} G_{RS}$$
$$c_1 = e_{surf1} \beta_{N1}$$
$$c_2 = e_{surf2} \beta_{N2}$$
$$G_{mob} = f_{cor} \frac{c_1 + c_2}{c_1 / G_{mob1} + c_2 / G_{mob2}}$$
$$\beta_{Neff} = \frac{c_1 + c_2}{e_{surf1} + e_{surf2}}$$

Channel Length Modulation

$$q^*_{im1} = q_{im} + 4$$
$$r_1 = q_{im} / q^*_{im1}$$
$$\Delta L / L = \mathbf{ALP} \times \ln\left(1 + \left(x_D - x_{Deff}\right) f_{vp}\right)$$
$$G_{\Delta L} = \frac{1}{1 + \Delta L / L \left(1 + \Delta L / L\right)}$$
$$\Delta L_1 / L = \left(\mathbf{ALP} + f_{alp1} r_1 / q^*_{im1}\right) \times \ln\left(1 + \left(x_D - x_{Deff}\right) f_{vp}\right)$$
$$F_{\Delta L} = \frac{1 + \Delta L_1 / L \left(1 + \Delta L_1 / L\right)}{1 + \Delta L / L \left(1 + \Delta L / L\right)}$$

© 2023 Cadence Design Systems, Inc.

Velocity Saturation

$$w_{sat1} = \frac{100 e_{surf1}}{100 + e_{surf1}}$$

$$\begin{cases} sat_{fact1} = 1/(1 - w_{sat1}\,\mathbf{THESATG}) & \text{if } \mathbf{THESATG} < 0 \\ sat_{fact1} = 1 + w_{sat1}\,\mathbf{THESATG} & \text{else} \end{cases}$$

$$w_{sat2} = \frac{100 e_{surf2}}{100 + e_{surf2}}$$

$$\begin{cases} sat_{fact2} = 1/(1 - w_{sat2}\,\mathbf{THESATB}) & \text{if } \mathbf{THESATB} < 0 \\ sat_{fact2} = 1 + w_{sat2}\,\mathbf{THESATB} & \text{else} \end{cases}$$

$$\delta x_{drift} = x_{driftD} - x_{driftS}$$

$$G_{\gamma} = f_{vsat}\,\delta x_{drift}\,\frac{sat_{fact1} + sat_{fact2}}{2}$$

$$z_{sat} = \left(\frac{G_{\gamma}}{G_{mob} G_{\Delta L}}\right)^2$$

$$G_{vsat} = G_{mob} G_{\Delta L} \sqrt{1 + z_{sat}}$$

Quantum Confinement

if QMC > 0:

$$qm_{fact1} = \frac{1 + k_1 qq\, 0.6 / \left(e_{surf1}{}^2 + 60\right)^{1/6}}{t_{ox1\,fact}}$$

$$qm_{fact2} = \frac{1 + k_2 qq\, 0.6 / \left(e_{surf2}{}^2 + 60\right)^{1/6}}{t_{ox2\,fact}}$$

$$qm_{fact} = \frac{e_{surf1} + e_{surf2}}{e_{surf1}/qm_{fact1} + e_{surf2}/qm_{fact2}}$$

else:

$$qm_{fact1} = 1$$

$$qm_{fact2} = 1$$

$$qm_{fact} = 1$$

© 2023 Cadence Design Systems, Inc.

Channel Current

If $q_{iS} > 10^{-6}$

$$Z_{iD} = \frac{Z_D \Sigma_D}{a_{1D} a_{2D}} - \frac{1}{q_{iD}} \left(\frac{A_{e1D}}{a_{1D}} + \frac{A_{e2D}}{a_{2D}} \right)$$

$$\begin{cases} d_D = \dfrac{Z_{iD} q_{iD}}{Z_{iD} + 1} & \text{if } q_{iD} > 10^{-6} \\ d_D = d_\infty & \text{else} \end{cases}$$

$$L_S = q_{iD} - q_{iS} - d_D \delta x_{drift}$$

$$L_D = q_{iD} - q_{iS} - d_S \delta x_{drift}$$

$$U_S = \sqrt{L_S{}^2 + 36(d_D - d_S)^2}$$

$$U_D = \sqrt{L_D{}^2 + 36(d_D - d_S)^2}$$

$$i_{drift1} = \left(q_{im} - \frac{U_S + U_D}{4} \right) \delta x_{drift}$$

$$\begin{cases} i_{drift2} = 9(d_D - d_S) \ln \left(\dfrac{L_D + U_D}{L_S + U_S} \right) & \text{if } |d_D - d_S| > 10^{-10} \\ i_{drift2} = 0 & \text{else} \end{cases}$$

$$\begin{cases} i_{drift3} = \dfrac{L_D U_D - L_S U_S}{4(d_D - d_S)} & \text{if } |d_D - d_S| > 10^{-10} \\ i_{drift3} = 0 & \text{else} \end{cases}$$

$$i_{drift} = i_{drift1} + i_{drift2} + i_{drift3}$$

else

$$d_D = d_\infty$$

$$i_{drift} = q_{im} \delta x_{drift}$$

$$i_{DS,norm} = i_{drift} + q_{iS} - q_{iD}$$

$$I_{DS} = \frac{F_{\Delta L}}{G_{vsat} qm_{fact}} \beta_{Neff} \phi_T{}^2 C_{Si}{}' i_{DS,norm}$$

© 2023 Cadence Design Systems, Inc.

Gate Current, Intrinsic Charges and Overlap Related Variables

Effective Gate Charge at Front and Back Interfaces

If $q_{iS} > 10^{-6}$

$$\hat{q}_{1S} = \frac{a_{1S}}{A_{e1S}/q_{iS} - Z_S}$$

$$\hat{q}_{1D} = \frac{a_{1D}}{A_{e1D}/q_{iD} - Z_D}$$

$$k_1 h_{10} = \frac{i_{DS,norm}}{\hat{q}_{1S} - \hat{q}_{1D}}$$

$$\hat{q}_{2S} = \frac{a_{2S}}{A_{e2S}/q_{iS} - Z_S}$$

$$\hat{q}_{2D} = \frac{a_{2D}}{A_{e2D}/q_{iD} - Z_D}$$

$$k_2 h_{20} = \frac{i_{DS,norm}}{\hat{q}_{2S} - \hat{q}_{2D}}$$

else

$$\zeta_1 = -2s_1\left(\frac{1}{k_1\hat{q}_{1\infty}} + \frac{1}{d_\infty}\right)$$

$$\zeta_2 = -2s_2\left(\frac{1}{k_2\hat{q}_{2\infty}} + \frac{1}{d_\infty}\right)$$

$$\xi_1 = \frac{\zeta_2/k_2 + (\zeta_2 - \zeta_1)/d_\infty - (\zeta_1/k_1 + \zeta_2/k_2)/\hat{q}_{1\infty}}{3 + 2(s_1/k_1 + s_2/k_2)}$$

$$\xi_2 = \frac{\zeta_1/k_1 + (\zeta_1 - \zeta_2)/d_\infty - (\zeta_2/k_2 + \zeta_1/k_1)/\hat{q}_{2\infty}}{3 + 2(s_2/k_2 + s_1/k_1)}$$

$$k_1 h_{10} = -\frac{1}{\hat{q}_{1\infty}(\xi_1\hat{q}_{1\infty} + 1/d_\infty)}$$

$$k_2 h_{20} = -\frac{1}{\hat{q}_{2\infty}(\xi_2\hat{q}_{2\infty} + 1/d_\infty)}$$

© 2023 Cadence Design Systems, Inc.

$$k_1h_1 = k_1h_{10}\frac{\sqrt{1+z_{sat}}}{1+3z_{sat}/2}$$

$$k_2h_2 = k_2h_{20}\frac{\sqrt{1+z_{sat}}}{1+3z_{sat}/2}$$

$$\Delta_{k1q1} = \frac{k_1q_{1D} - k_1q_{1S}}{2}$$

$$\Delta_{k2q2} = \frac{k_2q_{2D} - k_2q_{2S}}{2}$$

$$P_1 = \frac{\Delta_{k1q1}}{k_1h_1}$$

$$P_2 = \frac{\Delta_{k2q2}}{k_2h_2}$$

Surface Potential and Gate Dielectric Voltage Drop in Gate-Source Overlap Region

$$G_{ov} = \frac{\sqrt{2q\varepsilon_{ch}\mathbf{NOV}}}{C_{ox1}'\sqrt{\phi_{T0}}}$$

$$\xi_{ov} = 1 + \frac{G_{ov}}{\sqrt{2}}$$

$$\xi_{mrg,ov} = 10^{-5}\xi_{ov}$$

$$x_{g1,ov} = 1.25 + 0.7324648775G_{ov}$$

$$x_{S,ov} = \mathrm{SP_FDSOI_OV}\left(x_{gs,ov}\right)$$

$$x_{S,ovcv} = \mathrm{SP_FDSOI_OV}\left(x_{gs,ovcv}\right)$$

$$V_{ovS} = -\phi_{T0}\left(x_{gs,ov} + x_{S,ov}\right)$$

$$V_{ovS,cv} = -\phi_{T0}\left(x_{gs,ovcv} + x_{S,ovcv}\right)$$

© 2023 Cadence Design Systems, Inc.

Surface Potential and Gate Dielectric Voltage Drop in Gate-Drain Overlap Region

$$G_{ov} = \frac{\sqrt{2q\varepsilon_{ch}\mathbf{NOVD}}}{C_{ox1}'\sqrt{\phi_{T0}}}$$

$$\xi_{ov} = 1 + \frac{G_{ov}}{\sqrt{2}}$$

$$\xi_{mrg,ov} = 10^{-5}\xi_{ov}$$

$$x_{g1,ov} = 1.25 + 0.7324648775 G_{ov}$$

$$x_{D,ov} = \mathrm{SP_FDSOI_OV}\left(x_{gd,ov}\right)$$

$$x_{D,ovcv} = \mathrm{SP_FDSOI_OV}\left(x_{gd,ovcv}\right)$$

$$V_{ovD} = -\phi_{T0}\left(x_{gd,ov} + x_{D,ov}\right)$$

$$V_{ovD,cv} = -\phi_{T0}\left(x_{gd,ovcv} + x_{D,ovcv}\right)$$

Gate Current

Gate current calculation is not performed when the `SWIGATE` flag is set to 0.

© 2023 Cadence Design Systems, Inc.

Gate-to-Source Overlap Component

$$\psi_t = \text{MIN_FUNC}\left(V_{ovS} + D_{ov}, 0, 0.01\right)$$

$$G_{C2,oveff} = \frac{\textbf{GC2OVACC} + \textbf{GC2OVINV}\exp\left(x_{gs,ov}/2\right)}{1+\exp\left(x_{gs,ov}/2\right)}$$

$$G_{C3,oveff} = \frac{\textbf{GC3OVACC} + \textbf{GC3OVINV}\exp\left(x_{gs,ov}/2\right)}{1+\exp\left(x_{gs,ov}/2\right)}$$

$$G_{CQ,oveff} = \frac{G_{CQ,ovacc} + G_{CQ,ovinv}\exp\left(x_{gs,ov}/2\right)}{1+\exp\left(x_{gs,ov}/2\right)}$$

$$I_{G,oveff} = \frac{I_{G,ovacc} + I_{G,ovinv}\exp\left(x_{gs,ov}/2\right)}{1+\exp\left(x_{gs,ov}/2\right)}$$

$$\begin{cases} z_g = \text{MIN_FUNC}\left(\dfrac{\sqrt{V_{ovS}{}^2 + 10^{-6}}}{\textbf{CHIB}}, G_{CQ,oveff}, 10^{-6}\right) & \text{if } G_{C3,oveff} < 0 \\ z_g = \dfrac{\sqrt{V_{ovS}{}^2 + 10^{-6}}}{\textbf{CHIB}} & \text{else} \end{cases}$$

$$\Delta_{Si} = \exp\left(3 + x_{S,ov} + \psi_t/\phi_{T0}\right)$$

$$\Delta_{gate} = \exp\left(3 + x_{S,ov} + \left(\psi_t - V_{GS}\right)/\phi_{T0}\right)$$

$$I_{GS,ov} = I_{G,oveff}\ln\left(\frac{1+\Delta_{Si}}{1+\Delta_{gate}}\right)\exp\left(B_{ov}\left(z_g\left(G_{C2,oveff} + z_g G_{C3,oveff}\right) - 3/2\right)\right)$$

© 2023 Cadence Design Systems, Inc.

Gate-to-Drain Overlap Component

$$\psi_t = \text{MIN_FUNC}\left(V_{ovD} + D_{ov}, 0, 0.01\right)$$

$$G_{C2,oveff} = \frac{\mathbf{GC2OVACC} + \mathbf{GC2OVINV}\exp\left(x_{gd,ov}/2\right)}{1+\exp\left(x_{gd,ov}/2\right)}$$

$$G_{C3,oveff} = \frac{\mathbf{GC3OVACC} + \mathbf{GC3OVINV}\exp\left(x_{gd,ov}/2\right)}{1+\exp\left(x_{gd,ov}/2\right)}$$

$$G_{CQ,oveff} = \frac{G_{CQ,ovacc} + G_{CQ,ovinv}\exp\left(x_{gd,ov}/2\right)}{1+\exp\left(x_{gd,ov}/2\right)}$$

$$I_{G,oveff} = \frac{I_{G,ovaccD} + I_{G,ovinvD}\exp\left(x_{gd,ov}/2\right)}{1+\exp\left(x_{gd,ov}/2\right)}$$

$$\begin{cases} z_g = \text{MIN_FUNC}\left(\dfrac{\sqrt{{V_{ovD}}^2 + 10^{-6}}}{\mathbf{CHIB}}, G_{CQ,oveff}, 10^{-6}\right) & \text{if } G_{C3,oveff} < 0 \\ z_g = \dfrac{\sqrt{{V_{ovD}}^2 + 10^{-6}}}{\mathbf{CHIB}} & \text{else} \end{cases}$$

$$\Delta_{Si} = \exp\left(3 + x_{D,ov} + \psi_t/\phi_{T0}\right)$$

$$\Delta_{gate} = \exp\left(3 + x_{D,ov} + \left(\psi_t - V_{GD}\right)/\phi_{T0}\right)$$

$$I_{GD,ov} = I_{G,oveff}\ln\left(\frac{1+\Delta_{Si}}{1+\Delta_{gate}}\right)\exp\left(B_{ov}\left(z_g\left(G_{C2,oveff} + z_g G_{C3,oveff}\right) - 3/2\right)\right)$$

© 2023 Cadence Design Systems, Inc.

Gate-to-Channel Component

$$x_{DS} = -2\Delta_{k1q1}/k_1$$

$$V_m = \phi_T\left(\frac{x_{DS}}{2} - \ln\left(\frac{1+\exp\left(x_{DS}-x_{Deff}\right)}{2}\right)\right)$$

$$q_{1m} = \frac{q_{1S}+q_{1D}}{2}$$

$$V_{oxm} = \phi_T q_{1m}$$

$$\psi_t = \text{MIN_FUNC}\left(V_{oxm}+D_{ch},0,0.01\right)$$

$$\begin{cases} z_g = \text{MIN_FUNC}\left(\dfrac{\sqrt{{V_{oxm}}^2+10^{-6}}}{\textbf{CHIB}}, G_{CQ,ch}, 10^{-6}\right) & \textit{if } \textbf{GC3CH} < 0 \\ z_g = \dfrac{\sqrt{{V_{oxm}}^2+10^{-6}}}{\textbf{CHIB}} & \textit{else} \end{cases}$$

$$\Delta_{Si} = \exp\left(\left(x_{g1x} - q_{1m} + \left(\psi_t - \alpha_b - V_m\right)/\phi_T\right)\times n_{iginv}\right)$$

$$\Delta_{gate} = \Delta_{Si}\exp\left(-\left(V_{GS}-V_m\right)/\phi_T \times n_{iginv}\right)$$

$$I_{GC0} = I_{G,inv}\ln\left(\frac{1+\Delta_{Si}}{1+\Delta_{gate}}\right)\exp\left(B_{ch}\left(z_g\left(\textbf{GC2CH} + z_g\textbf{GC3CH}\right) - 3/2\right)\right)$$

© 2023 Cadence Design Systems, Inc.

Source/Drain Partitioning of Gate-to-Channel Current

If $x_{g1x} > 0$:

$$u_0 = \frac{\mathbf{CHIB}/\phi_T}{B_{ch}\left(\mathbf{GC2CH} + 2z_g\mathbf{GC3CH}\right)}$$

$$x = \frac{x_{DS}}{2u_0}$$

$$b = \frac{u_0}{k_1 h_1 / k_1}$$

$$B_g = b(1-b)/2$$

$$A_g = 1/2 - 3B_g$$

$$p_{GC} = (1-b)\frac{\sinh(x)}{x} + b\cosh(x)$$

$$p_{GD} = \frac{p_{GC}}{2} - B_g \sinh(x) - \frac{A_g}{x}\left(\cosh(x) - \frac{\sinh(x)}{x}\right)$$

else:

$$p_{GC} = 1$$

$$p_{GD} = 1/2$$

$$I_{GC} = I_{GC0} p_{GC}$$

$$I_{GCD} = I_{GC0} p_{GD}$$

$$I_{GCS} = I_{GC} - I_{GCD}$$

Gate-to-Source and Gate-to-Drain Total Currents

$$I_{GS} = I_{GCS} + I_{GS,ov}$$

$$I_{GD} = I_{GCD} + I_{GD,ov}$$

© 2023 Cadence Design Systems, Inc.

Gate Induced Drain/Source Leakage (GIDL/GISL)

Gate Induced Source Leakage

$$V_{tovS} = \sqrt{V_{ovS}{}^2 + \mathbf{CGIDL}^2 V_{SB}{}^2 + 10^{-6}}$$

$$I_{GISL} = -A_{GIDL} V_{SD} V_{ovS} V_{tovS} \exp\left(-\frac{B_{GIDL}}{V_{tovS}}\right)$$

Gate Induced Drain Leakage

$$V_{tovD} = \sqrt{V_{ovD}{}^2 + \mathbf{CGIDLD}^2 V_{DB}{}^2 + 10^{-6}}$$

$$I_{GIDL} = -A_{GIDLD} V_{DS} V_{ovD} V_{tovD} \exp\left(-\frac{B_{GIDLD}}{V_{tovD}}\right)$$

Charge Model

Quantum Mechanical Corrections

$$k_1 q_{1m} = \frac{k_1 q_{1S} + k_1 q_{1D}}{2}$$

$$k_2 q_{2m} = \frac{k_2 q_{2S} + k_2 q_{2D}}{2}$$

$$\begin{cases} k_1 q_{1eff} = k_1 q_{1m} - \dfrac{qm_{fact1} - 1}{qm_{fact1}} \left(e_{surf1} + k_2 q_{2m} - e_{surf2}\right) & \textit{if } \mathbf{QMC} > 0 \\ k_1 q_{1eff} = k_1 q_{1m} & \textit{else} \end{cases}$$

$$\begin{cases} k_2 q_{2eff} = k_2 q_{2m} - \dfrac{qm_{fact2} - 1}{qm_{fact2}} \left(e_{surf2} + k_1 q_{1m} - e_{surf1}\right) & \textit{if } \mathbf{QMC} > 0 \\ k_2 q_{2eff} = k_2 q_{2m} & \textit{else} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Intrinsic Charge Model

$$Q_G = C_{Si}' f_{area}\left(k_1 q_{1eff} + \frac{\Delta_{k1q1}}{3} P_1 \right) c_{sce1}$$

$$Q_B = C_{Si}' f_{area}\left(k_2 q_{2eff} + \frac{\Delta_{k2q2}}{3} P_2 \right) c_{sce2}$$

$$Q_D = -\frac{C_{Si}' f_{area}}{2}\left[\left(k_1 q_{1eff} + \frac{\Delta_{k1q1}}{3}\left(1 + P_1 - \frac{P_1^2}{5} \right) \right) c_{sce1} + \left(k_2 q_{2eff} + \frac{\Delta_{k2q2}}{3}\left(1 + P_2 - \frac{P_2^2}{5} \right) \right) c_{sce2} \right]$$

Parasitic Charges

Outer fringe and overlap charges

$$Q_{GS} = \mathbf{CFR} \times V_{GS}$$

$$Q_{GD} = \mathbf{CFRD} \times V_{GD}$$

$$Q_{ovS} = \mathbf{COV} \times V_{ovS,cv} / \mathrm{MAX_FUNC}\left(1 + \mathbf{COVDL} \times \delta l_{eff}, 0.1, 0.01\right)$$

$$Q_{ovD} = \mathbf{COVD} \times V_{ovD,cv} / \mathrm{MAX_FUNC}\left(1 + \mathbf{COVDL} \times \delta l_{eff}, 0.1, 0.01\right)$$

$$Q_{GB} = \mathbf{CGBOV} \times V_{GB}$$

Drain-to-source direct coupling

$$Q_{DS} = \mathbf{CSD} \times V_{DS}$$

Substrate Extrinsic Charge Model

$$Q_{BS} = -\left(C_{ox2}' \times A_{source,f} + \mathbf{CSDBP} \times P_{source,f} \right) V_{SB}$$

$$Q_{BD} = -\left(C_{ox2}' \times A_{drain,f} + \mathbf{CSDBP} \times P_{drain,f} \right) V_{DB}$$

© 2023 Cadence Design Systems, Inc.

Self-Heating

A temperature node named `Tnode` is used to compute the channel temperature elevation induced by the self-heating effect.

$$\Delta T_C = Temp(Tnode)$$

$$I_{th} = \frac{\Delta T_C}{R_{th}} - I_{DS} V_{DS}$$

$$Q_{th} = \mathbf{CTH} \times \Delta T_C$$

Noise Model

Channel Thermal Noise

$$d_m = -\frac{d_S + d_D}{2}$$

$$q_{im}^* = q_{im} + d_m$$

$$t_1 = \frac{q_{im}}{q_{im}^*}$$

$$t_2 = \left(-\frac{\Delta_{k1q1}}{6 k_1 h_{10}} \right)^2$$

$$R = \frac{1 + 3 z_{sat}/2}{\sqrt{1 + z_{sat}}} - 1$$

$$I_C = 1 - 12 t_2 R$$

$$g_{ideal} = \beta_{Neff} C_{Si}{}' \phi_T q_{im}^* \frac{F_{\Delta L}}{G_{vsat} qm_{fact}}$$

$$g_{Sid} = \frac{g_{ideal}}{I_C{}^2} \left(t_1 + 12 t_2 - 24 (1 + t_1) t_2 R \right)$$

$$S_{ids,th} = n_T g_{Sid}$$

© 2023 Cadence Design Systems, Inc.

Induced Gate Noise

Induced gate noise and its correlation with drain thermal noise are computed only when the `SWIGN` flag is set to 1.

$$C_{Geff} = (1 + z_{sat}) \frac{k_1 C_{Si}'}{qm_{fact1}} \textbf{AREAQ}$$

$$g_{Sig} = \frac{g_{ideal} {I_C}^2}{t_1/12 - (1/5 + t_1 - 12t_2)t_2 - 8/5(1 + t_1 - 12t_2)t_2 R}$$

$$S_{ig,th} = n_T g_{Sig} \frac{(2\pi f_{op} C_{Geff}/g_{Sig})^2}{1 + (2\pi f_{op} C_{Geff}/g_{Sig})^2}$$

The gate induced noise current is finally partitioned between the gate-source and the gate-drain branches, with a VDS dependent fraction equal to $1/2 + \sqrt{t_2}/4$ and $1/2 - \sqrt{t_2}/4$, respectively. The noise currents in these two branches are thus perfectly correlated and correspond to the following spectral densities:

$$S_{igs,th} = \left(\frac{1}{2} + \frac{\sqrt{t_2}}{4}\right)^2 S_{ig,th}$$

$$S_{igd,th} = \left(\frac{1}{2} - \frac{\sqrt{t_2}}{4}\right)^2 S_{ig,th}$$

Drain and Gate Thermal Noise Correlation

$$m_{igid} = \frac{\sqrt{t_2}}{{I_C}^2}(1 - 12t_2 - (t_1 + 96t_2/5 - 12t_1 t_2)t_2 R)$$

$$S_{igid,th} = n_T \frac{2j\pi f_{op} C_{Geff} m_{igid}}{1 + 2j\pi f_{op} C_{Geff}/g_{Sig}}$$

© 2023 Cadence Design Systems, Inc.

Verilog-A Implementation of Induced Gate Noise and Correlation

Since there is no noise function with frequency dependence suitable for the induced gate noise in Verilog-A, an internal node NSIG linked to the ground through a parallel RC circuit is used. The currents in the different branches are given by:

$$I(NOIR) = g_{Sia} V(NSIG)$$
$$I(NOIC) = \frac{d}{dt}\left(C_{Geff} V(NSIG)\right)$$
$$I(NOII) = \text{white_noise}\left(Mult_f n_T g_{Sig}\right)$$

The noise current in the gate-source and gate-drain branches is obtained by:

$$I_{gs,th} = \frac{d}{dt}\left(-\left(\frac{1}{2} + \frac{\sqrt{t_2}}{4}\right) C_{Geff} V(NSIG)\right)$$
$$I_{gd,th} = \frac{d}{dt}\left(-\left(\frac{1}{2} - \frac{\sqrt{t_2}}{4}\right) C_{Geff} V(NSIG)\right)$$

A variable c_{igid} is then defined to obtain the correct correlation between the drain thermal noise current and the gate induced one:

$$c_{igid} = m_{igid}\sqrt{\frac{g_{Sig}}{g_{Sid}}}$$

The channel thermal noise current is finally given as the sum of an uncorrelated part and a correlated one:

$$I_{ds,th} = \text{white_noise}\left(Mult_f S_{ids,th}\left(1 - c_{igid}{}^2\right)\right) + m_{igid} I(NOII)$$

© 2023 Cadence Design Systems, Inc.

Channel Flicker Noise

$$N_{unit} = \frac{C_{Si}'\phi_T}{q}$$

$$N^* = N_{unit} d_m$$

$$N_m^* = N_{unit}(q_{im} + 1)$$

$$\Delta N = N_{unit}(q_{iS} - q_{iD})$$

$$f_{NFE} = \text{MAX_FUNC}\left(1 + \frac{e_{surf1}\mathbf{NFE} + e_{surf2}\mathbf{NFEB}}{q_{im} + 1}, 0.01, 0.0001\right)$$

$$S_{ids,fl} = \frac{q\beta_{Neff}\phi_T{}^2 I_{DS}}{f_{op}{}^{\mathbf{EF}} G_{vsat} N^*}\left[\left(\mathbf{NFA} - N^*\mathbf{NFB} + N^{*2}\mathbf{NFC}\right)\ln\left(\frac{N_m^* + \Delta N/2}{N_m^* - \Delta N/2}\right) + \left(\mathbf{NFB} + \mathbf{NFC}\left(N_m^* - 2N^*\right)\right)\Delta N\right] f_{NFE}$$

Shot Noises

Gate current shot noise:

$$S_{igs,sh} = 2q|I_{GS}|$$

$$S_{igd,sh} = 2q|I_{GD}|$$

GIDL/GISL shot noise:

$$S_{ids,sh} = 2q|I_{GIDL} - I_{GISL}|$$

Total Current and Charges

Total currents in the branches and the total node charges are obtained as follows:

© 2023 Cadence Design Systems, Inc.

Static Currents

$$I_{DS,dc} = Mult_f \times \mathbf{TYPE} \times (I_{DS} + I_{GIDL} - I_{GISL})$$
$$I_{GS,dc} = Mult_f \times \mathbf{TYPE} \times I_{GS}$$
$$I_{GD,dc} = Mult_f \times \mathbf{TYPE} \times I_{GD}$$
$$I_{BS,dc} = 0$$
$$I_{BD,dc} = 0$$
$$I_{GB,dc} = 0$$

Total Charges

$$Q_{G,tot} = Mult_f \times \mathbf{TYPE} \times (Q_G + Q_{GS} + Q_{GD} + Q_{ovS} + Q_{ovD} + Q_{GB})$$
$$Q_{D,tot} = Mult_f \times \mathbf{TYPE} \times (Q_D + Q_{DS} - Q_{GD} - Q_{ovD} - Q_{BD})$$
$$Q_{B,tot} = Mult_f \times \mathbf{TYPE} \times (Q_B + Q_{BS} + Q_{BD} - Q_{GB})$$
$$Q_{S,tot} = -Q_{G,tot} - Q_{D,tot} - Q_{B,tot}$$

Dynamic Currents

$$I_{DS,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_D + Q_{DS})/dt$$
$$I_{GS,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_G + Q_{GS} + Q_{ovS})/dt$$
$$I_{GD,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_{GD} + Q_{ovD})/dt$$
$$I_{BS,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_B + Q_{BS})/dt$$
$$I_{BD,ac} = Mult_f \times \mathbf{TYPE} \times dQ_{BD}/dt$$
$$I_{GB,ac} = Mult_f \times \mathbf{TYPE} \times dQ_{GB}/dt$$

© 2023 Cadence Design Systems, Inc.

Operating Point Output

Voltages

First, the effective threshold voltage of the device has to be calculated at the transistor operating point:

$$r_{1,op} = \frac{k_2}{k_1(1+k_2)}$$

$$r_{2,op} = \frac{k_1}{k_2(1+k_1)}$$

$$x_{1sat,op} = \ln\left(k_1(1+r_{1,op})\frac{diff_{\min}}{A_0} \right) + 2$$

$$x_{2sat,op} = \ln\left(k_2(1+r_{2,op})\frac{diff_{\min}}{A_0} \right) + 2$$

$$x_{th1,op} = x_{1sat,op}(1+r_{1,op}) - x_{g2eff} r_{1,op}$$

$$x_{th2,op} = x_{2sat,op}(1+1/r_{2,op}) - x_{g2eff}/r_{2,op}$$

$$x_{g1th,op} = \frac{\text{MIN_FUNC}(x_{th1,op}, x_{th2,op}, 36) - x_{g2}}{\text{CICF}} + x_{g2}$$

$$V_{th} = \phi_T \left(\frac{x_{g1th,op} - E_g/(2\phi_{T0})}{c_{sce1}} - \delta x_{g1,DIBL} + \frac{E_g}{2\phi_T} \right) + V_{FB1}$$

The drain saturation voltage is computed, as follows:

$$V_{Dsat} = \phi_T x_{nDS,sat}$$

Component Statements

Model Definition

```
model modelName utsoi2 parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Definition

```
Name  d  g  s  b  [Tnode] ModelName parameter=value ...
```

Instance Parameters

1	`l=1.0e-6`	Channel length(m).
2	`w=1.0e-6`	Channel width(m).
3	`asource=1.0e-12`	Source region area (m^2).
4	`adrain=1.0e-12`	Drain region area (m^2).
5	`psource=1.0e-6`	Source region perimeter (m).
6	`pdrain=1.0e-6`	Drain region perimeter (m).
7	`sa=0.0`	Distance between OD-edge and poly at source side(m).
8	`sb=0.0`	Distance between OD-edge and poly at drain side(m).
9	`sd=0.0`	Distance between neighboring fingers(m).
10	`nf=1.0`	Number of fingers.
11	`mult=1.0`	Number of devices in parallel.
12	`m=1.0`	Number of devices in parallel.
13	`delvto=0.0`	Threshold voltage shift parameter (V).
14	`factuo=1.0`	Low-field mobility pre-factor.
15	`trise=0.0`	Temperature rise from ambient.
16	`isnoisy=yes`	Should device generate noise. Possible values are `yes` and `no`.
17	`dtemp`	Alias for trise.

Model Parameters

1	`swscale=0.0`	Parameter setting mode (local=0, global=1).
2	`version=2.00`	Model version number. Available versions are 2.00, 2.10, 2.11, 2.20, and 2.30. The default version is 2.00.

© 2023 Cadence Design Systems, Inc.

3	`swclipchk=0.0`	Flag for checking of parameters clipping (without=0, with=1).
4	`swsubdep=0.0`	Flag for substrate depletion model (without=0, with=1).
5	`swigate=0.0`	Flag for gate current (without=0, with=1).
6	`swgidl=0.0`	Flag for GIDL current (without=0, with=1).
7	`swshe=0.0`	Flag for self-heating effect (without=0, with=1).
8	`swign=1.0`	Flag for induced gate noise model (without=0, with=1).
9	`swjunasym=0.0`	Flag for source/drain junction asymmetry (without=0, with=1).
10	`qmc=1.0`	Quantum correction factor (no correction=0, full correction=1).
11	`type=1.0`	Channel type parameter, +1|n=NMOS -1|p=PMOS. Possible values are `p` and `n`.
12	`tr=21.0 C`	Nominal temperature.
12	`tref=21.0`	alias of TR, Nominal temperature (C).
13	`tmax=150.0`	Maximum self-heating temperature elevation (C).
14	`toxe=2.0e-09`	Front gate equivalent oxide thickness (m).
15	`tsi=1.0e-08`	Silicon or SiGe film thickness (m).
16	`xge=0.0`	Fraction of Ge content in the channel.
17	`tbox=1.0e-07`	Back gate oxide thickness (m).
18	`nch=0.0`	Thin film doping (n-type=negative value, p-type=positive value) (cm^-3).
19	`nsub=3.0e18`	Substrate doping (n-type=negative value, p-type=positive value) (cm^-3).
20	`ct=0.0`	Interface states factor.
21	`toxp=2.0e-09`	Front gate physical oxide thickness (m).
22	`nov=1.0e20`	Effective doping of overlap-ldd regions (no doping effect=0) (cm^-3).
23	`novd=1.0e20`	Effective doping of overlap-ldd regions ar drain side (cm^-3).
24	`vfb=0.0`	Flat-band voltage of the front gate at TR (V).

© 2023 Cadence Design Systems, Inc.

25	`vfbb=0.0`	Flat-band voltage of the back gate at TR (V).
26	`stvfb=0.0`	Temperature dependence of VFB and VFBB (V/K).
27	`cicf=1.0`	Long channel front interface coupling coefficient.
28	`cic=1.0`	Long channel back interface coupling coefficient.
29	`psce=0.0`	Short channel effect coefficient.
30	`psceb=1.0`	Short channel back to front interface asymmetry factor.
31	`pscedl=0.0`	Short channel modulation coefficient due to Leff variation.
32	`nsddc=1.0e22`	Source/Drain effective doping level for DC model (cm^-3).
33	`pscedlb=0.0`	Back bias dependence of short channel effect modulation.
34	`pnce=0.0`	Narrow channel effect on body factor.
35	`cf=0.0`	DIBL parameter.
36	`cfb=1.0`	DIBL back-to-front interface asymmetry factor.
37	`stcf=0.0`	Temperature dependence of CF, with same scaling as CF.
38	`cfd=0.2`	Drain voltage dependence parameter of DIBL (V).
39	`cfdl=0.0`	DIBL modulation coefficient due to Leff variation.
40	`cfdlb=0.0`	Back bias dependence of DIBL modulation.
41	`betn=5.0e-2`	Front channel aspect ratio times zero-field mobility (m^2/V/s).
42	`betnb=1.0`	Back channel over front channel zero-field mobility ratio.
43	`stbet=1.5`	Temperature dependence of BETN.
44	`cs=0.0`	Remote Coulomb scattering parameter at TR.
45	`csfi=0.0`	Field dependence of Coulomb scattering at front interface.
46	`csbi=0.0`	Field dependence of Coulomb scattering at back interface.
47	`stcs=0.0`	Temperature dependence of CS.

© 2023 Cadence Design Systems, Inc.

48	`thecs=1.5`	Remote Coulomb scattering exponent at TR.
49	`stthecs=0.0`	Temperature dependence of THECS.
50	`csthr=2.0`	Remote Coulomb scattering threshold level.
51	`csthrb=1.0`	Remote Coulomb scattering threshold asymmetry parameter.
52	`mue=0.0`	Front channel mobility reduction coefficient at TR (cm/MV).
53	`stmue=0.0`	Temperature dependence of MUE.
54	`themu=1.5`	Front channel mobility reduction exponent at TR.
55	`stthemu=0.0`	Temperature dependence of THEMU.
56	`xcor=0.0`	Front channel non-universality factor (V^-1).
57	`xcorb=1.0`	Asymmetry term of non-universality factor.
58	`stxcor=0.0`	Temperature dependence of XCOR.
59	`feta=1.0`	Effective field parameter.
60	`rs=30.0`	Source/Drain series resistance at TR (Ohm).
61	`rsig=0.0`	Source/Drain extension resistance coefficient.
62	`strs=0.0`	Temperature dependence of RS.
63	`rsg=0.0`	Transverse electric field dependence of RS.
64	`thersg=2.0`	Transverse electric field dependence exponent of RS.
65	`rsb=0.0`	Back bias dependence of RS.
66	`thesat=0.0`	Velocity saturation parameter at TR (V^-1).
67	`stthesat=(-0.1)`	Temperature dependence of THESAT.
68	`thesatg=0.0`	Front gate bias dependence of velocity saturation.
69	`thesatb=0.0`	Back gate bias dependence of velocity saturation.
70	`ax=8.0`	Linear/saturation transition exponent.
71	`alp=0.0`	CLM pre-factor.
72	`alp1=0.0`	CLM enhancement factor above threshold (V).
73	`alpb=0.0`	Back bias dependence of channel length modulation.
74	`vp=0.05`	CLM logarithm dependence factor (V).

© 2023 Cadence Design Systems, Inc.

75	`vpg=0.0`	Transverse electric field dependence of CLM logarithm factor.
76	`gco=0.0`	Gate tunneling energy adjustment in inversion.
77	`iginv=0.0`	Gate-to-channel current pre-factor (A).
78	`igovinv=0.0`	Gate-to-overlap current pre-factor in inversion (A).
79	`igovinvd=0.0`	Gate-to-overlap current pre-factor in inversion at drain side (A).
80	`igovacc=0.0`	Gate-to-overlap current pre-factor in accumulation (A).
81	`igovaccd=0.0`	Gate-to-overlap current pre-factor in accumulation at drain side (A).
82	`stig=0.0`	Temperature dependence of all gate currents.
83	`gc2ch=0.375`	Gate-to-channel current slope factor.
84	`gc3ch=0.063`	Gate-to-channel current curvature factor.
85	`gc2ov=0.375`	Gate current slope factor in overlaps.
86	`gc3ov=0.063`	Gate current curvature factor in overlaps.
87	`gc2ovinv=0.375`	Gate current slope factor for overlap regions in inversion mode.
88	`gc3ovinv=0.063`	Gate current curvature factor for overlap regions in inversion mode.
89	`gc2ovacc=0.375`	Gate current slope factor for overlap regions in accumulation mode.
90	`gc3ovacc=0.063`	Gate current curvature factor for overlap regions in accumulation mode.
91	`gcdov=0.0`	High drain voltage dependence of overlap gate current (V^-1).
92	`gcvdov=1.0`	Threshold of high drain voltage effect on overlap gate current (V).
93	`chib=3.1`	Tunneling barrier height (V).
94	`niginv=0.0`	Gate tunneling slope adjustment in subthreshold regime.
95	`agidl=0.0`	GIDL pre-factor (A/V^3).
96	`agidld=0.0`	GIDL pre-factor at drain side (A/V^3).

© 2023 Cadence Design Systems, Inc.

97	`bgidl=41.0`	GIDL probability factor at TR (V).
98	`bgidld=41.0`	GIDL probability factor at TR at drain side (V).
99	`stbgidl=0.0`	Temperature dependence of BGIDL (V/K).
100	`stbgidld=0.0`	Temperature dependence of BGIDL at drain side (V/K).
101	`cgidl=0.0`	Substrate bias dependence of GIDL (V^-1).
102	`cgidld=0.0`	Substrate bias dependence of GIDL at drain side (V^-1).
103	`dgidl=0.0`	High longitudinal field parameter of GIDL (V^-1).
104	`dgidld=0.0`	High longitudinal field parameter of GIDL at drain side (V^-1).
105	`areaq=1.0e-12`	Effective channel area for intrinsic CV (m^2).
106	`cgbov=0.0`	Oxide capacitance for gate-substrate overlap (F).
107	`nsdac=1.0e22`	Source/Drain effective doping level for AC model (cm^-3).
108	`fif=0.0`	Inner fringe capacitance prefactor.
109	`fsceac=0.0`	Short channel effect adjustment factor for charge model.
110	`cov=0.0`	Overlap capacitance per side (F).
111	`covd=0.0`	Overlap capacitance at drain side (F).
112	`covdl=0.0`	Overlap capacitance modulation coefficient due to Leff variation.
113	`covdlb=0.0`	Overlap capacitance modulation with back bias.
114	`dvfbov=0.0`	Overlap capacitance flat-band voltage adjustment (V).
115	`cfr=0.0`	Outer fringe capacitance per side (F).
116	`cfrd=0.0`	Outer fringe capacitance at drain side (F).
117	`csd=0.0`	Drain-source capacitance (F).
118	`csdbp=0.0`	Drain/source to substrate perimeter capacitance (F/m).
119	`rth=1.0e4`	Thermal resistance (K/W).
120	`strth=0.0`	Temperature dependence of RTH.
121	`cth=1.0e-11`	Thermal capacitance (J/K).

© 2023 Cadence Design Systems, Inc.

122	`fnt=1.0`	Thermal noise coefficient.
123	`nfa=8.0e+22`	First coefficient of flicker noise (V^-1/m^4).
124	`nfb=3.0e+07`	Second coefficient of flicker noise (V^-1/m^2).
125	`nfc=0.0`	Third coefficient of flicker noise (V^-1).
126	`nfe=0.0`	Flicker noise front transverse field effect coefficient.
127	`nfeb=0.0`	Flicker noise back transverse field effect coefficient.
128	`ef=1.0`	Frequency coefficient of flicker noise.
129	`lvaro=0.0`	Geometry-independent difference between physical and drawn gate lengths (m).
130	`lvarl=0.0`	Length dependence of LPS.
131	`lvarw=0.0`	Width dependence of LPS.
132	`lap=0.0`	Effective channel length reduction per side (m).
133	`wvaro=0.0`	Geometry-independent difference between physical and drawn field-oxide opening (m).
134	`wvarl=0.0`	Length dependence of WOD.
135	`wvarw=0.0`	Width dependence of WOD.
136	`wot=0.0`	Effective reduction of channel width per side (m).
137	`dlq=0.0`	Effective channel length additional offset for charge model (m).
138	`dwq=0.0`	Effective channel width additional offset for charge model (m).
139	`toxeo=2.0e-9`	Front gate equivalent oxide thickness (m).
140	`tsio=1.0e-8`	Silicon or SiGe film thickness (m).
141	`xgeo=0.0`	Fraction of Ge content in the channel.
142	`tboxo=1.0e-7`	Buried oxide thickness (m).
143	`ncho=0.0`	Thin film doping (n-type=negative value, p-type=positive value) (cm^-3).
144	`nsubo=3.0e18`	Substrate doping (n-type=negative value, p-type=positive value) (cm^-3).
145	`cto=0.0`	Interface states factor.
146	`toxpo=2.0e-09`	Front gate physical oxide thickness (m).

© 2023 Cadence Design Systems, Inc.

147	`novo=1.0e20`	Effective doping of overlap-ldd regions (no doping effect=0) (cm^-3).
148	`novdo=1.0e20`	Effective doping of overlap-ldd regions at drain side (cm^-3).
149	`vfbo=0.0`	Geometry-independent front gate flat-band voltage at TR (V).
150	`vfbl=0.0`	Length dependence of VFB (V).
151	`vfblexp=2.0`	Exponent describing length dependence of VFB.
152	`vfbl2=0.0`	Second order length dependence of VFB.
153	`vfblexp2=2.0`	Exponent of second order length dependence of VFB.
154	`vfbw=0.0`	Width dependence of VFB (V).
155	`vfblw=0.0`	Area dependence of VFB.
156	`vfbbo=0.0`	Geometry-independent back gate flat-band voltage at TR (V).
157	`vfblbo=1.0`	Roll-off back to front interface asymmetry factor.
158	`stvfbo=0.0`	Geometry-independent temperature dependence of VFB and VFBB (V/K).
159	`stvfbl=0.0`	Length dependence of STVFB.
160	`stvfbw=0.0`	Width dependence of STVFB.
161	`stvfblw=0.0`	Area dependence of STVFB.
162	`cicfo=1.0`	Long channel front interface coupling coefficient.
163	`cico=1.0`	Long channel back interface coupling coefficient.
164	`pscel=0.0`	Length dependence of PSCE.
165	`pscelexp=2.0`	Exponent describing length dependence of PSCE.
166	`pscew=0.0`	Width dependence of PSCE.
167	`pscebo=1.0`	Short channel back to front interface asymmetry factor.
168	`pscedll=0.0`	Short channel modulation coefficient due to Leff variation.
169	`pscedlw=0.0`	Width dependence of PSCEDL.
170	`nsddco=1.0e22`	Source/Drain effective doping level for DC model (cm^-3).

© 2023 Cadence Design Systems, Inc.

171	`pscedlbo=0.0`	Back bias dependence of short channel effect modulation.
172	`pncew=0.0`	Narrow channel effect on body factor for a width of WEN.
173	`cfl=0.0`	Length dependence of DIBL parameter.
174	`cflexp=2.0`	Exponent for length dependence of CF.
175	`cfw=0.0`	Width dependence of CF.
176	`cfbo=1.0`	DIBL back-to-front interface asymmetry factor.
177	`stcfo=0.0`	Temperature dependence of CF.
178	`stcfl=0.0`	Temperature dependence of CF, with same scaling as CF.
179	`cfdo=0.2`	Drain voltage dependence parameter of DIBL (V).
180	`cfdll=0.0`	DIBL modulation coefficient due to Leff variation.
181	`cfdlw=0.0`	Width dependence of CFDL.
182	`cfdlbo=0.0`	Back bias dependence of DIBL modulation.
183	`uo=5.0e-2`	Front channel zero-field mobility at TR (m^2/V/s).
184	`fbet1=0.0`	First length dependence modulation of BETN.
185	`fbet1w=0.0`	Width dependence of FBET1.
186	`lp1=1.0e-8`	First characteristic length of BETN scaling (m).
187	`lp1w=0.0`	Width dependence of LP1.
188	`fbet2=0.0`	Second length dependence modulation of BETN.
189	`lp2=1.0e-8`	Second characteristic length of BETN scaling (m).
190	`betw1=0.0`	First width dependence modulation of BETN.
191	`betw2=0.0`	Second width dependence modulation of BETN.
192	`wbet=1.0e-8`	Characteristic width of BETN scaling (m).
193	`betnl=0.0`	Second order length dependence of BETN.
194	`betnlexp=1.0`	Exponent for the second order length dependence of BETN.
195	`betnw=0.0`	Second order width dependence of BETN.

© 2023 Cadence Design Systems, Inc.

196	`betnbo=1.0`	Back channel over front channel zero-field mobility ratio.
197	`stbeto=1.5`	Geometry-independent temperature dependence of BETN.
198	`stbetl=0.0`	Length dependence of STBET.
199	`stbetw=0.0`	Width dependence of STBET.
200	`stbetlw=0.0`	Area dependence of STBET.
201	`cso=0.0`	Remote Coulomb scattering parameter at TR.
202	`csl=0.0`	Length dependence of CS.
203	`cslexp=1.0`	Exponent describing length dependence of CS.
204	`csw=0.0`	Width dependence of CS.
205	`cslw=0.0`	Area dependence of CS.
206	`csfio=0.0`	Field dependence of Coulomb scattering at front interface.
207	`csbio=0.0`	Field dependence of Coulomb scattering at back interface.
208	`stcso=0.0`	Temperature dependence of CS.
209	`stcsl=0.0`	Length dependence of STCS.
210	`stcsw=0.0`	Width dependence of STCS.
211	`stcslw=0.0`	Area dependence of STCS.
212	`thecso=1.5`	Remote Coulomb scattering exponent at TR.
213	`stthecso=0.0`	Temperature dependence of THECS.
214	`csthro=2.0`	Remote Coulomb scattering threshold level.
215	`csthrbo=1.0`	Remote Coulomb scattering threshold asymmetry parameter.
216	`mueo=0.0`	Front channel mobility reduction coefficient at TR (cm/MV).
217	`stmueo=0.0`	Temperature dependence of MUE.
218	`themuo=1.5`	Front channel mobility reduction exponent at TR.
219	`stthemuo=0.0`	Temperature dependence of THEMU.

© 2023 Cadence Design Systems, Inc.

220	`xcoro=0.0`	Geometry-independent part of non-universality factor (V^-1).
221	`xcorl=0.0`	Length dependence of XCOR.
222	`xcorlexp=1.0`	Exponent describing length dependence of XCOR.
223	`xcorw=0.0`	Width dependence of XCOR.
224	`xcorlw=0.0`	Area dependence of XCOR.
225	`xcorbo=1.0`	Asymmetry term of non-universality factor.
226	`stxcoro=0.0`	Temperature dependence of XCOR.
227	`fetao=1.0`	Effective field parameter.
228	`rsw1=30.0`	Source/Drain series resistance for channel width WEN at TR (Ohm).
229	`rsw2=0.0`	Higher-order width scaling of source/drain series resistance.
230	`rsigo=0.0`	Source/Drain extension resistance coefficient.
231	`strso=0.0`	Temperature dependence of RS.
232	`rsgo=0.0`	Transverse electric field dependence of RS.
233	`thersgo=2.0`	Transverse electric field dependence exponent of RS.
234	`rsbo=0.0`	Back bias dependence of RS.
235	`thesato=0.0`	Geometry-independent velocity saturation parameter at TR (V^-1).
236	`thesatl=0.0`	Length dependence of THESAT (s/m^2).
237	`thesatlexp=1.0`	Exponent for length dependence of THESAT.
238	`thesatw=0.0`	Width dependence of THESAT.
239	`thesatlw=0.0`	Area dependence of THESAT.
240	`stthesato=(-0.1)`	Geometry-independent temperature dependence of THESAT.
241	`stthesatl=0.0`	Length dependence of STTHESAT.
242	`stthesatw=0.0`	Width dependence of STTHESAT.
243	`stthesatlw=0.0`	Area dependence of STTHESAT.
244	`thesatgo=0.0`	Front gate bias dependence of velocity saturation.

© 2023 Cadence Design Systems, Inc.

245	`thesatbo=0.0`	Back gate bias dependence of velocity saturation.
246	`axo=8.0`	Geometry-independent linear/saturation transition exponent.
247	`axl=0.0`	Length dependence of AX.
248	`axlexp=1.0`	Exponent for length dependence of AX.
249	`alpl1=0.0`	Length dependence of CLM pre-factor ALP.
250	`alplexp=1.0`	Exponent for length dependence of ALP.
251	`alpl2=0.0`	Second order length dependence of ALP.
252	`alplexp2=2.0`	Exponent for second order length dependence of ALP.
253	`alpw=0.0`	Width dependence of ALP.
254	`alp1l1=0.0`	Length dependence of CLM enhancement factor above threshold ALP1 (V).
255	`alp1lexp=0.5`	Exponent for length dependence of ALP1.
256	`alp1l2=0.0`	Second order length dependence of ALP1.
257	`alp1lexp2=1.5`	Exponent for second order length dependence of ALP1.
258	`alp1w=0.0`	Width dependence of ALP1.
259	`alpbo=0.0`	Back bias dependence of channel length modulation.
260	`vpo=0.05`	CLM logarithm dependence factor (V).
261	`vpgo=0.0`	Transverse electric field dependence of CLM logarithm factor.
262	`gcoo=0.0`	Gate tunneling energy adjustment in inversion.
263	`iginvlw=0.0`	Gate to channel current pre-factor for a channel area of WEN.LEN (A).
264	`igovinvw=0.0`	Gate-to-overlap current pre-factor for a width of WEN in inversion (A).
265	`igovinvdw=0.0`	Gate-to-overlap current pre-factor for a width of WEN in inversion at drain side (A).
266	`igovaccw=0.0`	Gate-to-overlap current pre-factor for a width of WEN in accumulation (A).
267	`igovaccdw=0.0`	Gate-to-overlap current pre-factor for a width of WEN in accumulation at drain side (A).

© 2023 Cadence Design Systems, Inc.

268	`stigo=0.0`	Temperature dependence of all gate currents.
269	`gc2cho=0.375`	Gate-to-channel current slope factor.
270	`gc3cho=0.063`	Gate-to-channel current curvature factor.
271	`gc2ovo=0.375`	Gate current slope factor in overlaps.
272	`gc3ovo=0.063`	Gate current curvature factor in overlaps.
273	`gc2ovinvo=0.375`	Gate current slope factor for overlap regions in inversion mode.
274	`gc3ovinvo=0.063`	Gate current curvature factor for overlap regions in inversion mode.
275	`gc2ovacco=0.375`	Gate current slope factor for overlap regions in accumulation mode.
276	`gc3ovacco=0.063`	Gate current curvature factor for overlap regions in accumulation mode.
277	`gcdovl=0.0`	High drain voltage dependence of overlap gate current (V^-1).
278	`gcvdovo=1.0`	Threshold of high drain voltage effect on overlap gate current (V).
279	`chibo=3.1`	Tunneling barrier height (V).
280	`niginvo=0.0`	Gate tunneling slope adjustment in subthreshold regime.
281	`agidlw=0.0`	GIDL pre-factor for a width of WEN (A/V^3).
282	`agidldw=0.0`	GIDL pre-factor for a width of WEN at drain side (A/V^3).
283	`bgidlo=41.0`	GIDL probability factor at TR (V).
284	`bgidldo=41.0`	GIDL probability factor at TR at drain side (V).
285	`stbgidlo=0.0`	Temperature dependence of BGIDL (V/K).
286	`stbgidldo=0.0`	Temperature dependence of BGIDL at drain side (V/K).
287	`cgidlo=0.0`	Substrate bias dependence of GIDL (V^-1).
288	`cgidldo=0.0`	Substrate bias dependence of GIDL at drain side (V^-1).
289	`dgidll=0.0`	High longitudinal field parameter of GIDL (V^-1).

© 2023 Cadence Design Systems, Inc.

290	`dgidldl=0.0`	High longitudinal field parameter of GIDL at drain side (V^-1).
291	`cgbovo=0.0`	Geometry-independent gate-substrate overlap capacitance part (F).
292	`cgbovl=0.0`	Gate-substrate overlap capacitance for a length of LEN (F).
293	`nsdaco=1.0e22`	Source/Drain effective doping level for AC model (cm^-3).
294	`fifw=0.0`	Inner fringe capacitance prefactor for a width of WEN.
295	`fsceaco=0.0`	Short channel effect adjustment factor for charge model.
296	`lovo=0.0`	Overlap length for gate/source-drain hdd overlap capacitance (m).
297	`lovdo=0.0`	Overlap length for gate/drain hdd overlap capacitance (m).
298	`covdlo=0.0`	Overlap capacitance modulation coefficient due to Leff variation.
299	`covdlbo=0.0`	Overlap capacitance modulation with back bias.
300	`covdlw=0.0`	Width dependence of COVDL.
301	`dvfbovo=0.0`	Overlap capacitance flat-band voltage adjustment (V).
302	`cfro=0.0`	Corner related outer fringe capacitance (F).
303	`cfrdo=0.0`	Corner related outer fringe capacitance at drain side (F).
304	`cfrw=0.0`	Outer fringe capacitance per side for a width of WEN (F).
305	`cfrdw=0.0`	Outer fringe capacitance per side for a width of WEN at drain side (F).
306	`csdo=1.0`	Drain-source capacitance correction factor.
307	`csdbpo=0.0`	Drain/source to substrate perimeter capacitance (F/m).
308	`rtho=1.0e5`	Geometry-independent thermal resistance (K/W).
309	`rthl=0.0`	Length dependence of RTH.
310	`rthw=0.0`	Width dependence of RTH.

© 2023 Cadence Design Systems, Inc.

311	`rthlw=9.0`	Area dependence of RTH.
312	`strtho=0.0`	Temperature dependence of RTH.
313	`ctho=1.0e-12`	Geometry-independent thermal capacitance (J/K).
314	`lambtho=1.0e-7`	Characteristic length of lateral thermal coupling for multifinger devices (m).
315	`ftho=0.0`	First neighbour thermal coupling factor for multifinger devices.
316	`fnto=1.0`	Thermal noise coefficient.
317	`nfalw=8.0e22`	First coefficient of flicker noise (V^-1/m^4).
318	`nfblw=3.0e7`	Second coefficient of flicker noise (V^-1/m^2).
319	`nfclw=0.0`	Third coefficient of flicker noise (V^-1).
320	`nfeo=0.0`	Flicker noise front transverse field effect coefficient.
321	`nfebo=0.0`	Flicker noise back transverse field effect coefficient.
322	`efo=1.0`	Frequency coefficient of flicker noise.
323	`swstress=1.0`	Stress model selection flag (1= Previous STI stress model, 2= New channel stress model).
324	`saref=1.0e-6`	Reference distance between OD-edge and poly from one side (m).
325	`sbref=1.0e-6`	Reference distance between OD-edge and poly from other side (m).
326	`wlod=0.0`	Width parameter (m).
327	`kuo=0.0`	Mobility degradation/enhancement coefficient (m).
328	`kvsat=0.0`	Saturation velocity degradation/enhancement coefficient.
329	`tkuo=0.0`	Temperature dependence of KUO.
330	`lkuo=0.0`	Length dependence of KUO (m^LLODKUO).
331	`wkuo=0.0`	Width dependence of KUO (m^WLODKUO).
332	`pkuo=0.0`	Cross-term dependence of KUO (m^(LLODKUO+WLODKUO)).
333	`llodkuo=0.0`	Length parameter for UO stress effect.
334	`wlodkuo=0.0`	Width parameter for UO stress effect.

© 2023 Cadence Design Systems, Inc.

335	`kvtho=0.0`	Threshold shift parameter (Vm).
336	`lkvtho=0.0`	Length dependence of KVTHO (m^LLODVTH).
337	`wkvtho=0.0`	Width dependence of KVTHO (m^WLODVTH).
338	`pkvtho=0.0`	Cross-term dependence of KVTHO (m^(LLODVTH+WLODVTH)).
339	`llodvth=0.0`	Length parameter for VTH-stress effect.
340	`wlodvth=0.0`	Width parameter for VTH-stress effect.
341	`stetao=0.0`	Eta0 shift factor related to VTHO change (m).
342	`lodetao=1.0`	Eta0 shift modification factor for stress effect.
343	`strlambda=1.0e-7`	Relaxation characteristic length (m).
344	`stralpha=3.0`	Asymmetry parameter.
345	`strdvfbo=0.0`	Threshold shift parameter (V).
346	`strwdvfbo=0.0`	Width dependence of threshold shift parameter.
347	`strdcfl=0.0`	DIBL variation parameter.
348	`strruo=0.0`	Mobility degradation/enhancement coefficient.
349	`strtruo=0.0`	Temperature dependence of mobility degradation/ enhancement coefficient.
350	`strrvsat=0.0`	Saturation velocity degradation/enhancement coefficient.
351	`vthmod`	Vth output selector. 'std' outputs model equation Vth. `vthcc` outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter `vthmod`. Possible values are `std` and `vthcc`.
352	`ivth (A)`	Vth current parameter. The default value is taken from the options parameter `ivthn` or `ivthp`, depending on the type of the model.
353	`ivthw (m)`	Width offset for constant current Vth. The default value is taken from the options parameter `ivthw`.
354	`ivthl (m)`	Length offset for constant current Vth. The default value is taken from the options parameter `ivthl`.

© 2023 Cadence Design Systems, Inc.

355	`ivth_vdsmin (V)`	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter `ivth_vdsmin`.
356	`fntexc=0.0`	Excess noise coefficient.
357	`axl2=0.0`	Second order length dependence of AX.
358	`axlexp2=1.5`	Exponent for second order length dependence of AX.
359	`agidlo=0.0`	GIDL geometry-independent pre-factor (A/V^3).
360	`agidldo=0.0`	GIDL geometry-independent pre-factor at drain side (A/V^3).
361	`dgidlo=0.0`	High field geometry-independent parameter of GIDL (V^-1).
362	`dgidldo=0.0`	High field geometry-independent parameter of GIDL at drain side (V^-1).
363	`fntexcl=0.0`	Length dependence coefficient of excess noise.
364	`fntexclexp=2.0`	Length dependence exponent of excess noise.
365	`l=(30 1.0e-9)`	Designed Gate Length.
366	`nf=1`	Number of fins per finger.
367	`lmin=0.0 m`	Minimum channel length for which the model is valid.
368	`lmax=1.0 m`	Maximum channel length for which the model is valid.
369	`wmin=0.0 m`	Minimum channel width for which the model is valid.
370	`wmax=1.0 m`	Maximum channel width for which the model is valid.

Output Parameters

1	`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

1	`typeop`	MOSFET type.
2	`vth (V)`	Threshold voltage including back bias and drain bias effects.

© 2023 Cadence Design Systems, Inc.

3	`vds (V)`	Drain-Source DC voltage.
4	`vsb (V)`	Source-Bulk DC voltage.
5	`vdb (V)`	Drain-Bulk DC voltage.
6	`vgs (V)`	Gate-Source DC voltage.
7	`vgd (V)`	Gate-Drain DC voltage.
8	`vth_drive (V)`	Effective gate drive voltage including back bias and drain bias effects.
9	`vdsat (V)`	Drain saturation voltage.
10	`vdsat_marg (V)`	Saturation limit.
11	`ids (I)`	DC Channel current (excluding tunnel, GISL and GIDL currents).
12	`id (I)`	Total DC drain current.
13	`ig (I)`	Total DC gate current.
14	`is (I)`	Total DC source current.
15	`ib (I)`	Total DC bulk current.
16	`igidl (I)`	DC GIDL current.
17	`igisl (I)`	DC GISL current.
18	`igs (I)`	DC gate-source leakage current.
19	`igd (I)`	DC gate-drain leakage current.
20	`idb (I)`	DC drain-bulk current.
21	`isb (I)`	DC source-bulk current.
22	`gm`	DC transconductance.
23	`gmb`	DC bulk transconductance.
24	`go`	DC output conductance.
25	`gds`	DC output conductance.
26	`cdd (C)`	Drain capacitance.
27	`cdg (C)`	Drain to gate transcapacitance.
28	`cdb (C)`	Drain to bulk transcapacitance.
29	`cds (C)`	Drain to source transcapacitance.

© 2023 Cadence Design Systems, Inc.

30	cgd (C)	Gate to drain transcapacitance.
31	cgg (C)	Gate capacitance.
32	cgb (C)	Gate to bulk transcapacitance.
33	cgs (C)	Gate to source transcapacitance.
34	cbd (C)	Bulk to drain transcapacitance.
35	cbg (C)	Bulk to gate transcapacitance.
36	cbb (C)	Bulk capacitance.
37	cbs (C)	Bulk to source transcapacitance.
38	csd (C)	Source to drain transcapacitance.
39	csg (C)	Source to gate transcapacitance.
40	csb (C)	Source to bulk transcapacitance.
41	css (C)	Source capacitance.
42	co (C)	Output Drain-Source capacitance.
43	cm (C)	Capacitance element 1 for QS model.
44	cmb (C)	Capacitance element 2 for QS model.
45	cmx (C)	Capacitance element 3 for QS model.
46	tau1 (s)	Time constant related to NQS first frequency pole.
47	fqslim (Hz)	QS model frequency limit.
48	tk	MOSFET device temperature.
49	dtsh	Channel temperature elevation due to self-heating.
50	self_gain	Self gain.
51	rout (R)	Output resistance.
52	vearly (V)	Equivalent early voltage.
53	beff	Gain factor.
54	ft	Unity gain frequency.
55	rgate (R)	Gate resistance.
56	gmoveri	Gm over Id.
57	gmoverid	Gm over Id.
58	pwr (W)	Power dissipation.

© 2023 Cadence Design Systems, Inc.

59	region	Estimated operating region. Spectre outputs a number (0-4) in a raw file. Possible values are off, triode, sat, subth, and breakdown.
60	opdef	1: Device Physics notation. 2: Circuit Simulator notation.
61	ctype	Flag for channel type of MOSFET. 1: NMOS. -1: PMOS.
62	sdop	Operation mode related to channel type and drain-source voltage sign. Possible values are Forward and Reverse.
63	sdint	Flag for source drain interchange. 1: No S-D interchange, -1: S-D interchange.
64	cjd (C)	Total drain-bulk junction capacitance, including bottom and sidewall regions.
65	cjs (C)	Total source-bulk junction capacitance, including bottom and sidewall regions.
66	vth0 (V)	Zero-bias threshold voltage, excluding back-bias (body effect) and drain-bias effect (DIBL).

Parameter Index

In the following index, I refers to instance parameters, M refers to the model parameters section, O refers to the output parameters section, and OP refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of M-35 means the 35th model parameter.

adrain I-4
csthr M-50
m I-12
stthecs M-49
agidl M-95
csthrb M-51
meff O-1
stthecso M-213
agidld M-96
csthrbo M-215
mue M-52
stthemu M-55
agidldw M-282
csthro M-214
mueo M-216
stthemuo M-219
agidlw M-281
csw M-204
mult I-11
stthesat M-67

© 2023 Cadence Design Systems, Inc.

alp M-71
alp1 M-72
alp1l1 M-254
alp1l2 M-256
alp1lexp M-255
alp1lexp2 M-257
alp1w M-258
alpb M-73
alpbo M-259
alpl1 M-249
alpl2 M-251
alplexp M-250
alplexp2 M-252
alpw M-253
areaq M-105
asource I-3
ax M-70
axl M-247
axlexp M-248
axo M-246
ct M-20
cth M-121
ctho M-313
cto M-145
delvto I-13
dgidl M-103
dgidld M-104
dgidldl M-290
dgidll M-289
dlq M-137
dtsh OP-40
dvfbov M-114
dvfbovo M-301
dwq M-138
ef M-128
efo M-322
factuo I-14
fbet1 M-184
fbet1w M-185
fbet2 M-188
nch M-18
ncho M-143
nf I-10
nfa M-123
nfalw M-317
nfb M-124
nfblw M-318
nfc M-125
nfclw M-319
nfe M-126
nfeb M-127
nfebo M-321
nfeo M-320
niginv M-94
niginvo M-280
nov M-22
novd M-23
novdo M-148
novo M-147
nsdac M-107
stthesatl M-241
stthesatlw M-243
stthesato M-240
stthesatw M-242
stvfb M-26
stvfbl M-159
stvfblw M-161
stvfbo M-158
stvfbw M-160
stxcor M-58
stxcoro M-226
swclipchk M-3
swgidl M-6
swigate M-5
swign M-8
swjunasym M-9
swscale M-1
swshe M-7
swstress M-323
swsubdep M-4

© 2023 Cadence Design Systems, Inc.

beff OP-44
betn M-41
betnb M-42
betnbo M-196
betnl M-193
betnlexp M-194
betnw M-195
betw1 M-190
betw2 M-191
bgidl M-97
bgidld M-98
bgidldo M-284
bgidlo M-283
cbb OP-33
cbd OP-31
cbg OP-32
cbs OP-34
cdb OP-25
cdd OP-23
cdg OP-24
feta M-59
fetao M-227
fif M-108
fifw M-294
fnt M-122
fnto M-316
fsceac M-109
fsceaco M-295
ft OP-45
ftho M-315
gc2ch M-83
gc2cho M-269
gc2ov M-85
gc2ovacc M-89
gc2ovacco M-275
gc2ovinv M-87
gc2ovinvo M-273
gc2ovo M-271
gc3ch M-84
gc3cho M-270
nsdaco M-293
nsddc M-32
nsddco M-170
nsub M-19
nsubo M-144
pdrain I-6
pkuo M-332
pkvtho M-338
pnce M-34
pncew M-172
psce M-29
psceb M-30
pscebo M-167
pscedl M-31
pscedlb M-33
pscedlbo M-171
pscedll M-168
pscedlw M-169
pscel M-164
pscelexp M-165
tbox M-17
tboxo M-142
thecs M-48
thecso M-212
themu M-54
themuo M-218
thersg M-64
thersgo M-233
thesat M-66
thesatb M-69
thesatbo M-245
thesatg M-68
thesatgo M-244
thesatl M-236
thesatlexp M-237
thesatlw M-239
thesato M-235
thesatw M-238
tk OP-39
tkuo M-329

© 2023 Cadence Design Systems, Inc.

cds OP-26
cf M-35
cfb M-36
cfbo M-176
cfd M-38
cfdl M-39
cfdlb M-40
cfdlbo M-182
cfdll M-180
cfdlw M-181
cfdo M-179
cfl M-173
cflexp M-174
cfr M-115
cfrd M-116
cfrdo M-303
cfrdw M-305
cfro M-302
cfrw M-304
cfw M-175
gc3ov M-86
gc3ovacc M-90
gc3ovacco M-276
gc3ovinv M-88
gc3ovinvo M-274
gc3ovo M-272
gcdov M-91
gcdovl M-277
gco M-76
gcoo M-262
gcvdov M-92
gcvdovo M-278
gds OP-22
gm OP-20
gmb OP-21
gmoverid OP-47
ib OP-13
id OP-10
idb OP-18
ids OP-9
pscew M-166
psource I-5
pwr OP-48
qmc M-10
region OP-49
rgate OP-46
rout OP-42
rs M-60
rsb M-65
rsbo M-234
rsg M-63
rsgo M-232
rsig M-61
rsigo M-230
rsw1 M-228
rsw2 M-229
rth M-119
rthl M-309
rthlw M-311
rtho M-308
tmax M-13
toxe M-14
toxeo M-139
toxp M-21
toxpo M-146
tr M-12
trise I-15
tsi M-15
tsio M-140
type M-11
typeop OP-1
uo M-183
vds OP-3
vdsat OP-7
vdsat_marg OP-8
vearly OP-43
version M-2
vfb M-24
vfbb M-25
vfbbo M-156

© 2023 Cadence Design Systems, Inc.

cgb OP-29
cgbov M-106
cgbovl M-292
cgbovo M-291
cgd OP-27
cgg OP-28
cgidl M-101
cgidld M-102
cgidldo M-288
cgidlo M-287
cgs OP-30
chib M-93
chibo M-279
cic M-28
cicf M-27
cicfo M-162
cico M-163
cov M-110
covd M-111
covdl M-112
ig OP-11
igd OP-17
igidl OP-14
iginv M-77
iginvlw M-263
igisl OP-15
igovacc M-80
igovaccd M-81
igovaccdw M-267
igovaccw M-266
igovinv M-78
igovinvd M-79
igovinvdw M-265
igovinvw M-264
igs OP-16
is OP-12
isb OP-19
isnoisy I-16
ivth M-352
ivth_vdsmin M-355
rthw M-310
sa I-7
saref M-324
sb I-8
sbref M-325
sd I-9
self_gain OP-41
stbet M-43
stbetl M-198
stbetlw M-200
stbeto M-197
stbetw M-199
stbgidl M-99
stbgidld M-100
stbgidldo M-286
stbgidlo M-285
stcf M-37
stcfl M-178
stcfo M-177
stcs M-47
vfbl M-150
vfbl2 M-152
vfblbo M-157
vfblexp M-151
vfblexp2 M-153
vfblw M-155
vfbo M-149
vfbw M-154
vgs OP-5
vp M-74
vpg M-75
vpgo M-261
vpo M-260
vsb OP-4
vth OP-2
vth_drive OP-6
vthmod M-351
w I-2
wbet M-192
wkuo M-331

© 2023 Cadence Design Systems, Inc.

covdlb M-113
covdlbo M-299
covdlo M-298
covdlw M-300
cs M-44
csb OP-37
csbi M-46
csbio M-207
csd M-117
csd OP-35
csdbp M-118
csdbpo M-307
csdo M-306
csfi M-45
csfio M-206
csg OP-36
csl M-202
cslexp M-203
cslw M-205
cso M-201
ivthl M-354
ivthw M-353
kuo M-327
kvsat M-328
kvtho M-335
l I-1
lambtho M-314
lap M-132
lkuo M-330
lkvtho M-336
llodkuo M-333
llodvth M-339
lodetao M-342
lovdo M-297
lovo M-296
lp1 M-186
lp1w M-187
lp2 M-189
lvarl M-130
lvaro M-129
stcsl M-209
stcslw M-211
stcso M-208
stcsw M-210
stetao M-341
stig M-82
stigo M-268
stmue M-53
stmueo M-217
stralpha M-344
strdcfl M-347
strdvfbo M-345
strlambda M-343
strruo M-348
strrvsat M-350
strs M-62
strso M-231
strth M-120
strtho M-312
strtruo M-349
wkvtho M-337
wlod M-326
wlodkuo M-334
wlodvth M-340
wot M-136
wvarl M-134
wvaro M-133
wvarw M-135
xcor M-56
xcorb M-57
xcorbo M-225
xcorl M-221
xcorlexp M-222
xcorlw M-224
xcoro M-220
xcorw M-223
xge M-16
xgeo M-141

© 2023 Cadence Design Systems, Inc.

css OP-38 lvarw M-131 strwdvfbo M-346

© 2023 Cadence Design Systems, Inc.

53

ASM-HEMT Model

This chapter contains the following information about the ASM-HEMT model:

- Model Overview
- Model Equations
  - Physical Constants
  - Voltages Calculation and Pre Conditioning
  - Temperature Dependence
  - Surface Potential Calculation
  - Intrinsic Charge Calculation
  - Drain Current Model
  - Self Heating Model
  - Short Channel Effects
  - Access Region and Parasitic Resistances
  - Parasitic Capacitances
  - Trap Model
  - Gate Current Model
  - Field Plate Model
  - Noise Model
- Component Statements

© 2023 Cadence Design Systems, Inc.

Model Overview

Advanced SPICE model for GaN HEMTs, ASM-GaN-HEMT is a physics-based model for these devices. The model can be structured into following three parts:

- Core channel-charge or surface-potential calculations
- Core terminal current and charge model, and
- Models for real device effects in the device.

Model Equations

Physical Constants

Physical quantities in ASM-HEMT are in S.I. units unless specified otherwise.

$$q = 1.6 \times 10^{19}$$

$$\varepsilon_{AlGaN} = 10.66 \times 10^{-11}$$

$$K_B = 8.636 \times 10^{-5} eV/\mathrm{K}$$

$$\Upsilon 0 = 2.12 \times 10^{-12}$$

$$\Upsilon 1 = 3.73 \times 10^{-12}$$

$$DOS = 3.24 \times 10^{17}$$

Smoothing constant,

$$ep_{psi} = 0.3$$

© 2023 Cadence Design Systems, Inc.

Voltages Calculation and Pre Conditioning

Voltages Calculation

Voltages Calculation

$$V_{ds} = V_d - V_s \tag{3.2.1}$$

$$V_{gs} = V_g - V_s \tag{3.2.2}$$

$$V_{gd} = V_g - V_d \tag{3.2.3}$$

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.01} \tag{3.2.4}$$

$$V_{off,DIBL} = VOFF - (ETA0 - TRAPETA0 \cdot vcap + eta0_{trap}) \cdot \left(\frac{V_{dsx} \cdot VDSCALE}{\sqrt{V_{dsx}^2 + VDSCALE^2}} \right) \tag{3.2.5}$$

$$V_{gs,min} = V_{off,DIBL}(T) + V_{tv} ln\left(L/(2Wq \cdot DOS \cdot V_{tv}^2)\right) \tag{3.2.6}$$

$$V_{gs,eff} = \frac{1}{2}((V_{gs} - V_{gs,min}) + \sqrt{(V_{gs} - V_{gs,min})^2 + 0.0001}) \tag{3.2.7}$$

$$V_{g0} = V_{gs,eff} - V_{off,DIBL} \tag{3.2.8}$$

$$V_{g0,eff} = \frac{1}{2}\left(V_{g0} + \sqrt{V_{g0}^2 + 4ep_{psi^2}}\right) \tag{3.2.9}$$

© 2023 Cadence Design Systems, Inc.

$$V_{dsat} = \frac{(2VSAT(T)/\mu_{eff})L \cdot V_{g0,eff}}{(2VSAT(T)/\mu_{eff})L + V_{g0,eff}} \tag{3.2.10}$$

$$V_{d,eff} = V_{ds}\left(1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{DELTA}\right)^{\frac{-1}{DELTA}} \tag{3.2.11}$$

$$V_{gd0} = V_{g0} - V_{d,eff} \tag{3.2.12}$$

$$V_{gd,eff} = \frac{1}{2}\left(V_{gd0} + \sqrt{V_{gd0}^2 + 4ep_{psi}^2}\right) \tag{3.2.13}$$

Bias Independent Calculations

$$C_g = \frac{\epsilon_{AlGaN}}{TBAR} \tag{3.2.14}$$

$$C_{g,fp} = \frac{\epsilon_{AlGaN}}{DFP} \tag{3.2.15}$$

$$C_{g,sfp} = \frac{\epsilon_{AlGaN}}{DSFP} \tag{3.2.16}$$

$$\beta = \frac{C_g}{q \cdot DOS \cdot K_B \cdot T_{dev}} \tag{3.2.17}$$

$$\alpha_n = \frac{e}{\beta} \tag{3.2.18}$$

$$\alpha_d = \frac{1}{\beta} \tag{3.2.19}$$

© 2023 Cadence Design Systems, Inc.

Temperature Dependence

$$T_{dev} = T + V(rth) \tag{3.3.1}$$

$$cdsc = 1 + NFACTOR + (CDSCD + cdscd_{trap}) \cdot V_{dsx} \tag{3.3.2}$$

$$V_{tv} = KB \cdot T_{dev} cdsc \tag{3.3.3}$$

$$\begin{aligned} V_{off,DIBL}(T) =& V_{off,DIBL} - \left(\frac{T_{dev}}{TNOM} - 1\right) \cdot KT1 \\ &+ TRAPVOFF \cdot vcap + voff_{trap} \end{aligned} \tag{3.3.4}$$

$$U0(T) = U0 \left(\frac{T_{dev}}{TNOM}\right)^{UTE} \tag{3.3.5}$$

$$VSAT(T) = VSAT \left(\frac{T_{dev}}{TNOM}\right)^{AT} \tag{3.3.6}$$

$$\begin{aligned} NS0ACCS(T) =& NS0ACCS \left(1 - KNS0 \left(\frac{T_{dev}}{TNOM} - 1\right)\right) \\ &\cdot (1 + K0ACCS \cdot V_{g0,eff}) \end{aligned} \tag{3.3.7}$$

$$VSATACCS(T) = VSATACCS \left(\frac{T_{dev}}{TNOM}\right)^{ATS} \tag{3.3.8}$$

© 2023 Cadence Design Systems, Inc.

$$U0ACCS(T) = U0ACCS\left(\frac{T_{dev}}{TNOM}\right)^{UTES} \tag{3.3.9}$$

$$NS0ACCD(T) = NS0ACCS\left(1 - KNS0\left(\frac{T_{dev}}{TNOM} - 1\right)\right) \cdot (1 + K0ACCD \cdot V_{g0,eff}) \tag{3.3.10}$$

$$U0ACCD(T) = U0ACCD\left(\frac{T_{dev}}{TNOM}\right)^{UTES} \tag{3.3.11}$$

$$RSC(T) = RSC\left(1 + KRSC\left(\frac{T_{dev}}{TNOM} - 1\right)\right) \tag{3.3.12}$$

$$RDC(T) = RDC\left(1 + KRSC\left(\frac{T_{dev}}{TNOM} - 1\right)\right) \tag{3.3.13}$$

$$VBI(T) = VBI - \left(\frac{T_{dev}}{TNOM} - 1\right) KTVBI \tag{3.3.14}$$

$$CFG(T) = CFG - \left(\frac{T_{dev}}{TNOM} - 1\right) KTCFG \tag{3.3.15}$$

Surface Potential Calculation

Variation of surface potential with terminal gate voltage can be calculated as:

(3.4.1)

$$\psi_x(V_g) = V_f(V_g) + V_x$$

© 2023 Cadence Design Systems, Inc.

where V_f is the potential corresponding to Fermi level in triangular potential well and V_x is the voltage at the point at which surface potential is to be calculated.

V_f Calculation

Assuming the hetero junction as triangular potential well, we can get the position of sub bands by solving the Schrodinger's equation as follows:

(3.4.2)

$$E_n(eV) = \left(\frac{h^2}{2m_1}\right)\left(\frac{3}{2}\pi q\varepsilon\right)^{\frac{2}{3}}\left(n+\frac{2}{3}\right)$$

where $\mathcal{E}$ is electric field across the triangular potential well, n can take values 0,1,2..etc., $m1$ is effective mass of electron in triangular well and h is Planck's constant.

Considering only two lower subbands,

(3.4.3)

$$E_o = k_0\varepsilon^{\frac{2}{3}}$$

(3.4.4)

$$E_1 = k_1\varepsilon^{\frac{2}{3}}$$

By solving the Poisson's equation, we can get the relationship between electric field and sheet charge density,

$$\epsilon\mathcal{E} = qn_s \qquad (3.4.5)$$

Substituting (3.4.5) in (3.4.3) and (3.4.4)

$$E_0 = \gamma_0\mathcal{E}^{\frac{2}{3}} \qquad (3.4.6)$$

$$E_1 = \gamma_1\mathcal{E}^{\frac{2}{3}} \qquad (3.4.7)$$

© 2023 Cadence Design Systems, Inc.

Applying Fermi Dirac statistics,

$$n_s = DOS \int_{E_0}^{E_1} \frac{dE}{1 + e^{\frac{q(E-E_f)}{kT}}} + 2DOS \int_{E_1}^{\infty} \frac{dE}{1 + e^{\frac{q(E-E_f)}{kT}}} \qquad (3.4.8)$$

where DOS is two-dimensional density of states (DOS) in GaN. (It is DOS between E_0 and E_1 and 2DOS for above E_1). By solving the integration,

$$n_s = DOSV_{tv}\left(ln[(1 + e^{(E_f - E_0)/V_{tv}})(1 + e^{(E_f - E_1)/V_{tv}})]\right) \qquad (3.4.9)$$

Assuming AlGaN layer is completely ionized, from charge balance condition, you get,

$$n_s = \frac{\epsilon}{qd}(V_{g0} - V_f) = \frac{C_g}{q}(V_{g0} - V_f) \qquad (3.4.10)$$

$$\text{where } C_g = \frac{\epsilon}{d}$$

and d is taken as process parameter, TBAR.

Solving (3.4.6), (3.4.7), (3.4.9) and (3.4.10) equations for V_f is a difficult task as these equations are transcendental in nature.Variation of sub bands and V_f in the triangular potential well with V_g makes the calculation complicated.[17] Variation of V_f with V_g can be captured by dividing the operating region into three:

- $Sub - V_{off}$ region is where $V_g < V_{off}$

  In this region, $|E_f| >> E_0,\ E_1$ and $V_f \approx V_{g0}$. Applying these conditions to equation(3.4.9),

  $$n_{s,sub-V_{off}} = 2DOSV_{tv}e^{\frac{V_{g0}}{V_{tv}}} \qquad (3.4.11)$$

  Substituting (3.4.10) in (3.4.11):

  $$V_{f,sub-V_{off}} = V_{g0} - \frac{2qDV_{tv}}{C_g}e^{\frac{V_{g0}}{V_{tv}}} \qquad (3.4.12)$$

- $V_g > V_{off}$ and $E_f < E_0$

© 2023 Cadence Design Systems, Inc.

Since E_1 is higher than E_f, neglecting in (3.4.9) and applying `ln(1 +x) = x` for `x < 0`,

$$n_s = DV_{th}e^{\frac{E_f - E_0}{V_{tv}}} \qquad (3.4.13)$$

Using (3.4.3) and (3.4.10) in (3.4.13),

$$V_f^{\mathcal{I}} = V_{g0}\left(\frac{V_{th}ln(\beta V_{g0}) + \gamma_0(\frac{C_g V_{g0}}{q})^{\frac{2}{3}}}{V_{g0} + V_{tv} + \frac{2\gamma_0}{3}(\frac{C_g V_{g0}}{q})^{\frac{2}{3}}}\right) \qquad (3.4.14)$$

where, $e^{\frac{(E_f - E_1)}{V_{tv}}}$

- $V_g > V_{off}$ and $E_f < E_0$

  Since $E_1 >> E_f$, neglecting $e^{\frac{(E_f - E_1)}{V_{tv}}}$ in 3.4.9 and applying $ln(1+x) \approx lnx$ or `x > 0`

$$n_s = D(E_f - E_0) \qquad (3.4.15)$$

Using (3.4.3) and (3.4.10) in (3.4.15),

$$V_f^{\mathcal{II}} = V_{g0}\left(\frac{\beta V_{th}V_{g0} + \gamma_0(\frac{C_g V_{g0}}{q})^{\frac{2}{3}}}{V_{g0}(1+\beta V_{tv}) + \frac{2\gamma_0}{3}(\frac{C_g V_{g0}}{q})^{\frac{2}{3}}}\right) \qquad (3.4.16)$$

Combining V_f equations (3.4.14), (3.4.16) in $V_g > V_{off}$ regions,

$$V_{f,above} = V_{g0}(1 - H(V_{g0})) \qquad (3.4.17)$$

where

$$H(V_{g0}) = \frac{V_{g0} + V_{tv}[1 - ln(\beta V_{gon})] - \frac{\gamma_0}{3}(\frac{C_g V_{g0}}{q})^{\frac{2}{3}}}{V_{g0}(1 + \frac{V_{tv}}{V_{god}}) + \frac{2\gamma_0}{3}(\frac{C_g V_{g0}}{q})^{\frac{2}{3}}} \qquad (3.4.18)$$

© 2023 Cadence Design Systems, Inc.

Here, V_{g0n} and V_{gdn} are functions of V_{g0} given by the interpolation expression,

$$V_{g0x} = \frac{V_{g0}\alpha_x}{\sqrt{V_{g0}^2 + \alpha_x^2}} \qquad (3.4.19)$$

where $\alpha_n = e/\beta$ and $\alpha_d = 1/\beta$

Combining Sub-V_{off} region V_f equation (3.4.12) with $V_g > V_{off}$ region equation (3.4.17)

$$V_{f,unified} = V_{g0} - \frac{2V_{tv}ln(1 + e^{\frac{V_{g0}}{2V_{tv}}})}{\frac{1}{H(V_{g0,eff})} + (\frac{C_g}{qD})e^{-\frac{V_{g0}}{2V_{tv}}}} \qquad (3.4.20)$$

Here $V_{g0,eff}$ is equal to V_{g0} above V_{off} and is on the order of thermal voltage when $V_g < V_{off}$f and $1/V_{g0,p}$ becomes very small and equation(3.4.12) is obtained whereas in $V_g > V_{off}$, equation (3.4.17) is obtained.

But at V_{off}, subbands E_0 and E_1 are close to E_f. E_f -E_0 and E_f -E_1 = E_0. The calculation becomes complicated. So the Householder's numerical calculation method is used to get the accuracy upto femto volts. The final value for E_f is obtained using the iterative re-evaluation as under

$$V_f = V_{f,unified} - \frac{p}{q}\left(1 + \frac{pr}{2q^2}\right) \qquad (3.4.21)$$

Computation of p,q and r can be done as shown above. From 3.4.1, Ψ can be determined at source end by $\Psi = V_f + V_s$. For potential at drain end, V_{g0} and $V_{g0,eff}$ are replaced by V_{gd0} and $V_{gd,\ eff}$ respectively and can be calculated by $\Psi_d = V_f + V_{d,eff}$.

Intrinsic Charge Calculation

Accurate modelling of intrinsic charges require proper assignment of channel charge to the terminals. Q_g can be calculated as,

$$Q_g = -\int_0^L qWn_s(V_g, V_x)dx = -\int_0^L qWC_g(V_g0 - \psi(x))dx \qquad (3.5.1)$$

© 2023 Cadence Design Systems, Inc.

Expression for Quantities

Quantity	Expression
$k_{0,1}$	$\gamma_{0,1}\left(\frac{C_g}{q}\right)^{2/3}$
V_{gef}	$V_g - V_{off} - E_f$
$\xi_{0,1}$	$\exp\left(\frac{E_{f,unified} - k_{0,1}V_{gef}^{2/3}}{V_{th}}\right)$
p	$\frac{C_g}{q}V_{gef} - \sum_{i=0}^{1} DV_{th}\ln(\xi_i + 1)$
q	$-\frac{C_g}{q} - \sum_{i=0}^{1}\frac{D}{1+\xi_i^{-1}}\left(1 + (2/3)k_i V_{gef}^{-1/3}\right)$
r	$\sum_{i=0}^{1}\frac{\frac{2}{9}V_{gef}^{-4/3}Dk_i(1+\xi_i^{-1}) + \frac{D}{V_{th}}\left(1+\frac{2}{3}k_i V_{gef}^{-1/3}\right)^2}{\left(1+\xi_i^{-1}\right)^2}$

By using current continuity equation, that is, equating currents at drain end and at any point in the channel and neglecting the saturation of current we can get,

$$dx = \frac{L(V_g 0 - \psi + V_{tv})}{V_g 0 - \psi_m + V_{th}}(\psi_d - \psi_s) \qquad (3.5.2)$$

By substituting 3.5.2 in 3.5.1 and by integrating the equation with respect to Ψ, we can get,

$$Q_g = \frac{C_g LW}{V_{g0} - \psi_m + V_{tv}}[V_{g0}^2 + \frac{1}{3}(\psi_d^2 + \psi_s^2 + \psi_d\psi_s) - V_{g0}(\psi_d + \psi_s - V_{tv}) - V_{tv}\psi_m] \quad (3.5.3)$$

Ward-Dutton's partitioning method is used to determine the drain and source terminal charges.

$$Q_d = \int_0^L \frac{x}{L}Q_{ch}(V_g, V_x)dx \qquad (3.5.4)$$

$$Q_s = \int_0^L \left(1 - \frac{x}{L}\right)Q_{ch}(V_g, V_x)dx \qquad (3.5.5)$$

$$Q_g = -Q_s - Q_d \qquad (3.5.6)$$

© 2023 Cadence Design Systems, Inc.

By integrating equation (3.5.2) from source to any arbitrary point in the channel, we can get x in terms of Ψ ,

$$x = \frac{L(\psi(x) - \psi_s)}{V_{g0} - \psi_m + V_{tv}} \left(V_{g0} + V_{tv} - \frac{\psi(x) + \psi_s}{2} \right) \tag{3.5.7}$$

Substituting 3.5.7 and 3.5.2 in 3.5.4, you can get,

$$\begin{aligned} Q_d = -\frac{C_g LW}{120(V_{g0} - \psi_m + V_{tv})^2} [12\psi_d^3 + 8\psi_s^3 + \psi_s^2(16\psi_d - 5(V_{tv} + 8V_{g0})) \\ +2\psi_s(12\psi_d^2 - 5\psi_d(5V_{tv} + 8V_{g0}) + 10(V_{tv} + V_{g0})(V_{tv} + 4V_{g0})) \\ +15\psi_d^2(3V_{tv} + 4V_{g0}) - 60V_{g0}(V_{tv} + V_{g0})^2 \\ +20\psi_d(V_{tv} + V_{g0})(2V_{tv} + 5V_{g0})] \end{aligned} \tag{3.5.8}$$

Q_s can be obtained by using $Q_s = -Q_g - Q_d$

Drain Current Model

The drain current at any point x along the channel under the gradual channel approximation with drift diffusion model can be expressed as,

$$I_d = -\mu W Q_{ch} \frac{d\psi}{dx} + \mu W V_{th} \frac{dQ_{ch}}{dx} \tag{3.6.1}$$

Using $Q_{ch} = C_g(V_{g0} - \Psi)$, taking dx to the left side and integrating from 0 to L, we get $I_d L$ and on right side, integrating with respect to d Ψ from source side to the drain side potential, you get current equation as,

$$I_d = \frac{W}{L} \mu C_g (V_g 0 - \psi_m + V_{th}) \psi_{ds} \tag{3.6.2}$$

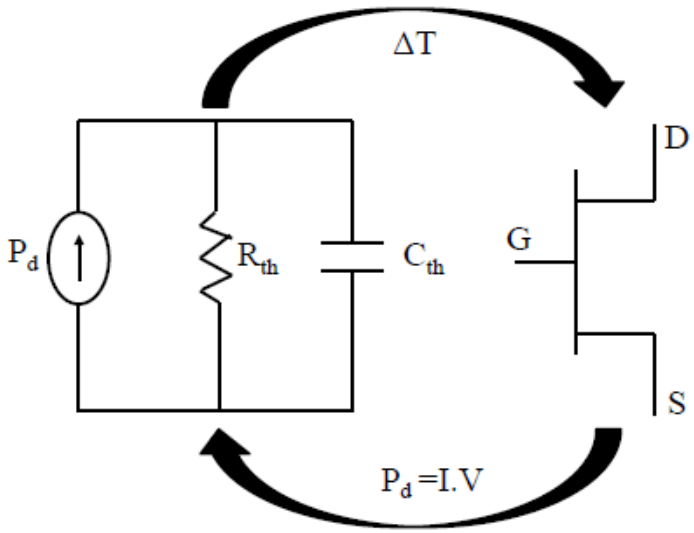
Where $\psi_m = (\psi_d + \psi_s)/2$, $\psi_d s = (\psi_d - \psi_s)$

© 2023 Cadence Design Systems, Inc.

Self Heating Model

The self-heating effect is modeled using the R-C network approach that consists of thermal resistance (RTH) and thermal capacitance (CTH). The thermal node voltage gives the rise in temperature that is added to the die temperature.

R-C thermal network for self-heating effect



Short Channel Effects

Short channel e.ects play an important role in determining the near to accurate currents.

Velocity Saturation

Velocity saturation is modeled as:

$$\mu_{eff,sat} = \frac{\mu_{eff}}{\sqrt{1 + (\mu_{eff}/VSAT \cdot E_x)^2}} \qquad (3.9.1)$$

© 2023 Cadence Design Systems, Inc.

where E_x is the lateral electric field and can be taken as (Ψ_d - Ψ_s)/L = Ψ_d s/L with L as the channel length of the device.

$$\mu_{eff,sat} = \frac{\mu_{eff}}{\sqrt{1 + THESAT^2 \cdot \psi_{ds}^2}} \qquad (3.9.2)$$

where, $THESAT$ is a model parameter with initial value μ_{eff} / VSAT · L.

DIBL

DIBL effect is included in V_{off} modeling.

$$V_{off,DIBL} = VOFF - (ETA0 - TRAPETA0 \cdot vcap + eta0_{trap}) \cdot \left(\frac{V_{dsx} \cdot VDSCALE}{\sqrt{V_{dsx}^2 + VDSCALE^2}} \right) \qquad (3.9.3)$$

Subthreshold Slope

Subthreshold slope tells about the leakage currents in the device. More subthreshold slope means more leakage currents. It is modeled in ASM-HEMT as follows:

$cdsc = 1 + NFACTOR + (CDSCD + cdsc_{trap}) \cdot V_{dsx}$ (3.9.4)

Channel Length Modulation

Channel length modulation reduces the effective length of the device thereby increasing the current in it. It is modeled in ASM-HEMT as follows:

$I_{ds,clm} = I_{ds} (1 + LAMBDA \cdot (V_{dsx} - V_{d,eff}))$ (3.9.5)

Access Region and Parasitic Resistances

Access region resistances are important in HEMTs as the distance between gate edge and source and drain edges are large and in the order of few μm. It can be modeled as bias dependent resistance.

© 2023 Cadence Design Systems, Inc.

Source Region Resistance

It includes bias dependent access region resistance, source contact resistance and resistance due to traps. If `RDSMOD = 1`,

$$R_{source} = \frac{RSC(T)}{W \cdot NF} + TRAPRS \cdot vcap + \frac{LSG}{W \cdot NF \cdot q \cdot NS0ACCS(T) \cdot U0ACCS(T)} \cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCS}\right)^{\frac{-1}{MEXPACCS}} \quad (3.10.1)$$

where

$I_{sat,source} = W \cdot NF \cdot NS0ACCS(T) \cdot VSATACCS(T)$

If $RDSMOD$ is zero, then $R_{source} = 10^{-6}$

Drain Region Resistance

It includes bias dependent access region resistance, source contact resistance and resistance due to traps. If `RDSMOD = 1`,

$$R_{drain} = \frac{RDC(T)}{W \cdot NF} + TRAPRD \cdot vcap + R_{trap}(T) + ron_{trap} + \frac{LDG}{W \cdot NF \cdot q \cdot NS0ACCD(T) \cdot U0ACCD(T)} \cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCD}\right)^{\frac{-1}{MEXPACCD}} \quad (3.10.2)$$

where $I_{sat,drain} = W \cdot NF \cdot NS0ACCD(T) \cdot VSATACCS(T)$

If $RDSMOD$ is zero, then $R_{drain} = 10^{-6}$

© 2023 Cadence Design Systems, Inc.

Gate Region Conductance

$$G_{gate} = RSHG\left(\frac{XGW + W/(3 \cdot NGCON)}{NGCON \cdot NF \cdot L}\right) \qquad (3.10.3)$$

If $G_{gate} > 0$

$G_{gate} = 1/G_{gate}$

else

$G_{gate} = 10^3$

Parasitic Capacitances

Access Region Capacitances

The access region capacitance particularly at the drain end of the device, which shows up in drain-source capacitance (C_{ds}), takes the form of a bias-dependent depletion capacitance and is formulated as follows:

$$C_{accd} = \frac{CJ0}{(1 + \frac{V_{ds}}{VBI})^{MZ}} \qquad (3.11.1)$$

Overlap Capacitances

CGSO, CDSO, CGDO and CGDL are presented as model parameters to include overlap capacitance effects.

Fringing Capacitances

Model parameters, CFD and CFG are included to get the e.ects of fringing capacitances.

© 2023 Cadence Design Systems, Inc.

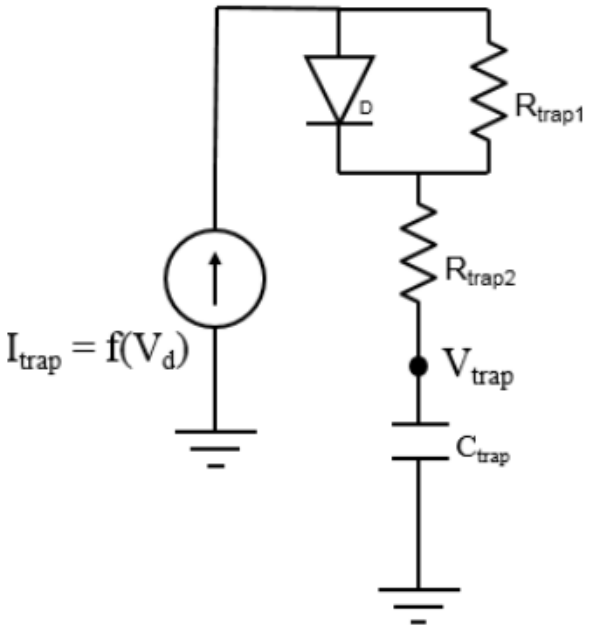
Trap Model

The presence of traps at the surface, in the barrier and the buffer layer are well-known in GaN HEMTs. These traps affect device characteristics significantly and give rise to the effects, such as drain-lag, gate-lag, knee walk-out, and dynamic on-resistance.

The trapping effects are modeled in ASM-HEMT model with the help of a subcircuit.

You can choose from four different trapping effects models: TRAPMOD=1, 2, 3, and 4 as described below. When TRAPMOD is set to 0, trapping effects are not modeled.

The topology for TRAPMOD=1 is shown in figure below.

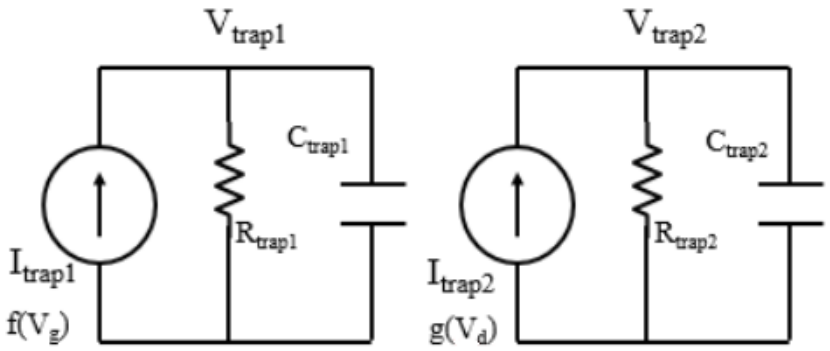


Modeling trapping effects in GaN HEMTs with the voltage Vtrap in this subcircuit for TRAPMOD=1.

The trap-voltage V_{trap} generated is fed back into the model and it updated parameters like the cut-off voltage, DIBL, source and drain-resistances to capture the effects of traps.

© 2023 Cadence Design Systems, Inc.

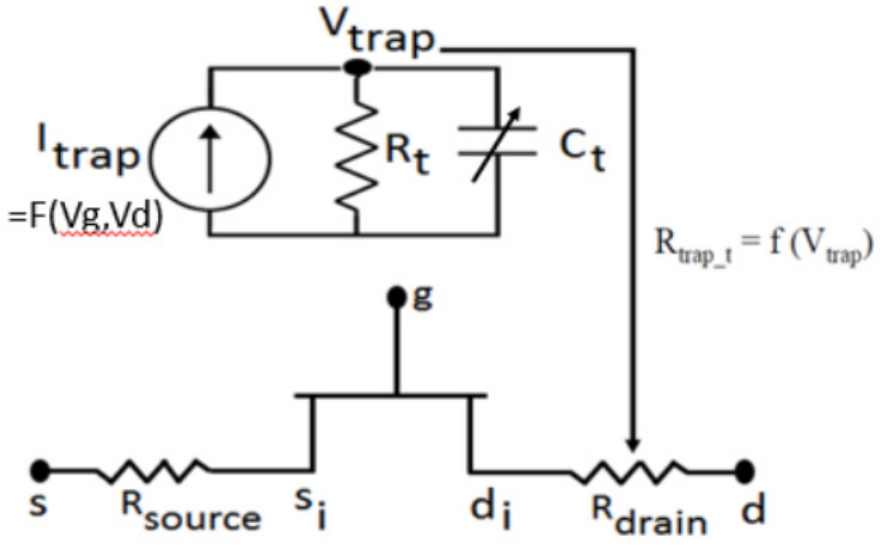
The topology for TRAPMOD=2 is shown below. In this case two different RC subcircuits are used.



Modeling trapping effects in GaN HEMTs with the voltage Vtrap1 and Vtrap2 in this subcircuit.

The trap voltages V_{trap1} and V_{trap2} update the parameters cut-off voltage, subthreshold slope, source and drain-resistances to capture the effects of traps. In this case, since the trap generation current is both a function of V_d and V_g this model is more flexible.

The topology for trap-model TRAPMOD=3 is shown below.



Modeling trapping e.ects in GaN HEMTs with the RC subcircuit.

© 2023 Cadence Design Systems, Inc.

This is recommended for modeling the GaN power device dynamic ON-resistance. Only the drain-side resistance is affected in this trap model.

Version 101.3.0 introduces Trap model 4 to describe the Drain-lag (DL) and Gate-lag (GL) phenomenon in GaN devices with most flexibility in tuning the model independently for DL and GL. In Trap model 4, the trap voltage is obtained with RC sub-circuits due to drain- and gate-bias change. The trap voltage changes key model parameters in pulsed simulation conditions only. DC and S-parameter simulations are not affected by the parameter change.

Gate Current Model

The modeling of gate current in ASM-HEMT is implemented using two diodes, one is for gate-to-source current and another is for gate-to-drain current. The current expressions are given below.

$$I_{gs} = W \cdot L \cdot NF \cdot \left[IGSDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGS \right] \left[exp\left\{ \frac{V_{gs}}{NJGS \cdot K_B \cdot T_{dev}} \right\} - 1 \right] \tag{3.13.1}$$

$$I_{gd} = W \cdot L \cdot NF \cdot \left[IGDDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGD \right] \left[exp\left\{ \frac{V_{gd}}{NJGD \cdot K_B \cdot T_{dev}} \right\} - 1 \right] \tag{3.13.2}$$

Here, `IGSDIO` and `IGDDIO` represent saturation currents of gate-source and gatedrain junction diodes, respectively. `NJGS` and `NJGD` are the diode current ideality factors and parameters `KTGS` and `KTGD` are used to capture the temperature dependence of gate saturation current.

© 2023 Cadence Design Systems, Inc.

Field Plate Model

Cross Coupling Capacitances

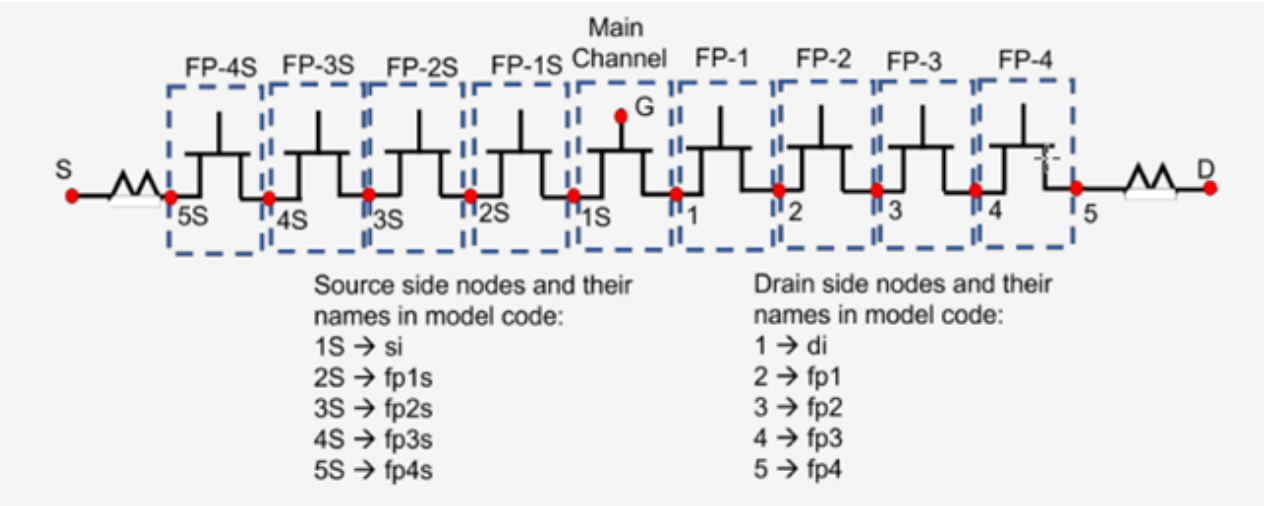
The two associated cross-coupling charges are evaluated in terms of the existing gate charge formulation as given below.

$$Q_{cc,cgd} = -CFP2SCALE \times WL_{FP2}C_{g,FP2}\left\{V_{go,FP2} - \frac{1}{2}\left(\psi_{s,FP2} + \psi_{d,FP2}\right)\right. \tag{3.14.1}$$
$$\left. + \frac{\left(\psi_{d,FP2} - \psi_{s,FP2}\right)^2}{12\left(V_{go,FP2} - \frac{K_BT}{q} - \frac{1}{2}\left(\psi_{s,FP2} + \psi_{d,FP2}\right)\right)^2}\right\}$$

$$Q_{cc,csd} = -CFP1SCALE \times WL_{FP1}C_{g,FP1}\left\{V_{go,FP1} - \frac{1}{2}\left(\psi_{s,FP1} + \psi_{d,FP1}\right)\right. \tag{3.14.2}$$
$$\left. + \frac{\left(\psi_{d,FP1} - \psi_{s,FP1}\right)^2}{12\left(V_{go,FP1} - \frac{K_BT}{q} - \frac{1}{2}\left(\psi_{s,FP1} + \psi_{d,FP1}\right)\right)^2}\right\}$$

$Q_{cc,cgd}$ and $Q_{cc,csd}$ represents the cross-coupling charge between the $FP1 - 2DEG_{FP2}$ and $FP2 - 2DEG_{FP1}$ respectively. $CFP2SCALE$ and $CFP1SCALE$ denote dimensionless scaling factors that determine the strength of cross-coupling plateaus observed in C_{gd} and C_{sd} respectively. These charges are assigned between the gate of one field-plate transistor and the source node of the other field-plate transistor.

© 2023 Cadence Design Systems, Inc.



Model representation of the Field-Plate model implementation and internal nodes is shown in the above figure with all the eight Field-Plates. These can be configured with the Field-Plate model selector switches.

Substrate Capacitance

The regional substrate charges are evaluated using the existing gate charge formulation given as:

$$Q_{sub,K} = -CSUBSCALE,K \times WL_K C_{g,K} \left\{ V_{go,K} - \frac{1}{2}\left(\psi_{s,K} + \psi_{d,K}\right) + \frac{\left(\psi_{d,K} - \psi_{s,K}\right)^2}{12\left(V_{go,K} - \frac{K_B T}{q} - \frac{1}{2}\left(\psi_{s,K} + \psi_{d,K}\right)\right)^2} \right\} \qquad (3.14.3)$$

where K is i, 1 and 2 for intrinsic transistor, $FP1$ transistor and $FP2$ transistor respectively.

$CSUBSCALE,K$ is a dimensionless scaling factor that controls the magnitude of the regional substrate charges.

Quantum Mechanical Effects

Due to the quantum nature of the $2DEG$ charge at the hetero-interface, the centroid shift of the probability distribution functions needs to be accounted for in the model. The resulting

© 2023 Cadence Design Systems, Inc.

increase in the barrier thickness, reduces the gate capacitance per unit area which subsequently is used in all the intrinsic charge equations.

$$C_g = \frac{\epsilon_{AlGaN}}{TBAR + ADOS/(1 + CDOS \cdot (Q_g/QM0))^{BDOS}} \tag{3.14.4}$$

Noise Model

Thermal and Flicker noise models are included in ASM-HEMT model.

Flicker Noise Model

The power spectral density (PSD) of the mean square fluctuations in number of occupied traps is given as:

$$S_N(f) = N_t \frac{k_B T_{dev}}{N_{P_t} f^{EF}} \tag{3.15.1}$$

where N_t is the concentration of traps (in cm^{-2}) and f is the frequency of operation. The N_{Pt} factor comes from tunneling probability and EF is a modeling parameter.This in turn gives the drain current noise PSD as:

$$S_{if}(f) = \frac{S_N(f)}{WL^2} \int_0^L \left(\frac{\partial I_{DS}}{\partial N_t}\right)^2 dx \tag{3.15.2}$$

Also,

$$I_{DS} = \mu W(-Q_{ch}(x)) \frac{\partial \psi}{\partial x} \tag{3.15.3}$$

$$\partial I_{DS} = \mu W(-Q_{ch}) \frac{\partial \psi}{\partial x} \left[\frac{1}{-Q} \frac{\partial(-Q)}{\partial N_t} \pm \frac{1}{\mu} \frac{\partial \mu}{N_t}\right] \partial N_t \tag{3.15.4}$$

$$\partial I_{DS} = I_{DS} \left[\frac{qR}{-Q_{ch}} \pm \frac{1}{\mu} \frac{\partial \mu}{\partial N_t}\right] \partial N_t \tag{3.15.5}$$

where $R = \frac{1}{q} \frac{\partial(-Q_{ch})}{\partial N_t}$.

© 2023 Cadence Design Systems, Inc.

The + or − sign depends on whether a trap is neutral or charged when filled, which will increase or decrease mobility. Using (3.15.2) and (3.15.5), we get the drain current noise PSD as:

$$S_{if}(f) = \frac{k_B T}{W L^2 f^{EF}} \frac{I_{DS}^2 K_r}{C_g^2} \Big[NOIA V_{th} C_g \left(\frac{1}{Q_{ch,d}} - \frac{1}{Q_{ch,s}} \right) + (NOIA + NOIB V_{th} C_g) ln \left(\frac{Q_{ch,d}}{Q_{ch,s}} \right) \tag{3.15.6}$$

$$+ (NOIB + NOIC V_{th} C_g)(-Q_{ch,d} + Q_{ch,s}) + \frac{NOIC}{2}(Q_{ch,d}^2 - Q_{ch,s}^2) \Big] \tag{3.15.7}$$

Thermal Noise Model

The noise PSD can be given as:

$$S_{it} = \frac{4 k_B T_{dev}}{I_D L_{eff}^2} \int_{\psi_s}^{\psi_d} g^2(\psi) d\psi \tag{3.15.8}$$

Where, $V_{go} - \psi_m + V_{th})(\psi_d - \psi_s)]$, $Q_{ch,(d/s)} = qC_g \left(V_{go} - \psi_{(d/s)} \right)$ and *NOIA*, *NIOIB* and *NOIC* are parameters that include terms like N_{Pt} and N_t.

The final noise PSD can therefore be written as:

$$S_{it} = \frac{4 k_B T_{dev}}{I_D L_{eff}^2} \left(\mu_{eff,sat} W q C_g \right)^2 \left(V_{go}^2 \psi_{ds} + \frac{\psi_d^3 - \psi_s^3}{3} - V_{go} \left(\psi_d^2 - \psi_s^2 \right) \right) \tag{3.15.9}$$

© 2023 Cadence Design Systems, Inc.

Component Statements

Model Definition

```
model modelName asm_gan parameter=value ...
```

Instance Definition

```
Name  d  g  s  b  [Tnode] ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

1	`l=0.25e-6`	Channel Length.
2	`w=200.0e-6`	Channel Width.
3	`nf=1`	Number of fingers.
4	`dfp1=50.0e-9`	Distance of FP1 from 2-DEG Charge.
5	`lfp1=1.0e-6`	Length of FP1.
6	`dfp2=100.0e-9`	Distance of FP2 from 2-DEG Charge.
7	`lfp2=1.0e-6`	Length of FP2.
8	`dfp3=150.0e-9`	Distance of FP3 from 2-DEG Charge.
9	`lfp3=1.0e-6`	Length of FP3.
10	`dfp4=200.0e-9`	Distance of FP4 from 2-DEG Charge.
11	`lfp4=1.0e-6`	Length of FP4.
12	`dtemp=0.0`	Temperature variability parameter.
13	`ngcon=1`	Number of gate contacts.
14	`m=1`	Multiplicity factor.
15	`trise=0.0`	Alias of dtemp.
16	`isnoisy=yes`	Should device generate noise. Possible values are no and yes.

Model Parameters

1	`version=101.0`	The model parameter "version" only accepts a real number value, like 101.0 for version=101.0. The available versions now are 101.0, 101.1, 101.2 and 101.3.
2	`tnom=27.0`	Nominal Temperature in degree Celsius.
3	`tbar=2.5e-8`	Barrier layer thickness.
4	`epsilon=10.66e-11`	Dielectric Permittivity of AlGaN layer.
5	`voff=(-2.0)`	Cut-off voltage.
6	`u0=170.0e-3`	Low field mobility.
7	`ua=0.0e-9`	Mobility Degradation coefficient first order.
8	`ub=0.0e-18`	Mobility Degradation coefficient second order.
9	`vsat=1.9e5`	Saturation Velocity.
10	`delta=2.0`	Exponent for Vdeff.
11	`at=0.0`	Temperature Dependence for saturation velocity.
12	`ute=(-0.5)`	Temperature dependence of mobility.
13	`lambda=0.0`	Channel Length Modulation Coefficient.
14	`eta0=1.0e-9`	DIBL Parameter.
15	`vdscale=5.0`	DIBL Scaling VDS.

© 2023 Cadence Design Systems, Inc.

16	`kt1=0.0e-3`	Temperature Dependence for Voff.
17	`thesat=1.0`	Velocity Saturation Parameter.
18	`nfactor=0.5`	Sub-voff Slope parameters.
19	`cdscd=1.0e-3`	Sub-voff Slope Change due to Drain Voltage.
20	`gamma0i=2.12e-12`	Schrodinger-Poisson solution parameter.
21	`gamma1i=3.73e-12`	Schrodinger-Poisson solution parameter.
22	`imin=1.0e-15`	Minimum Drain Current.
23	`shmod=1`	Switch to turn on and off self-heating model.
24	`rth0=5.0`	Thermal Resistance.
25	`cth0=1.0e-9`	Thermal Capacitance.
26	`rdsmod=0`	Switch for external source and drain resistances.
27	`vsataccs=50.0e3`	Saturation Velocity for access region: Source Side.
28	`ns0accs=5.0e17`	2-DEG Charge Density in per square meter in Source access region.
29	`ns0accd=5.0e17`	2-DEG Charge Density in per square meter in Drain access region.
30	`k0accs=0.0`	Vg dependence parameter of source side access region 2-DEG charge density.
31	`k0accd=0.0`	Vg dependence parameter of drain side access region 2-DEG charge density.
32	`u0accs=155e-3`	Access region mobility source-side.
33	`u0accd=155e-3`	Access region mobility drain-side.
34	`mexpaccs=2.0`	Exponent for access region resistance model.
35	`mexpaccd=2.0`	Exponent for access region resistance model.
36	`lsg=1.0e-6`	Length of Source-Gate Access Region.
37	`ldg=1.0e-6`	Length of Drain-Gate Access Region or Length of drain side access region.
38	`rsc=1.0e-4`	Source Contact Resistance.
39	`rdc=1.0e-4`	Drain Contact Resistance.
40	`kns0=0.0`	Temperature Dependence for 2-DEG charge density at access region.
41	`ats=0.0`	Temperature Dependence for saturation velocity at access region.
42	`utes=0.0`	Temperature dependence of mobility at access region: Source Side.
43	`uted=0.0`	Temperature dependence of mobility at access region: Drain Side.

© 2023 Cadence Design Systems, Inc.

44	krsc=0.0	Temperature dependence of Source Contact Resistance.
45	krdc=0.0	Temperature dependence of Drain Contact Resistance.
46	gatemod=0	Model Switch to turn on and off the gate current formulations.
47	njgs=2.5	Gate-source junction diode current ideality factor.
48	njgd=2.5	Gate-drain junction diode current ideality factor.
49	rnjgs=80.0	Gate-source junction diode rev. current slope factor.
50	rnjgd=80.0	Gate-drain junction diode rev. current slope factor.
51	igsdio=1.0	Gate-source junction diode saturation current.
52	igddio=1.0	Gate-drain junction diode saturation current.
53	rigsdio=1.0e-15	Gate-source junction diode rev. current frenkel-poole multiplier.
54	rigddio=1.0e-15	Gate-drain junction diode rev. current frenkel-poole multiplier.
55	vbis=1e-4	Gate-source junction diode built-in voltage.
56	vbid=1e-4	Gate-drain junction diode built-in voltage.
57	ebreaks=0.0	Fitting parameter for large rev bias gate current.
58	ebreakd=0.0	Fitting parameter for large rev bias gate current.
59	ktgs=0.0	Temperature co-efficient of gate-source junction diode current.
60	ktgd=0.0	Temperature coefficient of gate-drain junction diode current.
61	rktgs=0.0	Temperature co-efficient of reverse gate-source junction diode current.
62	rktgd=0.0	Temperature coefficient of reverse gate-drain junction diode current.
63	ktvbis=0.0	Temperature coefficient for built-in voltage source side.
64	ktvbid=0.0	Temperature coefficient for built-in voltage drain side.
65	ktnjgs=0.0	Temperature coefficient forward slope source-side.
66	ktnjgd=0.0	Temperature coefficient forward slope drain-side.
67	ktrnjgs=0.0	Temperature coefficient reverse slope source-side.
68	ktrnjgd=0.0	Temperature coefficient reverse slope drain-side.
69	trapmod=0	Model Switch to turn on and off the dynamic trapping effects.
70	remi=1.0	Drain lag emmission resistance.
71	cglag=10.0e-6	Gate lag trapping capacitance.

© 2023 Cadence Design Systems, Inc.

72	remig=1.0	Gate lag trapping resistance.
73	arcap=0.0	Drain lag trap potential tuning parameter.
74	brcap=0.5	Drain lag trap potential tuning parameter.
75	arcapg=0.0	Gate lag trap potential tuning parameter.
76	brcapg=0.5	Gate lag trap potential tuning parameter.
77	vdlmax=20.0	Drain lag parameter for limiting parameter change.
78	vglmax=5.0	Gate lag parameter for limiting parameter change.
79	dlvoff=0e-4	Voff tuning due to drain lag.
80	glvoff=0e-4	Voff tuning due to gate lag.
81	glu0=0e-4	U0 tuning due to drain lag.
82	glvsat=0e-4	VSAT tuning due to gate lag.
83	dlns0s=0e-4	Source-side 2-deg tune due to drain lag.
84	dlns0d=0e-4	Drain-side 2-deg tune due to gate-lag.
85	cdlag=1.0e-6	Trap Network capacitance.
86	rdlag=1.0e6	Trap Network resistance.
87	idio=1.0e0	Saturation Current parameter for trap model.
88	atrapvoff=0.1	Voff change due to trapping effects.
89	btrapvoff=0.3	Voff change with input power due to trapping effects.
90	atrapeta0=0	DIBL change due to trapping effects.
91	btrapeta0=0.05	DIBL change with input power due to trapping effects.
92	atraprs=0.1	Rs change due to trapping effects.
93	btraprs=0.6	Rs change with input power due to trapping effects.
94	atraprd=0.5	Rd change due to trapping effects.
95	btraprd=0.6	Rd change with input power due to trapping effects.
96	rtrap1=1.0	Trap Network1 Resistance.
97	rtrap2=1.0	Trap Network2 Resistance.
98	ctrap1=10.0e-6	Trap Network1 Capacitance.
99	ctrap2=1.0e-6	Trap Network2 Capacitance.
100	a1=0.1	Multiplication factor [1st network].
101	vofftr=1.0e-9	Trap contribution to voff [2nd network].
102	cdscdtr=1.0e-15	Trap contribution to cdscd [2nd network].
103	eta0tr=1.0e-15	Trap contribution to DIBL [2nd network].
104	rontr1=1.0e-12	Trap contribution to RON [1st network].
105	rontr2=1.0e-13	Trap contribution to RON [2nd network].
106	rontr3=1.0e-13	Trap contribution to RON.
107	rtrap3=1.0	Trap Network Resistance.
108	ctrap3=1.0e-4	Trap Network Capacitance.

© 2023 Cadence Design Systems, Inc.

109	`vatrap=10.0`	Division factor for V[trap1].
110	`wd=0.016`	Weak dependence of vdlr1 on Vdg.
111	`vdlr1=2.0`	Slope for region one.
112	`vdlr2=20.0`	Slope for region two.
113	`talpha=1.0`	Temperature dependence Coefficient.
114	`vtb=250.0`	Break Point for Vdg effect on Von.
115	`deltax=0.01`	Smoothing parameter.
116	`fastfpmod=0`	Fast field-plate model formulations [0:Conventional FP model; 1: Fast model calculations].
117	`fp1mod=0`	Field Plate Model Selector [0:No FP; 1:Gate FP; 2:Source FP;].
118	`fp1smod=0`	Source-side Field Plate Model Selector [0:No FP; 1:Gate FP; 2:Source FP;].
119	`fp2mod=0`	Drain-side Field Plate Model Selector [0:No FP; 1:Gate FP; 2:Source FP;].
120	`fp2smod=0`	Source-side Field Plate Model Selector [0:No FP; 1:Gate FP; 2:Source FP;].
121	`fp3mod=0`	Drain-side Field Plate Model Selector [0:No FP; 1:Gate FP; 2:Source FP;].
122	`fp3smod=0`	Source-side Field Plate Model Selector [0:No FP; 1:Gate FP; 2:Source FP;].
123	`fp4mod=0`	Drain-side Field Plate Model Selector [0:No FP; 1:Gate FP; 2:Source FP;].
124	`fp4smod=0`	Source-side Field Plate Model Selector [0:No FP; 1:Gate FP; 2:Source FP;].
125	`iminfp1=1.0e-15`	Minimum Drain Current FP1 region.
126	`vofffp1=(-25.0)`	voff for FP1.
127	`ktfp1=50.0e-3`	Temperature Dependence for vofffp1.
128	`u0fp1=100e-3`	FP1 region mobility.
129	`vsatfp1=100e+3`	Saturation Velocity of FP1 region.
130	`nfactorfp1=0.5`	Sub-voff Slope parameters for FP1.
131	`cdscdfp1=0.0`	Sub-voff Slope Change due to Drain Voltage for FP1.
132	`eta0fp1=1.0e-9`	DIBL Parameter for FP1.
133	`vdscalefp1=10.0`	DIBL Scaling VDS for FP1.
134	`gamma0fp1=2.12e-12`	Schrodinger-Poisson solution parameter for FP1.
135	`gamma1fp1=3.73e-12`	Schrodinger-Poisson solution parameter for FP1.
136	`iminfp2=1.0e-15`	Minimum Drain Current FP2 region.

© 2023 Cadence Design Systems, Inc.

137	`vofffp2=(-50.0)`	voff for FP2.
138	`ktfp2=50.0e-3`	Temperature Dependence for vofffp2.
139	`u0fp2=100e-3`	Carrier mobility of FP2 region.
140	`vsatfp2=100e+3`	Saturation velocity of FP2 region.
141	`nfactorfp2=0.5`	Sub-voff Slope parameters for FP2.
142	`cdscdfp2=0.0`	Sub-voff Slope Change due to Drain Voltage for FP2.
143	`eta0fp2=1.0e-9`	DIBL Parameter for FP2.
144	`vdscalefp2=10.0`	DIBL Scaling VDS for FP2.
145	`gamma0fp2=2.12e-12`	Schrodinger-Poisson solution parameter for FP2.
146	`gamma1fp2=3.73e-12`	Schrodinger-Poisson solution parameter for FP2.
147	`iminfp3=1.0e-15`	Minimum Drain Current FP3 region.
148	`vofffp3=(-75.0)`	voff for FP3.
149	`ktfp3=50.0e-3`	Temperature Dependence for vofffp3.
150	`u0fp3=100e-3`	FP3 region mobility.
151	`vsatfp3=100e+3`	Saturation Velocity of FP3 region.
152	`nfactorfp3=0.5`	Sub-voff Slope parameters for FP3.
153	`cdscdfp3=0.0`	Sub-voff Slope Change due to Drain Voltage for FP3.
154	`eta0fp3=1.0e-9`	DIBL Parameter for FP3.
155	`vdscalefp3=10.0`	DIBL Scaling VDS for FP3.
156	`gamma0fp3=2.12e-12`	Schrodinger-Poisson solution parameter for FP3.
157	`gamma1fp3=3.73e-12`	Schrodinger-Poisson solution parameter for FP3.
158	`iminfp4=1.0e-15`	Minimum Drain Current FP4 region.
159	`vofffp4=(-100.0)`	voff for FP4.
160	`ktfp4=50.0e-3`	Temperature Dependence for vofffp4.
161	`u0fp4=100e-3`	FP4 region mobility.
162	`vsatfp4=100e+3`	Saturation Velocity of FP4 region.
163	`nfactorfp4=0.5`	Sub-voff Slope parameters for FP4.
164	`cdscdfp4=0.0`	Sub-voff Slope Change due to Drain Voltage for FP4.
165	`eta0fp4=1.0e-9`	DIBL Parameter for FP4.
166	`vdscalefp4=10.0`	DIBL Scaling VDS for FP4.
167	`gamma0fp4=2.12e-12`	Schrodinger-Poisson solution parameter for FP4.
168	`gamma1fp4=3.73e-12`	Schrodinger-Poisson solution parameter for FP4.
169	`cgso=0.0e-18`	Gate-source overlap capacitance.
170	`cgdo=0.0e-18`	Gate-drain overlap capacitance.
171	`cdso=0.0e-18`	Cds capacitance parameter.
172	`cgdl=0.0e-15`	Vds bias dependence of parasitic gate drain overlap capacitance.

© 2023 Cadence Design Systems, Inc.

173	`vdsatcv=100.0`	Saturation voltage on drain side in CV Model.
174	`cbdo=0.0e-15`	Substrate capacitance parameter.
175	`cbso=0.0e-15`	Substrate capacitance parameter.
176	`cbgo=0.0e-15`	Substrate capacitance parameter.
177	`cfg=0.0e-18`	Fringing capacitance parameter.
178	`cfd=0.0e-18`	Fringing capacitance parameter.
179	`cfgd=0.0e-13`	Fringing capacitance parameter.
180	`cfgdsm=1.0e-24`	Capacitance smoothing parameter.
181	`cfgd0=0.0e-12`	Fringing capacitance parameter.
182	`cj0=0.0e-15`	Zero bias depletion capacitance.
183	`vbi=0.9`	Built in potential.
184	`ktvbi=0.0`	Temperature dependence of built in potential.
185	`ktcfg=0.0e-3`	Temperature dependence of Fringing capacitance.
186	`ktcfgd=0.0e-3`	Temperature dependence of Fringing capacitance.
187	`mz=0.5`	Grading factor of depletion capacitance.
188	`aj=100.0e-3`	Limiting factor of depletion capacitance in forward bias region.
189	`dj=1.0`	Fitting parameter.
190	`adosi=0.0`	Quantum mechanical effect pre-factor cum switch in inversion.
191	`bdosi=1.0`	Charge centroid parameter - slope of CV curve under QME in inversion.
192	`qm0i=1.0e-3`	Charge centroid parameter - starting point for QME in inversion.
193	`adosfp1=0.0`	Quantum mechanical effect pre-factor cum switch in inversion.
194	`bdosfp1=1.0`	Charge centroid parameter - slope of CV curve under QME in inversion.
195	`qm0fp1=1.0e-3`	Charge centroid parameter - starting point for QME in inversion.
196	`adosfp2=0.0`	Quantum mechanical effect pre-factor cum switch in inversion.
197	`bdosfp2=1.0`	Charge centroid parameter - slope of CV curve under QME in inversion.
198	`qm0fp2=1.0e-3`	Charge centroid parameter - starting point for QME in inversion.

© 2023 Cadence Design Systems, Inc.

199	`adosfp3=0.0`	Quantum mechanical effect pre-factor cum switch in inversion.
200	`bdosfp3=1.0`	Charge centroid parameter - slope of CV curve under QME in inversion.
201	`qm0fp3=1.0e-3`	Charge centroid parameter - starting point for QME in inversion.
202	`adosfp4=0.0`	Quantum mechanical effect pre-factor cum switch in inversion.
203	`bdosfp4=1.0`	Charge centroid parameter - slope of CV curve under QME in inversion.
204	`qm0fp4=1.0e-3`	Charge centroid parameter - starting point for QME in inversion.
205	`cfp1scale=0.0`	Coupling of charge under FP1.
206	`cfp2scale=0.0`	Coupling of charge under FP2.
207	`cfp3scale=0.0`	Coupling of charge under FP3.
208	`cfp4scale=0.0`	Coupling of charge under FP4.
209	`csubscalei=0.0`	Sub Capacitance scaling parameter.
210	`csubscale1=0.0`	Sub Capacitance scaling parameter.
211	`csubscale2=0.0`	Sub Capacitance scaling parameter.
212	`csubscale3=0.0`	Sub Capacitance scaling parameter.
213	`csubscale4=0.0`	Sub Capacitance scaling parameter.
214	`rgatemod=0`	Model Switch to turn on and off the gate resistance.
215	`xgw=0.0`	Distance from gate contact centre to dev edge.
216	`rshg=1.0e-3`	Gate sheet resistance.
217	`fnmod=0`	Switch to turn Flicker Noise Model ON [fnmod=1] or OFF [fnmod=0].
218	`tnmod=0`	Switch to turn Thermal Noise Model ON [tnmod=1] or OFF [tnmod=0].
219	`noia=15.0e-12`	Flicker Noise parameter.
220	`noib=0.0`	Flicker Noise parameter.
221	`noic=0.0`	Flicker Noise parameter.
222	`ef=1`	Exponent of frequency---Determines slope in log plot.
223	`tnsc=1.0e27`	Thermal noise scaling parameter.
224	`gdsmin=1.0e-12`	Shunt conduntance across channel and all field plates.
225	`bvdsl=200.0`	Drain-source breakdown due to punch-through.
226	`asl=0.0`	Breakdown model multiplier parameter.
227	`nsl=10.0`	Exponent in the breakdown model.

© 2023 Cadence Design Systems, Inc.

228	`kasl=0.0`	Temperature Dependence for asl parameters in breakdown.
229	`knsl=0.0`	Temperature Dependence for nsl parameters in breakdown.
230	`kbvdsl=0.0`	Temperature Dependence for bvdsl parameters in breakdown.
231	`ngcon=1`	Number of gate contacts.
232	`dfp1=50.0e-9`	Distance of FP1 from 2-DEG Charge.
233	`lfp1=1.0e-6`	Length of FP1.
234	`dfp2=100.0e-9`	Distance of FP2 from 2-DEG Charge.
235	`lfp2=1.0e-6`	Length of FP2.
236	`dfp3=150.0e-9`	Distance of FP3 from 2-DEG Charge.
237	`lfp3=1.0e-6`	Length of FP3.
238	`dfp4=200.0e-9`	Distance of FP4 from 2-DEG Charge.
239	`lfp4=1.0e-6`	Length of FP4.
240	`trise=0.0 C`	Temperature rise from ambient, alias of dtemp. It served as the default value of instance trise .

© 2023 Cadence Design Systems, Inc.

Output Parameters

1	`tempeff`	Effective temperature without selfheating temperature.
2	`meff`	Effective multiplicity factor (m-factor).

Operating-Point Parameters

1	`trise=0.0`	Alias of dtemp.
2	`idisi (A)`	Intrinsic drain-to-source current.
3	`vdisi (V)`	Intrinsic drain-to-source voltage.
4	`vgisi (V)`	Intrinsic drain-to-source voltage.
5	`gmi (A/V)`	Intrinsic trans-conductance.
6	`gdsi (A/V)`	Intrinsic output conductance.
7	`gmbi (A/V)`	Intrinsic bulk trans-conductance.
8	`igs (A)`	Gate to source current.
9	`igd (A)`	Gate to source current.
10	`qgi (C)`	Intrinsic gate charge.
11	`qdi (C)`	Intrinsic drain charge.
12	`qsi (C)`	Intrinsic source charge.
13	`qbi (C)`	Intrinsic bulk charge.
14	`cggi (F)`	Intrinsic gate capacitance.
15	`cgsi (F)`	Intrinsic gate-to-source capacitance.
16	`cgdi (F)`	Intrinsic gate-to-drain capacitance.
17	`cgbi (F)`	Intrinsic gate-to-bulk capacitance.
18	`cddi (F)`	Intrinsic drain capacitance.
19	`cdgi (F)`	Intrinsic drain-to-gate capacitance.
20	`cdsi (F)`	Intrinsic drain-to-source capacitance.
21	`cdbi (F)`	Intrinsic drain-to-bulk capacitance.
22	`cssi (F)`	Intrinsic source capacitance.
23	`csgi (F)`	Intrinsic source-to-gate capacitance.
24	`csdi (F)`	Intrinsic source-to-drain capacitance.
25	`csbi (F)`	Intrinsic source-to-bulk capacitance.
26	`cbbi (F)`	Intrinsic bulk capacitance.
27	`cbsi (F)`	Intrinsic bulk-to-source capacitance.
28	`cbdi (F)`	Intrinsic bulk-to-drain capacitance.
29	`cbgi (F)`	Intrinsic bulk-to-gate capacitance.
30	`t_total_k (K)`	Device temperature in Kelvin.

© 2023 Cadence Design Systems, Inc.

31	`t_total_c (deg C)`	Device temperature in Celsius.
32	`t_delta_sh (K)`	Increase in device temperature due to self-heating.
33	`rd (Ohm)`	Drain resistance.
34	`rs (Ohm)`	Source resistance.
35	`cgs (F)`	Total gate-to-source capacitance.
36	`cgd (F)`	Total gate-to-drain capacitance.
37	`pwr (W)`	Power at op point.

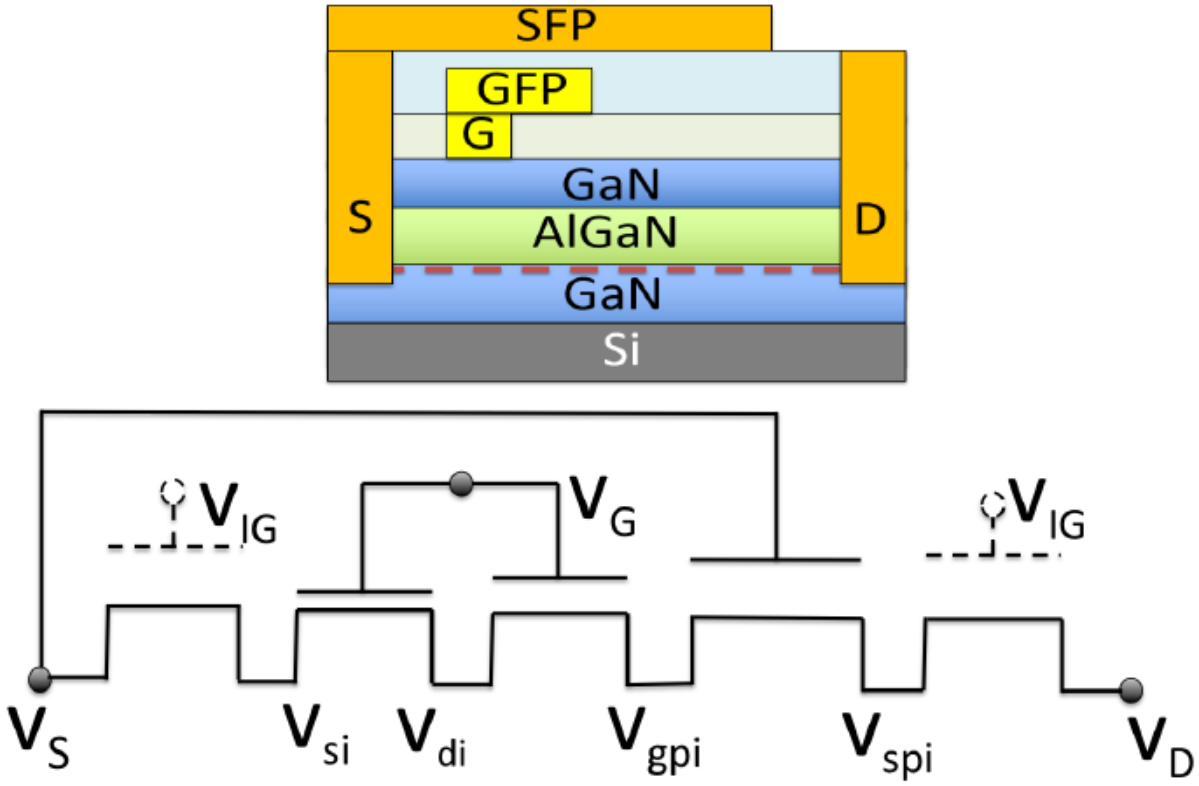
© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

54

MVSG Model

The MIT Virtual Source GaNFET (MVSG) model captures the device behavior under operating bias voltage.The device structure of GaN HEMT is shown in the figure below.



This chapter contains the following information about the MVSG model:

- Model Equations on page 3462
  - Transistor drain current formulation
  - Transistor channel charge formulation
  - Gate current formulation

© 2023 Cadence Design Systems, Inc.

- Charge trapping effects
- Device-noise: RF- and phase-noise modeling

■ Component Statements

Model Equations

Transistor drain current formulation

The current is evaluated using the following procedure. The master equation for drift current is given by:

1.

$$I_D/W = Q_{ix}V_x = Q_{ix}\mu_{eff}E_x = Q_{ix}\mu_{eff}\frac{d\psi}{dx}$$

Here ψ is the potential at location x. For the charge-based simplified all-region model, the channel layer charge is expressed as:

2.

$$\frac{dQ_{ix}}{d\psi} = C_{inv}$$

The effective mobility is given by:

3.

$$\mu_{eff} = \frac{\mu}{\left(1+\left(\frac{\frac{d\psi}{dx}}{L_g{}^{v}/\mu}\right)^{\beta}\right)^{1/\beta}}$$

Using equations 2 and 3, equation 1 can be rewritten as:

4.

$$I_D/W = Q_{ix}\frac{\mu}{\left(1+\left(\frac{dQ_{ix}}{C_{inv}L_g{}^{v}/\mu dx}\right)^{\beta}\right)^{1/\beta}}\frac{dQ_{ix}}{C_{inv}dx}$$

© 2023 Cadence Design Systems, Inc.

Using current continuity and assuming $\frac{dQ_{ix}}{dx} = \frac{Q_{is} - Q_{id}}{L_g}$ in the denominator of (4), we can integrate the above expression from `x=0` to `x=Lg` and `Qix=Qis` to `Qix=Qid`. The resulting current is given by:

5.

$$I_D/W = \frac{\mu}{2C_{inv}L_g} \frac{Q_{is}^2 - Q_{id}^2}{\left(1+\left(\frac{Q_{is}-Q_{id}}{C_{inv}L_g v/\mu}\right)^{\beta}\right)^{1/\beta}}$$

Here v is the carrier velocity combining strong and weak accumulation regimes. To make the current expression look similar to that of VS model equation 4 in equation 8, the equation 5 can be reformulated as follows:

6.

$$\frac{I_D}{W} = v\frac{1}{2C_{inv}V_{DSAT}} \frac{Q_{is}^2 - Q_{id}^2}{\left(1+\left(\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}} = v\frac{Q_{is}+Q_{id}}{2}F_{vsat}$$

where,

$$F_{vsat} = \frac{\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}}{\left(1+\left(\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}}$$

and, V_{DSAT} is similar to that in equation 5 in equation 8. V_{DSAT} must account for both strong and weak accumulation regimes and so should v. To do this we follow a similar procedure as shown below:

7a.

$$V_{DSAT} = V_{DSATS}(1 - F_f) + 2n\varphi_t F_f \quad \text{and } V_{DSATS} = \frac{v_{sat}L_g}{\mu}$$

$$v = v_{sat}(1 - F_f) + 2\varphi_t \frac{\mu}{L_g} F_f$$

v_{sat} is called the GaN saturation velocity which is similar to the saturation velocity in Si.

In the long channel limit, where transport is mobility limited, $V_{DSAT} \gg \frac{Q_{is}-Q_{id}}{C_{inv}}$, which means $F_{vsat} = \frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}$; and equation 6 reduces to:

© 2023 Cadence Design Systems, Inc.

8.

$$\frac{\mathrm{I_D}}{W} = v\frac{{Q_{is}}^2 - {Q_{id}}^2}{2C_{inv}V_{DSAT}}$$

Equation 8 is similar to the EKV model used for long channel MOSFETs. In shorter channel velocity saturation (`Vsat`) limit, $V_{DSAT} \ll \frac{Q_{is}-Q_{id}}{C_{inv}}$ and $F_{vsat} = 1$, which leads to a simple current expression:
9.

$$\frac{\mathrm{I_D}}{W} = v\frac{Q_{is}+Q_{id}}{2}$$

The expression for charges at the source-end and drain-end are given by:
10.

$$Q_{is} = 2C_{inv}\, n\, \varphi_t ln\left(1 + exp\frac{V_{GDi} - \mathrm{Vxs} - (V_T - \alpha\varphi_t F_f)}{2n\,\varphi_t}\right)\; Q_{id} = 2C_{inv}\, n\, \varphi_t ln\left(1 + exp\frac{V_{GSi} - \mathrm{Vxd} - (V_T - \alpha\varphi_t F_f)}{2n\,\varphi_t}\right)$$

Here, complete S/D symmetry is achieved using the charge formulation shown above. The terms Vxs and Vxd are in turn required to include velocity-saturation effects as shown:
11.

$$V_{XS} = \frac{V_{DSi}}{\left(1+(V_{DSi}/V_{DSAT})^{\beta}\right)^{1/\beta}}\;;\; V_{XD} = \frac{-V_{DSi}}{\left(1+(V_{DSi}/V_{DSAT})^{\beta}\right)^{1/\beta}}$$

The charge equations above are needed to model the subthreshold regime accurately. In the subthreshold regime the above equations are reduced to:
12.

$$Q_{is} = 2C_{inv}\, n\, \varphi_t exp\frac{V_{GSi} - (V_T - \alpha\varphi_t)}{2n\,\varphi_t}\;;\; Q_{id} = 2C_{inv}\, n\, \varphi_t exp\frac{V_{GDi} - (V_T - \alpha\varphi_t)}{2n\,\varphi_t}$$

© 2023 Cadence Design Systems, Inc.

Substituting (7) and (12) in (8), the current ID in subthreshold regime, where diffusion current dominates, is
13.

$$\frac{I_D}{W} = v\frac{1}{2C_{inv}V_{DSAT}}\frac{\left(2C_{inv}\,n\,\varphi_t exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}\right)^2-\left(2C_{inv}\,n\,\varphi_t exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}\right)^2}{\left(1+\left(\frac{2C_{inv}\,n\,\varphi_t exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}-2C_{inv}\,n\,\varphi_t exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}}$$

$$\approx 2\varphi_t\frac{\mu}{L_g}\frac{(2C_{inv}\,n\,\varphi_t)^2}{2C_{inv}2n\varphi_t}\left(exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{n\,\varphi_t}-exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{n\,\varphi_t}\right)$$

$$\frac{I_D}{W} = \varphi_t\frac{\mu}{L_g}\left(2C_{inv}\,n\,\varphi_t exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{n\,\varphi_t}-2C_{inv}\,n\,\varphi_t exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{n\,\varphi_t}\right)$$

This is similar to the sub threshold MOSFET diffusion current.

Transition from non-saturation to saturation current

In order to facilitate smooth transition from linear to saturation regimes under applied VDS. The charge expression at the source and drain-end is modified with VDS as:
14.

$$Q_{is(d)} = 2C_{inv}\,n\,\varphi_t ln\left(1+exp\frac{V_{Gd(s)i}-(+)V_{DSAT}F_{sat}-(V_T-\alpha\varphi_t F_f)}{2n\,\varphi_t}\right)$$

Where $V_{DSAT}F_{sat}$ is given by

15.

$$V_{DSAT}F_{sat} = V_{DSAT}\frac{V_{DSi}/V_{DSAT}}{\left(1+(V_{DSi}/V_{DSAT})^{\beta}\right)^{1/\beta}} = \frac{V_{DSi}}{\left(1+(V_{DSi}/V_{DSAT})^{\beta}\right)^{1/\beta}}$$

© 2023 Cadence Design Systems, Inc.

Here V_{DSAT} is as given in (7a) and $V_{DSi}=V_{Di}-V_{Si}$ is the intrinsic drain to source voltage. In the linear regime (at low V_{DSi}), $V_{DSAT}F_{SAT}$ approaches V_{DiSi} and Q_{id} in (14) becomes comparable to Q_{is}. Thus, the current formulation of (5) reduces to
16.

$$\frac{\mathrm{I_D}}{W}=\frac{\mu}{2C_{inv}L_g}\frac{{Q_{is}}^2-{Q_{id}}^2}{\left(1+\left(\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}}=\frac{\mu}{2C_{inv}L_g}\left({Q_{is}}^2-{Q_{id}}^2\right)\approx\frac{\mu Q_{is}}{C_{inv}L_g}\left(Q_{is}-Q_{id}\right)$$

GaN specific effects

17.

$$v_{xo}=\frac{v_{inj}}{\left(1+\theta_v\frac{Q_{ixo}}{C_{inv}}\right)}\left(1-\eta_v\mathrm{I_D}\mathrm{V_D}\right)$$

where, V_{inj} is the bias independent injection velocity at low channel charge.

Carrier mobility is modeled as:

$$\mu=\frac{\mu_0}{\left(1+\theta_\mu\frac{Q_{ixo}}{C_{inv}}\right)\left(1+\frac{\eta\mu\mathrm{I_D}\mathrm{V_D}}{T_o}\right)^{\varepsilon}}$$

Here $\theta_\mu, \eta_\mu \text{ and } \varepsilon$ are fitting parameters and T_0 is reference temperature.

Transistor channel charge formulation

Single moment partition method is used to get analytical closed form equations:

$$Q_{GSi}=\int_{x=0}^{x=L_g}\left(1-\frac{x}{L_g}\right)Q_{Gi}(\mathrm{x})\mathrm{dx}$$
$$Q_{GDi}=\int_{x=0}^{x=L_g}\left(\frac{x}{L_g}\right)Q_{Gi}(\mathrm{x})\mathrm{dx}$$

Here, Q_{Gi}(x) is the areal charge density at any point x in the channel. Q_{Gi}(x) and its dependence on bias depends on the mode of transport of carriers in the channel.

© 2023 Cadence Design Systems, Inc.

Gate charge in drift diffusion regime

The source and drain partitioned charges are based on Qinvs0 and Qinvd0 terms used for current formulation (DIBL effect is removed from these terms to avoid negative capacitances) and is therefore self-consistent with transport.

$$Q_{inv} = \frac{2}{3} W L_g \left[\frac{Q_{invs0}^2 + Q_{invd0}^2 + Q_{invs0} Q_{invd0}}{Q_{invs0} + Q_{invd0}} \right]$$

$$Q_s = \frac{2}{15} W L_g \left[\frac{2Q_{invs0}^3 + 3Q_{invd0}^3 + 4Q_{invs0}^2 Q_{invd0} + +6Q_{invd0}^2 Q_{invs0}}{Q_{invs0}^2 + Q_{invd0}^2 + 2Q_{invs0} Q_{invd0}} \right]$$

$$Q_d = Q_{inv} - Q_s$$

Field plate charges

$$Q_{C,FPX} = CC_{FPX}\, Wn_{FPX}\, \varphi_t ln\left(1 + exp\frac{V_{G(s)diFPX} - (V_{T,FPX} - \alpha\varphi_t F_f)}{n_{FPX}\, \varphi_t}\right)$$

The body capacitance associated with each FP is computed in the same way:

$$Q_{B,FPX} = CB_{FPX}\, Wn_{FPX}\, \varphi_t ln\left(1 + exp\frac{V_{BdiFPX} - (V_{T,FPX} - \alpha\varphi_t F_f)}{n_{FPX}\, \varphi_t}\right)$$

The capacitance associated with the gate field plate extension on the source-side is computed using similar method (instead of adding additional transistors for ease of computation). The capacitance is implemented only if `flagfpxs=1`.

$$Q_{S,FPX} = CS_{FPX}\, Wn_{FPX}\, \varphi_t ln\left(1 + exp\frac{V_{GsiFPX} - (V_{T,FPX} - \alpha\varphi_t F_f)}{n_{FPX}\, \varphi_t}\right)$$

© 2023 Cadence Design Systems, Inc.

Gate current formulation

The forward diode current is given by:

$$I_{Gsi(di)} = Wn_{gf}\, i_{js(d)} \left(\frac{T}{T_0}\right)^{egate} exp\frac{-P_{Gparam1} V_{jG}}{\varphi_t}\left(exp\frac{P_{Gs(d)} V_{Gsi(di)}}{\varphi_t} - 1\right)$$

where,

$$P_{Gs(d)} = P_{Gparams(d)}\left(\left(1 - fracs(d)\right)F_{f,gate} + fracs(d)\right)$$

In addition to forward current, the reverse GIDL and recombination currents are captured through empirical diode equations to account for drain voltage dependence on reverse-leakage gate currents.

$$I_{Grecsi(di)} = Wn_{gf}\, i_{recs(d)} \left(\frac{T}{T_0}\right)^{egate} \left(exp\frac{P_{Grecs(d)} F_{recs(d)}}{\varphi_t} - 1\right)$$

$$F_{recs(d)} = \frac{-V_{Gsi(di)}}{\left(1+\left(\frac{V_{Gsi(di)}}{V_{Gsatqs(d)}}\right)^{betarec}\right)^{1/betarec}}$$

Charge trapping effects

Source function for charge trapping which has the requisite bias and temperature dependence:

$$V_{tcollapse0} = trapfac * (alpha1\, V_{DG} + alpha3\left(exp\frac{V_{DG} - \text{vttrap}}{alphat2}\right))$$

Device-noise: RF- and phase-noise modeling

The noise sources are of two variants:

- RF-white noise associated with the device-level-noise sources

© 2023 Cadence Design Systems, Inc.

- low-frequency noise sources associated with charge-states in the device

RF-device-noise

The noise-power-spectral-density linked to the parasitic-resistances are given by:

$$I^2_{S,th}=4KT/R_S \;\; ; \;\; I^2_{D,th}=4KT/R_D \;\; ; \;\; I^2_{G,th}=4KT/R_G$$

Device-phase-noise

The phase-noise model adopted in the MVSG approach to capture the phase-noise in GaN-HEMTs and is given by:

$$I^2_{1/f}=K_f \frac{Wn_{gf}}{L} \frac{\left(\frac{|I_{DS}|}{Wn_{gf}}\right)^{af}}{f^{ffe}}$$

© 2023 Cadence Design Systems, Inc.

Component Statements

Model Definition

```
model modelName mvsg_gan parameter=value ...
```

Instance Definition

```
Name  d  g  s  b ModelName parameter=value ...
```

Instance Parameters

1	`m=1`	Multiplicity factor, number of devices in parallel.
2	`w=180.0e-6 m`	Width per Finger.
3	`l=250.0e-9 m`	Effective gate length.
4	`ngf=2`	Number of Fingers.
5	`trise=0 C`	Variability in device temperature.
6	`dtemp=0.0 C`	Device temperature offset from ambient.
7	`isnoisy=1`	Should device generate noise.

Model Parameters

1	`version=1.00`	Version number.
2	`tnom=27.0 deg C`	Reference temperature for the model.
3	`type=1`	nFET=1 pFET=-1.
4	`cg=4.00e-03 F/m`^{2}	Gate cap/area.
5	`cofsm=1.0e-9 F/m`	Gate - Source outer fringing cap/width.
6	`cofdm=1.0e-10 F/m`	Gate - Drain outer fringing cap/width.
7	`cofdsm=1.0e-10 F/m`	Source - Drain outer fringing cap/width.
8	`cofdsubm=0.0 F/m`	Sub - Drain outer fringing cap/width.

© 2023 Cadence Design Systems, Inc.

9	`cofssubm=0.0 F/m`	Sub - Source outer fringing cap/width.
10	`cofgsubm=0.0 F/m`	Sub - Gate outer fringing cap/width.
11	`rsh=150.0 Ohms/Sq`	2-DEG Sheet Resistance.
12	`rcs=800e-6 Ohms m`	Source contact resistance * Width.
13	`rcd=800e-6 Ohms m`	Drain contact resistance * Width.
14	`vx0=3.0e5 m/s`	Source injection velocity.
15	`mu0=0.135` m^2`/Vs`	Low-field mobility.
16	`beta=1.50`	Linear to saturation parameter.
17	`vto=(-2.72) V`	Threshold voltage.
18	`ss=0.120 V/dec`	Sub-threshold slope.
19	`delta1=16e-3`	DIBL Coefficient 1.
20	`delta2=0.0`	DIBL Coefficient 2.
21	`dibsat=10.0 V`	DIBL saturation Voltage.
22	`nd=0.0`	Punchthrough factor for subth slope.
23	`alpha=3.5`	Weak to strong inversion transition factor.
24	`lambda=0.0 1/V`	CLM parameter.
25	`vtheta=0.0 1/V`	Scattering: velocity reduction parameter with Vg.
26	`mtheta=0.0 1/V`	Scattering: mobility reduction parameter with Vg.
27	`vzeta=150e3 1/K`	vx0 dependence on temperature.
28	`vtzeta=(-0.4e-3) V/K`	vto dependence on temperature.
29	`epsilon=2.3`	Mobility dependence on temperature.
30	`rct1=0.0 1/K`	Linear Rsh and Rc temperature coefficient.
31	`rct2=0.0 1/K`^{2}	Quadratic Rsh and Rc temperature coefficient.
32	`flagres=0`	Flag parameter for resistor: resistor is chosen if flagres=1 or implicit transitor is chosen if flagres=0.
33	`lgs=3.0e-6 m`	Source access region (SAR) length parameter.
34	`vtors=(-650) V`	SAR threshold voltage.
35	`cgrs=5.0e-3 F/m`^{2}	SAR gate-cap/area.

© 2023 Cadence Design Systems, Inc.

36	vx0rs=100e3 m/s	SAR source injection velocity.
37	mu0rs=100e-3 m^2/Vs	SAR low-field mobility.
38	betars=1.00	SAR linear to saturation parameter.
39	delta1rs=100e-3	SAR DIBL Coefficient.
40	srs=0.100 V/dec	SAR Sub-threshold slope.
41	ndrs=0.0	SAR punchthrough factor for subth slope.
42	vthetars=0.0 1/V	SAR scattering: velocity reduction parameter with Vg.
43	mthetars=0.0 1/V	SAR scattering: mobility reduction parameter with Vg.
44	alphars=3.5	SAR weak to strong inversion transition factor.
45	lgd=4.85e-6 m	Drain access region (DAR) length parameter.
46	vtord=(-650) V	DAR threshold voltage.
47	cgrd=4.3e-3 F/m^2	DAR gate-cap/area.
48	vx0rd=100e3 m/s	DAR source injection velocity.
49	mu0rd=100e-3 m^2/Vs	DAR low-field mobility.
50	betard=1.00	DAR linear to saturation parameter.
51	delta1rd=0.35	DAR DIBL Coefficient.
52	srd=0.3 V/dec	DAR Sub-threshold slope.
53	ndrd=3.8	DAR punchthrough factor for subth slope.
54	vthetard=0.0 1/V	DAR scattering: velocity reduction parameter with Vg.
55	mthetard=0.0 1/V	DAR scattering: mobility reduction parameter with Vg.
56	alphard=3.5	DAR weak to strong inversion transition factor.
57	flagfp1=1	Flag parameter: GFP=1 or SFP=0.
58	lgfp1=0.0 m	FP Length.
59	vtofp1=(-44.5) V	FP threshold voltage.
60	cgfp1=2.0e-4 F/m^2	FP gate-cap/area.
61	flagfp1s=1	Flag parameter: cfp1s select=1 or cfp1s not select=0.

© 2023 Cadence Design Systems, Inc.

62	`cfp1s=1e-19 F/m`	FP (source-side) to source cap/width.
63	`ccfp1=0.9e-10 F/m`	Source or gate to drain (under FP) cap/width.
64	`cbfp1=0.0 F/m`	Body to drain (under FP) cap/width.
65	`vx0fp1=1.2e5 m/s`	FP source injection velocity.
66	`mu0fp1=0.2` m^2`/Vs`	FP low-field mobility.
67	`betafp1=1.00`	FP linear to saturation parameter.
68	`delta1fp1=0.0`	FP DIBL Coefficient.
69	`sfp1=3.2 V/dec`	FP Sub-threshold slope.
70	`ndfp1=0.0`	FP punchthrough factor for subth slope.
71	`vthetafp1=0.0 1/V`	FP scattering: velocity reduction parameter with Vg.
72	`mthetafp1=0.0 1/V`	FP scattering: mobility reduction parameter with Vg.
73	`alphafp1=1e-2`	FP weak to strong inversion transition factor.
74	`flagfp2=0`	Flag parameter: GFP=1 or SFP=0.
75	`lgfp2=0.0 m`	FP Length.
76	`vtofp2=(-74.5) V`	FP threshold voltage.
77	`cgfp2=1.0e-4 F/m`^{2}	FP gate-cap/area.
78	`flagfp2s=1`	Flag parameter: cfp1s select=1 or cfp1s not select=0.
79	`cfp2s=1e-19 F/m`	FP (source-side) to source cap/width.
80	`ccfp2=0.3e-10 F/m`	Source or gate to drain (under FP) cap/width.
81	`cbfp2=0.0 F/m`	Body to drain (under FP) cap/width.
82	`vx0fp2=1.2e5 m/s`	FP source injection velocity.
83	`mu0fp2=0.2` m^2`/Vs`	FP low-field mobility.
84	`betafp2=1.00`	FP linear to saturation parameter.
85	`delta1fp2=0.0`	FP DIBL Coefficient.
86	`sfp2=3.2 V/dec`	FP Sub-threshold slope.
87	`ndfp2=0.0`	FP punchthrough factor for subth slope.
88	`vthetafp2=0.0 1/V`	FP scattering: velocity reduction parameter with Vg.
89	`mthetafp2=0.0 1/V`	FP scattering: mobility reduction parameter with Vg.

© 2023 Cadence Design Systems, Inc.

90	`alphafp2=1e-2`	FP weak to strong inversion transition factor.
91	`flagfp3=0`	Flag parameter: GFP=1 or SFP=0.
92	`lgfp3=0.0 m`	FP Length.
93	`vtofp3=(-44.5) V`	FP threshold voltage.
94	`cgfp3=2.0e-4 F/m`^{2}	FP gate-cap/area.
95	`flagfp3s=1`	Flag parameter: cfp1s select=1 or cfp1s not select=0.
96	`cfp3s=1e-19 F/m`	FP (source-side) to source cap/width.
97	`ccfp3=0.9e-10 F/m`	Source or gate to drain (under FP) cap/width.
98	`cbfp3=0.0 F/m`	Body to drain (under FP) cap/width.
99	`vx0fp3=1.2e5 m/s`	FP source injection velocity.
100	`mu0fp3=0.2 m`^{2}`/Vs`	FP low-field mobility.
101	`betafp3=1.00`	FP linear to saturation parameter.
102	`delta1fp3=0.0`	FP DIBL Coefficient.
103	`sfp3=3.2 V/dec`	FP Sub-threshold slope.
104	`ndfp3=0.0`	FP punchthrough factor for subth slope.
105	`vthetafp3=0.0 1/V`	FP scattering: velocity reduction parameter with Vg.
106	`mthetafp3=0.0 1/V`	FP scattering: mobility reduction parameter with Vg.
107	`alphafp3=1e-2`	FP weak to strong inversion transition factor.
108	`flagfp4=0`	Flag parameter: GFP=1 or SFP=0.
109	`lgfp4=0.0 m`	FP Length.
110	`vtofp4=(-44.5) V`	FP threshold voltage.
111	`cgfp4=2.0e-4 F/m`^{2}	FP gate-cap/area.
112	`flagfp4s=1`	Flag parameter: cfp1s select=1 or cfp1s not select=0.
113	`cfp4s=1e-19 F/m`	FP (source-side) to source cap/width.
114	`ccfp4=0.9e-10 F/m`	Source or gate to drain (under FP) cap/width.
115	`cbfp4=0.0 F/m`	Body to drain (under FP) cap/width.
116	`vx0fp4=1.2e5 m/s`	FP source injection velocity.

© 2023 Cadence Design Systems, Inc.

117	`mu0fp4=0.2 m2/Vs`	FP low-field mobility.
118	`betafp4=1.00`	FP linear to saturation parameter.
119	`delta1fp4=0.0`	FP DIBL Coefficient.
120	`sfp4=3.2 V/dec`	FP Sub-threshold slope.
121	`ndfp4=0.0`	FP punchthrough factor for subth slope.
122	`vthetafp4=0.0 1/V`	FP scattering: velocity reduction parameter with Vg.
123	`mthetafp4=0.0 1/V`	FP scattering: mobility reduction parameter with Vg.
124	`alphafp4=1e-2`	FP weak to strong inversion transition factor.
125	`igmod=1`	Flag parameter for gate leakage 0=off, 1=on.
126	`rgsp=0.0 Ohms m`	Gate resistance * Width.
127	`vjg=1.1 V`	Gate diode cut in voltage.
128	`pg_param1=820e-3 1/V`	Something like 1/eta.
129	`pg_params=1.00 1/V`	G-S something like 1/eta*Vt.
130	`ijs=1.00e-12 A/m`	G-S reverse leakage current normalized to width.
131	`vgsats=1.00 V`	G-S high injection effect.
132	`fracs=0.5`	G-S fractional change in ideality factor due to high injection.
133	`alphags=10.0`	G-S high injection smoothing parameter.
134	`pg_paramd=1.00 1/V`	G-D something like 1/eta*Vt.
135	`ijd=1.00e-12 A/m`	G-D reverse leakage current normalized to width.
136	`vgsatd=1.00 V`	G-D high injection effect.
137	`fracd=0.5`	G-D fractional change in ideality factor due to high injection.
138	`alphagd=10.0`	G-D high injection smoothing parameter.
139	`pgsrecs=0.5`	G-S something like 1/eta for reverse recombination.
140	`irecs=1.0e-18 A/m`	G-S reverse leakage current normalized to width.

© 2023 Cadence Design Systems, Inc.

141	`vgsatqs=2.00 V`	G-S mimics depletion saturation.
142	`vbdgs=600 V`	G-S soft breakdown voltage of G-S diode.
143	`pbdgs=4.00 1/V`	G-S fitting parameter for breakdown: Something like 1/ eta*Vt.
144	`betarecs=2.00`	G-S linear to saturation parameter.
145	`kbdgates=00`	G-S fitting parameter to turn on the breakdown of G-S diode.
146	`pgsrecd=0.8`	G-D something like 1/eta for reverse recombination.
147	`irecd=2e-5 A/m`	G-D reverse leakage current normalized to width.
148	`vgsatqd=0.8 V`	G-D mimics depletion saturation.
149	`vbdgd=600 V`	G-D soft breakdown voltage of G-D diode.
150	`pbdgd=4.00 1/V`	G-D fitting parameter for breakdown: Something like 1/ eta*Vt.
151	`betarecd=0.25`	G-D linear to saturation parameter.
152	`kbdgated=00`	G-D fitting parameter to turn on the breakdown of G-D diode.
153	`rth=25 K/W`	Thermal resistance.
154	`cth=1e-4 s W/K`	Thermal capacitance.
155	`gmdisp=0`	Flag parameter for gm-dispersion 0=off, 1=on.
156	`taugmrf=1e-3 s`	gm-dispersion time constant.
157	`trapselect=0`	Select knob for charge trapping 0=off, 1=on.
158	`ctrap=1e-3 F`	DC-block capacitor.
159	`vttrap=230 V`	Trapping stress threshold voltage.
160	`taut=3e-5 s`	Trap time constant.
161	`alphat1=1e-4`	Trap coefficient 1 on bias stress.
162	`alphat2=21 V`	Trap coefficient 2 on bias stress.
163	`tempt=1e-4 1/K`	Temperature coefficient for trapping.
164	`noisemod=0`	Select knob for noise model 0=off, 1=on.
165	`shs=3.0`	G-S shot noise parameter.
166	`shd=3.0`	G-D shot noise parameter.

© 2023 Cadence Design Systems, Inc.

167	`kf=1.0e-4`	Flicker noise coefficient.
168	`af=2.0`	Flicker noise exponent.
169	`ffe=1.2`	Flicker noise exponent for frequency.
170	`minr=1.0e-3 Ω`	Minimum resistance.
171	`minl=1.0e-9 m`	Minimum length of access or FP regions for modeling them as transistors.
172	`minc=0.0 F`	Minimum capacitance.
173	`trise=0.0 C`	Temperature rise from ambient, alias of dtemp. It served as the default value of instance DTEMP.

Operating-Point Parameter

1	`trise=0 C`	Variability in device temperature.
2	`dtemp=0.0 C`	Device temperature offset from ambient.
3	`vgisi (V)`	Internal gate-source voltage.
4	`vdisi (V)`	Internal drain-source voltage.
5	`pdc (W)`	Total power dissipation from the device.
6	`idisi (A)`	Drain-to-source current in intrinsic transistor.
7	`igs (A)`	Gate-source gate-leakage current.
8	`igd (A)`	Gate-drain gate-leakage current.
9	`qgi (C)`	Intrinsic gate charge.
10	`qdi (C)`	Intrinsic drain charge.
11	`qsi (C)`	Intrinsic source charge.
12	`qbi (C)`	Intrinsic body charge.
13	`gmi (A/V)`	Intrinsic transconductance.
14	`gdsi (A/V)`	Intrinsic output-conductance.
15	`gmbsi (A/V)`	Intrinsic body-transconductance.
16	`cggi (F)`	Intrinsic gate-gate capacitance.
17	`cgdi (F)`	Intrinsic gate-drain capacitance.

© 2023 Cadence Design Systems, Inc.

18	`cgsi (F)`	Intrinsic gate-source capacitance.
19	`cgbi (F)`	Intrinsic gate-body capacitance.
20	`cdgi (F)`	Intrinsic drain-gate capacitance.
21	`cddi (F)`	Intrinsic drain-drain capacitance.
22	`cdsi (F)`	Intrinsic drain-source capacitance.
23	`cdbi (F)`	Intrinsic drain-body capacitance.
24	`csgi (F)`	Intrinsic source-gate capacitance.
25	`csdi (F)`	Intrinsic source-drain capacitance.
26	`cssi (F)`	Intrinsic source-source capacitance.
27	`csbi (F)`	Intrinsic source-body capacitance.
28	`cbgi (F)`	Intrinsic body-gate capacitance.
29	`cbdi (F)`	Intrinsic body-drain capacitance.
30	`cbsi (F)`	Intrinsic body-source capacitance.
31	`cbbi (F)`	Intrinsic body-body capacitance.
32	`cgs (F)`	Gate-to-source fringing capacitance.
33	`cgd (F)`	Gate-to-drain fringing capacitance.
34	`t_total_k (K)`	Actual device temperature in Kelvin.
35	`t_total_c (deg C)`	Actual device temperature in Celsius.
36	`t_delta_sh (K)`	Change in device temperature caused by self-heating.
37	`rs (Ω)`	Resistance of source access region.
38	`rd (Ω)`	Resistance of drain access region.
39	`per (W)`	Power at op point.

Parameter Index

In the following index, `I` refers to instance parameters, `M` refers to the model parameters section, `O` refers to the output parameters section, and `OP` refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the

© 2023 Cadence Design Systems, Inc.

description for that parameter. For example, a reference of `M-35` means the 35th model parameter.

af M-168	cofdsm M-7	lgfp2 M-75	sfp3 M-103
alpha M-23	cofdsubm M-8	lgfp3 M-92	sfp4 M-120
alphafp1 M-73	cofgsubm M-10	lgfp4 M-109	shd M-166
alphafp2 M-90	cofsm M-5	lgs M-33	shs M-165
alphafp3 M-107	cofssubm M-9	m I-1	srd M-52
alphafp4 M-124	csbi OP-27	minc M-172	srs M-40
alphagd M-138	csdi OP-25	minl M-171	ss M-18
alphags M-133	csgi OP-24	minr M-170	t_delta_sh OP-36
alphard M-56	cssi OP-26	mtheta M-26	t_total_c OP-35
alphars M-44	cth M-154	mthetafp1 M-72	t_total_k OP-34
alphat1 M-161	ctrap M-158	mthetafp2 M-89	taugmrf M-156
alphat2 M-162	delta1 M-19	mthetafp3 M-106	taut M-160
beta M-16	delta1fp1 M-68	mthetafp4 M-123	tempt M-163
betafp1 M-67	delta1fp2 M-85	mthetard M-55	tnom M-2
betafp2 M-84	delta1fp3 M-102	mthetars M-43	trapselect M-157
betafp3 M-101	delta1fp4 M-119	mu0 M-15	trise I-5
betafp4 M-118	delta1rd M-51	mu0fp1 M-66	trise M-173
betard M-50	delta1rs M-39	mu0fp2 M-83	trise OP-1
betarecd M-151	delta2 M-20	mu0fp3 M-100	type M-3

© 2023 Cadence Design Systems, Inc.

betarecs M-144
betars M-38
cbbi OP-31
cbdi OP-29
cbfp1 M-64
cbfp2 M-81
cbfp3 M-98
cbfp4 M-115
cbgi OP-28
cbsi OP-30
ccfp1 M-63
ccfp2 M-80
ccfp3 M-97
ccfp4 M-114
cdbi OP-23
cddi OP-21
cdgi OP-20
cdsi OP-22
cfp1s M-62
cfp2s M-79
cfp3s M-96
dibsat M-21
dtemp I-6
dtemp OP-2
epsilon M-29
ffe M-169
flagfp1 M-57
flagfp1s M-61
flagfp2 M-74
flagfp2s M-78
flagfp3 M-91
flagfp3s M-95
flagfp4 M-108
flagfp4s M-112
flagres M-32
fracd M-137
fracs M-132
gdsi OP-14
gmbsi OP-15
gmdisp M-155
gmi OP-13
idisi OP-6
mu0fp4 M-117
mu0rd M-49
mu0rs M-37
nd M-22
ndfp1 M-70
ndfp2 M-87
ndfp3 M-104
ndfp4 M-121
ndrd M-53
ndrs M-41
ngf I-4
noisemod M-164
pbdgd M-150
pbdgs M-143
pdc OP-5
pg_param1 M-128
pg_paramd M-134
pg_params M-129
pgsrecd M-146
pgsrecs M-139
pwr OP-39
vbdgd M-149
vbdgs M-142
vdisi OP-4
version M-1
vgisi OP-3
vgsatd M-136
vgsatqd M-148
vgsatqs M-141
vgsats M-131
vjg M-127
vtheta M-25
vthetafp1 M-71
vthetafp2 M-88
vthetafp3 M-105
vthetafp4 M-122
vthetard M-54
vthetars M-42
vto M-17
vtofp1 M-59
vtofp2 M-76
vtofp3 M-93

© 2023 Cadence Design Systems, Inc.

cfp4s M-113
cg M-4
cgbi OP-19
cgd OP-33
cgdi OP-17
cgfp1 M-60
cgfp2 M-77
cgfp3 M-94
cgfp4 M-111
cggi OP-16
cgrd M-47
cgrs M-35
cgs OP-32
cgsi OP-18
cofdm M-6
igd OP-8
igmod M-125
igs OP-7
ijd M-135
ijs M-130
irecd M-147
irecs M-140
isnoisy I-7
kbdgated M-152
kbdgates M-145
kf M-167
l I-3
lambda M-24
lgd M-45
lgfp1 M-58
qbi OP-12
qdi OP-10
qgi OP-9
qsi OP-11
rcd M-13
rcs M-12
rct1 M-30
rct2 M-31
rd OP-38
rgsp M-126
rs OP-37
rsh M-11
rth M-153
sfp1 M-69
sfp2 M-86
vtofp4 M-110
vtord M-46
vtors M-34
vttrap M-159
vtzeta M-28
vx0 M-14
vx0fp1 M-65
vx0fp2 M-82
vx0fp3 M-99
vx0fp4 M-116
vx0rd M-48
vx0rs M-36
vzeta M-27
w I-2

© 2023 Cadence Design Systems, Inc.

© 2023 Cadence Design Systems, Inc.

55

Josephson Junction Model (jj)

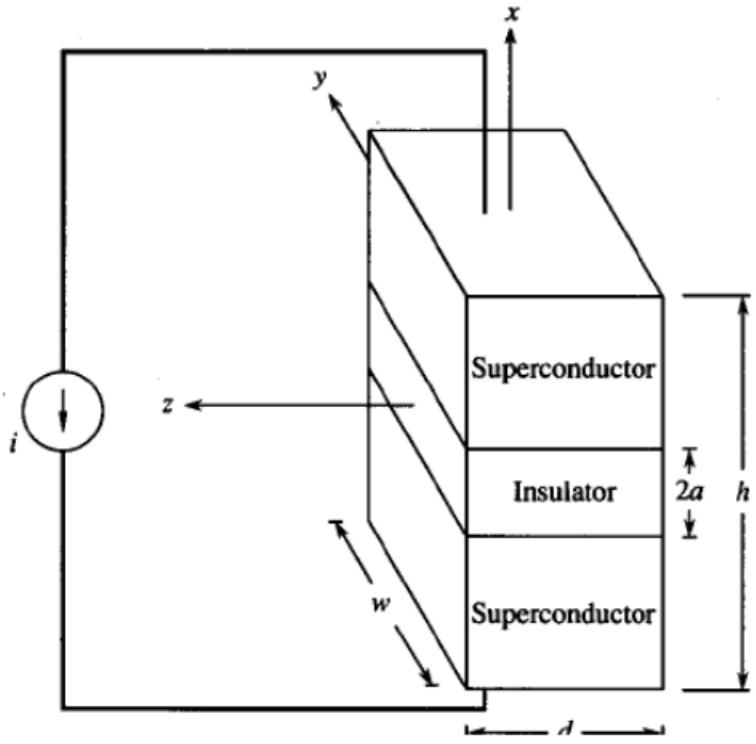
This chapter contains the following information about the Josephson Junction model:

- Model Overview
- Model Equations
- Component Statements

© 2023 Cadence Design Systems, Inc.

Model Overview

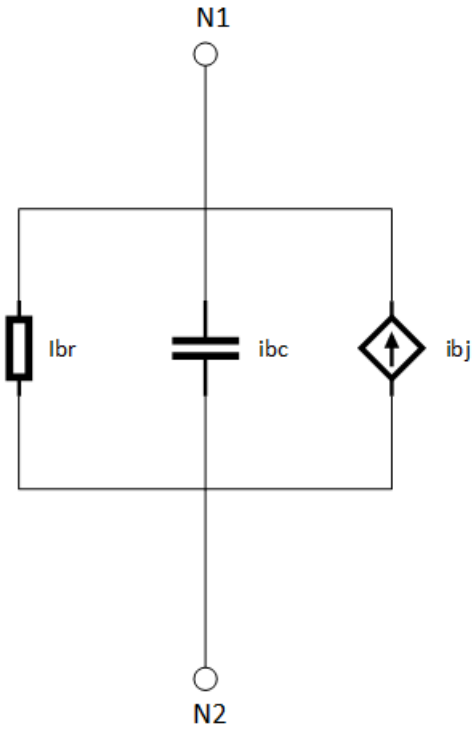
A Josephson junction is made by sandwiching a thin layer of a non-superconducting material between two layers of superconducting material. The devices are named after Brian Josephson, who predicted in 1962 that pairs of superconducting electrons could "tunnel" right through the non-superconducting barrier from one superconductor to another.



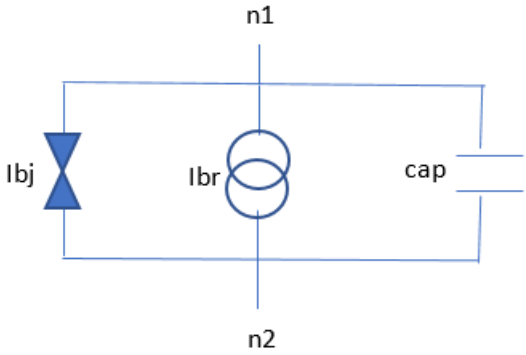
Josephson Junction model is for transient analysis only.

The topology is shown in the figure below.

© 2023 Cadence Design Systems, Inc.



Equivalent Circuit



Related Topics

Josephson Junction Model (jj)

© 2023 Cadence Design Systems, Inc.

Model Equations

(55-1)

$$Vj = V(n1) - V(n2)$$

$$scale = aream \times mfactor$$

$$ibc = cap \times \frac{dVj}{dt}$$

When `cct =1`,

(55-2)

$$ibj = scale \times icrit \times \sin\left(idt\left(\left(\frac{Vj}{3.29 \times 10^{-6}} \right), ic_{phase} \right) \right)$$

When `cct = 0`,

(55-3)

$$ibj = 0$$

When `cct=1`, Supercurrent Ibj has following expression:

(55-4)

$I_{bj} = icrit \times \sin(\phi)$, when $pijj = 0$.

and,

$I_{bj} = -icrit \times \sin(\phi)$, when $pijj \neq 0$.

Where,

© 2023 Cadence Design Systems, Inc.

(55-5)

$$\phi = ic_{phase} + \int_0^t \left(\frac{V_j}{\phi_0 - 2pi} \right) dt$$

and $\phi_0 - 2pi$ is constant.

When `rtype=1`, there is quasiparticle current `Ibr`. First part of the current has following expression:

(55-6)

$$Ibr1 = \frac{Vj}{rsub} \qquad \text{when,} \quad |vj| \le vgap - dv2$$

$$Ibr1 = \frac{Vj}{|Vj|} \cdot \left(i1 + (i2 - i1) \cdot \frac{|Vj| - Vgap + dv2}{delv} \right) \qquad \text{when,} \quad |vj| < vgap + dv2$$

$$Ibr1 = \frac{Vj}{|Vj|} \cdot \left(\frac{icrit}{icfct} + \frac{|Vj| - Vgap - dv2}{rnorm} \right) \qquad \text{other}$$

where, $dv2 = \frac{delv}{2.0}$, $i1 = \frac{vgap - dv2}{rsub}$ and $i2 = \frac{icrit}{icfct}$.

When `vshunt>0`, `Ibr` also considers another component `Ibr2`:

(55-7)

$$Ibr2 = \left(\frac{icrit}{vshunt} - \frac{1}{rsub} \right) \cdot Vj$$

Thus, the total quasiparticle current is:

```
Ibr = Ibr1 + Ibr2
```


© 2023 Cadence Design Systems, Inc.

Related Topics

Josephson Junction Model (jj)

© 2023 Cadence Design Systems, Inc.

Component Statements

Instance

Instance Syntax

```
Name  n1  n2 ModelName parameter=value ...
```

Instance Parameters

ic_phase=0	Initial condition phase.
phi=0	Initial condition phase.
ics=1e-3	Scaled critical current.
area=1.0	IC scale factor.
m=1.0	Multiplicity factor (number of DIODEs in parallel).

Model

Model Syntax

```
model modelName jj parameter=value ...
```

Model Parameters

pijj=0	Instance is a PI junction.
rtype=1	Quasiparticle current model.
cct=1	Critical current model.
tsfactor=0.2	Maximum phase step in radians.
icrit=1.0e-3	Critical current for unit area
cap=70e-12	Capacitance for unit area.
cmu=0.0	Capacitance scaling factor.

© 2023 Cadence Design Systems, Inc.

`vg=(2.8 1.0e-3)`	Gap voltage.
`vgap=2.8 1.0e-3`	Gap voltage.
`delv=(0.08 1.0e-3)`	Gap width.
`vm=16e-3`	Ic * subgap resistance.
`r0=16`	Subgap resistance.
`rsub=75.0`	Subgap resistance for unit area.
`icrn=1.6e-3`	Ic * normal resistance.
`rn=1.6`	Normal resistance.
`rnorm=1.6`	Normal resistance for unit area.
`vshunt=0`	Ic * shunt resistance voltage.
`gmu=0.0`	Conductance scaling factor.
`icfct=0.78539816339744830962`	Ic to Istep ratio.
`icfct=PI/4`	Ratio of critical current to quasiparticle current at gap.
`version=1.04`	Model version.
`vdpbak=7.0e-4`	Dropback voltage.
`dcphasemode=0`	Phase mode DC analyses.
`use_2pi=0`	Flag used to scale the phase into [0, 2pi], default as 0.
`enable_dcres=0`	Flag used to load the dc resistance. Default is `0`.

Operating-Point Parameters

`ibj (A)`	Junction branch current.
`qbc (C)`	Capacitor branch charge.
`ibr (A)`	Resistor branch current.
`op_phi`	Current phase.

Related Topics

Josephson Junction Model (jj)

© 2023 Cadence Design Systems, Inc.

56

LUTSOI Model

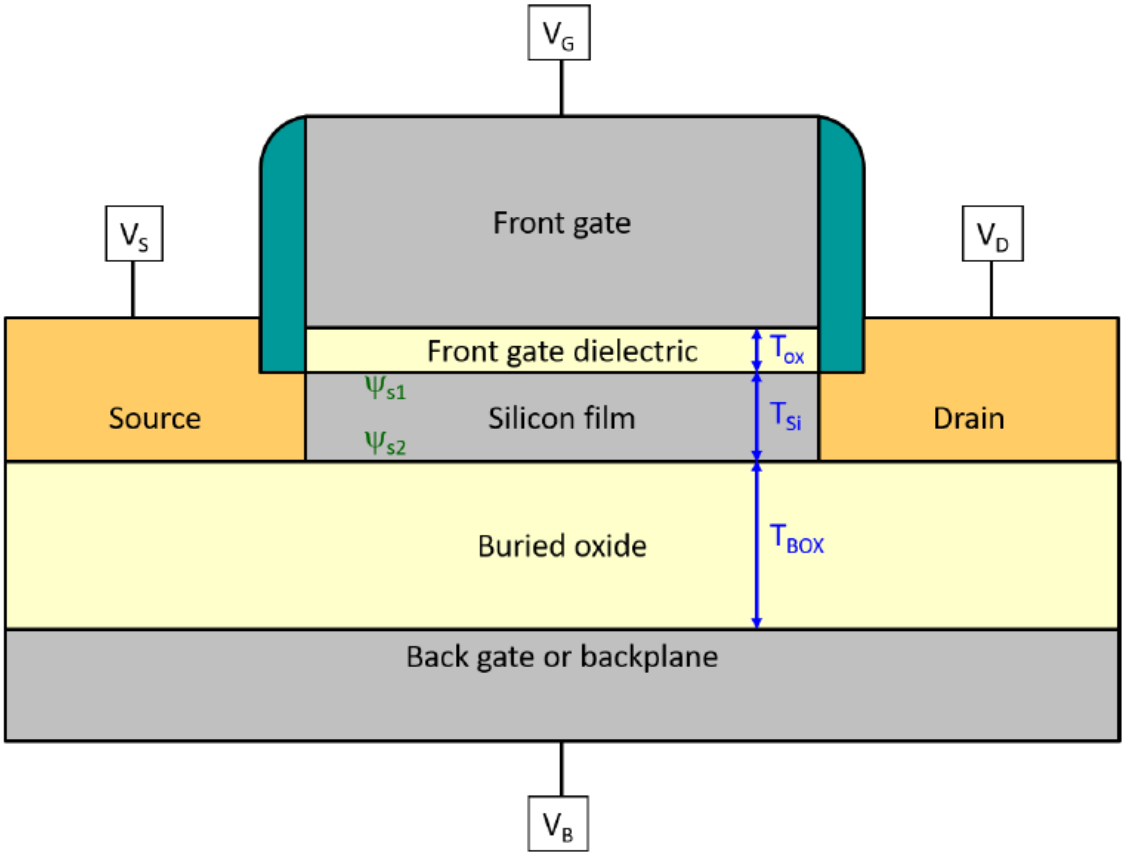
LUTSOI is a compact model dedicated to Fully-Depleted on Silicon-On-Insulator (FDSOI) technologies with low-doped channel. For more information, please refer to lutsoi model manual or contact info@cadence.com.

Model parameter "version" only accepts real number value, like 102.40 for version=102.4.0. The available versions are 102.40(102.4.0), 102.50(102.5.0), 102.60(102.6.0) and, 102.70(102.7.0).

This device is supported within altergroups.

© 2023 Cadence Design Systems, Inc.

The following figures illustrated the device architecture of this model.



It is a schematic cross-section of a FDSOI transistor, describing the characteristic thicknesses and the surface potentials at the front (Ψ_{s1}) and back (Ψ_{s2}) interfaces.

This chapter contains the following information about the LUTSOI model:

- Model Structure
- Version Update and Enhancements
  - L-UTSOI 102.7 Enhancements
  - L-UTSOI 102.6 Enhancements
- Geometrical dependences, stress effects and junction asymmetry
  - Scaling Equations
  - Stress model for SWSTRESS = 1
  - Stress model for SWSTRESS = 2

© 2023 Cadence Design Systems, Inc.

- Asymmetric junctions
- Model Equations
  - Internal parameters including temperature dependences
  - Terminal voltage conditioning
  - Backplane depletion
  - Channel current
  - Gate current, intrinsic charges and overlap related variables
  - Gate current
  - Impact ionization current
  - Charge model
  - Self-heating
  - Noise model
  - Total currents and charges
- Component Statements

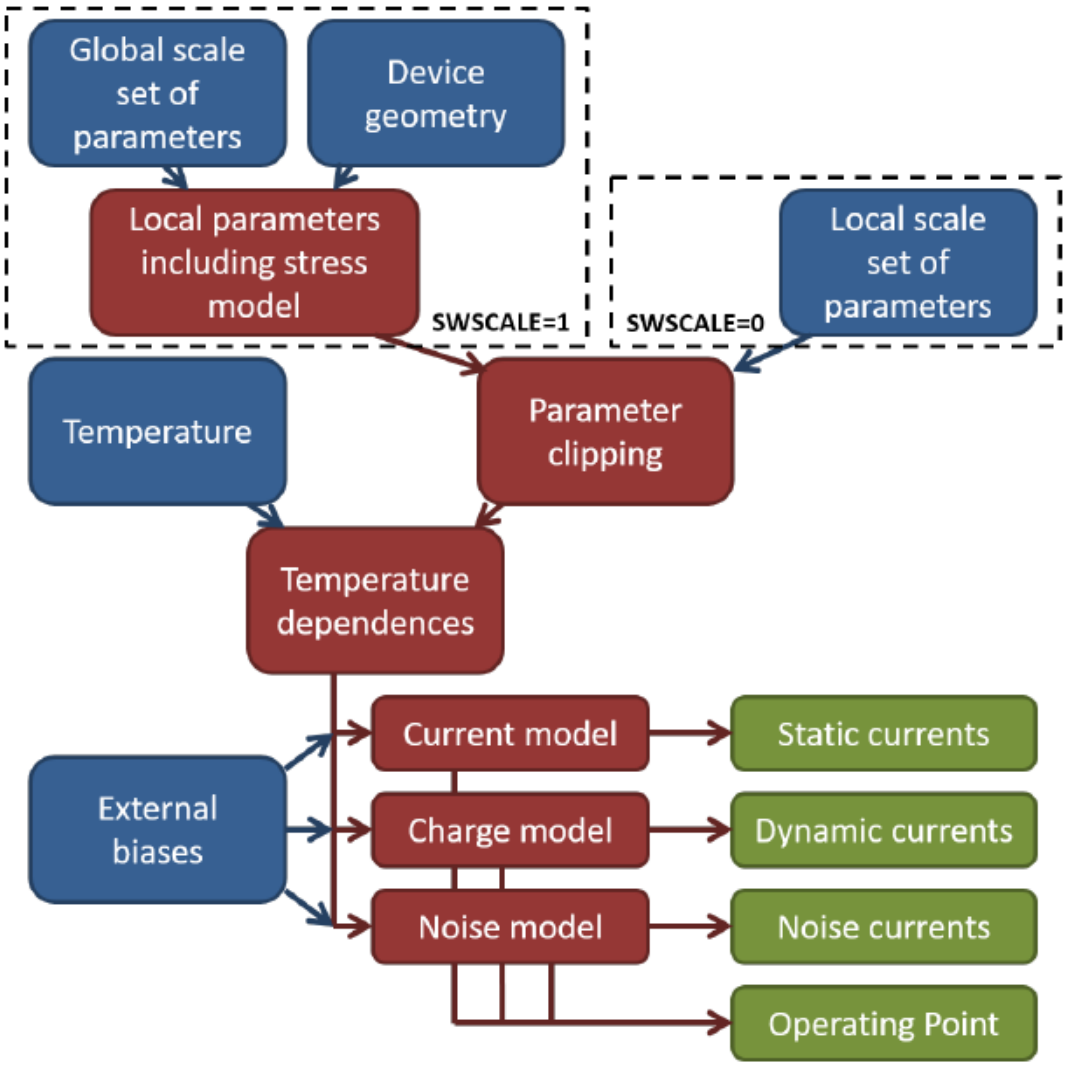
Model Structure

The structure is based on a hierarchical construction featuring two levels of parameter set:

- A local mode, in which the knowledge of the device geometry (channel length and width) is not needed. In this mode, the local parameter values are directly obtained from the model cards.
- A global mode, in which the local parameters are computed from the global model card and the device geometry through scaling laws (see Scaling Equations). The computed local parameters are then used to compute the model equations. In this mode, some local parameters can also be modified according to the stress model (see Stress model for SWSTRESS = 1 and Stress model for SWSTRESS = 2).

© 2023 Cadence Design Systems, Inc.

The following figure depicts the model structure.



Version Update and Enhancements

L-UTSOI 102.7 Enhancements

The 102.7 version of L-UTSOI includes the following updates:

- The following model parameters are added:
  - SWCRYO is added as flag for poly-depletion model

© 2023 Cadence Design Systems, Inc.

  - TMIN is added as minimum temperature.
  - ATMIN is added as minimum temperature slope.
  - BTMIN is added as minimum temperature smoothing parameter.
- The following output parameters are added:
  - IAVL is added as substrate current due to weak avelanche.
- When initializeModel, it uses SWCRYO to control different calculation of TKD.
- The change on op ouput, about "neff_op", "xth_1D_op", "e1_op", "e2_op", "x1sat_op", "x2sat_op".
- The calculation change about local parameters "neff", "neff_poly", "neff_sub","xb_sub", "dVfbpdep" , "xg10", "xg20", "xg20shift".
- Uses SWCRYO to control different calculation of "e1", "e2" in the section "Quantum mechanical corrections below threshold".
- Uses SWCRYO to control different calculation of "xg1x", "xg2x" in the section "Short channel effects".
- Change the calculation about parameter "frscsi" in the section "Mobility attenuation and series resistance at source side".
- Change the calculation about parameter "x_m" in the section "Gate-channel component of gate current".
- Change the flag about "xg1x" in the section "Source/drain partitioning of gate-channel current".
- Change the calculation about parameter "temp" in the section "Outer fringe and overlaps charges".

L-UTSOI 102.6 Enhancements

The 102.6 version of L-UTSOI includes the following updates:

1. When model parameter SWNQS is set to 1 or 0, the NQS effect is open or closed, respectively.
2. In NQS model, the following parameters are added to run the evaluation:

- KDRIFT is added as drift component parameter.
- KDIFF is added as diffusion component parameter.
- FRACINV is added as fraction of inversion charge for the second pole.

© 2023 Cadence Design Systems, Inc.

- KFRACINV is added as second pole frequency coefficient.
- KDRIFTO is added as geometry-independent drift component parameter.
- KDRIFTL is added as length dependence of KDRIFT.
- KDIFFO is added as geometry-independent diffusion component parameter.
- KDIFFL is added as length dependence of KDIFF.
- FRACINVO is added as geometry-independent fraction of inversion charge for the second pole.
- KFRACINVO is added as geometry-independent second pole frequency coefficient of the NQS transition.

Geometrical dependences, stress effects and junction asymmetry

Scaling Equations

Effective dimensions

Introduction of the number of fingers.

$$W_f = W/\mathbf{NF}$$

$$A_{source,f} = \mathbf{ASOURCE}/\mathbf{NF}$$

$$A_{drain,f} = \mathbf{ADRAIN}/\mathbf{NF}$$

$$P_{source,f} = \mathbf{PSOURCE}/\mathbf{NF}$$

$$P_{drain,f} = \mathbf{PDRAIN}/\mathbf{NF}$$

$$Mult_f = \mathbf{MULT} \times \mathbf{NF}$$

© 2023 Cadence Design Systems, Inc.

Effective length and width for current model.

$$L_{EN} = 10^{-6}$$

$$W_{EN} = 10^{-6}$$

$$\Delta L_{PS} = \mathbf{LVARO}\left(1 + \mathbf{LVARL}\frac{L_{EN}}{L}\right)\left(1 + \mathbf{LVARW}\frac{W_{EN}}{W_f}\right)$$

$$\Delta W_{OD} = \mathbf{WVARO}\left(1 + \mathbf{WVARL}\frac{L_{EN}}{L}\right)\left(1 + \mathbf{WVARW}\frac{W_{EN}}{W_f}\right)$$

$$L_E = L + \Delta L_{PS} - 2 \times \mathbf{LAP}$$

$$W_E = W_f + \Delta W_{OD} - 2 \times \mathbf{WOT}$$

Effective length and width for charge model.

$$L_{E,CV} = L + \Delta L_{PS} - 2 \times \mathbf{LAP} + \mathbf{DLQ}$$

$$W_{E,CV} = W_f + \Delta W_{OD} - 2 \times \mathbf{WOT} + \mathbf{DWQ}$$

Physical length and width for parasitic charges and self-heating.

$$L_{phy} = L + \Delta L_{PS}$$

$$W_{phy} = W_f + \Delta W_{OD}$$

Process parameters

TOXE = TOXEO

TSI = TSIO

XGE = XGEO

TBOX = TBOXO

© 2023 Cadence Design Systems, Inc.

NCH = NCHO

NSUB = NSUBO

CT = CTO

TOXP = TOXPO

NOV = NOVO

NOVD = NOVDO

$$\mathbf{VFB} = \mathbf{VFBO} + \frac{\mathbf{VFBL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{VFBLEXP}}}{1 + \mathbf{VFBL2}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{VFBLEXP2}}} + \mathbf{VFBW}\frac{W_{EN}}{W_E} + \mathbf{VFBLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}$$

$$\mathbf{VFBB} = \mathbf{VFBBO} + \mathbf{VFBLBO} \times \frac{\mathbf{TBOX}}{\mathbf{TOXE}} \times \frac{\mathbf{VFBL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{VFBLEXP}}}{1 + \mathbf{VFBL2}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{VFBLEXP2}}}$$

$$\mathbf{STVFB} = \mathbf{STVFBO}\left(1 + \mathbf{STVFBL}\frac{L_{EN}}{L_E}\right) \left(1 + \mathbf{STVFBW}\frac{W_{EN}}{W_E}\right)\left(1 + \mathbf{STVFBLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{NP} = \mathbf{NPO} \times \mathrm{MAX}\left(10^{-6}, 1 + \mathbf{NPL} \cdot \frac{L_{EN}}{L_E}\right)$$

Gate to interface coupling parameters

CICF = CICFO

© 2023 Cadence Design Systems, Inc.

CIC = CICO

$$\lambda_{2D} = \sqrt{\frac{\epsilon_{Si}(1-\mathbf{XGE}) + \epsilon_{Ge}\mathbf{XGE}}{\epsilon_{ox}}} \times \mathbf{TSI} \times (\mathbf{TOXE} + 4 \cdot 10^{-10})$$

$$\mathbf{PSCE} = 2 \times \mathbf{PSCEL} \left(\frac{\lambda_{2D}}{L_E}\right)^{\mathbf{PSCELEXP}} \left(1 + \mathbf{PSCEW}\frac{W_{EN}}{W_E}\right)$$

PSCEB = PSCEBO

NSDDC = NSDDCO

PSCEDLB = PSCEDLBO

PNCE = PNCEW $\frac{W_{EN}}{W_E}$

Drain Induced Barrier Lowering parameters

$$\mathbf{CF} = \mathbf{CFL} \left(\frac{\lambda_{2D}}{L_E}\right)^{\mathbf{CFLEXP}} \left(1 + \mathbf{CFW}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{CFB} = \mathbf{CFBO}$$

$$\mathbf{STCF} = \mathbf{STCFL} \left(\frac{\lambda_{2D}}{L_E}\right)^{\mathbf{CFLEXP}} \left(1 + \mathbf{CFW}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{CFD} = \mathbf{CFDO}$$

$$\mathbf{CFDL} = \frac{\mathbf{CFDLL}\frac{L_{EN}}{L_E}}{\max\left(1 + \mathbf{CFDLW}\frac{W_{EN}}{W_E}, 10^{-3}\right)}$$

$$\mathbf{CFDLB} = \mathbf{CFDLBO}$$

© 2023 Cadence Design Systems, Inc.

Mobility parameters

$$L_{P1eff} = \mathbf{LP1} \times \max\left(1 + \mathbf{LP1W}\frac{W_{EN}}{W_E}, 10^{-3}\right)$$

$$G_{PE} = \max\left(1 + \mathbf{FBET1}\left(1 + \mathbf{FBET1W}\frac{W_{EN}}{W_E}\right)\frac{1 - \exp\left(-L_E/L_{P1eff}\right)}{L_E/L_{P1eff}} + \mathbf{FBET2} \times \frac{1 - \exp\left(-L_E/L_{P2}\right)}{L_E/L_{P2}}, 10^{-6}\right)$$

$$G_{WE} = \max\left(1 + \mathbf{BETW1}\frac{W_{EN}}{W_E} + \mathbf{BETW2}\frac{W_{EN}}{W_E}\ln\left(1 + \frac{W_E}{\mathbf{WBET}}\right), 10^{-6}\right)$$

$$G_E = \mathbf{UO}\frac{G_{WE}}{G_{PE}}$$

In this model, UO is integrated into GE. This changes the signification of the THESAT related global parameters, as detailed in the velocity saturation parameters part.

$$\mathbf{BETN} = G_E\frac{W_E}{L_E}$$

$$\mathbf{BETNB} = \mathbf{BETNBO}$$

$$\mathbf{STBET} = \mathbf{STBETO}\left(1 + \mathbf{STBETL}\frac{L_{EN}}{L_E}\right)\left(1 + \mathbf{STBETW}\frac{W_{EN}}{W_E}\right)\left(1 + \mathbf{STBETLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{CS} = \left(\mathbf{CSO} + \mathbf{CSL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{CSLEXP}}\right)\left(1 + \mathbf{CSW}\frac{W_{EN}}{W_E}\right)\left(1 + \mathbf{CSLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{CSFI} = \mathbf{CSFIO}$$

$$\mathbf{CSBI} = \mathbf{CSBIO}$$

© 2023 Cadence Design Systems, Inc.

$$\mathbf{STCS} = \mathbf{STCSO}\left(1 + \mathbf{STCSL}\frac{L_{EN}}{L_E}\right)\left(1 + \mathbf{STCSW}\frac{W_{EN}}{W_E}\right)\left(1 + \mathbf{STCSLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{THECS} = \mathbf{THECSO}$$

$$\mathbf{STTHECS} = \mathbf{STTHECSO}$$

$$\mathbf{CSTHR} = \mathbf{CSTHRO}$$

$$\mathbf{CSTHRB} = \mathbf{CSTHRBO}$$

$$\mathbf{MUE} = \mathbf{MUEO}$$

$$\mathbf{STMUE} = \mathbf{STMUEO}$$

$$\mathbf{THEMU} = \mathbf{THEMUO}$$

$$\mathbf{STTHEMU} = \mathbf{STTHEMUO}$$

$$\mathbf{XCOR} = \left(\mathbf{XCORO} + \mathbf{XCORL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{XCORLEXP}}\right)\left(1 + \mathbf{XCORW}\frac{W_{EN}}{W_E}\right)\left(1 + \mathbf{XCORLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{XCORB} = \mathbf{XCORBO}$$

$$\mathbf{STXCOR} = \mathbf{STXCORO}$$

$$\mathbf{FETA} = \mathbf{FETAO}$$

© 2023 Cadence Design Systems, Inc.

Series resistance parameters

$$\mathbf{RS} = \mathbf{RSW1}\frac{W_{EN}}{W_E}\left(1 + \mathbf{RSW2}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{RSIG} = \mathbf{RSIGO}$$

$$\mathbf{STRS} = \mathbf{STRS}$$

$$\mathbf{RSG} = \mathbf{RSGO}$$

$$\mathbf{THERSG} = \mathbf{THERSGO}$$

$$\mathbf{RSB} = \mathbf{RSBO}$$

Velocity saturation parameters

$$\mathbf{THESAT} = G_E\left(\mathbf{THESATO} + \mathbf{THESATL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{THESATLEXP}}\right)\left(1 + \mathbf{THESATW}\frac{W_{EN}}{W_E}\right)\left(1 + \mathbf{THESATLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

Since **UO** has been included in GE (see (3.48)), **THESATL** is, in L-UTSOI, closely related to the saturation velocity itself.

$$\mathbf{STTHESAT} = \mathbf{STTHESATO}\left(1 + \mathbf{STTHESATL}\frac{L_{EN}}{L_E}\right)\left(1 + \mathbf{STTHESATW}\frac{W_{EN}}{W_E}\right)\left(1 + \mathbf{STTHESATLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{THESATG} = \mathbf{THESATGO}$$

$$\mathbf{THESATB} = \mathbf{THESATBO}$$

© 2023 Cadence Design Systems, Inc.

Saturation and Channel Length Modulation parameters

$$\mathbf{AX} = \frac{\mathbf{AXO}}{1 + \mathbf{AXL}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{AXLEXP}} \Big/ \left(1 + \mathbf{AXL2}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{AXLEXP2}}\right)}$$

$$\mathbf{ALP} = \frac{\mathbf{ALPL1}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{ALPLEXP}}}{1 + \mathbf{ALPL2}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{ALPLEXP2}}}\left(1 + \mathbf{ALPW}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{ALP1} = \frac{\mathbf{ALP1L1}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{ALP1LEXP}}}{1 + \mathbf{ALP1L2}\left(\frac{L_{EN}}{L_E}\right)^{\mathbf{ALP1LEXP2}}}\left(1 + \mathbf{ALP1W}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{ALPB} = \mathbf{ALPBO}$$

$$\mathbf{VP} = \mathbf{VPO}$$

$$\mathbf{VPG} = \mathbf{VPGO}$$

Gate current parameters

$$\mathbf{GCO} = \mathbf{GCOO}$$

$$\mathbf{IGINV} = \mathbf{IGINVLW}\frac{L_E}{L_{EN}}\frac{W_E}{W_{EN}}$$

$$\mathbf{IGOVINV} = \mathbf{IGOVINVW}\frac{W_E}{W_{EN}}$$

$$\mathbf{IGOVINVD} = \mathbf{IGOVINVDW}\frac{W_E}{W_{EN}}$$

$$\mathbf{IGOVACC} = \mathbf{IGOVACCW}\frac{W_E}{W_{EN}}$$

$$\mathbf{IGOVACCD} = \mathbf{IGOVACCDW}\frac{W_E}{W_{EN}}$$

© 2023 Cadence Design Systems, Inc.

$$\mathbf{STIG} = \mathbf{STIGO}$$

$$\mathbf{GC2CH} = \mathbf{GC2CHO}$$

$$\mathbf{GC3CH} = \mathbf{GC3CHO}$$

$$\mathbf{GC2OVINV} = \mathbf{GC2OVINVO}$$

$$\mathbf{GC3OVINV} = \mathbf{GC3OVINVO}$$

$$\mathbf{GC2OVACC} = \mathbf{GC2OVACCO}$$

$$\mathbf{GC3OVACC} = \mathbf{GC3OVACCO}$$

$$\mathbf{GCDOV} = \mathbf{GCDOVL}\frac{L_{EN}}{L_E}$$

$$\mathbf{GCVDOV} = \mathbf{GCVDOVO}$$

$$\mathbf{CHIB} = \mathbf{CHIBO}$$

$$\mathbf{NIGINV} = \mathbf{NIGINVO}$$

$$\mathbf{FNOVINV} = \mathbf{FNOVINVW}\frac{W_E}{W_{EN}}$$

$$\mathbf{FNOVINVD} = \mathbf{FNOVINVDW}\frac{W_E}{W_{EN}}$$

$$\mathbf{GCOVINVFN} = \mathbf{GCOVINFNO}$$

$$\mathbf{STIGFN} = \mathbf{STIGFNO}$$

© 2023 Cadence Design Systems, Inc.

Gate Induced Drain/Source Leakage (GIDL/GISL) parameters

$$\mathbf{AGIDL} = \mathbf{AGIDLO} + \mathbf{AGIDLW}\frac{W_E}{W_{EN}}$$

$$\mathbf{AGIDLD} = \mathbf{AGIDLDO} + \mathbf{AGIDLDW}\frac{W_E}{W_{EN}}$$

For gate currents, GIDL/GISL currents are not linked with LOVO in L-UTSOI.

$$\mathbf{BGIDL} = \mathbf{BGIDLO}$$

$$\mathbf{BGIDLD} = \mathbf{BGIDLDO}$$

$$\mathbf{STBGIDL} = \mathbf{STBGIDLO}$$

$$\mathbf{STBGIDLD} = \mathbf{STBGIDLDO}$$

$$\mathbf{CGIDL} = \mathbf{CGIDLO}$$

$$\mathbf{CGIDLD} = \mathbf{CGIDLDO}$$

$$\mathbf{DGIDL} = \mathbf{DGIDLO} + \mathbf{DGIDLL}\frac{L_{EN}}{L_E}$$

$$\mathbf{DGIDLD} = \mathbf{DGIDLDO} + \mathbf{DGIDLDL}\frac{L_{EN}}{L_E}$$

© 2023 Cadence Design Systems, Inc.

Impact Ionization Parameters

$$\mathbf{A1} = \mathbf{A1O}\left(1 + \mathbf{A1L}\frac{L_{EN}}{L_E}\right)\left(1 + \mathbf{A1W}\frac{W_{EN}}{W_E}\right)$$

$$\mathbf{A2} = \mathbf{A2O}$$

$$\mathbf{STA2} = \mathbf{STA2O}$$

$$\mathbf{A3} = \mathbf{A3O}\left(1 + \mathbf{A3L}\frac{L_{EN}}{L_E}\right)\left(1 + \mathbf{A3W}\frac{W_{EN}}{W_E}\right)$$

Charge model parameters

$$\mathbf{AREAQ} = L_{E,CV}W_{E,CV}$$

$$\mathbf{CGBOV} = \mathbf{CGBOVO} + \mathbf{CGBOVL}\frac{L_{phy}}{L_{EN}}$$

$$\mathbf{NSDAC} = \mathbf{NSDACO}$$

$$\mathbf{FIF} = \mathbf{FIFW}\frac{W_{E,CV}}{W_{EN}}$$

$$\mathbf{FSCEAC} = \mathbf{FSCEACO}$$

$$\mathbf{COV} = \epsilon_{ox}\frac{W_{E,CV}}{\mathbf{TOXE}}\mathbf{LOVO}$$

$$\mathbf{COVD} = \epsilon_{ox}\frac{W_{E,CV}}{\mathbf{TOXE}}\mathbf{LOVDO}$$

$$\mathbf{COVDL} = \frac{\mathbf{COVDLO}}{\max\left(1 + \mathbf{COVDLW}\frac{W_{EN}}{W_{E,CV}}, 10^{-3}\right)}$$

$$\mathbf{COVDLB} = \mathbf{COVDLBO}$$

© 2023 Cadence Design Systems, Inc.

$$\mathbf{DVFBOV} = \mathbf{DVFBOVO}$$

$$\mathbf{CFR} = \mathbf{CFRO} + \mathbf{CFRW}\frac{W_{phy}}{W_{EN}}$$

$$\mathbf{CFRD} = \mathbf{CFRDO} + \mathbf{CFRDW}\frac{W_{phy}}{W_{EN}}$$

$$\mathbf{CSD} = \mathbf{CSDO}\left(\epsilon_{Si}(1-\mathbf{XGE}) + \epsilon_{Ge}\mathbf{XGE}\right)\mathbf{TSI}\frac{W_E}{L_E}$$

$$\mathbf{CSDBP} = \mathbf{CSDBPO}$$

Self-heating parameters

$$z_{th} = \exp\left(-\frac{\mathbf{SD}+L}{\mathbf{LAMBTHO}}\right)$$

$$n_{th} = 1 + 2\times\mathbf{FTHO}\times z_{th}\frac{1-z_{th}-\left(1-z_{th}{}^{\mathbf{NF}}\right)/\mathbf{NF}}{(1-z_{th})^2}$$

$$\mathbf{RTH} = \frac{\mathbf{RTHO}\times n_{th}}{1+\mathbf{RTHL}\frac{L_{G,TH}}{L_{EN}}+\mathbf{RTHW}\frac{W_{G,TH}}{W_{EN}}+\mathbf{RTHLW}\frac{L_{G,TH}}{L_{EN}}\frac{W_{G,TH}}{W_{EN}}}$$

$$\mathbf{STRTH} = \mathbf{STRTHO}$$

$$\mathbf{CTH} = \frac{\mathbf{CTHO}}{n_{th}}\left(1+\mathbf{RTHL}\frac{L_{G,TH}}{L_{EN}}+\mathbf{RTHW}\frac{W_{G,TH}}{W_{EN}}+\mathbf{RTHLW}\frac{L_{G,TH}}{L_{EN}}\frac{W_{G,TH}}{W_{EN}}\right)$$

© 2023 Cadence Design Systems, Inc.

Noise model parameters

$$\mathbf{FNT} = \mathbf{FNTO}$$

$$\mathbf{FNTEXC} = \mathbf{FNTEXCL} \times \mathbf{BETN}^2 \times \left(\frac{W_{EN}}{W_E}\right)^2 \times \left(\frac{L_{EN}}{L_E}\right)^{\mathbf{FTNEXCLEXP}-2}$$

$$\mathbf{NFA} = \mathbf{NFALW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E} + \mathbf{NFAW}\frac{W_{EN}}{W_E}$$

$$\mathbf{NFB} = \mathbf{NFBLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}$$

$$\mathbf{NFC} = \mathbf{NFCLW}\frac{L_{EN}}{L_E}\frac{W_{EN}}{W_E}$$

$$\mathbf{EF} = \mathbf{EFO}$$

$$\mathbf{NFE} = \mathbf{NFEO}$$

$$\mathbf{NFEB} = \mathbf{NFEBO}$$

Stress model for SWSTRESS = 1

In this paragraph are reported the modifications brought to mobility, saturation velocity and threshold voltage parameters when the strained-SOI dedicated stress model is selected (**SWSTRESS** = 2).

© 2023 Cadence Design Systems, Inc.

Effective SA/SB related parameters

$$R_A = \frac{1}{\mathbf{NF}} \sum_{i=0}^{\mathbf{NF}-1} \frac{1}{\mathbf{SA} + L/2 + i(\mathbf{SD} + L)}$$

$$R_B = \frac{1}{\mathbf{NF}} \sum_{i=0}^{\mathbf{NF}-1} \frac{1}{\mathbf{SB} + L/2 + i(\mathbf{SD} + L)}$$

$$R_{A,ref} = \frac{1}{\mathbf{SAREF} + L/2}$$

$$R_{B,ref} = \frac{1}{\mathbf{SBREF} + L/2}$$

Modification of mobility related parameters

$$K_{u0} = \left(1 + \frac{\mathbf{LKUO}}{(L + \Delta L_{PS})^{\mathbf{LLODKUO}}} + \frac{\mathbf{WKUO}}{(W_f + \Delta W_{OD} + \mathbf{WLOD})^{\mathbf{WLODKUO}}} + \frac{\mathbf{PKUO}}{(L + \Delta L_{PS})^{\mathbf{LLODKUO}} (W_f + \Delta W_{OD} + \mathbf{WLOD})^{\mathbf{WLODKUO}}}\right) \left(1 + \mathbf{TKUO}\left(\frac{T_{KD}}{T_{KR}} - 1\right)\right)$$

$$\rho_\beta = \frac{\mathbf{KUO}}{K_{u0}} (R_A + R_B)$$

$$\rho_{\beta,ref} = \frac{\mathbf{KUO}}{K_{u0}} (R_{A,ref} + R_{B,ref})$$

$$\mathbf{BETN} = \frac{1 + \rho_\beta}{1 + \rho_{\beta,ref}} \mathbf{BETN}_{ref}$$

$$\mathbf{THESAT} = \frac{1 + \rho_\beta}{1 + \rho_{\beta,ref}} \frac{1 + \mathbf{KVSAT}\rho_{\beta,ref}}{1 + \mathbf{KVSAT}\rho_\beta} \mathbf{THESAT}_{ref}$$

© 2023 Cadence Design Systems, Inc.

Modification of threshold voltage related parameters

$$K_{vth0} = 1 + \frac{\mathbf{LKVTHO}}{(L + \Delta L_{PS})^{\mathbf{LLODVTH}}} + \frac{\mathbf{WKVTHO}}{(W_f + \Delta W_{OD} + \mathbf{WLOD})^{\mathbf{WLODVTH}}} + \frac{\mathbf{PKVTHO}}{(L + \Delta L_{PS})^{\mathbf{LLODVTH}} (W_f + \Delta W_{OD} + \mathbf{WLOD})^{\mathbf{WLODVTH}}}$$

$$\Delta R = R_A + R_B - R_{A,ref} - R_{B,ref}$$

$$\mathbf{VFB} = \mathbf{VFB}_{ref} + \frac{\mathbf{KVTHO}}{K_{vth0}} \Delta R$$

$$\mathbf{VFBB} = \mathbf{VFBB}_{ref} + \frac{\mathbf{KVTHO}}{K_{vth0}} \Delta R$$

$$\mathbf{CF} = \mathbf{CF}_{ref} + \frac{\mathbf{STETAO}}{K_{vth0}^{\mathbf{LODETAO}}} \Delta R$$

Stress model for SWSTRESS = 2

Effective SA/SB related parameters

$$R_A(i) = \left(1 - \exp\left(-\frac{\mathbf{SA} + L/2 + i(\mathbf{SD} + L)}{\mathbf{STRLAMBDA}}\right)\right)^{-\mathbf{STRALPHA}}$$

$$R_B(i) = \left(1 - \exp\left(-\frac{\mathbf{SB} + L/2 + (\mathbf{NF} - 1 - i)(\mathbf{SD} + L)}{\mathbf{STRLAMBDA}}\right)\right)^{-\mathbf{STRALPHA}}$$

$$g = 1 - \frac{1}{\mathbf{NF}} \sum_{i=0}^{\mathbf{NF}-1} \left(\frac{2}{R_A(i) + R_B(i)}\right)^{1/\mathbf{STRALPHA}}$$

$$R_{A,ref} = \left(1 - \exp\left(-\frac{\mathbf{SAREF} + L/2}{\mathbf{STRLAMBDA}}\right)\right)^{-\mathbf{STRALPHA}}$$

© 2023 Cadence Design Systems, Inc.

$$R_{B,ref} = \left(1 - \exp\left(-\frac{\mathbf{SBREF} + L/2}{\mathbf{STRLAMBDA}}\right)\right)^{-\mathbf{STRALPHA}}$$

$$g_{ref} = 1 - \left(\frac{2}{R_{A,ref} + R_{B,ref}}\right)^{1/\mathbf{STRALPHA}}$$

Modification of mobility related parameters

$$r_{uo} = \frac{\mathbf{STRRUO}}{1 + \mathbf{STRTRUO}\left(\frac{T_{KD}}{T_{KR}} - 1\right)}$$

$$\rho_\beta = r_{uo} \times g$$

$$\rho_{\beta,ref} = r_{uo} \times g_{ref}$$

$$\mathbf{BETN} = \frac{1 + \rho_\beta}{1 + \rho_{\beta,ref}}\mathbf{BETN}_{ref}$$

$$\mathbf{THESAT} = \frac{1 + \rho_\beta}{1 + \rho_{\beta,ref}}\frac{1 + \mathbf{STRRVSAT}\rho_{\beta,ref}}{1 + \mathbf{STRRVSAT}\rho_\beta}\mathbf{THESAT}_{ref}$$

Modification of threshold voltage related parameters

$$K_{vth0} = 1 + \mathbf{STRWDVFBO}\frac{W_f + \Delta W_{OD} + \mathbf{WLOD}}{W_{EN}}$$

$$\mathbf{VFB} = \mathbf{VFB}_{ref} + \frac{\mathbf{STRDVFBO}}{K_{vth0}}(g - g_{ref})$$

$$\mathbf{VFBB} = \mathbf{VFBB}_{ref} + \frac{\mathbf{STRDVFBO}}{K_{vth0}}(g - g_{ref})$$

$$\mathbf{CF} = \mathbf{CF}_{ref} + \mathbf{STRDCFL}\left(\frac{\lambda_{2D}}{L_E}\right)^{\mathbf{CFLEXP}}\left(1 + \mathbf{CFW}\frac{W_{EN}}{W_E}\right)(g - g_{ref})$$

© 2023 Cadence Design Systems, Inc.

Asymmetric junctions

After the calculations described in paragraphs 3.1, 3.2 and 3.3, local parameters are clipped according to the min/max values given in the parameters tables.

Then, if the switch parameter **SWJUNASYM** is equal to 0, drain and source junctions are assumed symmetrical and all parameters related to the drain junction are overwritten by their source side counterparts.

If **SWJUNASYM** = 0:

If **SWJUNASYM** = 0:

NOVD = NOV

IGOVINVD = IGOVINV

IGOVACCD = IGOVACC

AGIDLD = AGIDL

BGIDLD = BGIDL

STBGIDLD = STBGIDL

CGIDLD = CGIDL

DGIDLD = DGIDL

COVD = COV

CFRD = CFR

If **SWJUNASYM** = 1, the drain side related parameters are kept unchanged. Notice that, if some of the drain side parameters are not specified in the model card, they take their default value and not their source side counterpart value.

© 2023 Cadence Design Systems, Inc.

Model Equations

All the equations of the model are detailed in this section. The complete calculations of the surface potentials are given in Appendix A and Appendix B, and some useful functions are described in Appendix C.

Internal parameters including temperature dependences

The calculations include temperature dependences and are carried out from local scale parameters. Local scale parameters are in capital characters and bold font.

Transistor temperature

The current is evaluated using the following procedure. The master equation for drift current is given by:

$$T_{KR} = 273.15 + \mathbf{TR}$$

.

$$T_{KD} = 273.15 + T_{ambient}$$

As in Leti-UTSOI1, a temperature node is used to compute the elevation of the channel temperature with respect to the circuit temperature due to self-heating when the **SWSHE** flag is set to 1. This temperature elevation is given by ΔT_C. The channel temperature T_{KC} is thus given by:

$$\begin{cases} T_{KC} = T_{KD} + \Delta T_C & \text{if } \mathbf{SWSHE} = 1 \\ T_{KC} = T_{KD} & \text{else} \end{cases}$$

$$\Delta T = T_{KC} - T_{KR}$$

$$\phi_{T0} = \frac{k_B T_{KC}}{q}$$

© 2023 Cadence Design Systems, Inc.

Local process parameters

$$\epsilon_{ch} = \epsilon_{Si}(1 - \mathbf{XGE}) + \epsilon_{Ge}\mathbf{XGE}$$

$$E_{g,Si} = E_{g0,Si} - \frac{\alpha_{Si}{T_{KC}}^2}{\beta_{Si} + T_{KC}}$$

$$E_{g,Ge} = E_{g0,Ge} - \frac{\alpha_{Ge}{T_{KC}}^2}{\beta_{Ge} + T_{KC}}$$

$$\delta E_g = (E_{g,Ge} - E_{g,Si} + C_g(1 - \mathbf{XGE}))\,\mathbf{XGE}$$

$$E_g = E_{g,Si} + \delta E_g$$

$$n_{eff} = \frac{n_{i,fact,300}}{1 + \sqrt{10\mathbf{XGE}}} \left(\frac{T_{KC}}{300}\right)^{3/2} \exp\left(-\frac{E_g}{2\phi_{T0}}\right)$$

$$\delta V_{FB,ch} = 0.05\mathbf{XGE} - \delta E_g/2$$

$$\delta V_{FB1,NCH} = \frac{q \times \mathbf{NCH} \times 10^6 \times \mathbf{TSI}}{2\epsilon_{ox}}(\mathbf{TOXE} + 4 \times 10^{-10}\mathbf{QMC})$$

$$\delta V_{FB2,NCH} = \frac{q \times \mathbf{NCH} \times 10^6 \times \mathbf{TSI}}{2\epsilon_{ox}}(\mathbf{TBOX} + 4 \times 10^{-10}\mathbf{QMC})$$

© 2023 Cadence Design Systems, Inc.

Interface coupling internal parameters

$$\begin{cases} C'_{ox1} = \frac{\epsilon_{ox}}{\mathbf{TOXE}} & \text{if } \mathbf{PNCE} \leq 0 \\ C'_{ox1} = \frac{\epsilon_{ox}}{\mathbf{TOXE}}(1+\mathbf{PNCE}) & \text{else} \end{cases}$$

$$\begin{cases} C'_{ox2} = \frac{\epsilon_{ox}}{\mathbf{TBOX}}(1-\mathbf{PNCE}) & \text{if } \mathbf{PNCE} \leq 0 \\ C'_{ox2} = \frac{\epsilon_{ox}}{\mathbf{TBOX}} & \text{else} \end{cases}$$

$$C'_{Si0} = \frac{\epsilon_{ch}}{\mathbf{TSI}}$$

$$\phi_T = \phi_{T0}\left(1 + \mathbf{CT}\frac{T_{KR}}{T_{KC}}\right)$$

$$k_{1,1D} = \frac{C'_{ox1}}{C'_{Si0}}$$

$$k_{2,1D} = \frac{C'_{ox2}}{C'_{Si0}}$$

$$k_{eq,1D} = \frac{1}{1 + 1/k_{1,1D} + 1/k_{2,1D}}$$

$$C_{eq,1D} = C'_{Si0}k_{eq,1D}$$

$$PSCE_1 = \mathbf{PSCE}$$

$$PSCE_2 = \mathbf{PSCEB} \times \mathbf{PSCE} \times \mathbf{TBOX}/\mathbf{TOXE}$$

$$f_{A0} = \frac{2qn_{eff}\epsilon_{ch}}{\phi_T}$$

© 2023 Cadence Design Systems, Inc.

$$x_{th,1D} = \ln\left(\frac{{C'_{Si0}}^2}{2f_{A0}}\right)$$

$$x_{SD,dep} = \frac{q \times \mathbf{NSDDC} \times 10^6 \times \mathbf{TSI}}{2(C'_{ox1} + C'_{ox2})\phi_T}$$

Drain Induced Barrier Lowering internal parameters

$$CF_1 = \mathbf{CF} + \mathbf{STCF} \times \Delta T$$

$$CF_2 = \mathbf{CF} \times \mathbf{CFB} \times \frac{\mathbf{TBOX}}{\mathbf{TOXE}} + \mathbf{STCF} \times \Delta T$$

$$x_{d0} = \frac{\mathbf{CFD}}{\phi_T}$$

Backplane internal parameters

Since the backplane is located under the buried oxide of the device, it is assumed that its temperature is that of the environment. Thus, the self-heating effect is not included for the corresponding parameters and temperature T_{KD} is considered.

$$n_{eff,sub} = n_{i,fact,300}\left(\frac{T_{KD}}{300}\right)^{3/2}\exp\left(-\frac{E_{g,Si}}{2(k_B T_{KD}/q)}\right)$$

$$G_{f,sub} = \frac{\sqrt{2q\epsilon_{Si}\mathbf{NSUB} \times 10^6}}{C_{eq0}\sqrt{k_B T_{KD}/q}}$$

$$\xi_{sub} = 1 + \frac{G_{f,sub}}{\sqrt{2}}$$

$$\xi_{mrg,sub} = 10^{-5}\xi_{sub}$$

© 2023 Cadence Design Systems, Inc.

$$x_{b,sub} = \ln\left(\frac{\mathbf{NSUB} \times 10^6}{n_{eff,sub}}\right)$$

$$x_{n,sub} = 2x_{b,sub}$$

$$\begin{cases} type_{sub} = +1 & \text{if } \mathbf{NSUB} \geq 0 \\ type_{sub} = -1 & \text{else} \end{cases}$$

Gate poly-depletion parameters

When **SWPDEP** = 1, Gate poly-depletion is activated.

$$n_{eff,poly} = n_{i,fact,300}\left(\frac{T_{KD}}{300}\right)^{3/2} \exp\left(-\frac{E_{g,Si}}{2(k_B T_{KD}/q)}\right)$$

$$\delta V_{FB1,PDEP} = \phi_{T0}\left(\ln\left(\frac{\mathbf{NP} \times 10^6}{n_{eff,poly}}\right)\right)$$

$$K_p = \frac{\sqrt{2q\epsilon_{Si}\mathbf{NP} \times 10^6}}{\frac{\epsilon_{ox}}{\mathbf{TOXE}}}$$

© 2023 Cadence Design Systems, Inc.

Quantum mechanical correction internal parameters

1

$$\begin{cases} \delta V_{FB,qm} = 0 & \text{if } \mathbf{QMC} = 0 \\ \delta V_{FB,qm} = \frac{0.409618895}{10^{18}\mathbf{TSI}^2} & \text{if } \mathbf{QMC} > 0 \text{ and } \mathbf{TYPE} = +1\ (NMOS) \\ \delta V_{FB,qm} = \frac{0.723134895}{10^{18}\mathbf{TSI}^2} & \text{if } \mathbf{QMC} > 0 \text{ and } \mathbf{TYPE} = -1\ (PMOS) \end{cases}$$

$$\begin{cases} qq = 0 & \text{if } \mathbf{QMC} = 0 \\ qq = \frac{0.4QM_N\mathbf{QMC}}{(10^{18}\mathbf{TSI}^2\phi_T)^{1/3}} & \text{if } \mathbf{QMC} > 0 \text{ and } \mathbf{TYPE} = +1\ (NMOS) \\ qq = \frac{0.4QM_P\mathbf{QMC}}{(10^{18}\mathbf{TSI}^2\phi_T)^{1/3}} & \text{if } \mathbf{QMC} > 0 \text{ and } \mathbf{TYPE} = -1\ (PMOS) \end{cases}$$

$$V_{FB1} = \mathbf{TYPE}(\mathbf{VFB} + \mathbf{STVFB} \times \Delta T + \delta V_{FB,ch} + \delta V_{FB1,NCH}) + \delta V_{FB,qm} + \mathbf{DELVTO}$$

$$\begin{cases} V_{FB2} = \mathbf{TYPE}(\mathbf{VFBB} + \mathbf{STVFB} \times \Delta T + \delta V_{FB,ch} + \delta V_{FB2,NCH}) & \\ \quad + \delta V_{FB,qm} & \text{if } \mathbf{SWSUBDEP} = 0 \\ V_{FB2} = \mathbf{TYPE}(\mathbf{VFBB} + \mathbf{STVFB} \times \Delta T + \delta V_{FB,ch} + \delta V_{FB2,NCH} & \\ \quad + type_{sub} x_{b,sub}(k_B T_{KD}/q)) + \delta V_{FB,qm} & \text{else} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Mobility internal parameters

$$\beta_{N1} = \mathbf{FACTUO} \times \mathbf{BETN} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STBET}}$$

$$\beta_{N2} = \mathbf{FACTUO} \times \mathbf{BETN} \times \mathbf{BETNB} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STBET}}$$

$$\mu_E = \mathbf{MUE} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STMUE}}$$

$$\theta_\mu = \mathbf{THEMU} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STTHEMU}}$$

$$C_S = \mathbf{CS} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STCS}}$$

$$\theta_{CS} = \mathbf{THECS} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STTHECS}}$$

$$X_{cor} = \mathbf{XCOR} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STXCOR}}$$

$$f_{\mu E} = 10^{-8}\frac{\phi_T}{\mathbf{TSI}}\mu_E$$

$$q_{i1th,CS} = 0.5 \times \mathbf{CSTHR}$$

$$q_{i2th,CS} = q_{i1th,CS} \times \mathbf{CSTHRB}$$

$$\begin{cases} \eta_\mu = 1/2 \times \mathbf{FETA} & \text{if } \mathbf{TYPE} = +1\ (NMOS) \\ \eta_\mu = 1/3 \times \mathbf{FETA} & \text{if } \mathbf{TYPE} = -1\ (PMOS) \end{cases}$$

© 2023 Cadence Design Systems, Inc.

Series resistance internal parameters

$$R_S = \mathbf{RS} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STRS}}$$

$$f_{RS} = 2\phi_T R_S$$

Velocity saturation internal parameters

$$\theta_{sat} = \mathbf{FACTUO} \times \mathbf{THESAT} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STTHESAT+STBET}}$$

Notice the presence of the **FACTUO** pre-factor and of **STBET** in the temperature exponent. This contributes to decouple velocity saturation parameters from low longitudinal field mobility ones, and makes in particular **STTHESAT** the temperature exponent of the saturation velocity itself.

$$f_{vsat} = \phi_T \theta_{sat}$$

Channel Length Modulation internal parameters

$$\gamma_{AX} = \left(2^{16/\mathbf{AX}} - 1\right)^{3/8} - 1$$

$$f_{alp1} = \frac{\mathbf{ALP1}}{\phi_T}$$

Gate current internal parameters

$$I_{G,inv} = \mathbf{IGINV} \times \left(\frac{T_{KC}}{T_{KR}}\right)^{\mathbf{STIG}}$$

$$I_{G,ovinv} = \mathbf{IGOVINV} \times \left(\frac{T_{KC}}{T_{KR}}\right)^{\mathbf{STIG}}$$

© 2023 Cadence Design Systems, Inc.

$$I_{G,ovinvD} = \mathbf{IGOVINVD} \times \left(\frac{T_{KC}}{T_{KR}}\right)^{\mathbf{STIG}}$$

$$I_{G,ovacc} = \mathbf{IGOVACC} \times \left(\frac{T_{KC}}{T_{KR}}\right)^{\mathbf{STIG}}$$

$$I_{G,ovaccD} = \mathbf{IGOVACCD} \times \left(\frac{T_{KC}}{T_{KR}}\right)^{\mathbf{STIG}}$$

$$I_{G,fnovinv} = \mathbf{FNOVINV} \times \left(\frac{T_{KC}}{T_{KR}}\right)^{\mathbf{STIGFN}}$$

$$I_{G,fnovinvD} = \mathbf{FNOVINVD} \times \left(\frac{T_{KC}}{T_{KR}}\right)^{\mathbf{STIGFN}}$$

$$B_{ch} = \frac{4}{3}\frac{\sqrt{2qm_0\mathbf{CHIB}}}{\hbar}\mathbf{TOXP}$$

$$B_{ov} = \frac{4}{3}\frac{\sqrt{2qm_0\mathbf{CHIB}}}{\hbar}\mathbf{TOXP}$$

Note that, B_{ch} and B_{ov} are equal in L-UTSOI, since the Leti-UTSOI1 parameter **TOXOV** has been removed.

$$\begin{cases} G_{CQ,ch} = 0 & \text{if } \mathbf{GC3CH} \geq 0 \\ G_{CQ,ch} = -0.495 \times \mathbf{GC2CH}/\mathbf{GC3CH} & \text{else} \end{cases}$$

$$\begin{cases} G_{CQ,ovinv} = 0 & \text{if } \mathbf{GC3OVINV} \geq 0 \\ G_{CQ,ovinv} = -0.495 \times \mathbf{GC2OVINV}/\mathbf{GC3OVINV} & \text{else} \end{cases}$$

$$\begin{cases} G_{CQ,ovacc} = 0 & \text{if } \mathbf{GC3OVACC} \geq 0 \\ G_{CQ,ovacc} = -0.495 \times \mathbf{GC2OVACC}/\mathbf{GC3OVACC} & \text{else} \end{cases}$$

$$\alpha_b = \frac{E_g}{2}$$

© 2023 Cadence Design Systems, Inc.

$$D_{ch} = \phi_T \mathbf{GCO}$$

$$D_{ov} = \phi_{T0} \mathbf{GCO}$$

$$n_{iginv} = \frac{1}{1 + \mathbf{NIGINV} \times E_g/(2\phi_T)}$$

Gate Induced Drain/Source Leakage (GIDL/GISL) internal parameters

$$A_{GIDL} = \frac{4 \times 10^{-18}}{\mathbf{TOXP}^2} \mathbf{AGIDL}$$

$$A_{GIDLD} = \frac{4 \times 10^{-18}}{\mathbf{TOXP}^2} \mathbf{AGIDLD}$$

$$B_{GIDL} = 5 \times 10^8 \mathbf{TOXP} \times \mathbf{BGIDL} \times (1 + \mathbf{STBGIDL} \times \Delta T)$$

$$B_{GIDLD} = 5 \times 10^8 \mathbf{TOXP} \times \mathbf{BGIDLD} \times (1 + \mathbf{STBGIDLD} \times \Delta T)$$

Impact ionization internal parameters

$$a_2 = \mathbf{A2} \times \left(\frac{T_{KC}}{T_{KR}}\right)^{\mathbf{STA2}}$$

© 2023 Cadence Design Systems, Inc.

Charge model internal parameters

$$f_{area} = \phi_T \mathbf{AREAQ}$$

$$f_{SD,inner} = \frac{q \times \mathbf{NSDAC} \times 10^6}{4\epsilon_{ch}\phi_T}$$

$$x_{SD} = \ln\left(\frac{\mathbf{NSDAC} \times 10^6}{n_{eff}}\right)$$

$$f_{if} = 1.25 \times 10^{-6}\phi_T \mathbf{FIF}$$

Self-heating internal parameters

$$R_{th} = \mathbf{RTH} \times \left(\frac{T_{KR}}{T_{KC}}\right)^{\mathbf{STRTH}}$$

Noise model internal parameters

$$n_T = 4k_B T_{KC} \mathbf{FNT}$$

$$n_{T0} = 4k_B T_{KD} \mathbf{FNT}$$

$$f_{exc} = 10^{12} m_0 \mathbf{FNTEXC}$$

Terminal voltage conditioning

The input voltages used in the model are V_{GS}, V_{DS} and V_{SB} in nMOSFET and positive V_{DS} configuration (that is, sign of external voltages is reversed for pMOSFET, and source/drain are interchanged in case of negative VDS), from which V_{SD}, V_{GD}, V_{DB} and V_{GB} are computed. Then, dimensionless quantities are defined from these voltages.

© 2023 Cadence Design Systems, Inc.

Voltages for channel current and intrinsic charge models

$$x_d = \frac{V_{DS}}{\phi_T}$$

$$x_{dsx} = \frac{\sqrt{{V_{DS}}^2 + 0.01} - 0.1}{\phi_T}$$

$$x_{g10} = \frac{V_{GS} - V_{FB1}}{\phi_T} - \frac{x_d - x_{dsx}}{2}$$

$$x_{g20} = \frac{-V_{SB} - V_{FB2}}{\phi_T} - \frac{x_d - x_{dsx}}{2}$$

Voltages for overlap currents and charges

$$x_{gs,ov} = -\frac{V_{GS}}{\phi_{T0}}$$

$$x_{gd,ov} = -\frac{V_{GD}}{\phi_{T0}}$$

$$x_{gs,ovcv} = -\frac{V_{GS} - \mathbf{TYPE} \times \mathbf{DVFBOV} - E_g/2}{\phi_{T0}}$$

$$x_{gd,ovcv} = -\frac{V_{GD} - \mathbf{TYPE} \times \mathbf{DVFBOV} - E_g/2}{\phi_{T0}}$$

Backplane depletion

Depletion of the backplane is accounted for through the calculation of an effective backplane bias x_{g2eff}. If backplane depletion is not activated (**SWSUBDEP**=0), then x_{g2eff} is simply given by:

$$x_{g2eff} = x_{g20}$$

© 2023 Cadence Design Systems, Inc.

On the contrary, if backplane depletion is activated (**SWSUBDEP**=1), then the computation of x_{g2eff} uses a PSP-like surface potential calculation sequence. This computation is based on the analogy that the backplane is considered as the channel of a bulk MOSFET, which gate electrode is the front gate and which gate oxide capacitance is equal to the front gate oxide capacitance in series with the channel film capacitance and the buried oxide capacitance. The detailed calculation of x_{g2eff} is:

$$x_{g1int} = \mathbf{TYPE} \times type_{sub} \times x_{g10}$$

$$x_{g2int} = \mathbf{TYPE} \times type_{sub} \times x_{g20}$$

$$x_{gbint} = x_{g1int} - x_{g2int}$$

If $|x_{gbint}| \leq \xi_{mrg,sub}$:

$$\delta x_{g2,sub} = \frac{x_{gbint}}{\xi_{sub}} \left(1 + \frac{x_{gbint} G_{f,sub} (1 - \exp(-x_{n,sub}))}{6\sqrt{2} {\xi_{sub}}^2} \right)$$

Else if $x_{gbint} < -\xi_{mrg,sub}$:

$$y_g = -x_{gbint}$$

$$y_{sub} = 1.25 \frac{y_g}{\xi_{sub}}$$

$$\eta = \frac{y_{sub} + 10 - \sqrt{(y_{sub} - 6)^2 + 64}}{2}$$

$$a = (y_g - \eta)^2 + {G_{f,sub}}^2 (\eta + 1)$$

$$c = 2(y_g - \eta) - {G_{f,sub}}^2$$

$$\tau = -\eta + \ln\left(a / {G_{f,sub}}^2 \right)$$

$$y_0 = \sigma_3(a, c, \tau, \eta)$$

$$\Delta_0 = \exp(y_0)$$

© 2023 Cadence Design Systems, Inc.

$$\chi_0 = \frac{{y_0}^2}{2 + {y_0}^2}$$

$$\chi_1 = \frac{4y_0}{(2 + {y_0}^2)^2}$$

$$\chi_2 = \frac{8 - 12{y_0}^2}{(2 + {y_0}^2)^3}$$

$$p_C = 2(y_g - y_0) + {G_{f,sub}}^2(\Delta_0 - 1 + \exp(-x_{n,sub})(1 - \chi_1 - 1/\Delta_0))$$

$$q_C = (y_g - y_0)^2 + {G_{f,sub}}^2(y_0 - \Delta_0 + 1 + \exp(-x_{n,sub})(1 + \chi_0 - 1/\Delta_0 - y_0))$$

$$\delta x_{g2,sub} = -y_0 - \frac{2q_C}{p_C + \sqrt{{p_C}^2 - 2q_C(2 - {G_{f,sub}}^2(\Delta_0 + \exp(-x_{n,sub})(1/\Delta_0 - \chi_2)))}}$$

Else,

$$x_{g1} = 1.25 + 0.7324648775 G_{f,sub}$$

$$\frac{1}{\widetilde{x}_{g1}} = \frac{1.25\xi_{sub}/x_{g1} - 1}{x_{g1}}$$

$$\bar{x} = \frac{x_{gbint}}{\xi_{sub}}\left(1 + \frac{x_{gbint}}{\widetilde{x}_{g1}}\right)$$

$$w = 1 - \exp(-\bar{x})$$

$$x_1 = x_{gbint} + {G_{f,sub}}^2/2 - G_{f,sub}\sqrt{x_{gbint} + {G_{f,sub}}^2/4 - w}$$

$$b_x = x_{n,sub} + 3$$

$$\eta = \text{MIN_FUNC}(x_1, b_x, 5) - \frac{b_x - \sqrt{{b_x}^2 + 5}}{2}$$

© 2023 Cadence Design Systems, Inc.

$$\chi_0 = \frac{\eta^2}{2+\eta^2}$$

$$\chi_1 = \frac{4\eta}{(2+\eta^2)^2}$$

$$\chi_2 = \frac{8-12\eta^2}{(2+\eta^2)^3}$$

$$a = (x_{gbint} - \eta)^2 - {G_{f,sub}}^2 \left(\exp(-\eta) + \eta - 1 - \exp(-x_{n,sub})(\eta + 1 + \chi_0)\right)$$

$$b = 1 - {G_{f,sub}}^2 \times \frac{\exp(-\eta) - \chi_2 \exp(-x_{n,sub})}{2}$$

$$c = 2(x_{gbint} - \eta) + {G_{f,sub}}^2 \left(1 - \exp(-\eta) - \exp(-x_{n,sub})(1 + \chi_1)\right)$$

$$\tau = x_{n,sub} - \eta + \ln\left(\frac{a}{{G_{f,sub}}^2}\right)$$

$$x_0 = \sigma_2(a, b, c, \tau, \eta)$$

$$\Delta_0 = \exp(x_0)$$

$$\chi_0' = \frac{{x_0}^2}{2+{x_0}^2}$$

$$\chi_1' = \frac{4x_0}{(2+{x_0}^2)^2}$$

$$\chi_2' = \frac{8-12{x_0}^2}{(2+{x_0}^2)^3}$$

$$p_C = 2(x_{gbint} - x_0) + {G_{f,sub}}^2(1 - 1/\Delta_0 + \exp(-x_{n,sub})(\Delta_0 - 1 - \chi_1'))$$

$$q_C = (x_{gbint} - x_0)^2 - {G_{f,sub}}^2(x_0 - 1 + 1/\Delta_0 + \exp(-x_{n,sub})(\Delta_0 - 1 - \chi_0' - x_0))$$

© 2023 Cadence Design Systems, Inc.

$$\delta x_{g2,sub} = x_0 + \frac{2q_C}{p_C + \sqrt{{p_C}^2 - 2q_C(2 - {G_{f,sub}}^2(1/\Delta_0 + \exp(-x_{n,sub})(\Delta_0 - \chi_2')))}}$$

Finally,

$$x_{g2eff} = \mathbf{TYPE} \times type_{sub} \times (x_{g2int} + \delta x_{g2,sub})$$

Channel current

This part is dedicated to the calculation of the MOSFET channel current. Since this calculation preserves the formal symmetry between front and back interfaces, it is valid not only for Ultra-Thin Body and Buried oxide FDSOI transistors, but also for Independent Double Gate MOSFETs.

Quantum mechanical correction in subthreshold regime

To account for quantum confinement when the effect is activated (QMC>0), the effective geometry of the device is modified. In the correction detailed here, it is assumed that there is no charge in the channel. Note that his correction is only valid in the subthreshold regime.

If QMC > 0:

$$e_1 = \mathrm{MAX_FUNC}\left(k_{eq,1D}(x_{g10} - x_{g2eff}), 15, 225\right)$$

$$e_2 = \mathrm{MAX_FUNC}\left(-k_{eq,1D}(x_{g10} - x_{g2eff}), 15, 225\right)$$

$$C'_{Si} = \frac{C'_{Si0}}{1 - qq\left({e_1}^{-1/3} + {e_2}^{-1/3}\right)}$$

$$k_{1,1D,QM} = k_{1,1D}\frac{1 - qq\left({e_1}^{-1/3} + {e_2}^{-1/3}\right)}{1 + k_{1,1D}{e_1}^{-1/3}qq}$$

© 2023 Cadence Design Systems, Inc.

$$k_{2,1D,QM} = k_{2,1D}\frac{1 - qq\left({e_1}^{-1/3} + {e_2}^{-1/3}\right)}{1 + k_{2,1D}{e_2}^{-1/3}qq}$$

$$k_{eq,1D,QM} = \frac{1}{1 + 1/k_{1,1D,QM} + 1/k_{2,1D,QM}}$$

$$t_{ox1,fact} = 1 + k_{1,1D,QM}{e_1}^{-1/3}qq$$

$$t_{ox2,fact} = 1 + k_{2,1D,QM}{e_2}^{-1/3}qq$$

Else,

$$C'_{Si} = C'_{Si0}$$

$$k_{1,1D,QM} = k_{1,1D}$$

$$k_{2,1D,QM} = k_{2,1D}$$

$$k_{eq,1D,QM} = k_{eq,1D}$$

$$t_{ox1,fact} = 1$$

$$t_{ox2,fact} = 1$$

Short channel effects

$$\delta x_{WI,1D} = k_{eq,1D,QM}(x_{g10} - x_{g2eff})$$

$$\begin{cases} x_{WI,1D} = x_{g10} - \frac{\delta x_{WI,1D}}{k_{1,1D,QM}} + \ln\left(\frac{1+\exp(-\delta x_{WI,1D})}{2}\right) & \text{if } \delta x_{WI,1D} > 0 \\ x_{WI,1D} = x_{g2eff} + \frac{\delta x_{WI,1D}}{k_{2,1D,QM}} + \ln\left(\frac{1+\exp(\delta x_{WI,1D})}{2}\right) & \text{else} \end{cases}$$

$$x_{1D} = \text{MIN_FUNC}(x_{WI,1D}, x_{th,1D}, 4.0)$$

© 2023 Cadence Design Systems, Inc.

$$\delta l_{eff} = \sqrt{1 + 2\frac{x_{th,1D} - x_{1D}}{x_{SD,dep}}} - 1$$

$$x_{edge} = x_{1D} + x_{SD,dep}\delta l_{eff}$$

$$c_{sce1} = \frac{1}{1 + PSCE_1 \times \text{MAX_FUNC}(1 + \textbf{PSCEDLB} \times x_{g20}, 0.5, 0.01)}$$

$$c_{sce2} = \frac{1}{1 + PSCE_2 \times \text{MAX_FUNC}(1 + \textbf{PSCEDLB} \times x_{g20}, 0.5, 0.01)}$$

$$\delta x_{g1,DIBL} = 2CF_1 x_{d0}\left(\sqrt{1 + x_{dsx}/x_{d0}} - 1\right)(1 + \textbf{CFDL} \times \delta l_{eff})(1 + \textbf{CFDLB} \times x_{g20})$$

$$\delta x_{g2,DIBL} = 2CF_2 x_{d0}\left(\sqrt{1 + x_{dsx}/x_{d0}} - 1\right)(1 + \textbf{CFDL} \times \delta l_{eff})(1 + \textbf{CFDLB} \times x_{g20})$$

$$x_{g1} = (x_{g10} - x_{edge} + \delta x_{g1,DIBL})c_{sce1} + x_{edge} + \frac{x_d - x_{dsx}}{2}$$

$$x_{g2} = (x_{g2eff} - x_{edge} + \delta x_{g2,DIBL})c_{sce2} + x_{edge} + \frac{x_d - x_{dsx}}{2}$$

$$x_{g1x} = \text{MIN_FUNC}(x_{g2} + \textbf{CICF}(x_{g1} - x_{g2}), 600, 0.01)$$

$$x_{g2x} = \text{MIN_FUNC}(x_{g1} + \textbf{CIC}(x_{g2} - x_{g1}), 600, 0.01)$$

Interface coupling in subthreshold regime

$$k_1 = \frac{k_{1,1D,QM}}{c_{sce1}}$$

$$k_2 = \frac{k_{2,1D,QM}}{c_{sce2}}$$

$$k_{eq} = \frac{1}{1 + 1/k_1 + 1/k_2}$$

© 2023 Cadence Design Systems, Inc.

$$A_0 = \frac{f_{A0}}{{C'_{Si}}^2}$$

$$\delta x_{th} = \ln\left(\frac{1+k_1}{1+k_2}\right)$$

$$diff_{min} = 2\delta x_{th}\frac{\exp(\delta x_{th})+1}{\exp(\delta x_{th})-1}$$

$$\delta x_{WI} = k_{eq}(x_{g1x} - x_{g2x})$$

$$x_{1,WI0} = x_{g1x} - \delta x_{WI}/k_1$$

$$x_{2,WI0} = x_{g2x} + \delta x_{WI}/k_2$$

Inversion charge and related quantities at source side

The gate charge density at the source side q1S, normalized to $k_1 C'_{Si}\phi_T$, is computed as:

$$q_{1S} = \text{CHARGE_DENSITY}(x_{g1x}, x_{g2x}, 0)$$

Then, inversion and back gate charge densities, normalized to $C'_{Si}\phi_T$ and $k_2 C'_{Si}\phi_T$ respectively, are calculated:

$$A_{e1S} = A_0 \exp(x_{g1x} - q_{1S})$$

$$f_{qsqS} = {k_1}^2 {q_{1S}}^2 - A_{e1S}$$

© 2023 Cadence Design Systems, Inc.

If $f_{qsqS} < -0.005$:

$$f_{qctS} = \sqrt{|f_{qsqS}|}\cot\left(\sqrt{|f_{qsqS}|}/2\right)$$

$$f_{shS} = -\frac{f_{qsqS}}{\sin\left(\sqrt{|f_{qsqS}|}/2\right)^2}$$

$$f_{lnS} = \ln(f_{shS})$$

Else if $f_{qsqS} > 0.005$:

$$\zeta_S = \exp\left(-\sqrt{|f_{qsqS}|}\right)$$

$$f_{qctS} = \sqrt{|f_{qsqS}|}\frac{1+\zeta_S}{1-\zeta_S}$$

$$f_{shS} = \frac{4f_{qsqS}}{1-\zeta_S(2-\zeta_S)}\zeta_S$$

$$f_{lnS} = \ln\left(\frac{4f_{qsqS}}{1-\zeta_S(2-\zeta_S)}\right) - \sqrt{|f_{qsqS}|}$$

Else:

$$f_{qctS} = 2 + \frac{f_{qsqS}}{6}\left(1 - \frac{f_{qsqS}}{60}\left(1 - \frac{f_{qsqS}}{42}\right)\right)$$

$$f_{shS} = 4 - \frac{f_{qsqS}}{3}\left(1 - \frac{f_{qsqS}}{20}\left(1 - \frac{5f_{qsqS}}{126}\right)\right)$$

$$f_{lnS} = \ln(f_{shS})$$

© 2023 Cadence Design Systems, Inc.

If $1.01k_1q_{1S} + f_{qctS} \leq 0$:

$$q_{iS} = \frac{k_1q_{1S} - f_{qctS}}{1 - f_{shS}/A_{e1S}}$$

$$q_{2S} = \frac{q_{iS} - k_1q_{1S}}{k_2}$$

Else if $A_{e1S}k_1q_{1S} < 0.9{k_1}^2{q_{1S}}^2(k_1q_{1S} + f_{qctS})$:

$$q_{iS} = \frac{A_{e1S}}{k_1q_{1S} + f_{qctS}}$$

$$q_{2S} = \frac{q_{iS} - k_1q_{1S}}{k_2}$$

Else:

$$q_{2S} = x_{g2x} - x_{g1x} + q_{1S} + 2\ln(k_1q_{1S} + f_{qctS}) - f_{lnS}$$

$$q_{iS} = k_1q_{1S} + k_2q_{2S}$$

Some required quantities, including the drift electrostatic potential, are computed:

$$A_{e2D} = A_0 \exp(x_{g2x} - q_{2D} - x_{Deff})$$

If $q_{iS} > 10^{-6}$:

$$b_{1D} = A_{e1D}/k_1$$

$$b_{2D} = A_{e2D}/k_2$$

$$a_{1D} = b_{1D} + 2k_1q_{1D}$$

$$a_{2D} = b_{2D} + 2k_2q_{2D}$$

$$\Sigma_D = 2q_{iD} + b_{1D} + b_{2D}$$

© 2023 Cadence Design Systems, Inc.

$$\begin{cases} Z_D = \frac{-4 f_{qsqD} \Sigma_D}{q_{iD}(a_{1D}a_{2D}+2a_{1D}(q_{2D}+2)+2a_{2D}(q_{1D}+2))} & \text{if } |f_{qsqD}| > 0.005 \\ Z_D = \frac{A_{e1D}A_{e2D}\Sigma_D}{q_{iD}(a_{1D}A_{e1D}+a_{2D}A_{e2D}+a_{1D}a_{2D}q_{iD}\Gamma_D)} & \text{else} \\ \text{with } \Gamma_D = 1 + \frac{q_{iD}}{6}\left(1 - \frac{f_{qsqD}}{30}\left(1 - \frac{f_{qsqD}}{28}\left(1 - \frac{f_{qsqD}}{30}\right)\right)\right) & \end{cases}$$

Finally:

$$x_{driftD} = x_{Deff} + \ln(q_{iD})$$

Mid-point inversion charge

$$q_{im} = \frac{q_{iS} + q_{iD}}{2}$$

$$\delta x_{drift} = x_{driftD} - x_{driftS}$$

Mobility attenuation and series resistance

Front and back transverse effective fields, normalized to $C'_{Si}\phi_T/\epsilon_{ch}$:

$$e_{surf1D} = 2\ln(1 + \exp(k_1 q_{1D}/2))$$

$$e_{surf2D} = 2\ln(1 + \exp(k_2 q_{2D}/2))$$

$$e_{cpl1D} = e_{surf2D} - k_2 q_{2D}$$

$$e_{cpl2D} = e_{surf1D} - k_1 q_{1D}$$

$$e_{eff1D} = \eta_\mu e_{surf1D} + (1 - \eta_\mu) e_{cpl1D}$$

$$e_{eff2D} = \eta_\mu e_{surf2D} + (1 - \eta_\mu) e_{cpl2D}$$

© 2023 Cadence Design Systems, Inc.

Mid-values of surface and effective fields:

$$e_{surf1} = \frac{e_{surf1S} + e_{surf1D}}{2}$$

$$e_{surf2} = \frac{e_{surf2S} + e_{surf2D}}{2}$$

$$e_{cpl1} = \frac{e_{cpl1S} + e_{cpl1D}}{2}$$

$$e_{cpl2} = \frac{e_{cpl2S} + e_{cpl2D}}{2}$$

$$e_{eff1} = \frac{e_{eff1S} + e_{eff1D}}{2}$$

$$e_{eff2} = \frac{e_{eff2S} + e_{eff2D}}{2}$$

Non-universality correction factor:

$$f_{cor} = \frac{\text{MAX_FUNC}(1 + X_{cor}(e_{cpl1} + \mathbf{XCORB} \times e_{cpl2}), 0, 0.01)}{\text{MAX_FUNC}(1 + 0.2 \times X_{cor}(e_{cpl1} + \mathbf{XCORB} \times e_{cpl2}), 0, 0.01)}$$

Coulomb scattering term:

$$q_{i1m} = \frac{e_{surf1}}{e_{surf1} + e_{surf2}} q_{im}$$

$$q_{i2m} = \frac{e_{surf2}}{e_{surf1} + e_{surf2}} q_{im}$$

$$G_{CS} = \frac{C_S(1 + \mathbf{CSFI} \times e_{cpl1} + \mathbf{CSBI} \times e_{cpl2})}{(1 + q_{i1m}/q_{i1th,CS} + q_{i2m}/q_{i2th,CS})^{\theta_{CS}}}$$

© 2023 Cadence Design Systems, Inc.

Series resistance term:

$$\begin{cases} f_{RSG} = 1 - \mathbf{RSG} \times {q_{im}}^{\mathbf{THERSG}} & \text{if } \mathbf{RSG} < 0 \\ f_{RSG} = 1/(1 + \mathbf{RSG} \times {q_{im}}^{\mathbf{THERSG}}) & \text{else} \end{cases}$$

$$G_{RS} = f_{RS} C'_{Si} (q_{im} f_{RSG} + \mathbf{RSIG}) \times \text{MAX_FUNC}(1 - \mathbf{RSB} x_{g20}, 0, 0.01)$$

Total mobility degradation term, including high field mobility effect:

$$G_{mob1} = 1 + (f_{\mu E} \times e_{eff1})^{\theta_\mu} + G_{CS} + \beta_{N1} G_{RS}$$

$$G_{mob2} = 1 + (f_{\mu E} \times e_{eff2})^{\theta_\mu} + G_{CS} + \beta_{N2} G_{RS}$$

$$c_1 = e_{surf1} \beta_{N1}$$

$$c_2 = e_{surf2} \beta_{N2}$$

$$G_{mob} = f_{cor} \frac{c_1 + c_2}{c_1/G_{mob1} + c_2/G_{mob2}}$$

$$\beta_{Neff} = \frac{c_1 + c_2}{e_{surf1} + e_{surf2}}$$

Channel length modulation

$$q^*_{im1} = q_{im} + 4$$

$$\begin{cases} r_1 = \frac{q_{im}}{q^*_{im1}} \times 1/(1 + \mathbf{ALPB} \times q_{im2}) & \text{if } \mathbf{ALPB} > 0 \\ r_1 = \frac{q_{im}}{q^*_{im1}} \times (1 - \mathbf{ALPB} \times q_{im2}) & \text{else} \end{cases}$$

$$\Delta L/L = \mathbf{ALP} \times \ln\left(1 + \frac{x_D - x_{Deff}}{\mathbf{VP}/\phi_T + \mathbf{VPG} \times {q_{im}}^2}\right) \times r_1$$

$$G_{\Delta L} = \frac{1}{1 + \Delta L/L(1 + \Delta L/L)}$$

© 2023 Cadence Design Systems, Inc.

$$\Delta L_1/L = \left(\mathbf{ALP} + \frac{f_{alp1}}{q^*_{im1}}\right) \times \ln\left(1 + \frac{x_D - x_{Deff}}{\mathbf{VP}/\phi_T + \mathbf{VPG} \times {q_{im}}^2}\right) \times r_1$$

$$F_{\Delta L} = \frac{1 + \Delta L_1/L(1 + \Delta L_1/L)}{1 + \Delta L/L(1 + \Delta L/L)}$$

Velocity saturation

$$w_{sat1} = \frac{100 e_{surf1}}{100 + e_{surf1}}$$

$$\begin{cases} sat_{fact1} = 1/(1 - w_{sat1}\mathbf{THESATG}) & \text{if } \mathbf{THESATG} < 0 \\ sat_{fact1} = 1 + w_{sat1}\mathbf{THESATG} & \text{else} \end{cases}$$

$$w_{sat2} = \frac{100 e_{surf2}}{100 + e_{surf2}}$$

$$\begin{cases} sat_{fact2} = 1/(1 - w_{sat2}\mathbf{THESATB}) & \text{if } \mathbf{THESATB} < 0 \\ sat_{fact2} = 1 + w_{sat2}\mathbf{THESATB} & \text{else} \end{cases}$$

$$G_\gamma = f_{vsat}\delta x_{drift}\frac{sat_{fact1} + sat_{fact2}}{2}$$

$$z_{sat} = \left(\frac{G_\gamma}{G_{mob}G_{\Delta L}}\right)^2$$

$$G_{vsat} = G_{mob}G_{\Delta L}\sqrt{1 + z_{sat}}$$

Quantum confinement

Here is detailed the second quantum confinement correction that complements the correction described in Quantum mechanical correction internal parameters.

© 2023 Cadence Design Systems, Inc.

If QMC > 0:

$$qm_{fact1} = \frac{1 + k_1 \times qq \times 0.6/({e_{surf1}}^2 + 60)^{1/6}}{t_{ox1,fact}}$$

$$qm_{fact2} = \frac{1 + k_2 \times qq \times 0.6/({e_{surf2}}^2 + 60)^{1/6}}{t_{ox2,fact}}$$

$$qm_{fact} = \frac{e_{surf1} + e_{surf2}}{e_{surf1}/qm_{fact1} + e_{surf2}/qm_{fact2}}$$

Else:

$$qm_{fact1} = 1$$

$$qm_{fact2} = 1$$

$$qm_{fact} = 1$$

Channel current

If $q_{iS} > 10^{-6}$:

$$Z_{iD} = \frac{Z_D \Sigma_D}{a_{1D} a_{2D}} - \frac{1}{q_{iD}} \left(\frac{A_{e1D}}{a_{1D}} + \frac{A_{e2D}}{a_{2D}} \right)$$

$$\begin{cases} d_D = \frac{Z_{iD} q_{iD}}{Z_{iD}+1} & \text{if } q_{iD} > 10^{-6} \\ d_D = d_\infty & \text{else} \end{cases}$$

If $|d_D - d_S| > 10^{-3}$:

$$\begin{aligned} L_S &= q_{iD} - q_{iS} - d_D \delta x_{drift} \\ L_D &= q_{iD} - q_{iS} - d_S \delta x_{drift} \\ U_S &= \sqrt{{L_S}^2 + 1 + 36(d_D - d_S)^2} \\ U_D &= \sqrt{{L_D}^2 + 1 + 36(d_D - d_S)^2} \\ \delta i_{drift} &= \frac{L_S U_D - L_D U_S + \left(1 + 36(d_D - d_S)^2\right) \ln((L_D + U_D)/(L_S + U_S))}{4(d_D - d_S)} \end{aligned}$$

© 2023 Cadence Design Systems, Inc.

Else:

$$\delta i_{drift} = -\frac{\delta x_{drift}{}^3 (d_D - d_S)^2}{24\sqrt{1+36(d_D-d_S)^2}}$$

Else:

$$d_D = d_\infty$$

$$\delta x_{drift} = 0$$

$$i_{DS,norm} = q_{im}\delta x_{drift} + \delta i_{drift} + q_{iS} - q_{iD}$$

$$I_{DS} = \frac{F_{\Delta L}}{G_{vsat} qm_{fact}} \beta_{Neff} \phi_T{}^2 C'_{Si} i_{DS,norm}$$

Gate current, intrinsic charges and overlap related variables

Effective gate charge at front and back interfaces

If $q_{iS} > 10^{-6}$:

$$\hat{q}_{1S} = \frac{a_{1S}}{A_{e1S}/q_{iS} - Z_S}$$

$$\hat{q}_{1D} = \frac{a_{1D}}{A_{e1D}/q_{iD} - Z_D}$$

$$k_1 h_{10} = \frac{i_{DS,norm}}{\hat{q}_{1S} - \hat{q}_{1D}}$$

$$\hat{q}_{2S} = \frac{a_{2S}}{A_{e2S}/q_{iS} - Z_S}$$

$$\hat{q}_{2D} = \frac{a_{2D}}{A_{e2D}/q_{iD} - Z_D}$$

$$k_2 h_{20} = \frac{i_{DS,norm}}{\hat{q}_{2S} - \hat{q}_{2D}}$$

© 2023 Cadence Design Systems, Inc.

Else:

$$\zeta_1 = -2s_1\left(\frac{1}{k_1\hat{q}_{1\infty}} + \frac{1}{d_\infty}\right)$$

$$\zeta_2 = -2s_2\left(\frac{1}{k_2\hat{q}_{2\infty}} + \frac{1}{d_\infty}\right)$$

$$\xi_1 = \frac{\zeta_2/k_2 + (\zeta_2 - \zeta_1)/d_\infty - (\zeta_1/k_1 + \zeta_2/k_2)/\hat{q}_{1\infty}}{3 + 2(s_1/k_1 + s_2/k_2)}$$

$$\xi_2 = \frac{\zeta_1/k_1 + (\zeta_1 - \zeta_2)/d_\infty - (\zeta_2/k_2 + \zeta_1/k_1)/\hat{q}_{2\infty}}{3 + 2(s_2/k_2 + s_1/k_1)}$$

$$k_1h_{10} = -\frac{1}{\hat{q}_{1\infty}(\xi_1\hat{q}_{1\infty} + 1/d_\infty)}$$

$$k_2h_{20} = -\frac{1}{\hat{q}_{2\infty}(\xi_2\hat{q}_{2\infty} + 1/d_\infty)}$$

$$k_1h_1 = k_1h_{10}\frac{\sqrt{1 + z_{sat}}}{1 + 3z_{sat}/2}$$

$$k_2h_2 = k_2h_{20}\frac{\sqrt{1 + z_{sat}}}{1 + 3z_{sat}/2}$$

$$\Delta_{k1q1} = \frac{k_1q_{1D} - k_1q_{1S}}{2}$$

$$\Delta_{k2q2} = \frac{k_2q_{2D} - k_2q_{2S}}{2}$$

$$P_1 = \frac{\Delta_{k1q1}}{k_1h_1}$$

$$P_2 = \frac{\Delta_{k2q2}}{k_2h_2}$$

© 2023 Cadence Design Systems, Inc.

Surface potential and gate dielectric voltage drop in gate-source overlap region

$$G_{ov} = \frac{\sqrt{2q\epsilon_{ch}\mathbf{NOV} \times 10^6}}{C'_{ox1}\sqrt{\phi_{T0}}}$$

$$\xi_{ov} = 1 + \frac{G_{ov}}{\sqrt{2}}$$

$$\xi_{mrg,ov} = 10^{-5}\xi_{ov}$$

$$x_{g1,ov} = 1.25 + 0.7324648775 G_{ov}$$

$$x_{S,ov} = \text{SP_FDSOI_OV}(x_{gs,ov})$$

$$x_{S,ovcv} = \text{SP_FDSOI_OV}(x_{gs,ovcv})$$

$$V_{ovS} = -\phi_{T0}(x_{gs,ov} + x_{S,ov})$$

$$V_{ovS,cv} = -\phi_{T0}(x_{gs,ovcv} + x_{S,ovcv})$$

Surface potential and gate dielectric voltage drop in gate-drain overlap region

$$G_{ov} = \frac{\sqrt{2q\epsilon_{ch}\mathbf{NOVD} \times 10^6}}{C'_{ox1}\sqrt{\phi_{T0}}}$$

$$\xi_{ov} = 1 + \frac{G_{ov}}{\sqrt{2}}$$

$$\xi_{mrg,ov} = 10^{-5}\xi_{ov}$$

$$x_{g1,ov} = 1.25 + 0.7324648775 G_{ov}$$

$$x_{D,ov} = \text{SP_FDSOI_OV}(x_{gd,ov})$$

$$x_{D,ovcv} = \text{SP_FDSOI_OV}(x_{gd,ovcv})$$

© 2023 Cadence Design Systems, Inc.

$$V_{ovD} = -\phi_{T0}(x_{gd,ov} + x_{D,ov})$$

$$V_{ovD,cv} = -\phi_{T0}(x_{gd,ovcv} + x_{D,ovcv})$$

Gate current

The gate current calculation is not carried out when the flag **SWIGATE** is set to 0.

Gate to source overlap component

$$\psi_t = \text{MIN_FUNC}(V_{ovS} + D_{ov}, 0, 0.01)$$

$$G_{C2,oveff} = \frac{\mathbf{GC2OVACC} + \mathbf{GC2OVINV}\exp(x_{gs,ov}/2)}{1+\exp(x_{gs,ov}/2)}$$

$$G_{C3,oveff} = \frac{\mathbf{GC3OVACC} + \mathbf{GC3OVINV}\exp(x_{gs,ov}/2)}{1+\exp(x_{gs,ov}/2)}$$

$$G_{CQ,oveff} = \frac{G_{CQ,ovacc} + G_{CQ,ovinv}\exp(x_{gs,ov}/2)}{1+\exp(x_{gs,ov}/2)}$$

$$I_{G,oveff} = \frac{I_{G,ovacc} + I_{G,ovinv}\exp(x_{gs,ov}/2)}{1+\exp(x_{gs,ov}/2)}$$

$$I_{G,oveffFowler} = \frac{I_{G,fnovinv}\exp(x_{gs,ov}/2)}{1+\exp(x_{gs,ov}/2)} \times 10^{-6}$$

$$\begin{cases} z_g = \text{MIN_FUNC}\left(\frac{\sqrt{V_{ovS}{}^2+10^{-4}}}{\mathbf{CHIB}}, G_{CQ,oveff}, 10^{-6}\right) & \text{if } G_{C3,oveff} < 0 \\ z_g = \frac{\sqrt{V_{ovS}{}^2+10^{-4}}}{\mathbf{CHIB}} & \text{else} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$\Delta_{Si} = \exp\left(3 + x_{S,ov} + \frac{\psi_t}{\phi_{T0}}\right)$$

$$\Delta_{gate} = \exp\left(3 + x_{S,ov} + \frac{\psi_t - V_{GS}}{\phi_{T0}}\right)$$

$$f_{GS,ov} = \frac{1 + \exp(\mathbf{GCDOV}(V_{GD} - \mathbf{GCVDOV}))}{1 + \exp(\mathbf{GCDOV}(V_{GD} - \mathbf{GCVDOV}))\exp(\mathbf{GCDOV} \times V_{SD})}$$

$$\begin{aligned} I_{GS,ov} =& I_{G,oveff} \ln\left(\frac{1+\Delta_{Si}}{1+\Delta_{gate}}\right) \exp\left(B_{ov}\left(z_g(G_{C2,oveff} + z_g G_{C3,oveff}) - \frac{3}{2}\right)\right) \times f_{GS,ov} \\ & - I_{G,oveffowler} \exp\left(-B_{ov}\left(\frac{\mathbf{GCOVINVFN}}{z_g}\right)\right) \times f_{GS,ov} \end{aligned}$$

Gate to drain overlap component

$$\psi_t = \text{MIN_FUNC}(V_{ovD} + D_{ov}, 0, 0.01)$$

$$G_{C2,oveff} = \frac{\mathbf{GC2OVACC} + \mathbf{GC2OVINV}\exp(x_{gd,ov}/2)}{1 + \exp(x_{gd,ov}/2)}$$

$$G_{C3,oveff} = \frac{\mathbf{GC3OVACC} + \mathbf{GC3OVINV}\exp(x_{gd,ov}/2)}{1 + \exp(x_{gd,ov}/2)}$$

$$G_{CQ,oveff} = \frac{G_{CQ,ovacc} + G_{CQ,ovinv}\exp(x_{gd,ov}/2)}{1 + \exp(x_{gd,ov}/2)}$$

$$I_{G,oveff} = \frac{I_{G,ovaccD} + I_{G,ovinvD}\exp(x_{gd,ov}/2)}{1 + \exp(x_{gd,ov}/2)}$$

$$I_{G,oveffowler} = \frac{I_{G,fnovinvD}\exp(x_{gd,ov}/2)}{1 + \exp(x_{gd,ov}/2)} \times 10^{-6}$$

$$\begin{cases} z_g = \text{MIN_FUNC}\left(\frac{\sqrt{V_{ovD}{}^2 + 10^{-4}}}{\mathbf{CHIB}}, G_{CQ,oveff}, 10^{-6}\right) & \text{if } G_{C3,oveff} < 0 \\ z_g = \frac{\sqrt{V_{ovD}{}^2 + 10^{-4}}}{\mathbf{CHIB}} & \text{else} \end{cases}$$

© 2023 Cadence Design Systems, Inc.

$$\Delta_{Si} = \exp\left(3 + x_{D,ov} + \frac{\psi_t}{\phi_{T0}}\right)$$

$$\Delta_{gate} = \exp\left(3 + x_{D,ov} + \frac{\psi_t - V_{GD}}{\phi_{T0}}\right)$$

$$f_{GD,ov} = \frac{1 + \exp(\mathbf{GCDOV}(V_{GS} - \mathbf{GCVDOV}))}{1 + \exp(\mathbf{GCDOV}(V_{GS} - \mathbf{GCVDOV}))\exp(\mathbf{GCDOV} \times V_{DS})}$$

$$\begin{aligned} I_{GD,ov} =& I_{G,oveff} \ln\left(\frac{1+\Delta_{Si}}{1+\Delta_{gate}}\right) \exp\left(B_{ov}\left(z_g(G_{C2,oveff} + z_g G_{C3,oveff}) - \frac{3}{2}\right)\right) \times f_{GD,ov} \\ & - I_{G,oveffowlerD} \exp\left(-B_{ov}\left(\frac{\mathbf{GCOVINVFND}}{z_g}\right)\right) \times f_{GD,ov} \end{aligned}$$

Gate to channel component

$$x_{DS} = -2\Delta_{k1q1}/k_1$$

$$V_m = \phi_T\left(\frac{x_{DS}}{2} - \ln\left(\frac{1+\exp(x_{DS} - x_{Deff})}{2}\right)\right)$$

$$q_{1m} = \frac{q_{1S} + q_{1D}}{2}$$

$$V_{oxm} = \phi_T q_{1m}$$

$$\psi_t = \text{MIN_FUNC}(V_{oxm} + D_{ch}, 0, 0.01)$$

$$\begin{cases} z_g = \text{MIN_FUNC}\left(\frac{\sqrt{{V_{oxm}}^2 + 10^{-4}}}{\mathbf{CHIB}}, G_{CQ,ch}, 10^{-6}\right) & \text{if } \mathbf{GC3CH} < 0 \\ z_g = \frac{\sqrt{{V_{oxm}}^2 + 10^{-4}}}{\mathbf{CHIB}} & \text{else} \end{cases}$$

$$\Delta_{Si} = \exp\left(\left(x_{g1x} - q_{1m} + \frac{\psi_t - \alpha_b - V_m}{\phi_{T0}}\right) \times n_{iginv}\right)$$

$$\Delta_{gate} = \Delta_{Si} \exp\left(-\frac{V_{GS} - V_m}{\phi_T} \times n_{iginv}\right)$$

$$I_{GC0} = I_{G,inv} \ln\left(\frac{1+\Delta_{Si}}{1+\Delta_{gate}}\right) \exp\left(B_{ch}\left(z_g(\mathbf{GC2CH} + z_g\mathbf{GC3CH}) - \frac{3}{2}\right)\right)$$

© 2023 Cadence Design Systems, Inc.

Source/drain partitioning of gate to channel current

If $x_{g1x} > 0$:

$$u_0 = \frac{\mathbf{CHIB}/\phi_T}{B_{ch}(\mathbf{GC2CH} + 2z_g\mathbf{GC3CH})}$$

$$x = \frac{x_{DS}}{2u_0}$$

$$b = \frac{u_0}{k_1 h_1 / k_1}$$

$$B_g = \frac{b(1-b)}{2}$$

$$A_g = \frac{1}{2} - 3B_g$$

$$p_{GC} = (1-b)\frac{\sinh(x)}{x} + b\cosh(x)$$

$$p_{GD} = \frac{p_{GC}}{2} - B_g \sinh(x) - \frac{A_g}{x}\left(\cosh(x) - \frac{\sinh(x)}{x}\right)$$

Else:

$$p_{GC} = 1$$

$$p_{GD} = \frac{1}{2}$$

$$I_{GC} = I_{GC0} p_{GC}$$

$$I_{GCD} = I_{GC0} p_{GD}$$

$$I_{GCS} = I_{GC} - I_{GCD}$$

© 2023 Cadence Design Systems, Inc.

Gate to source and gate to drain total currents

$$I_{GS} = I_{GCS} + I_{GS,ov}$$

$$I_{GD} = I_{GCD} + I_{GD,ov}$$

Gate Induced Drain/Source Leakage (GIDL/GISL)

Gate induced source leakage

$$V_{tovS} = \sqrt{{V_{ovS}}^2 + \mathbf{CGIDL}^2 {V_{SB}}^2 + 10^{-6}}$$

$$I_{GISL} = -A_{GIDL} V_{SD} V_{ovS} V_{tovS} \exp\left(-\frac{B_{GIDL}}{V_{tovS}}\right) \frac{1 + \exp(\mathbf{DGIDL} \times V_{SD})}{2}$$

Gate induced drain leakage

$$V_{tovD} = \sqrt{{V_{ovD}}^2 + \mathbf{CGIDLD}^2 {V_{DB}}^2 + 10^{-6}}$$

$$I_{GIDL} = -A_{GIDLD} V_{DS} V_{ovD} V_{tovD} \exp\left(-\frac{B_{GIDLD}}{V_{tovD}}\right) \frac{1 + \exp(\mathbf{DGIDLD} \times V_{DS})}{2}$$

© 2023 Cadence Design Systems, Inc.

Impact ionization current

The following equations are only calculated when **SWIMPACT** = 1.

$$\Delta V_{sat} = (x_d - \mathbf{A3} \times x_{Deff}) \times \phi_T$$

$$M_{\text{avl}} = \begin{cases} 0 & \text{for } \Delta V_{sat} \leq 0 \\ \mathbf{A1} \times \Delta V_{sat} \times \exp\left(-\dfrac{a_2}{\Delta V_{sat}}\right) & \text{for } \Delta V_{sat} > 0 \end{cases}$$

$$I_{impact} = M_{avl} \times I_{DS}$$

Charge model

Quantum mechanical corrections

$$k_1 q_{1m} = \frac{k_1 q_{1S} + k_1 q_{1D}}{2} + \mathbf{FSCEAC} \frac{\delta x_{WI,1D} - \delta x_{WI}}{1 + q_{im}/4}$$

$$k_2 q_{2m} = \frac{k_2 q_{2S} + k_2 q_{2D}}{2} - \mathbf{FSCEAC} \frac{\delta x_{WI,1D} - \delta x_{WI}}{1 + q_{im}/4}$$

$$\begin{cases} k_1 q_{1eff} = k_1 q_{1m} - \frac{qm_{fact1}-1}{qm_{fact1}} q_{i1m} & \text{if } \mathbf{QMC} > 0 \\ k_1 q_{1eff} = k_1 q_{1m} & \text{else} \end{cases}$$

$$\begin{cases} k_2 q_{2eff} = k_2 q_{2m} - \frac{qm_{fact2}-1}{qm_{fact2}} q_{i2m} & \text{if } \mathbf{QMC} > 0 \\ k_2 q_{2eff} = k_2 q_{2m} & \text{else} \end{cases}$$

Intrinsic charge model

$$Q_G = C'_{Si} f_{area} \left(k_1 q_{1eff} + \frac{\Delta_{k1q1}}{3} P_1 \right)$$

© 2023 Cadence Design Systems, Inc.

$$Q_B = C'_{Si} f_{area} \left(k_2 q_{2eff} + \frac{\Delta_{k2q2}}{3} P_2 \right)$$

$$Q_D = -\frac{C'_{Si} f_{area}}{2} \left(k_1 q_{1eff} + \frac{\Delta_{k1q1}}{3} \left(1 + P_1 - \frac{{P_1}^2}{5} \right) + k_2 q_{2eff} + \frac{\Delta_{k2q2}}{3} \left(1 + P_2 - \frac{{P_2}^2}{5} \right) \right)$$

Parasitic charges

Inner fringe charges are computed if **FIF** > 0.

$$x_{effS} = x_{driftS} + x_{th,1D} + 2\ln(2)$$

$$x_{effD} = x_{driftD} + x_{th,1D} + 2\ln(2)$$

$$x_S^* = \text{MIN_FUNC}(x_{effS}, x_{th,1D}, 9.0)$$

$$x_D^* = \text{MIN_FUNC}(x_{effD}, x_{th,1D} + x_D, 9.0)$$

$$\lambda_f = \lambda_{2D} \sqrt{k_{eq} \left(\frac{1}{2} + \frac{1}{k_2} \right)}$$

$$\lambda_b = \lambda_{2D} \sqrt{k_{eq} \frac{k_1}{k_2} \left(\frac{1}{2} + \frac{1}{k_1} \right)}$$

$$x_{\alpha f} = {\lambda_f}^2 f_{SD,inner}$$

$$x_{\alpha b} = {\lambda_b}^2 f_{SD,inner}$$

$$x_{edge,fS} = x_S^* + 2x_{\alpha f} \left(\sqrt{1 + \frac{x_{SD} - x_S^*}{x_{\alpha f}}} - 1 \right)$$

$$x_{edge,fD} = x_D^* + 2x_{\alpha f} \left(\sqrt{1 + \frac{x_{SD} + x_D - x_D^*}{x_{\alpha f}}} - 1 \right)$$

© 2023 Cadence Design Systems, Inc.

$$x_{edge,bS} = x_S^* + 2x_{\alpha b}\left(\sqrt{1 + \frac{x_{SD} - x_S^*}{x_{\alpha b}}} - 1\right)$$

$$x_{edge,bD} = x_D^* + 2x_{\alpha b}\left(\sqrt{1 + \frac{x_{SD} + x_D - x_D^*}{x_{\alpha b}}} - 1\right)$$

$$Q_{GS,if} = -f_{if}C'_{Si}\lambda_f k_1 c_{sce1}\frac{\text{MAX_FUNC}(x_{edge,fS} - x_{effS}, 0.0, 1.0)^2}{x_{edge,fS} - x_S^*}$$

$$Q_{GD,if} = -f_{if}C'_{Si}\lambda_f k_1 c_{sce1}\frac{\text{MAX_FUNC}(x_{edge,fD} - x_{effD}, 0.0, 1.0)^2}{x_{edge,fD} - x_D^*}$$

$$Q_{BS,if} = -f_{if}C'_{Si}\lambda_b k_2 c_{sce2}\frac{\text{MAX_FUNC}(x_{edge,bS} - x_{effS}, 0.0, 1.0)^2}{x_{edge,bS} - x_S^*}$$

$$Q_{BD,if} = -f_{if}C'_{Si}\lambda_b k_2 c_{sce2}\frac{\text{MAX_FUNC}(x_{edge,bD} - x_{effD}, 0.0, 1.0)^2}{x_{edge,bD} - x_D^*}$$

Outer fringe and overlap charges:

$$Q_{GS} = \mathbf{CFR} \times V_{GS}$$

$$Q_{GD} = \mathbf{CFRD} \times V_{GD}$$

$$Q_{ovS} = \mathbf{COV} \times V_{ovS,cv}\text{MAX_FUNC}(1 - \mathbf{COVDL} \times \delta l_{eff}(1 - \mathbf{COVDLB} \times x_{g20}), 0.0, 0.01)$$

$$Q_{ovD} = \mathbf{COVD} \times V_{ovD,cv}\text{MAX_FUNC}(1 - \mathbf{COVDL} \times \delta l_{eff}(1 - \mathbf{COVDLB} \times x_{g20}), 0.0, 0.01)$$

$$Q_{GB} = \mathbf{CGBOV} \times V_{GB}$$

Drain to source direct coupling:

$$Q_{DS} = \mathbf{CSD} \times V_{DS}$$

© 2023 Cadence Design Systems, Inc.

Substrate extrinsic charge model:

$$Q_{BS} = -\left(\frac{\epsilon_{ox}}{\mathbf{TBOX}} \times A_{source,f} + \mathbf{CSDBP} \times P_{source,f}\right) V_{SB}$$

$$Q_{BD} = -\left(\frac{\epsilon_{ox}}{\mathbf{TBOX}} \times A_{drain,f} + \mathbf{CSDBP} \times P_{drain,f}\right) V_{DB}$$

Self-heating

A temperature node named `Tnode` is used to compute the channel temperature elevation induced by the self-heating effect.

$$\Delta T_C = \text{Temp}(\text{Tnode})$$

$$I_{th} = \frac{\Delta T_C}{R_{th}} - I_{DS}V_{DS}$$

$$Q_{th} = \mathbf{CTH} \times \Delta T_C$$

Noise model

Channel thermal noise

$$d_m = -\frac{d_S + d_D}{2}$$

$$q_{im}^* = q_{im} + d_m$$

$$t_1 = \frac{q_{im}}{q_{im}^*}$$

$$t_2 = \left(-\frac{\Delta_{k1q1}}{6k_1h_{10}}\right)^2$$

$$R = \frac{1 + 3z_{sat}/2}{\sqrt{1 + z_{sat}}} - 1$$

© 2023 Cadence Design Systems, Inc.

$$l_C = 1 - 12t_2R$$

$$g_{ideal} = \beta_{Neff} C'_{Si} \phi_T q^*_{im} \frac{F_{\Delta L}}{G_{vsat} qm_{fact}}$$

$$\begin{cases} S_{ids,exc} = f_{exc} \frac{I_{DS} x_{Deff} \phi_{T0}}{{l_C}^2 (1 + {G_\gamma}^2 / {G_{mob}}^2)} & \text{if } \mathbf{FNTEXC} > 0 \\ S_{ids,exc} = 0 & \text{else} \end{cases}$$

$$g_{Sid} = \frac{g_{ideal}}{{l_C}^2}(t_1 + 12t_2 - 24(1 + t_1)t_2R) + \frac{S_{ids,exc}}{n_{T0}}$$

$$S_{ids,th} = n_T g_{Sid}$$

Induced gate noise

Induced gate noise and its correlation with drain thermal noise are computed only when the **SWIGN** flag is set to 1.

$$C_{Geff} = (1 + z_{sat}) \frac{k_1 C'_{Si}}{qm_{fact1}} \mathbf{AREAQ}$$

$$g_{Sig} = \frac{g_{ideal} {l_C}^2}{t_1/12 - (1/5 + t_1 - 12t_2)t_2 - 8/5(1 + t_1 - 12t_2)t_2R}$$

$$S_{ig,th} = n_T g_{Sig} \frac{(2\pi f_{op} C_{Geff} / g_{Sig})^2}{1 + (2\pi f_{op} C_{Geff} / g_{Sig})^2}$$

The gate induced noise current is finally partitioned between the gate-source and the gate-drain branches, with a V_{DS} dependent fraction equal to $1/2 + (\sqrt{t_2})/4$ and $1/2 - (\sqrt{t_2})/4$ respectively. The noise currents in these two branches are thus perfectly correlated and correspond to the following spectral densities:

© 2023 Cadence Design Systems, Inc.

$$S_{igs,th} = \left(\frac{1}{2} + \frac{\sqrt{t_2}}{4}\right)^2 S_{ig,th}$$

$$S_{igd,th} = \left(\frac{1}{2} - \frac{\sqrt{t_2}}{4}\right)^2 S_{ig,th}$$

Drain and gate thermal noise correlation

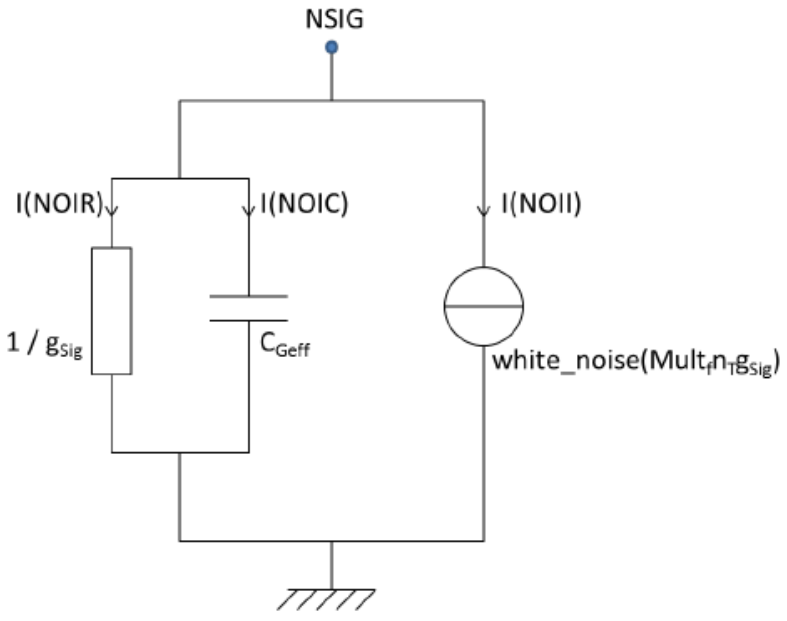
$$m_{igid} = \frac{\sqrt{t_2}}{{l_C}^2}(1 - 12t_2 - (t_1 + 96t_2/5 - 12t_1t_2)t_2R)$$

$$S_{igid,th} = n_T \frac{2j\pi f_{op} C_{Geff} m_{igid}}{1 + 2j\pi f_{op} C_{Geff}/g_{Sig}}$$

VerilogA implementation of induced gate noise and correlation

As there is no noise function with frequency dependence suitable for the induced gate noise in VerilogA, an internal node NSIG linked to the ground through a parallel RC circuit is used.

Consider the following circuit:



© 2023 Cadence Design Systems, Inc.

The equivalent circuit is described in the figure shown above and the currents in the different branches are given by:

$$I(\text{NOIR}) = g_{Sig} V(\text{NSIG})$$

$$I(\text{NOIC}) = \frac{d}{dt}\left(C_{Geff} V(\text{NSIG})\right)$$

$$I(\text{NOII}) = \text{white_noise}(Mult_f n_T g_{Sig})$$

The noise current in the gate-source and gate-drain branches is obtained by:

$$I_{gs,th} = \frac{d}{dt}\left(-\left(\frac{1}{2} + \frac{\sqrt{t_2}}{4}\right) C_{Geff} V(\text{NSIG})\right)$$

$$I_{gd,th} = \frac{d}{dt}\left(-\left(\frac{1}{2} - \frac{\sqrt{t_2}}{4}\right) C_{Geff} V(\text{NSIG})\right)$$

A variable c_{igid} is then defined to obtain the correct correlation between the drain thermal noise current and the gate induced one:

$$c_{igid} = m_{igid}\sqrt{\frac{g_{Sig}}{g_{Sid}}}$$

The channel thermal noise current is finally given as the sum of an uncorrelated part and a correlated one:

$$I_{ds,th} = \text{white_noise}\left(Mult_f S_{ids,th}(1 - {c_{igid}}^2)\right) + m_{igid} I(\text{NOII})$$

Channel flicker noise

$$N_{unit} = \frac{C'_{Si}\phi_T}{q}$$

$$N^* = N_{unit}$$

$$N^*_m = N_{unit}(q_{im} + 1)$$

$$\Delta N = N_{unit}(q_{iS} - q_{iD})$$

© 2023 Cadence Design Systems, Inc.

$$\Delta N = N_{unit}(q_{iS} - q_{iD})$$

$$f_{NFE} = \text{MAX_FUNC}\left(1 + \frac{e_{surf1}\mathbf{NFE} + e_{surf2}\mathbf{NFEB}}{q_{im} + 1}, 0.01, 0.0001\right)$$

$$S_{ids,fl} = \frac{q\beta_{Neff}{\phi_T}^2 I_{DS}}{{f_{op}}^{\mathbf{EF}} G_{vsat} N^*} f_{NFE} \times$$
$$\left(\left(\mathbf{NFA} - N^*\mathbf{NFB} + {N^*}^2\mathbf{NFC}\right)\ln\left(\frac{N_m^* + \Delta N/2}{N_m^* - \Delta N/2}\right) + \left(\mathbf{NFB} + \mathbf{NFC}(N_m^* - 2N^*)\right)\Delta N\right)$$

Shot noises

Gate current shot noise

$$S_{igs,sh} = 2q|I_{GS}|$$

$$S_{igd,sh} = 2q|I_{GD}|$$

GIDL/GISL current shot noise

$$S_{ids,sh} = 2q|I_{GIDL} - I_{GISL}|$$

Impact ionization current shot noise

$$S_{avl} = 2q \times (M_{avl} + 1) \times |I_{impact}|$$

Total currents and charges

Static currents

$$I_{DS,dc} = Mult_f \times \mathbf{TYPE} \times (I_{DS} + I_{GIDL} - I_{GISL} + I_{impact})$$

$$I_{GS,dc} = Mult_f \times \mathbf{TYPE} \times I_{GS}$$

© 2023 Cadence Design Systems, Inc.

$$I_{GD,dc} = Mult_f \times \mathbf{TYPE} \times I_{GD}$$

$$I_{BS,dc} = 0$$

$$I_{BD,dc} = 0$$

$$I_{GB,dc} = 0$$

Total charges

$$Q_{G,tot} = Mult_f \times \mathbf{TYPE} \times (Q_G + Q_{GS,if} + Q_{GD,if} + Q_{GS} + Q_{GD} + Q_{ovS} + Q_{ovD} + Q_{GB})$$

$$Q_{D,tot} = Mult_f \times \mathbf{TYPE} \times (Q_D + Q_{DS} - Q_{GD,if} - Q_{GD} - Q_{ovD} - Q_{BD,if} - Q_{BD})$$

$$Q_{B,tot} = Mult_f \times \mathbf{TYPE} \times (Q_B + Q_{BS,if} + Q_{BD,if} + Q_{BS} + Q_{BD} - Q_{GB})$$

$$Q_{S,tot} = -Q_{G,tot} - Q_{D,tot} - Q_{B,tot}$$

Dynamic currents

$$I_{DS,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_D + Q_{DS})/dt$$

$$I_{GS,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_G + Q_{GS,if} + Q_{GS} + Q_{ovS})/dt$$

$$I_{GD,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_{GD,if} + Q_{GD} + Q_{ovD})/dt$$

$$I_{BS,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_B + Q_{BS,if} + Q_{BS})/dt$$

$$I_{BD,ac} = Mult_f \times \mathbf{TYPE} \times d(Q_{BD,if} + Q_{BD})/dt$$

$$I_{GB,ac} = Mult_f \times \mathbf{TYPE} \times dQ_{GB}/dt$$

© 2023 Cadence Design Systems, Inc.

Component Statements

Model Definition

```
model modelName lutsoi parameter=value ...
```

Instance Definition

```
Name  d  g  s  b [Tnode] ModelName parameter=value ...
```


© 2023 Cadence Design Systems, Inc.

Instance Parameters

l	1.0e-06 m	Channel length.
w	1.0e-06 m	Channel width.
asource	1.0e-12 m^2	Source region area.
adrain	1.0e-12 m^2	Drain region area.
psource	1.0e-06 m	Source region perimeter.
pdrain	1.0e-06 m	Drain region perimeter.
sa	0.0 m	Distance between OD-edge and poly at source side.
sb	0.0 m	Distance between OD-edge and poly at drain side.
sd	0.0 m	Distance between neighboring fingers.
nf	1	Number of fingers.
m	1.0	Number of devices in parallel.
delvto	0.0 V	Threshold voltage shift parameter.
factuo	1.0	Low-field mobility pre-factor.
trise	0.0	Temperature rise from ambient.
dtemp	0.0	Temperature rise from ambient.
isnoisy	yes	Should device generate noise.

© 2023 Cadence Design Systems, Inc.

Model Parameters

swscale	0	Parameter set mode (local=0, global=1).
version	102.4	Model version.
swsubdep	0	Flag for substrate depletion model (without=0, with=1).
swigate	0	Flag for gate current (without=0, with=1).
swgidl	0	Flag for GIDL current (without=0, with=1).
swshe	0	Flag for self heating effect (without=0, with=1).
swign	1	Flag for induced gate noise model (without=0, with=1).
swjunasym	0	Flag for source/drain junction asymmetry (without=0, with=1).
swimpact	0	Flag for impact ionization current (without=0, with=1).
qmc	1.0	Quantum correction factor (no correction=0, full correction=1).
type	1	Channel type parameter, +1=NMOS - 1=PMOS.Possible values are p and n.
tr	21.0 C	Nominal temperature.
tref	21.0 C	Alias of TR, nominal temperature.
tmax	150.0 C	Maximum self-heating temperature elevation.

© 2023 Cadence Design Systems, Inc.

vthmod		Vth output selector. 'std' outputs model equation Vth. 'vthcc' outputs constant current Vth, and may impact simulation performance. The default value is taken from the options parameter 'vthmod'.Possible values are std and vthcc.
ivth	0.0	Vth current parameter. The default value is taken from the options parameter 'ivthn' or 'ivthp', depending on the type of the model.
ivthw	0.0	Width offset for constant current Vth. The default value is taken from the options parameter 'ivthw'.
ivthl	0.0	Length offset for constant current Vth. The default value is taken from the options parameter 'ivthl'.
ivth_vdsmin	0.05	Minimum Vds in constant current Vth calculating. The default value is taken from the options parameter 'ivth_vdsmin'.
toxe	2.0e-09 m	Front gate equivalent oxide thickness.
tsi	1.0e-08 m	Silicon or SiGe film thickness.
xge	0.0	Fraction of Ge content in the channel.
tbox	1.0e-07 m	Buried oxide thickness.
nch	0.0 cm^{-3}	Thin film doping (n-type=negative value, p-type=positive value).
nsub	3.0e18 cm^{-3}	Substrate doping (n-type=negative value, p-type=positive value).
ct	0.0	Interface states factor.

© 2023 Cadence Design Systems, Inc.

toxp	2.0e-09 m	Front gate physical oxide thickness.
nov	1.0e20 cm^{-3}	Effective doping of overlap-ldd regions.
novd	1.0e20 cm^{-3}	Effective doping of overlap-ldd regions ar drain side.
vfb	0.0 V	Flat-band voltage of the front gate at TR.
vfbb	0.0 V	Flat-band voltage of the back gate at TR.
stvfb	0.0 V/K	Temperature dependence of VFB and VFBB.
cicf	1.0	Long channel front interface coupling coefficient.
cic	1.0	Long channel back interface coupling coefficient.
psce	0.0	Short channel effect coefficient.
psceb	1.0	Short channel back to front interface asymmetry factor.
nsddc	1.0e22 cm^{-3}	Source/Drain effective doping level for DC model.
pscedlb	0.0	Back bias dependence of short channel effect modulation.
pnce	0.0	Narrow channel effect on body factor.
cf	0.0	DIBL parameter.
cfb	1.0	DIBL back to front interface asymmetry factor.
stcf	0.0 1/K	Temperature dependence of CF, with same scaling as CF.

© 2023 Cadence Design Systems, Inc.

cfd	0.2 V	Drain voltage dependence parameter of DIBL.
cfdl	0.0	DIBL modulation coefficient due to Leff variation.
cfdlb	0.0	Back bias dependence of DIBL modulation.
betn	5.0e-02 $m^2/V/s$	Front channel aspect ratio times zero-field mobility.
betnb	1.0	Back channel over front channel zero-field mobility ratio.
stbet	1.5	Temperature dependence of BETN.
cs	0.0	Remote Coulomb scattering parameter at TR.
csfi	0.0	Field dependence of Coulomb scattering at front interface.
csbi	0.0	Field dependence of Coulomb scattering at back interface.
stcs	0.0	Temperature dependence of CS.
thecs	1.5	Remote Coulomb scattering exponent at TR.
stthecs	0.0	Temperature dependence of THECS.
csthr	2.0	Remote Coulomb scattering threshold level.
csthrb	1.0	Remote Coulomb scattering threshold asymmetry parameter.
mue	0.0 cm/MV	Front channel mobility reduction coefficient at TR.
stmue	0.0	Temperature dependence of MUE.
themu	1.5	Front channel mobility reduction exponent at TR.

© 2023 Cadence Design Systems, Inc.

stthemu	0.0	Temperature dependence of THEMU.
xcor	0.0	Front channel non-universality factor.
xcorb	1.0	Asymmetry term of non-universality factor.
stxcor	0.0	Temperature dependence of XCOR.
feta	1.0	Effective field parameter.
rs	30.0 Ω	Source/Drain series resistance at TR.
rsig	0.0	Source/Drain extension resistance coefficient.
strs	0.0	Temperature dependence of RS.
rsg	0.0	Transverse electric field dependence of RS.
thersg	2.0	Transverse electric field dependence exponent of RS.
rsb	0.0	Back bias dependence of RS.
thesat	0.0 V^-1	Velocity saturation parameter at TR.
stthesat	(-0.1)	Temperature dependence of THESAT.
thesatg	0.0	Front gate bias dependence of velocity saturation.
thesatb	0.0	Back gate bias dependence of velocity saturation.
ax	8.0	Linear/saturation transition exponent.
alp	0.0	CLM pre-factor.
alp1	0.0 V	CLM enhancement factor above threshold.

© 2023 Cadence Design Systems, Inc.

alpb	0.0	Back bias dependence of channel length modulation.
vp	0.05 V	CLM logarithm dependence factor.
vpg	0.0	Transverse electric field dependence of CLM logarithm factor.
gco	0.0	Gate tunneling energy adjustment in inversion.
iginv	0.0 A	Gate to channel current pre-factor.
igovinv	0.0 A	Gate to overlap current pre-factor in inversion.
igovinvd	0.0 A	Gate to overlap current pre-factor in inversion at drain side.
igovacc	0.0 A	Gate to overlap current pre-factor in accumulation.
igovaccd	0.0 A	Gate to overlap current pre-factor in accumulation at drain side.
stig	0.0	Temperature dependence of all gate currents.
gc2ch	0.375	Gate to channel current slope factor.
gc3ch	0.063	Gate to channel current curvature factor.
gc2ovinv	0.375	Gate current slope factor for overlap regions in inversion mode.
gc3ovinv	0.063	Gate current curvature factor for overlap regions in inversion mode.
gc2ovacc	0.375	Gate current slope factor for overlap regions in accumulation mode.
gc3ovacc	0.063	Gate current curvature factor for overlap regions in accumulation mode.

© 2023 Cadence Design Systems, Inc.

gcdov	0.0 V^-1	High drain voltage dependence of overlap gate current.
gcvdov	1.0 V	Threshold of high drain voltage effect on overlap gate current.
chib	3.1 V	Tunneling barrier height.
niginv	0.0	Gate tunneling slope adjustment in subthreshold regime.
fnovinv	0.0 A	Extra gate to overlap current pre-factor in inversion.
fnovinvd	0.0 A	Extra gate to overlap current pre-factor in inversion at drain side.
gcovinvfn	0.2	Extra gate current slope factor for overlap regions in inversion mode.
stigfn	0.0	Temperature dependence of extra gate to overlap current.
agidl	0.0 A/V^3	GIDL pre-factor.
agidld	0.0 A/V^3	GIDL pre-factor at drain side.
bgidl	41.0 V	GIDL probability factor at TR.
bgidld	41.0 V	GIDL probability factor at TR at drain side.
stbgidl	0.0 V/K	Temperature dependence of BGIDL.
stbgidld	0.0 V/K	Temperature dependence of BGIDL at drain side.
cgidl	0.0 V^-1	Substrate bias dependence of GIDL.
cgidld	0.0 V^-1	Substrate bias dependence of GIDL at drain side.
dgidl	0.0 V^-1	High longitudinal field parameter of GIDL.

© 2023 Cadence Design Systems, Inc.

dgidld	0.0 V^-1	High longitudinal field parameter of GIDL at drain side.
a1	1.0	Impact ionization pre-factor.
a2	10.0	Impact ionization exponent at TR.
sta2	0.0	Temperature dependence of A2.
a3	1.0	Saturation voltage dependence of impact-ionization.
areaq	1.0e-12 m^2	Effective channel area for intrinsic CV.
cgbov	0.0 F	Oxide capacitance for gate-substrate overlap.
nsdac	1.0e22 cm^{-3}	Source/Drain effective doping level for AC model.
fif	0.0	Inner fringe capacitance prefactor.
fsceac	0.0	Short channel effect adjustment factor for charge model.
cov	0.0 F	Overlap capacitance per side.
covd	0.0 F	Overlap capacitance at drain side.
covdl	0.0	Overlap capacitance modulation coefficient due to Leff variation.
covdlb	0.0	Overlap capacitance modulation with back bias.
dvfbov	0.0 V	Overlap capacitance flat-band voltage adjustment.
cfr	0.0 F	Outer fringe capacitance per side.
cfrd	0.0 F	Outer fringe capacitance at drain side.

© 2023 Cadence Design Systems, Inc.

csd	1.04e-18 F	Drain-source capacitance.
csdbp	0.0 F/m	Drain/source to substrate perimeter capacitance.
rth	1.0e04 K/W	Thermal resistance.
strth	0.0	Temperature dependence of RTH.
cth	1.0e-11 J/K	Thermal capacitance.
fnt	1.0	Thermal noise coefficient.
fntexc	0.0	Excess noise coefficient.
nfa	8.0e22 V^-1/m^4	First coefficient of flicker noise.
nfb	3.0e07 V^-1/m^2	Second coefficient of flicker noise.
nfc	0.0 V^-1	Third coefficient of flicker noise.
nfe	0.0	Flicker noise front transverse field effect coefficient.
nfeb	0.0	Flicker noise back transverse field effect coefficient.
ef	1.0	Frequency coefficient of flicker noise.
kdrift	1.0	Drift component parameter of NQS effect.
kdiff	1.0	Diffusion component parameter of NQS effect.
fracinv	1.0	Fraction of inversion charge for the second pole of the NQS transition.

© 2023 Cadence Design Systems, Inc.

kfracinv	1.0e-15	Second pole frequency coefficient of the NQS transition.
swnqs	0	Non-quasi-static model flag. When model parameter SWNQS is set to 1 or 0, the NQS effect is open or closed, respectively.
lvaro	0.0 m	Geometry independent difference between physical and drawn gate lengths.
lvarl	0.0	Length dependence of LPS.
lvarw	0.0	Width dependence of LPS.
lap	0.0 m	Effective channel length reduction per side.
wvaro	0.0 m	Geometry-independent difference between physical and drawn field-oxide opening.
wvarl	0.0	Length dependence of WOD.
wvarw	0.0	Width dependence of WOD.
wot	0.0 m	Effective reduction of channel width per side.
dlq	0.0 m	Effective channel length additional offset for charge model.
dwq	0.0 m	Effective channel width additional offset for charge model.
toxeo	2.0e-09 m	Front gate equivalent oxide thickness.
tsio	1.0e-08 m	Silicon or SiGe film thickness.
xgeo	0.0	Fraction of Ge content in the channel.

© 2023 Cadence Design Systems, Inc.

tboxo	1.0e-07 m	Buried oxide thickness.
ncho	0.0 cm^{-3}	Thin film doping (n-type=negative value, p-type=positive value).
nsubo	3.0e18 cm^{-3}	Substrate doping (n-type=negative value, p-type=positive value).
cto	0.0	Interface states factor.
toxpo	2.0e-09 m	Front gate physical oxide thickness.
novo	1.0e20 cm^{-3}	Effective doping of overlap-ldd regions.
novdo	1.0e20 cm^{-3}	Effective doping of overlap-ldd regions at drain side.
vfbo	0.0 V	Geometry-independent front gate flat-band voltage at TR.
vfbl	0.0 V	Length dependence of VFB.
vfblexp	2.0	Exponent describing length dependence of VFB.
vfbl2	0.0	Second order length dependence of VFB.
vfblexp2	2.0	Exponent of second order length dependence of VFB.
vfbw	0.0 V	Width dependence of VFB.
vfblw	0.0 V	Area dependence of VFB.
vfbbo	0.0 V	Geometry-independent back gate flat-band voltage at TR.

© 2023 Cadence Design Systems, Inc.

vfblbo	0.0	Roll-off back to front interface asymmetry factor.
stvfbo	0.0 V/K	Geometry-independent temperature dependence of VFB and VFBB.
stvfbl	0.0	Length dependence of STVFB.
stvfbw	0.0	Width dependence of STVFB.
stvfblw	0.0	Area dependence of STVFB.
cicfo	1.0	Long channel front interface coupling coefficient.
cico	1.0	Long channel back interface coupling coefficient.
pscel	0.0	Length dependence of PSCE.
pscelexp	2.0	Exponent describing length dependence of PSCE.
pscew	0.0	Width dependence of PSCE.
pscebo	1.0	Short channel back to front interface asymmetry factor.
nsddco	1.0e22 cm^{-3}	Source/Drain effective doping level for DC model.
pscedlbo	0.0	Back bias dependence of short channel effect modulation.
pncew	0.0	Narrow channel effect on body factor for a width of WEN.
cfl	0.0	Length dependence of DIBL-parameter.
cflexp	2.0	Exponent for length dependence of CF.
cfw	0.0	Width dependence of CF.

© 2023 Cadence Design Systems, Inc.

cfbo	1.0	DIBL back to front interface asymmetry factor.
stcfl	0.0 1/K	Temperature dependence of CF, with same scaling as CF.
cfdo	0.2 V	Drain voltage dependence parameter of DIBL.
cfdll	0.0	DIBL modulation coefficient due to Leff variation.
cfdlw	0.0	Width dependence of CFDL.
cfdlbo	0.0	Back bias dependence of DIBL modulation.
uo	5.0e-02 $m^2/V/s$	Front channel zero-field mobility at TR.
fbet1	0.0	First length dependence modulation of BETN.
fbet1w	0.0	Width dependence of FBET1.
lp1	1.0e-08 m	First characteristic length of BETN scaling.
lp1w	0.0	Width dependence of LP1.
fbet2	0.0	Second length dependence modulation of BETN.
lp2	1.0e-08 m	Second characteristic length of BETN scaling.
betw1	0.0	First width dependence modulation of BETN.
betw2	0.0	Second width dependence modulation of BETN.
wbet	1.0e-08 m	Characteristic width of BETN scaling.
betnbo	1.0	Back channel over front channel zero-field mobility ratio.

© 2023 Cadence Design Systems, Inc.

stbeto	1.5	Geometry independent temperature dependence of BETN.
stbetl	0.0	Length dependence of STBET.
stbetw	0.0	Width dependence of STBET.
stbetlw	0.0	Area dependence of STBET.
cso	0.0	Remote Coulomb scattering parameter at TR.
csl	0.0	Length dependence of CS.
cslexp	1.0	Exponent describing length dependence of CS.
csw	0.0	Width dependence of CS.
cslw	0.0	Area dependence of CS.
csfio	0.0	Field dependence of Coulomb scattering at front interface.
csbio	0.0	Field dependence of Coulomb scattering at back interface.
stcso	0.0	Temperature dependence of CS.
stcsl	0.0	Length dependence of STCS.
stcsw	0.0	Width dependence of STCS.
stcslw	0.0	Area dependence of STCS.
thecso	1.5	Remote Coulomb scattering exponent at TR.
stthecso	0.0	Temperature dependence of THECS.
csthro	2.0	Remote Coulomb scattering threshold level.

© 2023 Cadence Design Systems, Inc.

csthrbo	1.0	Remote Coulomb scattering threshold asymmetry parameter.
mueo	0.0 cm/MV	Front channel mobility reduction coefficient at TR.
stmueo	0.0	Temperature dependence of MUE.
themuo	1.5	Front channel mobility reduction exponent at TR.
stthemuo	0.0	Temperature dependence of THEMU.
xcoro	0.0	Geometry-independent part of non-universality factor.
xcorl	0.0	Length dependence of XCOR.
xcorlexp	1.0	Exponent describing length dependence of XCOR.
xcorw	0.0	Width dependence of XCOR.
xcorlw	0.0	Area dependence of XCOR.
xcorbo	1.0	Asymmetry term of non-universality factor.
stxcoro	0.0	Temperature dependence of XCOR.
fetao	1.0	Effective field parameter.
rsw1	30.0 Ω	Source/Drain series resistance for channel width WEN at TR.
rsw2	0.0	Higher-order width scaling of source/drain series resistance.
rsigo	0.0	Source/Drain extension resistance coefficient.
strso	0.0	Temperature dependence of RS.

© 2023 Cadence Design Systems, Inc.

rsgo	0.0	Transverse electric field dependence of RS.
thersgo	2.0	Transverse electric field dependence exponent of RS.
rsbo	0.0	Back bias dependence of RS.
thesato	0.0 s/m^2	Geometry independent velocity saturation parameter at TR.
thesatl	0.0 s/m^2	Length dependence of THESAT.
thesatlexp	1.0	Exponent for length dependence of THESAT.
thesatw	0.0	Width dependence of THESAT.
thesatlw	0.0	Area dependence of THESAT.
stthesato	(-0.1)	Geometry independent temperature dependence of THESAT.
stthesatl	0.0	Length dependence of STTHESAT.
stthesatw	0.0	Width dependence of STTHESAT.
stthesatlw	0.0	Area dependence of STTHESAT.
thesatgo	0.0	Front gate bias dependence of velocity saturation.
thesatbo	0.0	Back gate bias dependence of velocity saturation.
axo	8.0	Geometry independent linear/saturation transition exponent.
axl	0.0	Length dependence of AX.
axlexp	1.0	Exponent for length dependence of AX.
axl2	0.0	Second order length dependence of AX.

© 2023 Cadence Design Systems, Inc.

axlexp2	1.5	Exponent for second order length dependence of AX.
alpl1	0.0	Length dependence of CLM pre-factor ALP.
alplexp	1.0	Exponent for length dependence of ALP.
alpl2	0.0	Second order length dependence of ALP.
alplexp2	2.0	Exponent for second order length dependence of ALP.
alpw	0.0	Width dependence of ALP.
alp1l1	0.0 V	Length dependence of CLM enhancement factor above threshold ALP1.
alp1lexp	0.5	Exponent for length dependence of ALP1.
alp1l2	0.0	Second order length dependence of ALP1.
alp1lexp2	1.5	Exponent for second order length dependence of ALP1.
alp1w	0.0	Width dependence of ALP1.
alpbo	0.0	Back bias dependence of channel length modulation.
vpo	0.05 V	CLM logarithm dependence factor.
vpgo	0.0	Transverse electric field dependence of CLM logarithm factor.
gcoo	0.0	Gate tunneling energy adjustment in inversion.
iginvlw	0.0 A	Gate to channel current pre-factor for a channel area of WEN.LEN.

© 2023 Cadence Design Systems, Inc.

igovinvw	0.0 A	Gate to overlap current pre-factor for a width of WEN in inversion.
igovinvdw	0.0 A	Gate to overlap current pre-factor for a width of WEN in inversion at drain side.
igovaccw	0.0 A	Gate to overlap current pre-factor for a width of WEN in accumulation.
igovaccdw	0.0 A	Gate to overlap current pre-factor for a width of WEN in accumulation at drain side.
stigo	0.0	Temperature dependence of all gate currents.
gc2cho	0.375	Gate to channel current slope factor.
gc3cho	0.063	Gate to channel current curvature factor.
gc2ovinvo	0.375	Gate current slope factor for overlap regions in inversion mode.
gc3ovinvo	0.063	Gate current curvature factor for overlap regions in inversion mode.
gc2ovacco	0.375	Gate current slope factor for overlap regions in accumulation mode.
gc3ovacco	0.063	Gate current curvature factor for overlap regions in accumulation mode.
gcdovl	0.0 V^-1	High drain voltage dependence of overlap gate current.
gcvdovo	1.0 V	Threshold of high drain voltage effect on overlap gate current.
chibo	3.1 V	Tunneling barrier height.

© 2023 Cadence Design Systems, Inc.

niginvo	0.0	Gate tunneling slope adjustment in subthreshold regime.
fnovinvw	0.0 A	Extra gate to overlap current pre-factor for a width of WEN in inversion.
fnovinvdw	0.0 A	Extra gate to overlap current pre-factor for a width of WEN in inversion at drain side.
gcovinvfno	0.2	Extra gate current slope factor for overlap regions in inversion mode.
stigfno	0.0	Temperature dependence of extra gate to overlap current.
agidlo	0.0 A/V^3	GIDL geometry independent pre-factor.
agidldo	0.0 A/V^3	GIDL geometry independent pre-factor at drain side.
agidlw	0.0 A/V^3	GIDL pre-factor for a width of WEN.
agidldw	0.0 A/V^3	GIDL pre-factor for a width of WEN at drain side.
bgidlo	41.0 V	GIDL probability factor at TR.
bgidldo	41.0 V	GIDL probability factor at TR at drain side.
stbgidlo	0.0 V/K	Temperature dependence of BGIDL.
stbgidldo	0.0 V/K	Temperature dependence of BGIDL at drain side.
cgidlo	0.0 V^-1	Substrate bias dependence of GIDL.
cgidldo	0.0 V^-1	Substrate bias dependence of GIDL at drain side.
dgidlo	0.0 V^-1	High field geometry independent parameter of GIDL.

© 2023 Cadence Design Systems, Inc.

dgidldo	0.0 V^-1	High field geometry independent parameter of GIDL at drain side.
dgidll	0.0 V^-1	High longitudinal field parameter of GIDL.
dgidldl	0.0 V^-1	High longitudinal field parameter of GIDL at drain side.
a1o	1.0	Geometry independent impact ionization pre-factor.
a1l	0.0	Length dependence of A1.
a1w	0.0	Width dependence of A1.
a2o	10.0	Impact ionization exponent at TR.
sta2o	0.0	Temperature dependence of A2.
a3o	1.0	Geometry independent saturation-voltage dependence of II.
a3l	0.0	Length dependence of A3.
a3w	0.0	Width dependence of A3.
cgbovo	0.0 F	Geometry independent gate-substrate overlap capacitance part.
cgbovl	0.0 F	Length dependent gate-substrate overlap capacitance part for a length of LEN.
nsdaco	1.0e22 cm^{-3}	Source/Drain effective doping level for AC model.
fifw	0.0	Inner fringe capacitance prefactor for a width of WEN.
fsceaco	0.0	Short channel effect adjustment factor for charge model.

© 2023 Cadence Design Systems, Inc.

lovo	0.0 m	Overlap length for gate/source-drain hdd overlap capacitance.
lovdo	0.0 m	Overlap length for gate/drain hdd overlap capacitance.
covdlo	0.0	Overlap capacitance modulation coefficient due to Leff variation.
covdlw	0.0	Width dependence of COVDL.
covdlbo	0.0	Overlap capacitance modulation with back bias.
dvfbovo	0.0 V	Overlap capacitance flat-band voltage adjustment.
cfro	0.0 F	Corner related outer fringe capacitance.
cfrdo	0.0 F	Corner related outer fringe capacitance at drain side.
cfrw	0.0 F	Outer fringe capacitance per side for a width of WEN.
cfrdw	0.0 F	Outer fringe capacitance per side for a width of WEN at drain side.
csdo	1.0	Drain-source capacitance correction factor.
csdbpo	0.0 F/m	Drain/source to substrate perimeter capacitance.
rtho	1.0e05 K/W	Geometry independent thermal resistance.
rthl	1.5	Length dependence of RTH.
rthw	3.0	Width dependence of RTH.
rthlw	4.5	Area dependence of RTH.

© 2023 Cadence Design Systems, Inc.

strtho	0.0	Temperature dependence of RTH.
ctho	1.0e-12 J/K	Geometry independent thermal capacitance.
lambtho	1.0e-07 m	Characteristic length of lateral thermal coupling for multifinger devices.
ftho	0.0	First neighbour thermal coupling factor for multifinger devices.
fnto	1.0	Thermal noise coefficient.
fntexcl	0.0	Length dependence coefficient of excess noise.
fntexclexp	2.0	Length dependence exponent of excess noise.
nfalw	8.0e22 V^{-1}/m^4	First coefficient of flicker noise.
nfaw	0.0 V^{-1}/m^4	Long channel first coefficient of flicker noise.
nfblw	3.0e07 V^{-1}/m^2	Second coefficient of flicker noise.
nfclw	0.0 V^{-1}	Third coefficient of flicker noise.
nfeo	0.0	Flicker noise front transverse field effect coefficient.
nfebo	0.0	Flicker noise back transverse field effect coefficient.
efo	1.0	Frequency coefficient of flicker noise.
swstress	1	Stress model selection flag: 0=disable, 1=classical STI stress model, 2=strained channel stress model.
saref	1.0e-06 m	Reference distance between OD-edge and poly from one side.

© 2023 Cadence Design Systems, Inc.

sbref	1.0e-06 m	Reference distance between OD-edge and poly from other side.
wlod	0.0 m	Width parameter.
kuo	0.0 m	Mobility degradation/enhancement coefficient.
kvsat	0.0	Saturation velocity degradation/enhancement coefficient.
tkuo	0.0	Temperature dependence of KUO.
lkuo	0.0 m^LLODKUO	Length dependence of KUO.
wkuo	0.0 m^WLODKUO	Width dependence of KUO.
pkuo	0.0 m^(LLODKUO+WLODKUO)	Cross-term dependence of KUO.
llodkuo	0.0	Length parameter for UO stress effect.
wlodkuo	0.0	Width parameter for UO stress effect.
kvtho	0.0 Vm	Threshold shift parameter.
lkvtho	0.0 m^LLODVTH	Length dependence of KVTHO.
wkvtho	0.0 m^WLODVTH	Width dependence of KVTHO.

© 2023 Cadence Design Systems, Inc.

pkvtho	0.0 m^(LLODVTH+WLODVTH)	Cross-term dependence of KVTHO.
llodvth	0.0	Length parameter for VTH-stress effect.
wlodvth	0.0	Width parameter for VTH-stress effect.
stetao	0.0 m	Eta0 shift factor related to VTHO change.
lodetao	1.0	Eta0 shift modification factor for stress effect.
strlambda	1.0e-07 m	Relaxation characteristic length.
stralpha	3.0	Asymmetry parameter.
strdvfbo	0.0 V	Threshold shift parameter.
strwdvfbo	0.0	Width dependence of threshold shift parameter.
strdcfl	0.0	DIBL variation parameter.
strruo	0.0	Mobility degradation/enhancement coefficient.
strtruo	0.0	Temperature dependence of mobility degradation/ enhancement coefficient.
strrvsat	0.0	Saturation velocity degradation/enhancement coefficient.
swpdep	0	Flag for poly-depletion model (without=0, with=1).
np	1.0e21 cm^{-3}	Gate poly-silicon doping.
npo	1.0e21 cm^{-3}	Geometry-independent gate poly-silicon doping.

© 2023 Cadence Design Systems, Inc.

npl	0.0	Length dependence of gate poly-silicon doping.
kdrifto	1.0	Geometry-independent drift component parameter of NQS effect.
kdriftl	0.0	Length dependence of KDRIFT.
kdiffo	1.0	Geometry-independent diffusion component parameter of NQS effect.
kdiffl	0.0	Length dependence of KDIFF.
fracinvo	1.0	Geometry-independent fraction of inversion charge for the second pole of the NQS transition.
kfracinvo	1.0e-15	Geometry-independent second pole frequency coefficient of the NQS transition.
l	(30*1.0e-9)	Designed Gate Length.
nf	1	Number of fins per finger.
lmin	0.0 m	Minimum channel length for which the model is valid.
lmax	1.0 m	Maximum channel length for which the model is valid.
wmin	0.0 m	Minimum channel width for which the model is valid.
wmax	1.0 m	Maximum channel width for which the model is valid.
swcryo		Flag for poly-depletion model (without=0, with=1).
tmin		Minimum temperature.
atmin		Minimum temperature slope.

© 2023 Cadence Design Systems, Inc.

`btmin`	Minimum temperature smoothing parameter.

Output Parameters

`meff`	Effective multiplicity factor (m-factor).
`iavl`	Substrate current due to weak avelanche.

Parameter Index

In the following index, `I` refers to instance parameters, `M` refers to the model parameters section, `O` refers to the output parameters section, and `OP` refers to the operating point parameters section. The number indicates where to look in the appropriate section to find the description for that parameter. For example, a reference of `M-35` means the 35th model parameter.

a1 M-112	cslexp M-209	lovdo M-319	strso M-237
a1l M-306	cslw M-211	lovo M-318	strth M-131
a1o M-305	cso M-207	lp1 M-195	strtho M-334
a1w M-307	css OP-35	lp1w M-196	strtruo M-374
a2 M-113	csthr M-55	lp2 M-198	strwdvfbo M-371
a2o M-308	csthrb M-56	lvarl M-142	stthecs M-54
a3 M-115	csthrbo M-221	lvaro M-141	stthecso M-219
a3l M-311	csthro M-220	lvarw M-143	stthemu M-60
a3o M-310	csw M-210	m I-11	stthemuo M-225
a3w M-312	ct M-26	meff O-1	stthesat M-72

© 2023 Cadence Design Systems, Inc.

adrain I-4
agidl M-102
agidld M-103
agidldo M-292
agidldw M-294
agidlo M-291
agidlw M-293
alp M-76
alp1 M-77
alp1l1 M-262
alp1l2 M-264
alp1lexp M-263
alp1lexp2 M-265
alp1w M-266
alpb M-78
alpbo M-267
alpl1 M-257
alpl2 M-259
alplexp M-258
alplexp2 M-260
alpw M-261
cth M-132
ctho M-335
cto M-157
delvto I-12
dgidl M-110
dgidld M-111
dgidldl M-304
dgidldo M-302
dgidll M-303
dgidlo M-301
dlq M-149
dtemp I-15
dtsh OP-40
dvfbov M-125
dvfbovo M-323
dwq M-150
ef M-140
efo M-347
factuo I-13
fbet1 M-193
fbet1w M-194
mue M-57
mueo M-222
nch M-24
ncho M-155
nf I-10
nf M-381
nfa M-135
nfalw M-341
nfaw M-342
nfb M-136
nfblw M-343
nfc M-137
nfclw M-344
nfe M-138
nfeb M-139
nfebo M-346
nfeo M-345
niginv M-97
niginvo M-286
nov M-28
novd M-29
stthesatl M-247
stthesatlw M-249
stthesato M-246
stthesatw M-248
stvfb M-32
stvfbl M-171
stvfblw M-173
stvfbo M-170
stvfbw M-172
stxcor M-63
stxcoro M-232
swgidl M-5
swigate M-4
swign M-7
swimpact M-9
swjunasym M-8
swpdep M-376
swscale M-1
swshe M-6
swstress M-348
swsubdep M-3

© 2023 Cadence Design Systems, Inc.

areaq M-116
asource I-3
ax M-75
axl M-253
axl2 M-255
axlexp M-254
axlexp2 M-256
axo M-252
beff OP-43
betn M-46
betnb M-47
betnbo M-202
betw1 M-199
betw2 M-200
bgidl M-104
bgidld M-105
bgidldo M-296
bgidlo M-295
cbb OP-31
cbd OP-34
cbg OP-32
fbet2 M-197
feta M-64
fetao M-233
fif M-119
fifw M-316
fnovinv M-98
fnovinvd M-99
fnovinvdw M-288
fnovinvw M-287
fnt M-133
fntexc M-134
fntexcl M-339
fntexclexp M-340
fnto M-338
fsceac M-120
fsceaco M-317
ft OP-44
ftho M-337
gc2ch M-88
gc2cho M-277
gc2ovacc M-92
novdo M-160
novo M-159
np M-377
npl M-379
npo M-378
nsdac M-118
nsdaco M-315
nsddc M-37
nsddco M-180
nsub M-25
nsubo M-156
pdrain I-6
pkuo M-357
pkvtho M-363
pnce M-39
pncew M-182
psce M-35
psceb M-36
pscebo M-179
pscedlb M-38
pscedlbo M-181
tbox M-23
tboxo M-154
thecs M-53
thecso M-218
themu M-59
themuo M-224
thersg M-69
thersgo M-239
thesat M-71
thesatb M-74
thesatbo M-251
thesatg M-73
thesatgo M-250
thesatl M-242
thesatlexp M-243
thesatlw M-245
thesato M-241
thesatw M-244
tk OP-39
tkuo M-354
tmax M-14

© 2023 Cadence Design Systems, Inc.

cbs OP-33
cdb OP-30
cdd OP-27
cdg OP-28
cds OP-29
cf M-40
cfb M-41
cfbo M-186
cfd M-43
cfdl M-44
cfdlb M-45
cfdlbo M-191
cfdll M-189
cfdlw M-190
cfdo M-188
cfl M-183
cflexp M-184
cfr M-126
cfrd M-127
cfrdo M-325
cfrdw M-327
gc2ovacco M-281
gc2ovinv M-90
gc2ovinvo M-279
gc3ch M-89
gc3cho M-278
gc3ovacc M-93
gc3ovacco M-282
gc3ovinv M-91
gc3ovinvo M-280
gcdov M-94
gcdovl M-283
gco M-81
gcoo M-270
gcovinvfn M-100
gcovinvfno M-289
gcvdov M-95
gcvdovo M-284
gds OP-22
gm OP-20
gmb OP-21
gmoverid OP-46
pscel M-176
pscelexp M-177
pscew M-178
psource I-5
pwr OP-48
qmc M-10
region OP-49
rgate OP-45
rout OP-42
rs M-65
rsb M-70
rsbo M-240
rsg M-68
rsgo M-238
rsig M-66
rsigo M-236
rsw1 M-234
rsw2 M-235
rth M-130
rthl M-331
rthlw M-333
toxe M-20
toxeo M-151
toxp M-27
toxpo M-158
tr M-12
tref M-13
trise I-14
tsi M-21
tsio M-152
type M-11
type OP-1
uo M-192
vds OP-2
vdsat OP-7
vdsat_marg OP-8
vearly OP-47
version M-2
vfb M-30
vfbb M-31
vfbbo M-168
vfbl M-162

© 2023 Cadence Design Systems, Inc.

cfro M-324
cfrw M-326
cfw M-185
cgb OP-26
cgbov M-117
cgbovl M-314
cgbovo M-313
cgd OP-24
cgg OP-23
cgidl M-108
cgidld M-109
cgidldo M-300
cgidlo M-299
cgs OP-25
chib M-96
chibo M-285
cic M-34
cicf M-33
cicfo M-174
cico M-175
cov M-121
ib OP-12
id OP-9
idb OP-18
ids OP-13
ig OP-10
igd OP-17
igidl OP-14
iginv M-82
iginvlw M-271
igisl OP-15
igovacc M-85
igovaccd M-86
igovaccdw M-275
igovaccw M-274
igovinv M-83
igovinvd M-84
igovinvdw M-273
igovinvw M-272
igs OP-16
is OP-11
isb OP-19
rtho M-330
rthw M-332
sa I-7
saref M-349
sb I-8
sbref M-350
sd I-9
self_gain OP-41
sta2 M-114
sta2o M-309
stbet M-48
stbetl M-204
stbetlw M-206
stbeto M-203
stbetw M-205
stbgidl M-106
stbgidld M-107
stbgidldo M-298
stbgidlo M-297
stcf M-42
stcfl M-187
vfbl2 M-164
vfblbo M-169
vfblexp M-163
vfblexp2 M-165
vfblw M-167
vfbo M-161
vfbw M-166
vgs OP-4
vp M-79
vpg M-80
vpgo M-269
vpo M-268
vsb OP-3
vth OP-5
vth_drive OP-6
vthmod M-15
w I-2
wbet M-201
wkuo M-356
wkvtho M-362
wlod M-351

© 2023 Cadence Design Systems, Inc.

covd M-122
covdl M-123
covdlb M-124
covdlbo M-322
covdlo M-320
covdlw M-321
cs M-49
csb OP-37
csbi M-51
csbio M-213
csd M-128
csd OP-38
csdbp M-129
csdbpo M-329
csdo M-328
csfi M-50
csfio M-212
csg OP-36
csl M-208
isnoisy I-16
ivth M-16
ivth_vdsmin M-19
ivthl M-18
ivthw M-17
kuo M-352
kvsat M-353
kvtho M-360
l I-1
l M-380
lambtho M-336
lap M-144
lkuo M-355
lkvtho M-361
llodkuo M-358
llodvth M-364
lmax M-383
lmin M-382
lodetao M-367
stcs M-52
stcsl M-215
stcslw M-217
stcso M-214
stcsw M-216
stetao M-366
stig M-87
stigfn M-101
stigfno M-290
stigo M-276
stmue M-58
stmueo M-223
stralpha M-369
strdcfl M-372
strdvfbo M-370
strlambda M-368
strruo M-373
strrvsat M-375
strs M-67
wlodkuo M-359
wlodvth M-365
wmax M-385
wmin M-384
wot M-148
wvarl M-146
wvaro M-145
wvarw M-147
xcor M-61
xcorb M-62
xcorbo M-231
xcorl M-227
xcorlexp M-228
xcorlw M-230
xcoro M-226
xcorw M-229
xge M-22
xgeo M-153

© 2023 Cadence Design Systems, Inc.