

Spectre® Classic Simulator, Spectre APS, Spectre X, Spectre XPS, Spectre FMC Analysis, and Legato Reliability Solution User Guide

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Preface

The Spectre® simulation platform contains a set of simulation technologies for circuit design and verification. It supports multiple netlist formats, all standard device models, a large variety of large and small signal analyses, design checking features, a large set of output formats, and advanced analyses like EMIR, RF, and device reliability.

Different simulation engines are integrated into the platform – Spectre SPICE engine, Spectre Accelerated Parallel Simulator (APS) for high-precision SPICE and scalable multi-core simulation performance, Spectre X Simulator for high-performance, high-capacity simulation to handle the largest pre- and post-layout designs with analog accuracy, which also includes extensive distribution capabilities designed to maximize a cloud or server farm use model, Spectre Extensive Partitioning Simulator (Spectre XPS), an advanced FastSPICE engine, which provides high performance simulation for SRAM, DRAM, and flash designs, and the Spectre FX simulator, the next-generation FastSPICE simulator from Cadence. With Spectre AMS Designer, you can mix any of the above analog solvers with the Cadence® Xcelium™ Parallel Logic Simulator.

Besides the comprehensive set of basic analyses, the Spectre circuit simulator and Spectre X provide the RF simulation capabilities to verify RF and communication circuits, such as mixers, oscillators, sample holds and switched-capacitor filters.

Additional information on the Spectre RF simulation option is covered in the *Spectre Circuit Simulator and Accelerated Parallel Simulator RF Analysis User Guide*.

This user guide assumes that you are familiar with:

- The development, design, and simulation of integrated circuits.
- SPICE simulation.
- Virtuoso® Analog Design Environment (ADE).

Licensing

Cadence offers both ala carte pricing plus a unique multi-mode simulation (MMSIM) license that can enable the Spectre simulation platform. Spectre circuit simulator, Spectre APS, Spectre® XPS, Spectre® X, and Spectre® FX are the base products. The features provided in these base products are listed in [Table A-1](#) on page 28, [Table A-2](#) on page 28, and [Table A-3](#) on page 29. In addition, the options available across each of these base products are listed in [Table A-4](#) on page 29. Both the base products and the options are accessible using Spectre MMSIM tokens.

For details on Spectre FX license requirements, see [*Spectre FX Circuit Simulator User Guide*](#).

For additional details on licensing, pricing and packaging contact your account manager.

Table A-1 Spectre® Circuit Simulator

Spectre Circuit Simulator Features
DC, small-signal analyses and transient
Monte Carlo, DC mismatch, Parametric sweep
Transient noise analysis
Reliability analysis
Encryption
AHDL Linter
Built-in Measurement Description Language (MDL)
MMSIM Toolbox for MATLAB® from The MathWorks
Cadence Proprietary Agemos Model
Cosimulation with Simulink® from The MathWorks
Broadband SPICE (BBSpice)

Table A-2 Spectre® Accelerated Parallel Simulator (Spectre APS)

Spectre APS Single-Core Features
All analyses and features in Spectre Circuit Simulator

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Spectre APS Single-Core Features
Parasitic Reduction
Parasitic Stitching
Postlayout Simulation
Static and Dynamic Circuit Checks

Table A-3 Spectre eXtensive Partitioning Simulator (Spectre XPS)

Dynamic and Power Simulation
Static and Dynamic Circuit Checks
Variation Analysis
Postlayout Simulation
AHDL Linter

Table A-4 Spectre Options for Spectre, Spectre APS, Spectre XPS, Spectre X, and Spectre FX

Spectre Option	Description
Spectre(R) RF option	Enables RF analysis with Spectre, Spectre APS, and Spectre X simulator
Spectre CPU Accelerator option	Enables multi-core simulation up to 64 cores with Spectre APS and Spectre XPS base products on a single machine or across a cluster of machines (distributed processing). In addition, it enables EMIR analysis with Spectre APS base product and Spectre Power option. To run multi-threading on 4 cores, you need 1 Spectre CPU Accelerator option. 2 Spectre CPU Accelerator options are required to perform multi-threading computation on 16 cores.

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Spectre Option	Description
Spectre X Multi-Core Option	Enables multi-core simulation up to 512 cores with Spectre X base product on a single machine or across a cluster of machines (distributed processing). To run multi-threading on 4 CPUs, you need 1 Spectre X Multi-Core Option. 2 Spectre X Multi-Core Options are required to perform multi-threading computation on 16 CPUs. 3 Spectre X Multi-Core Options are required to perform multi-threading computation on 64 CPUs and 4 Spectre X Multi-Core Options are required to perform multi-threading computation on 128 CPUs.
Spectre Power option	Enables EMIR analysis with Spectre X base product. It also enables EMIR analysis with Spectre APS base product and the Spectre CPU Accelerator option. This option is not available with Spectre base product.
Spectre Characterization Simulator option	Provides you access to the Spectre simulators for characterization simulation jobs only. It is only available as an option to Liberate characterization family of products. Please contact your account representative for further details.

Note: For details on the capabilities and features offered with the Spectre RF analysis option, refer to the *Spectre Circuit Simulator and Accelerated Parallel Simulator RF Analysis* User Guide.

License Requirement for Spectre FMC

The Spectre FMC Option license enables Spectre FMC Analysis. You can also use MMSIM tokens. Contact Cadence Customer Support for more details.

Legato Reliability Solution License

The Legato reliability solution license, which is a pack of 6 tokens (that are not the same as MMSIM tokens), is required to run the following reliability features. Contact Cadence Customer Support for more details.

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Table A-5 Legato Reliability Tokens

Feature	Number of tokens Required	Functionality
Analog Fault Simulation	3	Spectre transient fault analysis and Spectre direct fault analysis
Fault Generation	0	info what=bridges opens dhe Does not check out the license; however, checks for the availability of the license.
spectre_ddmrpt	0	spectre_ddmrpt Does not check out the license; however, checks for the availability of the license.
spectre_fsrpt	0	spectre_fsrpt Does not check out the license; however, checks for the availability of the license.
Electrothermal Simulation	2	Spectre electrothermal simulation Note: Electrothermal simulation requires a Celsius_Thermal license during Spectre thermal extraction, and 2 legato tokens during the remaining electrothermal simulation. The Celsius_Thermal license is released after thermal extraction is completed and then the 2 legato tokens are checked out.
RelXpert	4	RelXpert simulation Note: Product 33580: Spectre® RelXpert Reliability license is still available in SPECTRE 20.1.
Spectre self-heating	1	Spectre self-heating analysis
Spectre self-heating + Aging analysis	1	Spectre self-heating and Aging analysis
Monte Carlo + Aging analysis	1	Monte Carlo and Aging analysis

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Feature	Number of tokens Required	Functionality
RF reliability analysis	1	Spectre RF reliability analysis, such as <code>pss</code> , <code>pnoise</code> , <code>hb</code> , <code>hbnoise</code> , <code>sp</code> , <code>pac</code> , and <code>pxf</code> .
Spectre reliability with XPS S mode	1	Spectre reliability analysis with XPS SPICE mode
STB reliability analysis	1	Spectre STB reliability analysis

Note: The Legato reliability solution can also be run with MMSIM tokens.

License Checkout Order

The order in which the license features are checked out is determined either by a default checkout order or by a customized order that can be defined using the `+lorder` option. Spectre, Spectre APS, Spectre XPS, and Spectre X check for a license in the order specified using the `+lorder licenseList` option. Note that mixing of ala carte license and Spectre MMSIM tokens is not allowed.

To make it easier to specify license names with the `+lorder` option, a representative mnemonic license has been provided, as shown in [Table A-6](#) on page 32.

Table A-6 Mnemonic License Names and Corresponding License Feature

MMSIM	Virtuoso_Multi_mode_Simulation, Virtuoso_APS_MMSIM_Lk, Virtuoso_XPS_MMSIM_Lk Spectre_X_MMSIM_Lk
PRODUCT	Virtuoso_Spectre, Virtuoso_Acceler_Parallel_sc, Spectre_XPS, spectre_X_sc

You can specify the following for `licenseList`:

`+lorder PRODUCT` - Spectre attempts to check out the product and options combination licenses only. If the licenses are not available, Spectre generates an error.

`+lorder MMSIM` - Spectre attempts to check out the Virtuoso_Multi_mode_Simulation (Spectre MMSIM) tokens only.

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`+lorder PRODUCT:MMSIM` - Spectre attempts to check out product licenses first. If product licenses are not available, Spectre attempts to check out Spectre MMSIM tokens.

`+lorder MMSIM:PRODUCT` - Spectre attempts to check out Spectre MMSIM tokens first. If the tokens are not available Spectre attempts to check out product licenses.

The default license checkout order for features in Spectre, Spectre APS, Spectre XPS, and Spectre X base products is `PRODUCT:MMSIM`.

Using License Queuing

You can turn on license queuing by using the `lqtimeout` command line option:

```
spectre +lqtimeout time_in_seconds
```

If a license is not available when you begin a simulation job, the Spectre circuit simulator waits in queue for a license for the specified time. If you specify the value 0 for this option, the Spectre circuit simulator waits indefinitely for a license. The `lqtimeout` option has no default value for the standalone Spectre circuit simulator. If you invoke Spectre through the Analog Design Environment, the default value for `lqtimeout` is 900 seconds. You can use the `lqsleep` option to specify the interval (in seconds) at which the Spectre circuit simulator should check for license availability. The default value for `lqsleep` is 30 seconds.

```
spectre +lqsleep interval
```

For more information on any of the above options, see `spectre -h`.

Suspending and Resuming Licenses

You can direct Spectre to release licenses when suspending a simulation job. This feature is aimed for users of simulation farms, where the licenses in use by a group of lower priority jobs may be needed for a group of higher priority jobs.

To enable this feature, simply start Spectre with the `+lsuspend` command line option. Press `ctrl+z` to suspend the simulation run and release the licenses. All licenses are checked in. To resume simulation, press `fg`. These keystrokes may not work if you have changed the default key bindings. You can also use the `kill` command to suspend and resume the simulation. You can suspend a simulation with `kill -s TSTP <pid>`. To resume the simulation, type `kill -s CONT <pid>`.

Note: When distributing simulation jobs with a Distributed Resource Management System (DRMS), suspend the simulation and release licenses by sending the `TSTP` signal. Resume jobs by sending the `CONT` signal."

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For information on tracking token licensing, see the *Virtuoso® Software Licensing and Configuration Guide*.

In Virtuoso® ADE Product Suite, the `lqtimeout` and `lqsleep` options are controlled by the following options:

```
spectre.envOpts lsuspend boolean t
spectre.envOpts licQueueTimeOut string "900"
spectre.envOpts licQueueSleep string "30"
```

Related Documents for Spectre

This user guide contains information about the functionality. The following documents provide more information about Spectre RF and related products.

- The Spectre circuit simulator is often run within the analog circuit design environment, under the Cadence design framework II. To see how the Spectre circuit simulator is run under the analog circuit design environment, read the *Virtuoso ADE Explorer User Guide* and *Virtuoso ADE Assembler User Guide*.
- To learn more about specific parameters of components and analyses, consult the Spectre online help (`spectre -h`).
- To learn more about the equations used in the Spectre circuit simulator, consult the *Spectre Circuit Simulator Components and Device Models Reference* manual.
- To learn about the next-generation FastSPICE simulator, Spectre FX, see *Spectre FX Circuit Simulator User Guide*.
- The Spectre circuit simulator also includes a waveform display tool, Virtuoso Visualization and Analysis tool, to use to display simulation results. For more information about the tool, see the *Virtuoso Visualization and Analysis XL User Guide*.
- For more information about using the Spectre circuit simulator with Verilog-A, see the *Cadence Verilog-A Language Reference* manual.
- For more information about RF theory, see *Spectre Circuit Simulator RF Analysis Theory*.
- For more information about how you work with the design framework II interface, see *Cadence Design Framework II Help*.
- For more information about specific applications of Spectre analyses, see *The Designer's Guide to SPICE & Spectre*¹.

1. Kundert, Kenneth S. *The Designer's Guide to SPICE & Spectre*. Boston: Kluwer Academic Publishers, 1995.

Third Party Tools

To view any `.swf` multimedia files, you need:

- Flash-enabled web browser, for example, Internet Explorer 5.0 or later, Netscape 6.0 or later, or Mozilla Firefox 1.6 or later. Alternatively, you can download Flash Player (version 6.0 or later) directly from the [Adobe](#) website.
- Speakers and a sound card installed on your computer for videos with audio.

Typographic and Syntax Conventions

This list describes the syntax conventions used for the Spectre circuit simulator.

<code>literal</code>	Nonitalic words indicate keywords that you must enter literally. These keywords represent command (function, routine) or option names, filenames and paths, and any other sort of type-in commands.
<i>argument</i>	Words in italics indicate user-defined arguments for which you must substitute a name or a value. (The characters before the underscore (<code>_</code>) in the word indicate the data types that this argument can take. Names are case sensitive.
	Vertical bars (OR-bars) separate possible choices for a single argument. They take precedence over any other character.
[]	Brackets denote optional arguments. When used with OR-bars, they enclose a list of choices. You can choose one argument from the list.
{ }	Braces are used with OR-bars and enclose a list of choices. You must choose one argument from the list.
...	Three dots (...) indicate that you can repeat the previous argument. If you use them with brackets, you can specify zero or more arguments. If they are used without brackets, you must specify at least one argument, but you can specify more.

Important

The language requires many characters not included in the preceding list. You must enter required characters exactly as shown.

References

Text within brackets ([]) is a reference. See *Appendix A, References* of the *Spectre Circuit Simulator Reference* manual for more detailed information.

Introducing the Spectre Circuit Simulator

The Spectre[®] circuit simulator is a modern circuit simulator that uses direct methods designed to simulate analog and digital circuits at the differential equation level. The basic capabilities of the Spectre circuit simulator are similar in function and application to SPICE; however, the Spectre circuit simulator has not descended from SPICE. The Spectre and SPICE simulators use the same basic algorithms—such as implicit integration methods, Newton-Raphson, and direct matrix solution; however, every algorithm is newly implemented. Spectre algorithms, the best currently available, give you an improved simulator that is faster, more accurate, more reliable, and more flexible than previous SPICE-like simulators.

In addition to the baseline simulation functionalities, Spectre supports multiple simulation technologies in a common simulation platform, allowing you to choose the most effective technology for your application, but retaining the same Spectre simulation infrastructure - netlist format, analysis and options syntax, device models, output formats, and feature functions across all the technology choices. The Spectre simulator technology family includes the Spectre[®] Classic technology, the accelerated parallel simulation (APS) technology, the Spectre[®] X technology, and the extensive partitioning simulation (XPS) technology.

Spectre[®] APS maintains baseline Spectre simulation accuracy, fully supports all Spectre functionalities, and provides highly enhanced significant single- and multi-core simulation performance, with an effective simulation capacity of multi-million transistors and tens of millions of parasitic elements. For more information, see [The Spectre APS Circuit Simulator](#).

Spectre X introduces the next-generation SPICE simulation technology, significantly improves simulation performance and capacity over Spectre APS, and features with a simple high-level preset use model. With an effective simulation capacity of tens of millions of transistors and hundreds of millions of parasitic elements, the ability to exploit modern parallel computer architectures with over a hundred active cores, Spectre X is the technology of choice for the largest and most challenging contemporary simulation problems. For more information, see [The Spectre X Circuit Simulator](#).

Spectre[®] XPS, incorporating a completely new circuit partitioning and multi-rate technology, further extends the simulation performance and simulation capacity to effectively enable full-chip simulation at advanced process nodes. See [The Spectre XPS Circuit Simulator](#) for details on Spectre XPS.

This chapter discusses the following:

- Spectre Usability Features and Customer Service
- Variation Analysis
- Analog HDL
- AHDL Linter
- RF Capabilities

Spectre Usability Features and Customer Service

The following features and services help you use the Spectre circuit simulator easily and efficiently:

- You can run the Spectre circuit simulator standalone or run it under the Virtuoso® analog design environment. To see how the Spectre circuit simulator is run under the analog circuit design environment, read the *Virtuoso Analog Design Environment User Guide*. You can also run the Spectre circuit simulator in the Composer-to-Spectre direct simulation environment. The environment provides a graphical user interface for running the simulation.
- The Spectre circuit simulator gives you an online help system. With this system, you can find information about any parameter associated with any Spectre component or analysis. You can also find articles on other topics that are important to using the Spectre circuit simulator effectively.
- You can type `spectre -h` at the UNIX command line to get detailed information about a feature, analysis, model, and option.
- Spectre diagnosis mode, available as an `options` statement parameter, gives you information to help diagnose convergence problems.

Variation Analysis

In order to provide practical design robustness assessment to circuit designers, Spectre, Spectre APS, and Spectre XPS support a simple variation analysis capability. It enables you to impose different levels of variation on device performance characteristics, instead of being dependent on the foundry statistical model, thereby enabling circuit designers to explore circuit design robustness under different conditions. This capability is not meant to replace the traditional statistical analysis approach for yield estimation or optimization, but rather providing a tool for circuit designers to expose design sensitivity. With this new capability, statistical simulation can be performed on a larger scale, for example, full SRAM design.

The variation analysis follows the Spectre Monte Carlo use model, but does not require the identification and parameterization of statistical parameters. An example is shown below

```
statistics {  
    mismatch {  
        vary ids primitive=[bsim4] dist=gauss std=2.5 percent=yes  
    }  
}
```

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```
process {  
    vary ids primitive=[bsim4] dist=gauss std=4.5 percent=yes  
}  
  
mc1 montecarlo variations=mismatch seed=4321 numruns=3 method=vade {  
    tran1 tran stop=10n  
}
```

The example imposes a 2.5% Gaussian mismatch variation, plus a 4.5% Gaussian process variation, on all BSIM4 `Ids` currents.

When using the variation analysis, process and mismatch statements are used to define the `ids` variation. Additionally, the primitive, the distribution type, and the standard deviation need to be defined.

The variation analysis is enabled by the `method=vade` option (vade = Variation Aware Design Exploration) in the Monte Carlo statement. Spectre XPS supports all Monte Carlo options and distribution types “uniform”, “Gaussian”, “limit”, and “shift” whereas Spectre and Spectre APS support all Monte Carlo options and “uniform” and “Gaussian” distribution types.

Factor truncate is not supported for gamma distribution

Output of the variation analysis are family plots, measure file, and `montecarlo.mcdat` file. To view warning and errors of individual variation runs please check the `<netlist>_#.log` files.

Supported Features

The following table lists the features that are supported by Spectre, Spectre APS, Spectre MS, and Spectre XPS (SPICE, SRAM, DRAM, and Flash):

Feature Name	Spectre	Spectre APS	Spectre X	Spectre MS	XPS Flash	XPS SPICE	XPS SRAM	XPS DRAM
Transient Analysis	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
DC/AC Analysis	Yes	Yes	DC	No	No	Yes	No	No
RF (Shooting Analysis)	Yes	Yes	No	No	No	No	No	No
Reliability Analysis	Yes	Yes	Yes	Yes	Yes	Yes ¹	Yes	No
Postlayout simulation with DSPF include	Yes	Yes	Yes	Yes	Yes	Yes ²	Yes ³	No
Postlayout simulation with DSPF stitching	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Direct EMIR Analysis ⁴	No	Yes	Yes	No	No	No	No	No
Iterated EMIR Analysis ⁵	No	Yes	Yes	Yes	Yes	Yes	Yes	No
++parasitics	No	Yes	No	No	No	No	No	No
+postlayout	No	Yes	No	Yes/No ⁶	No	No	No	No
+preset	No	No	Yes	Yes/No ⁷	No	No	No	No
+errpreset	Yes	Yes	No	Yes/No ⁸	No	No	No	No
+postlpreset	No	No	Yes	Yes/No ⁹	No	No	No	No
Device Checks (asserts)	Yes	Yes	Yes	Yes	No	Yes	No	No
Circuit Checks (static)	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Circuit Checks (dynamic) ¹⁰	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Info	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
alter	Yes	Yes	No	No	Yes	Yes	Yes	Yes
MonteCarlo	Yes	Yes	Yes	No	No	Yes	Yes	No

1.Only agemos model is supported

2.Supported but not recommended

3.Supported but not recommended

4.Refer to [EMIR Analysis](#)

5.Refer to [EMIR Analysis](#)

6.Yes, if Spectre APS is used; No, if Spectre X is used

7.Yes, if Spectre X is used; No, if Spectre APS is used

8.Yes, Spectre APS is used; No, if Spectre X is used

9.Yes, if Spectre X is used; No, if Spectre APS is used

10.Refer to [Circuit Checks](#)

Analog HDL

The Spectre circuit simulator works with Verilog®-A, an analog high-level description language (AHDL). The Verilog-A language is an open standard and is part of the Spectre Verilog-A option. The Verilog-A language is upward compatible with Verilog-AMS, a powerful and industry-standard mixed-signal language.

The Verilog-A language uses functional description text files (modules) to model the behavior of electrical circuits and other systems. It allows you to create your own models by simply writing down the equations. The AHDL lets you describe models in a simple and natural manner. This is a higher level modeling language than previous modeling languages, and you can use it without being concerned about the complexities of the simulator or the simulator algorithms. In addition, you can combine AHDL components with Spectre built-in primitives.

The Verilog-A language lets designers of analog systems and integrated circuits create and use modules that encapsulate high-level behavioral descriptions of systems and components. The behavior of each module is described mathematically in terms of its terminals and external parameters applied to the module. Designers can use these behavioral descriptions in many disciplines (electrical, mechanical, optical, and so on).

The Verilog-A language borrows many constructs from Verilog and the C programming language. These features are combined with a minimum number of special constructs for behavioral simulation. These high-level constructs make it easier for designers to use a high-level description language for the first time.

For more information on Verilog-A, refer to the *Cadence® Verilog®-A Language Reference* manual.

AHDL Linter

You can use the AHDL Linter feature to analyze the Spectre/Spectre APS testcases containing Verilog-A models. The AHDL Linter feature enables you to detect issues in the Verilog-A models. AHDL Linter checks the design for:

- Design consistency, reusability, and portability
- Semantic correctness

AHDL linter consists of static and dynamic lint checks. Static lint checks are performed before analysis. Dynamic lint checks are performed during analysis for dynamic modeling issues.

AHDL Linter in Spectre/Spectre APS is activated using the following command-line options:

Spectre Baseline

```
%spectre -ahdllint netlist.scs
```

Spectre with APS

```
%spectre +aps -ahdllint netlist.scs
```

For more information on the AHDL Linter feature, refer to [AHDL Linter Checks](#).

RF Capabilities

The Spectre® circuit simulator RF analysis (Spectre RF) analyses add capabilities to the Spectre circuit simulator, such as direct, efficient computation of steady-state solutions and simulation of circuits that translate frequency.

For more information on RF analyses, refer to the *Spectre Circuit Simulator and Accelerated Parallel Simulator RF Analysis in ADE Explorer User Guide*.

Getting Started with the Spectre Circuit Simulator

This chapter discusses the following topics:

- [Using the Example and Displaying Results on page 46](#)
- [Sample Schematic on page 46](#)
- [Sample Netlist on page 48](#)
- [Instructions for a Spectre Simulation Run on page 52](#)
- [Viewing Your Output on page 54](#)

Using the Example and Displaying Results

In this chapter, you examine a schematic and its Spectre® circuit simulator netlist to get an overview of Spectre syntax. You also follow a sample circuit simulation. The best way to use this chapter depends on your past experience with simulators.

Carefully examine the schematic (see [Sample Schematic](#)) and netlist (see [Sample Netlist](#)) and compare Spectre netlist syntax with that of SPICE-like simulators you have used. If you have prepared netlists for SPICE-like simulators before, you can skim [Elements of a Spectre Netlist](#). With this method, you can learn a fair amount about the Spectre simulator in a short time.

Approach this chapter as an overview. You will probably have unanswered questions about some topics when you finish the chapter. Each topic is covered in greater depth in subsequent chapters. Do not worry about learning all the details now.

To give you a complete overview of a Spectre simulation, the example in this chapter includes the display of simulation results with Virtuoso Visualization and Analysis XL, a waveform display tool that is included with the Spectre simulator. If you use another display tool, the procedures you follow to display results are different. This user guide does not teach you how to display waveforms with different tools. If you need more information about how to display Spectre results, consult the documentation for your display tool.

The example used in this chapter is a small circuit, an oscillator; you run a transient analysis on the oscillator and then view the results. The following sections contain the schematic and netlist for the oscillator. If you have used SPICE-like simulators before, looking at the schematic and netlist can help you compare Spectre syntax with those of other simulators. If you are new to simulation, looking at the schematic and netlist can prepare you to understand the later chapters of this book.

You can also get more information about command options, components, analyses, controls, and other selected topics by using the `spectre -h` command to access the Spectre online help.

Sample Schematic

A schematic is a drawing of an electronic circuit, showing the components graphically and how they are connected together. The following schematic has several annotations:

■ Names of components

Each component is labeled with the name that appears in the instance statement for that component. The names for components are in italics (for example, *Q2*).

Names of nodes

Each node in the circuit is labeled with its unique name or number. This name can be either a name you create or a number. Names of nodes are in boldface type (for example, **b1**). Ground is node 0.

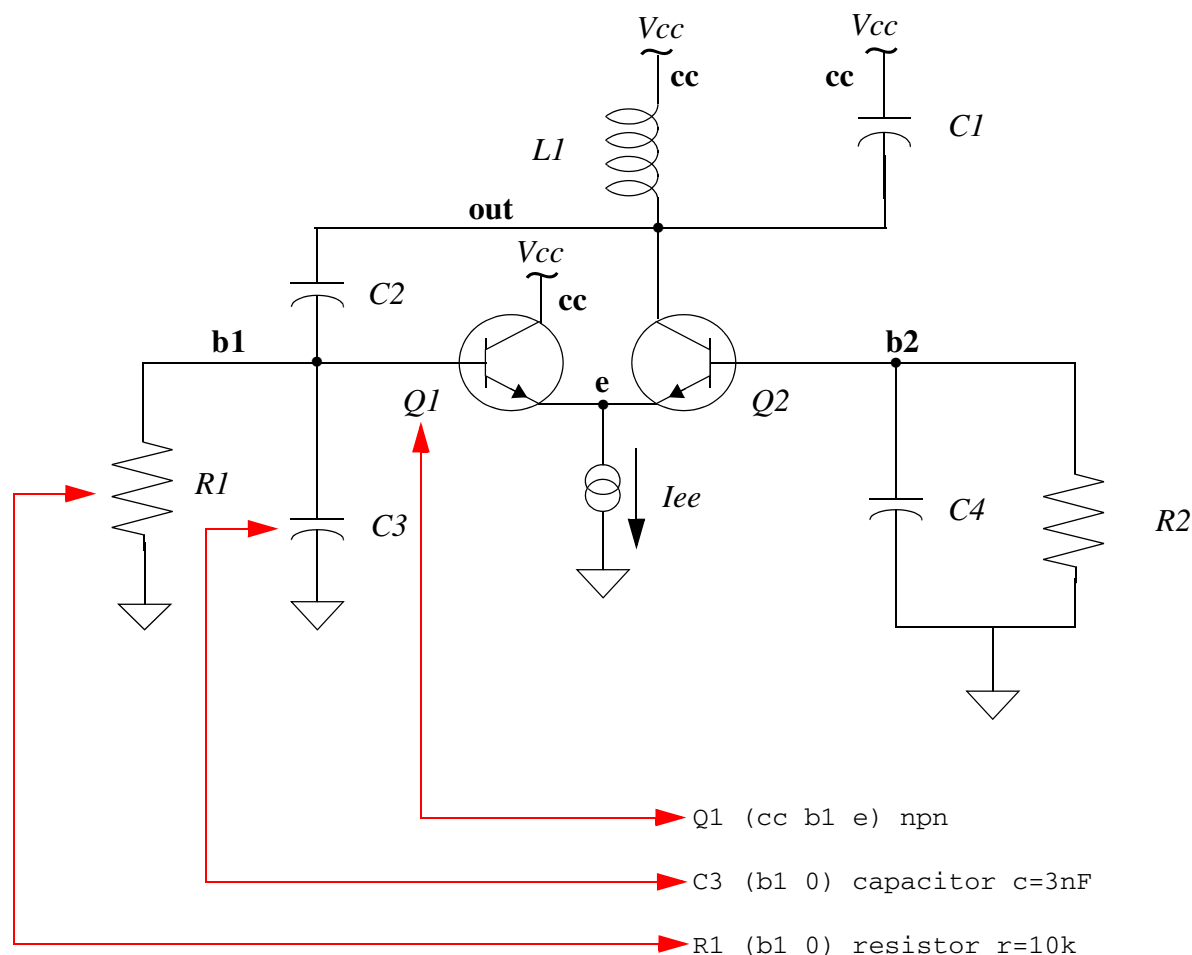
Sample instance statements

The schematic is annotated with instance statements for some of the components. Arrows connect the components in the schematic with their corresponding instance statements.

Bold Type = Names of nodes. All connections to ground have the same node name.

Italic Type = Names of components (also appear in the instance statement for each component).

↔ = Link between components and instance statements.



Sample Netlist

A netlist is an ASCII file that lists the components in a circuit, the nodes that the components are connected to, and parameter values. You create the netlist in a text editor such as `vi` or `emacs` or from one of the environments that support the Spectre simulator. The Spectre simulator uses a netlist to simulate a circuit.

```
// BJT ECP Oscillator
simulator lang=spectre

Iee (e 0)    isource dc=1mA
Vcc (cc 0)   vsource dc=5

Q1 (cc b1 e) npn
Q2 (out b2 e) npn

L1 (cc out) inductor l=1uH

C1 (cc out) capacitor c=1pf
C2 (out b1) capacitor c=272.7pF
C3 (b1 0) capacitor c=3nF
C4 (b2 0) capacitor c=3nF

R1 (b1 0) resistor r=10k
R2 (b2 0) resistor r=10k

ic cc=5

model npn bjt type=npn bf=80 rb=100 vaf=50 \
cjs=2pf tf=0.3ns tr=6ns cje=3pf cjc=2pf

OscResp tran stop=80us maxstep=10ns
```

← Comment (indicated by //)

← Indicates the file contains a Spectre netlist
(see the next section). Place below first line.

Instance statements

← Control statement (sets initial conditions)

Model statement

← Analysis statement

Elements of a Spectre Netlist

This section briefly explains the components, models, analyses, and control statements in a Spectre netlist. All topics discussed here (such as `model` statements or the `simulator lang` command) are presented in greater depth in later chapters. If you want more complete reference information about a topic, consult these discussions.

Title Line

The first line is taken to be the title. It is used verbatim when labeling output. Any statement you place in the first line is ignored as a comment. For more information about comment lines, see [“Basic Syntax Rules”](#) on page 139.

Simulation Language

The second line of the sample netlist indicates that the netlist is in the Spectre Netlist Language, instead of SPICE. For more information about the `simulator lang` command, see [“Spectre Language Modes”](#) on page 139.

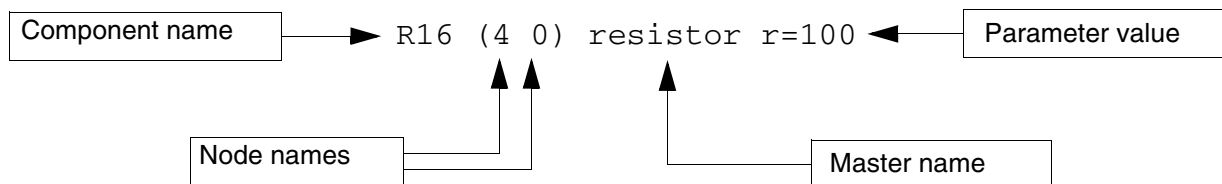
Instance Statements

The next section in the sample netlist consists of instance statements. To specify a single component in a Spectre netlist, you place all the necessary information for the component in a netlist statement. Netlist statements that specify single components are called instance statements. (The instance statement also has other uses that are described in [Chapter 8, “Spectre Netlists”](#).)

To specify single components within a circuit, you must provide the following information:

- A unique component name for the component
- The names of nodes to which the component is connected
- The master name of the component (identifies the type of component)
- The parameter values associated with the component

A typical Spectre instance statement looks like this:



Note: You can use balanced parentheses to distinguish the various parts of the instance statement, although they are optional:

```
R1 (1 2) resistor r=1  
Q1 (c b e s) npn area=10
```

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```
Gm (1 2) (3 4) vccs gm=.01
R7 (x y) rmod (r=1k w=2u)
```

Component Names

Unlike SPICE, the first character of the component name has no special meaning. You can use any character to start the component name. For example:

```
Load (out o) resistor r=50
Balun (in o pout nout) transformer
```

Note: You can find the exact format for any component in the parameter listings for that component in the Spectre online help.

Master Names

The type of a component depends on the name of the master, not on the first letter of the component name (as in SPICE); this feature gives you more flexibility in naming components. The master can be a built-in primitive, a model, a subcircuit, or an AHDL component.

Parameter Values

Real numbers can be specified using scientific notation or common engineering scale factors. For example, you can specify a 1 pF capacitor value either as `c=1pf` or `c=1e-12`. Depending on whether you are using the Spectre Netlist Language or SPICE, you might need to use different scale factors for parameter values. Only ANSI standard scale factors are used in Spectre netlists.

Control Statements

The next section of the sample netlist contains a control statement, which sets initial conditions.

Model Statements

Some components allow you to specify parameters common to many instances using the `model` statement. The only parameters you need to specify in the instance statement are those that are generally unique for a given instance of a component.

You need to provide the following for a `model` statement:

- The keyword `model` at the beginning of the statement

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- A unique name for the model (reference by master names in instance statements)
- The master name of the model (identifies the type of model)
- The parameter values associated with the model

The following example is a `model` statement for a bjt. The model name is `nnpn`, and the component type name is `bjt`. The backslash (`\`) tells you that the statement continues on the next line. The backslash must be the last character in the line because it escapes the carriage return.

```
model nnpn bjt type=npn bf=80 rb=100 vaf=50 \  
      cjs=2pf tf=0.3ns tr=6ns cje=3pf cjc=2pf
```

When you create an instance statement that refers to a `model` statement for its parameter values, you must specify the model name as the master name. For example, an instance statement that receives its parameter values from the previous `model` statement might look like this:

```
Q1 (vcc b1 e vcc) nnpn
```

Check documentation for components to determine which parameters are expected to be provided on the instance statement and which are expected on the model statement.

Analysis Statements

The last section of the sample netlist has the analysis statement. An analysis statement has the same syntax as an instance statement, except that the analysis type name replaces the master name. To specify an analysis, you must include the following information in a netlist statement:

- A unique name for the analysis statement
- Possibly a set of node names
- The name of the type of analysis you want
- Any additional parameter values associated with the analysis

To find the analysis type name and the parameters you can specify for an analysis, consult the parameter listing for that analysis in the Spectre online help (`spectre -h`).

The following analysis statement specifies a transient analysis. The analysis name is `stepResponse`, and the analysis type name is `tran`.

```
stepResponse tran stop=100ns
```

Instructions for a Spectre Simulation Run

When you complete a netlist, you can run the simulation with the `spectre` command.

- To run a simulation for the sample circuit, type the following at the command line:

```
spectre osc.scs
```

Note: `osc.scs` is the file that contains the netlist.

Following Simulation Progress

As the simulation runs, the Spectre simulator sends messages to your screen that show the progress of the simulation and provide statistical information. In the simulation of `osc.scs`, the Spectre simulator prints some warnings and notifications. The Spectre simulator tells you about conditions that might reduce simulation accuracy. When you see a Spectre warning or notification, you must decide whether the information is significant for your particular simulation.

Screen Printout

The printout for the `myuserguide.sp` simulation looks like this:

```
Simulating `myuserguide.sp' on spiceneh8c-2 at 11:24:05 AM, Wed May 11, 2011  
(process id: 19576).
```

```
Environment variable:
```

```
    SPECTRE_DEFAULTS==log %C:r.out -f sst2
```

```
Command line:
```

```
 \  
  /grid/cic/mmsimcm_v1/latest_build/tools.lnx86/spectre/bin/32bit/spectre \  
  myuserguide.sp +l myuserguide.log
```

```
Loading /grid/cic/mmsimcm_v1/latest_build/tools.lnx86/cmi/lib/5.0/  
libinfineon_sh.so ...
```

```
Loading /grid/cic/mmsimcm_v1/latest_build/tools.lnx86/cmi/lib/5.0/  
libphilips_sh.so ...
```

```
Loading /grid/cic/mmsimcm_v1/latest_build/tools.lnx86/cmi/lib/5.0/libsparm_sh.so  
...
```

```
Loading /grid/cic/mmsimcm_v1/latest_build/tools.lnx86/cmi/lib/5.0/  
libstmodels_sh.so ...
```

```
Time for NDB Parsing: CPU = 66.989 ms, elapsed = 206.596 ms.
```

```
Time accumulated: CPU = 66.989 ms, elapsed = 206.596 ms.
```

```
Peak resident memory used = 23.7 Mbytes.
```


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Time for Elaboration: CPU = 23.996 ms, elapsed = 52.902 ms.
Time accumulated: CPU = 90.985 ms, elapsed = 259.659 ms.
Peak resident memory used = 27.1 Mbytes.

Time for EDB Visiting: CPU = 0 s, elapsed = 133.991 us.
Time accumulated: CPU = 90.985 ms, elapsed = 259.945 ms.
Peak resident memory used = 27.2 Mbytes.

Circuit inventory:
 nodes 2
 isource 1
 resistor 2

Time for parsing: CPU = 3 ms, elapsed = 104.132 ms.
Time accumulated: CPU = 93.985 ms, elapsed = 364.199 ms.
Peak resident memory used = 27.7 Mbytes.

Transient Analysis `tran2': time = (0 s -> 10 ns)

Important parameter values:

start = 0 s
outputstart = 0 s
stop = 10 ns
step = 10 ps
maxstep = 200 ps
ic = all
skipdc = no
reltol = 1e-03
abstol(V) = 1 uV
abstol(I) = 1 pA
temp = 27 C
tnom = 27 C
tempeffects = all
errpreset = moderate
method = traponly
lteratio = 3.5
relref = sigglobal
cmin = 0 F
gmin = 1 pS

.....9.....8.....7.....6.....5.....4.....3.....2.....1.....0
Number of accepted tran steps = 54
Initial condition solution time: CPU = 0 s, elapsed = 186.92 us.
Intrinsic tran analysis time: CPU = 3.999 ms, elapsed = 3.73197 ms.

Total time required for tran analysis `tran2': CPU = 5.998 ms, elapsed = 114.853 ms.
Time accumulated: CPU = 99.983 ms, elapsed = 600.964 ms.
Peak resident memory used = 32.1 Mbytes.

Aggregate audit (11:24:06 AM, Wed May 11, 2011):
Time used: CPU = 107 ms, elapsed = 680 ms, util. = 15.7%.
Time spent in licensing: elapsed = 118 ms, percentage of total = 17.3%.
Peak memory used = 32.1 Mbytes.
Simulation started at: 11:24:05 AM, Wed May 11, 2011, ended at: 11:24:06 AM, Wed May 11, 2011, with elapsed time (wall clock): 680 ms.
spectre completes with 0 errors, 0 warning, and 0 notices.

▲ Narration of transient analysis progress

Viewing Your Output

The waveform display tool for this simulation example is Virtuoso Visualization and Analysis XL. Virtuoso Visualization and Analysis XL is not shipped with MMSIM6.1. To access Virtuoso Visualization and Analysis XL, install Virtuoso® Schematic Editor (Product number 34500) and Virtuoso® Analog Design Environment (Product number 34510) from the DFII CD.

In this section you will learn the following:

- How to start Virtuoso Visualization and Analysis XL
- How to plot signals
- How to change the color of a trace

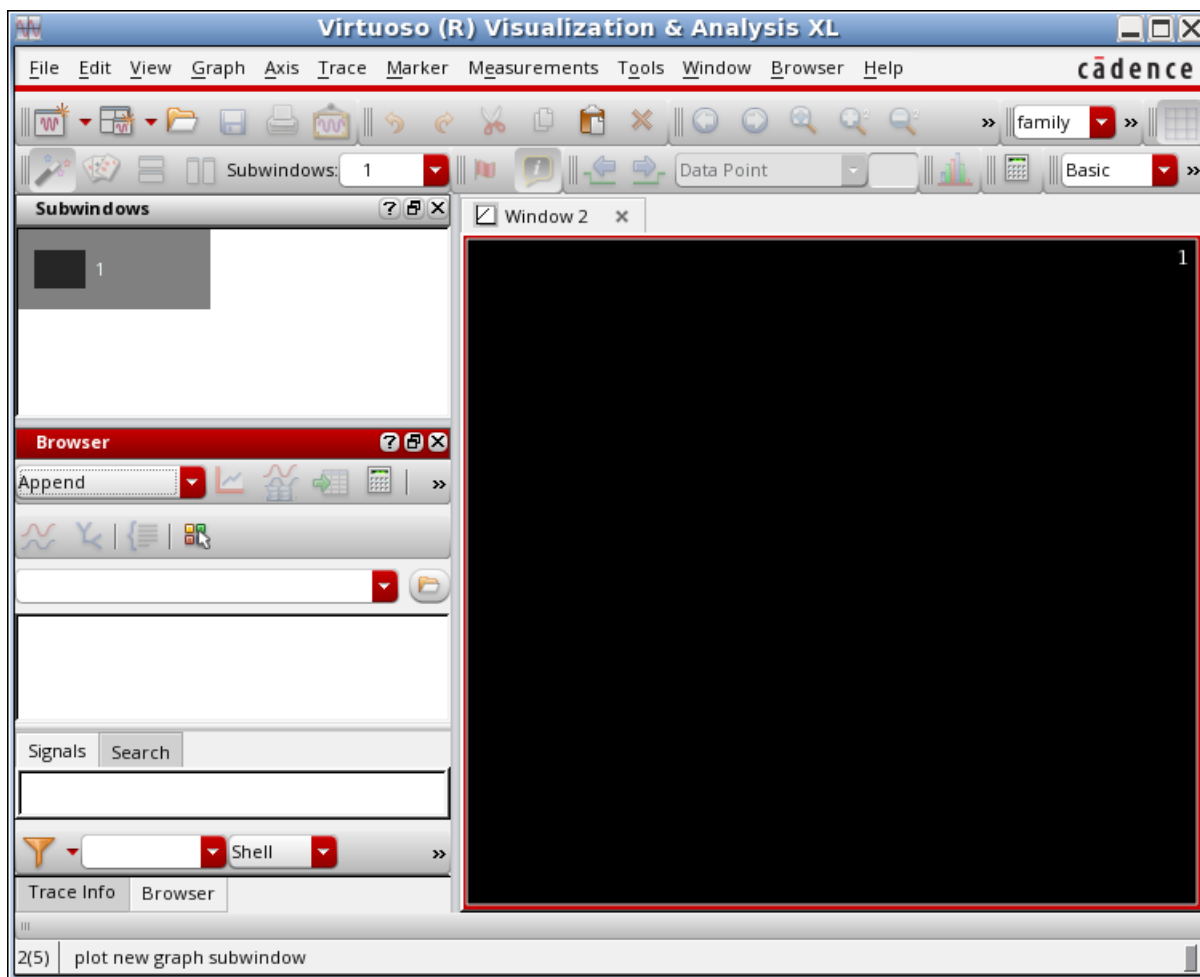
Starting Virtuoso Visualization and Analysis XL

- Type the following at the command line:

```
viva &
```

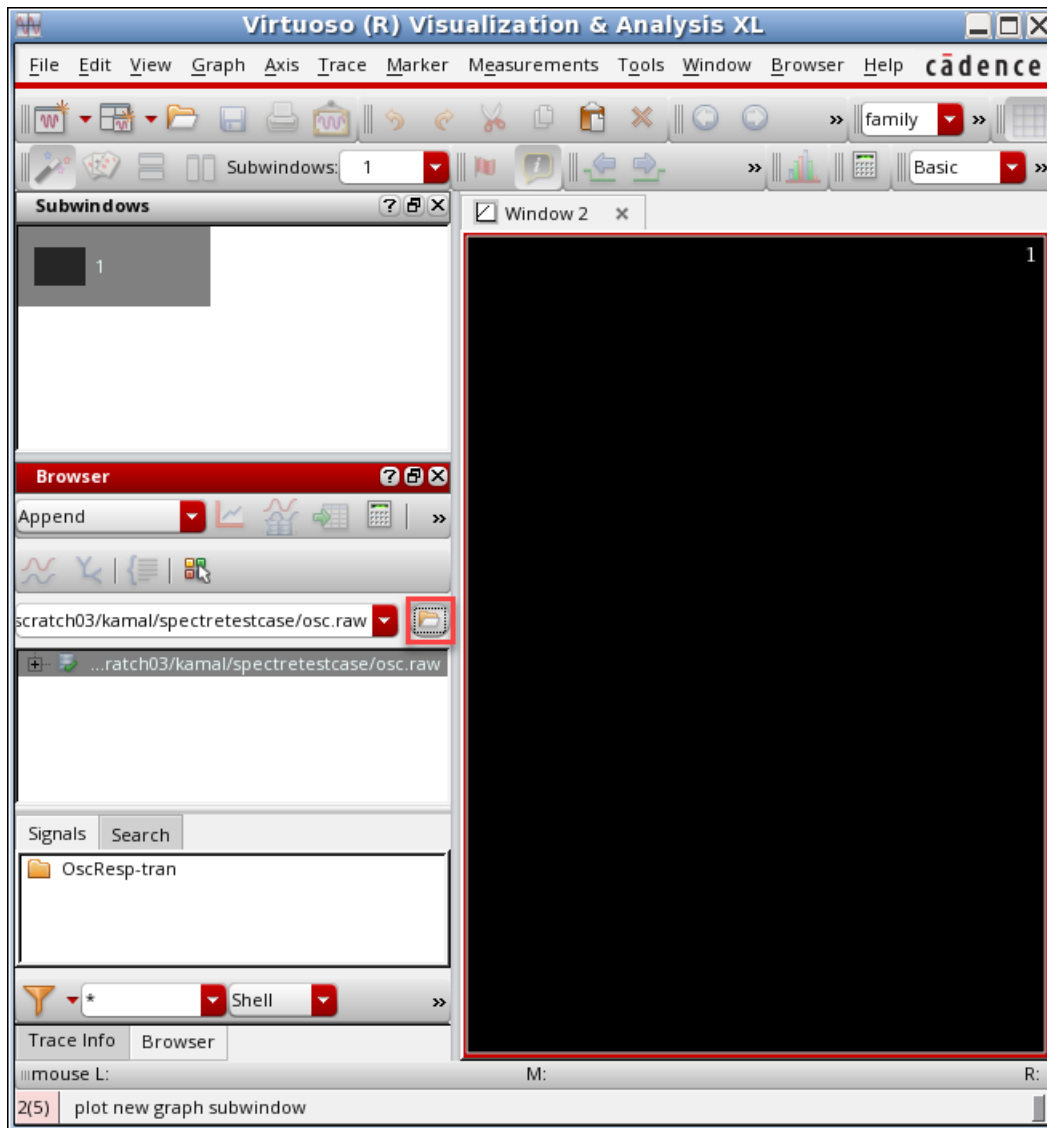
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The Virtuoso Visualization and Analysis XL window opens, as shown below.



Plotting Signals

1. In the Results Browser pane, click *Open Results* and browse to the directory containing the results, as shown below.

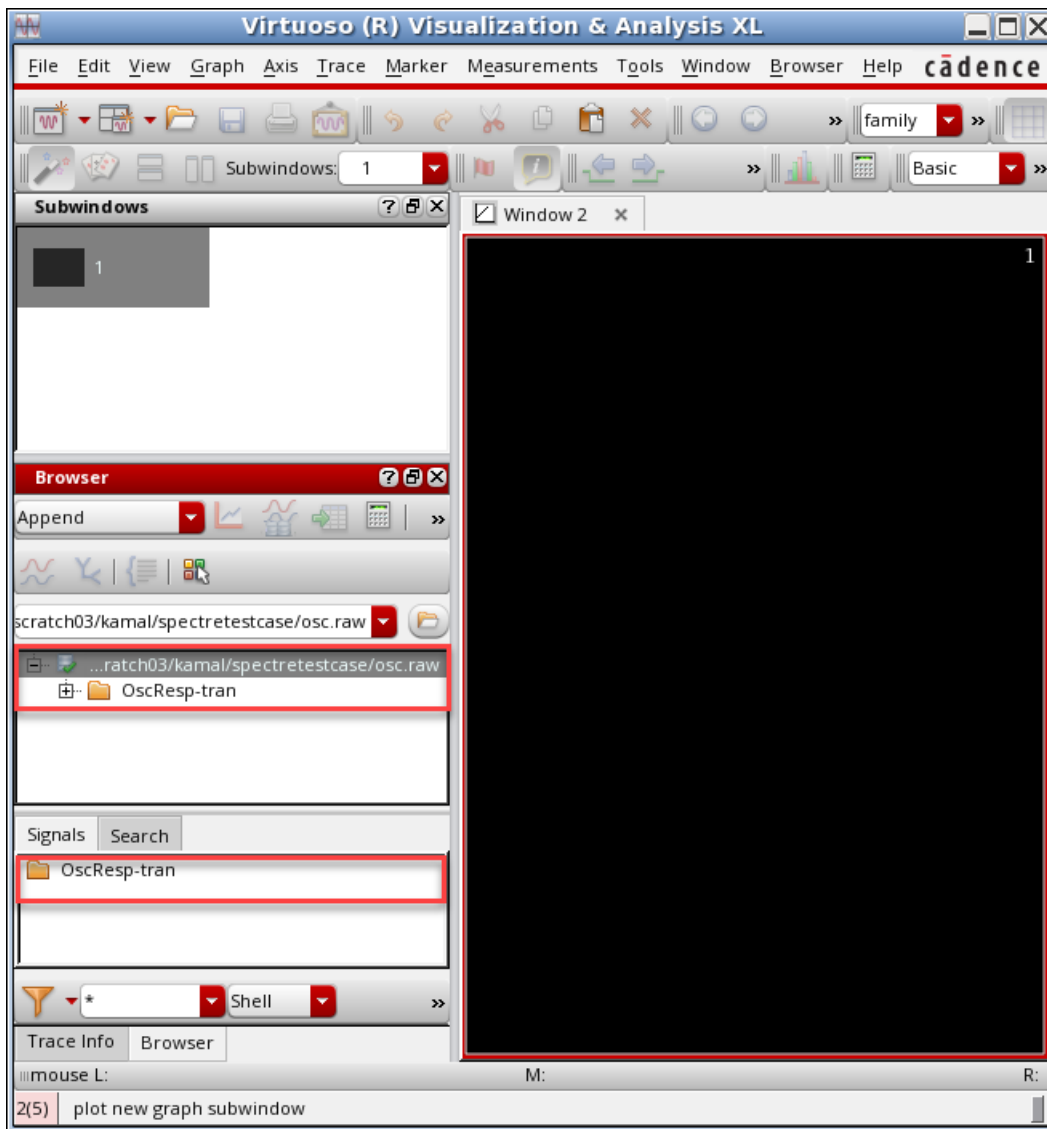


In the Results Browser the top pane displays the results directories and the bottom pane displays the datasets in the selected results directory.

2. Double-click the results directory on the top pane.

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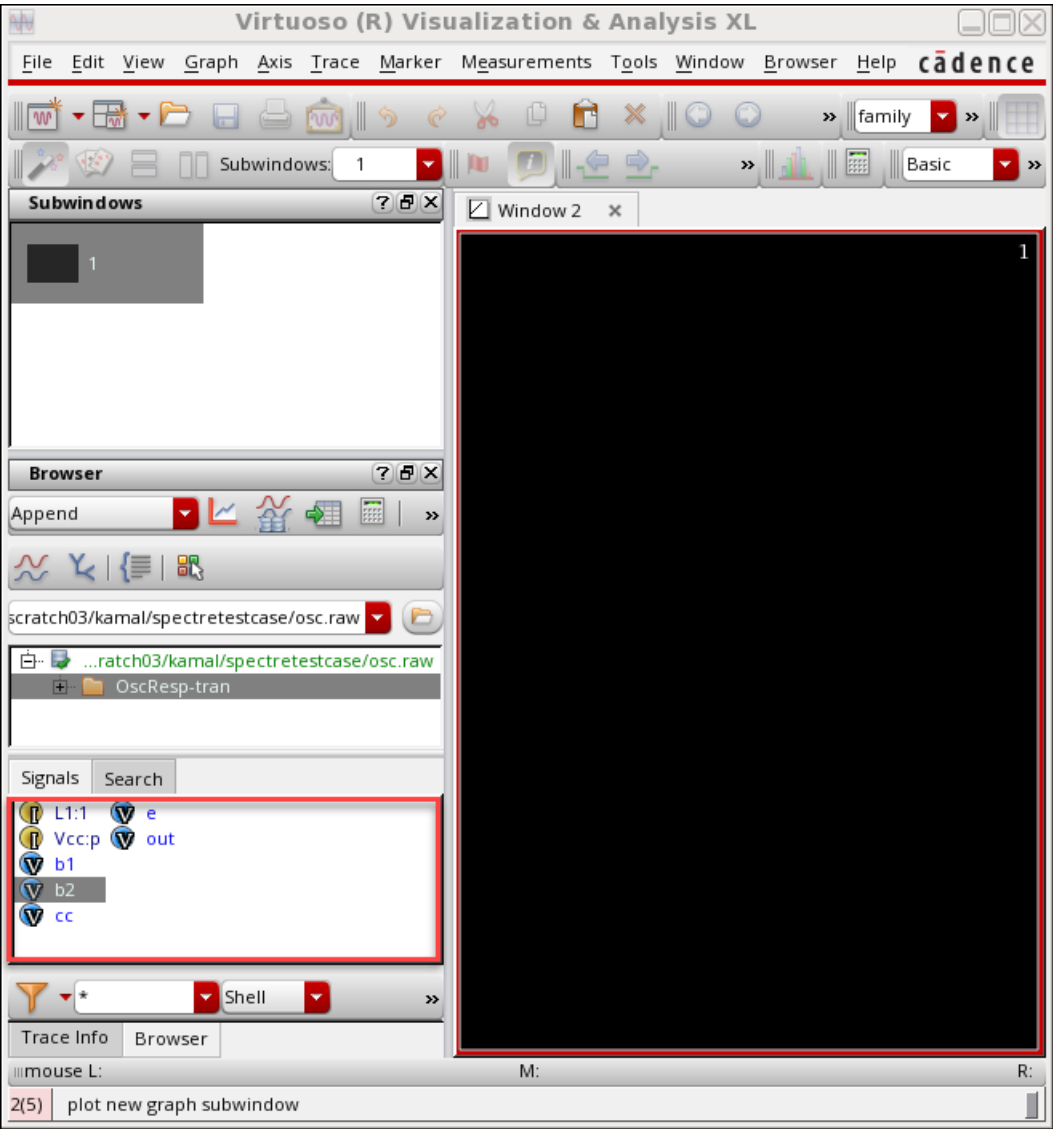
The results directory expands the directory containing data from different analyses (transient analysis in the example) is displayed in the bottom panel, as shown below.



3. Double-click the dataset directory. For example, `OscResp tran`.

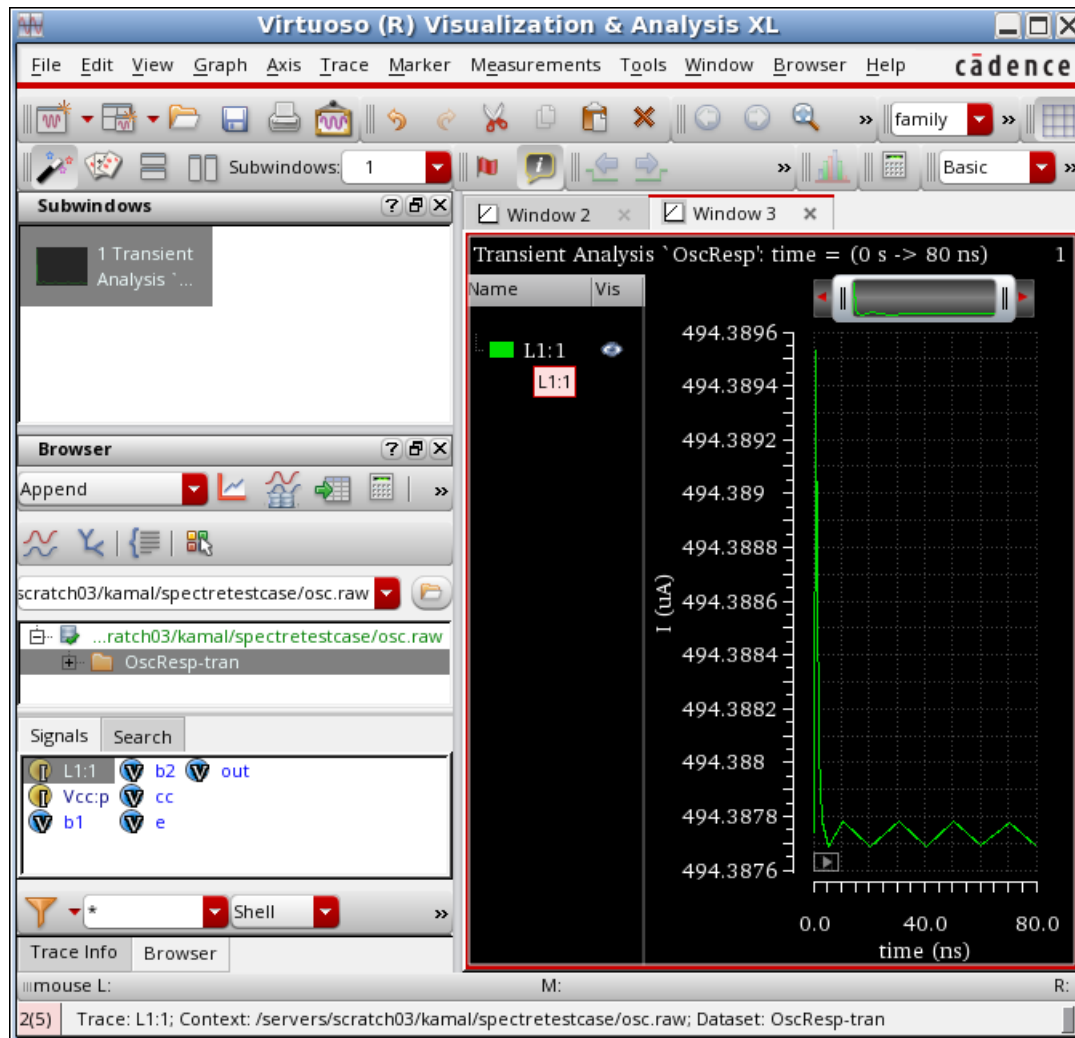
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The signals are displayed in the bottom panel, as shown below.



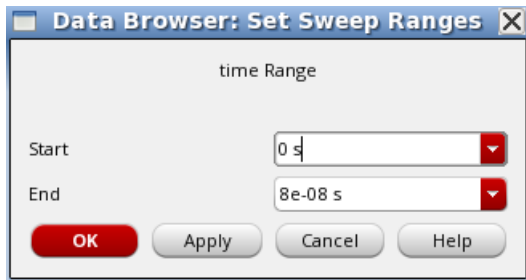
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4. Right-click the signal that you want to plot (for example, the current signal L1:1) and choose *Plot Signal* from the context menu. The signal is plotted, as shown below.



5. To plot a signal over a specific time range, select the signal and click the *Select Sweep Data* icon on the results browser toolbar.

The Set Sweep Ranges form is displayed, as shown below.



6. In the *Start* field, type the time at which you want the plot to begin.
7. In the *Stop* field, type the time at which you want the plot to end.
8. Click *Apply*.
9. Click the *Plot Signals* icon on the results browser toolbar.

Changing the Trace Color

To change the color of the trace,

1. Double-click on the trace.

The Trace Attributes dialog box appears.



2. Click on the foreground color, select the color for the trace.
3. Click *OK*.

Learning More about Virtuoso Visualization and Analysis XL

The Virtuoso Visualization and Analysis XL display tool gives you a number of additional options for displaying your data. To learn more about using Virtuoso Visualization and Analysis, see the *Virtuoso Visualization and Analysis XL User Guide*.

The Spectre APS Circuit Simulator

In addition to the baseline simulation functionalities, Spectre supports the APS technology that provides significant performance gain and simulation capacity over the baseline Spectre simulation with minimum or no accuracy degradation.

The Spectre® APS technology contains newer and better performance technologies to further speed up device evaluation, particularly speeding up the matrix solving part of computation that often dominates large and postlayout circuit simulation.

The Spectre APS technology supports multithreading on multi-core computer platforms.

This chapter discusses the following:

- [Starting Spectre APS Simulations](#)
- [Getting More Performance from Spectre APS Simulation](#)
- [Specifying Multithreading Options](#)
- [Simulation Diagnostics](#)
- [Spectre Mixed-Signal Design Simulation](#)

Starting Spectre APS Simulations

To start a Spectre APS simulation, type the following at the command line:

```
% spectre +aps commandline_options ...
```

You can specify an `errpreset` value with the `+aps` command-line option to override the `errpreset` value in all transient analyses in the netlist. When the `errpreset` value is not specified with the `+aps` command-line option, the `errpreset` value in the analysis statement is used.

For more information on the `errpreset` parameter, see [The errpreset Parameter](#).

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To run Spectre baseline:

```
% spectre [+errpreset=liberal | moderate | conservative ...] input.scs
```

To run Spectre with APS:

```
% spectre +aps[=liberal|moderate|conservative] netlist
```

or

```
% spectre +aps [+errpreset=liberal|moderate|conservative] netlist
```

Example

```
% spectre +aps=liberal adc.scs
```

In the above example, Spectre APS is launched using the liberal setting.

Getting More Performance from Spectre APS Simulation

Spectre APS uses identical simulation algorithms (numerical tolerance control, time step control, Newton iteration control, analytical device model, and so on) as baseline Spectre. It is designed to produce identical simulation results as baseline Spectre. Spectre is known to focus and produce accurate simulation results. Spectre APS preserves all of these numerical simulation algorithms and it is expected to produce a near identical simulation numerical noise floor as baseline Spectre. This tight accuracy correlation between baseline Spectre and Spectre APS does restrict some additional simulation performance.

To further speed up simulation, you can use the `++aps` simulation mode. The `++aps` simulation mode has exactly the same use model and simulation feature coverage as default Spectre APS. You can start a `++aps` simulation, as follows:

```
% spectre ++aps ...
```

`++aps` supports the same `errpreset` parameters and uses the same numerical tolerance controls as baseline Spectre and Spectre APS. However, it is not restricted to use the same time step and Newton iteration control algorithms. The `++aps` simulation produces a similar simulation numerical noise floor as baseline Spectre and Spectre APS.

Postlayout simulation often poses a severe simulation performance challenge. It makes DC analysis difficult to converge and transient simulation much longer to complete. There are many numerical techniques available in Spectre to address these challenges, such as parasitic RC reduction, effective and accurate coupling capacitor handling, and specific DC algorithm for postlayout simulation. A simple `+postlayout` command-line option is available in Spectre for maximizing postlayout simulation performance. You can start a Spectre APS simulation on a postlayout design, as shown below.

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```
% spectre ++aps +postlayout ...
```

To speed up the transient simulation for circuits containing a large number of mutual inductors, use the `+lopt` command-line option, as shown below.

```
% spectre +aps +lopt...
```

Circuit simulation performance is directly related to the core simulation engine, but often can be heavily skewed due to certain computationally intensive simulation features, such as device checking asserts, and large amount of current and power probing. To assist simulation performance debugging, a lightweight (`+lite`) simulation setting that automatically strips away all of these computationally intensive peripheral simulation features is available. You can enable the lightweight simulation, as follows:

```
% spectre +aps +lite ...
```

To improve the simulation accuracy of high-voltage circuits (where the maximum voltage is greater than 10 volts), or circuits that have convergence issues and report large capacitance values in the log file, you can set the `highvoltage` parameter in the `options` statement to `yes`.

```
opt1 options highvoltage=yes
```

Use this option with `moderate/liberal` mode, if the original simulation needs `conservative` mode to get accurate results.

Designs having different ground voltages may have an impact on the simulation accuracy. You can use the `vrefgnd` parameter in the `options` statement to make the default simulation tolerance criteria same for such designs. For example:

```
Opt options vrefgnd=gnd_node_name subckt=[sub1]
```

or

```
Opt options vrefgnd=gnd_node_name inst=[sub_inst1]
```

Specifying Multithreading Options

Spectre baseline, Spectre APS, Spectre X, and Spectre XPS S-mode technologies support multi-threaded computation on multi-core computer platforms. Spectre APS/XPS and Spectre X have better multithreading scaling compared to Spectre baseline technology.

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The default settings for multithreading are given below:

Simulator	Default Multithreading	Default number of threads when Multithreading is on	Maximum number of threads allowed
Spectre	Off	4	4
Spectre APS	On	8	64
Spectre X	On	8	512
Spectre XPS S-mode	On	8	64

To turn off multithreading, use the following commands:

```
% spectre -mt ...  
% spectre +aps -mt ...
```

To turn on the multithreading feature in baseline Spectre, use the following command:

```
% spectre +mt ...
```

There is no need to specify `+mt` for Spectre APS run because multithreading is on by default.

To manually specify the number of threads to be used, instead of the default threads, use the following command:

```
% spectre +mt=4 ...  
% spectre +aps +mt=4 ...  
% spectre +preset=ax +mt=4...  
% spectre +xps=s +mt=4 ...
```

Spectre supports various computer farm management tools, such as LSF, Sungrid engine, NetworkComputer, LoadLeveler, and netbatch with the following statement:

```
% spectre +aps +mt=lsf | sge | nc | loadleveler | farm | netbatch...
```

where the Spectre session will use the number of cores allocated by the farm tools.

To benefit from multithreading technology, a circuit should have at least 250 devices. When a circuit is too small, the multithreading option is turned off automatically.

Using the query Option

The `+query` command-line option with possible values of `mtinfo`, `meminfo`, `all`, `alllic`, and `tokenlic` (default) enables you to get an estimate of the number of threads or licenses required to run a simulation without actually running the simulation.

- `mtinfo` - prints the recommended number of threads required to run the simulation in a multi-threaded environment.
- `meminfo` - prints an estimate of the memory that would be required to run a design
- `all` - prints both the number of threads and the estimate of memory that would be required to run a design.
- `alllic` - prints all possible combination of licenses required to run a design.
- `tokenlic` - prints the number of Spectre MMSIM tokens required to run the design.

Example

```
% spectre +query=mtinfo +aps input.scs.....
```

Simulation Diagnostics

At times, you need additional debugging information to investigate the performance or convergence-related simulation issues. By default, the simulation log file now contains a pre-simulation summary and a post-transient simulation summary with suggestions on how to speed up the simulation further. In addition, you can use the Spectre command-line option, `+diagnose`, to dump additional debugging information into the simulation log file. The following is an example of using the `+diagnose` option:

```
% spectre +aps +diagnose input.scs
```

The `+diagnose` option automatically enables the AHDL linter feature, and outputs the following additional information to the log file:

- Convergence-related information for time steps less than 1ps. This can be controlled by using the `warnminstep` option.
- A summary containing statistics about time steps, nodes with convergence issues, and node or device activity information.

Note: The `+diagnose` option has minimal impact on the simulation time, however, it generates a lot of information and may not be appropriate for general use.

Spectre Mixed-Signal Design Simulation

The Spectre Mixed-Signal (MS) simulation mode delivers a high-performance transistor-level multi-rate simulation solution by combining a highly accurate SPICE engine (Spectre APS) together with a fast digital simulation engine (Spectre XPS). The identification between the analog and digital portions of the circuit is done automatically, with the added flexibility for advanced users to optimize it.

Spectre MS is fully integrated into the Spectre binary sharing the same product infrastructure with Spectre, Spectre APS, Spectre X, and Spectre XPS. The use model is identical to that of Spectre, with the netlist syntax, device models, analysis setups, and output formats being fully compatible.

Spectre MS speeds up both pre-layout and postlayout simulations. The supported postlayout simulation flows are: Virtuoso extracted view, included DSPF, backannotated DSPF/SPEF, and flat postlayout SPICE and Spectre netlist files.

Spectre MS supports most Spectre transient features including save, ic, nodeset, measure, vec/vcd, asserts, static design checks, selective dynamic design checks, RC reduction, and EMIR. It also supports dynamic parameters. However, dynamic parameters are supported only for the analog partition (APS). For more information on dynamic parameters, refer to the *Transient Analysis* section in the *Spectre Circuit Simulator Reference* manual.

Advanced simulation features, such as info, alter, device reliability, and montecarlo are currently not supported, however, support for these features may be added incrementally in future releases.

Note: The MS mode has been integrated into the Analog Design Environment (ADE) and is available starting with the IC6.1.6 ISR6 release. It is recommended to use the revised MS mode ADE integration in IC6.1.8 ISR14.

Starting an Spectre MS Simulation Run

You can invoke the MS mode using the Spectre binary with the following command:

```
% spectre +ms input.scs ...
```

You can specify the `errpreset` setting at the command line, with `+aps=liberal` being the default setting.

When the MS mode is enabled, a message is displayed in the log file stating the same.

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When using a SPICE runset, add the `+spice` option to ensure that the netlist convention and device models are interpreted in a consistent manner as traditional SPICE, instead of Spectre.

The MS mode supports multithreading on multicore machines. The multithreading use model and behavior are identical to Spectre APS.

Adjusting MS Speed and Accuracy

The Spectre MS mode supports all performance and accuracy settings of Spectre APS for the analog portion simulation. The default `errpreset` setting is `liberal`, which is sufficient for the functional verification of most mixed-signal designs.

The simulation speed and accuracy of digital portions in the MS mode can be controlled by the command-line option `speed=0/1/2/3`. The default value is 2, which is sufficient for most applications. Use `speed=0` for more accurate timing and power simulation of digital portions. `speed=1` is a little faster than `speed=0`. Use `speed=3` for fastest digital verification, however, this may have an impact on accuracy.

The following example shows the combination of analog options (`++aps=liberal`) with digital options (`speed=3`):

```
% spectre +ms ++aps=liberal +speed=3 input.scs
```

Digital Partitioning and Virtual Power Nodes

The Spectre MS mode automatically detects the digital functions in a given circuit. For cases where a design has explicit hierarchical digital or analog functions, you can manually identify the functional blocks (subcircuit, instance) by using the following Spectre options:

Spectre format:

```
optD options cktpreset=digital subckt=[dig_ctrl pll]
optA options cktpreset=analog subckt=[opamp adc]
```

or

```
optD options cktpreset=digital inst=[x1.xdig_ctrl x1.xpll]
optA options cktpreset=analog inst=[x2.xopamp x2.xadc]
```

SPICE format:

```
.options cktpreset=digital subckt=[dig_ctrl pll]
.options cktpreset=analog subckt=[opamp adc]
```

or

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```
.options cktpreset=digital inst=[x1.xdig_ctrl x1.xpll]
.options cktpreset=analog inst=[x2.xopamp x2.xadc]
```

Digital detection works seamlessly for digital circuitry with ideal DC power supplies or identified virtual power supplies. The MS mode not only detects the virtual power supplies (that is, internal VDD generator) in the design automatically, but also provides the flexibility to define the virtual power supply nodes manually. The log file provides information on the nodes that are identified as power/ground supplies and other nodes that are potential power/ground supplies. A sample log file report is shown below.

Digital Detection Vsource and Virtual Power Supply Node Summary

Type	#CC	#Bulk	Voltage	Name
GND	17239	34021	0	0
VSOURCE	16934	20923	3.3	AVDD
VPN	3798	2301	1.9	VDIG
VGND	3951	342	0	VGND1
Possible	202	50	TBD	I1.VDD_DIG
Possible	310	23	TBD	I1.RF_VDD
Possible	311	31	TBD	I1.VSS

For the detected nodes, the table reports the node type, the number of channel connections (#CC), the number of bulk connections (#Bulk), the node voltage, and the node name. The following node types are reported:

- GND - ground node.
- VSOURCE - ideal power supply node.
- VPN - virtual power supply node
- VGND - virtual ground node.
- Possible - potential power/ground supplies

Nodes of type GND, VSOURCE, VPN, and VGND are used as power supply and ground nodes when detecting digital circuitry. The Possible type refers to potential power/ground supplies that are not used for digital circuit detection.

You can define the virtual power supply nodes manually by using the `ms_vpn` option that defines the pairs of node names (wildcard is supported) and voltage values. The virtual ground nodes can be defined using the `ms_vgnd` option. The ground voltage is assumed to be 0V.

Spectre format:

```
opt1 options ms_vpn = [I1.VDD_DIG 1.8 I1.VDD_DIG1 3.3]
opt3 options ms_vgnd = [I1.VSS]
```

SPICE format:

```
.options ms_vpn = [I1.VDD_DIG 1.8 I1.VDD_DIG1 3.3]
.options ms_vgnd = [I1.VSS]
```

If required, you can define the global virtual power supply voltage by using the `ms_vpnv` option, as shown below.

Spectre format:

```
opt2 options ms_vpnv = 1.2
```

SPICE format:

```
.options ms_vpnv = 1.2
```

The default global value is 1.8V.

In case the virtual power supply voltage is not known, you can use the `auto_vpn` option to enable Spectre to detect the voltage automatically, as shown below.

Spectre format:

```
opt4 options ms_vpn = [I1.VDD_DIG auto_vpn I1.RF_VDD auto_vpn]
```

SPICE format:

```
.options ms_vpn = [I1.VDD_DIG auto_vpn I1.RF_VDD auto_vpn]
```

The maximum voltage for the device models in the digital simulation engine is detected automatically. If required, it can be set using the `vdd` option, as shown below.

Spectre format:

```
opt4 options vdd = 1.8
```

SPICE format:

```
.options vdd = 1.8
```

The default value is 3.3V.

Spectre MS DC Operating Point Calculation

The Spectre MS mode calculates the DC operating point before performing the transient simulation. By default, the DC operating point for the entire circuit is calculated by Spectre

APS (+msdc=aps). For cases where the Spectre APS operating point calculation takes too long, you can enable the mixed-signal DC calculation – Spectre APS for the analog partition and Spectre XPS for the digital partition, by using the +msdc=ms command-line option, as shown below.

```
% spectre +ms +msdc=aps input.scs
```

The above command calculates the DC operating point using Spectre APS.

```
% spectre +ms +msdc=ms input.scs
```

The above command enables the mixed-signal DC calculation.

Spectre MS Current Accuracy

When using ideal or strong virtual power supplies, Spectre MS mode properly calculates the current consumption based on the active and leakage currents of all driven analog and digital blocks.

However, when the virtual power supplies are weak, the following time window-based options may be used to obtain accurate current values:

```
opt1 options ms_vpni_start=1u ms_vpni_stop=10u
```

Since these options significantly impact the simulation performance, it is recommended to define the time window as small as possible. In addition, it is recommended not to enable these options during the ramp-up period.

Handling Macro Device Models

The Spectre MS mode, by default, effectively recognizes device models including BSIM3V3, BSIM4, BSIMCMG, BSIMSOI, PSP, and so on. Device recognition enables digital detection that is critical to ensure that the Spectre MS mode gets the best possible simulation performance. Even complicated device macro models with more than four terminals and additional elements (resistors, capacitors, parasitic diodes, parasitic BJT's) are automatically handled, if the first four terminals are the primary MOSFET `d g s b` terminals.

Complex elements with Verilog-A, behavior source (bsource), or multiple MOSFET elements inside require you to explicitly define the name of the macro model subcircuit, as follows:

Spectre format:

```
opt1 options macro_mos=[mos1 mos2]
```

SPICE format:

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```
.options macro_mos=[mos1 mos2]
```

Here, `mos1` and `mos2` are subcircuit definition names for macro device models.

If the first four terminals of the macro model are not `d g s b`, then the default macro model handling does not work. The required port detection and handling for such macro models can be enabled with the following option:

Spectre format:

```
opt1 options macro_mos_wrapper=yes
```

SPICE format:

```
.options macro_mos_wrapper=yes
```

Spectre MS Postlayout Simulation

The Spectre MS mode supports different postlayout simulation flows (Virtuoso extracted view, included DSPF files, and flat postlayout SPICE and Spectre netlist files), as well as DSPF/SPEF backannotation.

Non-backannotation Postlayout Simulation Flow

You can enable the Spectre MS postlayout simulation by using the `+postlayout` command-line option, as follows:

```
spectre +ms +postlayout input.scs
```

The flow automatically enables RC reduction, optimized RC element handling, and DC algorithms. You can set RC reduction in the analog portion simulation to be more conservative (`+postlayout=hpa`).

```
spectre +ms +postlayout=hpa input.scs
```

DSPF/SPEF Backannotation

The alternative DSPF/SPEF backannotation flow is enabled with the DSPF/SPEF backannotation options. This flow does not require the `+postlayout` command-line option.

Spectre format:

```
Opt1 options spf="I1 pll.spf
```

```
Opt2 options spef="I1 pll.spef
```

SPICE format:

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```
.options spf="I1 pll.spf
.options spef="I1 pll.spef
```

All RC backannotation-related Spectre options, such as `spfscale`, `spfxtorprefix`, and `spfaliasterm` are supported. If RC reduction is required, it can be enabled as part of the backannotation process (`spfrcr`, `spfrcrfmax`). For more information on these options, refer to [Parsing Options Used in Backannotation](#).

The Spectre MS logfile provides two backannotation reports. The first report summarizes the RC elements backannotated to the digital partitions, while the second report summarizes the RC elements backannotated to the analog partitions.

When using Spectre MS for postlayout designs, `+speed=3` is not recommended. For accuracy comparison, Spectre APS without RC reduction is recommended as the golden reference. The performance of Spectre XPS with `+postlayout` should be compared against Spectre APS with `+postlayout`.

Spectre MS Partitioning Report

Spectre MS provides the ability to print a partitioning report. The report provides information about the analog and digital portions of each subcircuit instance with more than 50 elements.

To print the partitioning report, use the `ms_part_report=depth` option as follows:

Spectre format:

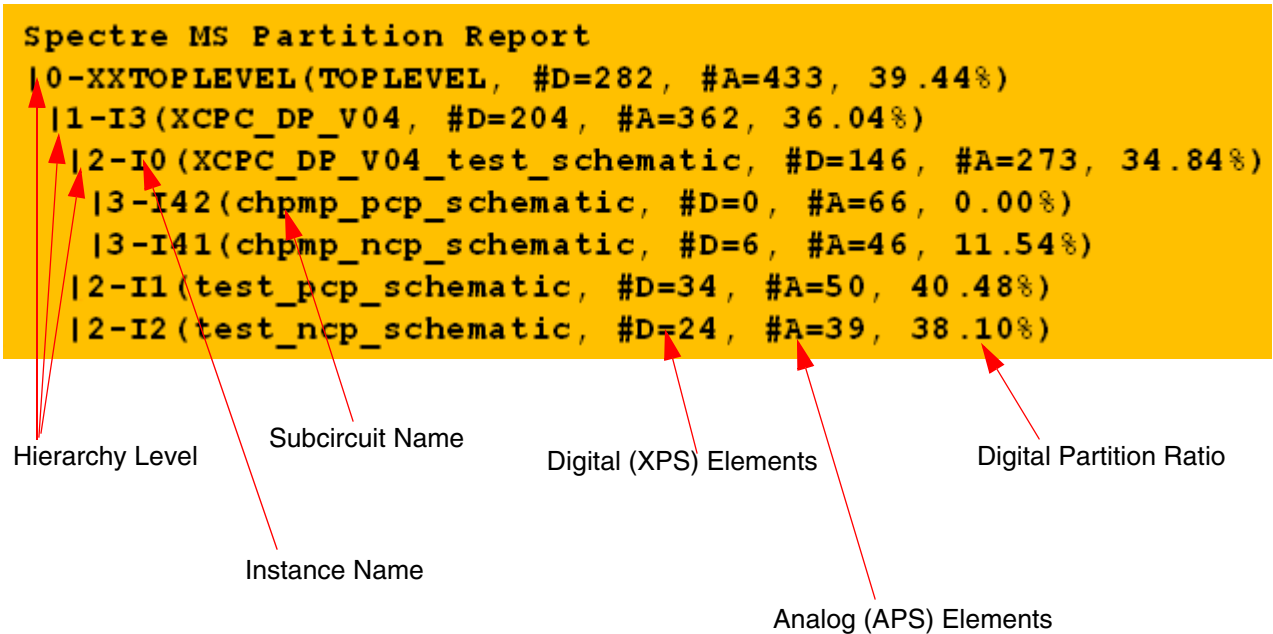
```
opt1 options ms_part_report=10
```

SPICE format:

```
.options ms_part_report=10
```

Here, *depth* is the hierarchical depth counted from top level (`depth=0`). The partition report is written to a file named `partition_<netlist>.rpt`.

The following is an example of the partitioning report:



The Spectre XPS Circuit Simulator

Spectre® eXtensive Partitioning Simulator (Spectre XPS) is the next generation transistor-level circuit simulator of Cadence that provides high simulation performance and large simulation capacity. It addresses the design and verification needs of full-chip low-power designs at advanced process nodes. In addition, it incorporates a completely new circuit partitioning and multirate technology, and provides reasonable accuracy for timing and power to meet the tighter design margins.

This chapter discusses the following topics:

- [Starting Spectre XPS Simulation Run](#) on page 78
- [Reviewing the Log File](#) on page 79
- [Output Files](#) on page 82
- [Multithreading Support](#) on page 85
- [Spectre XPS Options](#) on page 87
- [Post-layout simulation](#) on page 94
- [Spectre XPS SRAM Simulation](#) on page 96
- [Spectre XPS DRAM Simulation](#) on page 100
- [Spectre XPS Flash Simulation](#) on page 106

Starting Spectre XPS Simulation Run

Most of the command-line options that are used to run Spectre XPS simulation are the same as Spectre and Spectre APS.

To start a Spectre XPS simulation run, type the following at the command line:

```
spectre +xps +cktpreset=dram -64 -f fsdb +spice +mt=N -outdir run1 -outname xps_out  
top.sp
```

The following table lists the command-line options and their descriptions:

Option	Description
+xps	Enables the Spectre XPS simulator. The default simulator is Spectre baseline.
+cktpreset=dram	Specifies the Spectre XPS preset for DRAM simulation. The other presets include <code>pcram</code> , <code>sram</code> , and <code>flash</code> .
-64	Enables the 64-bit version of Spectre, which is required to run the simulation with memory greater than 4GB.
-f fsdb	Generates the waveform file in <code>fsdb</code> format.
+mt=N	Specifies the number of cores for multithreading. The default is a single thread.
+spice	Ensures that the netlist convention and device models are interpreted consistently as traditional SPICE, instead of Spectre.
-outdir run1	Defines the output directory for the simulation results and the simulation log file.
-outname xps_out	Defines the names of output files, including log file, waveform, and measure. The default name is the name of the top-level netlist file. If this option is specified, waveforms are saved in the output directory instead of the raw directory.
top.sp	Specifies the top-level netlist for simulation.

You can also get more information about command options, components, analyses, controls, and other selected topics by using the `spectre -h` command to access the Spectre online help.

Reviewing the Log File

Spectre XPS shares the same format for the output log file as Spectre and Spectre APS. The log file provides important information about the Spectre XPS simulation run. Therefore, it is recommended to review the log file after starting the simulation.

The output log file displays the following information:

- Warning/Info/Error messages related to netlist parsing, models, and MDL (.measure)
- Staged run time and memory consumption information
- Circuit inventory details
- Output statistics for probe/save and measurement
- Simulation mode and important parameters/options used
- Detailed transient simulation information, which is controlled by the `annotate` parameter in the `tran` statement

The following sections discuss some of the important information stored in the log file and the options to control the log file in detail.

Spectre XPS cktpreset Mode Information

In the Spectre XPS log file, the following message indicates that DRAM mode with multithreading is successfully enabled:

```
Notice from spectre during initial setup.
```

```
XPS Enabled ( cktpreset=dram ).
```

```
.....
```

```
Multithreading Enabled: 8 threads in the system with 20 available processors.
```

File Reading and Parsing Related Information

The Spectre XPS log file provides information on the files read in a simulation run, as shown below.

```
Readingfile: /projects/p100/simulation/xps_run/top.sp
```

```
Readingfile: /projects/p100/simulation/xps_run/netlist.cdl
```

```
Reading file: /projects/p100/simulation/xps_run//PDK/Spectre/v1.1/16nm_model.scs
```

Spectre XPS provides an option, `print_section`, with possible values of `no` and `yes` that enables you to print information about the library files read in the simulation. When this option

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is set to `no`, only the library file information is printed in the log file. However, when this option is set to `yes`, detailed sections of the library files read in the simulation are printed in the log file.

For example, if you specify `print_section=yes`, the log file displays the following information for the same example:

```
Readingfile: /projects/p100/simulation/xps_run/top.sp
Readingfile: /projects/p100/simulation/xps_run/netlist.cdl
Loading section: SS from file: /projects/p100/simulation/xps_run//PDK/Spectre/
v1.1/16nm_model.scs
Loading section: TT BIP_DIO from file: /projects/p100/simulation/xps_run//PDK/
Spectre/v1.1/16nm_model.scs
Loading section: TT_RES_DISRES from file: /projects/p100/simulation/xps_run//
PDK/Spectre/v1.1/16nm_model.scs
```

Output and IC/Nodeset Related Information

Spectre XPS provides useful information in the log file for the signals probed, measured, or set with IC/nodeset, especially with wildcards.

An example of the log file and the messages is given below.

Output statements:

```
.probe 4
.measure 1
save 0
```

Design checks inventory:

```
dyn_dcpath 2
dyn_exi 1
```

Wildcard match summary:

```
probe x(XI0.xTOP_0.xIO_SLICE.xio_right.*.vddpe) : 67
probe i(vv*) depth= 1:      3
probe i(XI0.*.x_mxmi41.mxppua) : 0
probe v(*) depth= 5:      3938
ic *.sao      64
ic *.ncored   32768
ic *.cored    32768
ic *.bl       0
ic *.nbl      0
```

Output and IC/nodeset summary:

```
probe 4008
measure 1
ic 65600
```

Options to Control Warning/Error Messages in Spectre XPS

Messages in the Spectre XPS simulator, like Spectre and Spectre APS, are categorized based on three severity levels: INFO, WARNING, and ERROR. In addition, each message includes a unique alphanumeric message ID enclosed in parentheses.

You can use the following global options to customize the number of messages and their severity based on ID:

Option	Description
maxwarns=5	Specifies the maximum number of times a warning message, with the same message ID, is generated per analysis. The default value is 5.
maxwarnstologfile=5	Specifies the maximum number of times a warning message, with the same message ID, is printed to the log file per analysis. The default value is 5.
maxnotestologfile=5	Specifies the maximum number of times an INFO message, with the same message ID, is printed to the log file per analysis. The default value is 5.

Examples

```
.option maxwarns=1
.option maxwarnstologfile=10
```

You can use the following options to control the number of messages or change the severity of a message based on ID:

```
.option warning_id=[SFE-3013] warning_limit=10
.option warning_id=[SPECTRE-17100] warning_change_severity=error
```

Transient Simulation Information

Use the parameter `annotate` in the `tran` statement to display the status of the transient simulation in the log file. It is recommended to set the value of the `annotate` parameter to `estimated` to display detailed information in the log file. For example:

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```
.tran 1n 1u annotate=estimated
```

The following is an example of the transient simulation information that is displayed in the log file:

```
transient0: time = 10.15 ns      (10.6 ), step = 735.2 fs      (764 u)
            cpu = 223.4 s, elapsed = 83.7 s, steps = 0, mem = 11770.8 MB
            estimated completion time: 00:11:49
transient0: time = 10.23 ns      (10.6 ), step = 3.639 ps      (3.78 m)
            cpu = 348.9 s, elapsed = 106.4 s, steps = 0, mem = 11771.8 MB
            estimated completion time: 00:14:54
transient0: time = 10.45 ns      (10.9 ), step = 69 ps          (71.7 m)
            cpu = 403.9 s, elapsed = 117.2 s, steps = 0, mem = 11773.2 MB
            estimated completion time: 00:16:01
transient0: time = 11.5 ns        (12 ), step = 413.6 ps        (430 m)
            cpu = 416.4 s, elapsed = 119.7 s, steps = 0, mem = 11774.0 MB
```

The above log file contains the following information related to transient simulation:

- The current CPU time/elapsed time for transient simulation
- The estimated time required to complete the rest of transient simulation.
- The time step of Spectre XPS. This information can be helpful to debug performance issues. Spectre XPS takes bigger time steps if there is no activity in the circuit.

Output Files

After a simulation completes, Spectre XPS writes the following output files based on the design setup:

- Log file: Defined using the `+log/=log/-log` command-line options
- Measure results: `*.measure` and `*.mt0` files
- Waveform files and format: Defined using the `-format` (or `-f`) command-line option
- Operating point files: `*.ic0` and `*.op0` files
- Circuit check results

Using the Command-Line Option `-outdir`

You can use the `-outdir` command-line option to specify the output directory for the simulation files.

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The following example demonstrates the location and names of the output files.

```
spectre -64 +xps +cktpreset=sram +speed=2 +spice -outdir xps_x4_out top.sp
```

The following are the file names and their locations:

```
xps_x4_out/  
|-- top.log  
|-- top.mt0  
|-- top.measure  
|-- top.ic0  
|-- top.op0  
|-- top.raw  
    |-- logFile  
    |-- transient1.tran.fsdb  
    |-- transient1.meas_tran  
    |-- top.sqlldb  
    |-- mmcheck2html.xsl  
    |-- traverse.css  
    |-- sorttable.js  
    |-- top.dynamic.xml  
    `-- top.dynamic.rpt
```

Using the Command-Line Option -outname

You can use the command-line option `-outname` to change the names of output files and their locations. When you use this option, the waveform files are moved from the `raw` directory to the specified output directory. The following is the syntax to specify the `-outname` command-line option:

```
-outname <out_dir_name>/<new_file_name>
```

Here, `out_dir_name` is the name of the output directory and `new_file_name` is the name of the new file. You can specify either of the two or both the options in a single statement.

Following are some of the examples of using the `-outname` command-line option.

Example1

```
spectre -64 +xps +cktpreset=sram +speed=x4 +spice -outname xps_x4_out/ top.sp
```

In the above example, the value, `xps_sp2_out/`, of the command-line option `-outname` contains a slash (/), which means it is a directory name. Specifying this option will cause the waveform files to move outside the `raw` directory.

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The file names and their locations are changed as follows:

```
xps_x4_outname/  
|-- top.fsdb  
|-- top.log  
|-- top.measure  
|-- top.mt0  
|-- top.ic0  
|-- top.op0  
|-- top.raw  
    |-- logFile  
    |-- transient1.meas_tran  
    |-- mmcheck2html.xsl  
    |-- traverse.css  
    |-- sorttable.js  
    |-- top.sqldb  
    |-- top.dynamic.xml  
    `-- top.dynamic.rpt
```

Example2

```
spectre -64 +xps +cktpreset=sram +speed=x4 +spice -outname out_newname top.sp
```

In the above example, only a name is specified with the `-outname` command-line option. This will cause the file name of the output files to change to the new one and the waveform files to move outside the raw directory. The file names and their locations are changed as follows:

```
./  
|-- new_outname.fsdb  
|-- new_outname.log  
|-- new_outname.measure  
|-- new_outname.mt0  
|-- new_outname.ic0  
|-- new_outname.op0  
|-- top.raw  
    |-- logFile  
    |-- transient1.meas_tran  
    |-- mmcheck2html.xsl  
    |-- traverse.css  
    |-- sorttable.js  
    |-- top.sqldb  
    |-- top.dynamic.xml  
    `-- top.dynamic.rpt
```


Example 3:

```
spectre -64 +xps +cktpreset=sram +speed=2 +spice -outname xps_x4_out/new_outname
top.sp
```

In the above example, both output directory and output file name are specified with the `-outname` command-line option. The file names and their locations are changed as follows:

```
xps_x4_out/
|-- new_outname.fsdb
|-- new_outname.log
|-- new_outname.measure
|-- new_outname.mt0
|-- new_outname.ic0
|-- new_outname.op0
|-- top.raw
    |-- logFile
    |-- transient1.meas_tran
    |-- mmcheck2html.xsl
    |-- traverse.css
    |-- sorttable.js
    |-- top.sqldb
    |-- top.dynamic.xml
    `-- top.dynamic.rpt
```

Multithreading Support

The Spectre XPS technology supports multithreading on multicore computer platforms. The default behavior is to use a single thread for Spectre XPS. You can enable the multithreading feature by using the `+mt` command-line option of the Spectre binary, as shown below.

```
spectre +xps +mt...
```

To manually specify the number of threads to be used, use the following command:

```
spectre +xps +mt=8 ...
```

When multithreading is enabled, the Spectre XPS log file displays the following information:

```
Multithreading Enabled: 8 threads in the system with 20 available processors.
```

To get maximum performance gain from multithreading, it is recommended that the CPU cores for Spectre XPS are within one socket. This is because the CPU cores in one socket have less communication overhead. Spectre XPS automatically selects the CPU cores for optimized performance. You just need to ensure that the number of CPU cores in one socket is greater than the number of specified threads.

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Note: The licensing requirement for Spectre XPS multi-threading is the same as Spectre APS.

To get the server information, use the following command:

```
spectre +query=sysinfo
```

The following hardware and OS platform information is generated. The server in this example has two sockets with 14 CPU cores in both.

```
OS      : Linux 2.6.18-194.el5 x86_64
Linux   : Red Hat Enterprise Linux Client release 5.5 (Tikanga)
Memory  : available 145.8051 GB          physical 405.6638 GB
Swap     : available 94.4486 GB  physical 137.4389 GB
CPU type: Intel(R) Xeon(R) CPU E5-2697 v3 @ 2.60GHz
Hyperthreading is disabled
```

Socket	Proc	Core	
0	0	0	2600.1
	2	1	2600.1
	4	2	2600.1
	6	3	2600.1
	8	4	2600.1
	10	5	2600.1
	12	6	2600.1
	14	8	2600.1
	16	9	2600.1
	18	10	2600.1
	20	11	2600.1
	22	12	2600.1
	24	13	2600.1
	26	14	2600.1
1	1	0	2600.1
	3	1	2600.1
	5	2	2600.1
	7	3	2600.1
	9	4	2600.1
	11	5	2600.1
	13	6	2600.1
	15	8	2600.1
	17	9	2600.1
	19	10	2600.1
	21	11	2600.1
	23	12	2600.1

25	13	2600.1
27	14	2600.1

To benefit from multithreading technology, a circuit should have at least 500 nodes. When a circuit is too small, multithreading is turned off automatically.

Spectre XPS Options

Spectre XPS can be configured to obtain optimized simulation results, performance, accuracy, and waveform file size. The general naming convention for the XPS configuration options is `sim_opt_optName`, which can be specified with:

Spectre format:

```
opt1 options sim_opt_optName=optValue {subckt=[subcktName]}
opt2 options sim_opt_optName=optValue {inst=[instanceName]}
```

SPICE format:

```
.options sim_opt_optName=optValue {subckt=[subcktName]}
.options sim_opt_optName=optValue {inst=[instanceName]}
```

Options Related to Circuit Partitioning

Spectre XPS supports the following two fundamental technologies for circuit partitions:

- Arbitrary partition can break the channel connections of transistors. Therefore, you should not tune this partition.
- To maintain good accuracy, a dynamic group is created for the partitions and their nodes with current conducting path and strong coupling. When the conditions are changed, the group may be destroyed to minimize the impact on performance.

Spectre XPS provides good usability with less user interfere on circuit partitions. However, you can use the `sim_opt_one_part` and `sim_opt_analog` options to fine-tune it for better accuracy/performance trade-off.

- `sim_opt_one_part=2 subckt=[subckt_name*]`

Specifies the name of the subcircuit to be partitioned. It is recommended to set this option locally for sensitive blocks. Wildcard can be used with the parameter `subckt`. Possible values are:

- ❑ 0: Uses the arbitrary partition algorithm to perform circuit partitioning. This is the default value.

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- ❑ 1: Treats the subcircuit as one partition. This is a conservative setting and is recommended for subcircuits with less than 100 MOSFETs.
- ❑ 2: Performs channel connect partitioning inside the subcircuit. The subcircuit may contain several hundreds of MOSFETs.

■ `sim_opt_analog=6 | 7 subckt=[subckt_name*]`

The `sim_opt_analog` option with possible values of 6 and 7 can be set on analog blocks to obtain high accuracy. The subcircuits with this option are forced to create a dynamic group during the whole transient.

- ❑ `sim_opt_analog=6` can be set on bias, charge pumps, regular blocks, or other sensitive analog blocks (500-10k devices) to obtain good accuracy. For example:

```
.options sim_opt_analog=6 subckt=[myCP myReg]
.options sim_opt_analog=6 inst=[xiCP xiReg]
```

- ❑ `sim_opt_analog=7` is more conservative than value 6 and improves Spectre XPS accuracy further. However, it is targeted at smaller blocks to minimize the impact on performance. For example:

```
.options sim_opt_analog=7 subckt=[myCP myReg]
.options sim_opt_analog=7 inst=[xiCP xiReg]
```

■ `sim_opt_circuit_detect`

The `sim_opt_circuit_detect=1` option enables Spectre XPS to detect sense amplifier and place it in one partition to obtain high accuracy. The default value is 0. For example:

```
.options sim_opt_circuit_detect=1
```

■ `sim_opt_analog_rc_part_merge`

By default, Spectre XPS places the RC network from other devices in a separate partition. You can use the `sim_opt_analog_rc_part_merge=1` option to enable Spectre XPS to place RC and other devices in the same partition to obtain high accuracy. The default value is 0.

```
.options sim_opt_analog_rc_part_merge=1
```

Options Related to RC

For postlayout simulation, RC reduction is one of the fundamental technology. Spectre XPS optimizes RC reduction based on the circuit type. It provides two high-level options, `sim_opt_rcr_sram` and `sim_opt_rcr_dram`, for SRAM and DRAM designs.

■ `sim_opt_rcr_sram="NULL"`

Flag to set a group of RC reduction options for SRAM simulation. The greater the value the more aggressive is RC reduction. You can set the following values with the `sim_opt_rcr_sram` option:

- ❑ `NULL`: The RC Reduction algorithm is enabled only for a SRAM application by specifying `+cktpreset=sram` at the command line. For the other applications, the value of this option is `NULL`, which means RC reduction is not enabled for SRAM.
- ❑ `1`: Performs conservative RC reduction for SRAM simulation at advanced technology nodes (below 10nm) and with smaller design margin, especially for designs with RC on power net. This value is set while using `speed=1` for SRAM simulation
- ❑ `2`: Performs moderate RC reduction for SRAM general timing simulation. This value is set while using `speed=2` for SRAM simulation.
- ❑ `3`: Performs liberal RC reduction for SRAM simulation with loose timing accuracy requirement, like function verification. This value is set while using `speed=5` for SRAM simulation.

■ `sim_opt_rcr_dram="NULL"`

Flag to set a group of RC reduction options for DRAM simulation. The greater the value the more aggressive is RC reduction. You can set the following values with the `sim_opt_rcr_sram` option:

- ❑ `NULL`: The RC Reduction algorithm is enabled only for a DRAM application by specifying `+cktpreset=dram` at the command line. For the other applications, the value of this option is `NULL`, which means RC reduction is not enabled for DRAM.
- ❑ `1`: Performs conservative RC reduction for DRAM simulation for better timing accuracy. This value is set while using `speed=1` for DRAM simulation.
- ❑ `2`: Performs moderate RC reduction for DRAM general timing simulation. This value is set while using `speed=2` for DRAM simulation.
- ❑ `3`: Performs liberal RC reduction for DRAM simulation with loose timing accuracy requirement, like function verification. This value is set while using `speed=5` for DRAM simulation.

The following are some other RC-related options to control SRAM and DRAM simulation runs:

Option	Type	Description
<code>sim_opt_fcpl</code>	Local	Splits the coupling caps smaller than the specified value to ground. The default value is $1e-17$ for XPS SRAM <code>speed=2</code> and $1e-16$ for XPS DRAM <code>speed=2</code> .
<code>sim_opt_rmin</code>	Local	Shorts the resistors with value less than the specified value. The default value is 0.01 for SRAM, 0.1 for DRAM, and 1 for others.
<code>sim_opt_rmax</code>	Local	Discards the resistors if the resistance is greater than the specified value. The default value is $1E+07$ for SRAM and $9.9E+08$ for DRAM.

Options Related to Models

For MOSFETs in postlayout simulation, a model is with Layout Dependent Effect (LDE). As a result, its instance parameters or model parameters may have unique values for each MOSFET instance. Spectre XPS uses two levels of table model to enable sharing between MOSFET instances with good accuracy:

- *Reference table model* – A fully dense model that is accurate. Spectre XPS models all the required model effects in it.
- *Ratio table* – While building the model with mini-SPICE solver, Spectre XPS checks its coefficient with the reference table. If the accuracy meets the pre-defined criteria, this MOSFET instance is referred to the reference table, and a ratio table is built to model the mismatch. Ratio table is a sparse table and its size is much smaller than the reference table.

You can use the `sim_opt_model` option to control the accuracy of the table. This option accepts the following four possible values. The greater the value the more conservative is the table model.

- ❑ 1: This is the default value. It uses the default table model for the generation of reference table and ratio table.
- ❑ 2: Uses a tighter criteria to perform sharing using the ratio table by adding more checks on current and charge.

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- ❑ 3: Disables the ratio table. You may set it for pre-layout cases because there is no Layout Dependent Effect. For postlayout cases it increases the memory.
- ❑ 4: Uses the equation model instead of the table model. It affects both performance and memory consumption. Set this option locally and use it for debugging purposes only.

Note: The conservative table model increases memory consumption because denser tables need to be saved. Therefore, it is recommended to use a greater value locally.

The following are some other model-related options that you can use:

Option	Type	Description
<code>sim_opt_bmodel</code>	Local	Specifies which blocks are behavioral blocks (containing bsources, Verilog-A, and so on) so that Spectre XPS can use specialized algorithms at these blocks to improve convergence. For example: <code>sim_opt_bmodel=1</code> <code>subckt=[flash_cell]</code>
<code>sim_opt_tbl_vdd</code>	Local	Specifies the typical voltage scope of the table model building in the circuit. For example, <code>sim_opt_tbl_vdd=1.5</code> .
<code>sim_opt_vpp</code>	Local	Specifies the extended voltage scope of the table model building. It should be set to a possible high voltage of the circuit. For example, <code>sim_opt_vpp=5</code> .

Option	Type	Description
<code>sim_opt_avg_cap</code>	Local	Defines the MOSFET core device capacitance model. A linear model can provide significant performance improvement over a nonlinear model. Since this option may introduce accuracy loss, especially for timing, it is recommended to use it only for designs that are not sensitive to nonlinear device capacitances. Possible values are: 0: Do not use average capacitance. This is the default value. 1: Enable the linear model for MOSFET device capacitance. 4: Enable the linear model with conditions. Devices with big width or length are excluded, but still use nonlinear device capacitances.

Option Related to SRAM Bitcell

To speed up SRAM simulation, especially for function verification, you can use the `detect_memcell` option to detect the bitcell for better performance. The `detect_memcell` option accepts the following two values:

- 0: Disables bitcell detection. This is the default in XPS, except SRAM function verification mode specified using `+xps +cktpreset=sram +speed=x6`.
- 1: Enables bitcell detection. It speeds up SRAM simulation; however, it may cause some timing accuracy loss. Therefore, it is recommended to use this option for SRAM function verification.

Note: Multithreading does not work if you specify `detect_memcell=1`.

Options to Control Error Tolerance

You can use the following options to control error tolerance:

Option	Type	Description
<code>sim_opt_step_ratio</code>	Local	If set to a positive value, it scales the error tolerance in XPS FastSPICE mode. The greater the value, the more aggressive is the scaling. It is recommended to set the option between 0.5 and 2 for XPS DRAM and XPS SRAM <code>speed=2</code> setting. The default value is 1, which means that the option has no effect.
<code>sim_opt_time_unit</code>	Local	Specifies the minimum time steps for Spectre XPS transient simulation. The default value is 1 ps.

Option to Report DC Non-Convergence

You can use the `sim_opt_dump_dc_report` option, with possible values of 0 (default) and 1, to print the DC non-convergence information. `sim_opt_dump_dc_report=1` prints detailed DC non-convergence information to a report file, `<netlist>.dcrpt`.

The criteria to write DC non-convergence is based on the sum of node currents. Based on Kirchhoff's Current Law (KCL), this current should be zero. If Spectre XPS DC does not converge fully for these nodes, their sum current is not zero. Spectre XPS reports the nodes with current larger than 0.1 μ A with the number of events (like time steps) in DC.

The following is an example of the `<netlist>.dcrpt` report with the lines sorted by node current value.

Node	Voltage	Current	#event	Node not converged
x1.net1	1.1	5e-6	18	x1.net1
x1.net2	0.5	1e-7	22	x1.net2
...				

Options to Control Waveform and Output

You can use the following global options to control the waveform and output:

Option	Type	Description
<code>sim_opt_compress_output</code>	Global	If set to 1, compresses the waveform file by eliminating the points close to a straight line. If set to 0, keeps all data points.
<code>sim_opt_compress_abstolv</code>	Global	Specifies the voltage tolerance for waveform compression. The default value is 0.001. Note: This option must be used with <code>sim_opt_compress_output=1</code> .
<code>sim_opt_compress_abstoli</code>	Global	Specifies the current tolerance for waveform compression. The default value is 1e-8. Note: This option must be used with <code>sim_opt_compress_output=1</code> .
<code>sim_opt_compress_reltolv</code>	Global	Specifies the relative voltage tolerance for waveform compression. The default value is 0. Note: This option must be used with <code>sim_opt_compress_output=1</code> .
<code>sim_opt_compress_reltoli</code>	Global	Specifies the relative current tolerance for waveform compression. The default value is 0. Note: This option must be used with <code>sim_opt_compress_output=1</code> .
<code>sim_opt_cur_wf</code>	Global	If set to 1, outputs the current probes to a separate waveform file. The default value is 0.

Post-layout simulation

Postlayout simulation with parasitic effects is essential for verification of memory designs like SRAM and DRAM, especially for timing accuracy. Like most of the postlayout simulations, two major effects need to be considered:

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- The parasitic elements, especially resistors and capacitors. Effective RC Reduction algorithm of Spectre XPS, empowered by the port merge technology, improves the run time significantly while maintaining good accuracy.
- The Layout Dependent Effect (LDE) for transistors introduces challenges for the table model in FastSPICE technology since each transistor may have unique model parameters.

Spectre XPS effectively addresses the challenges of advanced process nodes. Postlayout simulation is one of them. For more information, refer to [Chapter 17, “Postlayout Simulation,”](#).

Spectre XPS SRAM Simulation

For SRAM simulation, Spectre XPS supports a high performance/capacity FastSPICE mode (+xps) and a high accuracy SPICE mode (+xps=s). Each of these modes can be further optimized for timing simulation (+cktpreset=sram) and power simulation (+cktpreset=sram_pwr). In addition, there is a speed option (+speed) that can be used to trade-off accuracy and performance; speed=1 is the most accurate while speed=5 is the fastest.

The following table summarizes all available settings where ✓ indicates the availability of a particular setting:

Speed (+speed=#)	Spectre XPS FastSpice (+xps)		Spectre XPS Spice (+xps=s)	
	Timing (+cktpreset=sram)	Power (+cktpreset=sram_pwr)	Timing (+cktpreset=sram)	Power (+cktpreset=sram_pwr)
1	✓		Obsolete	Obsolete
2	✓	✓	Obsolete	Obsolete
3			Default	Default
4			Obsolete	Obsolete
5	Default	Default	Obsolete	Obsolete

The Spectre XPS use model has been updated for SRAM timing simulation. The updated use model combines the high performance/capacity and high accuracy modes. You can now use the +speed=x# option to control accuracy/performance. Legacy modes are also supported.

For example, to run a high-precision SRAM timing simulation, you can use the following command:

```
spectre +xps +cktpreset=sram +speed=x2...
```

To relax the accuracy criteria and obtain high performance, use the following command:

```
spectre +xps +cktpreset=sram +speed=x4...
```

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The following table summarizes all the available speeds and their corresponding legacy modes:

+speed	Legacy Mode	Suggested Application
x1	Open slot	NA
x2	+xps=s +speed=3 With optimized RCR options	Very high-precision timing simulation
x3	Open slot	NA
x4	+xps +speed=1	Optimized timing accuracy, especially for <=10nm process node with IR-drop of power net impact to timing
x5	+xps +speed=2	High-performance timing simulation
x6 (default)	+xps +speed=5	Function verification

When using a SPICE runset, add the `+spice` option to ensure that the netlist convention and device models are consistently interpreted as traditional SPICE, instead of Spectre.

Since most Spectre XPS applications are large postlayout designs, use the `-64` command-line option to enable the 64-bit version of Spectre.

The high accuracy SPICE mode (`+speed=x2`) supports multithreading computation on multi-core platforms. Multithreading is enabled by default in Spectre XPS SPICE mode and the default number of threads used is 8. The maximum number of threads allowed is 64. You can turn off multithreading by using the following command:

```
spectre +xps +cktpreset=sram +speed=x2 -mt ....
```

Note: Like Spectre APS, there is no need to specify `+mt` at the command line for Spectre XPS SPICE mode. However, if you want to manually specify the number of threads to be used, instead of the default maximum threads, you can use the `+mt` command-line option, as follows:

```
spectre +xps=s +mt=4....
```

XPS SRAM Timing Simulation

When simulation speed is the primary concern, the default (`speed=x6`) FastSPICE mode (`+xps`) can be invoked in an SRAM simulation, as shown below.

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```
spectre +xps +cktpreset=sram input.scs ...
```

The accuracy of the FastSPICE mode can be increased by using the `speed` option, as shown below.

```
spectre +xps +speed=x5|x4 +cktpreset=sram input.scs ... //(new use model)
spectre +xps +speed=2|1 +cktpreset=sram input.scs ... //(legacy use model)
```

To further increase the timing simulation accuracy, particularly for critical cut SRAM simulation, or small-medium sized full macro SRAM simulation, the SPICE mode (`speed=x2`) can be used, as follows:

```
spectre +xps +cktpreset=sram +speed=x2 input.scs ... //(new use model)
spectre +xps=s +cktpreset=sram input.scs ... //(legacy use model)
```

XPS SRAM Power Simulation

The SRAM timing simulation settings can be used in both timing and power simulation; however, a power simulation mode is available that further optimizes power and current accuracy and simulation performance.

To invoke power optimization in the FastSPICE simulation mode, use the following command:

```
spectre +xps +cktpreset=sram_pwr +speed=2 input.scs ...
```

This mode targets better performance with less physical memory consumption, and still maintains good accuracy for average current.

A more accurate mode is often used in power and current simulation if the peak current is also critical. The recommended setting is the same as accurate mode for timing simulation as follows:

```
spectre +xps +cktpreset=sram +speed=x2 input.scs ... //(only in the new use model)
```

XPS SRAM Postlayout Simulation

Spectre XPS is optimized to handle large postlayout SRAM designs. It directly simulates a flat DSPF/DPF/SPEF postlayout netlist by including the file that is commonly used in SRAM designs, as shown below.

Spectre format:

```
include "file.spf"
```

SPICE format:

```
.include "file.spf" (SPICE syntax)
```

Due to the tight timing requirement for SRAM memory, backannotation postlayout simulation flow is not supported in SRAM.

XPS SRAM Leakage Current Simulation

Leakage current and power are measured in various standby and power-down modes. Traditionally, these simulations require a careful selection of measurement time points, where the circuit signals have to settle down to a steady state. Spectre XPS accelerates the leakage current and power simulation by deploying a new methodology that requires you to only provide the time point where all input signals are at their steady state. For SRAM designs, the algorithm for leakage simulation has been enhanced, especially for power-off modes, including retention, array shutdown, and total shutdown.

To enable the leakage current and power simulation in Spectre XPS in multiple power mode, use the following options:

Spectre format:

```
opt1 options leaki_times=[4u 10u] //(defines input-steady state time points in
                                   multiple power mode)
save v1:p vdd:p //(current probes on power supplies)
```

SPICE format:

```
.options leaki_times=[4u 10u] //(defines input-steady state time points in
                                multiple power mode)
.probe tran i(v1) i(vdd) //(current probes on power supplies)
```

Following is an example of the command-line option to run the leakage simulation using SPICE runset:

```
spectre -64 +xps +cktpreset=sram_pwr +spice input.sp...
```

As a result of the above settings, Spectre XPS performs a transient simulation till 4 μ s. It also performs a leakage analysis with the circuit biased at the 4 μ s condition to calculate the leakage currents `i(v1)` and `i(vdd)`. Spectre XPS then continues transient simulation till 10 μ s and performs another leakage analysis with the circuit biased at the 10 μ s condition. The result of the leakage current simulation is reported in a file with the extension `leaki`, as shown below.

```
i(v1): t= 4.0000e-06   val= -2.1293e-10
i(vdd): t= 4.0000e-06   val= -3.1166e-09
i(v1): t= 1.0000e-05   val= -4.3421e-10
i(vdd): t= 1.0000e-05   val= -6.9654e-09
```

To enable the leakage current and power simulation in single power mode, use the following options:

Spectre format:

```
opt1 options sim_opt_auto_leaki=1 //(defines input-steady state time points in
                                     single power mode)
save v1:p vdd:p //(current probes on power supplies)
```

SPICE format:

```
.options sim_opt_auto_leaki=1 //(defines input-steady state time points in
                                     single power mode)

.probe tran i(v1) i(vdd) //(current probes on power supplies)
```

Handling SRAM Designs at Advanced Technology Nodes

With shrinking process nodes, such as 7nm, there are several challenges for FastSPICE simulators to meet the tighter accuracy requirements of SRAM designs. The XPS SRAM *speed=1* setting has been enhanced to handle the following challenges from the advanced process nodes, and provides the required timing accuracy:

- The IR drop caused by resistors and capacitors on a power net or a virtual power net (VPN) can significantly impact the timing accuracy. IR drop of several millivolts may result in 10+ps timing discrepancy of SRAM designs. You can use the XPS SRAM *speed=1* setting to simulate the IR drop accurately to meet the final timing accuracy. To reduce the performance overhead, it is recommended to use RC reduction while extracting the RCs on power net or VPN nodes.
- The voltage of power supply for advance process nodes may decrease under 500mV. You can use the XPS SRAM *speed=1* setting to provide good accuracy for most of the situations. For best accuracy results, set the option `sim_opt_step_ratio` option to a value between 0.5 to 1 (the smaller the value, the more conservative is the result).
- Due to the smaller size, the coupling effect is even stronger. This means that the number of coupling capacitors is greatly increased for the advanced process nodes. For better accuracy for coupling effect, set the option `sim_opt_fcap1` to $1e-18$ (the default value is $1e-17$ for XPS SRAM *speed=1* setting).
- For RC on signal net, such as bit line, word line, and sense amplifier, you can use the XPS SRAM *speed=1* setting for better timing and tighter accuracy requirements.

Spectre XPS DRAM Simulation

With advancing process technology nodes and high capacity of DRAM chips (including PCRAM), designers are facing increasing challenges to simulate and validate large full-chip DRAM designs with the extracted parasitic elements. The simulation accuracy requirement is tighter due to shrinking design margin.

Spectre XPS provides the following advantages for DRAM applications:

- Competitive performance empowered by multithreading support — The fundamental FastSPICE technology of Spectre XPS, including arbitrary partition, dynamic group, table model, and effective multirate, can work well for DRAM postlayout simulation.
- Accurate results for timing, voltage, and current signals — As the new generation FastSPICE simulator, Spectre XPS has been optimized to meet the accuracy challenges introduced by advanced process nodes and lower voltage supplies. Both areas that are critical for accuracy are handled effectively in Spectre XPS: RC reduction empowered by port merge for parasitic RC and the core solver with partition enabled.
- Simple and consistent use model — Spectre XPS provides a consistent use model for DRAM applications. A more conservative mode, `+speed=1`, is provided for better accuracy with acceptable performance degradation; normally less than 2X.
- Better handling of large DRAM designs — Spectre XPS reduces memory consumption, and therefore, it is suitable for big DRAM designs.

Spectre XPS DRAM Postlayout Simulation

Postlayout simulation with parasitic effects is essential for DRAM verification, especially for timing accuracy. Like most of the postlayout simulation scenarios, the following two major effects should be considered:

- Parasitic elements, especially resistors and capacitors. Effective RC Reduction algorithm of Spectre XPS, empowered by the port merge technology, greatly improves the run time while maintaining good accuracy.
- The Layout Dependent Effect (LDE) for transistors introduces the challenge for the table model of FastSPICE technology since each transistor may have unique model parameters.

Spectre XPS is optimized to address the challenges introduced by the advanced process nodes. Postlayout simulation is one of them.

For more information on the Postlayout simulation flow, refer to [Chapter 17, “Postlayout Simulation,”](#).

Starting an XPS DRAM Simulation Run

The Spectre XPS DRAM simulation can be run using the following command:

```
spectre -64 +xps +cktpreset=dram +speed=2 +mt=8 top.sp....  
spectre -64 +xps +cktpreset=pcram +mt=8 top.sp...
```

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Alternatively, you can specify the `+cktpreset` and `+speed` options in the netlist, as shown below.

```
.options cktpreset=dram#1|2|5
.options cktpreset=pcram
```

When the simulation is run, the following message in the Spectre XPS log file indicates that DRAM mode with multithreading capability is successfully enabled:

```
Notice from spectre during initial setup.
  XPS Enabled ( cktpreset=dram ).
.....
  Multithreading Enabled: 8 threads in the system with 20 available processors.
```

The Spectre XPS DRAM mode supports multithreading computation on multicore platforms. Multithreading is enabled by using the `+mt` option at the command line.

Overall Accuracy/Performance Tuning Strategy in Spectre XPS

Spectre XPS provides an application-based solution by using the `+cktpreset` command-line option. For example, to run a DRAM simulation, specify the `+cktpreset=dram` command-line option. The accuracy and performance can be optimized using the `+speed` option, which includes error tolerance definition for the simulator. For tuning error tolerance, it is important to first understand the accuracy requirement, and then choose the different values for the `+speed` option. Spectre XPS provides a complete set of simulation modes or high-level `+speed` settings that you specify at the command line to meet different requirements. These models are listed below in the order of increased accuracy.

Simulation Mode	Target Application	Spectre Command-Line Options	Note
Spectre XPS (speed=5)	Functional Verification	+xps +cktpreset=dram +speed=5	Optimized for performance
Spectre XPS (speed=2)	General timing and power simulation	+xps +cktpreset=dram	Can be used for general simulation
Spectre XPS DRAM (speed=1)	Better accuracy for timing and power simulation	+xps +cktpreset=dram +speed=1	Provides better accuracy than the default mode with reasonable slow down

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Simulation Mode	Target Application	Spectre Command-Line Options	Note
Spectre XPS SPICE model for DRAM	SPICE-level accuracy	+xps=s +cktpreset=dram	Uses the SPICE engine, but with optimization for RC in postlayout and provides better default trade-off accuracy/performance for DRAM applications. It targets the same accuracy level as the SPICE simulator, but with better performance and accuracy.
Spectre APS simulator	Golden accuracy	+aps	By default, no simplification or RC reduction is performed. Use this option as accuracy reference, if the simulation can be finished within reasonable time.

You can use the following high-level options for different simulation modes:

Modes	XPS SPICE mode	XPS DRAM speed=1	XPS DRAM speed=2 (default)	XPS DRAM speed=5
Solver	SPICE	FastSPICE	FastSPICE	FastSPICE
sim_opt_model	4	2	1	1
sim_opt_step_ratio	NA	0.5	1	2
sim_opt_rcr_dram	NA	1	2	5
sim_opt_fcpl	NA	1e-18	1e-16	1e-16

High Accuracy Mode

One of the targets of Spectre XPS, including the DRAM application, is to simplify the use model by reducing the tuning effort on a case-by-case basis. However, to maintain the flexibility of better accuracy/performance trade-off, you can use any of the following methods for a DRAM application:

- Specify `+speed=1` at the Spectre command line, as shown below.
`spectre -64 +xps +cktpreset=dram +speed=1 +spice ...`
- Specify the `cktpreset` and `speed` options in the netlist file, as shown below.

Spectre format:

```
Opt options cktpreset=dram#1
```

SPICE format:

```
.options cktpreset=dram#1
```

Note: Command-line options override the options specified in the netlist.

The above methods improve Spectre XPS accuracy by providing:

- Tighter error tolerance, especially for the lower voltage of power supply.
- Tighter time step control.
- Reduced threshold for coupling capacitor by splitting it from $1e-17$ F to $1e-18$ F. This threshold is defined using the `sim_opt_fcap1` option.
- Better accuracy for table model; however, it may increase memory consumption.

Function Verification Mode

The default speed option is `+speed=2` for Spectre XPS DRAM application. It can be applied to general timing and power simulation. For function verification, the timing accuracy requirement may be relaxed using a reasonable range; however, you still need to keep the correct function. Spectre XPS provides the following two methods to define the function verification mode for DRAM simulation:

- Specify `+speed=5` at the Spectre command line, as shown below.
`spectre -64 +xps +cktpreset=dram +speed=5 +spice ...`
- Specify the `cktpreset` and `speed` options in the netlist file, as shown below.

Spectre format:

```
Opt options cktpreset=dram#5
```

SPICE format:

```
.options cktpreset=dram#5
```

Note: Command-line options override the options specified in the netlist.

Accuracy for Analog Block in DRAM Simulation

In DRAM applications, most of the elements are from the DRAM bank or the peripheral logic blocks. However, there may still be some sensitive analog blocks inside it. You can set the `sim_opt_one_part` and `sim_opt_analog` options locally on such analog blocks to obtain high accuracy. It is recommended to set these options on small blocks to minimize the performance impact.

See [Options Related to Circuit Partitioning](#) on page 87 for information on these options.

Examples of local options for analog blocks in DRAM simulation

- `.option sim_opt_analog=7 subckt=[comparator SA]`
Use `sim_opt_analog=7` on comparator and sense amplifier for better accuracy, if required.
- `.option sim_opt_analog=7 subckt=[bandgap chg_pump]`
Use `sim_opt_analog=7` on bandgap and charge pump for better accuracy.
- `.option sim_opt_one_part=1 subckt=[vco delay_cell]`
Use `sim_opt_one_part=1` on oscillator or delay block for SPICE-like timing.
- `.option sim_opt_circuit_detection=1`
There is no need to set the local scope.
- `.option sim_opt_analog_rc_part_merge=1`
There is no need to set the local scope.

Spectre XPS Flash Simulation

Spectre XPS has been designed to significantly reduce the simulation time of flash memory designs. In addition, the target is to complete a fully extracted postlayout simulation on full chip design within acceptable accuracy degradation.

For flash simulation, Spectre XPS supports a high performance/capacity FastSPICE mode (+xps), and an accurate SPICE mode for small blocks in a flash design. The +speed command-line option that is used in SRAM application is not supported for flash designs.

Adjusting Speed and Accuracy of Spectre XPS Flash Memory Simulation

You can use two global options, `sim_opt_acc` and `sim_opt_analog`, to adjust the speed and accuracy settings of a Spectre XPS flash memory simulation.

The `sim_opt_acc` option with possible values of 2, 4, and 8 can be used to get better speed and accuracy.

- `sim_opt_acc=2` can be set on larger logic blocks (>10k devices) to get better performance.
- `sim_opt_acc=4` can be set to get accurate power simulation or postlayout backannotation run.
- `sim_opt_acc=8` can be set on smaller blocks (<500 devices) to get better timing accuracy.

The `sim_opt_analog` option with possible values of 6 and 7 can be set on pump/regulator blocks to obtain high accuracy.

- `sim_opt_analog=6` can be set on charge pumps, regular blocks, or other sensitive analog blocks (500-10k devices) to obtain good accuracy. For example:

```
.options sim_opt_analog=6 subckt=[myCP myReg]
.options sim_opt_analog=6 inst=[xiCP xiReg]
```

- `sim_opt_analog=7` is more conservative than value 6 and improves Spectre XPS accuracy further. However, it is targeted at smaller blocks to minimize the impact on performance. For example:

```
.options sim_opt_analog=7 subckt=[myCP myReg]
.options sim_opt_analog=7 inst=[xiCP xiReg]
```

Starting a Spectre XPS Flash Memory Simulation

You can invoke Spectre XPS flash simulation in FastSPICE mode, as shown below.

```
spectre +xps +cktpreset=flash input.scs ...
```

For small block-level designs that require high accuracy tolerance, the default SPICE mode can be used.

```
spectre +xps=s +cktpreset=flash input.scs ...
```

Note: The SPICE mode is not recommended for medium-to-large blocks in a flash design.

When using a SPICE runset, add the `+spice` option to ensure that netlist convention and device models are interpreted in a consistent manner as traditional SPICE, instead of Spectre. For large mixed-signal applications, it is recommended to use the 64-bit version of the tool with the `-64` command-line option.

A configuration file may be used (`+config file.cfg`) to obtain optimized simulation results. All control options can be specified either in netlist file `input.scs` or the configuration file.

Flash Memory Postlayout Simulation

Spectre XPS is optimized to handle large postlayout flash memory designs. It annotates the DSPF/DPF/SPEF file back to the pre-layout netlist through parasitic backannotation options, as shown below.

Spectre format:

```
Opt1 options spf="scope filename"  
Opt2 options dpf="scope filename"  
Opt3 options spef="scope filename"
```

SPICE format:

```
.options spf="scope filename"  
.options dpf="scope filename"  
.options spef="scope filename"
```

Here, `scope` can be a subcircuit or an instance.

The Spectre XPS parasitic backannotation flow shares the same methodology and controls as Spectre APS. For more information on the parasitic backannotation related control options, such as `spfscale`, `spfxtorprefix`, and `spfaliasterm`, refer to [Chapter 17, “Postlayout Simulation.”](#)

The Spectre X Circuit Simulator

Recent technology developments, advanced node adoption, and more than Moore designs have forced analog and custom IC designers to adopt new design practices to benefit from these advancements. These changes have resulted in the need to simulate larger designs with more postlayout parasitics. In addition, many custom IC designs, such as flash memory, MRAM, and sensor arrays now require SPICE-accurate simulations. To meet these demands, a new SPICE engine with much more performance and capacity than the current generation of circuit simulators is needed. Spectre[®] X is the next generation of the Spectre circuit simulator that addresses the need for a simulator capable of simulating the next generation of analog, mixed-signal, and custom IC designs.

Spectre X includes two major technologies:

- Enhanced simulation performance and capacity with a simple `+preset` use model
- Highly scalable multi-core simulation with `+mt`, and distributed multi-process simulation with `+xdp`

This chapter discusses the following topics:

- [License Requirements for Spectre X](#)
- [Using the Spectre X `+preset` Option](#)
- [Migrating from Spectre APS](#)
- [Using the Spectre X `+xdp` Option](#)
- [Using GPU with Spectre X](#)

License Requirements for Spectre X

The number of MMSIM token checked out depends on the number of CPU cores, as described below.

- Single core: 3 MMSIM tokens
- 2 – 4 cores: 6 MMSIM tokens
- 5 – 16 cores: 9 MMSIM tokens
- 17 – 64 cores: 12 MMSIM tokens
- 65 – 128 cores: 15 MMSIM tokens
- 129 – 256 cores: 18 MMSIM tokens
- 257 – 512 cores: 21 MMSIM tokens

Using the Spectre X +preset Option

Spectre X provides five high-level `+preset` options (`cx`, `ax`, `mx`, `lx`, `vx`) that allow you to trade off accuracy and performance. These high-level options not only control solver settings, but also enable parasitic optimization after automatically detecting postlayout designs. The `cx` mode provides the highest accuracy, while the `vx` mode provides the highest performance.

Spectre X ignores the Spectre APS command-line options `+aps`, `++aps`, `+postlayout`, `+errpreset`.

To start a Spectre X simulation, type the following at the command line:

```
% spectre +preset=mx input.scs
```

The following provides guidance on the `+preset` selection options:

Option Name	When to Use...

<code>cx</code>	when a golden simulation reference is needed
<code>ax</code>	for high-precision analog applications
<code>mx</code>	for most analog applications (default)
<code>lx</code>	for power management and other relaxed analog applications
<code>vx</code>	for custom IC verification

Spectre X `+preset` uses the same multi-core simulation approach and use model as Spectre APS. By default, 8 cores are used.

```
% spectre +preset=mx input.scs +mt=4
```

While postlayout optimization enabled by the `+preset` settings is sufficient in most cases, there may be designs that require you to adjust, or disable postlayout optimization. You can do this by using the `+postlpreset` command-line option, which accepts the following values: `off`, `cx`, `ax`, `mx`, `lx`, and `vx`. The `+postlpreset` command-line option can also be used to enforce postlayout optimization in case Spectre X does not detect the postlayout nature of a design.

```
% spectre +preset=mx +postlpreset=cx input.scs
```

By default, Spectre X ignores the user-specified simulation options that trade off performance and accuracy.

■ Transient options: `method`, `relref`, `lteratio`, `maxiters`, `maxstep`

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■ Netlist options: `reltol`, `residualtol`, `vabstol`, `iabstol`, `preserve_inst`

However, you can use the `-preset_override` command-line option to tell Spectre X to honor the user-specified simulation options, as shown below.

```
% spectre +preset=mx -preset_override input.scs
```

You can also specify the simulation options as a list, separated by a comma, with the `-preset_override` command-line option to tell Spectre X to selectively honor only those options and ignore the others, as shown below.

```
% spectre +preset=mx -preset_override=reltol,method input.scs
```

Dynamically Changing Parameters in Spectre X

You can use `steppreset`, a high-level solver parameter, to dynamically changed the Spectre X parameters. Possible values for this `steppreset` are `cx`, `ax`, `mx`, `lx` and `vx`.

The following solver options are adjusted with the `steppreset` change:

steppreset	dis_It e_rela x	fast out	trapve rsion	reltol	errpreset	method	relref	maxit ers	vrefbins	Iteration
CX	yes	yes	0	1.00E-04	conservative	gear2only	sigglobal	5	[1 3 5 10]	10
AX	yes	yes	0	1.00E-03	moderate	trap	sigglobal	5	[1 3 5 10]	3.5
MX	no	yes	0	1.00E-03	moderate	trap	allglobal	5	[1 3 5 10]	3.5
LX	yes	no	1	1.00E-03	liberal	trap	sigglobal	10	[1 3 5 10]	3.5
VX	no	yes	0	3.50E-03	liberal	trap	sigglobal	5	[3 5 10]	1

Migrating from Spectre APS

Experienced users of the Spectre APS simulator may have established a preferred set of simulation options for their design styles. The following table provides guidance on which Spectre X mode to use when migrating from Spectre APS to Spectre X:

APS Setting	conservative*	moderate**	liberal	Custom IC Verification
Spectre X +preset	cx or ax (start with ax)	ax or mx (start with mx)	lx or vx (start with lx)	vx

* The ax preset can in general provide sufficient accuracy in conservative runs. We recommend starting with ax and only use cx if your circuits require it.

** The lx preset may provide sufficient accuracy compared to moderate runs with much better performance, for example PMIC, High Voltage designs.

Using the Spectre X +xdp Option

Spectre X distributed simulation allows more computer cores across multiple computer hosts to further speed up DC and transient run time of large to very large, mainly postlayout circuits. A circuit is considered as large when there are at least 500,000 nodes. It has equivalent convergence and accuracy as Spectre X multi-core simulation. The netlist syntax, device models, analysis setups, and output formats are fully compatible with Spectre X multi-core simulation.

Spectre X distributed simulation supports the following:

- DC, transient, HB, assert, and output

Note: The Spectre X distributed HB analysis flow requires a special license. To use this flow, contact your Cadence representative.

- alter; instance and model parameter alter including topology change is supported
- sweep; instance and model parameter alter including topology change is supported
- info (limited support); `what=inst|oppoint` is not supported
- Monte Carlo analysis
- Reliability analysis
- LSF, SGE, PBS, and `rsh` (or `ssh`) methods for job distribution. The command-line options `+preset` and `+xdp` are required to invoke the distributed mode. If any of these options is missing, simulation is not run in distributed mode.

If an analysis or feature is not supported, Spectre X ignores it with a warning.

You can use the following command to distribute a job locally using `rsh` across two hosts, `hostA` and `hostB` (with each host using 16 cores):

```
% spectre +preset=mx +mt=16 +xdp=rsh +hosts "hostA:1 hostB:1" /hm/test/input.scs
```

Note: The specified path, for example, `/hm/test/input.scs`, should be network accessible.

If you need to use `ssh` instead of `rsh`, you must specify the `ssh` argument with the `+xdp` option; however, the `+hosts` argument may remain unchanged.

```
% spectre +preset=mx +mt=16 +xdp=ssh +hosts "hostA:1 hostB:1" /hm/test/input.scs
```

In the LSF use model, it is assumed that Spectre X is started using the LSF job submission command or a user-specific wrapper. Spectre X automatically detects this and queries LSF for a list of hosts allocated to the job by LSF and the number of cores allocated on each host.

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Add the `+xdp` command-line option only without `+mt` to ensure that distributed mode is started.

In the following example, the `bsub` command is used to request a total of 32 cores, on two machines, with 16 cores on each machine. Spectre X automatically uses the allocated cores and machines supplied by LSF.

```
% bsub -n 32 -q rnd -P myProject -R "OSREL==EE70 && CPUS>=16 span[ptile=16]" spectre
+preset=mx +xdp /hm/test/input.scs
```

If you want to use SGE instead of LSF, you can use the following equivalent command:

```
% qsub -l nodes=2,ppn=1,tpu=16 -V -cwd "spectre +preset=mx +xdp /hm/test/input.scs"
```

If you want to use PBS instead of LSF, you can use the following equivalent command:

```
% qsub -l select=2:ncpus=16 -q rnd -P myProject "spectre +preset=mx +xdp /hm/test/
input.scs"
```

In the LSF use model, you can use the `+ppn` option to control the number of processes per host. In the example below, the simulation will run on a total of 32 cores using two hosts, two processes on each host, with each process using eight threads.

```
% bsub -n 32 -q rnd -P myProject -R "OSREL==EE70 && CPUS>=16 span[ptile=16]" spectre
+preset=mx +xdp +ppn=2 /hm/test/input.scs
```

It is beneficial to use `+ppn` when you are running distributed HB simulation. It is recommended to set `+ppn` to the same number of sockets of the machines being used.

Notes on Spectre X Distributed Mode

- For DC and transient, Spectre X supports a process-based output by default where both master and worker processes simultaneously write the waveform output to individual files, thereby increasing the simulation speed. Currently, the process-based output is supported only in `psf`, `psfxl`, and `sst2` formats.
- It is recommended to use identical machine configurations for all the hosts, and an equal number of cores on each host for performance testing.
- Spectre X distributed mode supports up to 512 cores and can be used to simulate designs containing millions of devices.
- When running distributed simulation with `ssh`, it is required to use password-less mode by `ssh-keygen` to generate private and public key. Copy the public key to remote hosts before starting the simulation.
- Spectre APS `+dp` is no longer supported. Use Spectre X `+xdp` instead.

Using GPU with Spectre X

Spectre X lets you use graphics processing units (GPUs) in addition to CPUs. If there are GPUs available in the setup and you have large designs that have long-running transient analyses, postlayout or advanced node simulations, you can use GPU mode of Spectre X to speed up simulations.

Spectre X with GPU supports all `+preset` levels in the same way as done without GPU and there is no accuracy change in the results. When using GPUs, better performance is expected at high accuracy modes in the following order: CX > AX > MX > LX.

GPUs work in collaboration with CPUs. A CPU manages the simulation tasks and dispatches the heavy workload to the GPUs.

License Requirements for GPU

For details on the license requirements for GPU, contact Cadence Customer Support.

Use Model

To enable GPU for Spectre X, use the `+gpu` command-line option along with the `+preset` option.

```
spectre ... +gpu
```

When one or more GPUs are available and you want to use any of the available resources, the least loaded GPU device is automatically assigned.

To use a specific GPU device, specify the name of the device in the `+gpudev` command-line option.

```
spectre ... +gpu +gpudev device-id
```

For example:

```
spectre ... +gpu +gpudev 0
```

To specify multiple specific GPUs, use a range or list of device IDs.

Examples:

```
spectre -64 +preset cx +mt 8 +gpu=2 +gpudev 0,2
```

```
spectre -64 +preset cx +mt 8 +gpu=4 +gpudev 0-3
```

Spectre FMC Analysis

As the process feature sizes have scaled down, the impact of device mismatch on circuit performance has increased and more Monte Carlo simulations are required to analyze the impact of this mismatch on performance metrics. With standard Monte Carlo algorithms, it is not feasible (high cost) to complete even the one million Monte Carlo simulations needed in memory design to determine 4 sigma yield numbers. For high-sigma yield analysis, more than one billion simulations would be required.

Spectre FMC Analysis has an advanced algorithm to accelerate the high-sigma yield estimation. It lets you extract the useful statistical information without running the full set of Monte Carlo samples, especially for high-sigma analysis.

For more details, refer to the following topics:

[Technology and Overview](#)

[Use Model and Applications](#)

[Setup to Enhance the Performance of a Fast Monte Carlo Simulation](#)

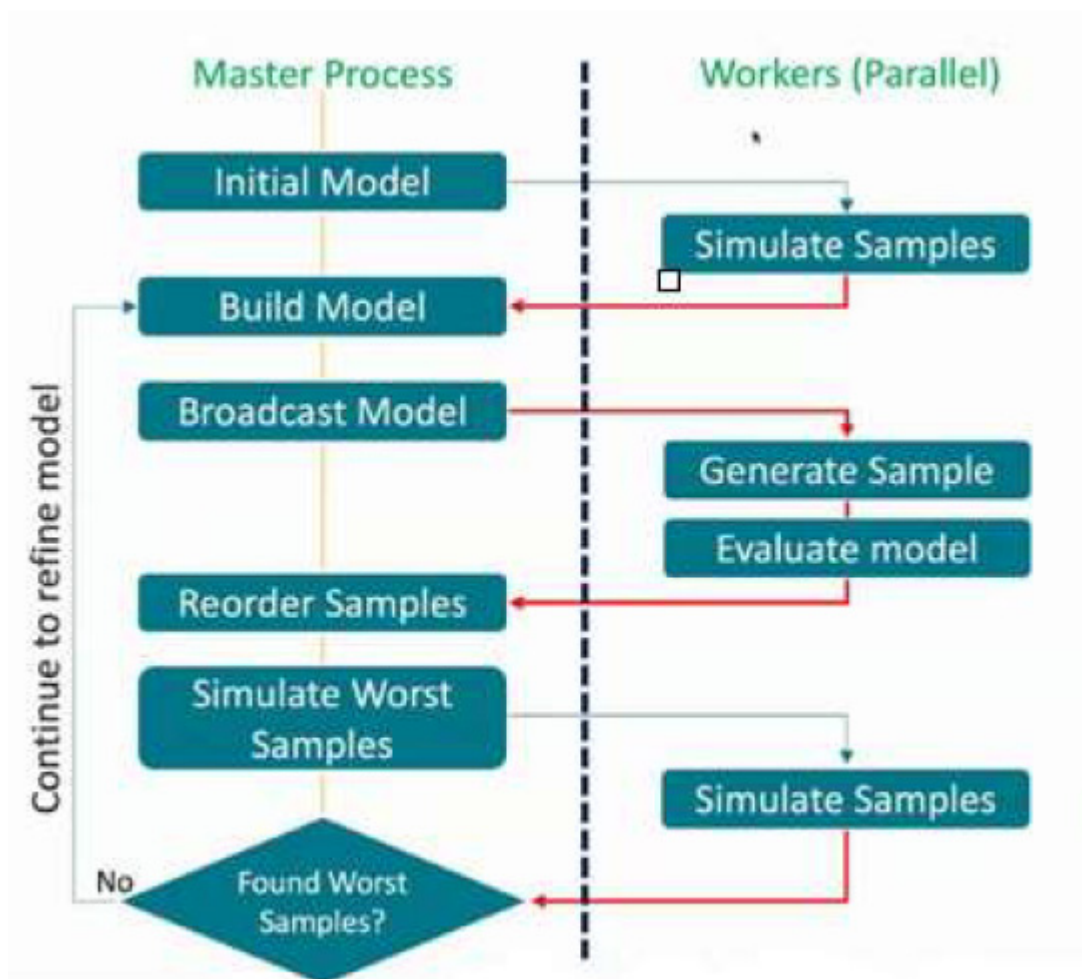
[Post-Process Fast Monte Carlo Data](#)

Technology and Overview

Fast Monte Carlo runs a group of samples initially and obtains the measurements. Then, the library with newer algorithm builds a model and predicts the worst sample based on the result and specifications set by user. It may take a few group iterations from model building, worst sampling prediction and verification to find out the tail of distribution. This Fast Monte Carlo technology improves performance greatly and reduces memory cost when compared to the normal Monte Carlo simulation.

In addition to the new approach adopted in Monte Carlo Analysis and the auto-stop enabled to shorten the simulation time, Fast Monte Carlo also supports multi-processes distribution to further speed up the performance. Sample generation, model evaluation and simulation are now processed by parallel workers.

A typical distribution flow for Fast Monte Carlo is shown below.



Use Model and Applications

In addition to the brute-force setup, the use model for Fast Monte Carlo analysis involves the following tasks:

[Setting up a Fast Monte Carlo Goal](#)

[Specifying the Fast Monte Carlo Method](#)

[Enabling Sweep Sigma Trend with Fast Monte Carlo in a Single Run](#)

[Specifying Other Parameters for Fast Monte Carlo](#)

[Enable Moments in Fast Monte Carlo](#)

Yield Estimation with Brute Force Monte Carlo

Setting up a Fast Monte Carlo Goal

From the netlist, identify a list of measurements that are used to verify the correct functional behavior of the design under test and specify those measurements as goals to drive the high-sigma analysis.

You can specify goals by using the `target` block in the `statistics` statement. Syntax of the `target` block is shown below.

The syntax for this block is as follows;

```
statistics {
  target {
    goal <measurement_name> min=<value>
    goal <measurement_name> max=<value>
    goal <measurement_name> min=<value> max =<value>
  }
}
```

You can specify either a single measurement name with a min goal, max goal or both min and max goals, or multiple measurement names with a min goal, max goal or both min and max goals.

The keyword of `max` intends to look for the worst tails on the positive sigma side of the statistics distribution while `min` is to find the negative sigma side. The values for min and max set the criteria for Spectre to count the number of #pass or #failed for each iteration. They can also be used for setting autostop conditions through parameter `fmcnumfails`.

Note: Only the measurements specified using `.MEASURE` syntax can be used as goals in Spectre command-line flow. The goal cannot be from a measurement that is defined using the MDL format or evaluated in a post-processing mode using OCEAN.

An example of a `targets` block is shown below.

```
.MEASURE tpdr
+ TRIG v(b) VAL='PWR_SUPPLY/2' FALL=1
TARG v(c) VAL='PWR_SUPPLY/2' RISE=1
.MEASURE tpdf
+ TRIG v(b) VAL='PWR_SUPPLY/2' RISE=1
TARG v(c) VAL='PWR_SUPPLY/2' FALL=1
.MEASURE tpd param='(tpdr+tpdf)/2'
Simulator lang=spectre
// Use the targets block in the statistics statement to
// define which measurements are to be analyzed with FMC

statistics {
  targets {
    goal tpd min=8p max=10p
  }
}
```

Best practices to avoid unnecessary issues that may seem like a product defect:

- If there are two or more measurements from the design that the you would like to use as a part of the high-sigma analysis, then it is better not to combine them in a single Spectre FMC run. For better accuracy and performance, it is better to do separate individual high-sigma runs for each measurement goal of interest.
- If there are two measurements where one is a timing measurement and one is voltage measurement, then it is advised not to mix these goals in a single Spectre FMC run.
- If you know that a min for the goal or a max for the goal would not make sense for a high sigma analysis, then it is advised to use either a min goal or a max goal for the specific measurement based on what is the actual criteria for a failure.

Specifying the Fast Monte Carlo Method

Use the `fmcmethod` parameter to specify the method or algorithm to be used and the outputs required for your design. FMC can use three methods, `worstsample`, `yield`, and `yieldest` to obtain the statistical result. Amongst the first two, it is recommended to use `worstsample` because it allows exploration of high-sigma tails with more useful information while `yield` is more of a pass/fail analysis.

The Worstsample Method

For `worstsample`, specify any two of the following three parameters in the Monte Carlo statement.

Parameter	Description
<code>numruns</code>	Controls the MC sample space of interest, or the total number of MC samples to be considered while trying to find the worst-case samples.
<code>fmcinitruns=50</code>	Specifies the number of runs in FMC initial group to build the model.
<code>fmcsigma</code>	Specifies a target yield in an easier form like a sigma value. Instead of specifying at target yield of 99.996832875816693 %, the user can specify it as a sigma value, <code>fmcsigma=4</code> . The maximum sigma value supported is 6 sigma.
<code>fmcnumtailsamples</code>	Controls the number of high sigma tail samples to be estimated.

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The following are examples of multiple combinations of any two parameters:

- Driving Spectre FMC by specifying the number of samples in the monte carlo sample space (numruns) and the target yield in the form of a sigma value (fmcsigma).

```
mcl montecarlo fmcmethod=worstsample numruns=1e6 fmcsigma=4.2 {  
    tran tran stop=3n  
}
```

- Driving Spectre FMC by specifying the number of samples in the monte carlo sample space (numruns) and specifying the number of worst-case tail samples (fmcnumtailsamples).

```
mcl montecarlo fmcmethod=worstsample numruns=1e6  
    fmcnumtailsamples=14 {  
    tran tran stop=3n  
}
```

- Driving Spectre FMC by only specifying the target yield in the form of a sigma value (fmcsigma) and the number of worst-case tail samples (fmcnumtailsamples) to be estimated. There is no need to specify total sampling number.

```
mcl montecarlo fmcmethod=worstsample fmcsigma=4.2  
    fmcnumtailsamples=14 {  
    tran tran step=1p stop=tran_time autostop=yes method=gear2  
}
```

The following settings are equivalent because for one million samples, the sample at 4.2 sigma is the 14th worst sample while FMC will report 14 samples and the sigma range is (4.2, 4.89) when numruns=1M fmcsigma=4.2.

```
"numruns=1M fmcsigma=4.2, or  
"fmcsigma=4.2 fmcnumtailsamples=14, or  
"numruns=1M fmcnumtailsamples=14
```

Below are examples of multiple combinations of any two parameters.

```
mcl montecarlo numruns=20000 firstrun=1 seed=12345 variations=all \  
donominal=no savefamilyplots=no \  
fmcmethod=worstsample fmcsigma=3 {  
    tran tran step=1p stop=2n  
}
```

The Yieldest Method

Spectre FMC estimates the failure rate based on the boundaries of measurement goal with much fewer sample set by fmcbudget. This feature provides the approximation result so that you can use it as a reference to set up the FMC worst sample simulation if you don't know what yield is expected for the design.

```
mcl montecarlo numruns=1e+6 fmcmethod=yieldest fmcbudget=3000 "  
  fmcconfidence=0.95 {  
    tran tran step=1p stop=tran_time autostop=yes method=gear2  
  }
```

Enabling Sweep Sigma Trend with Fast Monte Carlo in a Single Run

Use the `fmcswepsigma` parameter to `yes` to enable sweeping of variations from 3 sigma to a high sigma achieved with the number of samples in stages. It allows to get the entire trend in a single FMC run instead of running multiple simulations for 3 sigma, 4 sigma, 5 sigma and 6 sigma separately.

The following example shows how `fmcswepsigma` is specified in the `montecarlo` statement:

```
mcl montecarlo fmcmethod=worstsample numruns=1e6 fmcnumtailsamples=14  
fmcswepsigma=yes {tran tran stop=2n }
```

When running high sigma simulation is too expensive, this sigma sweeping based on lower sampling numbers can provide an idea of high sigma.

When `fmcswepsigma` is enabled, the simulation saves a file named `worst_by_stage_*.csv`. You can post-process this file with a python script `plot_sweep_sigma.py` to generate the sigma trend plots.

Related Topic

`plot_sweep_sigma`

Specifying Other Parameters for Fast Monte Carlo

The following table describes other Fast Monte Carlo parameters supported by Spectre.

Parameter	Description
<code>fmcconfidence=0.95</code>	Specifies the confidence value in the range 0.5 to 1. Default value is 0.95.
<code>fmcinitruns=50</code>	Specifies the number of runs in Fast Monte Carlo initial group required to build the model.

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<code>fmcnumfails=0</code>	Stops a certain spec during Fast Monte Carlo process when the number of failed iterations reach the value set for this parameter. By default, Fast Monte Carlo does not check failed iterations.
<code>fmcdumpcontribution=0</code>	Saves device mismatch contribution into the default Fast Monte Carlo file, <code>netlist.fmc.log</code>, in the descending order. Specify a positive value to save the number of devices for contribution. Specify a negative value to save the contribution for all devices. Specify zero to turn off the output.

Enable Moments in Fast Monte Carlo

The Fast Monte Carlo analysis is designated to identify the worst samples at both tails of distribution so that the moments are not supported by default. It can support the moments by increasing the default value of the `fmcinitruns` parameter from 50 to 1000. You can define this parameter explicitly in Monte Carlo statement to override the default number.

When the following statement is set, the moments computation for target goal distributions is enabled.

```
mcl montecarlo numruns=1e+6 firstrun=1 seed=12345 variations=all
    donominal=no savefamilyplots=no
    fmcmethod=worstsample fmcsigma=4.2 fmcmoments=yes {
        tran tran step=1p stop=tran_time autostop=yes method=gear2
    }
```

Initial group of size 1000 samples is used to compute the moments.

When simulation is done, the information about moments of 1000 samples is saved in the last section of output file of `*.fmc.log` as given below.

```
FMC moments of spec distributions:
Spec: tpd
Mean = 1.2226e-11
Variance = 1.49197e-24
Stddev = 1.22146e-12
Skewness = 0.662279
Kurtosis = 0.981272
```

Yield Estimation with Brute Force Monte Carlo

To estimate the sigma for the measurement goal with much fewer samples, you can use the `spectre_yieldest` command. This command runs the Brute Force Monte Carlo simulation.

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Syntax:

`spectre_yieldest [spectre_cmds...] [yieldest_cmds...] netlist_with_mc`

where,

`spectre_cmds` can be `+aps +mt=2`

`yieldest_cmds` can be one or more of the following:

- ❑ `-n NUMRUNS` specifies the total number of Monte Carlo iterations to predict yield estimation. Default is 3000.
- ❑ `-s SEED` specifies the seed for Monte-Carlo run (overrides netlist setting).
- ❑ `-c CONF` specifies the confidence level for confidence interval, default is 0.95 (95%).
- ❑ `-clean` does a clean rerun of Spectre even if the previous simulation result exist. By default, if `OUTDIR` exists and a previous `yieldest` output directory exists, it will reuse previous simulation results. Runs incrementally only if needed.
- ❑ `-plot` draws the estimated QQ plot for each goal.
- ❑ `-l LOGNAME` specifies the yield estimation log file name.
- ❑ `-o OUTDIR` specifies the yield estimation output directory.

`netlist_with_mc` is a regular netlist file that contains Monte Carlo analysis and statistical target (goal) definition. The netlist or configure file that contains the Monte Carlo analysis and the target goal has to be specified at the end of the command line.

Note: For consistent results between Fast Monte Carlo and Brute Force Monte Carlo, ensure that the `sampling`, `firstrun`, and `seed` parameters have the same values for both simulations. In Spectre, the default value of sampling method is `standard`. The default method in ADE is `lds`.

Setup to Enhance the Performance of a Fast Monte Carlo Simulation

The run time is truly critical when the sampling number of Monte Carlo runs a million times for a high sigma requirement. You can use the following features to enhance the performance of a Fast Monte Carlo run:

Distributing a Fast Monte Carlo Run

Parameters to Accelerate Performance

Enabling AutoStop to Save Run Time

Distributing a Fast Monte Carlo Run

The distribution process can be launched by `+mp` specified in Spectre command line. It is always recommended to enable `+mp` for Fast Monte Carlo to build up the model and predict worst samples with multiple workers to achieve the best performance speedup.

The Fast Monte Carlo analysis supports three distribution mechanisms.

- Job submission in farm with `lsf`, `sgs` or `nc`
- Using `rsh` and `ssh` on the remote systems
- Using `fork` to create multiple jobs on a single system

When using `fork` in distribution mode on a terminal of the requested farm machine, add `+mplauncher=ksh` in the command line to run all distributed processes on the same machine locally. Otherwise, Spectre launches multiple processes when it detects a farm environment.

Parameters to Accelerate Performance

You can add the following parameters in the Monte Carlo statement to accelerate the performance of a simulation:

Parameter	Description
<code>fmcmode=fast</code>	The FMC mode to control the balance between performance and accuracy. Possible values are <code>fast</code> and <code>conservative</code> .
<code>fmcmaxbufsize=1</code>	Specifies the FMC maximum buffer size. Default value is 1GB. For each process to store and process the sampling data, Spectre allocates memory of the size set by <code>fmcmaxbufsize</code> . If the assigned buffer size is less than the required size, the run time is limited due to the insufficient memory size. You can set <code>fmcmaxbufsize</code> to a larger size according to the physical memory size of the host to speed up the performance. Spectre automatically reduces the buffer size to the required size if <code>fmcmaxbufsize</code> is more than the size required.

Enabling AutoStop to Save Run Time

The target goal is defined by the `.measurement` statement. Most of time, the measurements are achieved prior to the stop time set in transient. You can stop the transient simulation once the measurements are completed to save the simulation time further.

Alternatively, enable auto-stop by setting `autostop=yes` in the transient statement.

```
tran tran step=lp stop=tran_time autostop=yes
```

Post-Process Fast Monte Carlo Data

Spectre provides the following two commands to let you post process the Monte Carlo data:

spectre_fmcverifier

plot_sweep_sigma

spectre_fmcverifier

This command lets you view the sample data distribution for the Brute Force Monte Carlo and Fast Monte Carlo, use the `spectre_fmcverifier` binary utility. It plots the QQ plot and histogram plot.

Syntax

```
spectre_fmcverifier [-h] [-mc MC] [-mcdir MCDIR] [-csvbfmc CSVBFMC]  
[-legendloc LEGENDLOC] [-worstnum WORSTNUM]  
[-fmc FMC] [-csvfmc CSVFMC] [-fmcnumruns FMCNUMRUNS] [-goal GOAL]  
[-qqplot] [-histo] [-plotsigma] [-plotall] [-switch]
```

Options

Parameter	Description
-h	Prints this help message and exits.
-mc MC	Specifies brute force montecarlo results mt0 file or MC scalar file (mcdat file).
-mcdir MCDIR	Specifies the results directory for brute force montecarlo, the binary collects all the mt0 files in the directory.
-csvbfmc CSVBFMC	Specifies brute force montecarlo results in CSV file.

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<code>-legendloc</code>	<code>LEGENDLOC</code>	Specifies the legend location. Default is UL (upper left). You can change it to LR (lower right), LL, or UR.
<code>-worstnum</code>	<code>WORSTNUM</code>	Specifies the worst #num samples to search from brute force montecarlo results mt0.
<code>-fmc</code>	<code>FMC</code>	Specifies the Spectre public logs. For example, <code>-fmc "log1 log2"</code>
<code>-csvfmc</code>	<code>CSVFMC</code>	Specifies FMC result in .csv file. You also needs to provide fmc numruns by <code>-fmcnumruns</code> , to enable the tool to plot qqplot.
<code>-fmcnumruns</code>	<code>FMCNUMRUNS</code>	Specifies FMC numruns by this parameter if want to plot qqplot by read fmc data through csv file. This number must be smaller or equal to the BFMC total numruns.
<code>-goal</code>	<code>GOAL</code>	Specifies the FMC goal(s) want to check. For example, <code>-goal "spike droop"</code>
<code>-qqplot</code>		Plots QQ-plots for FMC and BFMC. Comparison table is printed by default.
<code>-histo</code>		Plots a histogram for BFMC data.
<code>-plotsigma</code>		Plots a sigma distribution for different FMC number runs.
<code>-plotall</code>		Plots both QQ-plot and histogram.
<code>-switch</code>		Switches QQ-plot X/Y axis as sigma vs goal, instead of goal vs sigma.

plot_sweep_sigma

This python script post processes the data from FMC sigma sweeping. The output file `worst_by_stage_*.csv` is generated from FMC simulation with the goal name.

A file with `*_H` in its name contains the sigma values on maximum boundary. A file with `*_L` in its name contains the sigma values on minimum boundary.

Syntax

```
plot_sweep_sigma.py [options]
```

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Options

Parameter	Description
-h, --help	Displays this help message and exits
FILE, --file=FILE	Worst by stage file.
-l, --left	Extrapolates left tail.
-m MEASURE, --measure=MEASURE	Name of the measurement.
-q, --quiet	Specifies whether to print status messages to stdout

Examples:

```
%cdspython -64 ../bin/plot_sweep_sigma.py  
-f out_sweep_sigma_1M_mp327worst_by_stage_tpd_H.csv -m tpd
```

```
%cdspython -64 ../bin/plot_sweep_sigma.py -h
```

SPICE Compatibility

The Spectre® circuit simulator provides a SPICE compatibility mode, which eliminates the need for any netlist conversion in your flow.

For migration issues, see [*Spectre Circuit Simulator Migration Guide*](#).

You can add the `+spice` option to the `spectre` command line option:

```
spectre +spice options inputfile
```

The `+spice` option

- sets `tnom` and `temp` to 25C.
- sets parameter inheritance to global rather than the Spectre default of local. This means that global parameter definitions override local ones.
- sets flags on files that do not have an `.scs` extension or those that have sections with `simulator lang=spice` to be compatible with third-party simulators. This maps models in the SPICE sections to their Spectre equivalents, but does not modify Spectre files or sections.
- enforces `.IC` statements and initial conditions on elements for DC and OP analyses. By default, Spectre only forces initial conditions if the DC analysis `force` option is set.
- allows duplicate parameter definitions.

By default, Spectre does not allow duplicate parameter definitions. The `+spice` command-line option automatically sets the value of `redefinedparams` to `warning` and generates a warning for the redefined parameters.

- sets `auto_minductor` to `yes`.
- sets the default resistance to 1e-5, if it is not specified for the resistor.
- errors out if linear CCCS does not have coefficients.
- sets the sources to be `vcrspice` instead of `vcr`.

Support for SPICE Netlists

The Spectre circuit simulator can read syntax that is consistent with other commercial SPICE simulators. These features include, but are not limited to.

- Hierarchical identifiers

These are used to allow a parasitic device to connect to an internal node of the subcircuit.

- Miscellaneous SPICE syntax

Identifiers (instances, nodes, parameters, etc.) can include characters such as #, @ and |.

- Multiple namespaces

The same identifier can be used for different types of objects. In the following example,

```
.param res=1k
res res 0 res
.model res r r=res
```

res is an instance, node, model, and parameter.

- Global nodes

You can now have multiple global statements in a design.

- Mixed Spectre and SPICE syntax

You can include both Spectre and SPICE languages in a design, as long as you insert simulator `lang` switches.

- Behavioral primitives

The Spectre circuit simulator supports the SPICE feature that allows a source, resistor, capacitor and/or inductance value to be expressed as a behavioral expression.

- Library files and sections

The Spectre circuit simulator supports the `.lib` card for model inclusion.

- Model binning

With the new parser, the Spectre circuit simulator supports the syntax of popular SPICE models, including the syntax that allows you to bin models according to geometry size.

Note: All models in SPICE netlist sections are SPICE compatible.

Simulation Flow Compatible Options

Spectre also supports an extension of options used in the SPICE flow to better fit the existing simulation flow. These options are discussed below.

Options to Specify the Output Format

Option	Description
<code>outputcase=original</code>	Outputs all signal names in lower case or upper case. Possible values are <code>original</code> , <code>lower</code> , and <code>upper</code> .
<code>dotprobefmt=flat</code>	Prints the <code>.probe</code> signals with original name or hierarchical name. Possible values are <code>flat</code> and <code>hier</code> .

Options to Specify the Hierarchy Delimiter

Option	Description
<code>hier_delimiter="."</code>	Sets the hierarchical delimiter. The length of <code>hier_delimiter</code> should not be greater than 1, except the lead escape character.

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Option	Description
<code>hier_ambiguity=strict</code>	The default value is <code>strict</code>. When set to <code>lower</code>, the simulator partially flattens the hierarchy name from the back to check if an object can be found. As a result, the delimiter specified using <code>hier_delimiter</code> is treated as normal node name for signal matching. Possible values are <code>strict</code> and <code>lower</code>. Example: <pre>.options hier_delimiter="/" .options hier_ambiguity=lower .probe v(x1/x2/xnand/a) .ic v(x1/x2/xcell/mt)=1.2</pre> In the above example, <code>x1/x2</code> is an instance name and <code>xnand/ a</code> and <code>xcell/mt</code> are node names inside it. This typically happens in a DSPF file. When <code>hier_ambiguity=lower</code>, the character <code>/</code> is treated as a hierarchical delimiter for the instance <code>x1/x2</code>; however, it will be treated as part of the node name for nodes <code>xnand/a</code> and <code>xcell/mt</code>. As a result, the node names in <code>.ic</code> and <code>.probe</code> can be correctly matched.

Options to Control Duplicated Subcircuits, Measures, Instances, and Parameters

Spectre may generate an error for duplicate instance names, subcircuits, ports in a subcircuit, measures, models, and modules, based on strict and conservative rules. Spectre XPS provides the following options to modify the behavior and parse such duplicated definitions:

Option	Description
<code>duplicate_subckt=error</code>	Specifies whether duplicate subcircuit definitions are allowed. When set to <code>warning</code> or <code>ignore</code>, the simulator allows duplicate subcircuit definitions. If multiple subcircuit definitions are specified, the last one takes precedence. Possible values are <code>error</code>, <code>ignore</code>, and <code>warning</code>.

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Option	Description
<code>duplicateports=error</code>	Specifies whether duplicate ports are allowed in the subcircuit definition. When set to <code>warning</code> or <code>ignore</code> , duplicate ports are shorted. Depending on the value set, the simulator displays warning messages for duplicate ports, or does not display any message. When set to <code>error</code> , the simulator does not allow duplicate ports in the subcircuit definition and displays an error message. Possible values are <code>error</code> , <code>ignore</code> , and <code>warning</code> .
<code>duplicatemodel=error</code>	Specifies whether duplicate model definitions are allowed. When set to <code>warning</code> or <code>ignore</code> , the simulator allows duplicate model definitions. However, it honors only the last model definition. Depending on the value set, the simulator displays warning messages for duplicate model definitions, or does not display any message. When set to <code>error</code> , the simulator does not allow duplicate model definitions and displays an error message. Possible values are <code>error</code> , <code>ignore</code> , and <code>warning</code> .
<code>duplicate_measure=error first_win last_win</code>	
	Specifies whether duplicate measures are allowed. When set to <code>first_win</code> , the simulator allows duplicate measures, however, it honors only the first measure. When set to <code>last_win</code> , the simulator honors the last measure. When set to <code>error</code> , the simulator does not allow duplicate measure and displays an error message.
<code>duplicateinstance=error warning ignore</code>	
	Specifies whether duplicate instance definitions are allowed. When set to <code>warning</code> or <code>ignore</code> , the simulator allows duplicate instance definitions. If multiple instance definitions are specified, the last one takes precedence.
<code>redefinedparams=error warning ignore</code>	
	Specifies whether parameters can be redefined in the netlist. If a parameter is redefined multiple times, the last parameter definition takes precedence. The default value is <code>warning</code> in SPICE compatibility mode (<code>+spice</code>) and <code>error</code> in Spectre mode.

Option	Description
<code>redefinableparams=[param1 param2...]</code>	Specifies whether duplicate parameters definitions are allowed in the netlist for the specified parameters. For example: <code>opt1 options redefinableparams=[cx1 rx1]</code> If the above options statement is specified, Spectre will generate an error for all duplicate parameter definitions except the duplicate parameter definitions for the parameters <code>cx1</code> and <code>rx1</code> .
<code>duplicate_module=error</code>	Specifies whether duplicate module definitions are allowed. When set to <code>warning</code> or <code>ignore</code> , the simulator allows duplicate module definitions. However, it honors only the last module definition. Depending on the value set, the simulator displays warning messages for duplicate module definitions. When set to <code>error</code> , the simulator does not allow duplicate module definitions and displays an error message. Possible values are <code>error</code> , <code>ignore</code> , and <code>warning</code> .

Option to not Save the Waveform

Spectre XPS does not support SPICE options `.post` and `.probe`. In some situations, you may want to output only the measure file and not the waveform files, to save disk space. To do this, you can use the option `save=none`.

Note: The `save=none` option does not save any waveform; however, measure results, such as `.measure` and `.mt0` are still created for `.measure`.

Option to Enable or Disable the Safe Operation Area (SOA) Check

Spectre XPS supports the Safe Operation Area (SOA) check and its parameters that are often defined in the foundry model files. The SOA check is enabled by default. However, for large designs, the check may introduce performance overhead. You can use the `soa_warn` option with possible values of `yes` (default) and `no` to control the SOA check behavior. When `soa_warn=no` is specified, Spectre does not generate any warning for the SOA check. As a result, there is no performance overhead.

PSpice Netlist and Device Model Support

Spectre supports PSpice® netlist format targeting to include PCB components modeled in PSpice format into a Spectre integrated circuit simulation. This solution does not support PSpice-only designs. The top-level netlist and control statement need to be defined in Spectre, or SPICE format. The recommended approach is to define a subcircuit in PSpice netlist format and to instantiate the subcircuit in the Spectre netlist.

You can include a PSpice netlist in Spectre using the following statement.

```
pspice_include <file> (Spectre format)
.pspice_include <file> (SPICE format)
```

All content of the included file is required to be in PSpice format. If the file includes files, they are required to be in PSpice format. Elements and device models used in the PSpice netlist are simulated using PSpice default values and equations.

The Spectre PSpice feature does not support digital PSpice elements.

Spectre Netlists

This chapter discusses the following topics:

- [Instance Statements](#) on page 143
- [Analysis Statements](#) on page 147
- [Control Statements](#) on page 149
- [Model Statements](#) on page 152
- [Input Data from Multiple Files](#) on page 156
- [Structural Verilog](#) on page 161
- [Multidisciplinary Modeling](#) on page 162
- [Inherited Connections](#) on page 164

Netlist Statements

A Spectre® circuit simulator netlist describes the structure of circuits and subcircuits by listing components, the nodes that the components are connected to, the parameter values that are used to customize the components, and the analyses that you want to run on the circuit. You can use Verilog®-A to describe the behavior of new components that you can use in a netlist like built-in components. You can also define new components as a collection of existing components by using subcircuits.

A netlist consists of four types of statements:

- [Instance Statements](#) on page 57
- [Analysis Statements](#) on page 60
- [Control Statements](#) on page 63
- [Model Statements](#) on page 65

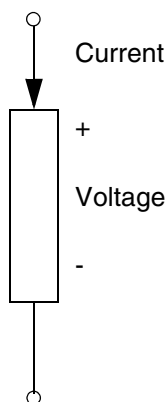
Before you can create statements for a Spectre netlist, you must learn some basic syntax rules of the Spectre Netlist Language.

Netlist Conventions

These are the netlist conventions followed by the Spectre simulator.

Associated Reference Direction

The reference direction for the voltage is positive when the voltage of the + terminal is higher than the voltage of the – terminal. A positive current arrives through the + terminal and leaves through the – terminal.



Ground

Ground is a common reference point in an electrical circuit. The value of ground is zero.

Node

A node is an infinitesimal connection point. The voltage everywhere on a node is the same. According to Kirchhoff's Current Law (also known as Kirchhoff's Flow Law), the algebraic sum of all the flows out of a node at any instant is zero.

Basic Syntax Rules

The following syntax rules apply to all statements in the Spectre Netlist Language:

- Field separators are blanks, tabs, punctuation characters, or continuation characters.
- Punctuation characters such as equal signs (=), parentheses (()), and colons (:) are significant to the Spectre simulator.
- You can extend a statement onto the next line by ending the current line with a backslash (\). You can use a plus sign (+) to indicate line continuation at the beginning of the next line. The preferred style is the \ at the end of the line.
- You can indicate a comment line by placing a double slash (//) at the beginning of the comment. The comment ends at the end of that line. You can also use an asterisk (*) to indicate a comment line. The preferred style is using //.
- You can indicate a comment for the remainder of a line by placing a space and double slash (//) anywhere in the line.

Spectre Language Modes

The Spectre netlist supports two language modes:

- Spectre mode (mostly discussed here)
- SPICE mode

You can specify the language mode for subsequent statements by specifying `simulator lang=mode`, where `mode` is `spectre` or `spice`.

Spectre mode input is fully case sensitive. In contrast, except for letters in quoted strings, SPICE mode converts input characters to lowercase. You can specify `insensitive=yes` along with `simulator lang=spectre` to make the Spectre mode case insensitive.

Creating Component and Node Names

When you create node and component names in the Spectre simulator, follow these rules.

- Do not use the name of an analysis (such as `tran`) or built-in primitive (such as `resistor`).
- Except for node names, names must begin with a letter or underscore. Node names can also be integers. However, you must not mix the node names that start with integers with other characters. Following are supported: `[0-9]+` or `_[a-z]{A-Z}(_[a-z]{A-Z}[0-9])+`.
- If the node name is an integer, leading zeros are significant in the Spectre language mode.
- Names can contain any number of letters, digits, or underscores.
- Names cannot contain nonalphanumeric characters, blanks, tabs, punctuation characters, or continuation characters (`\`, `+`, `-`, `//`, `*`) unless they are escaped with a backslash (`\`). The exception is bang (`!`), for example, `vdd!`.
- The following reserved words (case specified) should not be used as node names, net names, instance names, model names, or parameter names.

<code>M_1_PI</code>	<code>M_2_PI</code>	<code>M_2_SQRTPI</code>	<code>M_DEGPERRAD</code>
<code>M_E</code>	<code>M_LN10</code>	<code>M_LN2</code>	<code>M_LOG10E</code>
<code>M_LOG2E</code>	<code>M_PI</code>	<code>M_PI_2</code>	<code>M_PI_4</code>
<code>M_SQRT1_2</code>	<code>M_SQRT2</code>	<code>M_TWO_PI</code>	<code>P_C</code>
<code>P_CELSIUS0</code>	<code>P_EPS0P_H</code>	<code>P_K</code>	<code>P_Q</code>
<code>P_U0</code>	<code>abs</code>	<code>acos</code>	<code>acosh</code>
<code>altergroup</code>	<code>asin</code>	<code>asinh</code>	<code>atan</code>
<code>atan2</code>	<code>atanh</code>	<code>ceil</code>	<code>correlate</code>
<code>cos</code>	<code>cosh</code>	<code>else</code>	<code>end</code>
<code>ends</code>	<code>exp</code>	<code>export</code>	<code>floor</code>
<code>for</code>	<code>function</code>	<code>global</code>	<code>hypot</code>
<code>ic</code>	<code>if</code>	<code>inline</code>	<code>int</code>
<code>library</code>	<code>local</code>	<code>log</code>	<code>log10</code>
<code>march</code>	<code>max</code>	<code>min</code>	<code>model</code>

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nodeset	parameters	paramset	plot
pow	print	protect	pwr
real	return	save	sens
sin	sinh	sqrt	statistics
subckt	tan	tanh	to
truncate	vary		

Multiple Namespace

From release 5.0.32 onwards, you need not have unique names for device instances, models, nets, subcircuit parameters, enumerated named values for parameters, and netlist parameters that are expressions. Consider the following example:

```
simulator lang=spectre
parameters c1=1p c2=2p c10=c1+c2
parameters res=10k
res c10 0 resistor r=res
c10 c10 0 capacitor c=c10
run dc
spectre2 options currents=all
```

`res` is used as a parameter and instance name. `c10` is used as a node, instance, and parameter name. The Spectre circuit simulator can now read this netlist.

The Spectre circuit simulator can resolve ambiguous statements as shown in the example below:

```
parameters xyz=1
xyz 1 0 vsource dc=xyz
h1 3 0 ccvs probe=xyz rm=xyz
```

The Spectre circuit simulator assigns the instance `xyz` to `probe` and the parameter `xyz` to `rm`.

In the example below,

```
vcc vcc 0 vsource dc=1
save vcc
```

the Spectre circuit simulator saves the node `vcc` rather than the instance `vcc`. If you want to save the instance `vcc`, you must assign a different name to it.

Local NameSpace for subckt/model/verilogA

The Spectre circuit simulator supports local namespace for subckt/model/verilogA. The name is valid at the hierarchical level where it is defined and all levels below it. For subckt and model names, the namespace can be defined in the same netlist or in the included file. For verilogA, the namespace can only be invoked by the `ahdl_include` statement.

Example of model name:

```
simulator lang=spectre
vvdv vdd 0 vsource type=dc dc=1
I1 vdd 0 cap1
I2 vdd 0 cap2
I3 vdd 0 cap3

subckt cap1 a b
m1 b a b b nch w=10u l=5u
model nch bsim3v3 type=n mobmod=1 capmod=2 version=3.1 tox=9e-5 cdsc=1e-3 ends

subckt cap2 a b
m1 b a b b nch w=10u l=5u
model nch bsim3v3 type=n mobmod=1 capmod=2 version=3.2 tox=6.5e-5 cdsc=3e-3 ends

subckt cap3 a b
m1 b a b b nch w=10u l=5u
model nch bsim4 type=n mobmod=0 capmod=2 version=4.21 tox=3e-9 cdsc=2.58e-4 ends
```

In the above example, the model name `nch` cannot be accessed from the top level.

Escaping Special Characters in Names

If you have old netlists that contain names that do not follow Spectre syntax rules, you might still be able to run these netlists with the Spectre simulator. The Spectre Netlist Language permits the following exceptions to its normal syntax rules to accommodate old netlists. Use these features only when necessary.

If you place a backslash (\) before any printable ASCII character, including spaces and tabs, you can include the character in a name.

You can create a name from the following elements in the order given:

A string of digits, followed by

- ☐ Letters, underscores, or backslash-escaped characters, followed by
- ☐ A digit, followed by
- ☐ Underscores, digits, or backslash-escaped characters

This accommodates model or subcircuit libraries that use names like `\2N2222`.

Duplicate Specification of Parameters

If a parameter is specified more than once in the netlist, the Spectre circuit simulator uses the last specified value.

Instance Statements

In this section, you will learn to place individual components into your netlist and to assign parameter values for them.

Formatting the Instance Statement

To specify components, you use the instance statement. You format the instance statement as follows:

```
name [ ( node1 ... nodeN ) ] master [ [param1=value1] ... [paramN=valueN] ]
```

When you specify components with the instance statement, the fields have the following values:

<i>name</i>	The name you give to the statement. (Unlike SPICE instance names, the first character in Spectre instance names is not significant.)
[(<i>node1</i> ... <i>nodeN</i>)]	The names you give to the nodes that connect to the component. You have the option of putting the node names in parentheses to improve the clarity of the netlist. (See the examples later in this chapter.) You can use the hierarchical operator . to represent nodes inside a subcircuit hierarchy in your netlist. The Spectre circuit simulator supports forward referencing (retaining information about a node that is not defined yet, and mapping it when the node is defined) and relative path referencing (accessing a node with reference to the current scope). Look for examples in the section below. The simulator does not support hierarchical terminals in netlists.

master

This is the name of one of the following:
A built-in primitive (such as `resistor`)
A model
A subcircuit
An AHDL module (Verilog-A language)

Note: The instance statement is used to call subcircuits and refer to AHDL modules as well as to specify individual components. For more information about subcircuit calls, see [“Subcircuits”](#) on page 187. For more information about Verilog-A, see the *Verilog-A Language Reference* manual.

*parameter1=value1..
.parameterN=valueN*

This is an optional field you can repeat any number of times in an instance statement. You use it to specify parameter values for a component. Each parameter specification is an instance parameter, followed by an equal sign, followed by your value for the parameter. You can find a list of the available instance parameters for each component in the Spectre online help (`spectre -h`). As with node names, you can place optional parentheses around parameter specifications to improve the clarity of the netlist. For example, `(c=10E-12)`.

For subcircuits and ahdl modules, the available instance parameters are defined in the definition of the subcircuit or AHDL module. In addition, all subcircuits have an implicit instance parameter `m` for defining multiplicity. For more details about `m`, see [“Identical Components or Subcircuits in Parallel”](#) on page 145.

Examples of Instance Statements

In this example, a capacitor named `c1` connects to nodes 2 and 3 in the netlist. Its capacitance is `10E-12` Farads.

```
C1 (2 3) capacitor c=10E-12F
```

The following example specifies a component whose parameters are defined in a `model` statement. In this statement, `nPN` is the name of the model defined in a `model` statement that contains the model parameter definitions; `Q1` is the name of the component; and `o1`, `i1`, and `b2` are the connecting nodes of the component.

```
Q1 (o1 i1 b2) nPN
```

Note: The `model` statement is described in [Model Statements](#) on page 152. You can specify additional parameters for an individual component in an instance statement that refers to a `model` statement. You can find a list of available instance parameters and a list of available

model parameters for a component in the Spectre online help for that component (`spectre -h`).

Example of Forward Referencing in Hierarchical Nodes

```
simulator lang=spectre
...
c1 xa.mid 0 capacitor c=0.2p
...
xa 1 2 buffer
```

Example of Relative Path Referencing in Hierarchical Nodes

```
simulator lang=spectre
...
subckt wrapper a b
  x1 a b res_in_series
  rh x1.int1 x1.int2 resistor r=1
ends
x2 1 0 wrapper
```

Basic Instance Statement Rules

When you prepare netlists for the Spectre simulator, remember these basic rules:

- You must give each instance statement a unique name.
- If the *master* is a model, you need to specify the model.

Identical Components or Subcircuits in Parallel

If your circuit contains identical devices (or subcircuits) in parallel, you can specify this condition easily with the multiplication factor (*m*).

Specifying Identical Components in Parallel

If you specify an *m* value in an instance statement, it is as if *m* identical components are in parallel. For example, capacitances are multiplied by *m*, and resistances are divided by *m*. Remember the following rules when you use the multiplication factor:

- You can use *m* only as an instance parameter (not as a model parameter).

- The `m` value need not be an integer. The `m` value can be any positive real number.
- The multiplication factor does not affect short-channel or narrow-gate effects in MOSFETs.
- If you use the `m` factor with components that naturally compute branch currents, such as voltage sources and current probes, the computed current is divided by `m`. Terminal currents are unaffected.
- You can set the built-in `m` factor property on a subcircuit to a parameter and then `alter` it.

Example of Using `m` to Specify Parallel Components

In the following example, a single instance statement specifies four 4000-Ohm resistors in parallel.

```
Ro (d c) resistor r=4k m=4
```

The preceding statement is equivalent to

```
Ro (d c) resistor r=1k
```

Temperature Rise

The temperature rises from ambient. The `trise` parameter can be specified as a subcircuit parameter or a primitive parameter. The `trise` parameter has an accumulated effect for the subcircuit, the same as `m` has for parallel components.

```
subckt LoadOutput a b
    r1 (a b) resistor r=50k
    c1 (a b) capacitor c=2pF
ends LoadOutput
```

```
X1 (out 0) LoadOutput trise = 20
```

Subcircuit Temperature

The `temp` parameter can be specified as a subcircuit parameter or a primitive parameter. The `temp` parameter overwrites all the other temperature values set in options or `trise` parameter. It is an exclusive effective temperature for a specified subcircuit.

```
subckt LoadOutput a b
    r1 (a b) resistor r=50k
    c1 (a b) capacitor c=2pF
    xx1 (a b) RCsub trise = 5
ends LoadOutput
```

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```
subckt RSub 1 2
    rr1 (1 2) resistor r=10k
    cc1 (1 2) capacitor c=2pF
ends RSub
X1 (out 0) LoadOutput temp = 100
```

In the above example, Spectre simulates X1 with temperature at 100 celsius while X1 .xx1 is simulated with a temperature at 105 celsius.

Specifying Subcircuits in Parallel

If you place a multiplication factor parameter in a subcircuit call, you model *m* copies of the subcircuit in parallel. For example, suppose you define the following subcircuit:

```
subckt LoadOutput a b
    r1 (a b) resistor r=50k
    c1 (a b) capacitor c=2pF
ends LoadOutput
```

If you place the following subcircuit call in your netlist, the Spectre simulator models five LoadOutput cells in parallel:

```
x1 (out 0) LoadOutput m=5
```

Analysis Statements

In this section, you will learn to place analyses into your netlist and to assign parameter values for them. For more information on analyses, see and the Spectre online help (spectre -h).

Basic Formatting of Analysis Statements

You format analysis statements in the same way you format component instance statements except that you usually do not put a list of nodes in analysis statements. You specify most analysis statements as follows:

Name [(*node1* ... *nodeN*)] *Analysis Type* *parameter=value*

where

Name The name you give to the analysis.

`[([node1 ... nodeN])]` Names you give to the nodes that connect to the analysis. You have the option of putting the node names in parentheses to improve the clarity of the netlist. (See the examples later in this chapter.) For most analyses, you do not need to specify any nodes. You can use the hierarchical operator `.` to represent nodes inside a subcircuit hierarchy in your netlist. The Spectre circuit simulator supports forward referencing (retaining information about a node that is not defined yet, and mapping it when the node is defined) and relative path referencing (accessing a node with reference to the current scope). Look for examples in the section below. The simulator does not support hierarchical terminals in netlists.

Analysis Type Spectre name of the type of analysis you want, such as `ac`, `tran`, or `xf`. You can find this name by referring to the topics list in the Spectre online help (`spectre -h`).

parameter=value List of parameter values you specify for the analysis. You can specify values for any number of parameters. You can find parameter listings for an analysis by referring to the Spectre online help (`spectre -h`).

Note: The `noise`, `xf`, `pnoise`, and `pxf` analyses let you specify nodes, *p* and *n*, which identify the output of the circuit. When you use this option, you should use the full analysis syntax as follows:

```
Name> [p n] Analysis Type parameter=value
```

If you do not specify the *p* and *n* terminals, you must specify the output with a probe component.

Examples of Analysis Statements

The following examples illustrate analysis statement syntax.

```
XferVsTemp xf start=0 stop=50 step=1 probe=Rload param=temp freq=1kHz
```

This statement specifies a transfer function analysis (`xf`) with the user-supplied name `XferVsTemp`. With all transfer functions computed to a probe component named `Rload`, it sweeps temperature from 0 to 50 degrees in 1-degree steps at frequency 1 kHz. (For long statements, you must place a backslash (`\`) at the end of the first line to let the statement continue on the second line.)

```
Sparams sp stop=0.3MHz lin=100 ports=[Pin Pout]
```


This statement requests an S-parameter analysis (`sp`) with the user-supplied name `Sparams`. A linear sweep starts at zero (the default) and continues to .3 MHz in 100 linear steps. The `ports` parameter defines the ports of the circuit; ports are numbered in the order given.

The following example statement demonstrates the proper format to specify optional output nodes (`p n`):

```
FindNoise (out gnd) noise start=1 stop=1MHz
```

Basic Analysis Rules

When you prepare netlists for the Spectre simulator, remember these basic analysis rules:

- The Spectre simulator has no default analysis. If you do not put any analysis statements into a netlist, the Spectre simulator issues a warning and exits.
- For most analyses, if you specify an analysis that has a prerequisite analysis, the Spectre simulator performs the prerequisite analysis automatically. For example, if you specify an AC analysis, the Spectre simulator automatically performs the prerequisite DC analysis. However, if you want to run a `pac`, `pxf`, or `pnoise` analysis, you must specify the prerequisite `pss` analysis.
- You specify analyses in the order you want the Spectre simulator to perform them.
- You can perform more than one of the same type of analysis in a single Spectre run. Consequently, you can perform several analyses of the same type and vary parameter values with each analysis.
- You must give each analysis or control statement a unique name. The Spectre simulator requires these unique names to identify output data and error messages.

Control Statements

The Spectre simulator lets you place a sequence of control statements in the netlist. You can use the same control statement more than once. Spectre control statements are discussed throughout this manual. The following are control statements:

- `alter`
- `altergroup`
- `assert`
- `check`

- `checklimit`
- `ic`
- `info`
- `nodeset`
- `options`
- `paramset`
- `save`
- `set`
- `shell`
- `statistics`

Formatting the Control Statement

Control statements often have the same format as analysis statements. Like analysis statements, many control statements must have unique names. These unique names let the Spectre simulator identify the control statement if there are error messages or other output associated with the control statement. You specify most control statements as follows:

Name Control Statement Type parameter=value

where

<i>Name</i>	Unique name you give to the control statement.
<i>Control Statement Type</i>	Spectre name of the type of control statement you want, such as <code>alter</code> . You can find this name by referring to the topics list in the Spectre online help (<code>spectre -h</code>).
<i>parameter=value</i>	List of parameter values you specify for the control statement. You can specify values for any number of parameters. You can find parameter listings for a control statement by referring to the Spectre online help (<code>spectre -h</code>).

Examples of Control Statements

```
SetTemp alter param=temp value=27
```

The preceding example of an `alter` statement sets the temperature for the simulation to 27°C. The name for the `alter` statement is `SetTemp`, and the name of the control statement type is `alter`.

You cannot alter a device from one primitive type to another. For example,

```
inst1 (1 2) capacitor c=1pF
alterfail altergroup{
    inst1 (1 2) resistor r=1k
}
```

is illegal.

Another example of a control statement is the `altergroup` statement, which allows you to change the values of any modifiable device or netlist parameters for any analyses that follow. Within an alter group, you can specify parameter, instance, or model statements; the corresponding netlist parameters, instances, and models are updated when the `altergroup` statement is executed. These statements must be bound within braces. The opening brace is required at the end of the line defining the alter group. Alter groups cannot be nested or be instantiated inside subcircuits. Also, no topology changes are allowed to be specified in an alter group.

The following is the syntax of the `altergroup` statement:

```
Name altergroup ... {
    netlist parameter statements ...
```

and/or

```
    device instance statements ...
```

and/or

```
    model statements ...
```

and/or

```
    parameter statements ...
}
```

The following is an example of the `altergroup` statement:

```
v1 1 0 vsource dc=1
R1 1 0 Resistor R=1k
dc1 dc // this analysis uses a 1k resistance value
al altergroup {
    R1 1 0 Resistor R=5k
}
dc2 dc // this analysis uses a 5k value
```

Model Statements

`model` statements are designed to allow certain parameters, which are expected to be shared over many instances, to be given once. However, for any given component, it is predetermined which parameters can be given on `model` statements for that component.

This section gives a brief overview of the Spectre `model` statement. For a more detailed discussion on modeling issues (including parameterized models, expressions, subcircuits, and model binning), see [Chapter 9, “Parameter Specification and Modeling Features”](#).

Formatting the model Statement

You format the `model` statement as follows:

```
model name master [param1=value1 ... [param2=value2 ]]
```

The fields have the following values:

<code>model</code>	The keyword <code>model</code> (<code>.model</code> is used for SPICE mode).
<code>name</code>	The name you give to the model.
<code>master</code>	The master name of the component, such as <code>resistor</code> , <code>bjt</code> , or <code>tline</code> . This field can also contain the name of an AHDL module.
<code>parameter1=value1 ...<parameterN=valueN></code>	This is an optional field you can repeat any number of times in a <code>model</code> statement. Each parameter specification is a model parameter, followed by an equal sign, followed by the value of the parameter. You can find a list of the available model parameters for each component in the parameter listings of Spectre online help (<code>spectre -h</code>).

Creating a Model Alias

You can create an alias for a model as follows:

```
model alias_model original_model
```

<code>alias_model</code>	Alias for the model.
<code>original_model</code>	Model defined in the current scope.

For example,

```
model res resistor r=1K
model alias_res res
r1 (a b) alias_res
```

Creating an alias for a Subcircuit

You can also create an alias for a subcircuit (subckt) as follows:

```
model alias_subckt original_subckt
```

alias_subckt Alias for the subcircuit.

original_subckt Subcircuit defined in the current scope.

For example,

```
subckt sub a b
r1 (a b) r = 10k
ends
model alias_sub sub
x1 1 0 alias_sub
```

Examples of model Statements

The following examples give parameters for a `tline` model named `tuner` and a `bjt` model named `NPNbjt`.

```
model tuner tline f=1MHz alphac=9.102m dcr=105m
model NPNbjt bjt type=npn bf=100 js=0.1fA
```

Note: The backslash (\) is used as a continuation character in this lengthy `model` statement.

```
model NPNbjt2 bjt \
    type=npn is=3.38e-17 bf=205 nf=0.978 vaf=22 \
    ikf=2.05e-2 ise=0 ne=1.5 br=62 nr=1 var=2.2 isc=0 \
    nc=1.5 rb=115 re=1 rc=30.5 cje=1.08e-13 vje=0.995 \
    mje=0.46 tf=1e-11 xtf=1 itf=1.5e-2 cjc=2.2e-13 \
    vjc=0.42 mjc=0.22 xcjc=0.1 tr=4e-10 cjs=1.29e-13 \
    vjs=0.65 mjs=0.31 xtb=1.5 eg=1.232 xti=2.148 fc=0.875
```

The following example creates two instances of a `bjt` transistor model:

```
a1 (C B1 E S) NPNbjt
a2 (C B2 E S) NPNbjt2
```

Using analogmodel for Model Passing (analogmodel)

`analogmodel` is a reserved word in Spectre that allows you to bind an instance to different masters based on the value of a special instance parameter called `modelname`. An instance of `analogmodel` must have a parameter named `modelname` whose string value will be the name of the master this instance will be bound to. The value of `modelname` can be passed into subcircuits.

The `analogmodel` keyword is used by the Cadence Analog Design Environment to enable model name passing through the schematic hierarchy.

Sample Instance Statement

```
name [ ( ] node1 ... nodeN [ ) ] analogmodel modelname=mastername [[param1=value1]
...[paramN=valueN]]
```

<code>name</code>	Name of the statement or instance label.
<code>[(] node1 ... nodeN [)]</code>	Names of the nodes that connect to the component.
<code>analogmodel</code>	Special device name to indicate that this instance will have its master name specified by the value of the <code>modelname</code> parameter on the instance.
<code>modelname</code>	Parameter to specify the master of this instance indicated by <code>mastername</code> . The <code>mastername</code> must either be a valid string identifier or a netlist parameter that must resolve to a valid master name, a primitive, a model, a subckt, or an AHDL module.
<code>param1 param2...</code>	Parameter values for the component. Depending on the master type, these can either be device parameters or netlist parameters. It is optional to specify these parameter values.

Example

```
//example spectre netlist to illustrate modelname parameter
simulator lang=spectre
parameters b="bottom"
include "VerilogAStuff.va"
topInst1 (out in) top
topInst2 (out in) analogmodel modelname="VAMaster" //VAMaster is defined in
"VerilogAStuff.va"
```

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```
topInst3 (out in) analogmodel modelname="resistor" //topInst3 binds to a
primitive
topInst4 (out 0) analogmodel modelname="myOwnRes" //topInst4 binds to modelcard
"myOwnRes" defined below
v1 in 0 vsource dc=1
model myOwnRes resistor r=100
subckt top out in
    parameters a="mid"
    x1 (out in) analogmodel modelname=a //topInst1.x1 binds to "mid"
ends top
subckt mid out in
    parameters c="low"
    x1 (out in) analogmodel modelname=b //topInst1.x1.x1 binds to "bottom"
    x2 (out in) analogmodel modelname=c //topInst1.x1.x1.x2 binds to "low"
ends mid
subckt low out in
    x1 (out in) analogmodel modelname="bottom" //topInst1.x1.x1.x2.x1 binds to
"bottom"
ends low
subckt bottom out in
    x1 (out in) analogmodel modelname="resistor" //x1 binds to primitive
"resistor"
ends bottom
dcl dc
//"VerilogASTuff.va"
include "constants.h"
include "discipline.h"
module VAMaster(n1, n2);
inout n1, n2;
electrical n1, n2;
parameter r=1k;
    analog begin
        I(n1, n2) <+ V(n1, n2)/r;
    end
endmodule
```

Basic model Statement Rules

When you use the `model` statement,

- You can have several `model` statements for a particular component type, but each instance statement can refer to only one `model` statement.

- Occasionally, a component allows a parameter to be specified as either an instance parameter or as a model parameter. If you specify it as a model parameter, it acts as a default for instances. If you specify it as an instance parameter, it overrides the model parameter.
- Values for model parameters can be expressions of netlist parameters.

Input Data from Multiple Files

If you want to use data from multiple files, use the `include` statement to insert new files. When the Spectre simulator reads the `include` statement in the netlist, it finds the new file, reads it, and then resumes reading the netlist file.

If you have older netlist files you want to incorporate into your new, larger netlist, the `include` statement is particularly helpful. Instead of creating a completely new netlist, you can use the `include` statement to insert your old files into the netlist at the location you want.

Note: The Spectre simulator always assumes that the file being included is in SPICE language mode unless the extension of the filename is `.scs`.

Note: The Spectre circuit simulator can also read compressed files included using the `include` or `dspf_include` statements. To add the file using the `include` statement, the file must be compressed using gzip (`.gz` extension) or bzip2 (`.bz2` extension). To add a compressed file using the `dspf_include` statement, the file must be compressed using the gzip (`.gz` extension).

Syntax for Including Files

Including Verilog-A Modules

To include Verilog-A modules in your netlist, use the `ahdl_include` statement. The Spectre circuit simulator compiles the complete module during the initial simulation. The module is re-compiled during subsequent simulations only if it is modified. This may result in a performance improvement. If you are making frequent changes to the Verilog-A in your design, you can turn the one-step compilation off by using the following command:

```
setenv CDS_AHDL_CMI_ENABLE NO
```

Including Digital Vector Files

You can add a digital vector text file to a Spectre netlist using the following statement


```
vec_include filename
```

For a SPICE netlist, use the following statement

```
.vec filename
```

For more information on the digital vector file refer to [Appendix D, “Digital Vector File Format.”](#)

Including Verilog Value Change Dump Files

You can add a Verilog Value Change Dump (VCD) or an Extended VCD (EVCD) file to a Spectre netlist using the following statements respectively

```
vcd_include vcd_filename vcd_signal_info
```

```
evcd_include evcd_filename evcd_signal_info
```

For a SPICE netlist, use the following statements

```
.vcd_include vcd_filename vcd_signal_info
```

```
.evcd_include evcd_filename evcd_signal_info
```

For more information on the digital vector file refer to [Appendix E, “Verilog Value Change Dump Stimuli.”](#)

Formatting the include Statement

You can use any of two formatting options for the `include` statement. When you want to use C preprocessor (CPP) macro-processing capabilities within your inserted file, use the second format (`#include`). These are the two format options:

```
include "filename"
```

```
#include "filename"
```

The first option (`include`) is performed by the Spectre simulator itself. The second option (`#include`) is performed by the CPP. You must use the `#include` option when you have macro substitution in the inserted file.

Note: CPP is not supported in Spectre Direct.

Rules for Using the include Statement

Remember the following rules and guidelines when using the `include` statement:

- You must use the `#include` format if you want the CPP to process the inserted file. Also, you must specify that the CPP be run using the `-E` command line option when you start the Spectre simulator.
- Regardless of which include format you use, you can use the `-I` command line option, followed by a path, to have the Spectre simulator look for the inserted files in a specified directory, in addition to the current directory, just as you would for the CPP `#include`.

When you use the `-I` command-line option with `#include`, it triggers the C preprocessor (CPP) to parse the netlist file. You can use the `-disableCPP` command-line option along with the `-I` command-line option to disable the C preprocessor to parse the netlist file.

If you use both `-E` and `-disableCPP` options on the command line, along with the `-I` command-line option, the `-E` option takes precedence over the `-disableCPP` option, and C preprocessor is used to parse the netlist file.

- If *filename* is not an absolute path specification, it is considered relative to the directory of the including file that the Spectre simulator is reading, not from the directory in which the Spectre simulator was called.
- You must surround the *filename* in quotation marks.
- You can place a space and then a backslash-escaped newline (`\`) between `include` and *filename* for line continuation.
- You can place other `include` statements in the inserted file.
- With any of the `include` formats, you can set the language mode for the inserted file by placing a `simulator lang` command at the beginning of the file. The Spectre simulator assumes that the file to be included is in the SPICE language unless one of the following conditions occurs:
 - ❑ The file to be included has a `simulator lang=spectre` line at the beginning of the file. (The first line is not a comment title line, even in SPICE mode.)
 - ❑ The file to be included has a `.scs` file extension.
- With the `include` format, if you change the language mode in an inserted file, the language mode returns to that of the original file at the end of the inserted file.
- You cannot start a statement in an original file and end it in an inserted file or vice versa.
- You can use `include "~/filename"`, and the Spectre simulator looks for *filename* in your home directory. This does not work for `#include`.
- You can use environment variables in your include statements. For example,
`include "$MYMODELS/filename"`

The Spectre simulator looks for *filename* in the directory specified by `$MYMODELS`. This works for `include`, but not for `#include`.

There are two major differences between using `#include` and `include`:

- You can specify `#include` to run CPP and use macros and #-defined constants.
- `#include` does not expand special characters or environment variables in the filename.

Example of include Statement Use

In the following `include` statement example, the Spectre simulator reads initial program options and then inserts two files, `cmos.mod` and `opamp.ckt`. After reading these files, it returns to the original file and reads further data about power supplies.

```
// example of using include statement
global gnd vdd vss
simulator lang=spectre
parameters VDD=5
include "cmos.mod"
include "opamp.ckt"

// power supplies
Vdd    vdd    gnd    vsource dc=VDD
Vss    vss    gnd    vsource dc=-VDD
```

Reading Piecewise Linear (PWL) Vector Values from a File

You could type the following component description into a netlist:

```
v4 in 0 vsource type=pwl wave=[0 0 1n 0 2n 5 10n 5 11n 0 12n 0]
```

You could also enter the vector values and SI scalar values (p, n, u, m, k, M, G, and so on) from a file, in which case the component description might look like this:

```
v4 in 0 vsource type=pwl file="test.in"
```

You can use the `-I` command line option, followed by a path, to have the Spectre simulator look for the inserted files in a specified directory if they cannot be found in the current directory.

If you use an input file, the values in the file must look like the following:

```
0          0
1e-9       0
2e-9       5
10e-9      5
11e-9      0
12e-9      0
```

The following is an example of SI scalar values in the input file:

```
0 0
1u 4m
2u 3m
3u 2m
4u 1m
5u -1m
6u -2m
```

The input file may also contain design variables. For example, the input file can have time, value, or both time and value as variables. The expressions may also contain empty spaces. For example:

```
1u 0
4u volt1
time1 + 5u 0
time1+5u volt2
```

Note: There should be no ambiguity in the expression, otherwise, Spectre generates an error. For example, Spectre will generate an error if the following expression is specified in the PWL file:

```
time1 + 4u +5
```

Also see [vpwlf](#) for a definition of vpwlf source.

Using Library Statements

Another way to insert new files is to use the library statements. There are two statements: one to refer to a library and one that defines the library. A library is a way to group statements into multiple sections and selectively include them in the netlist by using the name of the section.

As for the include statement, the default language of the library file is SPICE unless the extension of the file is `.scs`; then the default language is the Spectre Netlist Language.

Library Reference

This statement refers to a library section. This statement can be nested. To see more information on including files, see `spectre -h include`. The name of the section has to match the name of the section defined in the library. The following is the syntax for library reference:

```
include "file" section=Name
```

where *file* is the name of the library file to be included. The library reference statement looks like an include statement, except for the specification of the library section. When the file is being inserted, only the named section is actually included.

Library Definition

The library definition has to be in a separate file. The library has to have a name. Each section in the library has to be named because this name is used by the library reference statement to identify the section to include. The *statements* within each section can be any valid statement. This is important to remember when using libraries in conjunction with alter groups because the `altergroup` statement is restrictive in what can be specified.

The optional names are allowed at the end of the section and library. Spectre does not check if these names match the names of the section or library.

The following is the syntax for library definition:

```
library libraryName
  section sectionName
    statements
  endsection [sectionName]
  section anotherName
    statements
  endsection [anotherName]
endlibrary [libraryName]
```

One common use of library references is within `altergroup` statements. For example:

```
a1 altergroup {
    //change models to "FAST" process corner
    include "MOSLIB" section=FAST
}
```

Structural Verilog

The Spectre circuit simulator supports structural Verilog netlist files for verification of digital circuits. This approach is typically used for standard cell designs, where the Verilog netlist file is generated by synthesis tools, and SPICE subcircuits are available for all standard cells.

The most common approach is to use a top-level SPICE file that contains the analysis statement, probes, measures, and simulation control statements, and also calls to one or more Verilog netlist files. The Verilog netlist files contain calls of basic cells, which are available in the SPICE netlist file.

You can also include Verilog files by using the `vlog_include` statement, as shown below.

```
vlog_include "file.v" supply0=gnd supply1=vdd insensitive=no|yes
```

Spectre reads the structural Verilog file `file.v`. The keywords are `supply0` and `supply1`. The `supply0` keyword must be set to the ground node used in the Verilog subcircuit and `supply1` must be set to the power supply node. If `insensitive=yes` is specified, the Verilog netlist file is parsed as case insensitive. If `insensitive=no` is specified, it is parsed as case sensitive. The default value is `no`.

Note: If the name of a module called by SPICE contains uppercase letters (for example, `top_MODULE`), then set `insensitive=yes` to use the `vlog_include` statement.

Unsupported Structural Verilog Features

Spectre does not support the following structural Verilog features:

- Multi-bit expression (for example, `3'fb1`)
- Arrayed instances
- `defparam`
- `triereg`, `triand`, `trior`, `tri0`, `tri1`, `wand`, and `wor` nets
- Strength and delay
- Generated instances
- User-defined procedures (UDPs)
- Attributes

Multidisciplinary Modeling

Multidisciplinary modeling involves setting tolerances and using predefined quantities.

Setting Tolerances with the `quantity` Statement

Quantities are used to hold convergence-related information about particular types of signals, such as their units, absolute tolerances, and maximum allowed change per Newton iteration. With the `quantity` statement, you can create quantities and change the values of their parameters. You set these tolerances with the `abstol` and `maxdelta` parameters, respectively. You can set the `huge` parameter, which is an estimate of the probable maximum value of any signal for that quantity. You can also set the `blowup` parameter to define an upward bound for signals of that quantity. If a signal exceeds the `blowup` parameter value, the analysis stops with an error message.

Generally, a reasonable value for the absolute tolerance of a quantity is 10^6 times smaller than its greatest anticipated value. A reasonable definition for the `huge` value of a quantity is 10 to 10^3 times its greatest expected value. A reasonable definition of the `blowup` value for a quantity is 10^6 to 10^9 times its greatest expected value.

Predefined Quantities

The Spectre Netlist Language has seven predefined quantities that are relevant for circuit simulation, and you can set tolerance values for any of them. These seven predefined quantities are

- Electrical current in Amperes (named I)
(Default absolute tolerance = 1 pA)
- Magnetomotive force in Amperes (named MMF)
(Default absolute tolerance = 1 pA-turn)
- Electrical potential in Volts (named V)
(Default absolute tolerance = 1 μ V; Default maximum allowable change per iteration = 300mV)
- Magnetic flux in Webers (named Wb)
(Default absolute tolerance = 1 nWb)
- Temperature in Celsius (named $Temp$)
(Default absolute tolerance = 100 μ C)
- Power in Watts (named Pwr)
(Default absolute tolerance = 1 nW)
- Unitless (named U)
(Default absolute tolerance = 1×10^{-6})

For more information, see `spectre -h quantity`.

quantity Statement Example

The electrical potential quantity has a normal default setting of 1 μ V for absolute tolerance (`abstol`) and 300 mV for maximum change per Newton iteration (`maxdelta`). You can change `abstol` to 5 μ V, reset `maxdelta` to 600 mV, define the estimate of the maximum voltage to be 1000 V, and set the maximum permitted voltage to be 10^9 with the following statement:

```
VoltQuant quantity name="V" abstol=5uV maxdelta=600mV  
huge=1000V blowup=1e9
```

`VoltQuant` is a unique name you give to the `quantity` statement.

The keyword `quantity` is the primitive name for the statement.

The `name` parameter identifies the quantity you are changing. (`V` is the name for electrical potential.)

`abstol`, `maxdelta`, `huge`, and `blowup` are the parameters you are resetting.

Note: The `quantity` statement has other uses besides setting tolerances. You can use the `quantity` statement to create new quantities or to redefine properties of an existing quantity, and you can use the `node` statement to set the quantities for a particular node. For more information about the `quantity` statement, see the Spectre online help (`spectre -h quantity`). For more information on the `node` statement, see `spectre -h node`. The following is an example of a `node` statement:

```
setToMagnetic t1 t2 node value="Wb" flow="MMF" strength=insist
```

Inherited Connections

Inherited connections is an extension to the connectivity model that allows you to create global signals and override their names for selected branches of the design hierarchy. The flexibility of inherited connections allows you to use

- Multiple power supplies in a design
- Overridable substrate connections
- Parameterized power and ground symbols

You can use an inherited connection so that you can override the default connection made by a signal or terminal. This method can save you valuable time. You do not have to re-create an entire subbranch of your design just to change one global signal.

For more detailed information on how to use inherited connections and net expressions with various Cadence® tools in the design flow, see the *Inherited Connections Flow Guide*.

Parameter Specification and Modeling Features

You can use the Spectre® circuit simulator models and AHDL modules in Spectre netlists. This chapter describes the powerful modeling capabilities of Spectre, including

- [Instance \(Component or Analysis\) Parameters](#) on page 166
- [Parameters Statement](#) on page 171
- [Expressions](#) on page 173
- [Subcircuits](#) on page 187
- [Inline Subcircuits](#) on page 196
- [Binning](#) on page 205
- [Scaling Physical Dimensions of Components and Device Model Technology](#) on page 218
- [Multi-Technology Simulation](#) on page 220

Instance (Component or Analysis) Parameters

In this section, you will learn about the types of component or analysis parameter values the Spectre circuit simulator accepts and how to specify them.

Types of Parameter Values

Spectre component or analysis parameters can take the following types of values:

- Real or integer expression, consisting of
 - Literals
 - Arithmetic or Boolean operators
 - Predefined circuit or subcircuit parameters
 - Built-in constants (fixed values) or mathematical functions (software routines that calculate equations)
 - Real or integer constants
- The name of a component instance or model
- The name of a component parameter
- A character string (must be surrounded by quotation marks)
- A name from a predefined set of names available to specify the parameter value (enumerated types)

Parameter Dimension

Component or analysis parameters can be either scalar or vector.

If a component or analysis parameter value is a group of numbers or names, you specify the group as a vector of values by enclosing the list of items in square brackets (`[]`)—for example, `coeffs=[0 0.1 0.2 0.5]` to specify the parameter values 0, 0.1, 0.2, and 0.5. You can specify a group of number pairs (such as time-voltage pairs to specify a waveform) as a vector of the individual numbers.

For a vector parameter assignment, you can use the `range` function to specify a range of values. Following is the syntax for the `range` function:

```
range(start, stop, step)
```

Here,

`start` - start value of the parameter range

`stop` - end value of the parameter range

`step` - number by which the parameter's value should be increased. The `step` argument is optional. If it is not specified, the default value is taken as 1. Negative values are also supported. The values can be integer or float.

For example,

```
<param_name>=[1 2 3 range(4, 10, 2)]
```

will return [1 2 3 4 6 8 10].

Remember these guidelines when you specify vectors of value:

- You can mix numbers and netlist or subcircuit parameter names in the same vector (`coeff=[0 coeff1 coeff2 0.5]`).
- You cannot leave a list of items empty.
- You can use expressions (such as formulas) to specify numbers within a vector. When you use a vector of expressions, each expression must be surrounded by parentheses (`coeff=[0 (A*B) C 0.5]`).
- You can use subcircuit parameters within vectors.

Parameter Ranges

Parameter ranges have hard limits and soft limits. Hard limits are enforced by the Spectre simulator; if you violate them, the Spectre simulator issues an error and terminates. You specify soft limits; if you violate them, the Spectre simulator issues a warning and continues. Soft limits are used to define reasonable ranges for parameter values and can help find “unreasonable” values that are likely errors. You can change soft limits, which are defined in one or more files. Use the `+param` command line option to use the suggested parameter range limits.

You can specify limits for any scalar parameter that takes either a real number, an integer, or an enumeration. To specify the limits of a parameter that takes enumerations, use the indices or index values associated with the enumerations. For example, consider the region parameter of the `bjt`. There are four possible regions (see `spectre -h bjt`):

- `off`
- `fwd`

- `rev`
- `sat`

Each enumeration is assigned a number starting at 0 and counting up. Thus,

- `off=0`
- `fwd=1`
- `rev=2`
- `sat=3`

The specification `bjt 3 <= region <= 1` indicates that a warning is printed if `region=rev` because the conditions `3 <= region` and `region <= 1` exclude only `region=2` and `region 2` is `rev`.

For more information on parameter range checking, see [Checking for Invalid Parameter Values](#) on page 191.

Help on Parameters

There are four main ways to get online help about Spectre component or analysis parameters.

spectre -help

When you type `spectre -help name`, where *name* is the name of a component or analysis, you get the following information:

- Parameter names
Related parameters are grouped together.
- Parameter defaults
- Units
- Parameter description

For analyses and controls, parameters are listed in the “Parameters” section. At the end of the longer parameter listings is the parameter index. This index lists the parameters alphabetically and gives the number that corresponds to where the parameter is in the numbered list.

For components, parameters are divided into up to four sections: “Instance Parameters,” “Model Parameters,” “Output Parameters,” and “Operating Point Parameters.” At the end of longer parameter listings is the parameter index. This index indicates where to find a parameter’s description with a letter and a number. The letter refers to the section (for example, *I* refers to the instance parameters section, *M* refers to the model parameters section, *O* refers to the output parameters section, and *OP* refers to the operating-point parameters section), and the number refers to where the parameter is in the numbered list.

spectre -helpsort

When you type `spectre -helpsort name`, where *name* is the name of a component or analysis, you get the same information as you do with `spectre -h name`, but the parameters are sorted alphabetically instead of divided into related groups.

spectre -helpfull

When you type `spectre -helpfull name`, where *name* is the name of a component or analysis, you get related parameters grouped as you do with `spectre -h name`, and you get the following additional information:

- Parameter type
- Parameter dimension—scalar or vector
- Parameter range

spectre -helpsortfull

When you type `spectre -helpsortfull name`, where *name* is the name of a component or analysis, you get the same information as you do with `spectre -helpfull name`, but the parameters are sorted alphabetically instead of divided into related groups.

Scaling Numerical Literals

If a parameter value is an integer or a floating-point number, you can scale it in the following ways:

- Follow the number with an *e* or an *E* and an integer exponent (for example, `2.65e3`, `5.32e-4`, `1E-14`, `3.04E6`)
- Use scale factors (for example `5u`, `3.26k`, `4.2m`)

Important

You cannot use both scale factors and exponents in the same parameter value. For example, the Spectre simulator ignores the *p* in a value such as 1.234E-3*p*.

Caution

The Spectre simulator also accepts additional data files, such as the waveform and noise files accepted by the independent sources or the S-parameter file accepted by the N-port. Generally, these files do not accept numbers with scale factors.

The Spectre mode (`simulator lang=spectre`) accepts only the following ANSI standard (SI) scale factors:

$T=10^{12}$	$G=10^9$	$M=10^6$	$K=10^3$	$k=10^3$
$_ =1$	$\% =10^{-2}$	$c=10^{-2}$	$m=10^{-3}$	$u=10^{-6}$
$n=10^{-9}$	$p=10^{-12}$	$f=10^{-15}$	$a=10^{-18}$	

Note: SI scale factors are case sensitive.

The Spectre simulator allows you to specify units, but only if you specify a scale factor. If specified, units are ignored. Thus,

```
c=1pf // units = "f"  
l=1uH // units = "H"
```

are accepted, but

```
r=50Ohms
```

is rejected because units are provided without a scale factor. For the last example, use

```
r=50_Ohms
```

SPICE mode (`simulator lang=spice`) accepts only the following SPICE scale factors:

Note: SPICE scale factors are not case sensitive. Any other scale factor is ignored (treated as 1.0).

$t=10^{12}$	$g=10^9$	$meg=10^6$	$k=10^3$	$p=10^{-12}$
$m=10^{-3}$	$mil=25.4 \times 10^{-6}$	$u=10^{-6}$	$n=10^{-9}$	$f=10^{-15}$



If you are not clear about the scaling rules for each simulation mode, you can cause errors in your simulation. For example, 1.0M is interpreted as 10^{-3} in the SPICE mode but as 10^6 in the Spectre mode.

Parameters Statement

In this section, you will learn about the circuit and subcircuit parameters (collectively known as netlist parameters) as defined by the `parameters` statement.

Circuit and Subcircuit Parameters

The Spectre Netlist Language allows real-valued parameters to be defined and referenced in the netlist, both at the top-level scope and within subcircuit declarations (run `spectre -h subckt` for more details on parameters within subcircuits).

The format for defining parameters is as follows:

```
parameters param=value param=value ...
```

Once defined, you can use parameters freely in expressions. The following are examples:

```
simulator lang=spectre
parameters p1=1 p2=2           // declare some parameters
r1 1 0 resistor r=p1           // use a parameter, value=1
r2 1 0 resistor r=p1+p2        // use parameters in an expression, value=3
x1 s1 p4=8                     // subckt "s1" is defined below, pass in value 8 for "p4"
subckt s1
  parameters p1=4 p3=5 p4=6    // note: no "p2" here, p1 "redefined"
  r1 1 0 resistor r=p1         // local definition used: value=4
  r2 1 0 resistor r=p2         // inherit from parent(top-level) value=2
  r3 1 0 resistor r=p3         // use local definition, value=5
  r4 1 0 resistor r=p4         // use passed-in value, value=8
  r5 1 0 resistor r=p1+p2/p3   // use local+inherited/local=(4+2/5)=4.4
ends
time_sweep tran start=0 stop=(p1+p2)*50e-6 // use 5*50e-6 = 150 us
dc_sweep dc param=p1 values=[0.5 1 +p2 (sqrt(p2*p2)) ] // sweep p1
```

Parameter Declaration

Parameters can be declared anywhere in the top-level circuit description or on the first line of a subcircuit definition. Parameters must be declared before they are used (referenced).

Multiple parameters can be declared on a single line. When parameters are declared in the top-level, their values are also specified. When parameters are declared within subcircuits,

their default values are specified. The value or default value for a parameter can be a constant, expression, a reference to a previously defined parameter, or any combination of these.

You can declare parameters between subcircuit definitions if the subcircuits do not refer to parameters in the parent scope defined after the subcircuit definition. If you want to use `altergroups`, you must declare all parameters before the subcircuit definitions.

Parameter Inheritance

Subcircuit definitions inherit parameters from their parent (enclosing subcircuit definition, or top-level definition). This inheritance continues across all levels of nesting of subcircuit definitions; that is, if a subcircuit `s1` is defined, which itself contains a nested subcircuit definition `s2`, then any parameters accessible within the scope of `s1` are also accessible from within `s2`. Also, any parameters declared within the top-level circuit description are also accessible within both `s1` and `s2`. However, any subcircuit definition can redefine a parameter that it inherited. In this case, if no value is specified for the redefined parameter when the subcircuit is instantiated, then the redefined parameter uses the locally defined default value, rather than inheriting the actual parameter value from the parent. See how the `r2` resistor is used in the examples in [Circuit and Subcircuit Parameters](#) on page 171.

Parameter Referencing

Spectre netlist parameters can be referenced anywhere that a numeric value is normally specified on the right-hand side of an `=` sign or within a vector, where the vector itself is on the right-hand side of an `=` sign. This includes referencing of parameters in expressions (run `spectre -h expressions` for more details on netlist expression handling), as indicated in the preceding examples. You can use expressions containing parameter references when specifying component or analysis parameter values (for example specifying the resistance of a resistor or the stop time of a transient analysis, as outlined in the preceding example), when specifying model parameter values in model statements (for example specifying `bf=p1*0.8` for a bipolar model parameter, `bf`), or when specifying initial conditions and nodesets for individual circuit nodes.

Altering/Sweeping Parameters

Just as certain Spectre analyses (such as `sweep`, `alter`, `ac`, `dc`, `noise`, `sp`, and `xf`) can sweep component instance or model parameters, they can also sweep netlist parameters. Run `spectre -h analysis` to see the particular details for any of these analyses, where `analysis` is the analysis of interest.

Expressions

An expression is a construct that combines operands with operators to produce a result that is a function of the values of the operands and the semantic meaning of the operators. Any legal operand is also an expression in itself. Legal operands include numeric constants and references to top-level netlist parameters or subcircuit parameters. Calls to algebraic and trigonometric functions are also supported. The complete lists of operators, algebraic, and trigonometric functions are given after some examples.

The following are examples:

```
simulator lang=spectre
parameters p1=1 p2=2           // declare some top-level parameters
r1 (1 0) resistor r=p1         // the simplest type of expression
r2 (1 0) resistor r=p1+p2      // a binary (+) expression
r3 (1 0) resistor r=5+6/2      // expression of constants, = 8
x1 s1 p4=8 // instantiate a subcircuit, defined in the following lines
subckt s1
parameters p1=4 p3=5 p4=p1+p3 // subcircuit parameters
  r1 (1 0) resistor r=p1       // another simple expression
  r2 (1 0) resistor r=p2*p2    // a binary multiply expression
  r3 (1 0) resistor r=(p1+p2)/p3 // a more complex expression
  r4 (1 0) resistor r=sqrt(p1+p2) // an algebraic function call
  r5 (1 0) resistor r=3+atan(p1/p2) // a trigonometric function call
  r6 (1 0) RESMOD r=(p1 ? p4+1 : p3) // the ternary operator
ends
// a model statement, containing expressions
model RESMOD resistor tc1=p1+p2 tc2=sqrt(p1*p2)
// some expressions used with analysis parameters
time_sweep tran start=0 stop=(p1+p2)*50e-6 // use 5*50e-6 = 150 us
// a vector of expressions (see notes on vectors below)
dc_sweep dc param=p1 values=[0.5 1 +p2 (sqrt(p2*p2))] // sweep p1
```

Where Expressions Can Be Used

The Spectre Netlist Language allows expressions to be used where numeric values are expected on the right-hand side of an = sign or within a vector, where the vector itself is on the right-hand side of an = sign. Expressions can be used when specifying component or analysis instance parameter values (for example, specifying the resistance of a resistor or the stop time of a transient analysis, as outlined in the preceding example), when specifying model parameter values in model statements (for example, specifying $bf=p1*0.8$ for a bipolar model parameter, *bf*), or when specifying initial conditions and nodesets for individual circuit nodes.

Operators

The operators in the following table are supported, listed in order of decreasing precedence. Parentheses can be used to change the order of evaluation. For a binary expression like $a+b$, a is the first operand and b is the second operand. All operators are left associative, with the exceptions of the “to the power of” operator ($**$) and the ternary operator ($? :$), which are right associative. For logical operands, any nonzero value is considered true. The relational and equality operators return a value of 1 to indicate true or 0 to indicate false. There is no short-circuiting of logical expressions involving $\&\&$ and $| |$.

Operator	Symbol(s)	Value
Unary +, Unary –	+, –	Value of the operand, negative of the operand.
To the power of	**	First operand to be raised to the power of the second operand.
Multiply, Divide	*, /	Product, quotient of the operands.
Binary Plus/Minus	+, –	Sum, difference of the operands.
Shift	<<, >>	First operand shifted left by the number of bits specified by the second operand; first operand shifted right by the number of bits specified by the second operand.
Relational	<, <=, >, >=	Less than, less than or equal, greater than, greater than or equal, respectively.
Equality	==, !=	True if the operands are equal; true if the operands are not equal.
Bitwise AND	&	Bitwise AND (of integer operands).
Bitwise Exclusive NOR	~^ (or ^~)	Bitwise exclusive NOR (of integer operands).
Bitwise OR		Bitwise OR (of integer operands).
Bitwise Exclusive OR	^	Bitwise exclusive OR (of integer operands).
Bitwise NOT	~	Bitwise NOT (of integer operand).
Logical AND	&&	True only if both operands true.
Logical OR		True if either operand is true.

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Operator	Symbol(s)	Value
Conditional selection	$(cond) ? x : y$	Returns x if $cond$ is true, y if not; where x and y are expressions.

Algebraic and Trigonometric Functions

The trigonometric and hyperbolic functions expect their operands to be specified in radians. The `atan2()` and `hypot()` functions are useful for converting from Cartesian to polar form.

Function	Description	Domain
<code>log(x)</code>	Natural logarithm	$x > 0$
<code>log10(x)</code>	Decimal logarithm	$x > 0$
<code>exp(x)</code>	Exponential	$x < 80$
<code>sqrt(x)</code>	Square root	$x > 0$
<code>min(x, y)</code>	Minimum value	All x , all y
<code>max(x, y)</code>	Maximum value	All x , all y
<code>abs(x)</code>	Absolute value	All x
<code>pow(x, y)</code>	x to the power of y	All x , all y
<code>sin(x)</code>	Sine	All x
<code>cos(x)</code>	Cosine	All x
<code>tan(x)</code>	Tangent	All x , except $x = n \cdot (\pi/2)$, where n is odd
<code>asin(x)</code>	Arc-sine	$-1 \leq x \leq 1$
<code>acos(x)</code>	Arc-cosine	$-1 \leq x \leq 1$
<code>atan(x)</code>	Arc-tangent	All x
<code>atan2(x, y)</code>	Arc-tangent of x/y	All x , all y
<code>hypot(x, y)</code>	$\sqrt{x^2 + y^2}$	All x , all y
<code>sinh(x)</code>	Hyperbolic sine	All x
<code>cosh(x)</code>	Hyperbolic cosine	All x
<code>tanh(x)</code>	Hyperbolic tangent	All x
<code>asinh(x)</code>	Arc-hyperbolic sine	All x

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Function	Description	Domain
<code>acosh(x)</code>	Arc-hyperbolic cosine	$x \geq 1$
<code>atanh(x)</code>	Arc-hyperbolic tangent	$-1 \leq x \leq 1$
<code>int(x)</code>	Integer part of x (number before the decimal)	
<code>ceil(x)</code>	Smallest integer greater than or equal to x	All x
<code>floor(x)</code>	Largest integer less than or equal to x	All x
<code>fmod(x, y)</code>	Floating-point remainder of x/y	$y \neq 0$

Using Expressions in Vectors

Expressions can be used as vector elements, as in the following example:

```
dc_sweep dc param=p1 values=[0.5 1 +p2 (sqrt(p2*p2)) ] // sweep p1
```

Note: When expressions are used within vectors, anything other than constants, parameters, or unary expressions (unary +, unary -) must be surrounded by parentheses. Vector elements should be space separated. The preceding `dc_sweep` example shows a vector of four elements: 0.5, 1, +p2, and `sqrt(p2*p2)`. Note that the square root expression is surrounded by parentheses.

Behavioral Expressions

Behavioral source enables you to model a resistor, inductor, capacitor, voltage or current source as a behavioral component. Using `bsource`, you can express the value of a resistance, capacitance, voltage or current as a combination of device operating points, node voltages, branch currents, and built in Spectre® circuit simulator expressions. `bsource` simulation performance has now been improved by compiling the `bsource` devices. This is explained in more detail in the `bsource` compilation section below.

The syntax for `bsource` is:

```
name (node1 node2) bsource behav_param param_list
```

where *behav_param* can be

<i>c=simple_expr</i>	Capacitance between the nodes.
<i>g=simple_expr</i>	Conductance between the nodes.
<i>i=generic_expr</i>	Current through bsource.
<i>l=simple_expr</i>	Inductance between the nodes.
<i>phi=simple_expr</i>	Flux in the bsource device.
<i>q=simple_expr</i>	Charge in bsource.
<i>r=simple_expr</i>	Resistance between the nodes.
<i>v=generic_expr</i>	Voltage across bsource.
<i>simple_expr</i>	A Spectre expression containing: ■ netlist parameters ■ current simulation time, \$time ■ current frequency, \$freq ■ node voltages, $v(a,b)$ where <i>a</i> and <i>b</i> are nodes or in the netlist or $v(a)$ which is the voltage between node <i>a</i> and ground. Note: In case of a bsource resistor, if <i>simple_expression</i> is of the form a/b, where $b=0$, then bsource clamps the value to $a*1e5$. For example, the value of Res1 will be clamped to $1e5$ in the following expression: <pre>Res1 (vdd2 0) resistor r=1/v(0);</pre> The resistor value can be controlled by using the global options <i>rclamp</i> and <i>rcut</i>. Refer to the <i>Spectre Circuit Simulator Reference</i> manual for more information on these options. ■ branch currents, $i("inst\_id:index")$, where <i>inst_id</i> is an instance name given in the netlist and <i>index</i> is the port index. The default value for index is 0.

For more information, type `spectre -h expressions` in a terminal window.

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`generic_expr` A simple expression that may contain `idt()` or `ddt()` as well.

`param_list` is `param_name=value`

`param_name` can be

Multiplicity factor

`m` The value of `m` defaults to 1.

Note: When `m` is greater than 1, Spectre reports the current as the sum of all `m` parallel devices for all elements except voltage sources. For voltage sources, Spectre reports the current for `m=1` only. This is because voltage sources are also used in current-controlled sources and there the requirement is to use the current from `m=1`.

Spectre reports the power for all elements as the sum of all `m` parallel devices.

Temperature Parameters

`tc1` Linear temperature co-efficient. Valid for all behavioural elements.
Default value is 0 1/C.

`tc2` Quadratic temperature co-efficient. Valid for all behavioural elements.
Default value is 0 C²

`temp` Parameter for ambient temperature. Valid for all behavioral elements. Default value is \$temperature - 273.15.

`tnom` Parameters measurement temperature. Valid for all behavioural elements.
Default value is 0.0.

`trise` Temperature rise for ambient. Valid for all behavioural elements.
Default value is 0.0

`T` Effective value of temperature. Valid for all behavioral elements. Default value is `temp+trise-tnom`.

`tc1c` Linear temperature coefficient of capacitor. Valid for resistor type behavioral element. Default value is 0 1/C.

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`tc2c` Quadratic temperature coefficient of capacitor. Valid for resistor type behavioral element. Default value is 0 C⁻².

Clipping Parameters

`max_val` Maximum value of bsource expression. Valid for all behavioural elements, but generally used with `i` and `v` elements for clipping the current or voltage between the specified values.

`min_val` Minimum value of bsource expression. Valid for all behavioural elements, but generally used with `i` and `v` elements for clipping the current or voltage between the specified values.

`bv_max` Generate a warning when bsource voltage of two terminals exceeds the value specified by `bv_max`. Valid for resistor and capacitor.

Noise Parameters

`af` Flicker noise exponent. Valid for `r` and `g` elements. Default value is 2.

`fexp` Flicker noise frequency exponent. Valid for `r`, `g`, `v`, and `i` elements. Default value is 1.

`ef` Alias of `fexp`.

`ldexp` Flicker (1/f) noise L exponent. Valid for `r` and `g` elements. Default value is 1.0.

`lf` Alias of `ldexp`.

`wdexp` Flicker (1/f) noise W exponent. Valid for `r` and `g` elements. Default value is 1.0.

`wf` Alias of `wdexp`.

`isnoisy` Specifies whether to generate noise. Valid for `r`, `g`, `i`, and `v` elements. Valid values are `yes` and `no`. Default value is `yes`.

`kf` Flicker noise co-efficient. Valid for `r` and `g` elements.

`white_noise` White noise expression. Valid for `v` and `i` elements.

`flicker_noise` Flicker noise expression. Valid for `v` and `i` elements.

where

Element	is a bsource with
r	resistance specified.
g	conductance specified.
v	voltage specified.
i	current specified.

All the parameters in the `param_name` table are instance parameters. *white_noise* and *flicker_noise* may be assigned behavioural expressions; the other parameters must be assigned constant or parametric expressions.

A bsource can also be declared as an instance of a model of a resistor, inductor, or capacitor. However, the behavioral expression can only be present on the instance of the model and not on the model itself.

Example:

```
simulator lang=spectre
vsrc s 0 vsource type=sine ampl=500.0 freq=100k
// declare a model of a resistor
model model_res resistor tc1=0.01 tc2=0.003
// declare an instance of the above model with a behavioral expression assigned to
//the r parameter
res1 s 0 model_res r=100*(1+(1/2)*v(s,0)+(1/3)*pow(v(s,0),2)) tc1=0.01
tran1 tran stop=50u
```

A bsource can also refer to the current of another instance. For example:

```
Ibsrc2 (0 net01) bsource i=i("Imon:1")
```

In such cases, the instances are searched as follows:

- If the name of the referenced instance starts with a dot (.), the tool searches for the instance at the top level and generates an error if the instance is not found. For example:

```
Ibsrc2 (0 out) bsource i=i(".Imon:1").
```
- If the name of the referenced instance contains a dot (.), the tool first searches for the instance at the top level. If the instance is not found at the top level, it searches for the instance at the local level. For example:

```
Ibsrc2 (0 out) bsource i=i("Iinst.Imon:1")
```
- For any other scenario, the tool first searches for the referenced instance at the local level and then the top level.

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Here is an example:

```
subckt INVDD0BWP I ZN VDD VSS
    M1 (ZN I VSS VSS) nch_mac l=40n w=155.00n multi=1
    M0 (ZN I VDD VDD) pch_mac l=40n w=205.00n multi=1
ends INVDD0BWP
// End of subcircuit definition.

subckt sim_bsource_inst out
    Ibsrc2 (0 out) bsource i=i(".Imon:1")
    V4 (net2 0) vsource dc=1.1 type=dc
    Ibsrc3 (0 out) bsource i=i("Imon:1")
    Ibsrc4 (0 out) bsource i=i("Imon.M1:1")
    Imon (0 net010 DVDD1P1 DGND) INVDD0BWP
ends sim_bsource_inst
// End of subcircuit definition.

// Library name: zz_sadayoshi_ban
// Cell name: sim_bsource
// View name: schematic_case3
Imon (0 net010 DVDD1P1 DGND) INVDD0BWP
Iinst (net02) sim_bsource_inst
```

In the above example:

Iinst.Ibsrc2 reference will find Imon.

Iinst.Ibsrc3 reference will find Iinst.Imon.

Iinst.Ibsrc4 reference will find Imon.M1.

Altergroup is not supported for models that have behavioral instances.

Parameters Supported

A model that is to be instantiated as a behavioral resistor, capacitor or inductor, can only have those parameters that are already supported for these behavioral primitives. The list of supported parameters is given below. Some of these parameters may only be allowed on instances. For those parameters that are valid on both the instance and model levels, the instance parameter is given priority if it is specified on both the model and the instance of the model.

Resistor

bsource supports `isnoisy`, `m`, `r`, `tc1`, `tc2`, `trise`, `kf`, `af`, `fexp`, `ldexp`, `wdexp`, `l`, `w`, `mr`, `tc1c`, `tc2c`.

The resistor type bsource model has two capacitors between each ports with ground. The parameter `tc1c` is the first-order temperature parameter of that capacitor, and `tc2c` is the second-order temperature parameter.

The final capacitor value is $C = C_0 * (1 + tc1c * T + tc2c * T * T)$, where T is the temperature, C_0 is capacitor when T is 0.

Capacitor

bsource supports `c`, `m`, `tc1`, `tc2`, `ic`, `trise`, and `ctype`.

Inductor

bsource supports `l`, `m`, `tc1`, `tc2`, and `trise`.

Examples of bsource

Nonlinear Resistor/Capacitor/Inductor Instance

```
res (n1 n2) bsource r=100*(1+(1/2)*v(n1,n2))
cond (n1 n2) bsource g=0.01*(1+(1/2)*v(n1,n2))
cap (n1 n2) bsource c=1.0e-6*(1+(1/2)*v(n1,n2))
ind (n1 n2) bsource l=0.1*(1+(1/2)*v(n1,n2))
```

Charge Model for Capacitor

```
cap (n1 n2) bsource q=1.0e-6*v(n1,n2)
```

Magnetic Flux Model for Inductor

```
ind (n1 n2) bsource phi=0.1*i(n1,n2)
```

Voltage and Current (Sinewave) Source

```
vsrc (n1 n2) bsource v=10.0*sin(2*pi*freq*$time)
isrc (n1 n2) bsource i=1.0e-3*sin(2*pi*freq*$time)
```

Current Controlled Current Sources

```
vsrc (n1 n2) vsource v=10
cccs1 (n3 n4) bsource i=gain*i("vsrc:0")
```

Current Controlled Voltage Sources

```
vsrc (n1 n2) vsource v=10
ccvsl (n3 n4) bsource v=100*i("vsrc:0")
```

Voltage Controlled Voltage Source

```
vsrc (n1 n2) resistor r=100k
vcvsl (n3 n4) bsource v=gain*v(n1,n2)
```

Voltage Controlled Current Source

```
vsrc (n1 n2) resistor r=100k
vcvsl (n3 n4) bsource i=v(n1,n2)/2000.0
```

Giving Maximum and Minimum Range for an Expression

```
res (n1 n2) bsource r=100*(1+(1/2)*v(n1,n2)) max_val=105 min_val=95
```

Giving Temperature Co-efficient for Resistor

```
res (n1 n2) bsource r=100 tc1=0.01 tc2=0.003 trise=10 tnom=30
```

Giving Flicker Noise Co-efficient for Resistor

```
res (n1 n2) bsource r=100 kf=1 af=1 fexp=1
```

Doing Altergroup with Bsource

```
vsrcl (n1 n2) bsource v=10*sin(2*pi*freq1*$time)
vsrcl2 (n3 n4) bsource v=10*cos(2*pi*freq2*$time)
cccs1 (n5 n6) bsource i=gain*i("vsrcl:0")
res (n5 n6) bsource r=100*(1+(1/2)*v(n5,n6))
tran1 tran stop=1u
altAnal altergroup {
cccs1 (n5 n6) bsource i=gain*i("vsrcl2:0")
res (n5 n6) bsource r=100*(1+(1/3)*pow(v(n5,n6),2))
}
tran2 tran stop=1u
```

bsource Compilation

Spectre automatically translates bsource components into verilogA models for simulation. As such, they are compiled prior to simulation just like any other verilogA model.

Built-in Constants

You can use built-in constants to specify parameter values.

The Spectre Netlist Language contains the built-in mathematical and physical constants listed in the following table. Mathematical constants start with **M_**, and physical constants start with **P_**.

Constant Name	Value	Description
M_E	2.7182818284590452354	e or escp(1)
M_LOG2E	1.4426950408889634074	log2(e)
M_LOG10E	0.43429448190325182765	log10(e)
M_LN2	0.69314718055994530942	ln(2)
M_LN10	2.30258509299404568402	ln(10)
M_PI	3.14159265358979323846	π
M_TWO_PI	6.28318530717958647652	2π
M_PI_2	1.57079632679489661923	$\pi/2$
M_PI_4	0.78539816339744830962	$\pi/4$
M_1_PI	0.31830988618379067154	$1/\pi$
M_2_PI	0.63661977236758134308	$2/\pi$
M_2_SQRTPI	1.12837916709551257390	$2/\pi$
M_SQRT2	1.41421356237309504880	$\sqrt{2}$
M_SQRT1_2	0.70710678118654752440	$\sqrt{1/2}$
M_DEGPERRAD	57.2957795130823208772	Number of degrees per radian (equal to $180/\pi$)
P_Q	$1.6021918 \times 10^{-19}$	Charge of electron in coulombs

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Constant Name	Value	Description
P_C	2.997924562×10^8	Speed of light in vacuum in meters/second
P_K	$1.3806226 \times 10^{-23}$	Boltzman's constant in joules/Kelvin
P_H	$6.6260755 \times 10^{-34}$	Planck's constant in joules times seconds
P_EPS0	$8.85418792394420013968 \times 10^{-12}$	Permittivity of vacuum in farads/meter
P_U0	$\pi \times (4.0 \times 10^{-7})$	Permeability of vacuum in henrys/meter
P_CELSIUS0	273.15	Zero Celsius in Kelvin

User-Defined Functions

The user-defined function capability allows you to build upon the provided set of built-in mathematical and trigonometric functions. You can write your own functions and call these functions from within any expression. The Spectre function syntax resembles that of C.

Defining the Function

The following is a simple example of defining a function with arguments of type real and results of type real:

```
real myfunc( real a, real b ) {  
    return a+b*2+sqrt(a*sin(b));  
}
```

When you define a function, follow these rules:

- Functions can be declared only at the top level and cannot be declared within subcircuits.
- Arguments to user-defined functions can only be real values, and the functions can only return real values. You must use the keyword `real` for data typing.
- The Spectre function syntax does not allow references to netlist parameters within the body of the function, unless the netlist parameter is passed in as a function argument.
- The function must contain a single `return` statement.

Note: If you create a user-defined function with the same name as a built-in function, the Spectre simulator issues a warning and runs the user-defined function.

Calling the Function

Functions can be called from anywhere that an expression can currently be used in the Spectre simulator. Functions can call other functions; however, the function must be declared *before* it can be called. The following example defines the function `myfunc` and then calls it:

```
real myfunc( real a, real b ) {  
    return a+b*2+sqrt(a*sin(b));  
}  
  
real yourfunc( real a, real b ) {  
    return a+b*myfunc(a,b); // call "myfunc"  
}
```

The next example shows how a user-defined function can be called from an expression in the Spectre netlist:

```
r1 (1 0) resistor r=myfunc(2.0, 4.5)
```

Predefined Netlist Parameters

There are two predefined netlist parameters:

- `temp` is the circuit temperature (in degrees Celsius) and can be used in expressions.
- `tnom` is the *measurement (nominal)* temperature (in degrees Celsius) and can be used in expressions.

For example:

```
r1 1 0 res r=(temp-tnom)*15+10k  
o1 options TEMP=55
```

For behavioral expressions, the values of `temp` and `tnom` are specified by the Spectre circuit simulator rather than being passed by the netlist.

Note: If you change `temp` or `tnom` using a `set` statement, `alter` statement, or simulator options card, all expressions with `temp` or `tnom` are reevaluated. Hence, you can use the `temp` parameter for temperature-dependent modeling (this does not include self-heating, however).

Subcircuits

The Spectre simulator helps you simplify netlists by letting you define subcircuits that you can place any number of times in the circuit. You can nest subcircuits, and a subcircuit definition can contain both instances and definitions of other subcircuits. The main applications of subcircuits are to describe the circuit hierarchy and to perform parameterized modeling. In this section, you learn to define subcircuits and to call them into the main circuit.

Formatting Subcircuit Definitions

You format subcircuit definitions as follows:

```
subckt SubcircuitName ([ node1 ... nodeN ])
    [ parameters name1=value1 ... [nameN=valueN]
    .
    .
    .
    instance, model, ic, or nodeset statements—or
      further subcircuit definitions
    .
    .
    .
ends [SubcircuitName]
```

<code>subckt</code>	The keyword <code>subckt</code> (<code>.subckt</code> is used in SPICE mode).
<code>SubcircuitName</code>	The unique name you give to the subcircuit. Note: The subcircuit name cannot start with a number. For example, if you specify <code>100_sub1</code> as the subcircuit name, the simulator will issue a warning message.
<code>(node1...nodeN)</code>	The external or connecting nodes of the subcircuit to the main circuit.
<code>parameters</code> <code>name1=value1...nameN=</code>	This is an optional parameter specification field. You can specify default values for subcircuit calls that refer to this subcircuit. The field contains the keyword <code>parameters</code> followed by the names and values of the parameters you want to specify.
<code>component</code> <code>instance</code> <code>statement</code>	The instance statements of your subcircuit, other subcircuit definitions, component statements, analysis statements, or <code>model</code> statements.
<code>ends</code> <code>SubcircuitName</code>	The keyword <code>ends</code> (or <code>.ends</code> in SPICE mode), optionally followed by the subcircuit name.

A Subcircuit Definition Example

The following subcircuit named `twisted` models a twisted pair. It has four terminals—`p1`, `n1`, `p2`, and `n2`. The parameter specification field for the subcircuit sets subcircuit call default values for parameters `zodd`, `zeven`, `veven`, `vodd`, and `len`. Remember that the specified parameters are defaults for subcircuit calls, not for the instance statements in the subcircuit. For example, if the subcircuit call leaves the `zodd` parameter unspecified, the value of `zodd` in `odd` is 50. If, however, the subcircuit call sets `zodd` to 100, the value of `zodd` in `odd` is 100.

```
subckt twisted (p1 n1 p2 n2)
  parameters zodd=50 zeven=50 veven=1 vodd=1 len=0
  odd (p1 n1 p2 n2) tline z0=zodd vel=vodd len=len
  tf1a (p1 0 e1 c1) transformer t1=2 t2=1
  tf1b (n1 0 c1 0) transformer t1=2 t2=1
  even (e1 0 e2 0) tline z0=zeven vel=veven len=len
  tf2a (p2 0 e2 c2) transformer t1=2 t2=1
  tf2b (n2 0 c2 0) transformer t1=2 t2=1
ends twisted
```

Indenting the contents of a subcircuit definition is not required. However, it is recommended to make the subcircuit definition more easily identifiable.

Subcircuit Example

```
GaAs Traveling Wave Amplifier
// GaAs Traveling-wave distributed amplifier (2-26.5GHz)
// Designed by Jerry Orr, MWTD Hewlett-Packard Co.
// 1986 MTT symposium; unpublished material.

global gnd vdd
simulator lang=spectre

// Models
model nGaAs gaas type=n vto=-2 beta=0.012 cgs=.148p cgd=.016p fc=0.5

subckt cell (o g1 g2)
  TL (o gnd d gnd) tline len=355u vel=0.36
  Gt (d g2 s) nGaAs
  Ctgd (d s) capacitor c=0.033p
  Cgg (g2 gnd) capacitor c=3p
  Gb (s g1 gnd) nGaAs
  Cbgd (s gnd) capacitor c=0.033p
  Ro (d c) resistor r=4k
  Co (c gnd) capacitor c=0.165p
ends cell

subckt stage (i0 o8)
  // Devices
  Q1 (o1 i1 b2) cell
  Q2 (o2 i2 b2) cell
  Q3 (o3 i3 b2) cell
  Q4 (o4 i4 b2) cell
  Q5 (o5 i5 b2) cell
  Q6 (o6 i6 b2) cell
  Q7 (o7 i7 b2) cell
```


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```
// Transmission lines
TLi1 (i0 gnd i1 gnd) tline len=185u z0=96 vel=0.36
TLi2 (i1 gnd i2 gnd) tline len=675u z0=96 vel=0.36
TLi3 (i2 gnd i3 gnd) tline len=675u z0=96 vel=0.36
TLi4 (i3 gnd i4 gnd) tline len=675u z0=96 vel=0.36
TLi5 (i4 gnd i5 gnd) tline len=675u z0=96 vel=0.36
TLi6 (i5 gnd i6 gnd) tline len=675u z0=96 vel=0.36
TLi7 (i6 gnd i7 gnd) tline len=675u z0=96 vel=0.36
TLi8 (i7 gnd i8 gnd) tline len=340u z0=96 vel=0.36
TLo1 (o0 gnd o1 gnd) tline len=360u z0=96 vel=0.36
TLo2 (o1 gnd o2 gnd) tline len=750u z0=96 vel=0.36
TLo3 (o2 gnd o3 gnd) tline len=750u z0=96 vel=0.36
TLo4 (o3 gnd o4 gnd) tline len=750u z0=96 vel=0.36
TLo5 (o4 gnd o5 gnd) tline len=750u z0=96 vel=0.36
TLo6 (o5 gnd o6 gnd) tline len=750u z0=96 vel=0.36
TLo7 (o6 gnd o7 gnd) tline len=750u z0=96 vel=0.36
TLo8 (o7 gnd o8 gnd) tline len=220u z0=96 vel=0.36

// Bias network
// drain bias
Ldd (vdd o0) inductor l=1u
R1 (o0 b1) resistor r=50
C1 (b1 gnd) capacitor c=9p
// gate 2 bias
R2 (b1 b2) resistor r=775
R3 (b2 gnd) resistor r=465
C2 (b2 gnd) capacitor c=21p
// gate 1 bias
R4 (i8 b3) resistor r=50
R5 (b3 gnd) resistor r=500
C3 (b3 gnd) capacitor c=12p

ends stage

// Two stage amplifier
P1 (in gnd) port r=50 num=1 mag=0
Cin (in in1) capacitor c=1n
X1 (in1 out1) stage
Cmid (out1 in2) capacitor c=1n
X2 (in2 out2) stage
Cout (out2 out) capacitor c=1n
P2 (out gn) port r=50 num=2

// Power Supply
Vpos vdd gnd vsorce dc=5

// Analyses
OpPoint dc
Sparams sp start=100M stop=100G dec=100
```

Rules to Remember

When you use subcircuits,

- You must place the same number of nodes in the same order in subcircuit definitions and their respective subcircuit calls.

- Models and subcircuits defined within a subcircuit definition are accessible only from within that subcircuit. You cannot use the model names in a subcircuit definition in statements from outside the subcircuit. You can, however, use both the model name and the subcircuit definitions in new subcircuits within the original subcircuit. Local models or subcircuits hide nodes or subcircuits with the same names defined outside the subcircuit.
- When you use model statements within subcircuit definitions, where model parameters are expressions of subcircuit parameters definitions, a new model is created for every instance of the subcircuit. These different models are “expanded models,” which are derived from the original `model` statement. Each of the new models has a unique name, and component instances created from the original `model` statement are instances of the new model created for the subcircuit. The full name of each new model is the flattened name of the subcircuit, followed by a dot (.), followed by the name of the model as given in the `model` statement. If you request the output of model data, you can see these expanded models in the output.
- Subcircuit parameter names are local only. You cannot access the value of a subcircuit parameter outside of the scope of the subcircuit in which it was declared.
- Parameter names must be lowercase if you want to instantiate components from SPICE mode.

Calling Subcircuits

To call a subcircuit, place an instance statement in your netlist. The nodes for this instance statement are the connections to the subcircuit, and the master field in the subcircuit call contains the name of the subcircuit. You can enter parameters in a subcircuit call to override the parameters in the subcircuit definition for that subcircuit call.

The following example shows a subcircuit call and its corresponding subcircuit definition. `cell` is the name of the subcircuit being called; `Q1` is the unique name of the subcircuit call; and `o1`, `i1`, and `b2` are the connecting nodes to the subcircuit from the subcircuit call. When you call the subcircuit, the Spectre simulator substitutes these connecting node names in the subcircuit call for the connecting nodes in the subcircuit definition: `o1` is substituted for `o`, `i1` is substituted for `g1`, and `b2` is substituted for `g2`. The length of transmission line `TL` is changed to 500 μm for this subcircuit call from its 355 μm default value in the subcircuit definition.

```

Q1 (o1 i1 b2) cell length=500um
    |
    | Subcircuit call
    |
subckt cell (o g1 g2)
    |
    | Substitutions
    |
parameters length=355um
    
```

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```
TL o gnd d gnd tline len=length vel=0.36
Gt d g2 s nGaAs
Ctgd d s capacitor c=0.033p
Cgg g2 gnd capacitor c=3p
Gb s g1 gnd nGaAs
Cbgd s gnd capacitor c=0.033p
Ro d c resistor r=10k
Co c gnd capacitor c=0.165p

ends cell
```

Modifying Subcircuit Parameter Values

The following example is a passive Bessel three-pole bandpass filter with default parameter values for bandwidth, termination resistance, and center frequency. The `bw`, `r0`, and `fc` parameters are given default values in the subcircuit, but you can change these values when you call the subcircuit. Changing the value of `bw`, `r0`, and `fc` in a subcircuit call changes the values of many parameters in instance statements that refer to these three parameters.

```
// define passive 3-pole bandpass filter
subckt filter (n1 n2)
  parameters bw=1 r0=1 fc=1
  C1 (n1 0) capacitor c=0.3374 / (6.2832 * bw * r0)
  L1 (n1 0) inductor l=(r0 * bw) / (0.3374 * 6.2832 * fc * fc)
  C2 (n1 n12) capacitor c=bw / (0.9705 * 6.2832 * fc * fc * r0)

  L2 (n12 n2) inductor l=(r0 * 0.9705) / (6.2832 * bw)
  C3 (n2 0) capacitor c=2.2034 / (6.2832 * bw * r0)
  L3 (n2 0) inductor l=(r0 * bw) / (2.2034 * 6.2832 * fc * fc)
ends filter

// instantiate 50 Ohm filter with 10.4MHz
// center frequency and 1MHz bandwidth
F1 (in out) filter bw=1MHz fc=10.4MHz r0=50
// instantiate 1 Ohm filter with 10Hz
// center frequency and 1Hz bandwidth
F2 (n1 n2) filter fc=10
```

Parameter values changed from defaults for these subcircuit calls

You can use such parameterized subcircuits when the Spectre simulator is reading either Spectre or SPICE syntax. Unlike subcircuit calls in SPICE, the names of Spectre subcircuit calls do not have to start with an `x`. This is useful if you want to replace individual components in an existing netlist with subcircuits for more detailed modeling.

Checking for Invalid Parameter Values

When you define subcircuits such as the one in [Modifying Subcircuit Parameter Values](#) on page 191, you might want to put error checking on the subcircuit parameter values. Such error checking prevents you from entering invalid parameter values for a given subcircuit call.

The Spectre `paramtest` component lets you test parameter values and generate necessary error, warning, and informational messages. For example, in the example of the bandpass filter in [Modifying Subcircuit Parameter Values](#) on page 191, the center frequency needs to be greater than half the bandwidth.

Here is a version of the previous three-pole filter that issues an error message if the center frequency is less than or equal to half the bandwidth:

```
* define passive 3-pole bandpass filter
subckt filter (n1 n2)
  parameters bw=1 r0=1 fc=1

  checkFreqs paramtest errorif=((bw/2-fc)>=0) \ ← paramtest
                                                component

  message="center frequency must be greater than half the
    bandwidth"
  C1 n1 0 capacitor c=0.3374 / (6.2832 * bw * r0)
  L1 n1 0 inductor l=(r0 * bw) / (0.3374 * 6.2832 * fc * fc)
  C2 n1 n12 capacitor c=bw / (0.9705 * 6.2832 * fc * fc * r0)
  L2 n12 n2 inductor l=(r0 * 0.9705) / (6.2832 * bw)
  C3 n2 0 capacitor c=2.2034 / (6.2832 * bw * r0)
  L3 n2 0 inductor l=(r0 * bw) / (2.2034 * 6.2832 * fc * fc)
ends filter
```

The `paramtest` component `checkFreqs` has no terminals and no effect on the simulation results. It monitors its parameters and issues a message if a given condition is satisfied by evaluating to a nonzero number. In this case, `errorif` specifies that the Spectre simulator issues an error message and stops the simulation. If you specify `printf`, the Spectre simulator prints an informational message and continues the simulation. If you specify `warnif`, the Spectre simulator prints a warning and continues.

For more information about specific parameters available with the `paramtest` component, see the parameter listings in the Spectre online help (`spectre -h`).

Enabling/Disabling Noise in Subcircuits

You can enable or disable noise in subcircuit instances by using the global `noiseon_inst` and `noiseoff_inst` options or the `isnoisy` parameter.

Note: The global `noiseon_inst` and `noiseoff_inst` options, if specified for the same instance, override the settings of the `isnoisy` parameter.

The `isnoisy` parameter can be specified in both subcircuit definitions and subcircuit instances. However, if the parameter is specified in both, the `isnoisy` parameter specified in the subcircuit instance gets higher priority. If the `isnoisy` parameter is also specified for a device instance, it gets the highest priority. In addition, if the `isnoisy` parameter is

specified at different hierarchy levels, the parameter at the higher hierarchy level gets higher priority.

Example1

```
subckt sub1 a b
    parameters isnoisy=no
    r1 a b 1k
ends
X1 1 0 sub1 isnoisy=yes
X2 1 0 sub1
X3 1 0 sub1 isnoisy=no
```

In the above example, noise will be enabled in X1.

Example 2

```
subckt sub1 a b
    parameters isnoisy=no
    X1 a 1 sub2 isnoisy=yes
    X2 1 b sub2
ends
subckt sub2 a b
    R1 a b 1K
ends
X1 1 0 sub1
```

In the above example, noise in X1.X1 will be enabled whereas noise in X1.X2 will be disabled.

Example3

```
subckt sub1 a b
    parameters isnoisy=no
    X1 a 1 sub2
    X2 1 b sub3
ends
subckt sub2 a b
    parameters isnoisy=yes
    R1 a b 1K
ends
subckt sub3 a b
    R1 a b 1K
ends
X1 1 0 sub1
```

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In the above example, noise in `X1.X1` will be enabled. Noise in `X1.X2` will be disabled.

Example4

```
subckt subl a b
    parameters isnoisy=no
    R1 a 1 1K isnoisy=yes
    R2 1 b 1K
ends
X1 1 0 subl
```

In the above example noise will be enabled for `X1.R1`. It will be disabled for `X1.R2`.

The relation between `noiseon_inst`, `noiseoff_inst`, and `isnoisy` parameters for an instance (say `X1`) is shown below.

	<code>noiseon_inst=[X1]</code>	<code>noiseoff_inst=[X1]</code>	<code>noiseon_inst</code> and <code>noiseoff_inst</code> not specified for <code>X1</code> , but <code>noiseon_inst</code> is specified for other instances	<code>noiseon_inst</code> and <code>noiseoff_inst</code> are not specified for <code>X1</code> , but <code>noiseoff_inst</code> is specified for other instances
<code>isnoisy=yes</code> specified for <code>X1</code>	Enable noise in <code>X1</code> A message is displayed stating that <code>isnoisy</code> is also specified for <code>X1</code> .	Disable noise in <code>X1</code> A message is displayed stating that <code>isnoisy</code> is also specified for <code>X1</code> and <code>noiseoff_inst</code> will override the <code>isnoisy</code> setting.	Enable noise in <code>X1</code>	Enable noise in <code>X1</code>
<code>isnoisy=no</code> is specified for <code>X1</code>	Enable noise in <code>X1</code> A message is displayed stating that <code>isnoisy</code> is also specified for <code>X1</code> and <code>noiseon_inst</code> will override the <code>isnoisy</code> setting.	Disable noise in <code>X1</code> A message is displayed stating that <code>isnoisy</code> is also specified for <code>X1</code> .	Disable noise in <code>X1</code>	Disable noise in <code>x1</code>
<code>isnoisy</code> is not specified for <code>X1</code>	Enable noise in <code>X1</code>	Disable noise in <code>x1</code>	Disable noise in <code>X1</code>	Enable noise in <code>X1</code>

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By default, all noise sources are enabled in all the devices in Spectre. The global `noiseon_inst` and `noiseoff_inst` options and the `isnoisy` parameter can only enable or disable all noise sources in a subcircuit instance. For example:

```
X1 a b c subl
X2 a b c subl
X3 a b c subl
opt options noiseoff_inst=[X1]
```

In the above example, all noise sources in instance `X1` are disabled and all noise sources in instances `X2` and `X3` are enabled.

You can use the global `noiseon_type` or `noiseoff_type` options to partially enable or disable the specific noise sources for a subcircuit instance. When you specify the `noiseon_type` option, it indicates that only the specified noise source is enabled and rest of the noise sources are disabled. Similarly, when you specify the `noiseoff_type` option, it indicates that only the specified noise source is disabled and rest of the noise sources are enabled.

Possible values for the `noiseon_type` and `noiseoff_type` options are `thermal`, `flicker`, `shot`, `ign`, and `all`.

Examples

```
X1 a b c subl
X2 a b c subl
X3 a b c subl
opt1 options noiseoff_inst=[X1]
opt2 options noiseoff_type=[flicker]
```

In the above example, the flicker noise source in `X1` is disabled. Rest of the noise sources in `X1` are enabled. All noise sources in `X2` and `X3` are enabled.

```
X1 a b c subl
X2 a b c subl
X3 a b c subl
opt1 options noiseoff_inst=[X1]
opt2 options noiseoff_type=[flicker]
opt3 options noiseon_type=[thermal]
```

In the above example, the flicker noise source in `X1` is disabled. The rest of the noise sources in `X1` are enabled. In addition, only the thermal noise source in `X2` and `X3` is enabled. The rest of the noise sources in `X2` and `X3` are disabled.

```
X1 a b c subl
X2 a b c subl
X3 a b c subl
```

```
opt1 options noiseoff_type=[flicker]
opt2 options noiseon_type=[thermal]
```

In the above example, `opt1 options` will have no effect because no noise has been disabled using `noiseon_inst`, `noiseoff_inst`, or `isnoisy`. The thermal noise source will be enabled for the X1, X2, and X3 instances and rest of the noise sources will be disabled.

Conditional Subcircuits

You can specify different conditions that determine which subcircuits the Spectre simulator instantiates for a given simulation. The determining conditions are computed from the values of parameters. You specify these conditions with the structural if statement. This statement lets you specify if-else statements in the netlist.

You can also define a subcircuit in a file and include the file inside the conditional statement using the `include` statement.

Inline Subcircuits

An inline subcircuit is a special case where one of the instantiated devices or models within the subcircuit does not get its full hierarchical name but inherits the subcircuit call name. The inline subcircuit is called in the same manner as a regular subcircuit. You format inline subcircuit definitions as follows:

```
inline subckt SubcircuitName [() node1 ... nodeN ()]
```

Depending on the use model, the body of the inline subcircuit typically contains one of the following:

- Multiple device instances, one of which is the `inline` component
- Multiple device instances (one of which is the `inline` component) and one or more parameterized models
- A single `inline` device instance and a parameterized model to which the device instance refers
- Only a single parameterized model

The `inline` component is denoted by giving it the same name as the inline subcircuit itself. When the subcircuit is flattened, as shown in the following section, the `inline` component does not acquire a hierarchical name such as `X1.M1` but rather acquires the name of the subcircuit call itself, `X1`. Any noninline components in the subcircuit acquire the regular hierarchical name, just as if the concept of inline subcircuits never existed.

Typically, a modeling engineer writes inline subcircuit definitions for a circuit design engineer to use.

Modeling Parasitics

You can model parasitics by adding parasitics components to a base component using inline subcircuits. The body of the inline subcircuit contains one `inline` component, the base component, and several regular components, which are taken to represent parasitics.

The following example of an inline subcircuit contains a MOSFET instance and two parasitic capacitances:

```
inline subckt s1 (a b)          // "s1" is name of subcircuit
  parameters l=1u w=2u
  s1 (a b 0 0) mos_mod l=l w=w // "s1" is "inline" component
  cap1 (a 0) capacitor c=1n
  cap2 (b 0) capacitor c=1n
ends s1
```

The following circuit creates a simple MOS device instance M1 and calls the inline subcircuit s1 twice (M2 and M3):

```
M1 (2 1 0 0) mos_mod
M2 (5 6) s1 l=6u w=7u
M3 (6 7) s1
```

This circuit flattens to the following equivalent circuit:

```
M1 (2 1 0 0) mos_mod
M2 (5 6 0 0) mos_mod l=6u w=7u // the "inline" component
                                // inherits call name
M2.cap1 (5 0) capacitor c=1n // a regular hierarchical name
M2.cap2 (6 0) capacitor c=1n
M3 (6 7 0 0) mos_mod l=1u w=2u // the "inline" component
                                // inherits call name
M3.cap1 (6 0) capacitor c=1n
M3.cap2 (7 0) capacitor c=1n
```

The final flattened names of each of the three MOSFET instances are M1, M2 and M3. (If s1 was a regular subcircuit, the final flattened names would be M1, M2.s1, and M3.s1.) However, the parasitic capacitors have full hierarchical names.

You can create an instance of the inline subcircuit cell in the same way as creating an instance of the specially tagged inline device. You can use `save` statements to probe this instance in the same way as a regular device, without having to

- Realize that the instance is actually embedded in a subcircuit
- Know that there are possible additional parasitic devices present
- Figure out the hierarchical name of the device of interest

A modeling engineer can create several of these inline subcircuits and place them in a library for the design engineer to use. The library then includes a symbol cell view for each inline subcircuit. The design engineer then places a symbol cell view on a design, which behaves just as if a primitive were being used. The design engineer can then probe the device for terminal currents and operating-point information.

Probing the Device

The Spectre simulator allows the following list of items to be saved or probed for primitive devices, including devices modeled as the inline components of inline subcircuits:

- All terminal currents
`save m1:currents`
- Specific (index) terminal current
`save m1:1 // #1=drain`
- Specific (named) terminal current
`save m1:s // "s"=source`
- Save all operating-point information
`save m1:oppoint`
- Save specific operating-point information
`save m1:vbe`
- Save all currents and operating-point information
`save m1`

Note: If the device is embedded in a regular subcircuit, you have to know that the device is a subcircuit and find out the appropriate hierarchical name of the device in order to save or probe the device. However, with inline components, you can use the subcircuit call name, just as if the device were not in a subcircuit.

Operating-point information for the inline component is reported with respect to the terminals of the inline component itself and not with respect to the enclosing subcircuit terminals. This results in the following cautions.

Caution: Parasitic Elements in Series with Device Terminals

If the parasitic elements are in series with the device terminals, the reported operating-point currents are correct, but reported operating-point voltages might be incorrect. For example, consider the case of an inline MOSFET device with parasitic source and drain resistances:

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```
inline subckt mos_r (d g s b)
  parameters p1=1u p2=2u
  mos_r (dp g sp b) mos_mod l=p1 w=p2 // "inline" component
  rd (d dp) resistor r=10 // series drain resistance
  rs (s sp) resistor r=10 // series source resistance
ends mos_r
```

If an instance M1 is created of this `mos_r` inline subcircuit and the operating point of M1 is probed, the drain-to-source current `ids` is reported correctly. However, the reported `vds` is not the same as $V(d) - V(s)$, the two wires that connect the subcircuit drain and source terminals. Instead, `vds` is $V(dp) - V(sp)$, which are nodes internal to the inline subcircuit.

Caution: Parasitic Elements in Parallel with Device Terminals

If the parasitic elements are in parallel with the device terminals, the reported voltages are correct, but the reported currents might be incorrect. For example, consider the following case of a MOSFET with source-to-bulk and drain-to-bulk diodes:

```
inline subckt mos_d (d g s b)
  parameters p1=1u p2=2u
  mos_d (d g s b) mos_mod l=p1 w=p2 // "inline" component
  d1 (d b) diode1 r=10 // drain-bulk diode
  d2 (s b) diode1 r=10 // source-bulk diode
ends mos_d
```

Here, the operating-point `vds` for the inline component is reported correctly because there are no extra nodes introduced by the inline subcircuit model. However, the reported `ids` for the inline device is not the same as the current flowing into terminal `d` because some of the current flows into the transistor and some through diode `d1`.

Parameterized Models

Inline subcircuits can be used in the same way as regular subcircuits to implement parameterized models. When an inline subcircuit contains both a parameterized model and an inline device referencing that model, you can create instances of the device, and each instance automatically gets an appropriately scaled model assigned to it.

For example, the instance parameters of an inline subcircuit can represent emitter width and length of a BJT device. Within that subcircuit, a model statement can be created that is parameterized for emitter width and length and scales accordingly. When you instantiate the subcircuit, you supply the values for the emitter width and length, and the device is instantiated with an appropriate geometrically scaled model. Again, the inline device does *not* get a hierarchical name and can be probed in the same manner as if it were a simple device and not actually embedded in a subcircuit.

In the following example, a parameterized model is declared within an inline subcircuit for a bipolar transistor. The model parameters are the emitter width, emitter length, emitter area,

and the temperature delta (`trise`) of the device above nominal. Ninety-nine instances of a 4x4 transistor are then placed, and one instance of a transistor with `area=50` is placed. Each transistor gets an appropriately scaled model.

```
* declare a subcircuit, which instantiates a transistor with
* a parameterized model. The parameters are emitter width
* and length.

inline subckt bjtmod (c b e s)
    parameters le=1u we=2u area=le*we trise=0
    model mod1 bjt type=npn bf=100+(le+we)/2*(area/1e-12) \
        is=1e-12*(le/we)*(area/1e-12)
    bjtmod (c b e s) mod1 trise=trise/"inline" component
ends bjtmod

* some instances of this subckt
q1 (2 3 1 0) bjtmod le=4u we=4u / trise defaults to zero
q2 (2 3 2 0) bjtmod le=4u we=4u trise=2
q3 (2 3 3 0) bjtmod le=4u we=4u
.
.
q99 (2 3 99 0) bjtmod le=4u we=4u
q100 (2 3 100 0) bjtmod le=1u area=50e-12
```

Since *each* device instance now gets its own unique model, this approach lends itself to statistical modeling of on-chip mismatch distributions, in which each device is taken to be slightly different than all the others on the same chip. The value of `bf` is the same for the first 99 transistors.

Inline Subcircuits Containing Only Inline model Statements

You can create an inline subcircuit that contains only a single model statement (and nothing else), where the model name is identical to the subcircuit name. This syntax is used to generate a parameterized model statement for a given set of parameters, where the model is then exported and can be referenced from one level outside the subcircuit. Instantiating the inline subcircuit in this case merely creates a model statement with the same name as the subcircuit call. The Spectre simulator knows that because the subcircuit definition contains only a `model` statement and no other instances, the definition is to be used to generate named models that can be accessed one level outside of the subcircuit. Regular device instances one level outside of the subcircuit can then refer to the generated model.

Because these are now instances of a model rather than of a subcircuit, you can specify device instance parameters with enumerated types such as `region=fwd`.

This technique is shown in the following example:

```
* declare an inline subcircuit that "exports" a parameterized model
inline subckt bjtmod
    parameters le=1u we=2u area=le*we
    model bjtmod bjt type=npn bf=100+(le+we)/2*(area/1e-12) \
        is=1e-12*(le/we)*(area/1e-12)
```

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```
ends bjtmod

* now create two "instances" of the inline subcircuit, that is,
* create two actual models, called mod1, mod2

mod1 bjtmod le=4u we=4u
mod2 bjtmod le=1u area=50e-12

* 99 instances of mod1 (all share mod1)
* and 1 instance of mod2.
q1 (2 3 1 0) mod1 region=fwd
q2 (2 3 2 0) mod1 trise=2
.
.
q99 (2 3 99 0) mod1
q100 (2 3 100 0) mod2
```

Because the syntax of creating an instance of a model is the same as the syntax of creating an instance of a subcircuit in the Spectre netlist, you can easily replace model instances with more detailed subcircuit instances. To do this, replace the `model` statement itself with a subcircuit definition of the same name.

When you do this in the Spectre Netlist Language, you do not have to change the instance statements. In SPICE, inline subcircuits start with `x`, so you need to rename all instance statements to start with `x` if you replaced a model with a subcircuit.

Process Modeling Using Inline Subcircuits

Another modeling technique is to specify geometrical parameters, such as widths and lengths, to a device such as a bipolar transistor and then to create a parameterized model based on that geometry. In addition, the geometry can be modified according to certain process equations, allowing you to model nonideal etching effects, for example.

You use inline subcircuits and some `include` files for process and geometric modeling, as in the following example files. The `ProcessSimple.h` file defines the process parameters and the bipolar and resistor devices:

```
// File: ProcessSimple.h

simulator lang=spectre

// define process parameters, including mismatch effects

parameters RSHSP=200 RSHPI=5k // sheet resistance, pinched sheet res
+ SPDW=0 SNDW=0 // etching variation from ideal
+ XISN=1 XBFN=1 XRSP=1 // device "mismatch" (mm)
parameters
+ XISNafac=100m XISNbfac=1m // IS scaling factors for mm eqns
+ XBFNafac=100m XBFNbfac=1m // BF " " " "
+ XRSPafac=100m XRSPbfac=1m // RS " " " "
+ RSHSPnom=200 RSHPInom=5k // sheet resistance nom. values
+ FRSHPI=RSHPI/RSHPInom // ratio of PI sheet res to nom
```

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```
// define "simple" bipolar and resistor devices

// a "base" TNSA subckt, that is, a simple "TNSA" bipolar transistor
// subcircuit, with model statement
inline subckt TNSA_B (C B E S)
    parameters MULT=1 IS=1e-15 BF=100
    model modX bjt type=npn is=IS bf=BF // a model statement
    TNSA_B (C B E S) modX m=MULT // "inline" device instance
ends TNSA_B

// a "base" resistor
// a simple "RPLR" resistor subcircuit
inline subckt RPLR_B (A B)
    parameters R MULT=1
    RPLR_B (A B) resistor r=R m=MULT // "inline" device
ends RPLR_B

// define process/geometry dependent bipolar and resistor devices

// a "geometrical/process" TNSA subcircuit
// a BJT subcircuit, with process and geometry effects modeled
// bipolar model parameters IS and BF are functions of effective
// emitter area/perimeter taking process factors (for example,
// nonideal etching) into account
inline subckt TNSA_PR (C B E S)
    parameters WE LE MULT=1 dIS=0 dBF=0
+       WEA=WE+SNDW // effective or "Actual" emitter width
+       LEA=LE+SNDW // effective or "Actual" emitter length
+       AE=WEA*LEA // effective emitter area
+       IS=1e-18*FRSHPI*AE*(1+(XISNafac/sqrt(AE)+XISNbfac)
+           *(dIS/2+XISN-1)/sqrt(MULT))
+       BF=100*FRSHPI*(1+(XBFNafac/sqrt(AE)+XBFNbfac)
+           *(dBF/2+XBFN-1)/sqrt(MULT))

    TNSA_PR (C B E S) TNSA_B IS=IS BF=BF MULT=MULT // "inline"
ends TNSA_PR

// a "geometrical/process" RPLR resistor subcircuit
// resistance is function of effective device geometry, taking
// process factors (for example, nonideal etching) into account
inline subckt RPLR_PR (A B)
    parameters Rnom WB MULT=1 dR=0
+       LB=Rnom*WB/RSHSPnom
+       AB=LB*(WB+SPDW)

    RPLR_PR (A B) RPLR_B R=RSHSP*LB/(WB+SPDW)*
+       (1+(XRSPafac/sqrt(AB)+XRSPbfac)*(dR/2+XRSP-1)/sqrt(MULT))
ends RPLR_PR
```

The following file, Plain.h, provides the designer with a plain device interface without geometrical or process modeling:

```
// File: Plain.h

simulator lang=spectre

// plain TNSA, no geometrical or process modeling
inline subckt TNSA (C B E S)
    parameters MULT=1 IS=1e-15 BF=100
```

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```
TNSA (C B E S) TNSA_B IS=IS BF=BF MULT=MULT // call TNSA_B
ends TNSA

// plain RPLR no geometrical or process modeling
inline subckt RPLR (A B)
  parameters R=1 MULT=1
  RPLR (A B) RPLR_B R=R MULT=MULT
ends RPLR
```

The following file, `Process.h`, provides the designer with the geometrical device interface:

```
// File: Process.h

simulator lang=spectre

// call to the geometrical TNSA model
inline subckt TNSA (C B E S)
  parameters WE=1u LE=1u MULT=1 dIS=0 dBF=0
  TNSA (C B E S) TNSA_PR WE=WE LE=LE \
    MULT=MULT dIS=dIS dBF=dBF // call TNSA_PR
ends TNSA

// call to the geometrical RPLR model
inline subckt RPLR (A B)
  parameters Rnom=1 WB=10u MULT=1 dR=0
  RPLR (A B) RPLR_PR Rnom=Rnom WB=WB \
    MULT=MULT dR=dR // call RPLR_PR
ends RPLR
```

The following example is a differential amplifier netlist showing how a design can combine process modeling with process and geometry effects:

```
// a differential amplifier, biased with a 1mA current source
simulator lang=spectre

include "ProcessSimple.h"
include "Process.h"

E1 (1 0) vsource dc=12

// pullup resistors, 4k ohms nominal
R1 (1 2) RPLR Rnom=4k WB=5 // 5 units wide, model will calc length
R2 (1 3) RPLR Rnom=4k WB=10 // 10 units wide, model will calc length

// the input pair
TNSA1 (2 4 5 0) TNSA WE=10 LE=10
TNSA2 (3 4 5 0) TNSA WE=10 LE=10

// no differential input voltage, both inputs tied to same source
E4 (4 0) vsource dc=5

// current source biasing
J5 (5 0) isource dc=1m

dcop dc
```

Component Model

The component model is a special device modeling approach similar to the inline subckt model. However, unlike the inline subcircuit model, it does not use a separate device instance call inside the subcircuit but contains only the model definition. It allows you to separate the model parameters that are common to all the device instances and the device instance parameters. With this approach, it reduces the number of instance parameters that need to be stored for each device instance, and therefore provides optimized memory consumption and performance for advanced node device models. The component block can only be defined at the top level. It cannot be defined inside a subcircuit definition.

```
subckt p_svt_new ( d g s b )
parameters ...
p_svt_new ( d g s b ) p_svt_c w=w l=l ad=ad as=as pd=pd ps=ps sd=sd nf=nf nrd=nrd
nrs=nrs dtemp=dtemp sca=sca ...
...
ends p_svt_new

component p_svt_c
parameters ...
model p_svt_c bsimbulk {
1: type=p
+vgs_max = 1.05 ... }
endcomponent p_svt_c
```

Model binning inside a component model is supported.

```
component nch
parameters paramtype=defined l = 3u w = 1u

model nch bsim4 {
    1: type=n lmin=1u lmax=2u wmin=1u wmax=2u vth0=0.5
    2: type=n lmin=2u lmax=4u wmin=2u wmax=4u vth0=0.4
    3: type=n lmin=2u lmax=4u wmin=4u wmax=6u vth0=0.3
}
endcomponent
```

There are three types of parameters that can be defined inside the component block.

- **local parameters** – `paramtype=local` (default)
 - ❑ The parameter is only defined and used inside the component.
 - ❑ The parameter is not defined at a higher level or used on the instance call.

- instance parameters – `paramtype=instance`
 - The parameter is defined at a higher level and used in the instance call.
 - This parameter need not be defined in the component section, except if a default value needs to be defined.
- local instance parameter – `paramtype=defined`
 - The parameter is defined inside the component section, however it is overwritten by the instance call.

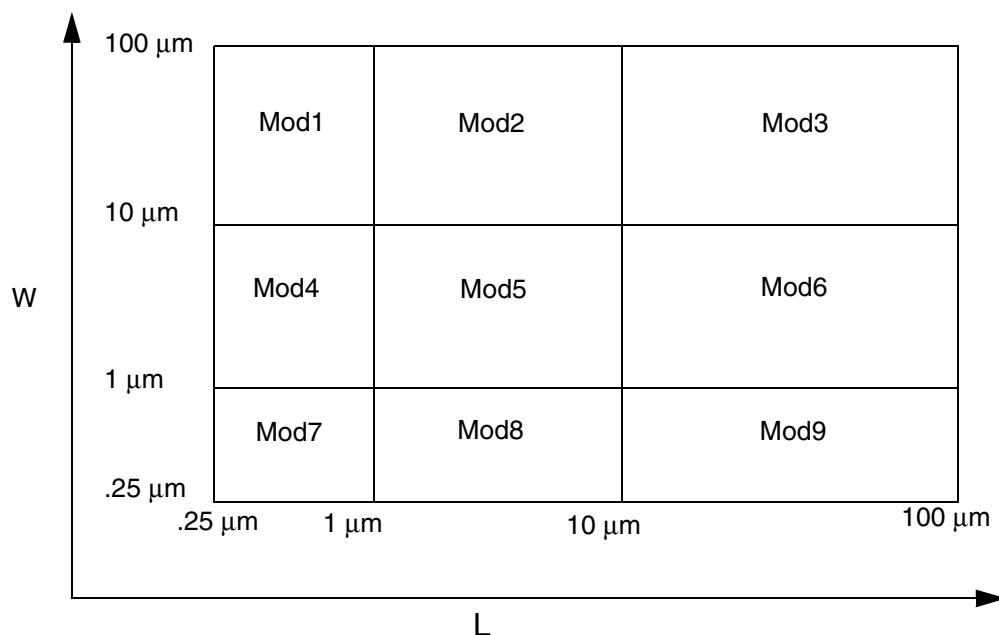
The parameter types can be defined inside the component block using the `paramtype` keyword. The `paramtype` keyword has to be the first item after the `parameters` keyword. The default value of `paramtype` is `local`.

```
component p_svt_c
parameters paramtype=local param_local=12e-12 ...
parameters paramtype=instance param_instance=1e-9 ...
parameters paramtype=defined param_defined=43e-6 ...
...
model p_svt_c bsimbulk {
1: type=p
+vgs_max = 1.05 ... ab=param_local cd=param_instance ef=param_defined ... }
endcomponent p_svt_c
```

Binning

Binning is the process of partitioning a device with different sizes into different models. Before BSIM 3v3, it was very difficult to fit all the devices with a single `model` statement over very wide ranges of device sizes. To improve fitting accuracy, you might characterize devices into several models with each model valid only for a limited range of device sizes.

For example, suppose you have a device with a length (L) from 0.25 μm to 100 μm and a width (W) from 0.25 μm to 100 μm . You might want to divide your device as follows (not drawn to scale).



In this example, nine models are used. These devices are divided into *bins*. For devices whose length lies between 1 μm and 10 μm and width lies between 10 μm and 100 μm, Mod6 is used. The model name within a group can be of type string as well as a number.

The process of generating these models is called binning. The binning process is usually identical for all simulators because the equations for binning are always the same:

$$P = P0 + Pl/Leff + Pw/Weff + Pp/(Leff*Weff)$$

There are two ways to do binning with the Spectre simulator:

- Auto model selection

For more information on auto model selection, see the following section.

- Conditional instances

For more information on using conditional instances, see [Conditional Instances](#) on page 208. For more information on using inline subcircuits for model selection, see [Scaling Physical Dimensions of Components and Device Model Technology](#) on page 218.

Auto Model Selection

Automatic model selection is a simulator feature that automatically assigns the correct models to devices based on their device sizes without using conditional instantiation.

Binning is usually used together with automatic model selection. Model selection is now automatic for MOSFETs, BSIM1, BSIM2, and BSIM3. Help on any one of these devices (for example, `spectre -h mos1`) gives you more details.

For the auto model selector program to find a specific model, the models to be searched need to be grouped together within braces. Such a group is called a model group. An opening brace is required at the end of the line defining each model group. Every model in the group is given a name followed by a colon and the list of parameters. Also, you need to specify the device length and width using the four geometric parameters `lmax`, `lmin`, `wmax`, and `wmin`. The selection criteria to choose a model is as follows:

```
lmin <= inst_length < lmax and    wmin <= inst_width < wmax
```

For example:

```
model ModelName ModelType {
  1:      lmin=2 lmax=4 wmin=1 wmax=2 vto=0.8
  2:      lmin=1 lmax=2 wmin=2 wmax=4 vto=0.7
  3:      lmin=2 lmax=4 wmin=4 wmax=6 vto=0.6
}
```

Then for a given instance

```
M1 1 2 3 4 ModelName w=3 l=1.5
```

the program searches all the models in the model group with the name `ModelName` and then picks the first model whose geometric range satisfies the selection criteria. In the preceding example, the auto model selector program chooses `ModelName.2`.

The following example shows multiple lines for each model statement within a group:

```
model pch mos2 {
  1:type=p vto=-0.65 gamma=0.47 lambda=0.09 \
    ld=0.45E-6 kp=0.33E-4 tox=0.21E-7 is=0.0 \
    lmin=0.5u lmax=1.5u wmin=1u wmax=3u \
    tnom=25 xl=3e-08 af=0.8824
  2:type=p vto=-0.69 gamma=0.44 lambda=0.09 \
    ld=0.45E-6 kp=0.33E-4 tox=0.21E-7 is=0.0 \
    lmin=1.5u lmax=2.5u wmin=3u wmax=5u
  3:type=p vto=-0.73 gamma=0.37 lambda=0.09 \
    ld=0.45E-6 kp=0.33E-4 tox=0.21E-7 is=0.0 \
    lmin=2.5u lmax=3.5u wmin=1u wmax=3u
  4:type=p vto=-0.77 gamma=0.34 lambda=0.09 \
    ld=0.45E-6 kp=0.33E-4 tox=0.21E-7 is=0.0 \
    lmin=3.5u lmax=4u wmin=3u wmax=5u
  ...
}
```

Then for the given instances,

```
m0 (nd ng ns nb) pch m=1.0 w=4u l=2u
m1 (pd pg ps pb) pch m=1.0 w=4u l=4u
```

the auto model selector selects `pch.2` for `m0` and `pch.4` for `m1`.

Conditional Instances

You can specify different conditions that determine which components the Spectre simulator instantiates for a given simulation. The determining conditions are computed from the values of parameters. You specify these conditions with the structural `if` statement. This statement lets you put `if-else` statements in the netlist.

You can also use conditional instantiation with inline subcircuits. For more information on using inline subcircuits, see [Scaling Physical Dimensions of Components and Device Model Technology](#) on page 218.

Formatting the if Statement

You format the structural `if` statement as follows:

```
if condition statement1 [else statement2]
```

<i>condition</i>	The <i>condition</i> fields are Boolean-valued expressions where any nonzero value is taken as “true.”
<i>statement</i>	The <i><statement1></i> and <i><statement2></i> fields contain one or more instance statements or <code>if</code> statements. The <code>else</code> part of the statement is optional.

An if Statement Example

The following example illustrates the use of the `if` statement. There are additional `if` statements in the *statement1* and *statement2* fields.

```
if (rseries == 0) {
    c1 (a b) capacitor c=c
    if (gparallel != 0) gp1 a b resistor r=1/gparallel
} else {
    r2 (a x) resistor r=rseries
    c2 (x b) capacitor c=c
    if (gparallel != 0) gp2 x b resistor r=1/gparallel
}
```

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In this example, the Spectre simulator puts different instance statements into the simulation depending on the values of two parameters, `rseries` and `gparallel`.

- If both `rseries` and `gparallel` are zero, the Spectre simulator includes the instance statement for capacitor `c1`. If `rseries` is zero and `gparallel` is nonzero, the Spectre simulator includes the instance statements for capacitor `c1` and resistor `gp1`.
- If `rseries` is nonzero and `gparallel` is zero, the Spectre simulator includes the instance statements for resistor `r2` and capacitor `c2`.
- If neither `rseries` nor `gparallel` is zero, the Spectre simulator includes the instance statements for resistor `r2`, capacitor `c2`, and resistor `gp2`.

Rules to Remember

When you use the `if` statement,

- If the `statement1` or `statement2` fields contain multiple statements, place these fields within braces (`{}`).
- End the `statement1` and `statement2` fields with newlines.
- Use a continuation character if you want to place a newline between the `if` and `condition` statements.
- When the `statement1` or `statement2` field is a single instance or `if` statement, an `else` statement is associated with the closest previous `if` statement.
- Do not use the parameters specified with the `options` statement inside the `if` expression, otherwise, you might get unexpected results. For example, do not use the following:

```
simOptions options tnom=25
if (tnom == 27) { //27 is the default value of tnom
r1 0 1 resistor r=10
} else {
r1 0 1 resistor r=20
}
```

Binning by Conditional Instantiation

You can use conditional instantiation to select an appropriate model based on certain ranges of specified parameters (model binning). This technique lets you decide and implement which parameters to bin on and is valid for any device that supports a model.

The Spectre Netlist Language has conditional instantiation. For example:

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```
subckt s1 (d g s b)
  parameters l=1u w=1u
  if (l < 0.5u) {
    m1 (d g s b) shortmod l=l w=w // short-channel model
  } else {
    m2 (d g s b) longmod l=l w=w // long-channel model
  }
  model shortmod vto=0.6 gamma=2 ..etc
  model longmod vto=0.8 gamma=66 ..etc
ends s1
```

Based on the value of parameter `l`, one of the following is chosen:

- A short-channel model
- A long-channel model

Previously, the transistor instances had to have unique names (such as `m1` and `m2` in the preceding example), even though only one of them could actually be chosen. Now, you can use the same name for both instances, provided certain conditions are met. The following example shows a powerful modeling approach that combines model binning (based on area) with inline subcircuits for a bipolar device:

```
// general purpose binning and inline models

simulator lang=spectre
parameters VDD=5

vcc (2 0) vsource dc=VDD
vin (1 0) vsource dc=VDD

q1 (1 2 0 0) npn_mod area=350e-12 // gets 20x20 scaled model
q2 (1 3 0 0) npn_mod area=25e-12 // gets 10x10 scaled model
q3 (1 3 0 0) npn_mod area=1000e-12 // gets default model

inline subckt npn_mod (c b e s) //generalized binning, based on area
  parameters area=5e-12
  if ( area < 100e-12 ) {
    npn_mod (c b e s) npn10x10 // 10u * 10u, inline device
  } else if ( area < 400e-12 ) {
    npn_mod (c b e s) npn20x20 // 20u * 20u, inline device
  } else {
    npn_mod (c b e s) npn_default // 5u * 5u, inline device
  }
  model npn_default bjt is=3.2e-16 va=59.8
  model npn10x10 bjt is=3.5e-16 va=61.5
  model npn20x20 bjt is=3.77e-16 va=60.5
ends npn_mod
```

The transistors end up having the name that they were called with (`q1`, `q2`, and `q3`), but each has the correct model chosen for its respective area. Model binning can be now achieved based on *any* parameter and for *any* device, such as resistor or bjt.

Changing the Condition Value In Conditional Instantiation

Changing the value of a parameter that results in a change of boolean if condition value is allowed only if there is no actual topology change and the following conditions are met:

- The number of instances in the `if` and `else` blocks are the same.
- The names of the instances in the `if` and `else` blocks are the same.
- Corresponding instances (with the same name) in the `if` and `else` blocks are instances of the same model or sub-circuit, or instances of two different models of the same primitive type.

For example, you can do the following:

```
model mos1 bsim3v3 <model-params-1>
model mos2 bsim3v3 <model-params-2>
model mos3 bsim3v3 <model-params-3>

if (p<=1)
    m1 1 1 0 0 mos1
else if (p<=2)
    m1 1 1 0 0 mos2
else
    m1 1 1 0 0 mos3
sweep1 sweep param=p values=[1 2 3]
```

The following example does not satisfy the second condition above, so the Spectre simulator errors out even though there is no actual topology change:

```
parameters p=1
if (p<=1)
    r1 1 0 resistor r=1K
else
    r2 1 0 resistor r=10K
all alter param=p value=2
```

Rules for General-Purpose Model Binning

The following set of rules exists for general-purpose model binning. Allowing multiple “instances” or “references” to the same-named device is possible only under the following conditions:

- The reference to the same-named device is possible only in a structural `if` statement that has both an `if` part and an `else` part.
- The conditions of the if statements must evaluate to a single device instance with a unique name in that scope.

Multiple references to the same-named device are only possible if there can only ever be one single instance of this device after all expressions have been evaluated, and each instance must be connected to the same nodes and represent the same device.

Examples of Conditional Instances

The following two examples show how to use conditional instances.

Fully Differential CMOS Operational Amplifier

This netlist describes and analyzes a CMOS operational amplifier and demonstrates several sophisticated uses of Spectre features. The example includes top-level netlist parameters, model library/section statements, multiple analyses, and configuring a test circuit with the `alter` statement.

The first file in the example is the main file for the circuit. This file contains the test circuit and the analyses needed to measure the important characteristics of the amplifier.

The main file is followed by files that describe the amplifier and the various models that can be selected. These additional files are placed in the netlist with `include` statements.

Voltage-controlled voltage sources transform single-ended signals to differential- and common-mode signals and vice versa. This approach does not generate or dissipate any power. The power dissipation reported by the Spectre simulator is that of the differential amplifier.

```
// Fully Differential Operational Amplifier Test Circuit
#define PROCESS_CORNER TYPICAL

simulator lang=spectre
global gnd vdd vss

parameters VDD=5.0_V GAIN=0.5

include "cmos.mod"      section=typical
include "opamp.ckt"

// power supplies
Vdd  (vdd  gnd)  vsource dc=VDD
Vss  (vss  gnd)  vsource dc=-VDD
// compute differential input
Vcm  (cmin gnd)  vsource type=dc dc=0 val0=0 val1=2 width=1u \
      delay=10ns
Vdif (in    gnd)  vsource type=dc dc=0 val0=0 val1=2 width=1u \
      delay=10ns
Ridif (in    gnd)  resistor
Eicmp (pin  cmin in    gnd)  vcvs gain=GAIN
Eicmn (nin  cmin in    gnd)  vcvs gain=-GAIN
// feedback amplifier
A1    (pout nout pvgn nvgn)  opamp
Cf1    (pout t1)  capacitor c=8p
Cf2    (nout t2)  capacitor c=8p
```


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```
Vt1    (t1    nvg)    vsource    mag=0
Vt2    (t2    pvq)    vsource    mag=0
Cl1    (pout  gnd)    capacitor  c=8p
Cl2    (out   gnd)    capacitor  c=8p
Ci1    (pin   pvq)    capacitor  c=2p
Ci2    (nin   nvg)    capacitor  c=2p
// compute differential output
Edif    (out   gnd  pout  nout) vcvs gain=1
Rodif    (out   gnd)    resistor
Ecmp    (cmout mid  pout  gnd) vcvs gain=GAIN
Ecmn    (mid   gnd  nout  gnd) vcvs gain=GAIN
Rocm    (cmout gnd)    resistor
//
// Perform measurements
//
spectre options save=lvlpub nestlvl=1
printParams info what=output where=logfile
// operating point
opPoint dc readns="%C:r.dc" write="%C:r.dc"
printOpPoint info what=oppoint where=logfile
// differential-mode characteristics
// closed-loop gain, Av = Vdif:p
// power supply rejection ratio, Vdd PSR = Vdd:p, Vss PSR = Vss:p
dmXferFunctions xf start=1k stop=1G dec=10 probe=Rodif
dmNoise noise start=1k stop=1G dec=10 \
    oprobe=Edif oportv=1 iprobe=Vdif iportv=1
// step response
dmEnablePulse alter dev=Vdif param=type value=pulse annotate=no
dmStepResponse tran stop=2us errpreset=conservative
dmDisablePulse alter dev=Vdif param=type value=dc annotate=no
// loop gain, Tv = -t1/nvg
// open-loop gain, av = out/(pvq-nvg)
dmEnableTest1 alter dev=Vt1 param=mag value=1 annotate=no
dmEnableTest2 alter dev=Vt2 param=mag value=-1 annotate=no
dmLoopGain ac start=1k stop=1G dec=10
dmDisableTest1 alter dev=Vt1 param=mag value=0 annotate=no
dmDisableTest2 alter dev=Vt2 param=mag value=0 annotate=no
// common-mode characteristics
// closed-loop gain, Av = Vcm:p
// power supply rejection ratio, Vdd PSR = Vdd:p, Vss PSR = Vss:p
cmXferFunctions xf start=1k stop=1G dec=10 probe=Rocm
cmNoise noise start=1k stop=1G dec=10 \
    oprobe=Rocm oportv=1 iprobe=Vcm iportv=1
// step response
cmEnablePulse alter dev=Vcm param=type value=pulse annotate=no
cmStepResponse tran stop=2us errpreset=conservative
cmDisablePulse alter dev=Vcm param=type value=dc annotate=no
// loop gain, Tv = -t1/nvg
// open-loop gain, av = 2*cmout/(pvq+nvg)
cmEnableTest1 alter dev=Vt1 param=mag value=1 annotate=no
cmEnableTest2 alter dev=Vt2 param=mag value=1 annotate=no
cmLoopGain ac start=1k stop=1G dec=10
cmDisableTest1 alter dev=Vt1 param=mag value=0 annotate=no
cmDisableTest2 alter dev=Vt2 param=mag value=0 annotate=no
The following file, opamp.ckt, contains the differential amplifier.
// opamp.ckt: Fully Differential CMOS Operational Amplifier
//
// This circuit requires the use of the cmos process models
simulator lang=spectre
// Folded-Cascode Operational Amplifier
```

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```
subckt opamp (pout nout pin nin)
// input differential pair
M1 (4 pin 1 1) nmos w=402.4u l=7.6u
M2 (5 nin 1 1) nmos w=402.4u l=7.6u
M18 (1 12 vss vss) nmos w=242.4u l=7.6u
// upper half of folded cascode
M3 (4 11 vdd vdd) pmos w=402.4u l=7.6u
M4 (5 11 vdd vdd) pmos w=402.4u l=7.6u
M5 (nout 16 4 vdd) pmos w=122.4u l=7.6u
M6 (pout 16 5 vdd) pmos w=122.4u l=7.6u
// lower half of folded cascode
M7 (nout 13 8 vss) nmos w=72.4u l=7.6u
M8 (pout 13 9 vss) nmos w=72.4u l=7.6u
M9 (8 12 vss vss) nmos w=122.4u l=7.6u
M10 (9 12 vss vss) nmos w=122.4u l=7.6u
// common-mode feedback amplifier
M11 (10 nout vss vss) nmos w=12.4u l=62.6u
M12 (10 pout vss vss) nmos w=12.4u l=62.6u
M13a (11 gnd vss vss) nmos w=12.4u l=62.6u
M13b (11 gnd vss vss) nmos w=12.4u l=62.6u
M14 (10 10 vdd vdd) pmos w=52.4u l=7.6u
M15 (11 10 vdd vdd) pmos w=52.4u l=7.6u
Cc1 (nout 11) capacitor c=1p
Cc2 (pout 11) capacitor c=1p
// bias network
M16 (12 12 vss vss) nmos w=22.4u l=11.6u
M17 (21 12 vss vss) nmos w=22.4u l=11.6u
M19 (13 13 14 vss) nmos w=22.4u l=21.6u
M20 (13 21 16 vdd) pmos w=52.4u l=7.6u
M21 (21 16 17 vdd) pmos w=26.4u l=11.6u
M22 (16 16 17 vdd) pmos w=26.4u l=11.6u
D1 (15 vss) dnp area=400n
D2 (14 15) dnp area=400n
D3 (18 17) dnp area=400n
D4 (vdd 18) dnp area=400n
Ib (gnd 12) isource dc=10u
ends opamp
```

The following file, `cmos.mod`, contains the models and uses the `library` and `section` statements to bin models into various process “corners.” See [Process File](#) on page 215 for a more sophisticated example, which also includes automatic model selection.

```
// cmos.mod: Spectre MOSFET model parameters --- CMOS process
//
// Empirical parameters, best, typical, and worst cases.
//
//
simulator lang=spectre
library cmos_mod

section fast // MOSFETS and DIODES for process corner "FAST"
model nmos mos3 type=n vto=1.04 gamma=1.34 phi=.55 nsub=1e15 \
    cgso=290p cgdo=290p cgbo=250p cj=360u tox=700e-10 \
    pb=0.914 js=1e-4 xj=1.2u ld=1.2u wd=0.9u uo=793 bvj=14
model pmos mos3 type=p vto=-0.79 gamma=0.2 phi=.71 nsub=1.7e16 \
    cgso=140p cgdo=140p cgbo=250p cj=80u tox=700e-10 \
    pb=0.605 js=1e-4 xj=0.8u ld=0.9u wd=0.9u uo=245 bvj=14
model dnp diode is=3.1e-10 n=1.12 cjo=3.1e-8 pb=.914 m=.5 bvj=45 \
    imax=1000
model dpn diode is=1.3e-10 n=1.05 cjo=9.8e-9 pb=.605 m=.5 bvj=45 \
```

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```
        imax=1000
endsection fast

section typical // MOSFETS and DIODES for process corner "TYPICAL"
  model nmos mos3 type=n vto=1.26 gamma=1.62 phi=.58 nsub=1e15 \
    cgso=370p cgdo=370p cgbo=250p cj=400u tox=750e-10 \
    pb=0.914 js=1e-4 xj=1u ld=0.8u wd=1.2u uo=717 bvj=14
  model pmos mos3 type=p vto=-1.11 gamma=0.39 phi=.72 nsub=1.7e16 \
    cgso=220p cgdo=220p cgbo=250p cj=100u tox=750e-10 \
    pb=0.605 js=1e-4 xj=0.65u ld=0.5u wd=1.2u uo=206 bvj=14
  model dnp diode is=3.1e-10 n=1.12 cjo=3.1e-8 pb=.914 m=.5 bvj=45 \
    imax=1000
  model dpn diode is=1.3e-10 n=1.05 cjo=9.8e-9 pb=.605 m=.5 bvj=45 \
    imax=1000
endsection typical

section slow // MOSFETS and DIODES for process corner "SLOW"
  model nmos mos3 type=n vto=1.48 gamma=1.90 phi=.59 nsub=1e15 \
    cgso=440p cgdo=440p cgbo=250p cj=440u tox=800e-10 \
    pb=0.914 js=1e-4 xj=0.8u ld=0.38u wd=1.5u uo=641 bvj=14
  model pmos mos3 type=p vto=-1.42 gamma=0.58 phi=.73 nsub=1.7e16 \
    cgso=300p cgdo=300p cgbo=250p cj=120u tox=800e-10 \
    pb=0.605 js=1e-4 xj=0.5u ld=0.1u wd=1.5u uo=167 bvj=14
  model dnp diode is=3.1e-10 n=1.12 cjo=3.1e-8 pb=.914 m=.5 bvj=45 \
    imax=1000
  model dpn diode is=1.3e-10 n=1.05 cjo=9.8e-9 pb=.605 m=.5 bvj=45 \
    imax=1000
endsection slow

endlibrary
```

Process File

This example of automatic model selection with the conditional `if` statement is more sophisticated than the previous example (in section [Fully Differential CMOS Operational Amplifier](#) on page 212). With this example, you ask for an `nmos` transistor, and the Spectre simulator automatically selects the appropriate model according to the process corner, the circuit temperature, and the device width and length. The selection is done by the parameterized inline subcircuit and the conditional `if` statement.

The `paramtest` statements create warnings if the model selection parameters are out of range. Models are assigned to instances depending on the initial values of their parameters when the circuit is input. Note that the instances are not reassigned to new models if the selection parameters later change. However, the models are updated if the circuit temperature is changed. Notice that even though `nmos` is defined as a subcircuit, it is called as if it is a MOSFET primitive.

The MOSFET model parameters are deleted to keep this example to a reasonable length, and ordinarily both the N- and P-channel models are in the same file. If you added the model parameters and a `pmos` model, this file could replace `cmos.mod` in the previous example.

```
// N-CHANNEL MOS --- 1u NMOS PROCESS
//
//
```

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```
// The following group of models represent N-channel MOSFETs over
// the following ranges:
//     lu <= l <= oo
//     lu <= w <= oo
//     0 <= T <= 55
//     process corners = {FAST, TYPICAL, SLOW}
// Warnings are issued if these limits are violated.
//
// This model takes 4 parameters, l, w, ls, and ld. The defaults for
// each of these parameters is lum.
//
//
//           +-----+
//       +-----+           +-----+ ---
//       |         |         |         | ^
//       |         |         |         | |
//       |<- ls ->|<--- l --->|<- ld ->| w
//       |         |         |         | |
//       |         |         |         | v
//       +-----+           +-----+ ---
//
//           Source      Gate      Drain
//
simulator lang=spectre
//
// Complain if global constants are out-of-range.
//
TooCold paramtest warnif=(temp < 0) \
    message="The nmos model is not accurate below 0 C."
TooHot paramtest warnif=(temp > 55) \
    message="The nmos model is not accurate above 55 C."
//
// Define inline subcircuit that implements automatic model selection
// this uses user-supplied parameters l and w which represent device
// geometry, and the built-in parameter temp, to perform model binning
// based on both geometry and temperature.
//
inline subckt nmos (d g s b)
    parameters l=lum w=lum ls=lum ld=lum
//
// Complain if subcircuit parameters are out-of-range.
//
TooShort paramtest warnif=(l < lum) \
    message="Channel length for nmos must be greater than lum."
TooThin paramtest warnif=(w < lum) \
    message="Channel width for nmos must be greater than lum."
TooNarrow paramtest warnif=(ls < lum) warnif=(ld < lum) \
    message="Stripe width for nmos must be greater than lum."
//
// Model selection
include "models.scs" // include all model definitions
include "select_model.scs " section=typical // include code to auto
// choose models
ends nmos
//
// Set the temperature
//
nmosSetTempTo27C alter param=temp value=27
```

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The following file, `models.scs`, contains the models, which depend on circuit temperature (`temp`). Each model parameter can take on one of two values, depending on the value of parameter `temp`.

```
//
// Fast models.
//
model fast_1x1 mos3 type=n vto=(temp >= 27_C) ? 0.8 : 0.77 // ...etc
model fast_1x3 mos3 type=n vto=(temp >= 27_C) ? 0.9 : 0.78 // ...etc
model fast_3x1 mos3 type=n vto=(temp >= 27_C) ? 0.95 : 0.79 // ...etc
model fast_3x3 mos3 type=n vto=(temp >= 27_C) ? 0.98 : 0.81 // ...etc
//
// Typical models.
//
model typ_1x1 mos3 type=n vto=(temp >= 27_C) ? 0.90 : 0.75 // ...etc
model typ_1x3 mos3 type=n vto=(temp >= 27_C) ? 0.91 : 0.73 // ...etc
model typ_3x1 mos3 type=n vto=(temp >= 27_C) ? 0.97 : 0.77 // ...etc
model typ_3x3 mos3 type=n vto=(temp >= 27_C) ? 0.99 : 0.84 // ...etc
//
// Slow models.
//
model slow_1x1 mos3 type=n vto=(temp >= 27_C) ? 0.92 : 0.76 // ...etc
model slow_1x3 mos3 type=n vto=(temp >= 27_C) ? 0.93 : 0.74 // ...etc
model slow_3x1 mos3 type=n vto=(temp >= 27_C) ? 0.98 : 0.78 // ...etc
model slow_3x3 mos3 type=n vto=(temp >= 27_C) ? 0.98 : 0.89 // ...etc
```

The following file, `select_models.scs`, uses the structural `if` statement to select models based on parameters `l` and `w`. Note that for MOS devices, this could also be achieved by using auto model selection (see `spectre -h mos3`), but this example illustrates model binning and model selection based on the structural `if` statement, which can be used to bin based on any combination of parameters, (not necessarily predefined device geometry models) and for any device type (that is, not limited to MOS devices only).

```
library select_models
section fast // select models for fast device, based on subckt
//parameters l,w
  if (l <= 3um) {
    if (w <= 3um) {
      nmos (d g s b) fast_1x1 l=l w=w ls=ls ld=ld
    } else {
      nmos (d g s b) fast_1x3 l=l w=w ls=ls ld=ld
    }
  } else {
    if (w <= 3um) {
      nmos (d g s b) fast_3x1 l=l w=w ls=ls ld=ld
    } else {
      nmos (d g s b) fast_3x3 l=l w=w ls=ls ld=ld
    }
  }
endsection fast
section typical
  if (l <= 3um) {
    if (w <= 3um) {
      nmos (d g s b) typ_1x1 l=l w=w ls=ls ld=ld
    } else {
      nmos (d g s b) typ_1x3 l=l w=w ls=ls ld=ld
    }
  }
endsection typical
```

```
    }
  } else {
    if (w <= 3um) {
      nmos (d g s b) typ_3x1 l=l w=w ls=ls ld=ld
    } else {
      nmos (d g s b) typ_3x3 l=l w=w ls=ls ld=ld
    }
  }
}
endsection typical
section slow
  if (l <= 3um) {
    if (w <= 3um) {
      nmos (d g s b) slow_1x1 l=l w=w ls=ls ld=ld
    } else {
      nmos (d g s b) slow_1x3 l=l w=w ls=ls ld=ld
    }
  } else {
    if (w <= 3um) {
      nmos (d g s b) slow_3x1 l=l w=w ls=ls ld=ld
    } else {
      nmos (d g s b) slow_3x3 l=l w=w ls=ls ld=ld
    }
  }
}
endsection slow
endlibrary
```

Scaling Physical Dimensions of Components and Device Model Technology

Selected components allow their physical dimensions to be scaled with global scale factors. When you want to scale the physical dimensions of these instances and models, you use the `scale` and `scalem` parameters in the `options` statement. Use `scale` for instances and `scalem` for models. The default value for both `scale` and `scalem` is 1.0. (For more information about the `options` statement, see [options Statement Format](#) on page 583 and the documentation for the `options` statement in Spectre online help `spectre -h options`.)

You can scale the following devices with `scale` and `scalem`:

- Capacitors—length (`l`) or width (`w`)
- Diodes—length (`l`) or width (`w`)
- Resistors—length (`l`) or width (`w`)
- Physical resistors (`phy_res`)—length (`l`) or width (`w`)
- MOSFET—length or width

Finding Default Measurement Units

The effects of `scale` and `scalem` depend on the default measurement units of the components you scale. To find the default measurement units for a component parameter, look up that parameter in the parameter listings of your Spectre online help (`spectre -h`). The default for measurement units is in parentheses. For example, the (m) in this entry from the `mos8` parameter descriptions in the Spectre online help (`spectre -h`) tells you that the default measurement unit for channel width is meters.

w (m) Channel width

Effects of `scale` and `scalem` with Different Default Units

`scale` and `scalem` affect only parameters whose default measurement units are in meters. For example, `vmax` is affected because its units are *m/sec*, but `ucrit` is not affected because its units are *V/cm*. Similarly, `nsub` is not affected because its units are *1/cm³*. You can check the effects of `scale` and `scalem` by adding an `info` statement with `what=output` and look for the effective length (`leff`) or width (`weff`) of a device. For more information about the `info` statement, see [The info Statement](#) on page 572.

The following table shows you the effects of `scale` and `scalem` with different units:

scale or scalem	Units	Scaling action
<code>scale</code>	meters (m)	Multiplied by <code>scale</code>
<code>scalem</code>	meters (m)	Multiplied by <code>scalem</code>
<code>scale</code>	meters ⁿ (m ⁿ) (With n a real number)	Multiplied by <code>scaleⁿ</code>
<code>scalem</code>	meters ⁿ (m ⁿ) (With n a real number)	Multiplied by <code>scalemⁿ</code>
<code>scale</code>	1/ meters (1/m)	Divided by <code>scale</code>
<code>scalem</code>	1/ meters (1/m)	Divided by <code>scalem</code>
<code>scale</code>	1/meters ⁿ (1/m ⁿ) (With n a real number)	Divided by <code>scaleⁿ</code>
<code>scalem</code>	1/meters ⁿ (1/m ⁿ) (With n a real number)	Divided by <code>scaleⁿ</code>

Scaling Device Model Technology

The `scalefactor` parameter in the `options` statement enables device model providers to scale device technology independent of the design dimension scaling done by circuit designers. The resulting device instance scaling is defined by `scale * scalefactor`. If the foundry uses a technology scale factor of 0.9 (`scalefactor=0.9`), and the circuit designer uses a design scale factor of 1e-6 (`scale=1e-6`), then the compounded scaling of the device instance dimension is 0.9e-6. Unlike the `scale` parameter, the `scalefactor` parameter cannot be used as a netlist parameter and cannot be altered or used in sweep statements.

Note: The `scalefactor` parameter does not apply to BJT devices.

String Parameters

You can use quoted character strings as parameter values. String values you might use as Spectre parameter values include filenames and labels. When you use a string as a parameter, enclose the string in quotation marks. In the following example, the value for the parameter named `file` is the character string `Spara.data`.

```
model sp_data nport file="Spara.data"
```

Multi-Technology Simulation

The Spectre circuit simulator supports a multi-technology simulation (MTS) mode that enables the simulation of a system consisting of blocks designed with different processes. Under this mode, models and modelgroups referenced using `include` or `ahdl_include` statements in a subcircuit are locally scoped to that subcircuit only. In addition, process options parameters (`temp`, `tnom`, `scale`, and `scalem`), when specified in a subcircuit, are locally scoped to that subcircuit only.

MTS mode is enabled by default across all Spectre simulators. To turn the MTS mode off, use the `-mts` command-line option.

Here is an example of a system consisting of blocks designed with different processes:

```
globaloptions options tnom=26 scale=1
subckt chip1 ( in out )
    ahdl_include "a.va"
    include "pmos_mode.scs"
    scopedoption1 options tnom=27 scale=0.1
    subckt inv ( in out )
        mp ( out in vdd vdd ) pmos w=1u l=3u
        mn ( out in 0 0 ) nmos w=1u l=3u
    ends inv
    subckt buffer ( in out )
        x1 ( in mid ) inv
        x2 ( mid out ) inv
```


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```
ends buffer
xa ( in out ) buffer
model nmos bsim3v3 type=n
ends chip1
subckt chip2 ( in out )
ahdl_include "b.va"
scopedoption2 options tnom=25 scale=0.2
subckt inv ( in out )
mp ( out in vdd vdd ) pmos w=1u l=3u
mn ( out in 0 0 ) nmos w=1u l=3u
ends inv
subckt buffer ( in out )
x1 ( in mid ) inv
x2 ( mid out ) inv
ends buffer
xa ( in out ) buffer
model pmos bsim3v3 type=p
model nmos bsim3v3 type=n
ends chip2
```

In the log file, you will see the following user options:

Global user options:

```
tnom = 26
scale = 1
```

Scoped user options:

```
tnom = 27      subckt=chip1
scale = 0.1    subckt=chip1
tnom = 25      subckt=chip2
scale = 0.2    subckt=chip2
```

You may disable some of the instances and subcircuits by using the `skip` option with the scope specified for MTS. For example,

```
Opt1 options skip=cut inst=[x1 x2]
Opt1 options skip=cut subckt=[sub1 sub2]
```

The possible values for the `skip` option are `none`, `load`, and `cut`. The default value is `none`. When you set the `skip` option to `cut`, the simulator leaves the instance terminals or subcircuit ports disconnected, when MTS is enabled.

Note: Spectre and Spectre APS do not support `skip=load`.

Specifying `cmin`

By default, the Spectre circuit simulator considers all options specified for a node as global options, and all nodes in the design share the same options. However, you can use `cmin` as a scoped option or with the `node` statement and use this capability to apply this option to the nodes in a certain scope to aid convergence.

Specifying `cmin` as a scoped option

You can specify `cmin` as a scoped option, as shown in the following examples:

```
Opt1 options cmin=0.001 sub=[sub1]
```

Here, the `cmin` value 0.001 will be applied to all nodes of the subcircuit instances whose master is `sub1`.

```
Opt2 options cmin=0.002 inst=[x1]
```

Here, the `cmin` value 0.002 will be applied to all nodes of the subcircuit instance `x1`.

The supported scope types for the `cmin` option are: `sub/subckt` and `dev/inst`.

Note: The scoped `cmin` option takes precedence over the global `cmin` option.

The scoped options are displayed under the Scoped user options section in the Spectre log file, as shown below.

```
Scoped user options:
    cmin = 0.001      sub=sub1
```

Specifying `cmin` with the `node` Statement

You can specify `cmin` with the `node` statement, as shown below.

```
Node1 (n1) node cmin=0
```

In the above example, the `cmin` value on node `n1` will be 0.

```
node1 (n1) node cmin=0 sub=[sub1 sub2 ..]
```

In the above example, `cmin=0` is applied to the internal node or port with the name `n1` for subcircuit instances whose master is `sub1` or `sub2`.

Note: You can specify `cmin` both as a scoped option and in the `node` statement. However, if there is a conflict, the `cmin` option specified in the `node` statement gets higher precedence than the scoped `cmin` option. If there is no conflict, their scope is merged.

Modeling for Signal Integrity

The performance of an IC design is no longer limited to how many million transistors a vendor fits on a single chip. With tighter packaging space, and increasing clock frequencies, packaging issues and system-level performance issues (such as crosstalk and transmission lines) are becoming increasingly significant.

At the same time, with the popularity of multi-chip packages, and increased I/O counts, package design itself is becoming more like chip design.

This chapter describes the modeling capability the Spectre circuit simulator provides to assess signal integrity for your design, and describes

- [N-Port Modeling](#) on page 224
- [Transmission Line Modeling](#) on page 237
- [Input/Output Buffer Modeling Using IBIS](#) on page 244

N-Port Modeling

When you model N-ports, you must first create a file listing the S, Y, or Z-parameters. Then you complete the modeling by using this file as input for an `nport` statement. You can create the S, Y, or Z-parameter file listing in two different ways.

- You can run an `sp` analysis and create a listing of S-parameter estimates automatically.
- If you already know the S-parameter values, you can create an S-parameter listing manually with a text editor such as `vi`.

The S, Y, or Z-parameter data file describes the characteristics of a linear N-port over a list of frequencies. The format of the data file used by the Spectre simulator is flexible and self documenting. The Spectre simulator native format describes N-ports with an arbitrary number of ports, specifies the reference resistance of each port, mentions the frequency with no hidden scale factors, and allows the S-parameters to be given in several formats. The Spectre circuit simulator can also read the Touchstone and CITIf file format.

You can set the `matrixform` parameter to specify a state-space model in your netlist. A state space model is a set of state space equations in matrix form describing a linear system. Use the `porttypes` parameter to specify the port types and the `portquantities` parameter to specify whether the port is current or voltage. For more information on state-space model parameters, see `spectre -h nport`.

N-Port Example

This example demonstrates the use of the `nport` statement.

```
// Two port test circuit
global gnd
simulator lang=spectre
// Models
model sp_data nport file="Spara.data"
// Components
```

Port1	(i1	gnd)	port	num=1			
TL1	(i1	gnd	o1	gnd)	tline	z0=25	f=1M
Port2	(o1	gnd)	port	num=2			
Port3	(i2	gnd)	port	r=50	num=3		
X1	(o2	gnd	o2	gnd)	sp_data		
Port4	(o2	gnd)	port	r=50	num=4		

```
// Analyses
Op_Point dc
Sparams sp stop=0.3MHz lin=100 ports=[Port1 Port3]
```

Creating an S-Parameter File Automatically

To create an S-parameter file automatically, run an `sp` analysis that sweeps frequency and set the output `file` parameter to `file="filename"`. The parameter `filename` is the name you select for the S-parameter file. For more information about specifying an `sp` analyses, see [Chapter 11, “Analyses”](#) and the parameter listings for the `sp` analysis in the Spectre online help (`spectre -h sp`).

Creating an S, Y, or Z-Parameter File Manually

To create an S, Y, or Z-parameter file manually in a text editor, observe the following guidelines and rules:

- The Spectre simulator accepts the following formats for S, Y, or Z-parameters: `real-imag`, `mag-deg`, `mag-rad`, `db-deg`, and `db-rad`. The formats do not have to be the same for each parameter. For clarity, use a comma to separate the two parts of an S, Y, or Z-parameter.
- Begin each file with a semicolon. Semicolons indicate comment lines.
- Use spaces, commas, and newlines as delimiters.
- You can enter the parameters in any order.
- You can specify any number of frequency points. The frequency points do not have to be equally spaced, but the frequency index must be in ascending or descending order.
- You must place the frequency specification before the S-parameters, and you must separate the frequency specification from the S-parameters with a colon.
- There is no limit to the number of ports. If either port number is greater than nine, place a colon between the two port numbers when you specify the S, Y, or Z-parameter format (`S13:15`).

Note: The S, Y, or Z-parameters can be given in any order and in any supported format, but the order and format used must be consistent through out the file and must match the order and format specified in the format line.

Reading the S, Y or Z-Parameter File

After you create the S, Y, or Z-parameter file, you must place instructions in the netlist for the Spectre simulator to read it. You can give these instructions with an `nport model` statement or directly on the instance line. The following example shows how to enter an S-parameter file into a netlist. This `model` statement reads S-parameters from the file `Spara.data`.

```
model Sdata nport file="Spara.data" datafmt=spectre|touchstone|citi|format|rfm|bnp
```

If the S-parameter file is not in the same directory as the Spectre simulator, you can use a path to the S-parameter file as a value for the `nport` statement `file` parameter, or you can specify a search path using the `-I` command line argument.

The Spectre circuit simulator reads the S, Y, or Z-parameter data file in the Spectre, CITIfile, or Touchstone format. If you do not specify the input file format, the Spectre circuit simulator detects it automatically by reading the first line in the input file as follows:

`;` as Spectre

`!` as Touchstone

`CITI` as CITIfile.

The Spectre circuit simulator supports

- two-port noise data and noise correlation matrix data in Spectre format
- two-port noise data in Touchstone format

Spectre Format

An S, Y, or Z-parameter file in the Spectre format must have a header. The header

- must have a comment beginning with a semicolon as the first line
- must define the reference resistance of ports and the S, Y, or Z-parameter formats
- can include any number of comment and blank lines.

When reading the file, the simulator ignores all the lines beginning with semicolons, spaces, commas, and newlines in the header. The simulator reads the numbers immediately after `=` on the lines after the `reference resistance` line as impedance data of the ports. The `format` section is treated as the format definition of S-parameter data entries.

You can enter the S, Y, or Z-parameters in any order, but the frequency must be first and is separated from the parameters with a colon. Each parameter can be expressed as

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(real,imag), (mag,deg), (mag,rad), (db,deg), or (db,rad). You can use commas to separate the two parts of a parameter.

Any number of frequency points can be presented. They do not need to be equally spaced, but the frequency index must be monotonic, and the frequency data must be given explicitly, with no hidden scale factors. There is no limit to the number of ports. S-parameters use the syntax `S13:15` when either port number is greater than 9.

Adding Noise Parameters

An S-parameter file in Spectre format can contain external two-port noise data as well as noise correlation matrix data. The syntax for two-port noise data is:

```
noiseformat freq: Fmin (mag|db) Gamma(real,imag|mag,deg|db,deg) Rn
```

followed by two-port noise parameters.

The syntax for general n-port noise data is:

```
noiseformat freq: CY1:1 CY2:2 CY1:2 CY2:2
```

followed by the noise coefficient matrix.

Example

A Spectre S-parameter file for three ports looks as follows:

```
; S-parameter data file 'port2.data'.
; Generated by spectre from circuit file 'gendata' during analysis swp.
; 12:13:06 PM, Fri May 8, 1998
reference resistance
    port3=137      ; is port p3
    port2=137      ; is port p2
    port1=137      ; is port p1

format  freq:      s33(real,imag)  s23(real,imag)
              s13(real,imag)  s32(real,imag)
              s22(real,imag)  s12(real,imag)
              s31(real,imag)  s21(real,imag)
              s11(real,imag)

0.00000000e+00:  0.333333,      0      -0.666667,      0
                  0.666667,      0      -0.666667,      0
                  0.333333,      0      0.666667,      0
                  0.666667,      0      0.666667,      0
                  0.333333,      0
2.50000000e+07:  0.549736,-0.0181715  -0.446126, 0.0466097
                  0.450264, 0.0181715  -0.446126, 0.0466097
                  0.546593,-0.0556029   0.446126,-0.0466097
                  0.450264, 0.0181715  -0.446126, 0.0466097
                  0.549736,-0.0181715
5.00000000e+07:  0.546094,-0.0359074  -0.437504, 0.0922889
```

Spectre Classic Simulator, Spectre APS, Spectre X, Spectre XPS, Spectre FMC Analysis, and Legato Reliability Solution User Guide

```
0.453906, 0.0359074      -0.437504, 0.0922889
0.533673, -0.10951       0.437504, 0.0922889
0.453906, 0.0359074      0.437504, 0.0922889
0.546094, -0.0359074
```

The following is an example of two-port noise data.

```
noiseformat freq: Fmin(mag)  Gamma(real,imag)      Rn
1.00000000e+09:   340.85      0.348552 .63566e-16  4.88929
2.00000000e+09:   340.85      0.348552 3.63566e-16  4.88929
3.00000000e+09:   340.85      0.348552 3.63566e-16  4.88929
4.00000000e+09:   340.85      0.348552 3.63566e-16  4.88929
5.00000000e+09:   340.85      0.348552 3.63566e-16  4.88929
```

The following is an example of a noise co-relation matrix:

```
noiseformat freq: CY1:1      CY2:1      CY1:2      CY2:2
1.00000000e+09:   0.344025 0.00632498 0.00632498 0.0259336
2.00000000e+09:   0.344025 0.00632498 0.00632498 0.0259336
3.00000000e+09:   0.344025 0.00632498 0.00632498 0.0259336
4.00000000e+09:   0.344025 0.00632498 0.00632498 0.0259336
5.00000000e+09:   0.344025 0.00632498 0.00632498 0.0259336
```

Touchstone Format

Spectre supports Touchstone 1 and Touchstone 2 (MMSIM11.1ISR12 onwards) file formats, which complies with the published standards. For the official Touchstone format documentation refer to http://www.eda.org/pub/ibis/touchstone_ver2.0/touchstone_ver2_0.pdf.

Note: Spectre does not support the H and G parameters in the Touchstone 2 file format.

CITIfile Format

CITIfile stands for Common Instrumentation Transfer and Interchange file format. A typical CITIfile package consists of a

- header containing keywords and setup information

- data section containing one or more data arrays

A data array is numeric data arranged with one data element per line. A data array starts after the BEGIN keyword, and the END keyword follows the last data element in an array.

Example

The following example shows the basic structure of a CITIfile package.

```
CITIFILE A.01.00
NAME Momentum.SP
CONSTANT NBR_OF_PORTS 2
CONSTANT NORMALIZATION 1
VAR freq MAG 12
DATA S[1,1] RI
DATA S[1,2] RI
...
VAR LIST BEGIN
1000000000
2000000000
...
VAR_LIST_END
BEGIN
0.017216494,      0
0.040005801,      0.116494405
...
END
BEGIN
0.9827835,        0
0.944136351,      -0.176952631
...
END
```

In the above example, the VAR_LIST_BEGIN section contains the frequency data points. Each data array block (marked by BEGIN and END keywords) corresponds to an S-parameter and contains the value of that parameter for each frequency point. The first block corresponds to S[1,1], the second block corresponds to S[1,2] and so on.

You can use the SEG_LIST keyword to specify a frequency range. For example,

```
SEG_LIST BEGIN
SEG 1000000000 4000000000 10
SEG_LIST_END
```

specifies that the frequency range is from 1000000000 to 4000000000 with intervals of 10.

Improving the Modeling Capability of the N-Port

You can set the value of the parameter `dcextrap` to `unwrap` or `constant` depending on your data file.

If your data file is not sampled adequately at low frequency (the lowest frequency point does not represent DC reasonably well) or if the data file has a long delay, you can set `dcextrap` to `unwrap`. When a dc point is not provided in the data file, the magnitude is determined based on the regression of some low-frequency data. The phase is determined by extracting the delay and setting the phase to the real axis. If the dc point is provided, the magnitude is interpolated while the phase is determined as mentioned above.

The default value is `constant`. In this case, if a dc point is provided in the data file, interpolation is performed for both the magnitude and phase. If a dc point is not provided in the data file, the low-frequency magnitude is held constant to the lowest data provided. The low-frequency phase is determined using a simple algorithm which sets it to closest point on the real axis from the lowest-frequency data point.

S-Parameter File Format Translator

The S-parameter data file format translator (`sptr`) is a separate program from the Spectre simulator. Since the Spectre circuit simulator now reads the Touchstone and CITIfile formats directly, you need to use the translator only if you have it built into your design flow.

Note: The translator does not support the MHARM, HPMNS, or Linear Neutral Model (LNM) formats any more.

Command Arguments

The following is a synopsis of the command line and arguments used to run the translator.

```
sptr [-i inputFormat] [-o outputFormat] [-f FreqScale] [-V | -version]  
[-format paramFormat] [inputFile] [outputFile]
```

Option	Description
<code>-i <i>inputFormat</i></code>	Input file format. Valid values: <code>spectre</code> , <code>touchstone</code> , <code>citifile</code> Default value: <code>spectre</code>

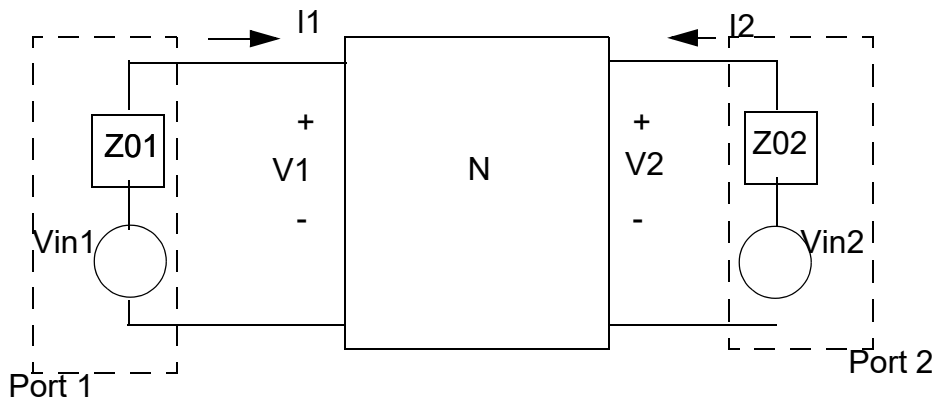
Option	Description
<code>-o outputFormat</code>	Output file format. Valid values: <code>spectre</code> and <code>touchstone</code> Default value: <code>spectre</code>
<code>-f FreqScale</code>	If frequency scale is not explicitly given in the input file, then, $\text{TrueFreq} = \text{GivenFreq} * \text{freqscale}$ Default value: <code>1.0</code> for Spectre and CITIfile formats. <code>1.0e09</code> for touchstone format.
<code>-V -version</code>	Prints the version information.
<code>-format</code> <code>paramFormat</code>	Parameter data format of the output file. Valid values: <code>RI</code> , <code>MA</code> , and <code>DB</code> Default value: <code>RI</code>
<code>inputFile</code>	Input file name.
<code>outputtFile</code>	Output file name.

Standard Scattering Parameter Modeling and Mixed-Mode Scattering Parameter Modeling

Standard S-parameters and mixed-mode S-parameters are defined in the following sections.

Standard S-parameters

A two-port network N can be characterized by standard S-parameters S11, S12, S21, and S22 as shown below:



$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

or

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

where the incident waves a_1 , a_2 , and the reflected waves b_1 , b_2 are:

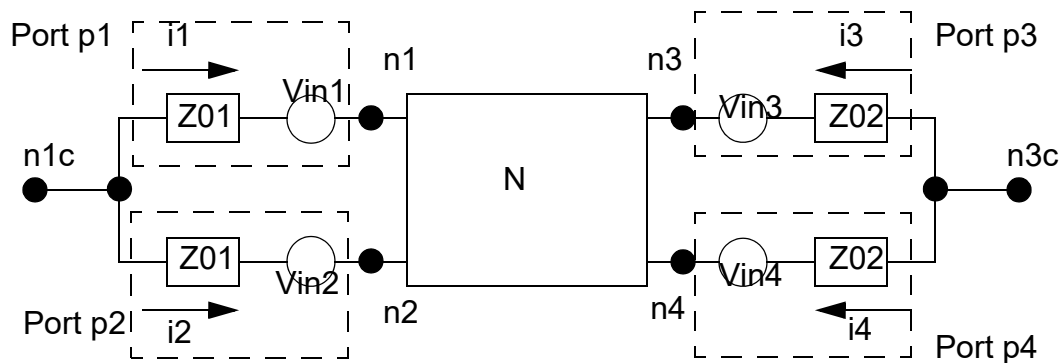
$$a_1 = \frac{V_1 + Z_{01}I_1}{2\sqrt{\text{Re}Z_{01}}} \quad a_2 = \frac{V_2 + Z_{02}I_2}{2\sqrt{\text{Re}Z_{02}}}$$

$$b_1 = \frac{V_1 - Z_{01}^*I_1}{2\sqrt{\text{Re}Z_{01}}} \quad b_2 = \frac{V_2 - Z_{02}^*I_2}{2\sqrt{\text{Re}Z_{02}}}$$

The values of S_{11} , S_{21} , S_{22} , and S_{12} can be obtained by the `sp` analysis.

Mixed-Mode S-Parameters

A 4-port network can be characterized by mixed-mode S-parameters.



where

$$a_{d1} = \frac{1}{2\sqrt{|Re(Z_{d1})|}}(v_{d1} + i_{d1}Z_{d1})$$

$$b_{d1} = \frac{1}{2\sqrt{|Re(Z_{d1})|}}(v_{d1} - i_{d1}Z_{d1}^*)$$

are differential incident wave and differential reflected wave between port pair (p1,p2), and

$Z_{d1} = Z_{01} + Z_{01} = 2Z_{01}$ is the differential impedance

$v_{d1} = v_1 - v_2$ is the differential voltage,

$i_{d1} = \frac{1}{2}(i_1 - i_2)$ is the differential current,

$v_1 = v_{n1} - v_{n1c}$ is the port 1 voltage, and

$v_2 = v_{n2} - v_{n1c}$ is the port 2 voltage.

Also,

$$a_{c1} = \frac{1}{2\sqrt{|Re(Z_{c1})|}}(v_{c1} + i_{c1}Z_{c1})$$

and
$$b_{c1} = \frac{1}{2\sqrt{|Re(Z_{c1})|}}(v_{c1} - i_{c1}Z_{c1}^*)$$

are common-mode incident wave and reflected wave between port pair (p1, p2), and

$Z_{c1} = (Z_{01}Z_{01})/(Z_{01} + Z_{01}) = 0.5Z_{01}$ is the common-mode impedance,

$v_{c1} = (v_1 + v_2)/2$ is the common-mode voltage,

$i_{c1} = i_1 + i_2$ is the common-mode current

with similar definitions of $a_{d2}, b_{d2}, a_{c2}, b_{c2}$ for port pair (p3,p4).

The mixed-mode S-parameters $s_{dd11}, s_{dd12}, \dots, s_{cc21}, s_{cc22}$ are defined as

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} s_{dd11} & s_{dd12} & s_{dc11} & s_{dc12} \\ s_{dd21} & s_{dd22} & s_{dc21} & s_{dc22} \\ s_{cd11} & s_{cd12} & s_{cc11} & s_{cc12} \\ s_{cd21} & s_{cd22} & s_{cc21} & s_{cc22} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = S_{mm} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \begin{bmatrix} S_{dd} & S_{dc} \\ S_{cd} & S_{cc} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix}$$

The values of the mixed-mode s-parameters $s_{dd11}, s_{dd12}, \dots, s_{cc21}, s_{cc22}$ can be obtained by `sp` analysis directly if `mode=mm` is used in the `sp` analysis. The mixed-mode s-parameters are also denoted here by sub-matrices S_{dd}, S_{dc}, S_{cd} , and S_{cc} : S_{dd} as the differential-mode s-parameters, S_{dc} the common-to-differential mode s-parameters, S_{cd} the differential-to-common mode s-parameters, and S_{cc} the common-mode s-parameters.

Conversion of Standard S-Parameters to Mixed Mode S-Parameters

Since the port-pairs (p1,p2) and (p3,p4) have the same impedance $Z_1 = Z_2 = Z_{01}, Z_3 = Z_4 = Z_{02}$, the mixed-mode waves become

$$a_{d1} = \frac{1}{\sqrt{2}}(a_1 - a_2), a_{c1} = \frac{1}{\sqrt{2}}(a_1 + a_2) \quad b_{d1} = \frac{1}{\sqrt{2}}(b_1 - b_2), b_{c1} = \frac{1}{\sqrt{2}}(b_1 + b_2)$$

$$a_{d2} = \frac{1}{\sqrt{2}}(a_3 - a_4), a_{c2} = \frac{1}{\sqrt{2}}(a_3 + a_4) \quad b_{d2} = \frac{1}{\sqrt{2}}(b_3 - b_4), b_{c2} = \frac{1}{\sqrt{2}}(b_3 + b_4)$$

or

$$\begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} = M \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \quad \begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = M \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}$$

The conversion formula is

$$S_{mm} = MS_{std}M^{-1}$$

It can be shown there is a linear relationship between the standard s-parameters S11, S12, ..., S44 (i.e. Sstd) to the mixed-mode s-parameters Sdd11, Sdd12, ..., Scc22 (i.e. Smm).

$$s_{dd11} = \frac{1}{2}(s_{11} - s_{12}) - \frac{1}{2}(s_{21} - s_{22}), s_{dd12} = \frac{1}{2}(s_{13} - s_{14}) - \frac{1}{2}(s_{23} - s_{24})$$

$$s_{dd21} = \frac{1}{2}(s_{31} - s_{32}) - \frac{1}{2}(s_{41} - s_{42}), s_{dd22} = \frac{1}{2}(s_{33} - s_{34}) - \frac{1}{2}(s_{43} - s_{44})$$

$$s_{dc11} = \frac{1}{2}(s_{11} + s_{12}) - \frac{1}{2}(s_{21} + s_{22}), s_{dc12} = \frac{1}{2}(s_{13} + s_{14}) - \frac{1}{2}(s_{23} + s_{24})$$

$$s_{dc21} = \frac{1}{2}(s_{31} + s_{32}) - \frac{1}{2}(s_{41} + s_{42}), s_{dc22} = \frac{1}{2}(s_{33} + s_{34}) - \frac{1}{2}(s_{43} + s_{44})$$

$$s_{cd11} = \frac{1}{2}(s_{11} - s_{12}) + \frac{1}{2}(s_{21} - s_{22}), s_{cd12} = \frac{1}{2}(s_{13} - s_{14}) + \frac{1}{2}(s_{23} - s_{24})$$

$$s_{cd21} = \frac{1}{2}(s_{31} - s_{32}) + \frac{1}{2}(s_{41} - s_{42}), s_{cd22} = \frac{1}{2}(s_{33} - s_{34}) + \frac{1}{2}(s_{43} - s_{44})$$

$$s_{cc11} = \frac{1}{2}(s_{11} + s_{12}) + \frac{1}{2}(s_{21} + s_{22}), s_{cc12} = \frac{1}{2}(s_{13} + s_{14}) + \frac{1}{2}(s_{23} + s_{24})$$

$$s_{cc21} = \frac{1}{2}(s_{31} + s_{32}) + \frac{1}{2}(s_{41} + s_{42}), s_{cc22} = \frac{1}{2}(s_{33} + s_{34}) + \frac{1}{2}(s_{43} + s_{44})$$

Combined Standard S-Parameters with Mixed-Mode S-Parameters

It is possible for a corner case that wave vectors be represented by mixing differential, common-mode, and regular waves. Then there are terms of

$$S_{ds}, S_{cs}, S_{sd}, S_{sc}$$

that relates mixed-mode to single-end conversions. For example, if there is an additional 5th port, and the `sp` analysis has `mode=m12m34s5`, then the wave vectors become

$$a_{mixed} = \begin{bmatrix} a_{d1} & a_{d2} & a_{c1} & a_{c2} & a_{s5} \end{bmatrix}^T \text{ and}$$

$$b_{mixed} = \begin{bmatrix} b_{d1} & b_{d2} & b_{c1} & b_{c2} & b_{s5} \end{bmatrix}^T$$

The mixed-mode s-parameters are related to standard s-parameters as

$$S_{mms} = \begin{bmatrix} S_{mm} & \begin{bmatrix} S_{ds} \\ S_{cs} \end{bmatrix} \\ \begin{bmatrix} S_{sd} & S_{sc} \end{bmatrix} & S_{ss} \end{bmatrix} = \begin{bmatrix} S_{mm} & \begin{bmatrix} \frac{1}{\sqrt{2}}(s_{15} - s_{25}) \\ \frac{1}{\sqrt{2}}(s_{35} - s_{45}) \\ \frac{1}{\sqrt{2}}(s_{15} + s_{25}) \\ \frac{1}{\sqrt{2}}(s_{35} + s_{45}) \end{bmatrix} \\ \begin{bmatrix} s_{51} - s_{52} & s_{53} - s_{54} & s_{51} + s_{52} & s_{53} + s_{54} \end{bmatrix} & s_{55} \end{bmatrix}$$

Examples

Spectre Mixed-Mode S-Parameter Format Examples

```
; S-parameter data file test.sparam.
; Tue Nov 8 11:38:04 2005
; Number of ports is 4
; mode = mm

reference resistance
    port4 = 50.000000
    port3 = 50.000000
    port2 = 50.000000
    port1 = 50.000000

format freq:   sdd1:1(real,imag)      sdd1:2(real,imag)
               sdc1:1(real,imag)      sdc1:2(real,imag)
               sdd2:1(real,imag)      sdd2:2(real,imag)
               sdc2:1(real,imag)      sdc2:2(real,imag)
               scd1:1(real,imag)      scd1:2(real,imag)
               scc1:1(real,imag)      scc1:2(real,imag)
               scd2:1(real,imag)      scd2:2(real,imag)
```



```

                scc2:1(real,imag)      scc2:2(real,imag)
5.000000000e+08:      -0.985696,      1.20713e-16      0.00520889,
0
...

```

Touchstone Mixed-Mode S-Parameter Format Example

```

! Libra (TM) Ver. 3.500.103.3
! Tue Nov  8 11:39:42 2005
! Number of ports is 4
! mode = mm
# Hz      S      RI      R      50.000000
! S11 = SDD11 S12 = SDD12 S13 = SDC11 S14 = SDC12
! S21 = SDD21 S22 = SDD22 S23 = SDC21 S24 = SDC22
! S31 = SCD11 S32 = SCD12 S33 = SCC11 S34 = SCC12
! S41 = SCD21 S42 = SCD22 S43 = SCC21 S44 = SCC22
! SCATTERING PARAMETERS :
5.000000000e+08      -0.985696  1.20713e-16  0.00520889      0      ...

```

Transmission Line Modeling

Multi-conductor transmission line models (MTLINE) are widely used in Spectre simulations. MTLINE is based on Quasi-TEM approximation and the telegrapher's equation, according to which

- An MTLINE can be uniquely characterized by RLGC matrices.
- Once the RLGC matrices have been determined, the behavior of the MTLINE can be predicted in any external environment.

MTLINE can be used to assess the signal integrity of a design in a wide range of interconnect modeling applications.

An MTLINE can have as many conductors as described in the input, with a minimum of two conductors where one conductor is used as a reference to define terminal voltages. The reference conductor can be ground. The order of conductors is the same as the order of the data in the input. It is assumed that all the conductors are of the same length and uniform along the length.

MTLINE accepts the following inputs (described below):

- Per-unit-length constant RLGC matrices
- Per-unit-length frequency dependent RLGC data

- 2-D field solver geometry and material information
- S-parameter data
- Single-conductor TLINE parameters

You can specify all MTLINE parameters (other than the conductor length) through an instance line or model line. When a parameter is specified both on the instance and model line, the value on the instance line takes precedence.

Constant RLGC Matrices

For narrow band applications, you can assume that transmission line characteristics are constant over the frequency you are interested in. The input to MTLINE is per-unit-length resistance (R), inductance (L), conductance (G), and capacitance (C) matrices, and is usually generated by a field solver. MTLINE accepts both full matrix descriptions, and lower-half matrix descriptions because these matrices are generally symmetric.

The following example describes the resistance matrix of a four conductor line system:

$$R = \begin{bmatrix} 50 & 10 & 1 \\ 10 & 50 & 10 \\ 1 & 10 & 50 \end{bmatrix} \quad \text{Ohm/meter}$$

The following model descriptions are equivalent:

```
model line mtline
+ r=[50 10 1
+   10 50 10
+   1 10 50]
+...
```

```
model line mtline
+ r=[50
+   10 50
+   1 10 50]
+...
```

In the past, the only information available to describe a transmission line system was constant RLGC matrices based on narrow band assumption. Some approximation is now used to make the model better cover frequency dependent effects such as skin effect and dielectric loss effect in wide band applications.

The following equation can be used to model skin effect with constant RLGC matrices:

$$R(f) = r + \sqrt{f} \times (1 + j) \times r_{skin}$$

The following equation can be used to model dielectric loss effect with constant RLGC matrices

$$G(f) = g + f \times g_{dloss}$$

where f stands for frequency.

Frequency-Dependent RLGC Data

Frequency dependent RLGC data is described in a data file through the parameter `file`. The frequency axis can be scaled with the `scale` parameter. The frequencies in the data file are then multiplied by `scale` before the simulator uses them. The default scale factor is unity.

The data file has a format section and a data section. Both full matrix and lower half matrix descriptions are accepted. Lines starting with `;` are interpreted as comment lines.

An example data file is shown below:

```
; Comments: rl.dat
FORMAT FREQ:  R1:1 R2:1 R2:2
               L1:1 L2:1 L2:2
0.001e+9:      4.444 0.000383 4.444
               4.565 0.3545  4.565
0.010e+9:      4.447 0.003834 4.447
               4.565 0.3545  4.565
0.100e+9       4.476 0.03834  4.476
               4.565 0.3545  4.565
1.000e+9       4.762 0.3834   4.762
               3.103 0.2357   3.103
10.00e+9       13.96 1.082    13.96
               2.718 0.2058   2.718
100.0e+9       56.88 3.294    56.88
               2.531 0.1866   2.531
; end of file rl.dat
```

You can mix constant RLGC parameters with frequency-dependent RLGC data. When a particular parameter (R, L, G, or C) is provided in both constant matrices and frequency-dependent data file, the value in the constant matrix is given priority. If only one frequency point is provided in the `file` parameter, it is assumed that the RLGC data is constant over the frequency of interest.

For best results, you should provide enough data points to cover low-frequency characteristics as well as the changing nature in the high-frequency range. A rule of thumb is that the lowest frequency point should be down to 1 kHz, and there should be at least 5 points per decade, particularly in the high-frequency range where RLGC data tends to change rapidly.

2-D Field Solver Geometry and Material Information

MTLINE supports a built-in 2-D field solver which has the same modeling engine as the standalone Line Model Generator (LMG) utility. The output of the 2-D field solver is RLGC data, which can be stored for re-use through the `file` parameter. This makes the actual RLGC model generation a one-time cost, given the field solver input remains unchanged.

Line Configuration

MTLINE supports four interconnect line configurations: microstrip line, strip line, coplanar waveguide, and substrate lossy line. You can specify the line configuration through the `linetype` parameter. The default is substrate lossy line.

Model Type

You can specify the model type through the `modeltype` parameter. For each line configuration, you can choose between three model types:

- For the narrow band model, the RLGC data is calculated at frequency $f_{\max}$ and assumed to be constant over the frequency of interest.
- In the wideband model, true frequency dependent RLGC data is calculated over the frequency of interest. This is the default value.
- In the lossless model, the internal inductance of the conductor is disregarded by setting the frequency value high: 50 GHz for cases without substrate loss and 15 GHz for cases with substrate loss. The value of $f_{\max}$ is ignored.

For most applications, you should choose the wideband model as it provides the best model accuracy.

Ground Plane

You can specify the ground planes through the `numgnd` parameter.

For microstrip line, the number of ground planes is 1 placed at the bottom of the 2-D interconnect cross section.

For strip line, the number of ground planes is 2 placed at both the bottom and top of the 2-D interconnect cross section.

For coplanar waveguide and substrate lossy line, the number of ground planes can be 1 or 2, placed at the bottom and top of the 2-D interconnect cross section. For coplanar waveguide, you can also specify 0 ground planes because two ground strips are added automatically to the cross section. You can specify the width, height, thickness, and spacing of these ground strips like you specify the signal line. For more information on signal lines, see [“Signal Line”](#) on page 241.

You can specify the thickness of the ground plane(s) with the `gndthickness` parameter and the ground plane conductivity with the `gndsigma` parameter.

Dielectric Layer

You can specify the dielectric layer through the `numlayer` parameter. Dielectric layers are stacked above the lower ground plane (when `numgnd=1`), or between the ground planes (when `numgnd=2`). There can be more than one dielectric layer.

You can specify the thickness of the dielectric layer through the `layerthickness` parameter, and the relative dielectric constant of the dielectric layer through the `er` parameter. Both `layerthickness` and `er` are of vector type to handle different layer geometries and layer properties.

When the number of elements in the vector is less than the number of layers, the value of the last element in the vector is applied to all of the remaining layers.

If a dielectric layer is lossy, either the `loss tangent` parameter ($\tan = \sigma / (w \cdot \epsilon_0)$) or the `loss sigma` parameter ($\sigma = \tan \cdot w \cdot \epsilon_0$) can be used. This is decided through the `dlosstype` parameter and the actual loss value(s) is provided through the `dloss` vector parameter.

Signal Line

You can specify signal line conductivity through the `linesigma` parameter. There can be more than one signal line. The geometry of the signal line(s) is decided through the `linewidth`, `linethickness`, `lineheight`, and `linespace` parameters. The parameter `lineheight` is the distance between the signal line and ground plane at the bottom of the 2-D interconnect cross section. The parameter `linespace` is the distance between the signal lines – it can be negative in order to describe overlapping signal lines.

Intermediate RLGC File

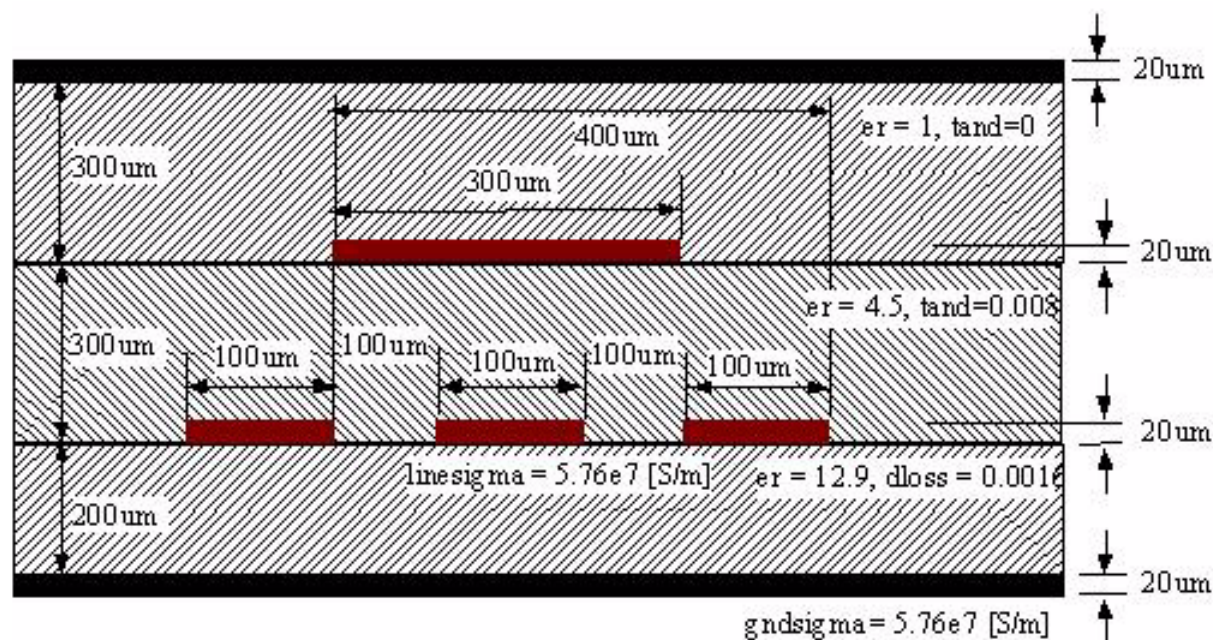
The 2-D field solver output can be stored in the `file` parameter to be used in subsequent simulations. This makes RLGC model generation a one-time effort.

If the `file` parameter is given, MTLINE first checks for the file:

- if the `file` exists, MTLINE checks if the RLGC data stored in the `file` matches the MTLINE 2-D field solver input. If it matches, the data is re-used. If it does not match, a new set of RLGC data is generated and the `file` is over-written.
- If the `file` does not exist, an RLGC model is generated by the field solver and the output is stored in `file`.

If the `file` parameter is not given, RLGC data is stored in the file `%C.rlgc` after the simulation.

The following diagram displays a cross-section of the 2-D solver:



The following shows an example model card:

```
Mxyz in1 out1 in2 out2 in3 out3 in4 out4
+ gnd gnd my_model len=100mm

model my_model mtlne
+ file="sim_results.dat" fmax=10e9
```

```
+  linetype = sublossline
+    modeltype = wideband
+    numgnd = 2
+    numlayer = 3

+  er = [12.9  4.5  1]
+    layerthickness = [200e-6  300e-6  300e-6]
+    dlosstype = tangent
+    dloss = [0.0016  0.008  0]

+  linewidth = [100e-6  100e-6  100e-6  300e-6]
+    linethickness = [20e-6]
+    lineheight = [200e-6  200e-6  200e-6  500e-6]
+    linespace=[100e-6  100e-6  -400e-6 ]
+    linesigma = 5.76e7

+  gndthickness = [20e-6  20e-6]
+    gndsigma = 5.76e7
```

S-Parameter Data

MTLINE also accepts an S-parameter data file to describe a transmission line system. Even though both MTLIN and NPORT accept S-parameter data, simulation accuracy can be different. A transmission line system with long delay often requires certain numerical manipulation to achieve better simulation accuracy, which you can achieve only by using MTLIN.

You can specify an S-parameter data file describing a transmission line system using the `file` parameter. MTLIN converts the frequency dependent S-parameter to frequency dependent RLGC data and stores the results in the file `%C.rlgc` for reuse in subsequent simulations.

If the `file` parameter corresponds to S-parameter data, MTLIN first checks the existence of the file `%C.rlgc` to determine if the S-to-RLGC extraction has been performed in a previous simulation.

The S-parameter data file formats supported are Touchstone, Spectre and Citi.

The physical length of the line must also be specified using the `len` parameter.

The ordering of the S-parameter input file should be in the format of input ports followed by the output ports of the transmission line system, or *Pin1, Pin2, Pin3, ..., Pout1, Pout2, Pout3, ...*.

TLINE Parameters

MTLINE has a more accurate and robust modeling algorithm than TLINE. However, to ease customer migration, MTLINE supports the old single-conductor TLINE parameters.

Due to a name conflict, the TLINE parameter `r` has been renamed as `seriesr` in MTLINE, and the TLINE parameter `g` has been renamed as `shuntg` in MTLINE.

In addition, the terminal maps between TLINE and MTLINE are different. The following TLINE syntax

```
Name ( t1 b1 t2 b2 ) tline <parameter=value> ...
```

should be mapped to the following MTLINE syntax

```
Name ( t1 t2 b1 b2 ) mtline <parameter=value> ...
```

For a detailed explanation of TLINE parameters, see `spectre -h tline`.

Input/Output Buffer Modeling Using IBIS

You can use IBIS to model integrated circuit drivers, receivers, and packaging, as well as whole circuit boards, containing multiple IBIS components. Parameters of IBIS model can be either obtained by transistor-level circuit simulation, or directly measured by the actual integrated circuit. Modeling with IBIS:

- is faster than the corresponding transistor level simulation since it is based on behavioral data, and ignores detailed circuit topology.
- does not reveal any sensitive information about the design technology or underlying fabrication process so the vendor's intellectual property is protected.

The IBIS buffer primitive is used to model IBIS drivers and receivers of various types. The rest of the IBIS file content, including series models, package parasitics, external package and board descriptions is modeled by subcircuits, which include resistors, inductors, capacitors, controlled sources, and transmission lines. Differential buffers are modeled by a pair of IBIS buffer primitives. Multi-stage buffers and other advanced buffer types are modeled by multiple IBIS buffer primitives, one for each buffer stage, added model, or submodel.

The IBIS buffer primitive can be used with or without a model card. Using a model card enables model sharing, which is an important feature in IBIS since a lot of pins share the same model characteristics. Using IBIS buffer primitive without a model card allows you to avoid translation of IBIS file into Spectre format, since all the required model information is obtained directly from the specified model section of the IBIS file.

IBIS Translator Model

The IBIS2SUBCKT utility translates IBIS data files into a Spectre netlist format. Input files must comply with IBIS standard, and have the extension `.ibs`, `.pkg`, or `.ebd`. The output file contains subcircuit definitions for all components described in the input files, as well as all necessary model cards.

Syntax

```
ibis2subckt -in IBIS files -out subckt file -corner {typ|min|max} -swsel int  
           -mdsel int
```

where

<code>-in</code>	Specifies the list of input files.
<code>-out</code>	Specifies the name of the output file.
<code>-corner</code>	Specifies the IBIS model corner for which the model is created. Default value: <code>typ</code>
<code>-swsel</code>	Defines the position of series switches. Default value: 1
<code>-mdsel</code>	Specifies the actual models from the IBIS model selector lists. Default value: 1

Example of an IBIS Component Subcircuit

In Figure 1, component pin terminals are shown on the left hand side of the subcircuit symbol. They are connected to the die pad terminals of the buffers through the package circuits. In this case, the simplest package model is shown consisting of lumped R, L, and C elements. IBIS specification allows for more advanced package models, with multiple stubs of lumped or distributed RLC, or coupling RLC matrices, similar to Spectre `mtline` primitive. Signal terminals of the buffers are connected to the signal terminals of the component subcircuit, shown on the right hand side. These terminals represent digital signals internal to the component. The number of signals depend on the buffer type. Output buffer has only one signal called `out`. Depending on the state of this signal (0, or 1V) the buffer drives its die pad terminal to low or high voltage. Input buffer has an `in` signal. The state of this signal changes when the die pad voltage crosses the threshold. The I/O buffer contains both driver and receiver, and therefore has three signal terminals: `in` signal is the output of the receiver; `out` is input for the driver; `enable` can be used to disable the driver by turning it into high impedance state. The terminator buffer has no signals and serves as an RC load for corresponding pin. IBIS standard also allows series or `series_switch` connectors between die pads. They are modeled by a subcircuit containing RLC or VCCS elements.

Figure 10-1 IBIS Component Circuit

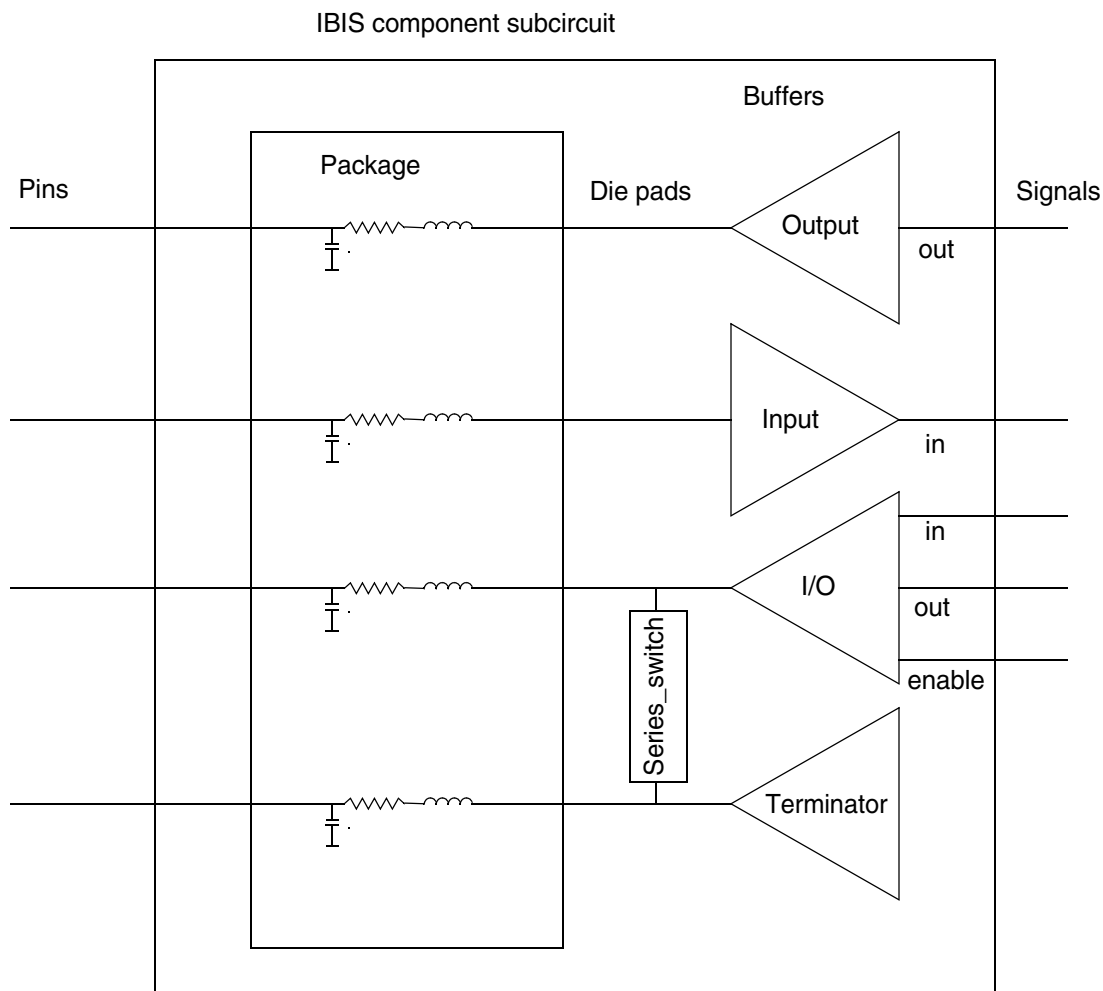
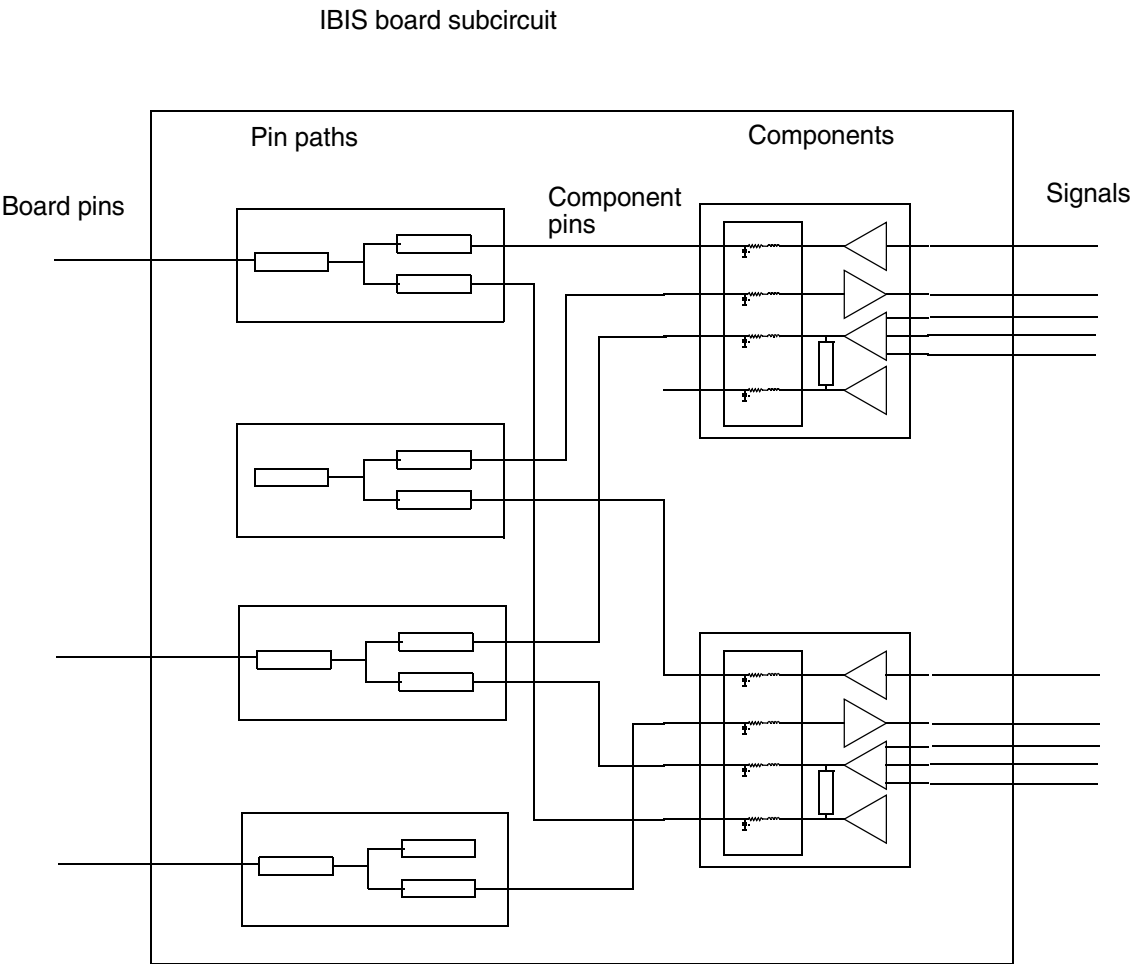


Figure 2 shows an example of an IBIS board subcircuit. Board pins are connected to the component pins through the pin path circuits. Each pin paths consist of a number of stubs connected in series or through the forks. A stub is either transmission line or lumped RLC. Components, which are instantiated on the board, are listed in the reference designation map section of the IBIS board file. Signal terminals of the board subcircuit are directly connected to the component signals.

Figure 10-2 IBIS Board Subcircuit



Analyses

This chapter discusses the following topics:

- [Types of Analyses](#) on page 250
- [Analysis Parameters](#) on page 253
- [Probes in Analyses](#) on page 254
- [Multiple Analyses](#) on page 255
- [Multiple Analyses in a Subcircuit](#) on page 257
- [DC Analysis](#) on page 258
- [AC Analysis](#) on page 261
- [Transient Analysis](#) on page 265
- [Fault Analysis](#) on page 283
- [Pole Zero Analysis](#) on page 414
- [Loopfinder Analysis](#) on page 416
- [Other Analyses \(sens, fourier, dcmatch, and stb\)](#) on page 418
- [Sweep Analysis](#) on page 437
- [Monte Carlo Analysis](#) on page 443
- [Spectre Reliability Analysis](#) on page 467
- [SpectreThermal Analysis](#) on page 535

Types of Analyses

This section gives a brief description of the Spectre® circuit simulator analyses you can specify. Spectre analyses frequently let you sweep parameters, estimate or specify the DC solution, specify options that promote convergence, and select annotation options. You can specify sequences of analyses, any number in any order. For a more detailed description of each analysis and its parameters, consult the Spectre online help (`spectre -h`).

- DC analysis (`dc`)—Finds the DC operating point or DC transfer curves of the circuit.
- AC/small signal analyses
 - AC analysis (`ac`)—Linearizes the circuit about the DC operating point and computes the steady-state response of the circuit to a given small-signal sinusoidal stimulus. This analysis is useful for obtaining small-signal transfer functions.
 - Noise analysis (`noise`)—Linearizes the circuit about the DC operating point and computes the total-noise spectral density at the output. The output can be either a voltage or a current. If you specify an input probe, the Spectre simulator computes the transfer function and the equivalent input-referred noise for a noise-free network.
 - Transfer function analysis (`xf`)—Linearizes the circuit about the DC operating point and performs a small-signal analysis. It calculates the transfer function from every source in the circuit to a specified output. The output can be either a voltage or a current.
 - S-parameter analysis (`sp`)—Linearizes the circuit about the DC operating point and computes S-parameters of the circuit taken as an N-port. You define the ports of the circuit with `port` statements. You must place at least one `port` statement in the circuit. The Spectre simulator turns on each port sequentially and performs a linear small-signal analysis. The Spectre simulator converts the response of the circuit at each port into S-parameters.
- Transient analyses
 - Transient analysis (`tran`)—Computes the transient response of the circuit over a specified time interval. You can specify initial conditions for this analysis. If you do not specify initial conditions, the analysis starts from the DC steady-state solution. You can influence the speed of the simulation by setting parameters that control accuracy requirements and the number of data points saved. For more information about the transient analysis, see [Transient Analysis](#) on page 265.
 - Time-domain reflectometer analysis (`tdr`)—Linearizes the circuit about the DC operating point and computes the reflection and transmission coefficients versus time. This is the time-domain equivalent of the S-parameter analysis.

- Pole Zero analysis (`pz`)— Linearizes the circuit about the DC operating point and computes the poles and zeros of the linearized network.
- RF analyses
 - Envelope Analysis (`envlp`) — Computes the envelope response of a circuit. The simulator automatically determines the clock period by looking through all the sources with the specified name. Envelope-following analysis is most efficient for circuits where the modulation bandwidth is orders of magnitude lower than the clock frequency. This is typically the case, for example, in circuits where the clock is the only fast varying signal and other input signals have a spectrum whose frequency range is orders of magnitude lower than the clock frequency. For another example, the down conversion of two closely placed frequencies can also generate a slow-varying modulation envelope. The analysis generates two types of output files, a voltage versus time (`td`) file, and an amplitude/phase versus time (`fd`) file for each of specified harmonic of the clock fundamental.
 - Harmonic Balance Steady State Analysis (HB) — Uses harmonic balance (in the frequency domain) to compute the response of circuits that have either one fundamental frequency (periodic steady-state, PSS) or that have multiple fundamental frequencies (Quasi-Periodic Steady State, QPSS). The simulation time required for an HB analysis is independent of the time-constants of the circuit. This analysis also determines the circuit's periodic or quasi-periodic operating point, which can then be used during a periodic or quasi-periodic time-varying small-signal analysis, such as HBAC or HBnoise.
 - Periodic Analyses — Spectre RF adds periodic large (PSS) and small-signal analyses (PAC, PSP, PXF, Pnoise, and Pstb) to Spectre simulation.
 - Quasi-Periodic Analyses — Spectre RF adds quasi-periodic large (QPSS) and small-signal analyses (QPAC, QPSP, QPXF, and QPnoise) to Spectre L simulation. For more information about the quasi-periodic analyses.
- Other analyses
 - Sensitivity analysis (`sens`)—Determines the sensitivity of output variables to input design parameters. The results are expressed as a ratio of the change in an output analysis variable to the change in an input design parameter. The output for the `sens` command is sent to the rawfile or to an ASCII file. For more information about sensitivity analysis, see [“Sensitivity Analysis on page 418”](#).
 - Fourier analysis (`fourier`)—Measures the Fourier coefficients of two different signals at a specified fundamental frequency without loading the circuit. The algorithm used is based on the Fourier integral rather than the discrete Fourier transform and therefore is not subject to aliasing. Even on broad-band signals, it computes a small number of Fourier coefficients accurately and efficiently.

Therefore, this Fourier analysis is suitable on clocked sinusoids generated by sigma-delta converters, pulse-width modulators, digital-to-analog converters, sample-and-holds, and switched-capacitor filters as well as on the traditional low-distortion sinusoids produced by amplifiers or filters.

- ❑ DC Match Analysis (`dcmatch`)—Computes the statistical deviation in the DC operating point of the circuit caused by device mismatch. For more information about the `dcmatch` analysis, see [DC Match Analysis](#) on page 423
- ❑ Stability Analysis (`stb`)—Linearizes the circuit about the DC operating point and computes loop gain, gain margin, and phase margin for a specific feedback loop or an active device. The stability of the circuit can be determined from the loop gain waveform. The `probe` parameter must be specified to perform stability analysis.

■ Advanced analyses

- ❑ Sweep analysis (`sweep`)—Sweeps a parameter executing a list of analyses (or multiple analyses) for each value of the parameter. The sweeps can be linear or logarithmic. Swept parameters return to their original values after the analysis. Sweep statements can be nested. For more information about the sweep analysis, see [Sweep Analysis](#).
- ❑ Fault analysis (`fault`)—Provides a transistor-level simulation capability that can be enabled in an analog test methodology to improve test coverage by identifying critical test patterns. Spectre transient fault analysis is very fast in handling a large numbers of faults. Spectre direct fault analysis provides high accuracy results when full fault analysis precision is required. For more information, see [Fault Analysis](#).
- ❑ Monte Carlo analysis (`montecarlo`)—Varies netlist parameters according to specified distributions and correlations, runs nested child analyses, and extracts specified circuit-performance measurements. You can apply both process and device-to-device mismatch variations and tag device instances as correlated or “matched pairs.” Use the Cadence analog circuit design environment Calculator expressions to measure the circuit performance. You can use the analog design environment graphics tools to plot scalar performance data, such as slew rates and bandwidths, as a histogram or scattergram. You can also display waveform data as cloud (family) plots. For more information about the Monte Carlo analysis, see [Monte Carlo Analysis](#) on page 443. For more information about using the Monte Carlo analysis with the analog design environment, see the *Advanced Analysis Tools User Guide*.

- Hot-electron degradation analysis—Lets you control the age of the circuit when simulating hot-electron degradation. For more information about the hot-electron degradation analysis, see [“Special Analysis \(Hot-Electron Degradation\)”](#) on page 213.

Analysis Parameters

You specify parameter values for analysis and control statements just as you specify those for component and model statements, but many analysis parameters have no assigned default values. You must assign values to these parameters if you want to use them. To assign values to these parameters, simply follow the parameter keyword with an equal sign (=) and your selected value. For example, to set the points per decade (`dec`) value to 10, you enter `dec=10`.

Note: Some parameters require text strings, usually filenames, as values. You must enclose these text strings in quotation marks to use them as parameter values.

When analysis parameters do have default values, these values are given in the parameter listings for that analysis in the Spectre online help (`spectre -h`).

A listing like the following tells you that the default value for parameter `lin` is 50 steps:

```
lin=50                      Emission coefficient parameters
```

Specifying Parameter Defaults in a File

You can use the `+paramdefault` command-line option to enable Spectre to read and apply the default values of parameters from a specified file. This enables you to specify the default values of the analysis parameters without the need to modify the netlist.

The syntax to specify the `+paramdefault` command-line option is as follows:

```
% spectre +paramdefault <filename> ....
```

`<filename>` is the name of the file containing the default values for parameters. The file should contain only the primitive analysis name (and/or option analysis), parameter name, and parameter value in one line. The following is an example of a parameter default file:

```
# Example comment for parameter defaults
tran compression wilddcardonly
tran annotate estimated
options wfmaxsize 30GB
```

The parameter value can be a string or double. For double values, scientific notation (for example, 1.54E+06) and unit suffix (for example, 1.54M) are supported. Expressions are not supported.

Spectre reads the parameter defaults from the specified file and applies them before applying the netlist parameters. Therefore, if the same parameter is specified in the netlist, it will have higher priority.

You can use the `+paramdefault` command-line option multiple times to specify multiple files. For example,

```
% spectre +paramdefault file1 +paramdefault file2
```

You can use the `=paramdefault <filename>` command-line option to read the specified file and ignore all previously specified files. The `=paramdefault` command-line option ignores only those files (specified using the `+paramdefault` command-line option) that are specified before it at the command line. For example:

```
% spectre +paramdefault file1 =paramdefault file2 +paramdefault file3
```

In the above example, only `file1` will be ignored because it has been specified before the `=paramdefault` option.

You can use the `-paramdefault` command-line option to disable the reading of any parameter defaults specified.

Probes in Analyses

Some Spectre analyses require that you set probes. Remember the following guidelines when you set probes:

- You can name any component instance as a probe.
- If the probe component measures a branch current, you can use it as either a current probe or a voltage probe. Component instances that do not calculate branch currents can be used only as voltage probes.
- If the probe component has more than two terminals, you specify which pair of terminals to use as the probe by specifying a port of the probe. In the following instance statement, port 1 is nodes 5 and 8, and port 2 is nodes 2 and 4.

```
bjt1 5 8 2 4 bmod1
```

- If the probe component measures more than one branch current, you specify which branch current to use as the probe by specifying a port. In the following instance statement, current port 1 is the branch from node 4 to node 5, and port 2 is the branch from node 8 to node 9.

```
tline2 4 5 8 9 tline
```

- Every component has a default probe type and port number.

In the following example, the netlist contains a resistor named `Rocm` and a voltage source named `Vcm`. These components are used as probes for the `noise` analysis statement. The parameters `oprobe` and `iprobe` specify the probe components, and the parameters `oportv` and `iporvtv` specify the port numbers.

```
cmNoise noise start=1k stop=1G dec=10 oprobe=Rocm oportv=1 iprobe=Vcm iportv=1
```

Multiple Analyses

This netlist demonstrates the Spectre simulator's ability to run many analyses in the order you prefer. In this example, the Spectre simulator completely characterizes an operational amplifier in one run. In analysis `OpPoint`, the program computes the DC solution and saves it to a state file whose name is derived from the name of the netlist file. On subsequent runs, the Spectre simulator reads the state information contained in this state file and speeds analysis by using this state information as an initial estimate of the solution.

Analysis `Drift` computes DC solutions as a function of temperature. The Spectre simulator computes the solution at the initial temperature and saves this solution to a state file to use as an estimate in the next analysis and in subsequent simulations.

Analysis `XferVsTemp` computes the small-signal characteristics of the amplifier versus temperature. Analysis `XferVsTemp` starts up quickly because it begins with the initial temperature of the DC solution that was placed in a state file by the previous analysis.

Analysis `LoopGain` computes the loop gain of an amplifier in closed-loop configuration. Analysis `LoopGain` starts quickly because it begins with the initial temperature of the DC solution that was placed in a state file during analysis `OpPoint`.

Analysis `XferVsFreq` computes several small-signal quantities of interest such as closed-loop gain, the rejection ratio of the positive and negative power supply, and output resistance. The analysis again starts quickly because the operating point remains from the previous analysis.

Analysis `StepResponse` computes the step response that permits the measurement of the slew-rate and settling times. The `alter` statement `please4` then changes the input stimulus from a pulse to a sine wave. Finally, the Spectre simulator computes the response to a sine wave in order to calculate distortion.

```
// ua741 operational amplifier
global gnd vcc vee
simulator lang=spectre

Spectre options audit=detailed limit=delta maxdeltav=0.3 \
    save=lvlpub nestlvl=1

// ua741 operational amplifier
model NPNdiode diode is=.1f imax=5m
model NPNbjt bjt type=npn bf=80 vaf=50 imax=5m \
    cje=3p cjc=2p cjs=2p tf=.3n tr=6n rb=100
model PNPbjt bjt type=pnv bf=10 vaf=50 imax=5m \
    cje=6p cjc=4p tf=1n tr=20n rb=20

subckt ua741 (pIn nIn out)
// Transistors
```

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```
Q1 1 pIn 3 vee NPNbjt
Q2 1 nIn 2 vee NPNbjt
Q3 5 16 3 vcc PNPbjt
Q4 4 16 2 vcc PNPbjt
Q5 5 8 7 vee NPNbjt
Q6 4 8 6 vee NPNbjt
Q7 vcc 5 8 vee NPNbjt
Q9 16 1 vcc vcc PNPbjt
Q14 vcc 13 15 vee NPNbjt
Q16 vcc 4 9 vee NPNbjt
Q17 11 9 10 vee NPNbjt
Q18 13 12 17 vee NPNbjt
Q20 vee 17 14 vcc PNPbjt
Q23 vee 11 17 vcc PNPbjt

// Diodes
Q8 vcc 1 NPNdiode
Q19 13 12 NPNdiode

// Resistors
R1 7 vee resistor r=1k
R2 6 vee resistor r=1k
R3 8 vee resistor r=50k
R4 9 vee resistor r=50k
R5 10 vee resistor r=100
R6 12 17 resistor r=40k
R8 15 out resistor r=27
R9 14 out resistor r=22

// Capacitors
C1 4 11 capacitor c=30p

// Current Sources
I1 16 vee isource dc=19u
I2 vcc 11 isource dc=550u
I3 vcc 13 isource dc=180u
ends ua741

// Sources
Vpos vcc gnd vsource dc=15
Vneg vee gnd vsource dc=-15
Vin pin gnd vsource type=pulse dc=0 \
    val0=0 val1=10 width=100u period=200u rise=2u \
    fall=2u tdl=0 tau1=20u td2=100u tau2=100u \
    freq=10k ampl=10 delay=5u \
    file="sine10" scale=10.0 stretch=200.0e-6
Vfb nin out vsource

// Op Amps
OA1 pin nin out ua741

// Resistors
Rload out gnd resistor r=10k

// Analyses

// DC operating point
pleasel alter param=temp value=25 annotate=no
OpPoint dc print=yes readns="%C:r.dc25"
write="%C:r.dc25"

// Temperature Dependence
Drift dc start=0 stop=50.0 step=1 param=temp \
    readns="%C:r.dc0" write="%C:r.dc0"
XferVsTemp xf start=0 stop=50 step=1 probe=Rload \
    param=temp freq=1kHz readns="%C:r.dc0"
```

```
// Gain
  please2 alter dev=Vfb param=mag value=1 annotate=no
  LoopGain ac start=1 stop=10M dec=10 readns="%C:r.dc25"
  please3 alter dev=Vfb param=mag value=0 annotate=no
// XF
  XferVsFreq xf start=1_Hz stop=10M dec=10 probe=Rload
// Transient
  StepResponse tran stop=250u
  please4 alter dev=Vin param=type value=sine
  SineResponse tran stop=150u
```

Multiple Analyses in a Subcircuit

You might want to run complex sets of analyses many times during a simulation. To simplify this process, you can group the set of analyses into a subcircuit. Because subcircuit definitions can contain analyses and control statements, you can put the analyses inside a single subcircuit and perform the multiple analyses with one call to the subcircuit. The Spectre simulator performs the analyses in the order you specify them in the subcircuit definition. Generally, you do not mix components and analyses in the same subcircuit definition. For more information about formats for subcircuit definitions and subcircuit calls, see [Chapter 7, “Analyses.”](#)

Example

The following example illustrates how to create and call subcircuits that contain analyses.

Creating Analysis Subcircuits

```
subckt sweepVcc()
  parameters start=0 stop=10 Ib=0 omega=1G steps=100
  setIbb alter dev=Ibb param=dc value=Ib
  SwpVccDC dc start=start stop=stop dev=Vcc lin=steps/2SwpVccAC ac dev=Vcc
  start=start stop=stop lin=steps \freq=omega/6.283185
ends sweepVcc
```

This example defines a subcircuit called `sweepVcc` that contains the following:

- A list of parameters with default values for `start`, `stop`, `Ib`, `omega`, and `steps`

This list of defaults is optional.

These defaults are for the subcircuit call. For example, if you call `sweepVcc` and do not specify values for the `start` and `stop` parameters in the subcircuit call, the sweeps for analyses `SwpVccDC` and `SwpVccAC` start at 0 and end at 10, the values specified as defaults. If, however, you specify `start=1` and `stop=5` as parameter values in the

subcircuit call, the `start` and `stop` parameters in `SwpVccDC` and `SwpVccAC` take the values 1 and 5, respectively.

- A control statement, `setIbb`, which alters the `dc` parameter of the component named `Ibb` to the numerical value of `Ib`
- Two analysis statements, `SwpVccDC` and `SwpVccAC`, which run a DC analysis followed by an AC analysis

Calling Analysis Subcircuits

Each subcircuit call for `sweepVcc` in the netlist causes all the analyses in the `sweepVcc` to be performed. Each of the following statements is a subcircuit call to subcircuit `sweepVcc`:

```
Ibb1uA sweepVcc stop=2 Ib=1u
Ibb3uA sweepVcc stop=2 Ib=3u
Ibb10uA sweepVcc stop=2 Ib=10u
Ibb30uA sweepVcc stop=2 Ib=30u
Ibb100uA sweepVcc stop=2 Ib=100u
```

Note the following important syntax features:

- Each subcircuit call has a unique name.
- Each subcircuit call overrides the default values for the `stop` and `Ib` parameters.
- The `start`, `steps`, and `omega` parameters are not defined in the subcircuit calls. They take the default values assigned in the subcircuit.

DC Analysis

The DC analysis finds the DC operating point or DC transfer curves of the circuit. To generate transfer curves, specify a parameter and a sweep range. The swept parameter can be circuit temperature, a device instance parameter, a device model parameter, a netlist parameter, or a subcircuit parameter for a particular subcircuit instance. You can sweep the circuit temperature by giving the parameter name as `param=temp` with no `dev`, `mod`, or `sub` parameter. You can sweep a top-level netlist parameter by giving the parameter name with no `dev`, `mod`, or `sub` parameter. You can sweep a subcircuit parameter for a particular subcircuit instance by specifying the subcircuit instance name with the `sub` parameter and the subcircuit parameter name with the `param` parameter. After the analysis has completed, the modified parameter returns to its original value.

The syntax is as follows:

```
Name dc parameter=value ...
```

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You can specify sweep limits by giving the end points or by providing the center value and the span of the sweep. Steps can be linear or logarithmic, and you can specify the number of steps or the size of each step. You can give a step size parameter (`step`, `lin`, `log`, `dec`) and determine whether the sweep is linear or logarithmic. If you do not give a step size parameter, the sweep is linear when the ratio of stop to start values is less than 10, and logarithmic when this ratio is 10 or greater. If you specify the `oppoint` parameter, Spectre computes and outputs the linearized model for each nonlinear component.

Nodesets help find the DC or initial transient solution. You can supply them in the circuit description file with `nodeset` statements, or in a separate file using the `readns` parameter. When nodesets are given, Spectre computes an initial guess of the solution by performing a DC analysis while forcing the specified values onto nodes by using a voltage source in series with a resistor whose resistance is `rforce`. Spectre then removes these voltage sources and resistors and computes the true solution from this initial guess.

Nodesets have two important uses. First, if a circuit has two or more solutions, nodesets can bias the simulator towards computing the desired one. Second, they are a convergence aid. By estimating the solution of the largest possible number of nodes, you might be able to eliminate a convergence problem or dramatically speed convergence.

When you simulate the same circuit many times, we suggest that you use both the `write` and `readns` parameters and give the same filename to both parameters. The DC analysis then converges quickly even if the circuit has changed somewhat since the last simulation, and the nodeset file is automatically updated.

You may specify values to force for the DC analysis by setting the parameter `force`. The values used to force signals are specified by using the `force` file, the `ic` statement, or the `ic` parameter on the capacitors and inductors. The `force` parameter controls the interaction of various methods of setting the force values. The effects of individual settings are

<code>force=none</code>	Any initial condition specifiers are ignored.
<code>force=node</code>	The <code>ic</code> statements are used, and the <code>ic</code> parameter on the capacitors and inductors are ignored.
<code>force=dev</code>	The <code>ic</code> parameters on the capacitors and inductors are used, and the <code>ic</code> statements are ignored.
<code>force=all</code>	Both the <code>ic</code> statements and the <code>ic</code> parameters are used, with the <code>ic</code> parameters overriding the <code>ic</code> statements.

If you specify a `force` file with the `readforce` parameter, force values read from the file are used, and any `ic` statements are ignored.

Once you specify the force conditions, the Spectre simulator computes the DC analysis with the specified nodes forced to the given value by using a voltage source in series with a resistor whose resistance is `rforce` (see `options`).

Selecting a Continuation Method

The Spectre simulator normally starts with an initial estimate and then tries to find the solution for a circuit using the Newton-Raphson method. If this attempt fails, the Spectre simulator automatically tries several continuation methods to find a solution and tells you which method was successful. Continuation methods modify the circuit so that the solution is easy to compute and then gradually change the circuit back to its original form. Continuation methods are robust, but they are slower than the Newton-Raphson method.

If you need to modify and resimulate a circuit that was solved with a continuation method, you probably want to save simulation time by directly selecting the continuation method you know was previously successful.

You can select the continuation method with the `homotopy` parameter of the `set` or `options` statements. In addition to the default setting, `all`, five settings are possible for this parameter – `gmin` stepping (`gmin`), source stepping (`source`), the pseudotransient method (`ptran`), damped pseudotransient method (`dptran`), and `none`. You can prevent the use of continuation methods by setting the `homotopy` parameter to `none`.

From the MMSIM6.2.1 release onwards, you can specify more than one homotopy method and the Spectre circuit simulator tries them in the order in which they are specified.

In the following example, the Spectre circuit simulator tries the `gmin` stepping solution to help dc converge. If it fails to converge, then Spectre tries the `source` stepping solution.

```
dc1 dc homotopy=[gmin source]
```

Enabling Fast DC Simulation

In some situations, especially for larger circuits, it can be difficult to converge to the exact DC operating point, and Spectre can spend a significant time converging to the final solution. The `+fastdc` command-line option enables you to speed up the DC simulation in Spectre and APS for large-scale circuits and for cases where DC convergence is very slow, or there is a difficulty in DC convergence. The DC solution from `+fastdc` is generally an approximate solution, but it is sufficient to start transient analysis. Since the solution is not the exact DC, measurements made at the DC point, or a simulation that requires a very accurate DC solution may have problems with the `+fastdc` command-line option.

The `+fastdc` command-line option accepts a set of values, ranging from 0-4. The default is 4, which is the fastest solution. 0 is the most accurate, and is very close to the exact DC solution, and as a result, it is the slowest of the 5 settings. It is recommended to first use the `+fastdc` command-line option when DC convergence is a problem, either slow or difficult. Then, if the circuit or measurements require a more accurate solution reduce the value of `+fastdc` option.

The fast DC simulation can be turned on from the command line as shown below.

```
% spectre +fastdc ...  
% spectre +aps +fastdc ...
```

AC Analysis

The AC analysis linearizes the circuit about the DC operating point and computes the response to all specified small sinusoidal stimulus. For more information on specifying small sinusoidal stimulus, see [Chapter 3, Analysis Statements](#), in *Spectre Circuit Simulator Reference*.

The Spectre simulator can perform the analysis while sweeping a parameter. The parameter can be frequency, temperature, component instance parameter, component model parameter, or netlist parameter. If changing a parameter affects the DC operating point, the operating point is recomputed on each step. You can sweep the circuit temperature by giving the parameter name as `temp` with no `dev` or `mod` parameter. You can sweep a netlist parameter by giving the parameter name with no `dev` or `mod` parameter. After the analysis has completed, the modified parameter returns to its original value.

The syntax is as follows:

```
Name ac parameter=value ...
```

You can specify sweep limits by giving the end points or by providing the center value and the span of the sweep. Steps can be linear or logarithmic, and you can specify the number of steps or the size of each step. You can give a step size parameter (`step`, `lin`, `log`, `dec`) to determine whether the sweep is linear or logarithmic. If you do not give a step size parameter, the sweep is linear when the ratio of stop to start values is less than 10, and logarithmic when this ratio is 10 or greater. All frequencies are in Hertz.

The small-signal analysis begins by linearizing the circuit about an operating point. By default, this analysis computes the operating point if it is not known or recomputes it if any significant component or circuit parameter has changed. However, if a previous analysis computed an operating point, you can set `prevoppoint=yes` to avoid recomputing it. For example, if you use this option when the previous analysis was a transient analysis, the operating point is the state of the circuit on the final time point.

S-Parameter Analysis

The S-Parameter (sp) analysis is the most useful linear small signal analysis for low noise amplifiers. It linearizes the circuit about the DC operating point and computes the S-parameters of the circuit taken as an N-port. In the netlist, the `port` statements define the ports of the circuit. Each active port is turned on sequentially, and a linear small-signal analysis is performed. Spectre converts the response of the circuit at each active port into S-parameters and outputs these parameters. There must be at least one active port statement in the circuit.

If the list of active ports is specified with the `ports` parameter, the ports are numbered sequentially from one in the order given. Otherwise, all ports present in the circuit are active, and the port numbers used are those that were assigned on the port statements.

You can use the `file` parameter to specify a file that enables Spectre to output the S-parameters into the specified file, which can later be read-in by the `nport` component. For example:

```
sp sp ports=[RF] file=my_file
```

In the above example, Spectre will output the S-parameters to the file `my_file`.

By default, Spectre outputs the data in `spectre` format. You can also output the data in `touchstone` format by using the `datafmt` parameter with the `sp` analysis statement in the netlist file.

Spectre can perform AC/SP analysis while sweeping a parameter. The parameter can be frequency, temperature, component instance parameter, component model parameter, or netlist parameter. If changing a parameter affects the DC operating point, the operating point is recomputed at each step. After the analysis is complete, the modified parameter returns to its original value.

You can define sweep limits by specifying the end points or the center value and span of the sweep. Steps can be linear or logarithmic, and you can specify the number of steps or the size of each step. You can specify a step size parameter (`step`, `lin`, `log`, or `dec`) to determine whether the sweep is linear or logarithmic. If you do not specify a step size parameter, the sweep is linear when the ratio of stop to start values is less than 10 and logarithmic when this ratio is 10 or greater. All frequencies are in Hertz. For example:

```
sp sp ports[RF PORT0] start=500M stop=4G lin=8 file=my_file
```

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The above statement will output the following in the file `my_file`.

```
S-parameter data file my_file.
; Tue Mar  8 16:06:32 2016
; Number of ports is 2

reference resistance
    port2 = 50.000000
    port1 = 50.000000

format freq:  s1:1(real,imag)  s2:1(real,imag)
               s1:2(real,imag)  s2:2(real,imag)

5.00000000e+08:    0.135545,    -0.28255    -5.56159,    2.66473
                  0.0286224,    -0.00325088   -0.17437,    0.0375907
5.70000000e+08:    0.105948,    -0.303501   -5.27849,    2.87959
                  0.0281592,    -0.00341752   -0.169918,    0.0400223
6.40000000e+08:    0.0761615,    -0.320808   -4.99178,    3.05738
                  0.0276926,    -0.00352527   -0.165409,    0.0418974
7.10000000e+08:    0.0466286,    -0.334701   -4.70627,    3.20058
                  0.0272304,    -0.00357811   -0.160921,    0.043247
7.80000000e+08:    0.0177212,    -0.345472   -4.42593,    3.31223
                  0.0267786,    -0.00358094   -0.156518,    0.0441141
8.50000000e+08:   -0.0102675,    -0.353445   -4.15385,    3.39566
                  0.0263421,    -0.00353915   -0.152251,    0.0445482
9.20000000e+08:   -0.0371224,    -0.358956   -3.89233,    3.45426
                  0.0259243,    -0.00345821   -0.148154,    0.0446008
9.90000000e+08:   -0.0626977,    -0.362333   -3.64292,    3.49136
                  0.0255274,    -0.00334346   -0.144253,    0.0443227
1.06000000e+09:   -0.0869065,    -0.363886   -3.40657,    3.51007
                  0.0251529,    -0.0031999   -0.140562,    0.0437622
```

If `donoise=yes` is specified, the noise correlation matrix is computed. In addition, if the output is specified using `oprobe`, the amount that each noise source contributes to the output is computed. Finally, if an input is also specified (using `iprobe`), the two-port noise parameters are computed (`F`, `Fmin`, `NF`, `NFmin`, `Gopt`, `Bopt`, and `Rn`).

If the `mode` parameter is set to `mm`, differential and common-mode S-parameters (denoted as mixed-mode S-parameters) are calculated. For `mode=mm`, there must be $2N$, with $N > 1$, active port statements in the circuit. The mixed-mode S-parameters are calculated referring to the pairing of the ports, with the port numbers ordered in pair as (1,2) (3,4), and so on in the ports list. With `mode=mm`, Spectre calculates differential-to-differential, differential-to-common, common-to-differential, and common-to-common S-parameters. A combination of mixed-mode and standard S-parameters is calculated if the mode parameter is set to, say, `m12m34s5`. Then, additional differential-to-standard, common-to-standard, standard-to-

differential, and standard-to-common S-parameters are calculated. In the example of mode=m12m34s5, the standard single-end port is port number 5, the two mixed-mode port pairs are (1,2) and (3,4); with Spectre placing restriction of the number on active ports to 5 given in the port list.

Spectre also supports probes in S-parameter analysis. Sprobe is a special component to allow in-situ probing of impedances and S parameters looking out of the two terminals. If the `sprobes` parameter is specified, the parameters `S1`, `S2`, `Z1`, `Z2`, and `StabIndex` of the specified probe are computed and output to a raw file. Here `S1` is the scattering parameter looking left from the probe, `S2` is the scattering parameter looking right from the probe, `Z1` is the impedance looking left from the probe, `Z2` is the impedance looking right from the probe, and `StabIndex` is the stability Index. `Gamma1` and `Gamma2` are the reflection impedance coefficients. However, since `Gamma1=S1` and `Gamma2=S2`, they do not require recalculation.

Sprobe is defined in `spectre.cfg`; therefore, it is automatically included in the Spectre flow.

Sprobe can be specified independently in a single `sp` statement or an `sprobe` and a normal S-parameter analysis can be specified in a single `sp` statement, as shown below.

Single probe calculation in one `sp` analysis

```
sprobe1 (1 2) sprobe
sp0 sp sprobes=[sprobe1] <parameter=value>
```

Probes and normal S-Parameter analysis in a single `sp` statement

```
sprobe1 (1 2) sprobe
sprobe2 (3 4) sprobe
sp0 sp ports=[p1 p2] sprobes=[sprobe1 sprobe2] ...
```

If both `sprobes` and `ports` are specified, `ports` are used to compute the normal S parameters and `sprobes` are used to compute the probe parameters.

The parameters are output in the `<netlist_name>.raw` directory, as follows:

- The standard s, y, z parameters are output to the file `<sp_analysis_name>.sp`.
- The probe `S1`, `S2`, `Z1`, and `Z2` parameters are output to the file `<sp_analysis_name>.sprobe.sp`.
- `StabIndex` is output to the file `<sp_analysis_name>.sprobe-StabIndex.sp`

You can open the file in the Virtuoso Visualization and Analysis tool and plot the results.

For more information on S-Parameter analysis options, refer to *S-Parameter Analysis (sp)* section in the *Spectre Circuit Simulator Reference* manual.

Transient Analysis

The transient analysis computes the transient response of a circuit over the specified interval.

You can adjust transient analysis parameters in several ways to meet the needs of your simulation. Setting parameters that control the error tolerances, the integration method, and the amount of data saved lets you choose between maximum speed and greatest accuracy in a simulation.

This section also tells you about parameters you can set that improve transient analysis convergence.

Sweeping Parameters During Transient Analysis

You can modify temperature, tolerance, and design parameter settings at device, subcircuit, or model level during a transient analysis.



Use dynamic parameters only for design parameters that cannot be changed using a regular pwl source. Using a pwl source-based approach for changing parameters during transient simulation is a more efficient way when compared to using dynamic parameters.

The syntax is:

```
Name tran param=param_name, { param_vec=[ t1 val1 t2 val2...] | param_file=file },  
[ dev=d1 | mod=m1 | sub=s1 ], param_step=time
```

where

Name	Name of the transient analysis.
param=param_name	Dynamic parameter name. The parameter name can be a design parameter, errpreset, method, relref, maxstep, isnoisy, lteratio, reltol, residualtol, vabstol, iabstol, temp, and tnom.
param_vec=[t1 val1 t2 val2...]	Time points and values of the parameter.
param_file=file	File name if the param_vec is defined in a separate file.

`dev=d1 | mod=m1 | sub=s1`

Defines local scope for design parameters. Can be a device model instance (`dev`), device model name (`mod`), or subcircuit instance name (`sub`). Does not apply to `temp`, `reltol`, `residualtol`, `vabstol`, `iabstol`, or `isnoisy`.

`param_step=time`

Specifies whether the `time_value` pair given by the `param_vec` parameter is to be updated in one step, or as a series of steps. See Examples 1 and 2 below. Default value: 0

`faultreadic`

Specifies the file that contains the initial condition (ic) information related to fault sensitivity analysis.

Example 1

```
dotran tran stop=100ns \  
  param=temp param_vec=[0ns 20 50ns 25 100ns 75] param_step=0
```

This statement begins the simulation at a temperature of 20C, increases the temperature to 25C at 50ns, and increases the temperature to 75C at 100ns.

Example 2

```
dotran tran stop=100ns \  
  param=temp param_vec=[0ns 20 50ns 25 100ns 75] param_step=10n
```

This statement increases the temperature by 1C every 10ns from 0ns to 50ns, and by 10C every 10ns from 50ns to 100ns.

Example 3

```
dotran tran stop=100ns \  
  param=reltol param_vec=[0ns 1.0e-3 100ns 1.0e-2] param_step=0 ]
```

In this example, the relative convergence tolerance `reltol` is 1e-3 at the beginning of the simulation, and is changed to 1e-2 at 100ns.

Example 4

```
dotran tran stop=2u \  
  noisefmax=10G noiseseed=1 param=isnoisy param_vec=[0ns 0 500ns 1 ]
```

This statement turns transient noise off from time 0 to 500ns and turns it back on at 500ns.

Example 5

```
pset1 paramset {
    time reltol temp p1 m1:l
    0n    1e-3    27    1    1u
    10n   1e-3    50    2    1u
    20n   1e-4    50    2    2u
    30n   1e-5    75    3    2u
}
dotran tran paramset=pset1 stop=100n param_step=0
```

This paramset statement changes multiple parameters during the transient simulation. The values of the reltol, temp, p1, and m1:l parameters change at the timepoints specified in the paramset table.

Example 6

```
tran2 tran stop=100n param=reltol param_file=reltol.txt
reltol.txt:
; vector definition for reltol
tscale 1.0e-9
time value
10 1e-4
50 1e-3
```

This statement changes the reltol value to 1e-4 at 10ns, and changes the reltol value to 1e-3 at 50ns.

Balancing Accuracy and Speed

The following list displays the Spectre circuit simulator parameters that trade accuracy for speed. See `spectre -h options` for more information on any of these parameters.

- Tolerance control parameters – reltol, vabstol, and iabstol
- Transient control parameters – errpreset, relref, lteratio, method, and maxstep
- Parasitic node reduction parameter – maxrsd

The errpreset Parameter

errpreset is a transient analysis parameter that works in a way similar to speed except that it has fewer settings and controls fewer parameters. You can set errpreset to three different values:

- liberal

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- moderate
- conservative

At `liberal`, the simulation is fast but less accurate. The `liberal` setting is suitable for digital circuits or analog circuits that have only short time constants. At `moderate`, the default setting, simulation accuracy approximates a SPICE2 style simulator. At `conservative`, the simulation is the most accurate but also slowest. The `conservative` setting is appropriate for sensitive analog circuits. If you still require more accuracy than that provided by `conservative`, tighten error tolerance by setting `reltol` to a smaller value.

Description of `errpreset` Parameter Settings

The effect of `errpreset` on other parameters is shown in the following table. In this table, $T = \text{stop} - \text{start}$.

<code>errpreset</code>	<code>reltol</code>	<code>relref</code>	<code>method</code>	<code>maxstep</code>	<code>Iteratio</code>
<code>liberal</code>	<code>×10.0</code>	<code>sigglobal</code>	<code>trapgear2</code>	<code>Interval/50</code>	<code>3.5</code>
<code>moderate</code>	<code>×1.0</code>	<code>sigglobal</code>	<code>traponly</code>	<code>Interval/50</code>	<code>3.5</code>
<code>conservative</code>	<code>×0.1</code>	<code>alllocal</code>	<code>gear2only</code>	<code>Interval/100</code>	<code>10.0</code>

The description in the previous table has the following exceptions:

- The `errpreset` parameter sets the value of `reltol` as described in the table, except that the value of `reltol` cannot be larger than 0.01.
- Except for `reltol` and `maxstep`, `errpreset` does not change the value of any parameters you have specified.
- With `maxstep`, the specified value in the preceding table is an upper bound. You can always specify a smaller `maxstep` value.

If you need to check the `errpreset` settings for a simulation, you can find these values in the log file.

Uses for `errpreset`

You adjust `errpreset` to the speed and accuracy requirements of a particular simulation. For example, you might set `errpreset` to `liberal` for your first simulation to see if the circuit works. After debugging the circuit, you might switch to `moderate` to get more accurate

results. If the application requires high accuracy, or if you want to verify that the `moderate` solution is reasonable, you set `errpreset` to `conservative`.

You might also have different `errpreset` settings for different types of circuits. For logic gate circuits, the `liberal` setting is probably sufficient. A `moderate` setting might be better for analog circuits. Circuits that are sensitive to errors or circuits that require exceptional accuracy might require a `conservative` setting.

Tolerance Control Parameters

You can control the accuracy of the solution to the discretized equation by setting the `reltol` and `xabstol` (where *x* is the access quantity, such as *v* or *i*) parameters in an `options` or `set` statement. These parameters determine how well the circuit conserves charge and how accurately the Spectre simulator computes circuit dynamics and steady-state or equilibrium points.

You can set the integration error or the errors in the computation of the circuit dynamics (such as time constants), relative to `reltol` and `abstol` by setting the `lteratio` parameter.

$$\text{Tolerance}_{\text{NR}} = \text{abstol} + \text{reltol} * \text{Ref}$$

$$\text{Tolerance}_{\text{LTE}} = \text{Tolerance}_{\text{NR}} * \text{lteratio}$$

The `Ref` value is determined by your setting for `relref`, the relative error parameter, as explained in [“Adjusting Relative Error Parameters”](#) on page 173.

In the previous equations, $\text{Tolerance}_{\text{NR}}$ is a convergence criterion that bounds the amount by which Kirchhoff’s Current Law is not satisfied as well as the allowable difference in computed values in the last two Newton-Raphson (NR) iterations of the simulation. $\text{Tolerance}_{\text{LTE}}$ is the allowable difference at any time step between the computed solution and a predicted solution derived from a polynomial extrapolation of the solutions from the previous few time steps. If this difference is greater than $\text{Tolerance}_{\text{LTE}}$, the Spectre simulator shortens the time step until the difference is acceptable.

From the previous equations, you can see that tightening `reltol` to create more strict convergence criteria also diminishes the allowable local truncation error ($\text{Tolerance}_{\text{LTE}}$). You might not want the truncation error tolerance tightened because this adjustment can increase simulation time. You can prevent the decrease in the time step by increasing the `lteratio` parameter to compensate for the tightening of `reltol`.

Adjusting Relative Error Parameters

You determine the treatment of the relative error with the `relref` parameter. The `relref` parameter determines which values the Spectre simulator uses to compute whether the relative error tolerance (`reltol`) requirements are satisfied.

You can set `relref` to the following options:

- The `relref=pointlocal` setting compares the relative errors in quantities at each node relative to the current value of that node.
- The `relref=alllocal` setting compares the relative errors in quantities at each node to the largest value of that node for all past time points.
- The `relref=sigglobal` or `relref=allglobal` settings compare relative errors in each of the circuit signals to the maximum of all the signals in the circuit.
- In addition, the `relref=allglobal` setting compares equation residues (the amount by which Kirchhoff's Current Law [also known as Kirchhoff's Flow Law] is not satisfied) for each node to the maximum current floating onto the node at any time in that node's past history.

Setting the Integration Method

The `method` parameter specifies the integration method. You can set the `method` parameter to adjust the speed and accuracy of the simulation. The Spectre simulator uses three different integration methods: the backward-Euler method, the trapezoidal rule, and the second-order Gear method. The `method` parameter has six possible settings that permit different combinations of these three methods to be used. The following table shows the possible settings and what integration methods are allowed with each:

	Backward-Euler	Trapezoidal Rule	Second-Order Gear
euler	•		
traponly		•	
trap	•	•	
gear2only			•
gear2	•		•
trapgear2	•	•	•

The trapezoidal rule is usually the best setting if you want high accuracy. This method can exhibit point-to-point ringing, but you can control this by tightening the error tolerances. The trapezoidal method is usually not a good choice to run with loose error tolerances because it is sensitive to errors from previous time steps. If you need to use very loose tolerances to get a quick answer, it is better to use second-order Gear.

While second-order Gear is more accurate than backward-Euler, both methods can overestimate a system's stability. This effect is less with second-order Gear. You can also reduce this effect if you request high accuracy.

Artificial numerical damping can reduce accuracy when you simulate low-loss (high-Q) resonators such as oscillators and filters. Second-order Gear shows this damping, and backward-Euler exhibits heavy damping.

Improving Transient Analysis Convergence

If the circuit you simulate can have infinitely fast transitions (for example, a circuit that contains nodes with no capacitance), the Spectre simulator might have convergence problems. To avoid these problems, set `cmin`, which is the minimum capacitance to ground at each node, to a physically reasonable nonzero value.

You also might want to adjust the time-step parameters, `step` and `maxstep`. `step` is a suggested time step you can enter. Its default value is `.001*(stop - start)`. `maxstep` is the largest time step permitted.

Controlling the Amount of Output Data

The Spectre simulator normally saves all computed data in the transient analysis. Sometimes you might not need this much data, and you might want to save only selected results. At other times, you might need to decrease the time interval between data points to get a more precise measurement of the activity of the circuit. You can control the number of output data points the Spectre simulator saves for the transient analysis in these ways:

- With strobing, which lets you select the time interval between the data points the Spectre simulator saves. The simulator forces a time step on each point it saves, so the data is computed, not interpolated.
- With skipping time points, which lets you select how many data points the Spectre simulator saves
- With data compression, which eliminates repetitive recording of signal values that are unchanged

- With the `outputstart` parameter, which lets you specify the time when the Spectre simulator starts saving data points
- With the `infotime` parameter, which lets you specify specific times to save operating-point data instead of for all time points

Changing the Time Interval between Data Points (Strobing)

Strobing changes the interval between data points. You use strobing to eliminate some unwanted high-frequency signal from the output, just as a strobe light appears to freeze rapidly rotating machinery. With strobing, you can demodulate AM signals or hide the effect of the clock in clocked waveforms. You can also dramatically improve the accuracy of external Fast Fourier Transform (FFT) routines. To perform strobing, you set the following parameters in the transient analysis:

- `strobeperiod`: Sets the time interval between the data points that the Spectre simulator saves. `strobestep` is equivalent to `strobeperiod`.
- `skipstart` (optional), which tells the Spectre simulator when to start strobing. This parameter is also used to skip data points. `strobstart` is equivalent to `skipstart`.
- `skipstop` (optional), which tells the Spectre simulator when to stop strobing. This parameter is also used to skip data points. `strobstop` is equivalent to `skipstop`.
- `strobedelay` (optional), which lets you set a delay between the `skipstart` time and the first strobe point `strobeoutput=strobeonly`
- `strobeoutput`: Specifies which time points to output during strobe. Possible values are `strobeonly`, `all`, and `none`.
- `strobefreq`: This is the reciprocal of `strobeperiod` (`strobestep`).
- `sstrobetimes=[...]`: Specifies times in ascending order when strobe output is to be performed.

Telling the Spectre Simulator How Many Data Points to Save

By telling the Spectre simulator to save only every *N*th data point, you can reduce the size of the results database generated by the Spectre simulator. You tell the Spectre simulator to save every *N*th data point with the following parameters:

- With the `skipcount` parameter, which you set to *N* to make the Spectre simulator save every *N*th data point
- The `skipstart` parameter, which tells the Spectre simulator when to start skipping parameters. This parameter is also used in strobing.

- The `skipstop` parameter, which tells the Spectre simulator when to stop skipping parameters. This parameter is also used in strobing.

Examples of Strobing and Skipping

In the following example, the Spectre simulator starts skipping data points at Time=10 seconds and continues to skip points until Time=35 seconds. During this 25-second period, the Spectre simulator saves only every third data point.

```
ExSkipSt tran skipstart=10 skipstop=35 skipcount=3
```

In this example, the Spectre simulator starts strobing at Time=5 seconds and continues until Time=20 seconds. During this 15-second period, the Spectre simulator saves data points every 10 seconds.

```
ExStrobe tran skipstart=5 skipstop=20 strobeperiod=10
```

This example is identical to the previous one except that it sets a delay of 2 seconds between the `skipstart` time and the first strobe point.

```
ExStrobe2 tran skipstart=5 skipstop=20 strobeperiod=10 strobedelay=2
```

In the following example, Spectre starts strobing at 100.01ns (`skipstart+strobedelay`) with a strobe period of 20ps. The strobing is ending at 200ns.

```
tran1 tran skipstart=100ns skipstop=200n strobeperiod=20p strobedelay=10p
```

In the following example, the user given strobe points are enforced.

```
tr1 tran stop=20n strobetimes=[3.23n 5.01n 10.17n 15.98n 16.11n 19.01n]
```

Waveform Compression

Some circuits, such as mixed analog and digital designs and circuits with switching power supplies, have substantial amounts of signal latency. If unchanged signal values for these circuits are repetitively written for each time point to a transient analysis output file, this output file can become very large. You can reduce the size of output files for such transient analyses with the Spectre simulator's waveform compression feature. With waveform compression, the Spectre simulator writes output data for a signal only when the value of that signal changes.

Using waveform compression is not always appropriate. The Spectre simulator writes fewer signal values when you turn on waveform compression, but it must write more data for every signal value it records. For circuits with small amounts of signal latency, waveform compression might actually increase the size of the output file.

You can enable waveform compression globally, for user-defined hierarchy levels, or for individual `save` statements.

You can turn on waveform compression globally by adding the parameter `compression=all | no | wilddcardonly` to the transient analysis command line in a Spectre netlist. The `all` option enables compression globally, `no` (default) disables compression, and `wilddcardonly` compresses waveforms produced by `save` statements using wildcards and settings like `save=all`, `currents=all`, `subcktprobelvl=n`. For example:

```
DoTran1 tran stop=20e-6 compression=all
```

You can add the parameter `complvl=1 | 2 | . . .` in the transient analysis statement to define the level up to which the compression should be enabled. `complvl=1` lets the signals at all hierarchical levels to be compressed, including the top level. `complvl=2` compresses all signals on hierarchical level 2 and below. You can set `complvl=2` to keep the signals from the top hierarchical level uncompressed. For example:

```
DoTran2 tran stop=20e-6 complvl=2
```

Note: The `complvl` parameter takes precedence over the `compression` parameter. Therefore, if both parameters are set in the `tran` statement, the `compression` parameter is ignored.

You can set `compression=yes | no` in the `save` statement to define whether the signals in the `save` statement should be compressed. The signals in the `save` statement are not compressed by default. Setting `compression=yes` forces the compression of the signals in the `save` statement. For example:

```
save * compression=yes
```

Note: The `compression` parameter in the `save` statement takes precedence over the `complvl` and `compression` parameters specified in the `tran` statement. For example:

```
save g s d compression=no  
tran1 tran complvl=1 compression=all save=all
```

In the above example, Spectre will compress all signals except the voltage for `g`, `s`, and `d`.

You can set `compreltol=0.001`, `compvabstol=1.0e-3V`, `compiabstol=1.0e-12A` parameters in the `tran` statement to customize the compression algorithm. For example:

```
DoTran3 tran stop=20e-6 compleltol=0.005 compvabstol=5.0e-3V compiabstol=1.0e-11A
```

You cannot apply waveform compression to operating-point parameters, including terminal currents that are calculated internally rather than with current probes. If you want waveform compression for terminal currents, you must specify that these currents be calculated with current probes. You can specify that all currents be calculated with current probes by placing `useprobes=yes` in an `options` statement.



Adding probes to circuits that are sensitive to numerical noise might affect the solution. In such cases, an accurate solution might be obtained by reducing `reltol`.

Note: When multiple `save` statements with overlapping compression scope are specified, the compression statement specified later takes higher precedence.

Telling Spectre to Save Operating-Point Data at Specific Times

In addition to saving operating-point data in a `dc` analysis, Spectre allows this data to be saved at user-specified times during a transient analysis. This data can be saved as a waveform or text information. See [Chapter 13, “Specifying Output Options,”](#) to learn how to select and save this data using the `info` analysis.

The parameters `infonames` and `infotimes` are used to define which `info` analyses need to be performed at which time point. By default, the time points and the analyses defined using these parameters are paired.

```
tr1 tran stop=10n infotimes=[2n 5n] infonames=[info1 info2]
info1 info what=oppoint where=file file=info1
info2 info what=captab where=file file=info2
```

In the above example, the operating-point analysis `info1` is performed at 2ns, and the `captab` calculation `info2` is performed at 5ns.

You can use the `infotime_pair=no` parameter to unpair the time points and analyses defined using the `infotimes` and `infonames` parameters. In that case, all analyses specified using the `infonames` parameter are performed at all times specified using the `infotimes` parameter. For example:

```
tr1 tran stop=10n infotimes=[2n 5n] infonames=[info1] infotime_pair=no
info1 info what=oppoint where=file file=oppoint_file
```

In the above example the operating point analysis `info1` is performed at 2ns and 5ns, and the operating-point information for both time points is written into the file `oppoint_file`.

You can use the `optype` parameter from the `info` analysis to output the operating point information related to currents, voltages, or the complete operating point information in a SPICE-compatible format. The `optype` parameter accepts the following values.

`current` - Output operating point information related to node voltages and currents

`voltage` - Output operating point information related to voltages only

`all` - Output complete operating point information including currents and voltage.

The node voltages are stored in a file with extension `.ic0` and the `vsource` current and device information is saved in a file with extension `.op0`.

The `optype` based SPICE-compatible operating point output can be written for selected subcircuits only (`subckt`), and for selected hierarchical levels (`depth`).

For example:

```
opinfo info what=oppoint optype=voltage subckt=pll depth=2
```

The above command will write only the node voltages for nodes inside the subckt `pll` with a hierarchical depth of 2.

You can use the `oppoint` parameter of the `info` analysis to output the operating point information for devices and stacked devices, and node voltages and currents. The `oppoint` parameter accepts the following values:

`node` - Report only node voltages and source currents

`dev` - Report the operating point information of only the devices

`subckt` - Report the operating point information of only the stacked devices

`allddev` - Report the operating point information of regular and stacked devices

`all` - Report devices, stacked devices and node voltage/source currents

The operating point information is stored based on the value specified for the `where` parameter. For example, if you specify `where=file`, by default, the operating point information is stored in a `*.oppoint` file. You can change the file name using the `file` parameter. If you do not specify the `where` parameter, the operating point information is saved in the log file.

For example:

```
opinfo info what=oppoint where=file oppoint=dev
```

The above command saves the operating point information of only the devices in a file.

Calculating Transient Noise

Transient noise provides the benefit of examining the effects of large signal noise on many types of systems. It gives you the opportunity to examine the impact of noise in the time domain on various circuit types without requiring access to the SpectreRF analyses. This

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capability is an extension to the current transient analysis, and is accompanied by enhancements to several calculator functions, allowing you to calculate multiple occurrences of measurements such as risetime and overshoot. Spectre provides both a single run and multiple run method of simulating transient noise. The single run method, which involves a single transient run over several cycles of operation, is best suited for applications where undesirable start-up behavior is present. The multiple run method, which involves a statistical sweep of several iterations over a single period, is recommended for users who are able to take advantage of distributed processing.

Set the following parameters to calculate noise during a transient analysis.

`trannoisemethod=default`

Use this option to enable the adaptive noise step control. Possible values are `default` and `adaptive`.

`noisefmax=0` (Hz)

The bandwidth of pseudorandom noise sources. A valid (nonzero) `noisefmax` turns on the noise sources during transient analysis. The maximum time step of the transient analysis is limited to $0.5/\text{noisefmax}$.

`noisescale=1`

Noise scale factor applied to all generated noise. It can be used to artificially inflate the small noise to make it visible over transient analysis numerical noise floor, but it should be small enough to maintain the nonlinear operation of the circuit.

`noiseseed`

Seed for the random number generator. Specifying the same seed allows you to reproduce a previous experiment.

`mc_auto_noiseseed=no`

Use this option to regenerate the seed at every monte carlo iteration. Possible values are `yes` and `no`.

`noisefmin` (Hz)

If specified, the power spectral density of noise sources depend on frequency in the interval from `noisefmin` to `noisefmax`. Below `noisefmin`, noise power density is constant. The default value is `noisefmax`, so that only white noise is included and noise sources are evaluated at `noisefmax` for all models. $1/\text{noisefmin}$ cannot exceed the requested time duration of transient analysis.

`noiseon=[...]`

The list of instances to be considered as noisy during transient noise analysis.

`noiseoff=[...]`

The list of instances to be considered as not noisy during transient noise analysis.

Example

```
trl tran stop=4u noiseifmax=5G noiseifmin=1Meg noiseseed=1 noisescale=10 \
param=isnoisy param_vec=[0 1 10ns 0 50ns 1]
trl tran stop=4u noiseifmax=5G noiseupdate=step noiseseed=1 noisescale=10
```

Performing Small-Signal Analyses during a Transient Analysis

You can perform an AC and/or noise analysis at specific times during a transient analysis. The Spectre circuit simulator stops the transient analysis at the specified times, saves operating point information, and performs the AC and/or noise analysis.

This type of simulation is useful when you want to run an AC analysis after getting past specific start-up behavior, or when there is more than one point along the transient run that can be thought of as steady-state.

The syntax for performing a small-signal analysis during transient analysis is:

```
Name tran stop=stop actimes=time acnames=name
```

Where:

<i>Name</i>	The name of the transient analysis
<i>stop</i>	The time at which the transient analysis is to be put on hold.
<i>actimes</i>	The time points at which the analyses specified by <i>acnames</i> are performed.
<i>acnames</i>	The names of the analyses to be performed at each time point in the <i>actimes</i> array. Allowed child analyses are: ac, noise, sp, stb, or xf.

```
mytran tran stop=5n actimes=[3n 4n] acnames=[myac noise1]
myac ac ...
noise1 (1 0) noise ...
```

In the above example, *myac* analysis will be called at 3n and *noise1* analysis will be called at 4n. You can specify *actime_pair=no* to call both *myac* and *noise1* analyses at both time points. For example:

```
mytran tran stop=5n actimes=[3n 4n] acnames=[myac noise1] actime_pair=no
myac ac ...
noise1 (1 0) noise ...
```

In the above example, both *myac* and *noise1* analyses will be called at 3n and 4n.

Performing DCMatch Analysis during a Transient Analysis

You can perform DCMatch analysis at specific times during a transient analysis. The Spectre circuit simulator stops the transient analysis at the specified time, and performs DCMatch analysis.

The syntax for performing DCMatch analysis during transient analysis is:

```
Name tran stop=stop infonames=[name] infotimes=[time]
```

Where:

<i>name</i>	The name of the DCMatch analysis.
<i>time</i>	The time at which the transient analysis is to be put on hold and dcmatch analysis needs to be performed.

Example

```
Name tran stop=10n infonames=[dcmatch1] infotimes=[1n]
```

In the above example, dcmatch1 analysis will be called at 1n.

Generating EMIR Output During Transient Analysis

You can use transient analysis in Spectre/Spectre APS to generate the binary *tranName_emir_vavo.db* database file, which can be directly used by VAVO/VAEO for electro-migration (EM) and IR-drop analysis. This significantly improves the efficiency and capability of Spectre in the VAVO/VAEO flow.

The syntax for generating EMIR output during transient analysis is as follows:

```
Name tran [emirformat=vavo|none] [emirstart=time] [emirstop=time]  
[emirfile=dbfileName]
```

Where:

<i>Name</i>	The name of the transient analysis.
<i>emirformat</i>	Turns on the <i>vavo.db</i> file output capability. Possible values are <i>vavo</i> and <i>none</i> . Default is <i>none</i> .
<i>emirstart/emirstop</i>	Specifies the time window start and stop times. The default of start and stop times are same as the start and stop times for transient analysis, respectively.

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`emirfile` Specifies the name of the EM/IR output database file. Default is `tranName_emir_vavo.db`. This file is saved in the raw directory.

Example

```
tran1 tran stop=15s errpreset=moderate emirformat=vavo emirfile="testDB"
emirstart=1s emirstop=15s
```

Calculates the required information for EM and IR analysis and saves it in the `tran1_emir_vavo.db` file.

Performing Event-Triggered Analysis During Transient Analysis

At times, you may want to trigger an action in transient analysis whenever there is a change in the circuit behavior. For example, when the voltage at node `n1` (`v(n1)`) crosses `vdd/2`, you may want to enable asserts. The event-triggered analysis enables you to capture events in the circuit and perform actions based on those events.

The general form of an event expression is `"@(basic_event, N) + delay".`

Here, `N` is the selector of the event. A positive value for `N` means the `N`th occurrence of the `basic_event` needs to be selected. A negative value means the `N`th occurrence and the occurrence just before the `N`th occurrence of the `basic_event` needs to be selected. A value 0 means all occurrences of the `basic_event` need to be selected. If `N` is not specified, it means the first occurrence of the `basic_event` needs to be selected.

`delay` specifies the delay time after the selected event occurrences. You should specify a positive value for `delay`.

Both `N` and `delay` are optional. However, if specified, they must be a constant SFE expression. For example, the following event expression is valid:

```
"@(assert1, myparam0 + 1) + myparam1+myparam2"
```

The following event expressions are invalid:

```
"@(assert1) + V(out)"
```

```
"@(assert1) +@(event)"
```

The event name should be enclosed within parentheses. In addition, when specifying an event expression in the netlist, you must enclose the expression within double quotes or parentheses. For example, `"@(event)"` or `(@(event))`.

You can capture the following events during transient analysis:

- An explicit time (number/parameter)
`@(time),@(param_name)`
- Time when the design variable changes from zero to non-zero
`@(inst_name:variable_name)`
- Time when an assert is triggered
`@(assert_name)`
- Time when a measurement completes
`@(meas_name)`
- Delay event
`@(event) +10n`
- Event selection
`@(event,2)`

You may perform the following actions when an event is triggered:

- Run the analysis specified at `actimes/infotimes`
- Change a dynamic parameter
- Enable/disable asserts
- Enable/disable diagnostics

Example1

```
simulator lang=spice
.measure vout_avg avg v(out) from=1u to=5u
simulator lang=spectre
tran tran stop=10u param=reltol param_vec=[0 1e-4 "@(vout_avg)" 1e-2]
```

In the above example, the value of `reltol` will change from `1e-4` to `1e-2` after the measurement `vout_avg` is finished.

Example2

```
assert1 assert expr="v(out)>vdd/2"
tran tran stop=10u infotimes=["@(assert1)"] infoname=op_info
op_info info what=oppoint where=file
```

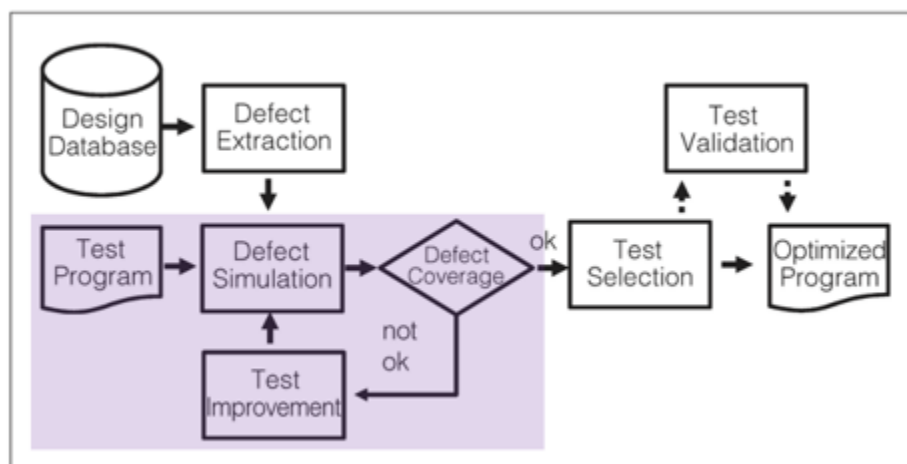
In the above example, the operating information will be output to a file when `assert1` is triggered for the first time.

Fault Analysis

Spectre fault analysis provides a transistor-level simulation capability that can be enabled in an analog test methodology to improve test coverage by identifying critical test patterns. Spectre transient fault analysis is very fast in handling a large numbers of faults. Spectre direct fault analysis provides high accuracy results when full fault analysis precision is required.

Analog Test Overview

A typical analog test methodology consists of defect creation, fault analysis, and test optimization for better test vector, or better defect coverage.



Defect Creation

Design defects are the input to fault analysis. Realistic defects can be extracted from the schematic design according to certain rules, or from the layout, based on the design geometry.

Fault Analysis

The defects are modeled as faults and provided to the Spectre circuit simulator to perform fault analysis. Without any simulation performance optimization, a complete fault analysis can take significant amount of time when the number of defects is large.

Application of Fault Analysis

Spectre analog fault analysis provides the capability to estimate fault coverage by generating a detection matrix. In addition, it can be used as part of functional safety analysis.

The defect detection matrix can be obtained by comparing the faulty simulation results with nominal (faultless) data. You can further optimize the test to improve the defect coverage based on the defect detection matrix.

In functional safety applications, fault detection is tracked for both functional and diagnostic modules, but reported separately. Functional safety report can be generated based on fault analysis results.

Defect Detection Matrix

The following figure shows an example of detection matrix created by processing the fault simulation:

Detection Matrix:

		0.0025/d	0.003/d	0.0035/d	0.004/d	0.0045/d	0.005/d	0.0055/d	0.006/d	0.0065/d	Total
bridge_1	D	D	G	G	G	G	G	G	G	D	D
bridge_2	G	G	G	G	G	G	G	G	G	G	G
bridge_3	D	D	D	G	G	G	G	G	G	D	D
open_1	G	G	G	G	D	D	D	D	D	G	D
open_2	D	D	D	G	G	G	G	G	G	D	D
open_3	D	D	G	G	G	G	G	G	G	D	D
Coverage		66.67%	66.67%	33.33%	0.00%	16.67%	16.67%	16.67%	16.67%	66.67%	83.33%

Test engineers can use the detection matrix to identify the optimum test vector and fault time points, or to minimize the subset of production tests to meet the required percentage of defect coverage. For example, the fault points at 3.0ms, and 4.5ms, capture most of the defects.

Functional Safety Report

If the faults are detected by asserts by specifying the boundaries, a functional safety report can be generated based on the assert violation output, as shown below.

```
Failure Mode ID:      000
Failure Mode:         SPF

Diagnostic coverage    :      50.00%
Fault tolerance        :      83.33%
Coverage reported by checker :      66.67%
Faults that are safe   :      66.67%

Safe_undetected        :      16.67%
Safe_detected          :      50.00%
Dangerous_detected     :      16.67%
Dangerous_undetected   :      16.67%
```

Fault detection is enabled for both functional and diagnostic modules and is classified according to the ISO 26262 standard that classifies safe/dangerous and detected/undetected defects.

Fault Analysis Technology

You can perform fault analysis in Spectre by using one of the following approaches:

- **Direct Fault analysis.** In the direct fault analysis flow, faults are injected at the beginning of each analysis type, such as dc, ac, transient, and so on. This mode provides the most accurate results. However, when the number of faults is large, the simulation takes much longer to complete.
- **Transient Fault Analysis:** Transient fault analysis addresses the challenge of long simulation time. In this simulation flow, a circuit with fault list is simulated together with the fault times specified on the time axis. Spectre starts regular transient analysis till the time it reaches the fault time point. At each fault time, the following actions are performed:
 - ❑ A fault-free transient state is saved
 - ❑ A fault is injected into the circuit
 - ❑ With fault-free state used as the initial condition, transient fault simulation is continued with regular time step control and accuracy settings
 - ❑ The result is saved and the database is cleaned when all fault solutions are found

- ❑ Fault-free transient simulation is restored and continues till the next test time point

Fault List

In fault analysis, it is mandatory to specify a fault list that defines the type and location of faults. The fault list can be extracted from the schematic design, the layout design, or from customized fault creation tools. Spectre supports bridge (short), open, and custom faults.

The following is the syntax to specify faults in a fault block:

```
name faults <parameter=value> [weight_factor=<expression>] \
[weight_expr=<expression>] [sub=subckt_model |inst=instance] {
    bridge {
        <name> ( <node1> <node2> ) r = <expression> [dev=<instance>] \
            [weight=value] ]
    }
    short {
        <name> ( <node1> <node2> ) r = <expression> [dev=<instance>] [weight=value]
    }
    open {
        <name> ( <node> ) r = <expression> [ c = <expression> ] [weight=value]
        { instance1[:terminal] [instance2[:terminal2]]... }
    }
    custom {
        <name_ins> (<node1> <node2...>) <subckt_model> [param=<expr>]
        <name_replace> (<node1> <node2...>) <subckt_model> [param=<expr>]
            original_inst=<name_orig>
        <name_open> (<node>) fault_subckt=<subckt_model> [param=<expr>]
            {instance1[:terminal1][instance2[:terminal2]]...}
    }
    parametric {
        <name> faultalter param=<name> value=<value> [dev=<name> | mod=<name> |
            sub=<name>] [weight=<value>] [sample=<value>]
    }
}
```

The `faults` block is used to specify the fault groups to be simulated in fault analysis. Each block may contain several sub-blocks with keywords according to the type of fault – bridge (or equivalently short), open, custom, and parametric.

The `bridge` block (or `short` block) specifies the resistance value between any two nodes of a circuit. The node names may be specified hierarchically.

Within a `faults` block, the `bridge`, `short`, `open`, `custom`, and `parametric` blocks are optional. If none are specified, a warning message is generated and the `faults` block is ignored. If more than one `bridge`, `short`, `open`, `custom`, or `parametric` blocks are specified within a `faults` block, they are concatenated and treated as one block. Every fault name in a `faults` block must be unique. Duplicate names result in an error. You can use global parameters in `expression`.

More than one `faults` block may be specified in the netlist and each `faults` block must have a unique name and a set of parameters associated with it.

The fault block parameters `sub=subckt_model` and `inst=instance` enable you to use the local node and instance names in the fault statements within the subcircuit or the subcircuit instance scope. This is useful when the original fault list is created and verified based on one design which is defined later as a subcircuit and instantiated in another bigger design.

For example, in VCO design, one of the bridges is created as

```
bridge_1 (net10 net20) r=10 dev=M2 //mosn d g
```

Later, if VCO is included in the PLL design as a subcircuit `VCO` and instantiated as `I0`, the fault list has to be modified manually as

```
bridge_1 (top.I0.net10 top.I0.net20) r=10 dev=top.I0.M2 // mosn d g
```

If `sub=VCO` or `inst=top.I0` is specified in the fault block, then no modification is needed. Spectre takes care of the node tracing with subcircuit or instance name.

By default, all faults in the list have equal weights while calculating the fault coverage rate. You can use the `weight_expr` and `weight_factor` parameters to redefine fault weighting using the weight expression for different faults and fault blocks.

The `param` and `value` parameters can be specified with vectors or scalar value.

The optional parameter `dev` in `bridge|short` statement refers to the specific instance to which the fault is related.

Bridges

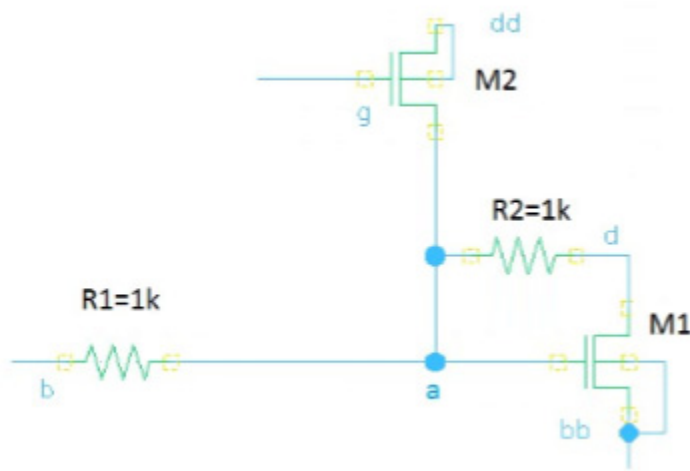
Bridge faults represent catastrophic failures due to two nets being shorted together, where the nets are shorted by a low-value resistor. The fault statement in the `bridge (short)` block specifies two nodes to be shorted in the netlist and a resistance value specified using parameter `r`. The node names may be specified hierarchically.

The following example shows the sequential insertion and analysis of bridge.

```
R1 (a b) resistor r=1k
```

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```
R2 (a d) resistor r=1k
M1 (d a bb bb) nmos
M2 (a g dd dd) nmos
```



The `bridge_1` instance in the following example performs insertion of a 10 Ohm resistor between terminals `g` and `s` of `M2`.

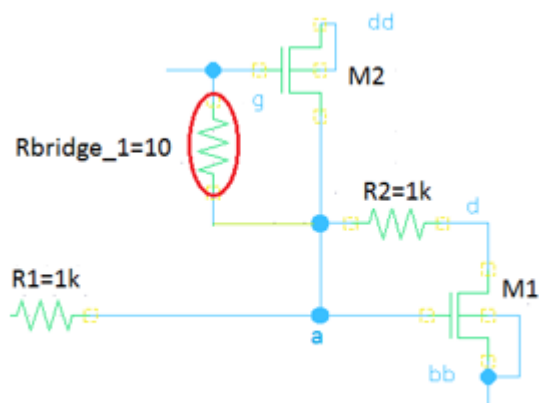
```
parameters resBridge=10
Bridges faults {
  bridge {
    bridge_1 (g a) r=resBridge dev=M2 //mosn g s
  }
}
```

The commented notations in the fault statement are included as additional information about a faulty device. In the above example, `mosn` is the model name (it can be a primitive, or a subcircuit name) and `g` and `s` are the names of the shorted pins.

The net connectivity after the insertion of `bridge_1` can be described by the following netlist:

```
R1 (a b) resistor r=1k
R2 (a d) resistor r=1k
M1 (d a bb bb) nmos
M2 (a g dd dd) nmos
```

```
Rbridge_1 (g a) resistor r=10
```



When fault simulation starts, Spectre adjusts the connectivity accordingly.

Opens

Open faults represent catastrophic failures due to a break in a net, where `open` is represented by a high-value resistor. The open can also be represented as an impedance or a shunt combination of a resistor and capacitor. The `open` block specifies the nodes that are split into two.

The `node` in the statement is the name of the net that is broken by the open fault. The parameter `r` specifies the resistance between the new fault node and the original node. An optional parameter `c` specifies the capacitance between the new fault node and the original node.

The last block describes the topology change providing the list of the instances or terminals to be connected to the new node. All terminals or instances, not specified in the list, remain connected to the original node. If no instance list is specified, a warning message is generated and the fault is ignored.

The terminals are specified either by name, or numerically, starting from 1. That is, terminal number 1 is the first terminal of the instance. If the specified terminal number of an instance in the instance list is not connected to the original node, an error message is generated. If no terminal list is specified for an instance, all terminals of that instance, connected to the original node, are connected to the new node. The node and instance names can be specified hierarchically. Device and subcircuit instances can be used for topology change description.

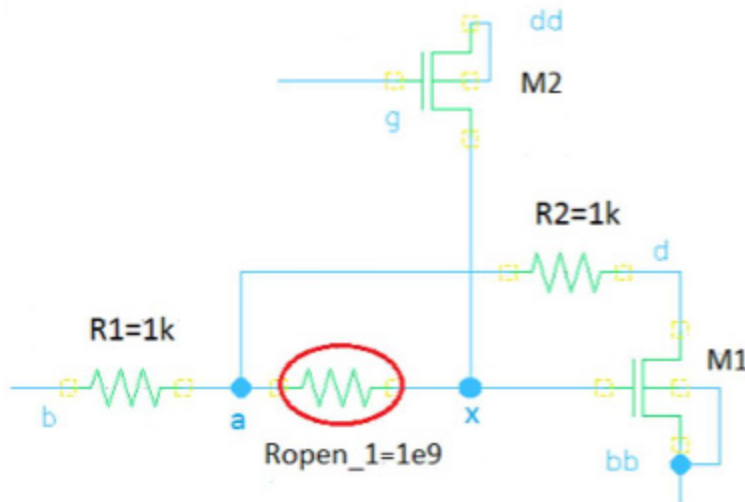
The example netlist below illustrates the open fault injection. The open fault instance `open_1` requests splitting the node `a` into two nodes, where the original node `a` stays connected to `R1`

and R2, and the new node *x* is connected to M1 : *g* and M2 : *d*. A 1 GOhm resistor is inserted between the original and new nodes.

```
parameters resOpen=1e9
Opens faults {
  open {
    open_1 (a) r=resOpen { M2:d M1:g } //mosn g
  }
}
```

The connectivity after the insertion of `open_1` can be described by the following netlist:

```
R1 (x b) resistor r=1k
R2 (x d) resistor r=1k
M1 (d x bb bb) nmos
M2 (x g dd dd) nmos
Ropen_1 (a x) resistor r=1e9
```



You can use the definition of the open fault to probe the voltage or current at the new node (*x*). In the example below, the terminals specified in the open fault will be connected to the new node.

```
open_1 (a) r=resOpen { M2:d M1:g }
```

Use the `save` statement to probe the voltage at the new node, as shown below.

```
save a M2.d
```

or

```
save a M1.g
```

The current through the open fault should be very small. To verify the current value, you can use the `save` statement, as follows:

```
save M2:d
```

or

```
save M1:g
```

When the open instance statement contains several terminals, any terminal can be used in the `save` statement.

Probing of current and voltage at the new node is available in direct fault analysis and detailed raw files are saved when `faultsave=all` is used. These signals are not saved in `tran_faults.raw` and `table` files.

Note: The goal of probing is to provide a method to debug or investigate one or few open faults, and not for the definition of `M2.d` as a fault detection signal.

Custom Faults

Spectre supports three types of custom faults: custom insertion, custom replacement and custom open. The custom fault model is specified as a subcircuit and defined outside the fault block. The custom subcircuit instances are specified in the `custom` fault block. Spectre injects the custom instances into the original netlist when fault simulation is requested and applies the connectivity accordingly.

For insertion faults, the number of terminals in the `custom` fault statement must match the number of terminals of the custom subcircuit.

For replacement faults, the number of terminals in the `custom` fault statement must match the number of terminals of the custom subcircuit and the device or the subcircuit instance to be replaced.

The custom open fault statement and the custom subcircuit must have two terminals always. A warning message is generated when an inconsistent terminal number is detected.

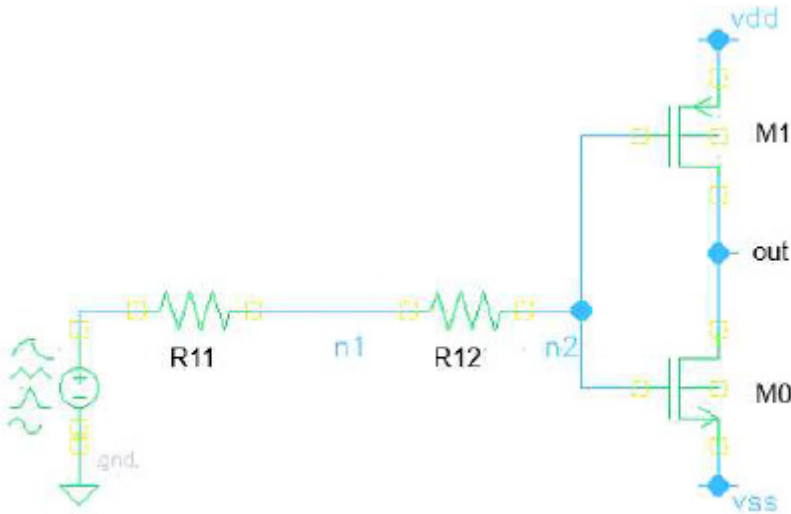
You can use a Verilog-A model as a faulty subcircuit by including it as a part of the Spectre subcircuit definition.

The custom fault injection and simulation is compatible with all available direct fault analysis (DFA) and transient fault analysis (TFA) parameters, similar to bridge and open faults.

The following example netlists and schematics are used to illustrate the sequential insertion and analysis of different types of custom faults:

Custom Insertion Fault

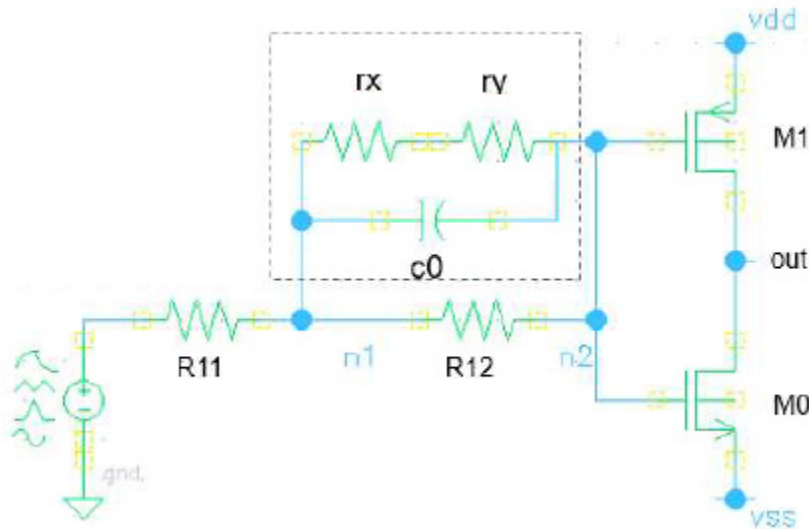
For custom insertion fault, the customized subcircuit instance is connected to the nodes specified in the `fault` statement to perform fault simulation. The example below shows that fault instance `I0` is inserted into the nominal circuit by not connecting `n1` and `n2`.



```
InsertBlock faults paramsubckt=1n {
    custom {
        I0 (n1 n2) insFaultRC
    }
}

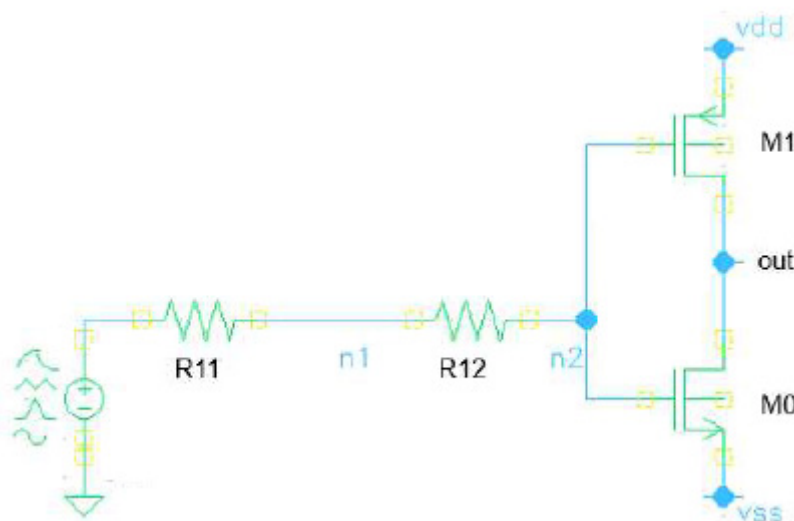
subckt insFaultRC n11 n22
    rx (n11 net0) resistor r=100
    ry (net0 n22) resistor r=200
    cl (n11 n22) capacitor c=100f
ends insFaultRC
```


The circuit connectivity with the custom insertion fault injected is shown in the following figure:



Custom Replacement Fault

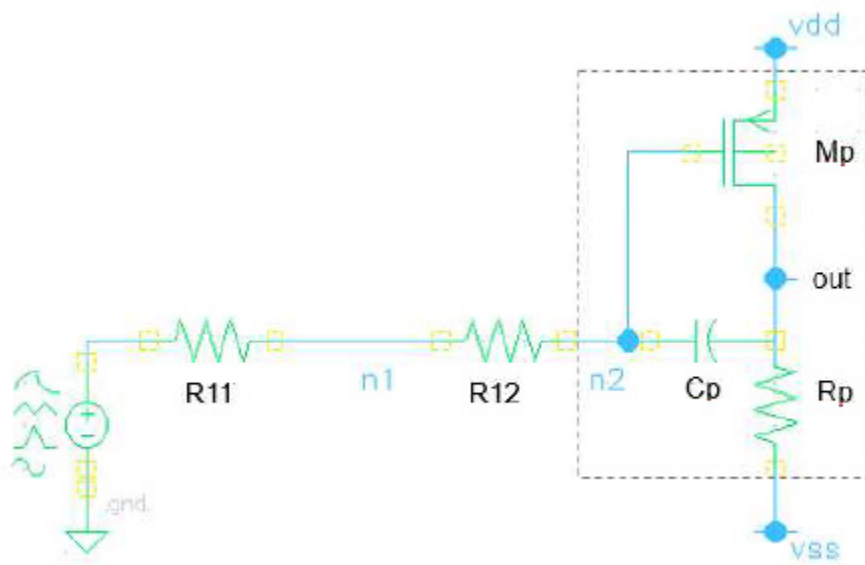
For the custom replacement fault, the device or subcircuit instance specified as `original_inst` is replaced by the custom subcircuit. The order and number of terminals should match.



```
ReplaceBlock faults paramsubckt=1p {
  custom {
    I0 (n2 out vdd vss) replFaultSubckt original_inst=I1.INV0
```

```
    }  
}  
subckt replFaultSubckt in out vdd vss  
    Mp (vdd in out out) pch w=2u l=0.1u  
    Cp (in out) capacitor c=1p  
    Rp (out vss) resistor r=1k  
ends replFaultSubckt
```

The above example shows how the original instance defined with `original_inst=I1.INV0` in the above figure is replaced by the fault subcircuit of `replFaultSubckt` and schematic changes, as shown below.

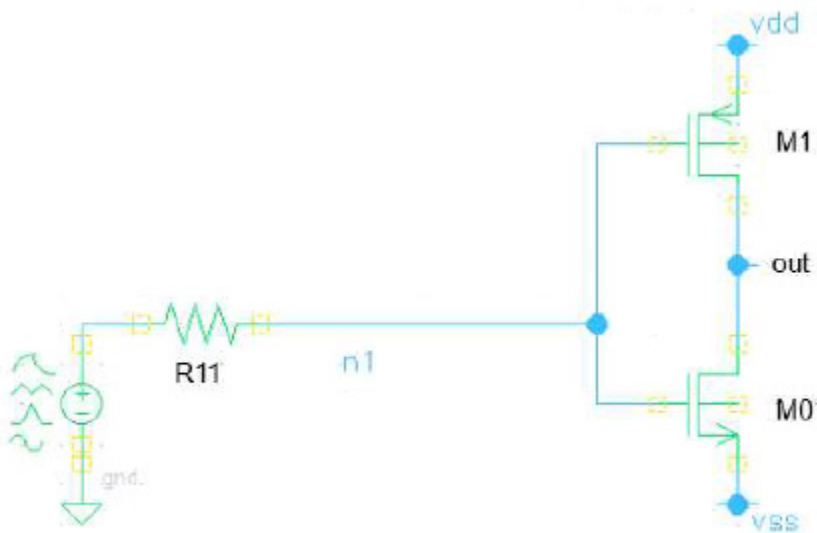


Custom Open Fault

For custom open fault, the node specified in the `open` statement is split into two nodes and the custom subcircuit fault is inserted. The valid terminal number for custom open subcircuit is 2.

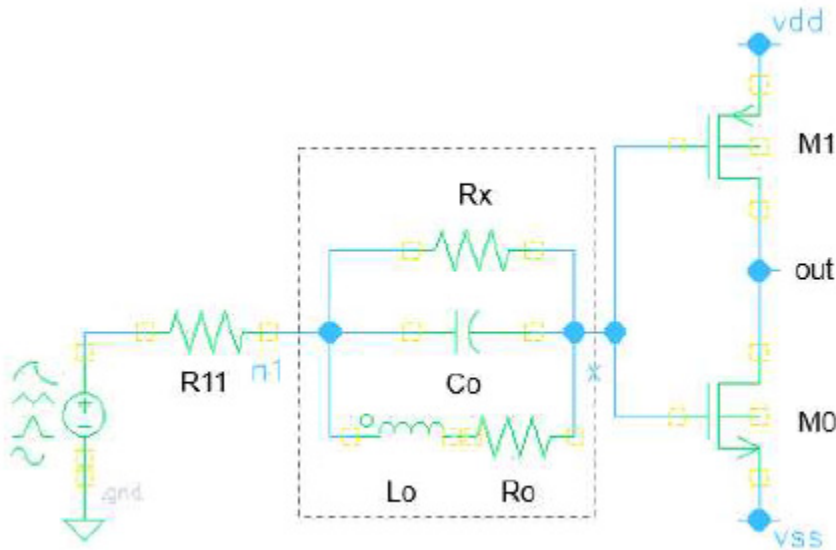
The terminal connectivity is handled similarly to the regular open faults. The first terminal of custom subcircuit is connected to the original node while the second terminal is connected to the new node.

In the following example, the two terminal instances get inserted between the original node N1 and the new node X.



```
OpenBlock faults paramsubckt=1n {
  custom {
    I0 (n1) opnFaultSubckt {M1:g M0:g}
  }
}
subckt opnFaultSubckt in out
  Rx (in out) resistor r=1k
  Co (in out) capacitor c=1p
  Lo (in net) inductor l=10n
  Ro (net out) resistor r=100
```

```
ends opnFaultSubckt
```



Extended Custom Open Model for MOS Gate Open

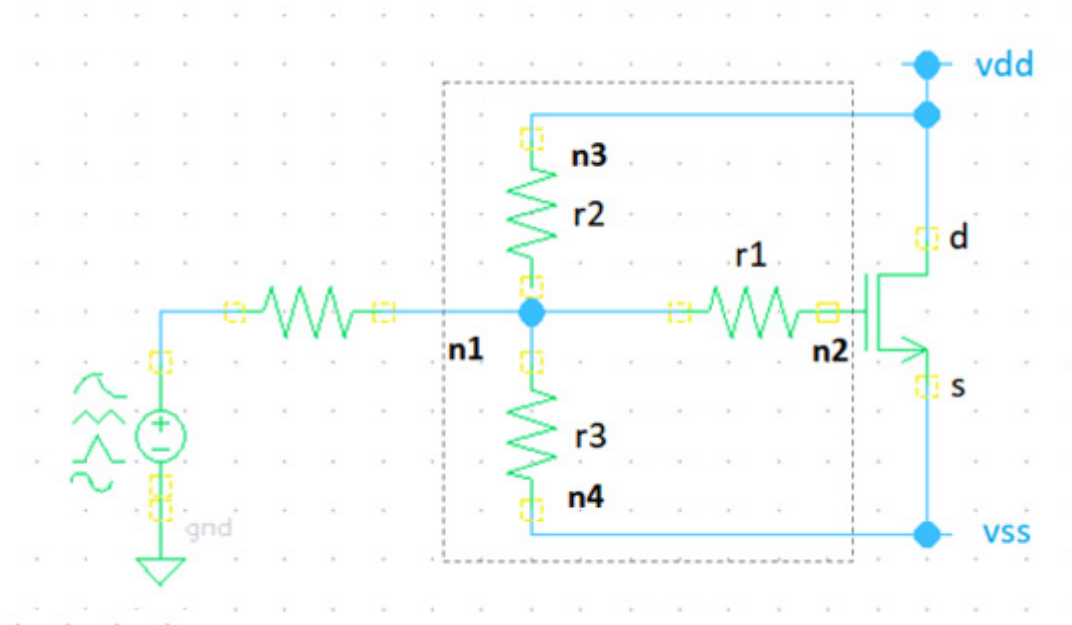
Resistive Divider

The subcircuit based on resistive divider can be considered as one of custom gate open models for a MOS device.

The custom gate open subcircuit can be defined as below.

```
//n1 existing gate, n2-g n3-d n4-s
subckt Rdiv4 n1 n2 n3 n4
parameters amplf=0.9
r1 (n1 n2) resistor r=1T //gu g
r2 (n1 n3) resistor r=1T*(1-amplf) //gu d
r3 (n1 n4) resistor r=1T*amplf //gu s
ends Rdiv4
```

```
customgen options faultcustompreserve=[Rdiv4]
```



Schematic Circuit with Custom RDIV Open Injected at Gate

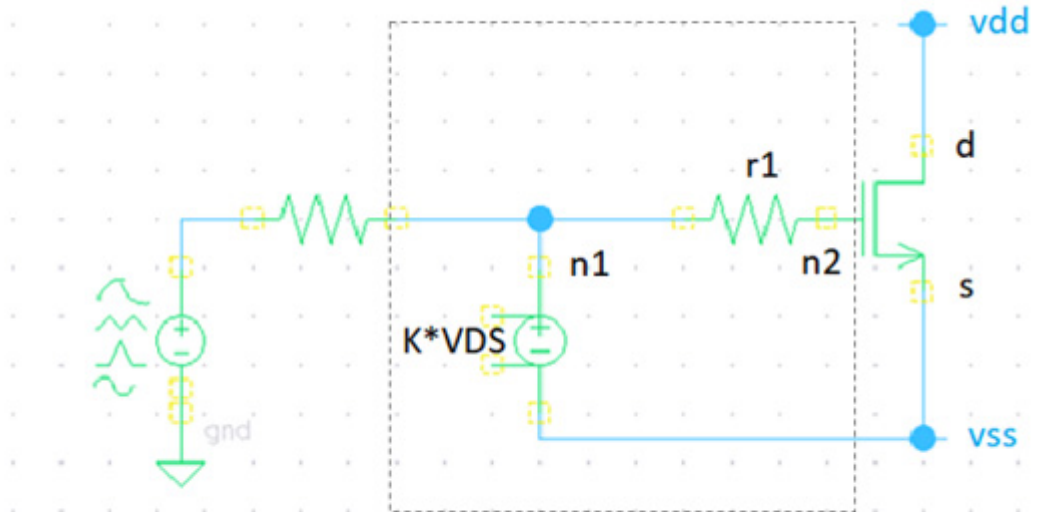
When generating custom open gate of resistive divider with info analysis, the order of terminal names specified in `faultterminal=[..]` for a transistor must follow the connectivity of custom subcircuit, i.g. gate (n2), drain (n3) and source (n4). Node n1 defined in custom subcircuit is reserved for the existing gate to be opened while n2 is the new node created at gate.

```
opnG1 info what=customopen faultdev=bsim4 faultterminal=[g d s] faultcustom=RDIV
opnG2 info what=customopen faultdev=[nch pch] faultterminal=[2 1 3]
faultcustom=RDIV
```

Voltage Controlled Voltage Source Based Model

The subcircuit based on voltage controlled voltage source also can be used to simulate the open gate of a MOS device. A sample of subcircuit definition is shown below.

```
//n1-existing gate, n2-g pos-d neg-s
subckt XOPN n1 n2 pos neg
  VS1 ( n1 neg pos neg ) vcvs gain=0.1
  R1 ( n1 n2 ) resistor r=1T
ends XOPN
customgen options faultcustompreserve=[XOPN]
```



Schematic Circuit with Custom VCVS Open Injected at Gate

To generate the custom open gate fault list based on the resistive divider model in info analysis, the order of terminal names specified in `faultterminal=[...]` for a transistor must follow the connectivity of custom subcircuit, i.g. gate (n2), drain (pos) and source (neg). Node n1 defined in custom subcircuit is reserved for the existing gate to be opened, while n2 is the new node created at gate.

```
opnG1 info what=customopen faultdev=bsim4 faultterminal=[g d s] faultcustom=XOPN
opnG2 info what=customopen faultdev=[nch pch] faultterminal=[2 1 3]
faultcustom=XOPN
```

Custom Faults with Multiple Bridges

There is a way to support multiple bridges with custom subcircuit approach. First, define a couple of bridges and connect to different ports in the subcircuit. Next, create faults by instantiating the subcircuit manually.

```
subckt Two_Bridges (n11 n22 n33 n44)
    r1 (n11 n22) resistor r=10
    r2 (n33 n44) resistor r=10
ends Two_Bridges

multiBridges faults {
    custom {
        mB1 ( n0 n1 out vdd) Two_Bridges
        mB2 ( n1 n2 out vdd) Two_Bridges
    }
}
```

With the first fault mB1, the bridge r1 is shorting R11 while the r2 is shorting the drain and source of PM0 simultaneously and the second fault mB2, the r1 is shorting R12 while the r2 is shorting the drain and source of PM0 simultaneously.

Parametric Faults

Parametric (or soft) faults are used to simulate the variations in the principal parameters of circuit elements. They do not change the topology of the circuit. A parametric fault can be a process parameter, or the first-order electrical characteristic of a circuit element.

The `parametric` block specifies the `faultalter` statements for multiple parameters to be changed. The circuit temperature, a device instance parameter, a device model parameter, a netlist parameter or a particular subcircuit instance can be used in the `faultalter` statement.

```
paramFaults faults {
  parametric {
    paramFault_1 faultalter dev=vd param=dc value=-5
    paramFault_2 faultalter dev=vd param=dc value=0
    paramFault_3 faultalter dev=vd param=dc value=5
  }
}
```

In the example above, three `dc` values are specified with the `faultalter` statement.

You can also change the sub-circuit instance parameter, model parameter and global parameter.

```
softFaults faults {
  parametric {
    subFault_1 faultalter sub=INV param=w value=700n
    modFault_2 faultalter mod=NMOS param=vth0 value=0.65
    gloFault_3 faultalter param=temp value=125
  }
}
```

Creating a Fault List

To perform fault analysis, a fault list is a critical input to model the defect of an analog test. The Spectre `info` analysis generates the fault list, based on primitives, models, or subcircuits of a given design. Three types of the resistive fault are supported with `info`: bridges, opens, and custom faults.

Syntax for Fault Creation

```
nameList info
    what=bridges|opens|customreplace|custominsert|customopen|faultparam
    [where=file] [file=filename.scs] [faultblock=nameBlock] [faultdev=[...]]
    [faultcustom=faultsubckt] [faultres=resValue] [faultcap=capValue]
    [faultterminals=[...]] [faultrule=2427] [faultcollapse=yes]
    [weight_expr=expression] [weight_factor=1] [faultlocal=no]
    [faultduplicate=no] [faultparam=name] [faultvalues=[...]]
    [faultpercentage=[...]] [faultfile=filename] [faultstart=val1]
    [faultstop=val2] [faultstep=val3] [inst=[...]] [subckt=[...]] [xinst=[...]]
    [xsubckt=[...]]
```

Here:

<code>faultblock</code>	Specifies the names of the fault blocks to be generated. Default is the name of the <code>info</code> analysis.
<code>faultdev=[dev1 dev2...]</code>	Specifies the fault devices by primitive name, subcircuit name, or model name. Default value is <code>all</code> .
<code>faultcustom=[...]</code>	Specifies the custom fault subcircuit by <code>subckt</code> model name from the netlist.
<code>faultres</code>	Specifies the resistance value for bridges or opens. The default value is 100 Ohms for bridges and 1 GOhms for opens.
<code>faultcap</code>	Specifies the capacitance value for open faults. The default value is 0 F.
<code>faultterminals</code>	Specifies the terminals of fault devices for open or short handling. The default value is all terminals.
<code>faultstuckat</code>	Supply node names to generate stuck-at fault list when 'what=bridges'.
<code>subckt</code>	Faults are generated for all instances of the specified subcircuits.
<code>inst</code>	Faults are generated for the specified subcircuit instances.
<code>xsubckt</code>	All instances of the specified subcircuits are excluded from fault generation.
<code>xinst</code>	All specified subcircuit instances are excluded from fault generation.

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<code>faultlevel</code>	Defines the hierarchical level of the design to be considered during the fault list generation. By default, Spectre generates faults in subcircuits at all levels of the design.
<code>faultmaxcount</code>	Upper bound for number of faults to be generated before collapsing.
<code>faultrule</code>	Comply with IEEE 2427 requirements for fault list generation. Possible values are <code>none</code> and <code>2427</code> . Default is <code>none</code> .
<code>faultcollapse</code>	If set to <code>yes</code> , only one fault is included in the fault list for each set of equivalent faults having the same topology. Possible values are <code>no</code> and <code>yes</code> .
<code>weight_expr</code>	Expression to define the fault weighting function.
<code>weight_factor</code>	Value to define weighting factor for given block in the fault list. Default value is 1.
<code>faultlocal</code>	If set to <code>yes</code> , when <code>inst</code> or <code>subckt</code> is specified, the local node names are used during fault generation. Possible values are <code>yes</code> and <code>no</code> . Spectre does not support local annotation in the fault list for primitive devices. For example, when <code>faultlocal=yes</code> and <code>inst=[M1]</code> are specified in <code>info</code> analysis, where M1 is an <code>bsim4</code> instance, Spectre prints a warning and ignores <code>faultlocal=yes</code> .
<code>faultduplicate</code>	By default, duplicate faults are included in all fault lists when multiple <code>info</code> analyses are specified for fault generation. This parameter lets you choose whether or not to include duplicate faults. Possible values are: ■ <code>yes</code>: The tool performs fault simulation for all fault from the list. This is the default value. ■ <code>no</code>: Identical and equivalent faults are excluded from simulation.
<code>faultpercentage</code>	Percentage deviation in value for the <code>faultparam</code> that needs to be altered
<code>faultparam</code>	Generate parametric faults for device, model or global parameter to be altered.

<code>faultvalues=[val1 val2 ...]</code>	The set of values for <code>faultparam</code> to be altered.
<code>faultfile</code>	File name which contains the fault values.
<code>faultstart, faultstop, faultstep</code>	The sweeping values for <code>faultparam</code> to be altered.

The following parameters are specified with the `what` argument of the `info` statement:

<code>customreplace</code>	Generates custom replacement faults to replace the devices listed in <code>faultdev</code> with subcircuit specified in <code>faultcustom</code> .
<code>custominsert</code>	Generates custom insertion faults by connecting the subcircuit specified in <code>faultcustom</code> to the terminals <code>faultterminals</code> of devices listed in <code>faultdev</code> .
<code>customopen</code>	Generates custom open faults of subcircuit specified in <code>faultcustom</code> that needs to be injected at each specified terminal of <code>faultdev</code> .

Scoping Options

<code>subckt=[sub1 sub2]</code>	Faults are generated for all the instances of the specified subcircuits.
<code>inst=[inst1 inst2]</code>	Faults are generated for the instances within the specified subcircuits.
<code>xsubckt=[sub1 sub2]</code>	Fault generation is skipped for all instances of the specified subcircuits.
<code>xinst=[inst1 inst2]</code>	Fault generation is skipped for the instances within the specified subcircuits.

Fault List Generation for Spectre X

When generating a fault list for Spectre X simulations, it is recommended to set the `faultmerge` Spectre option to `yes`, which is its default value.

When running simulations with this fault list, set the `+postlpreset` command-line option to `off` because if the circuit is eligible for fault reduction and `+postlpreset=off` is not set, some faults from the list may get ignored during simulation.

Fault Collapsing and Weighting Function

In analog fault simulation, *fault collapsing* implies that any number of defects that result in the same circuit topology can be collapsed into a single defect for simulation purpose. For example, two or more faults are called equivalent when they short the same nets related to different circuit instances. In Spectre, fault collapsing is the process of detection of equivalent faults and taking them into consideration while calculating the detection coverage.

By default, Spectre applies `m` factor as weight values during the fault list generation. In Spectre APS, in addition to the `m` factor, the topology optimization for parallel devices is taken into account as a factor to weight values during fault generation. Such `m` factor application to fault weighting is set by default in both Spectre and Spectre APS unless `faultcollapse=no` specified in `info` analysis.

The following table shows the weighting calculation with different options and fault types:

	bridges	opens
<code>info faultcollapse=yes</code> (default)	equivalent faults get collapsed, weight= weight_expr * m factor \ [*parallel devices number with +aps]	equivalent faults get collapsed, weight= weight_expr * m factor \ [*parallel devices number with +aps]
<code>info faultcollapse=no</code>	no collapsing; weight is equal to weight_expr only device m factor is not included.	no collapsing; weight is equal to weight_expr only device m factor is not included.
<code>info faultcollapse=yes</code> <code>faultlocal=yes</code>	equivalent faults gets collapsed, weight= weight_expr * m factor \ [*parallel devices number with +aps] node annotation is local to inst/sub in the faults statement.	weight= weight_expr * m factor \ [*parallel devices number with +aps] no collapsing of local node annotation <code>faultcollapse=yes</code> is recommended in TFA/DFA statement.
<code>info faultcollapse=no</code> <code>faultlocal=yes</code>	no collapsing; weight is equal to weight_expr only device m factor is not included. node annotation is local to inst/sub in the faults statement.	no collapsing; weight is equal to weight_expr only device m factor is not included. node annotation is local to inst/sub in the faults statement.

Spectre provides the possibility of fault weighting instead of using the equal weight. The expression including the circuit or instance parameters can be used as the weighting function. For example, the area of a MOS device can be considered as a weight for the bridge or open faults related to those devices.

The weighting function is specified in the `faults` statement as an expression using the keyword `weight_expr`, which may include parameters belonging to the `dev` instance from the `bridge` statement, or instance from curly brackets in the `open` fault statement. The

supported weighting function expression is the same as the expression supported by the `assert` statement. For example, device parameters and its operating points can be used with arithmetic operators. The weighting function expression is evaluated for every fault in a given fault block only once per simulation during the fault activation process.

Note: Do not use `m` factor in `weight_expr` since it is applied by default.

With `faultcollapse=no`, Spectre generates a fault list without grading, that is with weight values equal 1. In such cases, `m` factor is excluded from consideration. If you need to estimate the weighting expression values without collapsing factors (including `m` factor), you can specify `faultcollapse=no` in the `info analysis` statement.

Note that the weighting expression is supported for bridges and opens only, not for custom, or parametric faults. Nevertheless, constant `weight_expr` or `weight_factor` is still applicable.

Bridge Faults

The following two bridges are an example of equivalent faults that can be collapsed during simulation:

```
bridge_1 (vp10 I12.Y) r=10 dev=I12.I0.MN1 //g45n1svt g s
bridge_2 (vp10 I12.Y) r=10 dev=I12.I0.MP1 //g45p1svt g s
```

During fault generation, if you specify the fault collapsing option `faultcollapse=yes` in `info analysis`, the above fault list will be represented as one fault statement with the weight value as 2.

```
bridge_1 (vp10 I12.Y) r=10 dev=[I12.I0.MN1 I12.I0.MP1] weight=2
```

In the above example, we considered that original faults, `bridge_1` and `bridge_2`, have `weight=1`, which is default value. All faults have default weight of 1 if the weighting expression is not provided.

If the given weighting expression cannot be evaluated for some faults in the fault list, those faults will have the weight equals 0.

During fault collapsing, the final weight is calculated as the sum of weights of all equivalent faults.

If the original fault list is generated with `faultcollapse=no`, fault collapsing can be applied before performing simulation using `faultcollapse=yes` in the transient analysis.

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The following figure shows the fault list generated with `info` analysis with the given weighting expression.

```
block1 faults weight_factor=0.9 weight_expr=w*1 {
  bridge {
    block1_bridge_1 ( 0 out ) r=200 dev=I0.MN01 weight=3.025e-10 // NMOS1 s d
    block1_bridge_2 ( 0 pd ) r=200 dev=I0.MN02 weight=2.24e-12 // NMOS1 s g
    block1_bridge_3 ( 0 xpd ) r=200 dev=I0.MN03 weight=2.24e-12 // NMOS1 s g
    ... ..
  }
}
block2 faults weight_factor=0.1 weight_expr=w {
  bridge {
    block2_bridge_1 ( vdda I0.net69 ) r=200 dev=I0.XR2 weight=8e-07 // resmod 1 2
    block2_bridge_2 ( vdda I0.net51 ) r=200 dev=I0.XR1 weight=7e-07 // resmod 1 2
  }
}
```

If the parameter `weight` is specified in the individual fault and `weight_expr` is also specified in the `faults` statement, like the fault list in above example, then, the explicit fault value has higher priority and weighting expression is not evaluated for that fault. This rule allows you to adjust some weight values manually before or after the fault list is generated and the given expression is evaluated.

If some of the device terminals are shorted, the weight multiplier for that device is based on the number of shorted terminals. For example, let us consider `bridge_fault (n1 n2)` for the following scenario.

```
info what=bridges faultdev=mosn faultterminals=[ d g s b]
```

- 1) M0 (n1 n2 n3 n4) mosn ...
multiplier = 1
- 2) M0 (n1 n2 n2 n3) mosn ...
multiplier = 2
- 3) M0 (n1 n2 n2 n2) mosn ...
multiplier = 3
- 4) M0 (n1 n1 n2 n2) mosn ...
multiplier = 4

In general, $\text{multiplier} = \text{number\_of\_shorted\_terminals\_at\_n1} * \text{number\_of\_shorted\_terminals\_at\_n2}$ for bridge inserted between `n1` and `n2`.

If `weight_expr=constant_value` is same for all the bridges before collapsing, then $\text{weight\_after\_collapsing} = \text{multiplier} * \text{const}$. If you manually assign different

weights for each bridge connected to different terminals, then `weight_after_collapsing = sum (weights_for_each_collapsed_bridge)`.

Open Faults

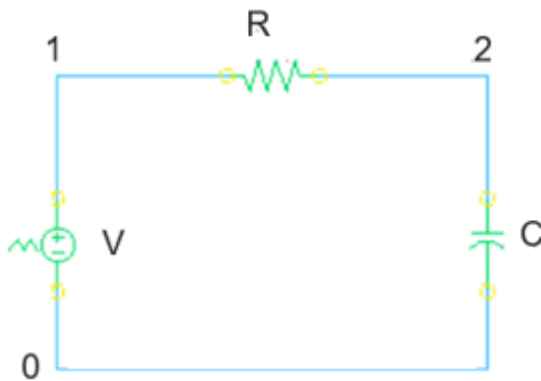
Open fault collapsing is different from the bridge collapsing since the collapsing condition for open faults is encountered lesser than bridge collapsing.

When two open faults are equivalent, they can be collapsed only if the union of all the terminals from {...} of both the statements is exactly the full set of terminals connected to the given node.

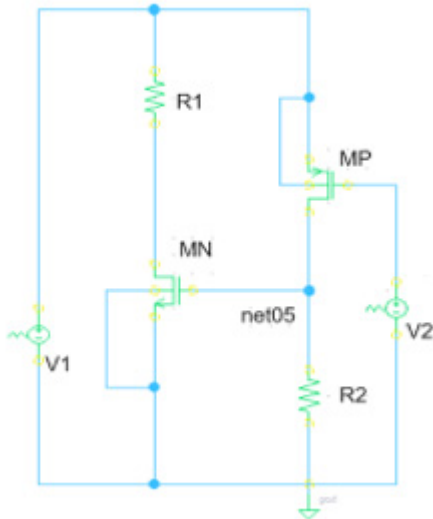
Spectre can handle the collapsing of only two opens because of the complexity that arises when too many terminals are connected to the same node. Below are a few examples explaining how the open faults collapsing works.

- Open faults defined on the same node but containing no identical terminals disconnected from a given node can be collapsed.

```
open_1 ( 2 ) r=1e9 { R }  
open_2 ( 2 ) r=1e9 { C }
```



- In the following schematic, each set of the equivalent opens for node `net05` can be collapsed.



```

Opn1 (net05) r=1G {MN:g} and Opn2 (net05) r=1G {MP:d R2:1}
Opn3 (net05) r=1G {MP:d} and Opn4 (net05) r=1G {MN:g R2:1}
Opn5 (net05) r=1G {R2:1} and Opn6 (net05) r=1G {MN:g MP:d}
    
```

- For two-terminal primitives, open faults for each terminal, for example, `open_1` and `open_3` shown below, are identical but redundant faults. Two separate opens are generated independent of the `faultrule` parameter in the `info` statement when `faultcollapse` is set to `no`. This behavior is aligned with IEEE2427. When `faultcollapse` is set to `yes`, one open fault with `weight=2` is generated.

```

open_1 ( 2 ) r=1e9 { R }
open_3 ( 1 ) r=1e9 { R }
    
```

For non two-terminal primitives, during open fault generation, when `faultcollapse=no` is set, the `m` factor is ignored according to the rule in the above table; `weight=1` is evaluated for every instance when no weight expression is given. If `weight_expr=w*1` is set, the weight is evaluated using $3u*2u=6e-12$ for the following instance.

```

M1 d g s b nch w=3u l=2u m=2
    
```

When `faultcollapse=yes` (which is the default) and `weight_expr=w*1` is given, Spectre APS evaluates the expression and applies the `m` factor during collapsing by using $3u*2u*2=12e-12$. The `weight=2` is evaluated when no expression is defined.

The open faults related to the parallel devices can be collapsed only in the Spectre APS mode. They are taken into account as extra factors to `weight_expr` values. However, the collapsing of parallel opens is not supported in Spectre baseline.

Limiting in Weight Expression

When the `faultdev` parameter is not specified or contains multiple types of devices or models, the weighting function in `weight_expr` may not be evaluated for some of the models. This occurs when the weighting function contains the parameter which does not belong to all models where the fault list is generated. In such situations, Spectre generates a warning message and assigns 0 as weight for that fault. To avoid 0 weight values, you can use the functions `fmin` and `fmax` with `weight_expr`.

In the following example, the use of `fmax` prevents the weight from becoming zero if the fault instance does not have parameters `w` (width), or `l` (length). If `w*l` cannot be evaluated, `1e-12` is assigned as the weight value.

```
weight_expr=fmax(w*l, 1e-12)
```

You can use `fmin` to limit the `weight_expr` values. In the following example, `fmin` clamps the maximum resistance which is used as the weighting function:

```
weight_expr=fmin(0.1, 0.001*r)
```

Weighted Likelihood Calculation

Some faults are more likely to occur than others; therefore, a test that detects the more likely faults will have a higher coverage than the one that detects the less likely faults. For this reason, Spectre allows you to calculate the defect coverage using the likelihood-weighted sum of the detected faults divided by the likelihood-weighted sum of all simulated faults. The parameters `weight_expr` and/or `weight_factor` in the `faults` statement can be used to specify weighted likelihood of the faults during fault list generation, or for an existing fault list.

The likelihood of a fault occurrence can be based on the circuit element area, proximity of the adjacent interconnect, length of the interconnect, or other factors. The weighting function expression `weight_expr` can be used to specify these types of effects, based on each device instance for a particular fault.

Defects can also be weighted by their potential impact on performance, safety, or reliability. For example, open and shorts may have different impact and likelihood for different applications. The `weight_factor` parameter allows you to specify the likelihood for all faults in a given fault block. It is a constant value for a specific block.

When the fault list consists of total N number of faults in one or multiple blocks, Spectre calculates the total weight by adding the weight of each fault. The weighted likelihood of the n th fault w_n is the weight value of that specific fault (based on `weight_expr` evaluation) normalized by the total weight of all faults, as shown below.

$$W_n = w_n / \sum_1^N w_i .$$

If a fault list consists of K fault blocks with `weight_factor`= ω_k , and the number of faults in each j th fault block is N_j then the weighted likelihood of the n th fault from the k th fault block is calculated as:

$$W_{kn} = \frac{\omega_k w_n}{\sum_{j=1}^K \left(\omega_j \sum_{i=1}^{N_j} w_i \right)}$$

The default value of the weight factor are $w=1$ and $\omega=1$. The default weighted likelihood value of each fault is given by:

$$W = \frac{1}{\sum_{j=1}^K N_j}$$

If `weight_expr` is not specified in the `info` analysis statement to generate the fault list, the weighted likelihood is calculated based on `weight=1` or `weight=#` due to fault collapsing for the individual fault.

The calculated value of weighted likelihood can be found in the table file when the simulation is completed.

To follow P2427 standard, Spectre skips a fault when its weight equals zero and prints a message indicating the same in the log file. Such faults are classified as `Unevaluated` in post-processing for the DDM and FuSa reports.

```
Fault analysis for func_s_bridge_15 : 3 time steps
Fault analysis of func_s_bridge_16 skipped because of zero weight.
Fault analysis for func_s_bridge_17 : 12 time steps
```

Fault Generation and Simulation With `faultcollapse` and `faultmerge`

The total number of generated faults using `info` analysis can be different with the different option settings of `faultcollapse` and `faultmerge`.

Two or more faults are considered equivalent when they produce the same circuit topology when they are injected even if they are related to different circuit instances or terminals. The `faultcollapse` option regulates the detection of equivalent faults and may reduce the total number of faults to be injected for simulation.

The `faultmerge` option deals with iterative and parallel device instances during fault list generation. By default, `faultmerge=yes`, all terminals of iterative or parallel devices are

shorted or opened simultaneously. As a result, the generated faults have higher weight values and the total fault count is decreased.

When `faultmerge=no` is specified, Spectre preserves all instances related to `faultdev` list, and the faults are generated separately for each iterative or parallel device instances. As a result, the fault count may be higher in the generated list and the fault simulation time may increase.

When the option `preserve_inst=all` is specified, `faultmerge=yes` has no effect.

When the number of faults get reduced by collapsing or merging, Spectre changes the weights of faults kept in the final fault list according to the following rules:

- With `faultcollapse=yes` and `faultmerge=yes`, the least number of faults are generated. The `weight` parameter in the `fault` statement considers the number of merged faults for iterated instances and parallel devices and the number of equivalent faults. This is the default setting in Spectre.
- With `faultcollapse=no` and `faultmerge=no`, the faults are generated separately for all iterated and parallel instances, and equivalent faults are included in the list. This settings results into the biggest number of faults to be simulated.
- With `faultcollapse=yes` and `faultmerge=no`, the equivalent faults are collapsed by changing the weighting factors. However, the faults sharing the same nodes but different type of devices in iterated or parallel instances are split into the individual faults.
- With `faultcollapse=no` and `faultmerge=yes`, the equivalent faults are not collapsed; however, the iterated or parallel instances are considered during fault generation with weighting factors applied.

Creating Open Faults When Two Terminals of an Instance are Connected to the Same Node

There are some applications where the transistors have their terminals tied together for a specific purpose. For example, if a variable capacitor is desired, you may connect the terminals of source and drain together and the capacitance between gate and drain is varied by the voltage crossing it. To create an open fault at the node where there are two terminals of element are shorted, the following syntax and examples cover all the possibilities using which you can generate the open fault:

1. Only the D terminal connects to the new fault node split from the original node

```
FaultOpen_1 info what=open faultterminals=[D] faultdev=bsim4 faultres=1e+9
Info1_open_1 (VDD) r=1e+9 { I0.MP0:D }
```

2. Only the S terminal connects to the new fault node

```
FaultOpen_2 info what=open faultterminals=[S] faultdev=bsim4 faultres=1e+9
Info1_open_2 (VDD) r=1e+9 { I0.MP0:S }
```

3. Both D and S terminals connect to the new fault node

```
FaultOpen_3 info what=open faultterminals=[D S] faultdev=bsim4 faultres=1e+9
Info1_open_3 (VDD) r=1e+9 { I0.MP0:D I0.MP0:S }
```

4. If no `faultterminals` are specified, the open faults are generated for all the terminals of `bsim4` where the gate and source terminals are connected to the new fault node.

```
FaultOpen_4 info what=open faultdev=bsim4 faultres=1e+9
Info2_open_1 (VDD) r=1e+9 { I0.MP0:D I0.MP0:S }
Info2_open_2 (VOUT) r=1e+9 { I0.MP0:B }
Info2_open_3 (VIN) r=1e+9 { I0.MP0:G }
```

If you need both 1) and 2) in one simulation, you can specify two `info` analyses and save the results to the same file.

Custom Fault Generation

To generate the custom fault list using `info` analysis, you need to define the faulty subcircuits, include the definition in the nominal netlist, and set the option `faultcustompreserve`.

`faultcustompreserve [name]`: specifies the list of subcircuit names to be used for custom insertion, replacement, or open generation.

Generating Faults at the Schematic Boundaries for a Subcircuit

Spectre enables you to generate faults for a subcircuit at the schematic boundaries only, and not for all primitives within the subcircuit.

```
subckt pmos d g s b
parameters l=1u w=10u
    M0 d2 g2 s2 b2 pchmod l=l w=w
    rd d d2 resistor r=1
    rg g g2 resistor r=1
    rs s s2 resistor r=1
    rb b b2 resistor r=1
ends pmos
```

```
model pchmod bsim4 type=p mobmod=0 capmod=2 version=4.21 tox=3e-9 vth0=-0.42
```

...

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To generate faults for a subcircuit at the schematic boundaries, you need to define the options for subcircuit names in the vector, along with the option `faultmacro=yes`.

```
opt options mosmacro=[pmos] faultmacro=yes
short_block info what=bridges where=file faultdev=[pmos] \
    file="fault_list.scs" faultblock="bfault" faultres=10
```

Using the `info` analysis and options defined above, the fault list is generated as below.

```
bfault faults {
    bridge {
        bfault_bridge_1 ( 0 d ) r=10 dev=MP          // pmos d      g
        bfault_bridge_2 ( 0 g ) r=10 dev=MP          // pmos d      s
        bfault_bridge_3 ( 0 s ) r=10 dev=MP          // pmos d      b
        bfault_bridge_4 ( d g ) r=10 dev=MP          // pmos g      s
        bfault_bridge_5 ( d s ) r=10 dev=MP          // pmos g      b
        bfault_bridge_6 ( g s ) r=10 dev=MP          // pmos s      b
    }
}
```

Generating Faults According to IEEE P2427 Standard

You can use the option `faultrule=2427` in the `info` statement to generate faults that comply with the IEEE P2427 standard. Using `faultrule=2427` in the `info` statement enables you to generate the bridge or open fault list without specifying the `faultdev` and `faultterminals` parameters. Spectre generates all possible faults for all devices according to the requirements of the device terminals from IEEE P2427. The following table lists the number of faults for each type of device when no other fault parameter is specified:

Primitive/Device	Terminal Index for Bridges	Terminal Index for Opens
bipolar, mosfet, jeft	1, 2, 3	1, 2, 3
resistor, capacitor, diode	1, 2	1
inductor	1, 2	1
vsource	1, 2	1
isource	1, 2	1
bsource	All	all
verilog	All	all
controlled sources	All	all

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iprobe, mutual inductor	None	none
transmission line, port, relay	All	all
Unknown	All	all

If `faultdev` and `faultterminals` parameters are specified along with `faultrule=2427`, `faultdev` and `faultterminals` values are processed instead of the predefined values. Rest of the devices that are not specified in `faultdev` retain the predefined values.

For example, if both `bsim4` and `bsim3v3` models are used in the same netlist with the following `info` statement, Spectre will generate 3 bridges for each `bsim4` device and 1 bridge for each `bsim3v3` instance.

```
Bridge_2427 info what=bridges faultrule=2427 faultdev=bsim3v3 \
faultterminals=[d s]
```

With the same `info` statement, with `faultrule=none`, Spectre will generate only 1 bridge per each `bsim3v3` instance and skip all the other devices.

```
Bridge_None info what=bridges faultrule=none faultdev=bsim3v3 \
faultterminals=[d s]
```

For options `mosmacro=[subcktName]` and `faultmacro=yes`, the type of device or primitive is unknown with no predefined rule when `faultrule=2427` is applied; all the terminals are taken into consideration during the fault generation.

Examples on Fault generation Using info Analysis

Following are some examples on fault generation using `info` analysis:

- The following example creates bridge faults across drain, gate, and source terminals for primitive `bsim4` only within the scope of subcircuit instance `I1.xosc`.

```
FaultList1 info what=bridges where=file file=faultList1.scs
faultblock=b4Bridges faultdev=bsim4 faultterminals=[d g s] faultres=10
inst=I1.xosc
```

- The following example creates bridge faults for subcircuit instance `INV` across first and second terminals within the scope of subcircuit `xmem`.

```
FaultList2 info what=bridges where=file file=faultList2.scs
faultblock=invBridges faultdev=INV faultterminals=[1 2] faultres=10
subckt=xmem
```

- The following example generates stuck-at faults by specifying the nets `vdd` and `gnd` using the `faultstuckat` parameter and `what=bridges`, as shown below.

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```
FaultListStuckat info what=bridges faultstuckat=[vdd gnd] where=file
file=faultStuckat.scs faultblock=b4stuckat faultdev=bsim4 faultterminals=[d g
s] faultres=10 inst=I1.xosc
```

- The following example creates open faults for bsim4 transistors at gate and drain terminals by inserting 1 G resistors. The transistors in subcircuit instance of I0.xmem are excluded.

```
FaultList3 info what=opens where=file file=faultList3.scs faultblock=b4Opens
faultdev=bsim4 faultterminals=[g d] faultres=1G xinst=I0.xmem
```

- The following example creates open faults for all resistor instances at the first terminal by inserting a 1 G resistor. The resistors defined in subcircuit xosc are excluded:

```
FaultList4 info what=opens where=file file=faultList4.scs faultblock=resOpens
faultdev=resistor faultterminals=[1] faultres=1G xsubckt=xosc
```

- When multiple defect parameters are defined in faultres=[100 500 1000], three different fault blocks are generated with different resistor values. The defect parameter sweeping is supported by parameter range(start, stop, step).

```
BRG1 info what=bridges file=bridges.scs faultdev=bsim4 faultres=[100 500 1000]
BRG2 info what=bridges file=bridges.scs faultdev=bsim4
faultres=[range(100,1000,300)]
```

- The following example generates the parametric faults of altering global temperature for the circuit.

```
FaultParam1 info what=faultparam where=file file=faultList8.scs
faultparam=temp faultvalues=[-50 0 25 50]
```

- The following example generates the parametric faults with specifying values in percentage. The temperature values altered are 21.6 and 40.5 if nominal temperature is 27.

```
FaultParam11 info what=faultparam where=file file=faultList88.scs
faultparam=temp faultpercentage=[-20 50]
```

- The following example generates parametric faults by altering the gate length for all bsim4 devices:

```
FaultParam2 info what=faultparam where=file file=faultList9.scs faultparam=l
faultstart=1p faultstop=5p faultstep=1p faultdev=bsim4
```

- The following example generates parametric faults by altering the gate length for all devices in specific subcircuit one by one:

```
FaultParam3 info what=faultparam where=file file=faultList10.scs faultparam=l
faultstart=1p faultstop=5p faultstep=1p faultdev=bsim4 inst=I0.I1
```

- The following example generates faults of altering both gate width and length for all bsim4 devices:

```
FaultParam4 info what=faultparam where=file file=faultList11.scs
faultdev=bsim4 faultparam==[w l] faultvalues=[1e-6 1e-5 5e-6 5e-5]
or
```

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```
FaultParam4 info what=faultparam where=file file=faultList11.scs
faultdev=bsim4 faultparam=[w l] faultfile=param.dat
```

or

```
FaultParam4 info what=faultparam where=file file=faultList11.scs
faultdev=bsim4 faultparam=[w l] faultpercent=[-50 -10 10 50]
```

- When multiple defect parameters are defined in `faultres=[100 500 1000]`, three different fault blocks are generated with different resistor values. The defect parameter sweeping is supported by the parameter range(start, stop, step).

```
BRG1 info what=bridges file=bridges.scs faultdev=bsim4 \
      faultres=[100 500 1000]
```

```
BRG2 info what=bridges file=bridges.scs faultdev=bsim4 \
      faultres=[range(100,1000,300)]
```

- The following example generates custom faults of `faultsubckt` to replace `bsim4` devices.

```
FaultList5 info what=customreplace where=file file=faultList5.scs
faultcustom=faultsubckt faultdev=bsim4
```

- The following example generates the parametric faults of altering the default value of a model parameter.

```
FaultParam5 info what=faultparam where=file file=faultList12.scs
faultparam=tox faultstart=4n faultstop=10n faultstep=2n faultdev=mosn
```

- The following example generates the parametric faults of altering the value of a subcircuit parameter.

```
faultparam6Faultparam6 info what=faultparam where=file file=faultList13.scs
faultparam=res faultvalues=[1e3 2e3 10e3] faultdev=I1.I1
```

- The following example generates the parametric faults of altering the parameters of a circuit element.

```
Faultparam7 info what=faultparam file= faultList14.scs faultdev=vsource
faultparam=[vall rise fall] faultstart=[1 1m 1.5m] faultstep=[1 0.1m 0.1m]
faultstop=7
```

- The following example generates open faults of `faultsubckt` to be inserted at each terminal of `bsim4` devices.

```
FaultList7 info what=customopen where=file file=faultList7.scs
faultcustom=faultsubckt faultdev=bsim4 faultterminals=[d g s]
```

Note: Custom fault subcircuit must have the same matching number of terminals as `faultdev`. If `faultdev` has more terminals than the custom fault subcircuit, then `faultterminals` is used for matching.

The following two examples show the notations of custom insertion. The original resistor instances of `R11` and `R12` will be inserted with sub-circuit `fault_to_insert` in parallel.

```
custom {
```

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```
insTest_insert_1 ( n0 n1 ) fault_to_insert      // R11 resistor
insTest_insert_2 ( n1 n2 ) fault_to_insert      // R12 resistor
}
```

For custom replacement, the original instance X1 which instantiates sub-circuit of `invx` will be replaced by `fault_to_replace`.

```
custom {
    repTest_replace_1 ( n2 out vdd vss ) fault_to_replace original_inst=X1 /
/ X1    invx
}
```

For the custom open, the commenting notation explains the terminal index 2 of resistor `Rin` splits into two nodes and subcircuit `fault_to_open` is inserted in between.

```
custom {
    repTest_open_1 ( n2 ) fault_subckt=fault_to_open { Rin:2 }    // Rin
resistor 2
}
```

- The following example generates parametric faults by altering the global temperature for the circuit.

```
FaultParam1 info what=faultparam where=file file=faultList8.scs
faultparam=temp faultvalues=[-50 0 25 50]
```

- The following example generates the parametric faults by altering the nominal temperature by a percentage value. The altered temperature values are 21.6 and 40.5 if the nominal temperature is 27.

```
FaultParam11 info what=faultparam where=file file=faultList88.scs
faultparam=temp faultpercentage=[-20 50]
```

- The following example generates parametric faults by altering the gate length for all `bsim4` devices.

```
FaultParam2 info what=faultparam where=file file=faultList9.scs faultparam=l
faultstart=1p faultstop=5p faultstep=1p faultdev=bsim4
```

- The following example generates parametric faults by altering the gate length for all devices in specific subcircuit one by one.

```
FaultParam3 info what=faultparam where=file file=faultList10.scs faultparam=l
faultstart=1p faultstop=5p faultstep=1p faultdev=bsim4 inst=I0.I1
```

- The following example generates parametric faults by altering the gate length for one specific device.

```
FaultParam4 info what=faultparam where=file file=faultList11.scs faultparam=l
faultstart=1p faultstop=5p faultstep=1p faultdev=I0.I1.MN1
```

- The following example generates parametric faults by altering the default value of a model parameter.

```
FaultParam5 info what=faultparam where=file file=faultList12.scs
faultparam=tox faultstart=5p faultstop=50p faultstep=5p faultdev=mosn
```


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- The following example generates parametric faults by altering the value of a subcircuit parameter.

```
Faultparam6 info what=faultparam where=file file=faultList13.scs
faultparam=res faultvalues=[1e3 2e3 10e3] faultdev=I1.I1
```

Fault Generation with Option `faultlocal`

When `faultlocal=yes` is enabled with parameter `inst=[...]` or `sub=[...]`, the local node names for faults are created in fault generation.

When faults are generated with the `faultlocal` parameter, the subcircuit name is created in fault block, the nodes in fault list are referred to the subcircuit as shown in the following example:

```
func_s info what=bridges where=file file=faultlist_noweightexpr.scs
faultdev=[bsim4] faultterminals=[1 2 3] subckt=pll_reg_bg faultlocal=yes
```

The fault list for this example is shown below.

```
func_s faults sub=pll_reg_bg {
  bridge {
    func_s_bridge_1 ( agnd_h vbg ) r=10 dev=[M12 M16] weight=2 // bsim4 s d
    func_s_bridge_2 ( agnd_h en_hn ) r=10 dev=I0.M6 // bsim4 s d
    func_s_bridge_3 ( agnd_h en_fh ) r=10 dev=I1.M6 // bsim4 s d
    func_s_bridge_4 ( agnd_h net097 ) r=10 dev=M11 // bsim4 s d
    func_s_bridge_5 ( agnd_h net0164 ) r=10 dev=M18 // bsim4 s d
  }
}
```

When generating faults without setting parameter `faultlocal`, or . The nodes in fault list show the hierarchical names from the top level in the circuit.

```
func_s info what=bridges where=file file=faultlist_noweightexpr.scs
faultdev=[bsim4] faultterminals=[1 2 3] subckt=pll_reg_bg
```

The fault list for this example is shown below.

```
func_s faults {
  bridge {
    func_s_bridge_1 ( 0 bandgap ) r=10 dev=[I0.M12 I0.M16] weight=2 // bsim4 s d
    func_s_bridge_2 ( 0 I0.en_hn ) r=10 dev=I0.I0.M6 // bsim4 s d
    func_s_bridge_3 ( 0 I0.en_fh ) r=10 dev=I0.I1.M6 // bsim4 s d
    func_s_bridge_4 ( 0 I0.net097 ) r=10 dev=I0.M11 // bsim4 s d
    func_s_bridge_5 ( 0 I0.net0164 ) r=10 dev=I0.M18 // bsim4 s d
  }
}
```

Layout-Based Fault Generation

Spectre info analysis for fault list generation is enhanced to support post-layout circuits with accurate transistor-level netlist (DSPF) using the following parameters.

`faultextract=no | spf | sch`

- Enables layout-based fault list generation when a dspf file is included in the netlist. Possible values are `no`, `spf` and `sch`.
- When set to `spf`, the generated fault list is compatible with the original post-layout netlist (with `dspf_include` file).
- When set to `sch`, the generated fault list is compatible with schematic netlist (with `dspf_include` file).
- When `faultextract=no`, it is the default setting when post-layout netlist is used.

Default is `no`.

`what=bridges faultextract=spf`

Generates shorts across all plausible (per parasitic capacitor), interconnect net pairs including all signal nets, power-ground nets, shorts between nets on adjacent layouts such that at most one short is modeled per net pair.

`what=opens faultextract=spf`

Generates an open on each unique branch of interconnect net including all signal nets and power-ground nets, such that at most one open is modeled per branch.

Note: `faultextract` is not supported for stuck-at faults.

<code>faultcmin</code>	Defines the minimum capacitance value an extracted parasitic capacitor must have to be identified as a bridge defect during the generation of faults. The extracted parasitic capacitors will not be identified as short defects if $C < \text{faultcmin}$. By default, <code>faultcmin=1e-20</code>.
<code>faultrmin</code>	Defines the minimum resistance value an extracted parasitic resistor must have to be identified as an open defect during the generation of faults. The extracted segment resistors will not be identified as open defect locations if $R < \text{faultrmin}$. By default, <code>faultrmin=0.001</code>.
<code>faultlevel</code>	Defines the highest hierarchical level of subcircuits to generate faults. 0 is used for top level faults.
<code>faultlayer=[...]</code>	Layer numbers on which layout-based faults are to be identified. Set this option to 0 to identify faults on all layers including the connectivity between layers. Set it to a set of layer numbers, <code>[x y ...]</code>, to identify faults on those layers, or set it to a range, <code>[(x,y)]</code>, to identify faults for all layers in the range, excluding the connectivity between layers in both cases.

Spectre identifies at most one short defect per net pair, firstly transistor-shorts would occupy net pairs if the terminals are specified in `faultterminals=[...]`. After that, net-shorts locations are identified by the largest parasitic coupling capacitor in the net pair. Multiple open defects on the same branch is prevented. Primarily branches are taken by transistor-opens if the terminals are specified in `faultterminals=[...]`. Next, opens are identified per branch if the parasitic resistor exceeds the threshold.

`what=bridges faultterminals=[...]`

List of device terminals to be considered for fault generation. By default, all terminals of `faultdev` are considered.

`what=opens faultterminals=[...]`

List of device terminals to be considered for fault generation. By default, `[d g s][1 2 3]` of `faultdev` are considered. This should be for MOS devices only.

Transistor-shorts and net-shorts can be equivalent and therefore, represented by only one short when their parasitic coupling capacitors located in the same net pair. Parameter `weight` is not supported for layout-based fault list. Similarly, branch-opens can be ignored if the branch has contained a transistor-open. A major application of `faultextract` option is to generate net-shorts and branch-opens.

The following examples explain the fault identification for net shorts and transistor shorts in a layout-based netlist:

- The following example generates only net-shorts

```
...what=bridges faultextract=spf
```

- The following example generates only net-shorts for parasitic C

```
...what=bridges faultextract=spf faultdev=[capacitor]
```

- The following example generates all net-shorts and all transistor-shorts

```
...what=bridges faultextract=spf faultdev=[*]
```

- The following example generates all net-shorts and transistor-shorts for `g45nlsvt` and `g45plsvt`

```
...what=bridges faultextract=spf faultdev=[g45nlsvt g45plsvt]
```

- The following example generates only transistor-shorts identical to info analysis with `faultextract=no`

```
...what=bridges faultextract=spf faultdev=[resistor g45nlsvt g45plsvt ]
```

The following examples explain the fault identification for branch opens and transistor opens in layout-based netlist:

- The following example generates only branch opens:

```
...what=opens faultextract=spf
```

- The following example generates only branch-opens for parasitic R:

```
...what=opens faultextract=spf faultdev=[resistor]
```

- The following example generates all branch opens and all transistor opens:

```
...what=opens faultextract=spf faultdev=[*]
```

- The following example generates all branch opens and transistor opens for `g45nlsvt` and `g45plsvt`:

```
...what=opens faultextract=spf faultdev=[g45nlsvt g45plsvt]
```

- The following example generates only transistor-opens, identical to info analysis with `faultextract=no`:

```
...what=opens faultextract=spf faultdev=[g45nlsvt g45plsvt]
```

- The following examples create net shorts and branch opens:

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```
BridgeList info what=bridges faultextract=spf file=bridges.scs faultcmin=1f
OpenList info what=opens faultextract=spf file=opens.scs faultcmin=0.1
```

- With DSPF included in the netlist, you may specify `faultextract=sch` to create schematic transistor shorts. However, an open fault is not compatible in schematic option.

```
BridgeList info what=bridges faultextract=sch file=bridges.scs faultcmin=1f
```

Use Model of faultlayer

The parameter `faultlayer` is valid only when `faultextract` is specified in info analysis. The detailed use model for `faultlayer` and `faultlevel` is given below.

- When `faultlayer=0`, faults generated for all layers, including the connectivity between layers.
- When `faultlayer=[3 5]`, faults generated only for layer #3 and #5, excluding the connectivity between different layers.
- When `faultlayer=[range(1, 8)]`, faults generated for all layers from #1 to #8, excluding the connectivity between different layers.
- When `faultlevel=#LVL` and `faultlayer=$lvl` are both specified, then faults are generated only for the instances with hierarchical depth $\leq$ #LVL, and only belonging to the levels of \$lvl according to LAYER_MAP from dspf.

For example, when `faultlevel=2 faultlayer=[4 7]` is specified and applied to the dspf file, The hierarchical depth ≤ 2 (X0/X##/N1) are first filtered and then the same layers of #4 and #7 are applied for fault injection.

```
C111 VDD X0/X11/N1 3.50548e-18 $X=299.92 $Y=19.5155 $lvl1=2 $lvl2=1
C222 VDD X0/X22/N1 2.91933e-18 $X=299.989 $Y=19.516 $lvl1=2 $lvl2=1
C333 VDD X0/X33/N1 2.83581e-18 $X=300.055 $Y=21.04 $lvl1=3 $lvl2=1
C444 VDD X0/X44/N1 1.49123e-18 $X=300.2605 $Y=22.9175 $lvl1=7 $lvl2=7
C555 VDD X0/X55/N1 1.48015e-18 $X=300.604 $Y=22.9645 $lvl1=7 $lvl2=1
C666 VDD X0/X66/N1 6.02522e-18 $X=300.5905 $Y=15.8025 $lvl1=4 $lvl2=4
```

Use Model Examples of a Layout-Based Fault Simulation

With the fault list generated with info statement, as well as with `faultextract` included in the netlist, you can run fault simulation for DFA or TFA with APS or Spectre X. Using Spectre X, APS with `+postlayout` may reduce the fault universe from the original fault list. Spectre prints warnings in the case when original connectivity cannot be retained.

Post-Layout Fault Simulation

1. Include the fault list generated by `faultextract=spf`.
2. If required, include other fault lists generated without `faultextract` for the given netlist.
3. Add Direct Fault Analysis DFA, or Transient Fault Analysis TFA statement into original netlist.
4. Perform simulation using Spectre, APS with `postlayout=upa/hpa/default`, or Spectre X with `preset=cx/ax/mx/lx/vx`.

Pre-Layout Fault Simulation

1. Generate fault lists with `faultextract=sch`.
2. Comment-out '`dspf_include`' in original netlist or use related schematics netlist for fault simulation only.
3. Include fault lists from step 1.
4. If required, include other fault lists generated without `faultextract` for the schematic netlist.
5. Add DFA, or TFA statement into the netlist.
6. Perform simulation using Spectre, APS, or Spectre X with `preset=cx/ax/mx/lx/vx`.

Note: One step simulation is not supported in layout-based fault simulation.

Fault Universe Details Saved from Fault Generation

According to IEEE P2427 requirements, Analog Fault Analysis provide a way to save the fault universe information in SQLite DB. A parameter `faultuniverse` is introduced in info analysis to specify the db file name to save fault universe details.

```
brg info what=bridges file=faultlist.scs faultuniverse=funiverse.db
opn info what=opens file=faultlist.scs faultuniverse=funiverse.db
```

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You can then use any DB browser for SQLite to open the file and check the contents.

	ID	Name	Model	Multiplier	DefectSite	Defect	Weight
	Filter	Filter	Filter	Filter	Filter	Filter	Filter
1	brg_bridge_1	X0.M21.nch2 X0.M22.nch2	hisim_hv	1	sub - g	bridge 100 Ohm	3.0
2	brg_bridge_2	X0.M22.nch2	hisim_hv	1	sub - d	bridge 100 Ohm	1.0
3	brg_bridge_3	VSS1	vsouce	1	n - p	bridge 100 Ohm	1.0
4	brg_bridge_4	X0.M21.c0 X0.M21.nch2 X0.M22.c0 ...	capacitor	1	n - p	bridge 100 Ohm	5.0
5	brg_bridge_5	VDD1	vsouce	1	n - p	bridge 100 Ohm	1.0
6	brg_bridge_6	VDD2	vsouce	1	n - p	bridge 100 Ohm	1.0
7	brg_bridge_7	X0.M21.nch2	hisim_hv	1	sub - b	bridge 100 Ohm	1.0

The ALL_DEFECT_UNIVERSE table shows all the faults with the common information as above. Choose MOS-DEFECTS from the Table drop-down list to display the columns for the four terminal nodes, length and width.

	ID	Name	D	G	S	B	Model	L	W	Multiplier	DefectSite	Defect	Weight
	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
1	brg1_bridge_9	X0.M12.nch1	V12	V11	VSS1	VSS1	bsim3v3	9.0e-08	5.0e-06	1	g - d	bridge	1.0
2	brg1_bridge_12	X0.M12.nch1	V12	V11	VSS1	VSS1	bsim3v3	9.0e-08	5.0e-06	1	d - b	bridge	2.0
3	opn1_open_7	X0.M12.nch1	V12	V11	VSS1	VSS1	bsim3v3	9.0e-08	5.0e-06	1	d	open	2.0
4	opn1_open_17	X0.M11.nch1	V11	V11	VSS1	VSS1	bsim3v3	9.0e-08	5.0e-06	1	s	open	1.0

With these tables, it is convenient to analyze or debug the fault issue if needed.

Fault Generation Based on Circuit Activity Analysis

Certain circuit elements that do not affect the intended application of the integrated circuit under any specified operation can be considered as unused circuitry during fault analysis. According to IEEE P2427, defects in unused circuitry can be excluded from calculation of defect coverage. Defects that are likely not to be detected by any conceivable test can be considered as potentially undetectable. Such potentially undetectable defects may be counted as undetected without simulating them according to IEEE P2427.

Performing analysis of DUT activity before generating the defect universe (fault list) lets you identify the unused circuitry, or the circuit elements with no or low activity. Faults related to such elements may be considered as potentially undetectable and are excluded from injection and simulation.

In Spectre fault generation with `info` analysis, the `infonames=[...]` parameter is used to trace the activity in transient so that the potentially undetectable faults are assigned by zero weight and excluded from fault simulation.

In the following statements, the transient analysis enables the signal activity tracing for fault generation with `infonames=[...]` specified

```
info1 info what=bridges faultdev=bsimcmg faultactivethresh=0.05
info2 info what=opens faultdev=bsimcmg faultactivethresh=0.05
tran1 tran stop=1m infonames=[info1 info2] infotimes=[0.75m 0.75m]
faultactivevabstol=0.11 faultactiveiabstol=5u
```

The following parameter is supported for activity analysis in `info` statement:

<code>faultactivethresh=0</code>	The minimum activity ratio of the circuit element to identify the related faults as potentially undetectable. The value is calculated as the ratio of time points when the element was active to the total number of active time points.

The following parameters are supported for activity analysis in `transient` statement:

<code>faultactivevabstol=100m</code>	The minimum voltage value to consider the element as active for fault list generation purposes.
<code>faultactiveiabstol=1u</code>	The minimum current value to consider the element as active for fault list generation purposes.
<code>faultactiveiabstol=1u</code>	The time to begin circuit activity tracing for fault list generation.

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Note: The activity tracing is fully time-step based. It is supported for transient analysis only.

The example faults below are generated based on the activity tracing in transient analysis, these faults with zero weight are excluded from fault injection and simulation. However, they are saved in the table file. Currently, the faults with zero weight are classified as 'unevaluated' in detailed detection reports.

```
bridge {
  tran_000_sh_bridge_1 ( 0 VDD ) r=100 dev=[I1 I1.I1 I1.I2 V1] weight=5           // X2  0    d
  tran_000_sh_bridge_2 ( 0 VIN ) r=100 dev=[I1 I1.I1 I1.I1.R1 I2 I2.I1 I2.I1.R1 V2] weight=7 // X2  0    g
  tran_000_sh_bridge_3 ( 0 VS ) r=100 dev=[I1 I1.I2 I2 I2.I1 I2.I2 V3] weight=0     // X2  0    d
  tran_000_sh_bridge_4 ( 0 VB ) r=100 dev=[I1 I1.I1 I1.I2 I1.I2.C1 I2 I2.I1 I2.I2 I2.I2.C1 V4] weight=0 // X2  0    b
  tran_000_sh_bridge_5 ( 0 I1.n1 ) r=100 dev=[I1.I1 I1.I2] weight=3                // X2  0    s
  tran_000_sh_bridge_6 ( 0 I2.n1 ) r=100 dev=[I2.I1 I2.I2] weight=0                // X2  0    s
  tran_000_sh_bridge_7 ( VDD VIN ) r=100 dev=[I1 I1.I1 I1.I1.I1 I1.I1.I1.M1] weight=4 // X1  d    g
  ... ..
}
```

Fault Generation for Design Hierarchy Extraction

Spectre provides the Design Hierarchy Extraction (DHE) feature that can be used in Cadence Safety Solution. With `info` analysis, the design hierarchy is saved in a format that is compatible with Midas Safety Platform and is used for FMEDA management.

DHE is enabled with the keyword `what=dhe` in `info` analysis.

<code>dheminarea=0um^2</code>	The lower bound of an area value for a device to be considered during design hierarchy extraction.
<code>dhesubckt=[...]</code>	Design hierarchy is generated for all instances of the specified subcircuits.
<code>dheinst=[...]</code>	Design hierarchy is generated for the specified subcircuit instances.
<code>dhexsubckt=[...]</code>	All instances of the specified subcircuits are excluded from the design hierarchy.
<code>dhexinst=[...]</code>	The specified subcircuit instances are excluded from the design hierarchy.
<code>dheparams=[...]</code>	Name of the file that provides the rules to calculate area for subcircuits when <code>what=dhe</code> .

An example `info` statement is shown below.

```
DHE info what=dhe file=topdhe
```

After the simulation is run successfully, you can use the `topdhe.db` file, which is saved in the `output` directory, as an input file for Midas.

The following example shows how to save the design hierarchy in the format that is compatible with Midas Safety Platform and then used for FMEDA management.

```
DHEParam info what=dhe where=file file="mydhe.txt" dheparams=subckt.txt
```

where the `subckt.txt` file contains optional rules mentioned below to calculate the area for specified subcircuit. Wildcards can be used in subcircuit names.

```
### subckt name : area expr
mcell      :      1*w*nf*m + 1*p*(nf-1)*m
mincap*    :      ls*ws*mf
fetcap*    :      wr*lr*multi
```

Fault Selection and Sampling

Fault injection and simulation can be an extremely time-consuming task for large designs. Spectre provides the capability to perform simulation process for a portion of the original fault list, or to pick only specific faults for debugging purposes. Spectre scoping option allows to simulate the fault injection for different blocks of design separately without changing the complete fault list. The results can be merged during postprocessing.

The following parameters can be applied for selection of a subset of the fault universe during transient or sweep analysis for fault simulation:

<code>faults=[...]</code>	Names of the fault blocks in the fault list to perform transient fault analysis. The default value is <code>faults=[*]</code> .
<code>faultsid=[...]</code>	Indexes of faults from the fault list to perform fault analysis. If specified, simulation performed for requested subset of fault list. Faults index can be a discrete number, series of numbers, or a range of numbers specified <code>range (start, stop)</code> .
<code>faultsname=[...]</code>	Names of faults from the list to perform fault analysis. If specified, simulation is performed for the requested subset of the fault list.
<code>faultsinst=[...]</code>	List of instances to perform fault analysis. If specified, simulation is performed only for faults within the specified instances.

Spectre also provides a few sampling techniques in the cases where all possible defect simulation becomes impractical. To enable random fault sampling in Spectre, it is enough to specify just the number of samples you prefer to simulate. Based on the accuracy and simulation time requirements, you can change the default settings of the sampling-related options.

The list of parameters for random fault sampling in sweep (DFA) or transient (TFA) analyses:

<code>faultsamplenum</code>	Number of random samples out of the total fault count. The default value is the selected fault count.

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<code>faultsampleratio=[R1 R2]</code>	A set of two values R1 and R2 to simulate the samples between the given range. Each value is the number of random samples (in percentage) out of the total fault count in the list. <code>faultsampleratio=R</code> is equivalent to <code>faultsampleratio=[0 R]</code>. The default value is 100%.
<code>faultseed</code>	Starting seed for random number generator.
<code>faultsamplemethod</code>	Specifies the random number distribution, or sorting algorithm to be used for fault sampling. Possible values are <code>random</code> , <code>weightsorted</code> , <code>randomweighted</code> , and <code>randomuniform</code> .
<code>faultsamplereplace</code>	Perform fault sampling with sample replacement during fault analysis. Possible values are <code>no</code> and <code>yes</code>. Default value is <code>no</code>.
<code>faultsamples</code>	File name to save sampled fault list when <code>faultsamplemethod</code> is specified.
<code>faultdetratio</code>	Auto-stop fault simulation when the specified detection ratio in percentage achieved; detection coverage estimated according to sampling method specified.
<code>faultconfidlevel</code>	Auto-stop fault simulation when the specified detection ratio achieved with given confidence level; compatible only with <code>randomweighted</code> and <code>randomuniform</code> sampling methods when <code>faultdetratio</code> is specified; Clopper-Pearson interval used to estimate confidence.

There are two choices to specify the number of samples out of the fault universe according to the fault blocks specified by the `faults` parameter. In the transient or sweep analysis statement, you may use either `faultsampleratio=R` to set the percentage (in the range from 0% to R%) to perform random sampling. With the setting of `faultsampleratio=[R1 R2]`, Spectre generates the number of samples between R1% and R2% of total number of faults. The simulation results with incremental percentage sampling can be merged later during postprocessing.

If both `faultsampleratio` and `faultsamples` are specified in the netlist, the parameter defined later in the statement will overwrite the one defined earlier.

Weighted Random Sampling

When `faultsamplemethod=randomweighted`, discrete random number distribution is used for fault sampling. Sampling process picks integer values according to the discrete probability distribution where weighted likelihood is considered as a predefined probability of being selected for each fault in the fault list.

Spectre provides the possibility to generate the fault list with the weight assigned to each or some faults based on the netlist information. For instance, we can assume that the likelihood of defects in a transistor is proportional to its area, the likelihood of defects in the design-intend resistors and capacitors can be proportional to their resistance and capacitance respectively. The following info analyses statements can be used in such a case to generate bridge faults:

```
Info1 info what=bridges faultdev=bsim4 weight_expr=w*1
Info2 info what=bridges faultdev=resistor weight_expr=r weight_factor=1e-12
Info3 info what=bridges faultdev=capacitor weight_expr=c weight_factor=1e5
```

Here, the parameter `weight_factor` is used as a proportionality constant to correlate the likelihood of defects related to the different type of devices. You may run the fault generation process a few times to estimate the weight values in different fault blocks, and to adjust `weight_factor` accordingly before starting fault sampling and simulation.

If the fault list is generated without `weight_expr` specified, Spectre assigns the weight values based on multiplication factor of related devices, and the number of collapsed faults when the option `faultcollapse=yes` is used in the fault list generation. The weight values will be integers in such a case and the default weight is 1.

The weighted random sampling can be performed with or without replacement. By default, sampling is performed with replacement, which means that the selected fault remains in the sampling pool and may be sampled again. With this method, the simulated fault number can be fewer than the number of samples. Setting `faultsamplereplace=no` in sweep or tran statement can disable the replacement of samples.

In the `randomweighted` sampling method, it is assumed that each fault has an assigned weighted likelihood w_i . The weighted likelihood for all faults is normalized before the sampling process starts.

$$\sum_{k=1}^N w_k = 1$$

Thus, the fault list contains an absolute value of fault weights, the table file contains the normalized weight values, i.e. the weighted likelihood.

If n samples are selected from the fault list, the simulation consists of N fault statements. The discrete probability distribution is used to draw samples.

$$P(i; w_1, w_2, \dots, w_N) = w_i$$

The weighted likelihood w_i is considered as the probability of the given fault to be selected for simulation.

In sampling with replacement:

- The faults with larger weighted likelihood can be sampled multiple times
- The number of simulations can be less than number of selected samples n
- The estimated defect coverage is calculated as the ratio of the sum of weighted likelihoods of detected samples n_d to the sum of weighted likelihoods of all samples n .

$$\frac{w_d}{w_n} = \sum_{k=1}^{n_d} w_k / \sum_{k=1}^n w_k$$

- The recurring samples are counted according to the number of times selected

In sampling without replacement:

- Each fault can be sampled only once
- Faults with larger weighted likelihood have higher probability to be drawn
- The number of simulations equals the number of selected samples
- The estimated defect coverage is the ratio of the sum of weighted likelihoods of detected samples to the sum of weighted likelihoods of all sampled faults.

$$\frac{w_d}{w_n} = \sum_{i=1}^{n_d} w_i / \sum_{k=1}^n w_k$$

Confidence interval can be evaluated based on the estimated detection coverage for weighted random sampling using `spectre_ddmrpt` or `spectre_fsrpt`.

Uniform Random Sampling

The uniform random sampling method can be selected using `faultsamplemethod=randomuniform` in `sweep` or `tran` statement. This method excludes the weighted likelihood from consideration despite the weight may be included in the fault list. This setting can also be useful when the fault list contains mixed types of faults and the weighting expression can be hard to evaluate for some portion of the faults from the list.

Sampling is performed without replacement by default. Setting `faultsamplereplace=no` in `sweep` or `tran` statement can enable replacement in sampling process.

In `randomuniform` sampling method, the uniform discrete distribution for integers is used to draw the samples.

$$P(i; 1, N) = \frac{1}{N}, 1 \leq i \leq N.$$

Each fault out of N faults from the list has the same probability to be selected for simulation.

In sampling with replacement:

- Any fault can be sampled multiple times
- The number of simulations can be less than the number of selected samples
- The estimated defect coverage is defined as the ratio of the detected samples to the total number of samples. The recurring samples are counted according to the number of times selected

In sampling without replacement:

- Any fault can be sampled only once
- The number of simulations equals the number of requested samples
- The estimated defect coverage is the ratio of detected fault samples to the total number of requested samples

Confidence interval can be evaluated based on the estimated detection coverage for uniform random sampling using `spectre_ddmrpt` or `spectre_fsrpt`.

Weighted Sorted Sampling

When the fault list includes weighting values, Spectre provides the method to select for simulation only a subset of faults that have the largest weighted likelihood. This approach allows to reduce the simulation time to estimate the defect coverage by excluding from injection the faults that have relatively small weighted likelihood or undefined weight.

The fault list with weight can be generated as described in [Weighted Random Sampling](#), that is, by using `weight_expr` and `weight_factor` parameters in `info analysis`, or by applying the fault collapsing option.

The parameter `faultsamplemethod=weightsorted` in `sweep` or `tran` statement enables the weight sorted sampling. Spectre chooses the requested number of samples with the

largest weighted likelihood for the fault simulation. The number of samples can be specified by `faultsamplenum` or `faultsampleratio` parameter.

The estimated defect coverage is calculated as the ratio of the sum of weighted likelihoods of detected samples to the sum of weighted likelihood of all the selected samples.

Since the weight sorted sampling is not random, confidence interval estimation is not supported for this method.

Confidence Interval Sampling

Spectre supports two approaches for confidence interval calculation with the given confidence level α : Clopper-Pearson formula and Wald formula.

After the fault simulation is complete, confidence interval can be calculated by using postprocessing utilities `spectre_ddmrpt` or `spectre_fs rpt`.

The formula for the Clopper-Pearson exact method forms the confidence interval by using the relationship between binominal distribution and beta distribution.

$$\left[B\left(\frac{\alpha}{2}; n_d, n - n_d + 1\right), B\left(1 - \frac{\alpha}{2}; n_d + 1, n - n_d\right) \right]$$

where, $B(\cdot; a, b)$ is the beta distribution quantile function with the shape parameters a, b that depend on the number of the total n and the detected n_d fault samples. When the proportion or the estimated coverage depends on weighted likelihood, the shape parameters are modified accordingly.

$$\left[B\left(\frac{\alpha}{2}; n w_d, n(w_n - w_d) + 1\right), B\left(1 - \frac{\alpha}{2}; n w_d + 1, n(w_n - w_d)\right) \right]$$

The choice of Wald formula in Spectre includes the finite population correction and the continuity correction for a small sample size.

$$p \pm \left(z \sqrt{\frac{p(1-p)}{n-1} (1 - w_n) + 1/2n} \right)$$

where,

■ z is $\left(1 - \frac{\alpha}{2}\right)$

percentile of the standard normal distribution for the requested confidence level α .

- The likelihood of simulated samples is

$$w_n = \sum_{k=1}^n w_k$$

- The proportion of the likelihood of all detected samples to all simulated is

$$p = \frac{\sum_{k=1}^{n_d} w_k}{w_n}$$

- $\sum_{k=1}^N w_k = 1$

when the weighted likelihood is not considered, then $w_n = n/N$, and $p = n_d/n$.

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Benchmark Test of Fault Sampling, Simulation, and Confidence Interval Estimation

The following table represents the experimental results of Spectre random sampling techniques and can be used as a guidance to choose an appropriate approach for fault injection and simulation for designs with a large defect count.

Number of samples, %		10				20				30				95			
Random sampling method		weighted		uniform		weighted		uniform		weighted		uniform		weighted		uniform	
Reference coverage for 100 faults, %		91.68		73.0		91.68		73.0		91.68		73.0		91.68		73.0	
Sampling with replacement		yes	no	yes	no	yes	no	yes	no	yes	no	yes	no	yes	no	yes	no
Number of detected samples		10	10	8	8	20	19	17	16	29	28	23	23	87	70	74	69
Weighted likelihood of detected samples		0.414	0.376	-	-	0.849	0.637	-	-	1.162	0.811	-	-	3.264	0.916	-	-
Weighted likelihood of all samples		0.414	0.376	-	-	0.849	0.675	-	-	1.2	0.862	-	-	3.422	0.999	-	-
Estimated defect coverage, %		100.0	100.0	80.00	80.00	100.0	94.38	85.00	80.00	96.84	94.13	76.67	76.67	95.38	91.68	77.89	72.63
Clopper-Pearson Formula	95% Lower limit	41.06	37.54	44.39	44.39	80.48	67.53	62.11	56.34	84.88	77.34	57.72	57.72	92.49	84.21	68.22	62.52
	95% Upper limit	100.0	100.0	97.48	97.48	100.0	99.95	96.79	94.27	99.88	99.56	90.07	90.07	97.39	96.36	85.77	81.28
	99% Lower limit	27.85	24.48	35.18	35.18	73.21	58.83	55.05	49.34	80.47	71.51	52.01	52.01	91.50	81.65	65.15	59.38
	99% Upper limit	100.0	100.0	98.91	98.91	100.0	99.99	98.24	96.42	99.97	99.85	92.71	92.71	97.85	97.29	87.75	83.54
Wald formula	95% Lower limit	95.00	95.00	67.12	50.21	97.50	85.98	77.66	61.41	92.05	89.29	70.36	62.12	92.30	91.07	72.96	70.09
	95% Upper limit	100.0	100.0	92.88	100.0	100.0	100.0	92.34	98.59	100.0	98.97	82.97	91.21	98.45	92.30	82.83	75.17
	99% Lower limit	95.00	95.00	64.64	42.42	97.50	84.13	76.14	56.36	91.07	88.29	68.90	58.07	91.50	91.04	71.58	69.46
	99% Upper limit	100.0	100.0	95.36	100.0	100.0	100.0	93.86	100.0	100.0	99.97	84.43	95.26	99.25	92.33	84.21	75.81
TFA (timezero) elapsed time, s	Reference 100 faults	155.5															
	Sampled faults	11.8	13.7	17.7	18.8	16.8	23.8	31.8	34.9	23.8	36.7	44.9	47.7	43.4	145.8	103.7	147.7
DFA elapsed time, s	Reference 100 faults	188.7															
	Sampled faults	14.2	17	20.1	21.9	22.1	30.8	36.5	40.1	31.1	46.2	52.7	56.8	55.1	176.4	124.9	178.1

In this example, the fault list consists of the bridges between the gate, drain, and source pins of MOS transistors (`faultdev=bsim4 faultterminals=[g d s]`), and the opens for the gate and drain terminals of the same devices (`faultdev=bsim4 faultterminals=[g d]`) from the `pll_reg_bg` cell of the design under test. After

excluding one short that is related to the output signal and ground node, the defect universe includes 58 bridges and 42 opens. For both, bridge and open faults, the gate area was specified as a weighting function, `weight_expr=w*1`. Spectre asserts were used to specify the detection limits. Also, the `faultautostop=all` option was enabled during fault injection and simulation to auto-stop transient analysis once the injected fault is detected by the asserts.

When we analyze all faults, the reference defect coverage for this test is 91.65% with fault weighting and 73% without fault weighting.

To begin, a fault count of 100 was selected to perform simulation in a short time and to trace the estimated values in the cases when sample representation is very low. It was then incrementally increased, and then close to the total fault amount was used. Table 3 includes data for the number of samples 10%, 20%, 30%, and 95% of total (for example, `faultsampleratio=10`). Each sampling choice was simulated with two methods `faultsamplemethod=randomweighted`, `faultsamplemethod=randomuniform`. These are shown in the `weighted` and `uniform` columns of the table. Each sampling method was performed with and without replacement of samples during the random sampling process. The `faultsamplerreplace=yes|no` setting is shown in the `yes` and `no` columns in the table.

The estimated defect coverage is evaluated by `spectre_ddmrpt`. In case of uniform sampling, it is calculated as the ratio of detected samples to the number of all samples. In case of random weighted sampling, it is calculated as the ratio of the sum of weighted likelihood of detected samples to the sum of weighted likelihoods of all selected samples. The data in the table includes all these values for each sample choice. As expected, the estimated coverage is improved with increasing number of samples. Sampling without replacement has some advantage in accuracy.

For the estimation of confidence interval, `spectre_ddmrpt` is used with the `-cl` option to specify the required confidence level (for example, `-cl 99`), and `-cr CP`, or `-cr W` to specify the choice of the preferred formula. As expected, a higher confidence level makes the confidence interval wider. Increasing the sample size reduces the interval. As a rule, sampling with replacement reports a smaller confidence interval.

The last four rows in the table 3 include the fault injection and simulation performance for Spectre APS. Each number represents the elapsed time to perform the transient analysis simulation for each set of samples, and the related random sampling specifications. The simulation was run with two methods, TFA with `faultmethod=timezero` and DFA. The reference simulation time for all 100 faults is shown for both methods. Sampling with replacement has a considerable advantage in terms of the simulation time in all cases.

In general, as the sample number becomes closer to the total fault number, more precise confidence intervals and estimated defect coverage are expected. When the combination of

`randomweighted` and `faultsamplereplaced=yes` is used (Spectre default settings), you can expect more accurate confidence interval bounds as well as better performance. In comparison to this, using `faultsamplereplaced=no` predicts more accurate estimated defect coverage. In addition, fault sampling and simulation in TFA requires less time than in DFA.

Defect Detection Using Weighted Likelihood

With weighting function and weighted likelihood information, Spectre calculates the weighted likelihood for each fault based on its ratio to the total weights within the block. The value of weighted likelihood is saved in fault table file. The weighted likelihood is used to compute the defect coverage in the generation of both detection matrix (with `spectre_ddmrpt`) and functional safety reports (with `spectre_fsrpt`), as well as fault sampling selection.

The following example shows the weighted likelihood calculation. Let us consider the fault list which consists of two fault blocks:

```
block1 faults weight_factor=0.9 weight_expr=w*1 {
    bridge {
        block1_bridge_1 (0 out) r=200 dev=I0.MN01
        block1_bridge_2 (0 pd) r=200 dev=I0.MN02
        block1_bridge_3 (0 xpd) r=200 dev=I0.MN03
    }
}
block2 faults weight_factor=0.1 weight_expr=w {
    bridge {
        block2_bridge_1 (vdda I0.net69) r=200 dev=I0.XR2
        block2_bridge_2 (vdda I0.net51) r=200 dev=I0.XR1
    }
}
```

The total weight is the sum of weight for all faults in each block multiplied by its weight factor. For example:

```
total_weight = w_block1*0.9 + w_block2*0.1
```

where `w_block1` and `w_block2` are calculated as:

```
w_block1 = I0.MN01.w*I0.MN01.1 + I0.MN02.w*I0.MN02.1 + I0.MN03.w*I0.MN03.1
w_block2 = I0.XR1.w+ I0.XR2.w
```

The weighted likelihood for each fault is calculated by taking the `weight_factor` normalized to total weight factor into account for each fault block:

```
W_f1 = (0.9*I0.MN01.area)/total_weight
W_f2 = (0.9*I0.MN02.area)/total_weight
```

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```
W_f3 = (0.9*I0.MN03.area)/total_weight
W_f4 = (0.1*I0.XR1.w)/total_weight
W_f5 = (0.1*I0.XR2.w)/total_weight
```

The weighted likelihood is calculated for each fault and saved as the parameter `weight` in the table file which is generated during fault simulation, as shown below.

```
title: Fault analysis
analysis: transient
weight_expr : w*I, w
total faults: 32
simulated: 32

parameters:nominal=0
Test_Points  IDDOUT  P2PVAL  OFF  DELAY  resistance  iterations
1.000000E-06  0.000E+00  0.000E+00  1.619E+00  0.000E+00  1.602e+38  2
1.500000E-06  0.000E+00  0.000E+00  1.619E+00  0.000E+00  1.602e+38  2
2.300000E-06  1.119E-08  1.527E-01  1.619E+00  0.000E+00  1.602e+38  2

1: block1_bridge_1 ( 0 out ) r=200 weight=0.0656023 dev=I0.MN01
1.000000E-06  0.000E+00  0.000E+00  -1.650E+00  0.000E+00  200  2
1.500000E-06  0.000E+00  0.000E+00  -1.650E+00  0.000E+00  200  2
2.300000E-06  1.339E-08  1.830E-04  -1.650E+00  0.000E+00  200  2

2: block1_bridge_2 ( 0 pd ) r=200 weight=0.000485782 dev=I0.MN02
1.000000E-06  0.000E+00  0.000E+00  1.620E+00  0.000E+00  200  2
1.500000E-06  0.000E+00  0.000E+00  1.620E+00  0.000E+00  200  2
2.300000E-06  1.119E-08  1.527E-01  1.620E+00  0.000E+00  200  2

3: block1_bridge_3 ( 0 xpd ) r=200 weight=0.000485782 dev=I0.MN03
1.000000E-06  0.000E+00  0.000E+00  1.620E+00  0.000E+00  200  2
1.500000E-06  0.000E+00  0.000E+00  1.620E+00  0.000E+00  200  2
2.300000E-06  1.120E-08  1.527E-01  1.620E+00  0.000E+00  200  2
... ..
31: block2_bridge_1 ( vdda I0.net69 ) r=200 weight=0.0533333 dev=I0.XR2
1.000000E-06  0.000E+00  0.000E+00  1.620E+00  0.000E+00  200  2
1.500000E-06  0.000E+00  0.000E+00  1.620E+00  0.000E+00  200  2
2.300000E-06  1.120E-08  1.527E-01  1.620E+00  0.000E+00  200  2

32: block2_bridge_2 ( vdda I0.net51 ) r=200 weight=0.0466667 dev=I0.XR1
1.000000E-06  0.000E+00  0.000E+00  1.620E+00  0.000E+00  200  2
1.500000E-06  0.000E+00  0.000E+00  1.620E+00  0.000E+00  200  2
2.300000E-06  1.119E-08  1.527E-01  1.620E+00  0.000E+00  200  2
```

Weighting function

Total simulated faults

Weighted likelihood

Instance's w and I for calculating weighted likelihood

Instance's w for calculating weighted likelihood

Fault Sampling Output and Confidence Interval Calculation

When fault simulation is performed using random sampling, the fault table file contains the sampling information that includes the sampling method, the total fault number, the number of faults being sampled and simulated.

For the randomweighted and randomuniform sampling methods, the samples can be selected either with or without replacement. When `faultsampleresplace=yes` is set, then any particular fault can be selected more than once. As a result, the simulated fault number may be less than the number of samples. If a fault was sampled `n` times, then its statement contains `sample=n` parameter in the table file. `sample=1` is default value, and usually not specified in the table file.

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Both sampling methods support the confidence interval calculation by using `spectre_ddmrpt` or `spectre_fs rpt`. Both `spectre_ddmrpt` and `spectre_fs rpt` allow you to calculate confidence interval when the random sampling-based simulation is finished, or the fault table file is available.

```

title: Fault analysis
analysis: transient
weight_expr : w*1
total faults: 30
sampled: 20
simulated: 10

```

faultsamplenum=20

Total simulated faults

```

parameters:nominal=0
Test_Points  IDDOUT  P2PVAL  OFF  DELAY  resistance  iterations
1.000000E-06  0.000E+00  0.000E+00  3.312E-04  5.566E-08  1.602e+38  2
1.500000E-06  0.000E+00  0.000E+00  3.312E-04  5.566E-08  1.602e+38  2
2.300000E-06  -9.426E-08  9.218E-01  3.312E-04  5.566E-08  1.602e+38  2

1: OPAMP1_bsim_bridge_1 ( 0 out ) r=200 weight=0.0728914 dev=X1.mn001 sample=4
1.000000E-06  0.000E+00  0.000E+00  -1.637E+00  0.000E+00  200  2
1.500000E-06  0.000E+00  0.000E+00  -1.637E+00  0.000E+00  200  2
2.300000E-06  -9.379E-08  2.285E-05  -1.637E+00  0.000E+00  200  2

2: OPAMP1_bsim_bridge_4 ( out vdda ) r=200 weight=0.116626 dev=X1.mp001
1.000000E-06  0.000E+00  0.000E+00  9.798E-01  0.000E+00  200  2
1.500000E-06  0.000E+00  0.000E+00  9.798E-01  0.000E+00  200  2
2.300000E-06  -1.355E-06  1.826E-02  9.798E-01  0.000E+00  200  2

... ..

7: OPAMP1_bsim_bridge_17 ( out X1.net158 ) r=200 weight=0.116626 dev=X1.mp001 sample=3
1.000000E-06  0.000E+00  0.000E+00  1.462E-03  5.613E-08  200  2
1.500000E-06  0.000E+00  0.000E+00  1.462E-03  5.613E-08  200  2
2.300000E-06  -2.557E-06  8.819E-01  1.462E-03  5.613E-08  200  2

8: OPAMP1_bsim_bridge_22 ( vdda X1.net158 ) r=200 weight=0.160901 dev=X1.mppd1 sample=6
1.000000E-06  0.000E+00  0.000E+00  -5.634E-01  0.000E+00  200  2
1.500000E-06  0.000E+00  0.000E+00  -5.634E-01  0.000E+00  200  2
2.300000E-06  -6.076E-08  1.542E-01  -5.634E-01  0.000E+00  200  2

```

Sampled for multiple times

You can choose either Clopper-Pearson or Wald formula using parameter `--cr (--confrule) CP|W`.

Default confidence level is 95%. The option `-cl` allows to customize the value.

The following command generates the fault detection report for all signals at `faulttime=2.3e-6`:

```

.../bin/spectre_ddmrpt mytest.tranFault.table -t 2.3e-6 -cl 97 -o
report_ddmrpt_CI.txt

```

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The confidence interval values are saved for each signal by using the default Clopper-Pearson formula for confidence level 97%.

Time Points: 2.3e-06
 Signals: IDDOUT, P2PVAL, OFF, DELAY
 Detection absolute tolerance: 1e-06
 Total Defects: 30
 Sampled: 20
 Simulated: 10

Detection Matrix:

	2.3e-06/IDDOUT	2.3e-06/P2PVAL	2.3e-06/OFF	2.3e-06/DELAY	Total
OPAMP1_bsim_bridge_1	G	D	D	G	D
OPAMP1_bsim_bridge_4	D	D	D	G	D
OPAMP1_bsim_bridge_7	G	D	D	G	D
OPAMP1_bsim_bridge_8	G	D	D	G	D
OPAMP1_bsim_bridge_9	G	D	D	G	D
OPAMP1_bsim_bridge_15	D	G	G	G	D
OPAMP1_bsim_bridge_17	D	G	D	G	D
OPAMP1_bsim_bridge_22	G	D	D	G	D
OPAMP1_bsim_bridge_27	G	D	D	G	D
OPAMP1_bsim_bridge_28	G	G	G	G	G
Estimated Coverage	25.00%	75.00%	90.00%	0.00%	95.00%
97% Lower Limit	7.61%	48.54%	65.95%	0.00%	72.85%
97% Upper Limit	51.46%	92.39%	99.06%	18.94%	99.92%

Under some circumstances, you would find the fault number being simulated is inconsistent to what you expect. The table given below shows how Spectre performs the fault simulation with the fault list is provided.

Status of faultcollapse	Simulation Behavior
sim default	removes identical faults (not based on weight value); open devices get extended; the sample fault list contains the weighting according to the fault list generation rule
sim faultcollapse=no	removes identical faults (not based on weight value); open devices get extended; the sample fault list contains the weighting according to the fault list generation rule
sim faultcollapse=yes	removes identical faults (not based on weight value); open devices get extended; equivalent faults get collapsed

Applying Fault Weighting and Sampling in Fault Simulation

When generating fault list with info analysis, the weighting function can be specified as an expression for each fault and weight factor with constant value for each fault group.

```
g1_b info what=bridges where=file file=faultlist.scs faultdev=[bsim4]  
faultterminals=[d g s] inst=[XI79] weight_expr=w*1 weight_factor=0.5
```

```
g2_g info what=opens where=file file=faultlist.scs faultdev=[bsim4]  
faultterminals=[g] inst=[XI79] weight_expr=w*1 weight_factor=0.3
```

```
g2_ds info what=opens where=file file=faultlist.scs faultdev=[bsim4]  
faultterminals=[d s] inst=[XI79] weight_expr=w*1 weight_factor=0.2
```

Alternatively, you can manually add the weighting value to each fault.

```
g1_b faults weight_factor=0.5 {  
  bridge {  
    g1_b_bridge_1 ( VDDa! VSS! ) r=100 dev=XI79.M78 // nana s d  
    g1_b_bridge_2 ( VDDa! net033 ) r=100 dev=XI79.M83 // pana s g  
    ...  
  }  
}  
g2_g faults weight_factor=0.3 {  
  open {  
    g2_g_open_1 ( VSS! ) r=1e+09 { XI79.M77:g } // nana g  
    g2_g_open_2 ( VSS! ) r=1e+09 { XI79.M78:g } // nana g  
    ...  
  }  
}  
g3_ds faults weight_factor=0.2 {  
  open {  
    g3_ds_open_1 ( VDDa! ) r=1e+09 { XI79.M27:s } // pana s  
    g3_ds_open_2 ( VDDa! ) r=1e+09 { XI79.M50:s } // pana s  
    ...  
  }  
}
```


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When fault simulation finishes and the fault table is generated, the fault results are saved in fault table file where each fault shows 'weight=#' parameter with weighted likelihood value. The weighted likelihood is normalized weight values according to all defects simulated.

```
1: g1_b_bridge_1 ( VDDa! VSS! ) r=100 weight=0.00626566 dev=XI79.M78
1.000000E-02 0.000E+00 0.000E+00 6.693E-06 0 100 2
5.000000E-02 0.000E+00 0.000E+00 1.400E+00 0 100 2
1.000000E-01 0.000E+00 0.000E+00 1.400E+00 0 100 2
...
106: g2_g_open_1 ( VSS! ) r=1e+09 weight=0.0037594 { XI79.M77:g }
1.000000E-02 0.000E+00 0.000E+00 6.695E-06 0 1e+09 2
5.000000E-02 0.000E+00 0.000E+00 1.400E+00 0 1e+09 2
1.000000E-01 0.000E+00 0.000E+00 1.400E+00 0 1e+09 2
...
145: g3_ds_open_1 ( VDDa! ) r=1e+09 weight=0.00250627 { XI79.M27:s }
1.000000E-02 0.000E+00 0.000E+00 6.695E-06 0 1e+09 3
5.000000E-02 0.000E+00 0.000E+00 1.400E+00 0 1e+09 2
1.000000E-01 0.000E+00 0.000E+00 1.400E+00 0 1e+09 2
...
```

The defect coverage can be calculated based on the weighting of detected faults with spectre_ddmrpt post-processing.

```
Time Points: 0.01, 0.05, 0.1
Signals: bg
Detection absolute tolerance: 1e-06
Total Defects: 222
Total defect coverage: 44.59%
Total weighted defect coverage: 52.76%
```

Detection Matrix:

	0.01/bg	0.05/bg	0.1/bg	Total	Likelihood
Weighted Coverage	17.29%	44.24%	44.24%	52.76%	1
g1_b_bridge_1	G	G	G	G	0.00626566
...	G	G	G	G	0.00626566
g2_g_open_1	G	G	G	G	0.0037594
...	G	G	G	G	0.0037594
g3_ds_open_1	G	G	G	G	0.00250627
...	G	G	G	G	0.00250627
g3_ds_open_3	G	G	G	G	0.00250627

The alternative usage is to enable the auto-stop of fault simulation on the detection criteria set by user. Spectre stops the entire fault simulation when the defect coverage 50% is achieved in the example below. The given confidence level faultconfidlevel can be further specified along with the detection ratio when fault sample method of randomuniform or randomweighted is chosen. Please refer to chapter 4.8.2 for the detail descriptions.

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```
DFA sweep faults=[*] faultsamplemethd=randomweighted faultdetratio=50
faultconfidlevel=95 faultseed=12345
```

```
Time Points: 0.01, 0.05, 0.1
Signals: bg
Detection absolute tolerance: 1e-06
Total Defects: 222
Sampled: 222
Simulated: 137
Sampling method: random weighted with replacement
Estimated weighted coverage: 57.66%
```

Detection Matrix:

	0.01/bg	0.05/bg	0.1/bg	Total	Likelihood
Weighted Coverage	22.97%	44.59%	44.59%	57.66%	0.71
95% Lower Limit	17.61%	37.94%	37.94%	50.87%	-
95% Upper Limit	29.07%	51.39%	51.39%	64.24%	-
g1_b_bridge_1	G	G	G	G	0.00626566
...	G	G	G	G	0.00626566

The same setting can be applied to transient statement for TFA simulation.

Assert Checking

Assert violation can be used as a fault detection technique by specifying the boundaries. A fault is detected when an assert violation is triggered. To distinguish the checking of fault analysis from the regular `assert` check, you can add the `safecheck` parameter in the `assert` statement which is used in post-processing of assert violations to generate the functional safety report (see [Functional Safety Report Based on Assert Violations](#)).

```
safecheck=[ none | func | check ]
```

`safecheck=func` defines an assert that detects violation in the functional module of the design. `safecheck=check` defines an assert that detects violation in the diagnostic module (checker) of the design. The violations triggered by `safecheck=func` show the safety status (Safe or Dangerous), while the violations triggered by `safecheck=check` indicate the detection status (Detected or Undetected) in the functional safety report. A combination of both types represents the complete functional safety report for a given design. For fault defect detection matrix, defining `safecheck=check` is sufficient.

The following table lists the built-in functions that are supported by assert checking for fault analysis:

<code>abs</code>	<code>asin</code>	<code>cos</code>	<code>I</code>
<code>ln</code>	<code>mod</code>	<code>round</code>	<code>sqrt</code>
<code>acos</code>	<code>asinh</code>	<code>acosh</code>	<code>iinteg</code>
<code>log10</code>	<code>pow</code>	<code>settlingtime</code>	<code>tan</code>
<code>argmax</code>	<code>atan</code>	<code>exp</code>	<code>im</code>
<code>mag</code>	<code>re</code>	<code>sign</code>	<code>tanh</code>
<code>argmin</code>	<code>atanh</code>	<code>floor</code>	<code>int</code>
<code>max</code>	<code>real</code>	<code>sin</code>	<code>trim</code>
<code>acosh</code>	<code>avg</code>	<code>freq</code>	<code>integ</code>
<code>min</code>	<code>rms</code>	<code>sinh</code>	<code>V</code>

Enabling Asserts for Fault Simulation

Regular asserts are used extensively to check the device operation during the DC, transient, and AC frequency domain analyses. Usually, asserts are defined in the model library to check the safe operation area (SOA) for various devices. The simulation slows down because of the large number of asserts being enabled. Therefore, in fault simulation, asserts are enabled for

fault detection only in the `checklimit` statement using the `enable=[fault_assert]` option, while the regular asserts are disabled to avoid long simulation time.

Note: The enabled checks are applied to all subsequent analyses till the next `checklimit` statement is encountered. Therefore, the `checklimit` statement should be added prior to the analysis where the asserts are applied; for example, `sweep` or `tran` analysis.

Verilog-A Asserts

In addition to the device-based asserts, Spectre also supports Verilog-A asserts that can be used for fault detection and functional safety analysis.

Following is the syntax to specify an assert in Verilog-A:

```
$cds_violation(Id, Message, Data, Option);
```

Here:

- `Id` represents the name of the assert as a constant string
- `Message` represents the violation message
- `Data` represents the expression of the analog circuit
- `Option` represents the id number to indicate the type of assert; same as the `safecheck` parameter in device-based assert. Possible values are:
 - 0 (`safecheck=none`)
 - 1 (`safecheck=func`)
 - 2 (`safecheck=check`)

The example below shows how to generate an assert violation in a Verilog-A application.

```
module my_va_assert(signal1, signal2);
    inout signal1, signal2;
    electrical signal1, signal2;

    analog begin
        if( V(signal1, signal2) > 2.501 ) begin
            $cds_violation("assert1", "Input voltage exceeds 2.501!", \
                V(signal1, signal2), 2);
        end
    end
end
endmodule
```

The following statement creates an instance of Verilog-A assert, which is the same as creating a regular instance.

```
AM net1 net2 my_va_assert
```

In the functional safety report, the assert is printed as

```
AM.assert1 assert safecheck=check module=my_va_assert
```

Defining Fault Times

Fault times provide the following two functionalities:

- Faults are injected only at or prior to some given time points in transient fault analysis.
- These time points can be used to save the fault result into a table file. These time points are called fault times.

For fault simulation, you can specify the fault times using any of the following methods:

- Specify the sweeping points by using the `faultstart`, `faultstop`, and `faultstep` parameters
- Specify the discrete time points using the `faulttimes` parameter
- List the fault times in a separate file to be included in simulation
- Define the assert and specify the `faultevent` parameter

Example 1

```
faultstart=0.5m faultstop=1.0m faultstep=0.5m
```

Example 2

```
faulttimes = [0.5m 0.75m 1.0m]
```

Example 3

```
faultfile = "./file_test_points.txt"
```

Fault times in the `./file_test_points.txt` file can be defined as follows:

```
//fault time point
0.5m
0.75m
1.0m
```

Specifying Event-Triggered Fault Times

Besides the constant time points for faults to be injected, Spectre provides the flexibility where the time can be determined dynamically as the violation of asserts specified in the `faultevent` vector. The `faultevent` vector can contain one, or several event expressions, similar to Spectre event triggered analysis.

The general form of event expression is specified as follows:

`"@(basic_event, N) + delay"`

Here:

<i>basic_event</i>	Name of the assert that defines the event to be triggered.
<i>N</i>	Selector of the event. If <i>N</i> is a positive value, it means to select the <i>N</i> th occurrence of the event. If <i>N</i> is a negative value, it means to select the <i>N</i> th occurrence and the occurrence just before the <i>N</i> th occurrence of the <code>basic_event</code> . If <i>N</i> is 0, it means to select all occurrences. If <i>N</i> is not specified, it means to select the first occurrence.
<i>delay</i>	The delay time after the selected event occurrences. A positive value should be specified for <code>delay</code> .

Note: *N*=0 (that is, `"@(assert1, 0)"`) is not supported in current implementation, If you specify 0 as the value for *N*, only the first occurrence will be processed. The same basic event with different values for *N* can be specified to cover multiple occurrences.

Example

```
assert1 assert dev=M1 expr="V(d)" min=0 max=0.3
assert2 assert dev=M2 expr="V(g)" min= -0.7 max=0
tranETAttran stop=1u faultmethod=leadtime faultleadtime=100n \
annotate=status faultevent=["@(assert1)" "@(assert2, 2) + 5n"]
```

In the example above, Spectre will first perform the nominal transient simulation to collect two fault times; the first violation triggered by `assert1`, and the second assert violation issued by `assert2` with 5ns in delay. The nominal simulation will stop automatically, and the transient fault simulation will start with `faulttimes` set at event times.

You can use the `faultevent` parameter along with static fault times specified in transient analysis statement.

Stopping Fault Simulation Automatically

You can use the `faultautostop` parameter in the transient statement to stop the fault simulation automatically based on the assert violation. The `faultautostop` parameter is supported in both direct and transient fault analysis. Possible values for `faultautostop` are: `no`, `func`, `check`, `both`, and `all`.

<code>faultautostop=no</code>	Stop the fault simulation automatically when a fault is detected based on assert violation.
<code>faultautostop=func</code>	Stop the fault simulation automatically if any assert with <code>safecheck=func</code> is violated.
<code>faultautostop=check</code>	Stop the fault simulation automatically if any assert with <code>safecheck=check</code> is violated.
<code>faultautostop=both</code>	Stop the fault simulation automatically if both asserts with <code>safecheck=func</code> and <code>safecheck=check</code> are violated.
<code>faultautostop=all</code>	Stop the fault simulation automatically if any assert with <code>safecheck=func</code> or <code>safecheck=check</code> is violated.

Ensure that asserts do not get violated for the nominal transient simulation because they are the golden reference data. You can use the `faultsafecheck` parameter to terminate the fault simulation if the violation is triggered during the nominal run. The default value for the `faultsafecheck` parameter is `no`.

Stopping the Fault Simulation Automatically on Detection Coverage

You can also stop the fault simulation automatically when the required fault detection rate is achieved. The detection rate monitoring is based on the assert violations, therefore, `faultautostop` is required to be defined in the same analysis. Spectre starts the detection rate tracing with the value given to `faultdetratio` when the first `R`% of faults are injected.

`faultdevratio=R` – Stops the fault simulation automatically when the specified detection ratio is achieved, where `R` is the percentage of detected faults out of the total fault numbers.

Setting `faultdetratio=80` means that the simulation will stop when fault detection rate is 80% of the total number of faults.

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You need to specify `faultautostop=func|check|both|all` with `faultdetratio`.

Stopping the simulation automatically based on the detection rate is supported in both direct and transient fault analysis. The feature is compatible with fault sampling, the detection ratio is calculated according to number of samples specified.

You can further specify the detection ratio to be achieved with the given confidence level `faultconfidlevel` for the fault sample methods `randomuniform` or `randomweighted` only.

The following are the prerequisites to perform the autostop based on the detection coverage:

- Specify one or a few Spectre `assert` statements, or a Verilog-A `assert` with the `safecheck` parameter to trace fault detection status.
- Add `faultautostop=check|func|both|all` in transient analysis
- Add `faultdetratio=R` in the transient (TFA) statement, or sweep (DFA) analysis, where `R%` is the expected detection coverage ratio.

The following table shows the use model and the autostop criteria based on the parameters specified in the `tran` or `sweep` statement:

Options in tran/sweep analysis statement	Simulation effect when the fault list consists of N faults, and D is the number of detected faults	Note on Autostop
<code>faultdetratio=R</code>	Fault injection and simulation continues while $D/N * 100 < R$.	All N faults may be simulated if R is too high or detection limits are too strict.
<code>faultdetratio=R</code> <code>faultsampleratio=r</code> (or <code>faultsampleratio=n</code>) <code>faultsamplemethod=any</code>	$N * r / 100$ (or n) faults randomly sampled. Sample injection and simulation continues while $D * 100 / N * r < R$ (or $D / n < R$)	All sampled faults may be simulated if R is too high, or detection limits are too strict, or the number of samples is small.
<code>faultdetratio=R</code> <code>faultconfidlevel=L</code> <code>faultsamplemethod=randomweighted</code> (or <code>randomuniform</code>)	Fault sampling and simulation continues while [lower bound of current DC with confidence L] < [lower bound of DC=R with confidence L]	All N faults may be simulated if R or L is too high, or detection limits are too strict.
<code>faultdetratio=R</code> <code>faultconfidlevel=L</code> <code>faultsampleratio=r</code> (or <code>faultsampleratio=n</code>) <code>faultsamplemethod=randomweighted</code> (or <code>randomuniform</code>)	Fault sampling and simulation continues while [lower bound of current DC with confidence L] < [lower bound of DC=R with confidence L], or, the number of samples reach $N * r / 100$ (or n), whichever happens first.	No more than $N * r / 100$ (or n) faults will be sampled and simulated if the autostop condition is not satisfied.

Fault simulation in the job distribution mode is compatible with this feature while the `faultdetratio` is calculated for each process locally.

Exiting Fault Analysis Based on Maximum Time Limit

When fault simulation takes much longer than the nominal simulation time, you can use `faultlimtime` parameter to set the absolute time (in hours) to exit the current fault simulation. There is no default value. The following message is generated in the log file when the elapsed time is reached during slow fault simulation.

```
Simulation of fault bridge_1 achieved limit 0.1 h. Analysis 'myDirect-001_myfault'
was terminated at 21.822 us.
```

```
(Remove 'faultlimtime' parameter to avoid early termination.)
```

```
Number of accepted tran steps =                241
```

Exiting Fault Analysis Because of Convergence Difficulty

A fault injection into the circuit may cause circuit instability, problems with convergence, or trigger oscillations that can result in more time steps and longer simulation time. With `faultlimsteps=yes` as default, Spectre monitors the number of time steps taken in fault analysis and automatically exits the simulation when the step count becomes huge in comparison to the nominal simulation. The following message is displayed in the log file when a fault simulation is exited. The iterations saved in table file are set to 0 to indicate early termination.

```
Simulation of fault bridge_22 is too slow. Analysis 'directfault-022_tran' was
terminated at 1.92212 ms.
```

```
(Specify 'faultlimsteps=no' to avoid early termination.)
```

```
Number of accepted tran steps =                62594
```

```
Notice from spectre during transient analysis `directfault-022_tran', during Sweep
analysis `directfault'.
```

```
Trapezoidal ringing is detected during tran analysis.
```

```
Please use method=trap for better results and performance.
```

To prevent early termination, specify `faultlimsteps=no` in the `tran` statement.

The maximum steps allowed to perform one fault simulation can be explicitly set with the parameter `faultmaxsteps=N`. The simulation will be terminated if it does not complete earlier than the specified step count.

```
swp-001_dfa: time = 51.17 us      (2.56 %), step = 2.864 us      (143 m%)
swp-001_dfa: time = 171.3 us     (8.56 %), step = 40 us         (2 %)
swp-001_dfa: time = 251.3 us     (12.6 %), step = 40 us         (2 %)
```

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Simulation of fault func_s_bridge_30 achieved limit 1000 steps. Analysis 'swp-001_dfa' was terminated at 1000 step.

(Remove 'faultmaxsteps' parameter to avoid early termination.)

Files Generated for Fault Simulation

Fault Table File

The fault simulation results are saved in a table file where solutions at the fault times are grouped for each fault. The saving is limited to the signals specified in the `save` statement. The name of the table file is `netlistname.tranname.table`.

The following is a sample table file:

title: Fault analysis analysis: transient undefined: 1.60000E+38								
parameters:nominal=0								
Test_Points	dd	d	gg	g	s	resistance	iterations	
5.000000E-04	5.000E+00		4.450E+00	3.125E+00	1.562E+00	5.495E-02	1.602e+38	2
7.500000E-03	5.000E+00		4.874E+00	1.875E+00	9.375E-01	1.263E-02	1.602e+38	2
1: bridge_1 (g 0) r=10								
5.000000E-04	5.000E+00		5.000E+00	3.125E+00	3.064E-02	1.072E-09	10	2
7.500000E-03	5.000E+00		5.000E+00	1.875E+00	1.838E-02	7.194E-10	10	2
2: bridge_2 (dd 0) r=10								
5.000000E-04	5.000E+00		4.450E+00	3.125E+00	1.562E+00	5.495E-02	10	2
7.500000E-03	5.000E+00		4.874E+00	1.875E+00	9.375E-01	1.263E-02	10	2
3: bridge_3 (d 0) r=10								
5.000000E-04	5.000E+00		4.901E-02	3.125E+00	1.562E+00	4.953E-03	10	2
7.500000E-03	5.000E+00		4.926E-02	1.875E+00	9.375E-01	2.498E-03	10	2
4: short_1 (g 0) r=100								
5.000000E-04	5.000E+00		5.000E+00	3.125E+00	2.604E-01	9.802E-07		
7.500000E-03	5.000E+00		5.000E+00	1.875E+00	1.563E-01	4.275E-08		
5: short_2 (dd 0) r=100								
5.000000E-04	5.000E+00		4.450E+00	3.125E+00	1.562E+00	5.495E-02		
7.500000E-03	5.000E+00		4.874E+00	1.875E+00	9.375E-01	1.263E-02		
6: short_3 (d 0) r=100								
5.000000E-04	5.000E+00		4.227E-01	3.125E+00	1.562E+00	3.500E-02	100	2
7.500000E-03	5.000E+00		4.445E-01	1.875E+00	9.375E-01	1.105E-02	100	2
7: open_1 (d) r=1e+09 { Mn:1 }								
5.000000E-04	5.000E+00		5.000E+00	3.125E+00	1.562E+00	5.589E-07	1e+09	2
7.500000E-03	5.000E+00		5.000E+00	1.875E+00	9.375E-01	4.446E-07	1e+09	2
8: open_2 (g) r=1e+09 { Mn:2 }								
5.000000E-04	5.000E+00		4.729E+00	3.125E+00	1.562E+00	2.705E-02	1e+09	2
7.500000E-03	5.000E+00		4.637E+00	1.875E+00	9.375E-01	3.627E-02	1e+09	2
9: open_3 (g) r=1e+09 { R3:2 }								
5.000000E-04	5.000E+00		5.000E+00	3.125E+00	3.125E-06	4.324E-10	1e+09	2
7.500000E-03	5.000E+00		5.000E+00	1.875E+00	1.875E-06	4.324E-10	1e+09	2

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Note: `iterations=0` or `iterations=1` has a special meaning in the table. If a fault simulation fails to converge or is terminated by Spectre due to slow simulation with `faultlimsteps=yes`, the value of iterations is set to 0. The value 1 indicates that the fault simulation has been stopped automatically.

When no fault time point is specified for fault simulation, the only time point for fault result saved is the transient stop time, as shown in the table below.

2: bridge_2 (dd 0) r=10						
1.200000E-02	0.000E+00	6.753E-21	0.000E+00	7.193E-28	-6.753E-22	10
3: bridge_3 (d 0) r=10						
1.200000E-02	0.000E+00	1.733E-25	0.000E+00	1.034E-22	-1.753E-24	10
4: open_1 (d) r=1e+09						
1.200000E-02	0.000E+00	3.604E-16	0.000E+00	-2.076E-16	5.350E-18	1e+9

Assert Violation Database

If asserts are defined in the netlist for fault detection, the assert violations, by default, are saved in an SQL database. You can use the `checklimitdest=both` option to save the results in both log file and SQL database.

The assert violations are also saved in the fault table file as 0 or 1, where, 0 indicates that a fault is undetected and 1 indicates that the fault is detected.

Spectre Direct Fault Analysis

Direct fault analysis uses `sweep` to iterate over the fault list and run the nested child analyses, such as `tran`, `dc`, `ac`, and so on.

Use Model

The following is the use model for Spectre direct fault analysis:

```
DirectName sweep faults=[ * | faultblock1...] nominal=[yes|no] [faultsid=[...]]  
[faultsname=[...]] [faultsinst=[...]] faulttablefmt=[txt|bin]  
faultsamplenum=sampleNum faultsampleration=[R1 R2] faultseed=seedValue  
faultsamplemethod=faultMethod faultsamplereplace=[yes|no] faultsort=[yes|no]  
faultcollapse=[yes|no] faultduplicate=[yes|no] faultsaver=testpoints  
faultddm=filePath faultdb=filePath faultleadtime=[...]s faultmaxiters=maxIters  
analysisName tran|dc|ac  
}
```

Here:

<code>faults=[*]</code>	Specifies the fault analysis sweeps for all faults.
<code>faults=[faultsblock..]</code>	Specifies the fault analysis sweeps for the specified blocks.
<code>nominal=yes</code>	Performs nominal fault-free simulation along with fault simulation.
<code>faultsid=[...]</code>	Specifies the indexes of faults from the list to be considered during simulation.
<code>faultnames=[...]</code>	Specifies the names of the faults from the list to be considered during simulation.
<code>faultinst=[...]</code>	Specifies the list of instances to be considered during fault simulation.
<code>faulttablefmt=[txt bin]</code>	Format of the fault table file. Possible values are <code>txt</code> and <code>bin</code> .
<code>faultcollapse=no</code>	Perform bridge fault collapsing in the list before fault simulation. Possible values are <code>no</code> and <code>yes</code> .
<code>faultsamplenum</code>	Number of samples in simple random sampling of fault list during simulation.

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<code>faultsampleratio=[R1 R2]</code>	A set of two values R1 and R2 to simulate the samples between the given range. Each value is the number of random samples (in percentage) out of the total fault count in the list. <code>faultsampleratio=R</code> is equivalent to <code>faultsampleratio=[0 R]</code>. You can give two values to perform independent simulations with an increased number of samples to improve accuracy. For example, use <code>faultsampleratio=10</code> during initial campaign, then <code>faultsampleratio=[10 15]</code> in second fault injection campaign, and merge results, if needed.
<code>faultseed</code>	Optional starting seed for random number generator during fault sampling.
<code>faultsamplemethod</code>	Method to be used for fault sampling. Possible values are <code>random</code>, <code>randomweighted</code>, <code>randomuniform</code>, and <code>weightsorted</code>.
<code>faultsamplereplace=yes</code>	Perform fault sampling with sample replacement during fault analysis. Possible values are <code>no</code> and <code>yes</code>. When set to <code>no</code>, samples can get repeated. This option works only when <code>faultsamplemethod=randomweighted</code> or <code>faultsamplemethod=randomuniform</code>.
<code>faultsamples</code>	File name to save the sample fault list when <code>faultsamplemethod</code> is specified.
<code>faultdetratio</code>	Stop the fault simulation automatically when the specified detection ratio is achieved.
<code>faultconfidlevel</code>	Stop the fault simulation automatically when the specified detection ratio is achieved with the given confidence level.

`faultduplicate`

By default, duplicate faults are included in all fault lists when multiple `info` analyses are specified for fault generation. This parameter lets you choose whether or not to include duplicate faults.

Possible values are:

- `yes`: The tool performs fault simulation for all fault from the list. This is the default value.
- `no`: Identical and equivalent faults are excluded from simulation.

`faultsort`

Perform fault simulation according to the order given in the fault list. If set to `no`, random order is applied. Possible values are `no` and `yes`. The default value is `yes`.

You can use the `savadatainseparatedir` parameter with possible values of `no` (default), `yes`, and `name` to save the results in separate directories. The directory is named as `SAFE_separate/<dirNumber>/mytran.tran.tran` where `<dirNumber>` corresponds to the sweep index when the `savadatainseparatedir=yes`, and fault name when `savadatainseparatedir=name`.

Direct Fault Simulation for Transient Analysis

The following is the syntax for direct fault simulation for transient analysis.

```
DirectName sweep faults=[ * | faultblock1... ] nominal=[yes|no] [faultsid=[
...]] [faultsname=[...]] [faultsinst=[...]] {

    TranName tran stop=10u step=1p

}
```

The following is an example of running the transient simulation for all faults blocks including the fault-free simulation before the direct fault analysis starts.

```
Directfault sweep faults=[*] nominal=yes {
    tran1 tran start=0 stop=3e-3 annotate=status
}
```

The following example shows that only second, fourth, fifth, sixth, seventh, and eighth faults are selected to run direct fault analysis.

```
Selectfault sweep faults=[*] faultsid=[2 range(4,8)] {
```

```
tran1 tran start=0 stop=3e-3 annotate=status
}
```

Direct Fault Simulation for DC Analysis

The following is an example of direct fault simulation for DC analysis:

```
DirectName sweep faults=[ * | faultblock1...] nominal=[yes|no][faultsid=[
...]][faultsname=[...]][faultsinst=[...]]
{
    DCName dc
}
```

Note: For DC analysis, direct fault analysis supports only one data point DC simulation; sweeping for `dev`, `mod`, or `param` is not supported.

Direct Fault Simulation for Other Analyses

For other analyses, such as AC analysis, Spectre can perform simulation, but does not support post-processing for functional safety report.

```
DirectName sweep faults=[ * | faultblock1...] nominal=[yes|no][faultsid=[
...]][faultsname=[...]][faultsinst=[...]]
{
    ACName ac start=1e3 stop=1e9
}
```

Functional Safety Report Based on Assert Violations

When a fault simulation is performed, a functional safety report is generated based on the result of assert violation that contains important information for analog fault test. Spectre provides the capability to measure the functional safety of the design using single-point fault metric (SPFM) and latent fault metric (LFM).

In the functional safety application, a design includes two modules, a functional module and a safety mechanism module. The `safecheck=func` parameter is used to track the functional module while `safecheck=check` is used for checking the safety mechanism module. Both `safecheck=func` and `safecheck=check` are mandatory to generate the functional safety report.

Spectre contains an executable file named `spectre_fsrpt` that is designed to post-process the log files and the assert violations when fault simulation is complete.

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The functional safety report consists of safety report summary, detection summary, list of observation points, and diagnostic and detection detail matrix. If `safecheck=check` is specified, the column `Detection` is generated. If both `safecheck=func` and `safecheck=check` are specified, the column `Safety` is generated. The last section displays the coverage summary in percentage, as shown in the following figure.

```

Failure Mode ID: 000
Failure Mode: SPF

Diagnostic coverage : 50.00%
Fault tolerance : 83.33%
Coverage reported by checker : 66.67%
Faults that are safe : 66.67%

Safe_undetected : 16.67%
Safe_detected : 50.00%
Dangerous_undetected : 16.67%
Dangerous_detected : 16.67%
Not_Classified : 0.00%

Note: Metrics calculated above are based on the user defined fault list which might or might not be the fault universe.

Observation points:
DEV_BIAS assert dev=Mn expr=V(g,s) min=-4e-08 max=2.501 message=Device bias limit exceeded | (violated)

Detection points:
LOAD_CAP assert expr=v(d) min=-2.2e-07 max=5 duration=1e-06 message=Load Cap limit exceeded | (violated)
LOAD_CAP2 assert expr=v(g,g) min=-8e-08 max=2.501 message=Load Cap2 limit exceeded | (violated)

Fault Detection Matrix:

```

Fault Idx	F:DEV_BIAS	C:LOAD_CAP	C:LOAD_CAP2	Safety	Fault Info
1	G	G	G	Safe_undetected	fault_bridges_bridge_1 (0 dd) r=10
2	G	G	U (+2.45 / 2.5 = +97.96%)	Safe_detected	fault_bridges_bridge_6 (0 g) r=10
3	L (-1.18e-08 / -4e-08 = -29.49%)	G	G	Dangerous_undetected	fault_bridges_bridge_7 (0 d) r=10
4	G	G	U (+2.5 / 2.5 = +99.92%)	Safe_detected	fault_opens_open_7 (g) r=1e+09 { R3:2 }
5	G	G	L (-7.82e-06 / -8e-08 = -9.78%)	Safe_detected	fault_opens_open_9 (d) r=1e+09 { Mn:d }
6	L (-5.51e-06 / -4e-08 = -138%)	L (-4.93e-09 / -2.2e-07 = -2.24%)	L (-1.94e-07 / -8e-08 = -2.43%)	Dangerous_detected	fault_opens_open_10 (g) r=1e+09 { Mn:g }

```

Legend:
G - Good, measurement consistent with fault-free circuit within error bound
L - Detected with lower bound violation
U - Detected with upper bound violation
D - Detected with violations of both lower and upper bound
N - Not testable (error occurred during analysis, e.g. non-convergence)
E - Error definition in expression itself
- - Unevaluated

```

■ The legend for functional and safety check is as follows:

- ☐ G: Not detected, measurement consistent with fault-free circuit within error bound
- ☐ D: Detected, no clear definition of lower or upper bound (multiple violations, ...)
- ☐ L: Detected with lower bound violation
- ☐ U: Detected with upper bound violation
- ☐ E: Error definition in expression itself
- ☐ N: Untestable (non-convergence, any failure of fault simulation, fixed power / ground value, ...)
- ☐ -: Cannot evaluate (wrong expression, or asserts not violated prior to `autostop` triggered by the another assert)

■ Detection summary displays the following information:

- ☐ If the assert is marked as D, U, or L then it is Detected
- ☐ If all asserts are G, they are Undetected

- ❑ Any output for N, E, or – is
 - marked as X if that is the only assert check
 - ignored if there are multiple assert checks

■ Safety Summary

- ❑ C1 (Safe_undetected) when fault is undetected by both safecheck=func and safecheck=[check]
- ❑ C2 (Safe_detected) when fault is undetected by safecheck=func but detected by safecheck=[check]
- ❑ C3 (Dangerous_detected) when fault is detected by both safecheck=func and safecheck=[check]
- ❑ C4 (Dangerous_undetected) when fault is detected by safecheck=func but undetected by safecheck=[check]

■ Peak violation of asserts

- ❑ Maximum value of the absolute deviation if there are multiple violations.
- ❑ When min or max is non-zero
 - $[diff \text{ (peak value - min|max)}] \text{ "/" min|max} = \text{deviation in \%}$
Example: `"(1.23e-3 / 2 = 6.15e-2%)"`
- ❑ When either min or max is zero
 - $[peak \text{ value}] \text{ "/ 0} = inf$
Example: `"(1.23e-3 / 0 = inf)"`

■ Summary in Percentage (Total=C1+C2+C3+C4)

- ❑ Diagnostic coverage = $[C3 / (C3 + C4)]$
- ❑ Fault tolerance = $[(C1 + C2 + C3) / Total]$
- ❑ Coverage reported by checker = $[(C2 + C3) / Total]$
- ❑ Faults that are safe = $[(C1 + C2) / Total]$
- ❑ Safe_undetected = $C1 / Total$
- ❑ Safe_detected = $C2 / Total$
- ❑ Dangerous_detected = $C3 / Total$
- ❑ Dangerous_undetected = $C4 / Total$

□ Fault coverage = Detected / (Detected + Undetected) x100%

When fault sampling is applied in DFA with `faultsamplemethod=randomweighted` or `faultsamplemethod=randomuniform`, the confidence interval metrics are calculated and included in the FuSa report automatically based on the default confidence level 95%.

```
Failure Mode ID:      000
Failure Mode:        SPF

Sampling Estimated Metrics with 95% confidence level:

Diagnostic coverage      :      100.00% [ 94.13% , 100.00% ]
Fault tolerance         :      100.00% [ 94.13% , 100.00% ]
Coverage reported by checker :      100.00% [ 94.13% , 100.00% ]
Faults that are safe     :           0.00% [ 0.00% , 5.87% ]

Safe_undetected         :           0.00% [ 0.00% , 5.87% ]
Safe_detected           :           0.00% [ 0.00% , 5.87% ]
Dangerous_detected      :      100.00% [ 94.13% , 100.00% ]
Dangerous_undetected    :           0.00% [ 0.00% , 5.87% ]
Not_Classified          :           0.00% [ 0.00% , 5.87% ]

Detected                26
Undetected              0
Sampled                 61
Estimated coverage for full fault simulation
with 95% confidence level :      100.00% [ 94.13% , 100.00% ]
```

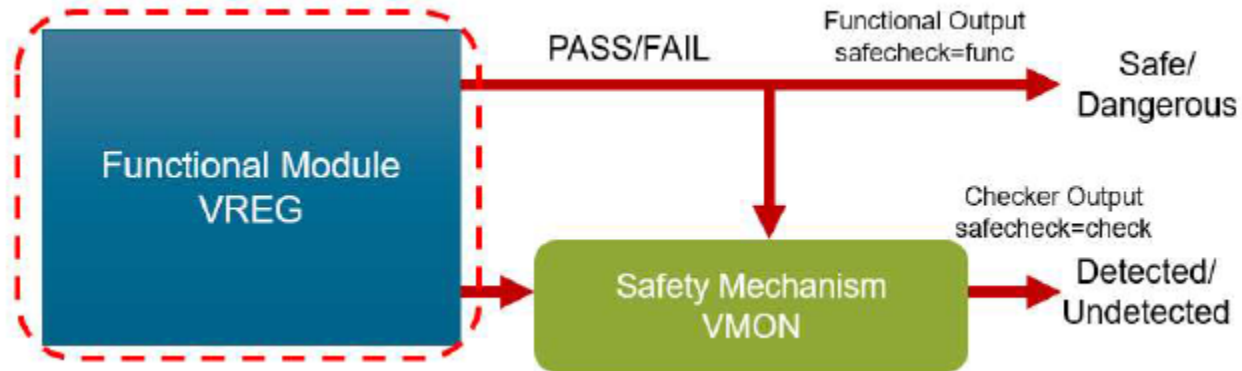
Using Spectre for Functional Safety Verification

Fault analysis can be used to simulate the diagnostic coverage by simulating each failure mode in the design identified in the FMEDA Verification Plan. In the FMEDA Verification Plan, the failure modes are defined, as well as, the type of fault metrics are analyzed. The results are reported in terms of Single Point Fault (SPF), or Latent Fault (LF).

Single Point Fault (SPF)

Single point faults are faults in a functional module that violate the safety goal. The purpose of the analysis is to identify if the dangerous faults are detected by the safety mechanism.

Let us discuss this with an example of a voltage regulator design, as shown below.



In the figure above, `VREG` block is the functional module and `VMON` block is the safety mechanism module.

To illustrate single point faults, consider a voltage regulator used in an ECU. The voltage regulator (`VREG`) block is the functional module. The safety mechanism or checker is a window comparator used to monitor the output in `VREG`. If the output of `VREG` is outside the safe operating range, then the `VMON` block will report that a dangerous condition has been detected at the output of `VREG`.

In Spectre Fault Analysis, two types of assertions are defined. A `safecheck=func` assertion is used to check the output of the functional module and determine if the safety goal has been violated. `safecheck=check` is used to monitor the output of the safety mechanism and determine if the violations of the safety goal have been detected.

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The diagnostic coverage report is generated based on the violations of the safety goal from the functional module and the ability of the safety mechanism to detect those violations. The report is shown below.

```
Failure Mode ID:      000
Failure Mode:         SPF

Diagnostic coverage   : 50.00%
Fault tolerance      : 83.33%
Coverage reported by checker : 66.67%
Faults that are safe  : 66.67%

Safe_undetected      : 16.67%
Safe_detected        : 50.00%
Dangerous_undetected : 16.67%
Dangerous_undetected : 16.67%
Not_Classified       : 0.00%

Note: Metrics calculated above are based on the user defined fault list which might or might not be the fault universe.

Observation points:
DEV_BIAS assert dev=Mn expr=V(g,s) min=-4e-08 max=2.501 message=Device bias limit exceeded | (violated)

Detection points:
LOAD_CAP assert expr=V(d) min=-2.2e-07 max=5 duration=1e-06 message=Load Cap limit exceeded | (violated)
LOAD_CAP2 assert expr=v(g,g) min=-8e-08 max=2.501 message=Load Cap2 limit exceeded | (violated)

Fault Detection Matrix:

| Fault Idx | F:DEV_BIAS | C:LOAD_CAP | C:LOAD_CAP2 | Safety | Fault Info |
|-----|-----|-----|-----|-----|-----|
| 1 | G | G | G | Safe_undetected | fault_bridges_bridge_1 ( 0 dd ) r=10 |
| 2 | G | G | G | Safe_detected | fault_bridges_bridge_6 ( 0 g ) r=10 |
| 3 | L ( -1.18e-08 / |-4e-08| = -29.49% ) | G | G | Dangerous_undetected | fault_bridges_bridge_7 ( 0 d ) r=10 |
| 4 | G | G | G | Safe_detected | fault_opens_open_7 ( g ) r=1e+09 { R3:2 } |
| 5 | G | G | G | Safe_detected | fault_opens_open_9 ( d ) r=1e+09 { Mn:d } |
| 6 | L ( -5.51e-06 / |-4e-08| = -138 ) | L ( -4.93e-09 / |-2.2e-07| = -2.24% ) | L ( -1.94e-07 / |-8e-08| = -2.43 ) | Dangerous_detected | fault_opens_open_10 ( g ) r=1e+09 { Mn:g } |

Legend:
G - Good, measurement consistent with fault-free circuit within error bound
L - Detected with lower bound violation
U - Detected with upper bound violation
D - Detected with violations of both lower and upper bound
N - Not testable (error occurred during analysis, e.g. non-convergence)
E - Error definition in expression itself
- - Unevaluated
```

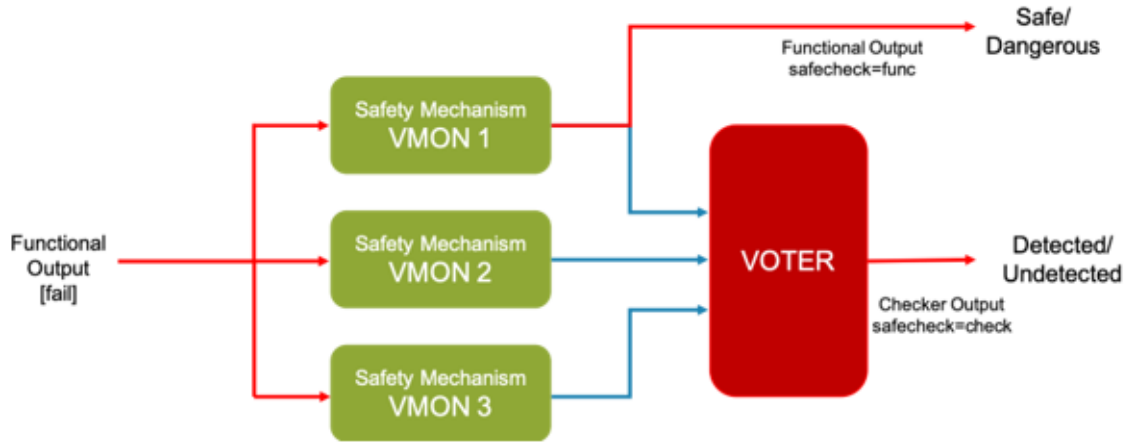
Latent Faults

Latent faults are the faults in the safety mechanism. These faults do not become active until a fault occurs in the functional module. In the Voltage Regular example, the faults in VMON block are active when the output of VREG is in a dangerous state. Since there is a fault in the VMON block, the dangerous fault may not be detected. So a latent fault is a fault in the safety mechanism module (checker/diagnostic module) which results in a functional failure not being detected.

To test for a latent fault, the input of VMON is forced to a dangerous state and the output of the safety mechanism is monitored to check if the fault is detected. The detection is performed by a separate diagnostic block used to monitor the safety mechanism. An example of a diagnostic block for the safety mechanism might be redundancy to improve the diagnostic coverage. In the example, three VMON blocks are used and if two or more detections are made, it means that there is a fault. Another approach for detecting latent faults would be to use an Analog Built-In Self-Testing (ABIST) block to periodically monitor whether or not the safety mechanism can detect failures. For example, use a DAC to apply a dangerous state at the input of the VMON block to monitor if it is detected.

Latent Faults can be of the following two types:

- **Latent Fault Continuous (LF-C):** If the output of the safety mechanism is monitored continuously to identify the latent faults, a continuous safety mechanism for latent faults is used. Simulating for latent faults when a continuously monitoring checker is used is equivalent to simulating for single point faults. The safety mechanism becomes the *functional module* of the test and the checker is the *safety mechanism* of the test, as shown in the following figure.



- Asserts are defined for both functional and checker blocks and enabled for fault simulation. When the simulation is performed, `spectre_fsrpt` is used to generate the functional safety report.

```
%spectre_fsrpt -FM LFC -FMID 111 dfa.log -o LFC.fsrpt
```

Failure Mode ID:	111
Failure Mode:	LFC
Diagnostic coverage	: 55.56%
Fault tolerance	: 81.82%
Coverage reported by checker	: 63.64%
Faults that are safe	: 59.09%
Safe_undetected	: 18.18%
Safe_detected	: 40.91%
Dangerous_undetected	: 22.73%
Dangerous_undetected	: 18.18%
Not_Classified	: 0.00%

Note: Metrics calculated above are based on the user defined fault list which might or might not be the fault universe.

Observation points:
DEV_BIAS assert dev=Mn expr=V(g,s) min=-4e-08 max=2.501 message=Device bias limit exceeded | (violated)

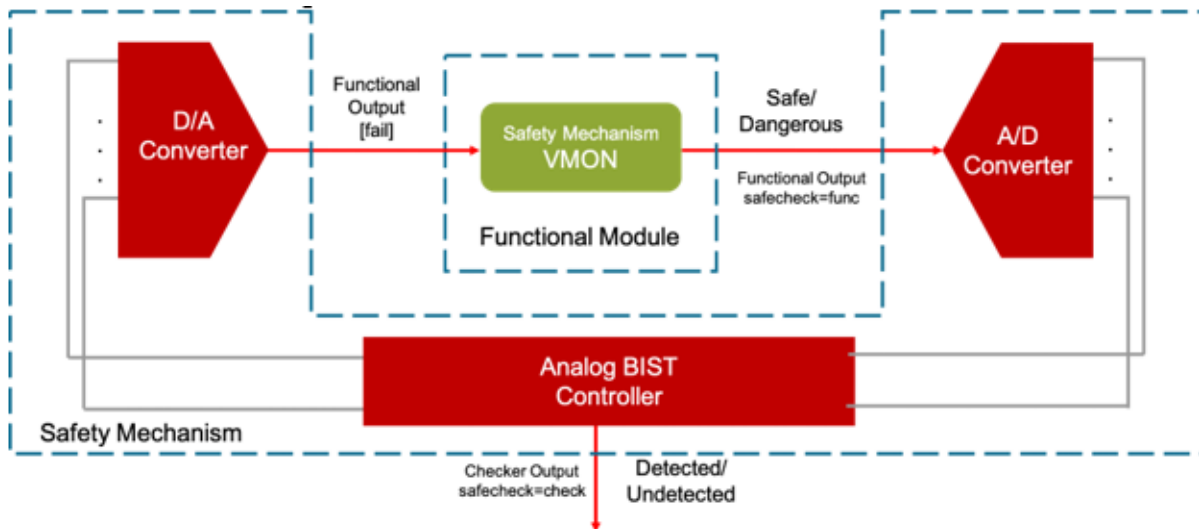
Detection points:
LOAD_CAP assert expr=V(d) min=-2.2e-07 max=5 duration=1e-06 message=Load Cap limit exceeded | (violated)
LOAD_CAP2 assert expr=V(g,g) min=-8e-08 max=2.501 message=Load Cap2 limit exceeded | (violated)

Fault Detection Matrix:

Fault Idx	F:DEV_BIAS	C:LOAD_CAP	C:LOAD_CAP2	Safety	Fault Info
1	G	G	G	Safe_undetected	fault_bridges_bridge_1 (0 dd) r=10
2	G	G	G	Safe_undetected	fault_bridges_bridge_2 (0 gg) r=10
3	L (-1.31e-08 / -4e-08 = -32.73%)	G	G	Dangerous_undetected	fault_bridges_bridge_3 (dd d) r=10
4	G	G	G	Safe_undetected	fault_bridges_bridge_4 (0 s) r=10
5	U (+2.45 / 2.5 = +97.96%)	D (-1.26e-07 / -2.2e-07 = -57.10%)	G	Dangerous_detected	fault_bridges_bridge_5 (gg s) r=10
6	G	G	U (+2.45 / 2.5 = +97.96%)	Safe_detected	fault_bridges_bridge_6 (0 g) r=10
7	L (-1.18e-08 / -4e-08 = -29.49%)	G	G	Dangerous_undetected	fault_bridges_bridge_7 (0 d) r=10
8	L (-0.45 / -4e-08 = -1.13e+07)	G	G	Dangerous_undetected	fault_bridges_bridge_8 (d s) r=10
9	U (+0.99 / 2.5 = +3.96%)	G	D (-1.5 / -8e-08 = -1.87e+07)	Dangerous_detected	fault_bridges_bridge_9 (d g) r=10
10	G	U (+0 / 5 = +0.00%)	U (+2.05 / 2.5 = +81.90%)	Safe_detected	fault_bridges_bridge_10 (s g) r=10
11	G	L (-0.00767 / -2.2e-07 = -3.49e+04)	G	Safe_detected	fault_opens_open_1 (dd) r=1e+09 (Vdd:p)
12	G	G	G	Safe_undetected	fault_opens_open_2 (gg) r=1e+09 (Vg:p)
13	G	L (-0.00766 / -2.2e-07 = -3.48e+04)	L (-7.82e-09 / -8e-08 = -9.78%)	Safe_detected	fault_opens_open_3 (dd) r=1e+09 (R1:l)
14	G	L (-0.00767 / -2.2e-07 = -3.49e+04)	G	Safe_detected	fault_opens_open_4 (d) r=1e+09 (R1:2)
15	L (-0.00374 / -4e-08 = -9.34e+04)	D (-3.87e-07 / -2.2e-07 = -1.76%)	L (-7.74e-09 / -8e-08 = -9.67%)	Dangerous_detected	fault_opens_open_5 (s) r=1e+09 (R2:1)
16	G	G	U (+2.5 / 2.5 = +99.92%)	Safe_detected	fault_opens_open_6 (gg) r=1e+09 (R3:1)

- **Latent Fault Periodic (LF-P):** If the output of the safety mechanism is monitored periodically to identify latent faults, then a periodic safety mechanism for latent faults is

used. An example of simulating for latent faults with periodic monitoring using analog Build-In Self-Testing (ABIST) module is shown below.



LF-P is a two-step process.

- In the first step:
 - Asserts are defined for both functional and checker blocks. Fault simulation is performed when functional asserts are enabled, and checker asserts are disabled.
 - Faults that are detected as Dangerous are identified to be used in the second step. The report contains the Safe and Dangerous faults classification.

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```
%spectre_fsrt -FM LFP -FMID 000 dfa_1.log -dang \
fault_list_dang.scs -o LFP_func.fsrt
```

```
Failure Mode ID:    000
Failure Mode:      LFP
```

Note: Metrics calculated above are based on the user defined fault list which might or might not be the fault universe.

```
Observation points:
DEV_BIAS assert dev=Mn expr=V(g,s) min=-4e-08 max=2.501 message=Device bias limit exceeded | (violated)
```

Fault Detection Matrix:

Fault Idx	F:DEV_BIAS	Safety	Fault Info
1	G	Safe	fault_bridges_bridge_1 (0 dd) r=10
2	G	Safe	fault_bridges_bridge_2 (0 gg) r=10
3	L (-1.31e-08 / -4e-08 = -32.73%)	Dangerous	fault_bridges_bridge_3 (dd d) r=10
4	G	Safe	fault_bridges_bridge_4 (0 s) r=10
5	U (+2.45 / 2.5 = +97.96%)	Dangerous	fault_bridges_bridge_5 (gg g) r=10
6	G	Safe	fault_bridges_bridge_6 (0 g) r=10
7	L (-1.18e-08 / -4e-08 = -29.49%)	Dangerous	fault_bridges_bridge_7 (0 d) r=10
8	L (-0.45 / -4e-08 = -1.13e+07)	Dangerous	fault_bridges_bridge_8 (d s) r=10
9	U (+0.09 / 2.5 = +3.60%)	Dangerous	fault_bridges_bridge_9 (d g) r=10
10	G	Safe	fault_bridges_bridge_10 (s g) r=10
11	G	Safe	fault_opens_open_1 (dd) r=1e+09 { Vdd:p }
12	G	Safe	fault_opens_open_2 (gg) r=1e+09 { Vg:p }
13	G	Safe	fault_opens_open_3 (dd) r=1e+09 { R1:1 }
14	G	Safe	fault_opens_open_4 (d) r=1e+09 { R1:2 }
15	L (-0.00374 / -4e-08 = -9.34e+04)	Dangerous	fault_opens_open_5 (s) r=1e+09 { R2:1 }
16	G	Safe	fault_opens_open_6 (gg) r=1e+09 { R3:1 }
17	G	Safe	fault_opens_open_7 (g) r=1e+09 { R3:2 }
18	U (+2.5 / 2.5 = +99.92%)	Dangerous	fault_opens_open_8 (g) r=1e+09 { R4:1 }
19	G	Safe	fault_opens_open_9 (d) r=1e+09 { Mn:d }
20	L (-5.51e-06 / -4e-08 = -138)	Dangerous	fault_opens_open_10 (g) r=1e+09 { Mn:g }
21	G	Safe	fault_opens_open_11 (s) r=1e+09 { Mn:s }
22	L (-3.67e-05 / -4e-08 = -918)	Dangerous	fault_opens_open_12 (0) r=1e+09 { Mn:b }

Legend:

- G - Good, measurement consistent with fault-free circuit within error bound
- L - Detected with lower bound violation
- U - Detected with upper bound violation
- D - Detected with violations of both lower and upper bound
- N - Not testable (error occurred during analysis, e.g. non-convergence)
- E - Error definition in expression itself
- - Unevaluated
- X - Unknown detection status

❑ In the second step:

- Dangerous fault list is included in the netlist. Checker asserts are enabled and functional asserts are disabled to perform simulation.
- A report is generated that contains the Detected and Undetected faults classifications for all the dangerous faults.

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```
% spectre_fsrpt -FM LFP -FMID 111 dfa_2.log -o
LFP_check.fsrpt
```

```
Failure Mode ID: 111
Failure Mode: LFP

Note: Metrics calculated above are based on the user defined fault list which might or might not be the fault universe.

Detection points:
LOAD_CAP assert expr=v(d) min=-2.2e-07 max=5 duration=1e-06 message=Load Cap limit exceeded | (violated)
LOAD_CAP2 assert expr=v(gg,g) min=-8e-08 max=2.501 message=Load Cap2 limit exceeded | (violated)

Fault Detection Matrix:
```

Fault Idx	C:LOAD_CAP	C:LOAD_CAP2	Detection	Fault Info
1	G	G	Undetected	fault_bridges_bridge_3 (dd d) r=10
2	D (-1.26e-07 / -2.2e-07 = -57.10%)	G	Detected	fault_bridges_bridge_5 (gg g) r=10
3	G	G	Undetected	fault_bridges_bridge_7 (0 d) r=10
4	G	G	Undetected	fault_bridges_bridge_8 (d s) r=10
5	G	D (-1.5 / -8e-08 = -1.87e+07)	Detected	fault_bridges_bridge_9 (d g) r=10
6	D (-3.87e-07 / -2.2e-07 = -1.76)	L (-7.74e-09 / -8e-08 = -9.67%)	Detected	fault_opens_open_5 (s) r=1e+09 (R2:1)
7	D (-1.28e-07 / -2.2e-07 = -58.18%)	L (-3.38e-07 / -8e-08 = -4.22)	Detected	fault_opens_open_8 (g) r=1e+09 (R4:1)
8	L (-4.93e-09 / -2.2e-07 = -2.24%)	L (-1.94e-07 / -8e-08 = -2.43)	Detected	fault_opens_open_10 (g) r=1e+09 (Mn:g)
9	G	G	Undetected	fault_opens_open_12 (0) r=1e+09 (Mn:b)

Legend:

- C - Good, measurement consistent with fault-free circuit within error bound
- L - Detected with lower bound violation
- U - Detected with upper bound violation
- D - Detected with violations of both lower and upper bound
- N - Not testable (error occurred during analysis, e.g. non-convergence)
- E - Error definition in expression itself
- - Unevaluated
- X - Unknown detection status

- You can merge LFP_func.fsrpt and LFP_check.fsrpt to get SD, SU, DD, DU classification and calculate the diagnostic coverage.
- ```
%spectre_fsrpt LFP_func.fsrpt LFP_check.fsrpt -FM LFP -
FMID 222 -o LFP_full.fsrpt
```

```
Failure Mode ID: 222
Failure Mode: LFP

Diagnostic coverage (*) : 55.56%
Fault tolerance : 81.82%
Coverage reported by checker : 22.73%
Faults that are safe : 59.09%

Dangerous_detected : 22.73%
Dangerous_undetected : 18.18%
Not_Classified : 59.09%

Note: Metrics calculated above are based on the user defined fault list which might or might not be the fault universe.

Observation points:
DEV_BIAS assert dev=Mn expr=v(g,s) min=-4e-08 max=2.501 message=Device bias limit exceeded | (violated)

Detection points:
LOAD_CAP assert expr=v(d) min=-2.2e-07 max=5 duration=1e-06 message=Load Cap limit exceeded | (violated)
LOAD_CAP2 assert expr=v(gg,g) min=-8e-08 max=2.501 message=Load Cap2 limit exceeded | (violated)

(*)WARNING: Fault simulation(s) with unknown detection status (X) exist in the Safety column of the table(Fault idx = 0, 1, 3, 5, 9, 10, 11, 12, 13, 15, 16, 18, 20).
Report may not be accurate.

Fault Detection Matrix:
```

| Fault Idx | F:DEV_BIAS                            | C:LOAD_CAP                             | C:LOAD_CAP2                         | Detection  | Safety               | Fault Info                                  |
|-----------|---------------------------------------|----------------------------------------|-------------------------------------|------------|----------------------|---------------------------------------------|
| 1         | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_bridges_bridge_1 ( 0 dd ) r=10        |
| 2         | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_bridges_bridge_2 ( 0 gg ) r=10        |
| 3         | L ( -1.31e-08 /  -4e-08  = -32.73% )  | G                                      | G                                   | Detected   | Dangerous_undetected | fault_bridges_bridge_3 ( dd d ) r=10        |
| 4         | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_bridges_bridge_4 ( 0 s ) r=10         |
| 5         | U ( +2.45 /  2.5  = +97.90% )         | D ( -1.26e-07 /  -2.2e-07  = -57.10% ) | G                                   | Detected   | Dangerous_detected   | fault_bridges_bridge_5 ( gg g ) r=10        |
| 6         | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_bridges_bridge_6 ( 0 g ) r=10         |
| 7         | L ( -1.18e-08 /  -4e-08  = -29.49% )  | G                                      | G                                   | Detected   | Dangerous_undetected | fault_bridges_bridge_7 ( 0 d ) r=10         |
| 8         | L ( -0.45 /  -4e-08  = -1.13e+07 )    | G                                      | G                                   | Detected   | Dangerous_undetected | fault_bridges_bridge_8 ( d s ) r=10         |
| 9         | U ( +0.09 /  2.5  = +3.60% )          | G                                      | D ( -1.5 /  -8e-08  = -1.87e+07 )   | Detected   | Dangerous_detected   | fault_bridges_bridge_9 ( d g ) r=10         |
| 10        | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_bridges_bridge_10 ( s g ) r=10        |
| 11        | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_opens_open_1 ( dd ) r=1e+09 ( Vdd:p ) |
| 12        | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_opens_open_2 ( gg ) r=1e+09 ( Vg:p )  |
| 13        | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_opens_open_3 ( dd ) r=1e+09 ( R1:1 )  |
| 14        | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_opens_open_4 ( d ) r=1e+09 ( R1:2 )   |
| 15        | L ( -0.00374 /  -4e-08  = -9.34e+04 ) | D ( -3.87e-07 /  -2.2e-07  = -1.76 )   | L ( -7.74e-09 /  -8e-08  = -9.67% ) | Detected   | Dangerous_detected   | fault_opens_open_5 ( s ) r=1e+09 ( R2:1 )   |
| 16        | G                                     | -                                      | -                                   | Undetected | Safe_X               | fault_opens_open_6 ( gg ) r=1e+09 ( R3:1 )  |



## Getting Started With Direct Fault Analysis Using Asserts

The following example of Direct Fault Analysis provides a guidance on how to generate the functional safety report based on the assert setup approach.

Direct fault analysis evaluates the asserts with `safecheck` throughout the simulation. The `faultstart` and `faultstop` options only affect the creation of the table file. Direct fault analysis can also be used for generating the fault detection report. Refer to [Spectre Transient Fault Analysis](#) for defect detection matrix generation based on fault table file.

## Preparing and Starting Direct Fault Analysis

Once the fault list is ready, you need to set up the direct fault analysis, as shown below.

- Specify the asserts to be checked for both functional and diagnostic modules, as shown below, as shown below.

```
DEV_BIAS assert safecheck=func dev=Mn expr="V(g,s)" min=-4e-8 max=2.501
message="Device bias limit exceeded"

LOAD_CAP assert safecheck=check expr="V(d)" min=-22e-8 max=5 duration=1u
message="Load Cap limit exceeded"

LOAD_CAP2 assert safecheck=check expr="v(gg,g)" min=-8e-8 max=2.501
message="Load Cap2 limit exceeded"
```

- Enable `checklimit` for fault simulation related asserts only followed by the direct fault analysis statement.

```
faultcheck checklimit enable=[DEV_BIAS LOAD_CAP LOAD_CAP2]
```

- Specify the direct fault analysis statement for running child transient analysis for all faults, as shown below.

- ☐ Without specifying the fault times

```
Directfault sweep faults=[*] {
tran1 tran start=0 stop=3e-3 annotate=status
}
```

- ☐ By specifying the fault times, the fault result is saved in a table file at the fault time points.

```
Directfault sweep faults=[*] {
tran1 tran start=0 stop=3e-3 annotate=status faulttimes=[0.5m 7.5m]
}
```

- Run the simulation as follows.

```
%spectre +aps report_dfa.scs +log report_dfa.log -o out_fusa_dfa/
```

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## Viewing Data Output

In the log file, the list of faults is reported in the Circuit inventory section, as shown below.

Circuit inventory:

```
nodes 6
assert 5
mos11010 1
resistor 6
vsource 2
```

Design checks inventory:

```
bridge 10
assert 3
open 12
```

SAFE: nominal\_SAFE = 0 (0 %) -----> fault free simulation, index=0

+++++

Time for SAFE itNum=0: CPU = 9.999 ms, elapsed = 10.07294798 s.

Time accumulated: CPU = 304.953 ms, elapsed = 41.14494801 s.

Peak resident memory used = 46.5 Mbytes.

Notice from spectre at faults\_SAFE = 0 during transient analysis `SAFE-000\_tran1', during Sweep analysis `SAFE'.

No checklimit analysis defined for asserts. A default checklimit analysis 'SpectreChecklimitAnal' has been created with all asserts enabled.

The following asserts will be enabled for all subsequent analyses until the next checklimit analysis statement is found:

DEV\_BIAS : ON

LOAD\_CAP : ON

LOAD\_CAP2 : ON

\*\*\*\*\*

Transient Analysis `SAFE-000\_tran1': time = (0 s -> 12 ms)

\*\*\*\*\*

DC simulation time: CPU = 999 us, elapsed = 353.8131714 us.

... ..

SAFE-000\_tran1: time = 300.3 us (2.5 %), step = 17.95 us (150 m%)

SAFE-000\_tran1: time = 987.7 us (8.23 %), step = 93.86 us (782 m%)

SAFE-000\_tran1: time = 1.655 ms (13.8 %), step = 240 us (2 %)

SAFE-000\_tran1: time = 2.135 ms (17.8 %), step = 240 us (2 %)

SAFE-000\_tran1: time = 2.808 ms (23.4 %), step = 192.3 us (1.6 %)

SAFE-000\_tran1: time = 3.315 ms (27.6 %), step = 17.41 us (145 m%)

... ..

+++++

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```
SAFE: bridge_1_SAFE = 1 (11.11111111 %) ---> Sweeps from 1st fault
 bridge_1_SAFE;index=1

+++++
Time for SAFE itNum=1: CPU = 0 s, elapsed = 179.0523529 us.
Time accumulated: CPU = 350.946 ms, elapsed = 41.21105385 s.
Peak resident memory used = 48.2 Mbytes.

Transient Analysis `SAFE-001_tran1': time = (0 s -> 12 ms)

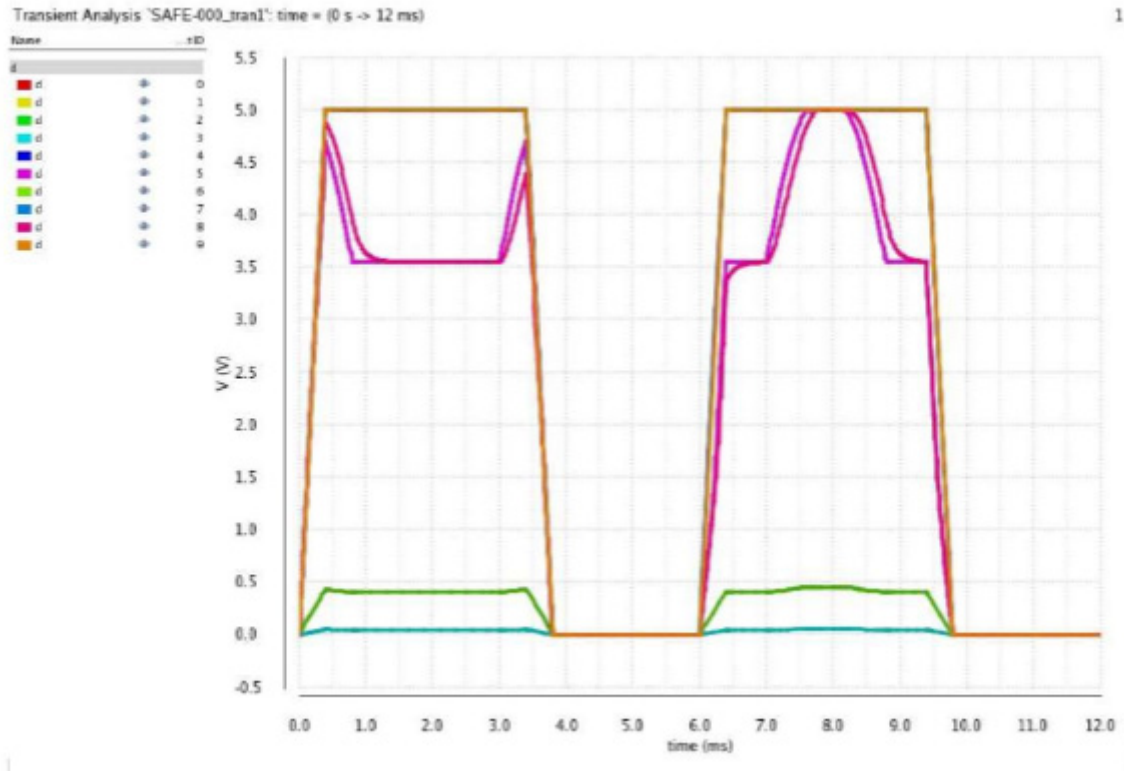
DC simulation time: CPU = 0 s, elapsed = 174.0455627 us.
...
SAFE-001_tran1: time = 969.6 us (8.08 %), step = 85.16 us (710 m%)
SAFE-001_tran1: time = 1.62 ms (13.5 %), step = 240 us (2 %)
SAFE-001_tran1: time = 2.34 ms (19.5 %), step = 240 us (2 %)
SAFE-001_tran1: time = 2.82 ms (23.5 %), step = 240 us (2 %)
```

The data is saved in the raw directory (out\_fusa\_dfa/report\_dfa.raw/) with the following names:

- Sweep for transient analysis: [SweepName-sweepIndex\_TranName].tran.tran, for example, SAFE-001\_tran1.tran.tran
- Assert violations are saved in sqldb format: *NetlistName*.sqldb, for example, direct\_fault.sqldb
- Sweep for transient assert violation if a violation is triggered:  
[SweepName-sweepIndex\_TranNameViolations].violations, for example, SAFE-007\_tran1Violations.violations

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When the raw data is plotted in the waveform viewer, each curve represents one fault result with the fault id shown in the legend, as shown below.  $i_d=0$  is the nominal fault-free result. The fault table file shows more details about the fault id associated with the fault statement.



### Post-processing for Functional Safety Report

You can use the Spectre binary `spectre_fsrpt` to generate the functional safety report based on the assert violation for Direct Fault Analysis on screen, or direct the output to a file. The script reads the log file and looks for the path of `sqldb` file for violations.

```
%.../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log
%.../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt
```

You may run a few fault tests with the same test bench for different fault lists and generate one functional safety report for each test. The `spectre_fsrpt` binary helps you merge all these reports to a complete one.

The following is an example of running three fault simulations for different fault lists:

```
spectre +aps direct_fault_1.scs -outdir out_merge_1/
spectre +aps direct_fault_2.scs -outdir out_merge_2/
spectre +aps direct_fault_3.scs -outdir out_merge_3
```

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The following is an example of generating three functional safety reports for different simulations:

```
%../bin/spectre_fsrpt out_merge_1/fl_dfa_merge_1.log -o FuSa_1.txt
%../bin/spectre_fsrpt out_merge_2/fl_dfa_merge_2.log -o FuSa_2.txt
%../bin/spectre_fsrpt out_merge_3/fl_dfa_merge_3.log -o FuSa_3.txt
```

The following is an example of merging three reports into one functional safety report:

```
%../bin/spectre_fsrpt FuSa_1.txt FuSa_2.txt FuSa_3.txt -o FuSa_Full.txt
```

You can extract the new fault list for the C1(SU), C2(SD), C3(DD), and C4(DU) (see [Functional Safety Report Based on Assert Violations](#) for definition of C1, C2, C3, and C4) categories to a file for further simulation during the generation of the functional safety report, as shown below.

```
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt \
-DU DU_Fault_List.scs
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt \
-DD DD_Fault_List.scs
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt \
-SD SD_Fault_List.scs
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt \
-SU SU_Fault_List.scs
```

In addition to the options, such as -DU, -SU, -SD, and -DD, you can save the fault lists to a file based on either Detection or Safety column in the report using the following options:

- **-safe *filename*** saves all faults from report with Safe\_\* status

```
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt \
-safe safe_Fault_List.scs
```
- **-dang *filename*** saves all faults from report with Dangerous\_\* status

```
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt \
-dang dangerous_Fault_List.scs
```
- **-det *filename*** saves all faults from report with \*\_Detected status

```
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt \
-det detected_Fault_List.scs
```
- **-undet *filename*** saves all faults from report with \*\_Undetected status

```
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o FuSa_dfa.txt \
-undet undetected_Fault_List.scs
```

When the fault simulation only contains one type of assert and the report has either Detection or Safety column, the -DU, -SU, -SD, and -DD options are not applicable and spectre\_fsrpt generates a warning and ignores the request.

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- Options `-safe`, and `-dang` can be used only when `Safety` column exists in the report.

```
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o Func_dfa.txt \
-safe safe_Fault_List.scs
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o Func_dfa.txt \
-dang dangerous_Fault_List.scs
```

- Options `-det` and `-undet` can be used when the `Detection` column exists in the report.

```
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o Check_dfa.txt \
-det detected_Fault_List.scs
%../bin/spectre_fsrpt out_fusa_dfa/report_dfa.log -o Check_dfa.txt \
-undet detected_Fault_List.scs
```

In the functional safety report, the solutions and violations are listed for the detected faults in relative percentage, as shown below.

| Fault Idx | F:assert1           | C:assert2                             | C:assert3 | Detection  | Safety             | Fault Info                  |
|-----------|---------------------|---------------------------------------|-----------|------------|--------------------|-----------------------------|
| 0         | U ( +4 /  1  = +4 ) | U ( +0.000702 /  0.00075  = +93.57% ) | D         | Detected   | Dangerous detected | nominal (golden) simulation |
| 1         | G                   | G                                     | G         | Undetected | Safe_undetected    | bridge_1 ( g 0 ) r=10       |
| 2         | G                   | U ( +0.0042 /  0.00075  = +5.6 )      | D         | Detected   | Safe detected      | bridge_2 ( d 0 ) r=10       |
| 3         | G                   | G                                     | D         | Detected   | Safe detected      | open_1 ( d ) r=1e+09 { Mn:d |
| 4         | G                   | G                                     | G         | Undetected | Safe_undetected    | open_2 ( g ) r=1e+09 { R3:2 |

With parameter `-s --short` added in command line, `spectre_fsrpt` generates the table without solutions display, as shown below.

| Fault Idx | F:assert1 | C:assert2 | C:assert3 | Detection  | Safety             | Fault Info                    |
|-----------|-----------|-----------|-----------|------------|--------------------|-------------------------------|
| 0         | U         | U         | D         | Detected   | Dangerous detected | nominal (golden) simulation   |
| 1         | G         | G         | G         | Undetected | Safe_undetected    | bridge_1 ( g 0 ) r=10         |
| 2         | G         | U         | D         | Detected   | Safe detected      | bridge_2 ( d 0 ) r=10         |
| 3         | G         | G         | D         | Detected   | Safe detected      | open_1 ( d ) r=1e+09 { Mn:d   |
| 4         | G         | G         | G         | Undetected | Safe_undetected    | open_2 ( g ) r=1e+09 { R3:2 } |

## Including or excluding Instances with the Given Hierarchical Name

While generating the defect coverage based on hierarchy or design scope in the netlist, you can apply the scope parameters `-i` or `-I` to include or `-x` to exclude a subset of the fault list that belongs to the specified subcircuit instances.

```
%spectre_fsrpt inp.log ---inst "'X1 Xa*'"
%spectre_fsrpt inp.log ---xinst "'X1.X*'"
```

## Generating a Report Based on the Name of Signals/Asserts

Use parameter `-s` to generate the report only for the selected signals or asserts. You can specify a comma-separated list of signals or asserts to specify multiple signals or asserts. Wildcards `'` and `'` are also supported when an expression is enclosed in quotes.

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```
%spectre_fsrpt -sh -s avg_qqq, vgs_g45n1svt_LEV1 out/input.log
> report_signals.txt
```

| Fault Idx | F:avg_qqq | C:vgs_g45n1svt_LEV1 | Detection | Safety             |
|-----------|-----------|---------------------|-----------|--------------------|
| 0         | U         | U                   | Detected  | Dangerous_detected |
| 1         | U         | U                   | Detected  | Dangerous_detected |
| 2         | U         | U                   | Detected  | Dangerous_detected |

```
%spectre_fsrpt -sh -s avg_qqq'vgs_g45n1svt_LEV1' out/input.log
> report_wilds.txt
```

| Fault Idx | F:avg_qqq | C:vgs_g45n1svt_LEV1 | C:vgs_g45n1svt_LEV2 | Detection | Safety             |
|-----------|-----------|---------------------|---------------------|-----------|--------------------|
| 0         | U         | U                   | U                   | Detected  | Dangerous_detected |
| 1         | U         | U                   | G                   | Detected  | Dangerous_detected |
| 2         | U         | U                   | G                   | Detected  | Dangerous_detected |

## Merging Reports for the Faults with Same Connection but Different Fault ID

By default, same fault is included only once when merging the report files. With parameter `-r (--incredund)` specified in command, `spectre_fsrpt` includes redundant faults with different IDs into a combined report when merging several report files.

```
%spectre_fsrpt -r spfm_1.rpt spfm_2.rpt > merge_incl.rpt
```

## Using the `faultautostop` Feature in Direct Fault Analysis

You can use the `faultautostop` parameter to enable the autostop feature in direct fault analysis. Fault simulation stops whenever an assert violation is triggered for the defined check. The example shows that autostop has been enabled by using `faultautostop=both`, which is required for functional safety report generation. You can also set `faultautostop=func` or `faultautostop=check`, if required.

```
SAFE sweep faults=[*] {
 tran1 tran stop=12e-3 annotate=status faulttimes=[5m 6.5m] \
 faultautostop=both
}
```

When `faultautostop=func|check|both|all`, the violation triggered by at least one of the asserts causes the simulation to stop automatically. Asserts that are not violated before autostop are marked as untestable (-) in the functional safety report.

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The format of the output table file of signals and currents remains the same; they are independent of autostop. All data for the time points after the autostop gets replicated from the last found solution and the iterations value is set to 1, as shown in the following figure.

|                           |                                                     |           |           |           |            |    |   |
|---------------------------|-----------------------------------------------------|-----------|-----------|-----------|------------|----|---|
| 1: bridge_1 ( g 0 ) r=10  | The data is replicated from the last found solution |           |           |           |            |    |   |
| 5.000000E-03              | 5.000E+00                                           | 5.000E+00 | 2.537E+00 | 2.487E-02 | 9.090E-10  | 10 | 1 |
| 6.500000E-03              | 5.000E+00                                           | 5.000E+00 | 2.537E+00 | 2.487E-02 | 9.090E-10  | 10 | 1 |
| 2: bridge_2 ( dd 0 ) r=10 | Number of iterations set to 1 for autostop          |           |           |           |            |    |   |
| 5.000000E-03              | 0.000E+00                                           | 4.465E-17 | 5.000E+00 | 2.500E+00 | -4.465E-18 | 10 | 2 |
| 6.500000E-03              | 5.000E+00                                           | 3.548E+00 | 5.000E+00 | 2.500E+00 | 1.452E-01  | 10 | 2 |

The log file displays a message about autostop and the fault simulation getting terminated, as shown in red below.

```
Fault analysis for bridge_1 : 22 time steps
Intrinsic bridge_1 analysis time: CPU = 62.991 ms, elapsed = 74.63693619 ms.
DC simulation time: CPU = 1 ms, elapsed = 536.9186401 us.
Fault analysis for bridge_2 : 361 time steps
Intrinsic bridge_2 analysis time: CPU = 17.997 ms, elapsed = 18.2697773 ms.
DC simulation time: CPU = 0 s, elapsed = 524.9977112 us.
Fault analysis for bridge_3 : 183 time steps
Intrinsic bridge_3 analysis time: CPU = 9.999 ms, elapsed = 10.31899452 ms.
DC simulation time: CPU = 0 s, elapsed = 522.1366882 us.
Fault analysis for open_1 : 182 time steps
Intrinsic open_1 analysis time: CPU = 9.998 ms, elapsed = 10.59818268 ms.
DC simulation time: CPU = 0 s, elapsed = 493.0496216 us.
Warning from spectre at time = 3.8 ms during transient analysis `timezero'.
WARNING (SPECTRE-4103): LOAD_CAP2.open_2: Instance , Load Cap2 limit
exceeded.
Expression `v(gg,g)' having value -121.3205893e-09 has exceeded its lower bound `-
80e-09'.
Fault open_2 detected with assert. Analysis terminated due to autostop at 3.8 ms.
Warning from spectre at time = 3.8 ms during transient analysis `timezero'.
WARNING (SPECTRE-4121): LOAD_CAP2.open_2: instance , Load Cap2 limit
exceeded.
Expression `v(gg,g)' exceeds its lower bound `-80e-09' . Peak value was -
121.3205893e-
09 at time 3.8e-03. Total duration of overshoot was 0.
Fault analysis for open_2 : 5159 time steps
Intrinsic open_2 analysis time: CPU = 227.965 ms, elapsed = 228.9030552 ms.
DC simulation time: CPU = 0 s, elapsed = 524.0440369 us.
Warning from spectre at time = 400.2020912 us during transient analysis `timezero'
WARNING (SPECTRE-4104): LOAD_CAP2.open_3: Instance , Load Cap2 limit
exceeded.
```



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```
Expression `v(gg,g)` having value 2.501260569 has exceeded its upper bound `2.501'.
Fault open 3 detected with assert. Analysis terminated due to autostop at
400.2020912 us
```

## Improving Performance

Direct fault analysis provides the most accurate results; however, it takes long to complete the simulation when the fault list is long, or the nominal simulation is slow. To speed up the simulation for direct fault analysis, you can use the `distribute` option to distribute a sweep analysis across multiple machines. Using the `fork`, `lsf`, or `sge` option, you can choose to launch the child processes. You can use the command-line option `+mp=<numprocesses>` to specify the number of child processes to be launched.

## Job Distribution

To enable the distributed mode of Direct Fault Analysis, use `+mp` at the Spectre command line. With the following statement, the master job requests one CPU and issues three new `bsub` commands with the same set of `bsub` parameters used for the master. The master job and the first child job forked from the master are run in one CPU, while the remaining child jobs are distributed in different CPUs. In case the first (forked) child job completes sooner, it waits for all the distributed child jobs to finish and then the results of all the jobs are merged.

```
%bsub -R "(OSNAME==Linux)" "spectre +aps -mt +mp=3 direct_fault.scs -outdir
fullpath/out_dfa_mp/"
```

You can set different LSF queues for the master and child jobs using the environment variable `CDS_MMSIM_MP_QUEUE`. Setting this variable to a particular queue submits the distributed jobs in that queue. The master job runs in the original queue specified in the `bsub` command while submitting the job.

For example, if you set the value of the `CDS_MMSIM_MP_QUEUE` environment variable to `batch` (`setenv CDS_MMSIM_MP_QUEUE batch`) and run the test case containing sweep analysis and `+mp` in a `bsub` command with interactive queue, the parent job is run in the interactive queue and the distributed jobs are run in batch queue in LSF.

You can enable multithreading for each job. The following examples shows that each job runs with `mt=4` on one host:

```
%bsub -R "(OSNAME==Linux) span[hosts=1]" -n 4 "spectre +aps +mt=lsf +mp=3
direct_fault.scs -outdir fullpath/out_dfa_mp/"
```

To run the distribution on one machine, you may use the following command with a single thread.

```
%spectre +aps -mt +mp=3 direct_fault.scs -outdir out_dfa_mp/
```

During DFA, it is hard to predict the expected performance for a group of faults since it depends on many factors, such as type of faults, detectability, triggered oscillation, and so on. You can use the `faultsort` option for better load balancing. When `faultsort` is set to `no`, the order of faults to be simulated is based on random sampling. As a result, the faults assigned to a specific process are simulated according to the number of samples.

```
myDFA sweep faults=[*] faultsort=no {
DFA tran start=0 stop=100p annotate=status faultautostop=check
}
```

The default setting `faultsort=yes` keeps the existing order according to the faults defined in the fault list.

### Using the Automated Three-Step Process

To provide a more convenient way to perform functional safety analysis, an automated three steps process is implemented to integrate the fault generation, direct fault simulation, and perform post-processing for functional safety report. You can use the `+fsa` command-line option to automate the process of performing functional safety analysis. You need at least one `assert` statement with the `safecheck` parameter specified in the netlist to run the automated flow.

### Specifying the Fault List

To run functional safety analysis, the existing fault list can be included, or a new fault list can be generated using `info` analysis. Following three scenarios are possible:

- `info` analysis for fault generation precedes the direct fault analysis (sweep analysis) or transient fault analysis (transient analysis) in the netlist  
or
- A fault list is included in the netlist and direct fault analysis (sweep analysis) or transient fault analysis (transient analysis) is specified  
or
- `info` analysis for fault generation precedes direct fault analysis or transient fault analysis, and a fault list is included in the netlist. In this case, both fault lists will be used in direct fault analysis.

If neither `info` analysis for fault generation is specified nor the fault list is included in the netlist, Spectre generates an error message and skips fault simulation.

**Note:** Custom fault simulation is not available in the `+fsa` mode.

## Performing Direct Fault Analysis with +fsa

You need to define a `sweep` or `tran` analysis in the netlist to perform either direct fault analysis or transient fault analysis for the automated simulation. Following are the rules to handle the `faults` parameter in the `sweep` or `tran` statement:

- If a fault list is included in the netlist, the `faults` parameter keeps the functionality as defined (`faults=[*]`, or `faults=[block_1 block_2]`)
- If `info` analysis for fault generation is specified, without `faultblock=block_name`, then `faults=[*]` will enforce all generated faults to be considered in direct fault analysis or transient fault analysis
- If `info` analysis has `faultblock=block_name` specified, then the name of the block can be used in `faults=[block_name]`

Fault scoping parameters in `sweep` (`faultsid`, `faultsname`, `faultsinst`) are supported.

When direct fault analysis completes, `spectre_fsrpt` runs automatically to generate the functional safety report. The data is saved as `log_file_name.fsrpt` in the same path as the regular log file.

## Enabling One Step Simulation

If the `info` statement for fault generation is defined in the netlist and transient statement is specified either for direct fault analysis or transient fault analysis, Spectre performs one step simulation for the faults created by the `info` statement.

## Spectre Transient Fault Analysis

Spectre direct fault analysis is applicable only for small-sized designs, or a small fault count. In most practical cases, direct method may take months or years to finish the simulation.

Spectre transient fault analysis improves the performance of analog fault simulation and delivers results with the required accuracy, within reasonable time. Spectre uses the abstraction of only applying the faults at user-defined transient time points (fault times). Different methods are available for injecting the faults at the fault time points. The methods differ in how long (how many steps/iterations) they inject the fault.

The longer the injection interval, the higher is the chance to match the direct fault simulation reference, and therefore, the better is the accuracy. However, the longer the injection interval, the longer is the simulation time. The shorter the injection interval, the less likely is the chance that the fault will impact the circuit behavior. On the other hand, the simulation time is fast, and it may still provide an initial overview of the fault impact.

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The following is the syntax for transient fault analysis:

```
TFAName tran start=0 stop=50n [faults=[* | faultblock1...] faulttimes=[...]]
```

You can specify the following fault parameters with transient analysis:

|                                               |                                                                                                                                                                                                                                                              |
|-----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>faulttimes=[...]</code>                 | Fault times in ascending time order where transient fault analysis is performed                                                                                                                                                                              |
| <code>faultstart, faultstop, faultstep</code> | Fault start time, stop time and time interval between start and stop time.                                                                                                                                                                                   |
| <code>faultfile</code>                        | Name of the file that contains the fault times in ascending time order for transient fault.                                                                                                                                                                  |
| <code>faultevent</code>                       | The fault times to perform fault simulation when the events are triggered.                                                                                                                                                                                   |
| <code>faultautostop</code>                    | Stop the fault analysis automatically when the fault is detected based on assert violation. Possible values are <code>no</code> , <code>func</code> , <code>check</code> , <code>both</code> , and <code>all</code> . The default value is <code>no</code> . |
| <code>faultdetratio</code>                    | Stop the fault simulation automatically when the specified detection ratio is achieved.                                                                                                                                                                      |
| <code>faultconfidlevel</code>                 | Stop the fault simulation automatically when the specified detection ratio is achieved with the given confidence level.                                                                                                                                      |
| <code>faultskipdc</code>                      | Enforce <code>skipdc=yes</code> during fault analysis when there is no solution found during the initial DC analysis. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>yes</code> .                                     |
| <code>faultstrobe=no</code>                   | Time point strobe will be enabled during fault analysis. Possible values are <code>no</code> and <code>yes</code> .                                                                                                                                          |
| <code>faultmethod=linear</code>               | Simulation method used for transient fault analysis. Possible values are <code>linear</code> , <code>maxiters</code> , <code>onestop</code> , <code>leadtime</code> , and <code>timezero</code> . The default value is <code>linear</code> .                 |
| <code>faulttablefmt=[txt   bin]</code>        | Format of the fault table file. Possible values are <code>txt</code> and <code>bin</code> .                                                                                                                                                                  |
| <code>faultsid=[...]</code>                   | Indexes of faults from the list to perform transient fault analysis. If specified, simulation is performed for the requested subset of fault list.                                                                                                           |

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|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>faultsname=[...]</code>       | Name of faults from the list to perform transient fault analysis. If specified, simulation is performed for the requested subset of fault list.                                                                                                                                                                                                                                                                                                                                                                 |
| <code>faultsinst=[...]</code>       | List of instances to perform transient fault analysis. If specified, simulation is performed only for faults within given instances.                                                                                                                                                                                                                                                                                                                                                                            |
| <code>faultsamplenum</code>         | Number of samples in simple random sampling of fault list during simulation.                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <code>faultsamplratio</code>        | <p>A set of two values R1 and R2 to simulate the samples between the given range. Each value is the number of random samples (in percentage) out of the total fault count in the list.</p> <p><code>faultsamplratio=R</code> is equivalent to <code>faultsamplratio=[0 R]</code>.</p>                                                                                                                                                                                                                           |
| <code>faultseed=1</code>            | Optional starting seed for random number generator during fault sampling.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <code>faultsamplmethod</code>       | Method to be used for fault sampling. Possible values are <code>random</code> , <code>randomweighted</code> , <code>randomuniform</code> , and <code>weightsorted</code> . Default is <code>random</code> .                                                                                                                                                                                                                                                                                                     |
| <code>faultsamplereplace=yes</code> | Perform fault sampling with sample replacement during fault analysis. Possible values are <code>no</code> and <code>yes</code> .                                                                                                                                                                                                                                                                                                                                                                                |
| <code>faultduplicate</code>         | <p>By default, duplicate faults are included in all fault lists when multiple <code>info</code> analyses are specified for fault generation. This parameter lets you choose whether or not to include duplicate faults.</p> <p>Possible values are:</p> <ul style="list-style-type: none"><li>■ <code>yes</code>: The tool performs fault simulation for all fault from the list. This is the default value.</li><li>■ <code>no</code>: Identical and equivalent faults are excluded from simulation.</li></ul> |
| <code>faultsort</code>              | Perform fault simulation according to the order given in the fault list. If set to <code>no</code> , random order applied. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>yes</code> .                                                                                                                                                                                                                                                                                   |
| <code>faultcollapse</code>          | Perform bridge fault collapsing in the list before fault simulation. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>no</code> .                                                                                                                                                                                                                                                                                                                                          |

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|                                   |                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>faultsave</code>            | Set of data to be saved during transient fault analysis. Possible values are <code>testpoints</code> , <code>all</code> , and <code>none</code> . The default value is <code>testpoints</code> .                                                                                                                                                    |
| <code>faultddm</code>             | File containing the command line options to run <code>spectre_ddmrpt</code> when fault simulation is finished.                                                                                                                                                                                                                                      |
| <code>faultdb</code>              | File name to save fault simulation data in the format specified by <code>faultfmt</code> .                                                                                                                                                                                                                                                          |
| <code>faultfmt</code>             | File format to save fault simulation data. Possible values are <code>csv</code> , <code>xl</code> , and <code>sql</code> .                                                                                                                                                                                                                          |
| <code>faultleadtime=[...]s</code> | The lead time intervals where the fault will be injected before the fault time when <code>faultmethod=leadtime</code> .                                                                                                                                                                                                                             |
| <code>faultmaxiters</code>        | Maximum number of iterations per time step for transient fault analysis. The default value is 50 for fault method <code>maxiters</code> , 10 for <code>onestep</code> , and 5 for other methods.                                                                                                                                                    |
| <code>faultlimsteps</code>        | Exit the slow simulation automatically for the faults taking above average number of time steps. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>yes</code> .                                                                                                                                                 |
| <code>faultlimtime</code>         | Maximum elapsed time allowed to perform one fault simulation (in hours). The simulation exits if it does not finish earlier than the specified time.                                                                                                                                                                                                |
| <code>faultsafecheck</code>       | Enable autostop during the nominal simulation when the assert with <code>safecheck</code> specified has been violated. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>no</code> .                                                                                                                            |
| <code>faultreorder</code>         | Enable matrix reordering during transient fault analysis. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>no</code> .                                                                                                                                                                                         |
| <code>faultreadic</code>          | Specifies the file that contains the initial conditions for transient fault analysis.                                                                                                                                                                                                                                                               |
| <code>faulttrampsteps</code>      | Maximum number of steps for fault conductance stepping to improve convergence after fault injection with method <code>maxiters</code> .                                                                                                                                                                                                             |
| <code>faulttrampinterval</code>   | <p>The coefficient (between 0 and 1) to define the size of time interval to ramp fault conductance after fault injection when <code>faultmethod=leadtime</code> is specified. The default value is 0.</p> <p>The tool ramps up the conductance for open faults and ramps it down for bridges. This option is not compatible with custom faults.</p> |

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|                           |                                                                                                                                                                                                                                                              |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>faultic</code>      | Perform dc analysis after the fault injection as an initial condition for each fault transient simulation. Possible values are <code>no</code> , <code>bridge</code> , <code>open</code> , <code>custom</code> , <code>param</code> , and <code>all</code> . |
| <code>maxstepratio</code> | Maximum time step ratio for custom <code>errpreset</code> .                                                                                                                                                                                                  |
| <code>reltolratio</code>  | Reltol ratio for custom <code>errpreset</code> .                                                                                                                                                                                                             |
| <code>faultstrobe</code>  | Time point strobe will be enabled during fault analysis. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>no</code> .                                                                                                   |

When the value of the `faultstrobe` parameter is set to `yes`, parameters given in the table below can be used to output the fault simulation points into a fault table file. With the `leadtime` or `timezero` method, Spectre saves only `faulttimes=[]` into a fault table file although fault simulation is run over some time intervals (for example, `faultleadtime` interval for `leadtime`, and full transient time for `timezero`). You can use `faultstrobe=yes` and the `strobestart|strobestop|strobestep|strobeperiod` parameters to save additional strobe points into the fault table to save the simulation without injecting the faults too many times.

|                                                |                                                                                                                                                    |
|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>strobestart strobestop strobestep</code> | Spectre saves the strobing time points into table file during fault analysis when <code>faultstrobe=yes</code> .                                   |
| <code>strobeperiod</code>                      | Spectre saves the strobe interval (in seconds) into a table file during fault analysis when <code>faultstrobe=yes</code> . The default value is 0. |
| <code>skipstart</code>                         | The time to start skipping of output data during fault analysis when <code>faultstrobe=yes</code> . The default value is 0.                        |
| <code>skipstop</code>                          | The time to stop skipping of output data during fault analysis when <code>faultstrobe=yes</code> . The default value is 0.                         |

**Note:** `strobestart`, `strobestop`, and `strobestep` are the same as `skipstart`, `skipstop`, and `strobeperiod`.

The parameter `skipstart` may contain several time points specified incrementally and `strobeperiod` is applied to every `skipstart` value. For example, when `skipstart=[1n 2n 3n]` and `strobeperiod=10n`, then the strobing time points are `1n`, `2n`, `3n`, `11n`, `12n`, `13n`, `21n`, and so on.

## Selecting the Fault Analysis Method

The choice of fault simulation method can be specified using the `faultmethod=[method]` parameter in Spectre transient analysis. Possible values for `faultmethod` are: `linear`, `maxiters`, `onestep`, `leadtime`, and `timezero`.

The unique technology of Spectre's transient fault analysis, which allows to speed up the performance, is based on temporary fault injection, only in the vicinity of the fault times during transient simulation. When fault-free simulation reaches the fault time, the state of faultless circuit is saved and used as an initial guess for the fault injected circuit. Fault simulation starts at the time point with the method set in the transient analysis statement.

The following methods are supported in transient fault analysis.

### ■ `faultmethod=linear`

With a fault injected, Spectre simulates one time step at the fault time and limits the number of Newton iterations to one. Simulation interrupted early allows you to estimate the sensitivity of the design to a particular fault at the given time point. This is the default method and has the fastest performance for fault analysis with limited accuracy. This is the default method.

### ■ `faultmethod=maxiters`

Spectre integrates the time step at the fault time taking multiple Newton iterations till it converges or `faultmaxiters` is reached. The default value is 50 for `maxiters`, 10 for `onestep`, and 5 for other methods. You can use the `faultrampsteps` parameter with `maxiters` to improve convergence and reduce the number of iterations required. The resistance of the injected bridge is ramped gradually from a large value to the value specified in the fault list. The recommended value for `faultrampsteps` is 10.

### ■ `faultmethod=onestep`

This method performs as `maxiters` initially. However, if the simulation does not converge, it reduces the time step and continues the iterations until a solution is found. Multiple time steps may be needed in some situations, which may affect the simulation performance.

### ■ `faultmethod=leadtime`

When higher accuracy is needed, defect should be taken into consideration prior to each fault time with the time interval of `faultleadtime`. For one of the fault time points, for example, `faulttime_i`, the fault is injected at `(faulttime_i-faultleadtime)`, and Spectre performs the transient fault simulation by using the Newton iteration and time step control till `faulttime_i` is reached. The `faultleadtime` parameter specifies the leading time intervals where the fault is injected before the fault times when `faultmethod=leadtime`.



- ❑ `faultleadtime=val`: Specifies constant lead time for all fault times
- ❑ `faultleadtime=[val1 val2 val3]`: Specifies different lead times for different points. If the number of fault times is greater than the number of specified intervals, the last lead time is applied for the remaining points.

The optional parameter `faultrampinterval` can be used with the `faultleadtime` method. This coefficient (between 0 and 1) defines the portion of the lead time interval to ramp up the fault conductance after the fault injection to improve convergence. The default value is 0.25.

By default, Spectre uses the nominal simulation states as initial conditions for each fault to start the fault simulation. However, it is difficult to converge to the correct value when the actual fault result is far away from the nominal value. You can use `faultic=yes` to enable Spectre to perform dc analysis after the fault injection to find better initial conditions instead of the nominal solution. Possible values are `no`, `bridge`, `open`, `custom`, `param`, and `all`.

## ■ `faultmethod=timezero`

The fault is injected at time zero and a complete transient fault analysis is performed for every time step. However, the faulty result is saved only at the required fault times. This is the most accurate mode; however, the simulation takes much longer.

The following table provides a comparison of the different fault methods:

| Method                                      | Linear        | maxiters            | onestep                                                                    | leadtime                                                           | timezero                                             |
|---------------------------------------------|---------------|---------------------|----------------------------------------------------------------------------|--------------------------------------------------------------------|------------------------------------------------------|
| Time steps/ iterations with fault injection | One iteration | Multiple iterations | Time step at fault time, or multiple steps (if current step gets rejected) | All time steps within the interval [faulttime-leadtime, faulttime] | All time steps starting from time zero to fault time |
| Accuracy                                    | Lowest        | Low                 | Middle                                                                     | High                                                               | Highest                                              |
| Performance                                 | Highest       | High                | Middle                                                                     | Low                                                                | Lowest                                               |

## Generating the Defect Detection Matrix Report Based on Fault Table File

To screen the defect devices out of high volume production, it is important to select the effective fault times to measure the critical ports and signals during transient fault analysis.

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The tested signals, ports, or currents can be specified using the `save` statement or measurement definition, just like the transient, dc, and sweep simulation. You can choose to save the complete set of fault analysis results, or the results at each fault time only. This can be controlled by the option `faultsave` whose default value is `testpoints`.

```
faultsave=[testpoints|all|none]
```

By default, fault analysis saves the fault simulation results only at the fault times and stores them in the `tran_faults.tran` file. When `faultsave=all`, the `fault_timestep.tran` file is saved in addition to the fault time data. It is recommended not to use `faultsave=all` for large fault lists because it occupies a lot of disk space. In addition, `faultsave=all` works for all methods except `linear`.

You can use the `faultsave=none` option to avoid any simulation slowdown due to waveform saving and also reduce the disk space usage. Simulation results are saved only in the fault table file.

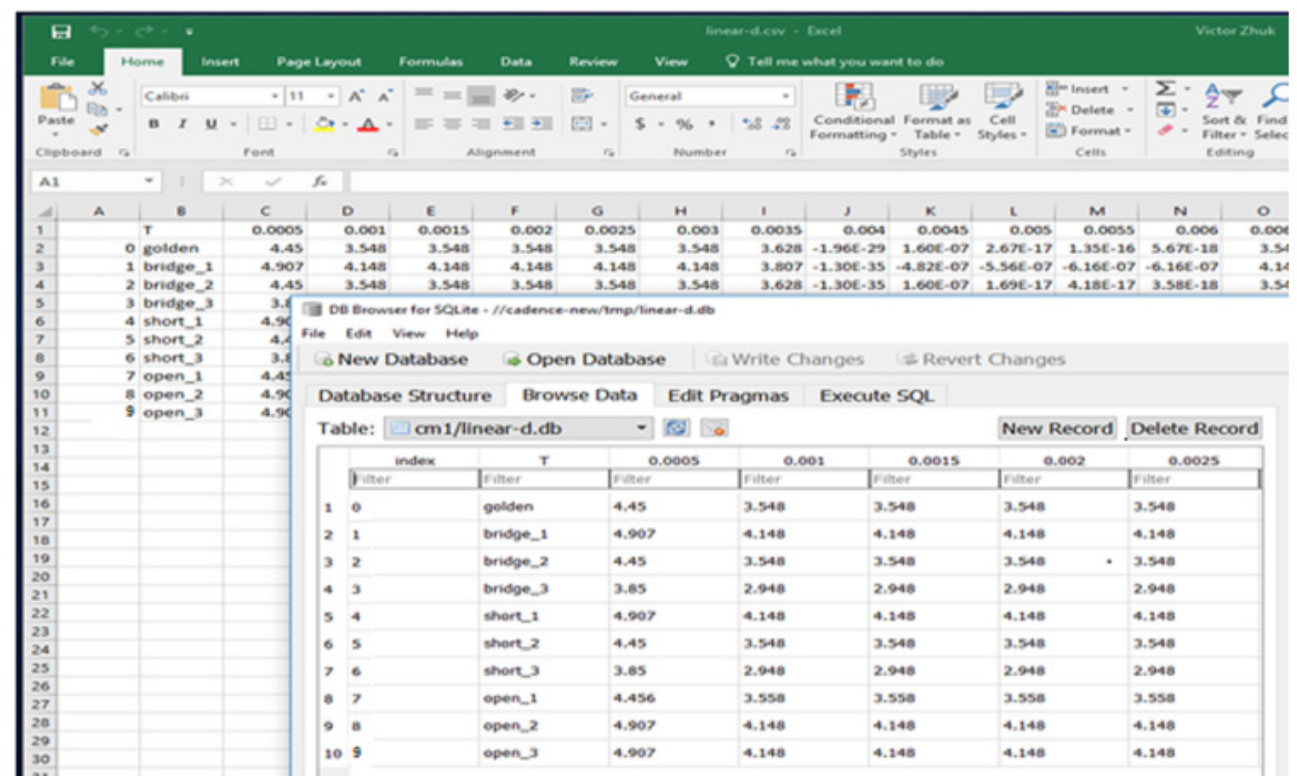
You can use the following two parameters (supported in both DFA and TFA) to choose the format in which to save the file:

- `faultfmt`: File format to save the fault simulation data. Possible values are `csv`, `xl`, and `sql`.
- `faultdb`: File name to save the fault simulation data in the format specified using `faultfmt`.

The following figure shows the sample fault simulation data generated using the above parameters for both formats. The tables are generated as fault IDs/names vs. fault times. For

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each test port (saved signal), a separate file is generated. The name of the signal is added as a suffix to the faultdb name.



## Assert Checking and Autostop in Transient Fault Analysis

Assert checking (see [Assert Checking](#)) evaluates the violation continuously over the transient time. Transient fault analysis does the same for fault methods `timezero` and `leadtime`. For `linear`, `maxiters` and `onestep`, Spectre evaluates the assert checking only at fault times.

You can enable autostop by using the option `faultautostop=func|check|both|all` based on the detection of assert violation.

Assert detection is saved in a transient fault table file to provide assert compatibility for direct fault analysis.

Single Point Fault (SPF) and Latent Faults (multiple points) are also applied to Transient Fault Analysis.

## Getting Started with Transient Fault Analysis

### *Preparing and Starting Transient Fault Analysis*

Spectre transient fault analysis requires a complete simulation test bench with fault list, fault time(s), test signal(s)/port(s), and the fault method defined using the `tran` analysis statement. Fault analysis is ignored when this critical information is missing. To perform transient fault analysis, you need to perform the following:

- Specify the test signals/ports to be checked using the `save` statement, as shown below.

```
save d g s
```

- Specify the fault times and fault method and some of the faults in the transient statement, as shown below.

```
leadtime tran start=0 stop=12e-3 errpreset=conservative maxiters=5
+ faults=[fault_bridges fault_opens]
+ faultstname=[fault_bridges_bridge_6 fault_bridges_bridge_1
...
...
+ faulttimes=[2.5m 5.5m 7.5m]
+ faultmethod=leadtime faultleadtime=0.1m
```

**Note:** The `faultstop` time must not be beyond the transient stop time.

- Run the simulation, as shown below.

```
%spectre report_tfa_leadtime.scs +l tfa_leadtime.log -outdir out_ddm_tfa/
```

**Note:** The command-line option to run the fault simulation is the same as transient simulation. All the commands to adjust accuracy and performance for transient simulation are also applied to transient fault simulation.

- To run a full fault simulation with the faults injected at time zero and enable autostop, use the examples of the transient statement and the Spectre command, as shown below.

```
timezero tran start=0 stop=12e-3 errpreset=conservative maxiters=5 +
.....
+ faulttimes=[7.5m] faultmethod=timezero
+ faultautostop=all
%spectre tfa_timezero_autostop.scs -outdir out_tfa_autostop/
```

### *Viewing Data Output of Transient Fault Analysis*

In the log file, the list of faults is reported in circuit inventory, as shown below.

Circuit inventory:

|          |   |
|----------|---|
| nodes    | 6 |
| mos11010 | 1 |

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```
resistor 5
vsource 2
Design checks inventory:
 bridge 10
 assert 3
 open 12
Fault parameter values:
 faultmethod = leadtime
 faultleadtime = 100 us
 faulttimes = [5 ms 5.5 ms 6 ms 6.5 ms]
```

The Spectre log file also reports the transient fault simulation by printing the fault numbers which failed to converge at every fault time(s). The counting of time step for each fault is also monitored and printed. If the counting is too large, Spectre switches the `faultmethod` to `maxiters` automatically.

The following is an example of the Spectre log file:

```

Transient Analysis `leadtime': time = (0 s -> 12 ms)

Opening the PSF file out_faults/test_fault.raw/leadtime.tran.tran ...
Important parameter values:
 start = 0 s
 outputstart = 0 s
 stop = 12 ms
 step = 12 us
 maxstep = 120 us

 relref = alllocal
 cmin = 0 F
 gmin = 1 fS
 rabssshort = 1 mOhm
... ..
leadtime: time = 300.5 us (2.5 %), step = 3.067 us (25.6 m%)
leadtime: time = 926.3 us (7.72 %), step = 63.13 us (526 m%)
leadtime: time = 1.526 ms (12.7 %), step = 120 us (1 %)
leadtime: time = 2.126 ms (17.7 %), step = 120 us (1 %)
leadtime: time = 2.726 ms (22.7 %), step = 120 us (1 %)
leadtime: time = 3.3 ms (27.5 %), step = 6.726 us (56.1 m%)
leadtime: time = 3.942 ms (32.8 %), step = 58.15 us (485 m%)
 Transient fault analysis started at fault time 5 ms.
```

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Fault analysis for fault\_bridges\_bridge\_1 : 2 time steps

Fault analysis for fault\_bridges\_bridge\_2 : 5 time steps

Fault analysis for fault\_bridges\_bridge\_3 : 2 time steps

Fault analysis for fault\_opens\_open\_1 : 2 time steps

Fault analysis for fault\_opens\_open\_2 : 9 time steps

Fault analysis for fault\_opens\_open\_3 : 2 time steps

Transient fault analysis finished at time 5 ms : 6 (100.00%) simulations succeeded.

leadtime: time = 5.1 ms (42.5 %), step = 200 us (1.67 %)

Transient fault analysis started at fault time 5.5 ms.

Fault analysis for fault\_bridges\_bridge\_1 : 3 time steps

Fault analysis for fault\_bridges\_bridge\_2 : 6 time steps

Fault analysis for fault\_bridges\_bridge\_3 : 3 time steps

Fault analysis for fault\_opens\_open\_1 : 3 time steps

Fault analysis for fault\_opens\_open\_2 : 15 time steps

Fault analysis for fault\_opens\_open\_3 : 3 time steps

Transient fault analysis finished at time 5.5 ms : 6 (100.00%) simulations succeeded.

leadtime: time = 5.815 ms (48.5 %), step = 120 us (1 %)

Transient fault analysis started at fault time 6 ms.

Fault analysis for fault\_bridges\_bridge\_1 : 3 time steps

Fault analysis for fault\_bridges\_bridge\_2 : 6 time steps

Fault analysis for fault\_bridges\_bridge\_3 : 3 time steps

Fault analysis for fault\_opens\_open\_1 : 3 time steps

Fault analysis for fault\_opens\_open\_2 : 15 time steps

Fault analysis for fault\_opens\_open\_3 : 3 time steps

Transient fault analysis finished at time 6 ms : 6 (100.00%) simulations succeeded.

leadtime: time = 6.302 ms (52.5 %), step = 5.143 us (42.9 m%)

Transient fault analysis started at fault time 6.5 ms.

Fault analysis for fault\_bridges\_bridge\_1 : 11 time steps

If some of the faults from the list take more time steps than the average step count, Spectre, by default, terminates that simulation and generates a message in the log file, as shown below.

Warning from spectre at time = 79.024 us during transient analysis `Leadtime'.

WARNING (SPECTRE-16872): Transient fault simulation is too slow for b\_X123\_fault\_2 and was terminated at time 100 us.

This approach, along with `faultlimsteps=yes`, allows you to avoid situations when some run sticks with minimal time stepping, or a fault triggers oscillations and number of steps increase multifold, and therefore, one fault may take hours to finish. It is applied to the `leadtime` and `timezero` test methods; however, sometimes, you may see the same

warning message with the `onestep` method. You may note that the simulation finishes when the slow fault is run separately because of no average step count recorded.

To disable the termination of fault simulation due to slow performance, use the `faultlimsteps` parameter.

- `faultlimsteps=yes`: Exit the slow simulation automatically for the faults taking above average number of time steps. Possible values are `no` and `yes`. The default value is `yes`.
- `faultlimsteps=no`: Continue fault simulation even if it is slow.

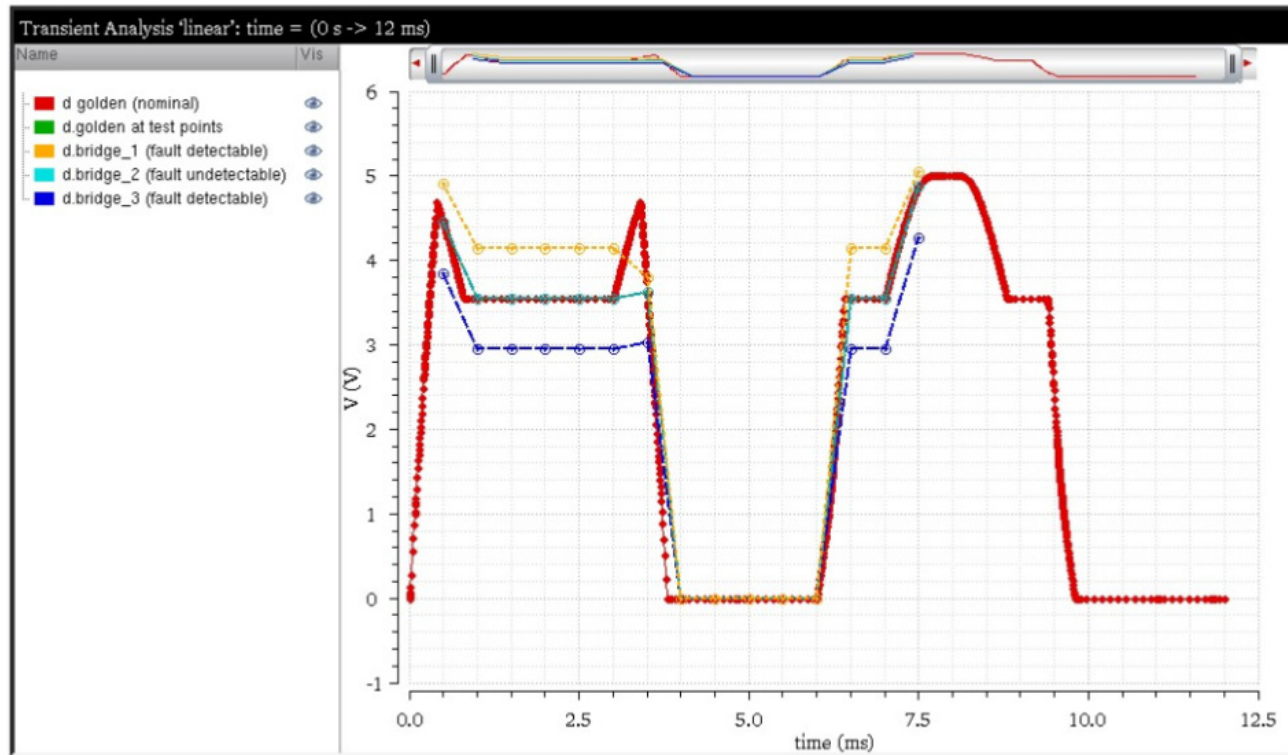
The data is saved in the raw directory (`out_test/tfa_test_fault.raw/`) with the following names in pairs:

- Transient analysis: `[TranName].tran.tran`, for example, `linear.tran.tran`
- Transient fault analysis: `[TranName_faults].tran`, for example, `linear_faults.tran`

The waveform plot below shows the fault data saved with the default setting `faultsave=testpoints`.

- The nominal transient (without faults) is consistent with the golden saved in the fault raw file only at fault times.

- The fault result of `bridge_2` is the same as golden data indicating that the fault is not detectable while `bridge_1` and `bridge_3` are off golden, which shows that the faults are detectable.



With the option `faultsave=all`, in addition to the above fault waveforms, extra files are generated for each fault at every fault time in the format `[FaultName-TestPointTime].tran.tran`. For example, `bridge_1-1.00e-03.tran.tran`. This option is not recommended because it generates a large data file.

In addition to the raw file, a textual fault table is generated with the name `[Netlist].[TranName].table`. For example, if the following statements are specified in the netlist,

```
leadtime tran start=0 stop=12e-3 faultstart=0.5m faultstep=0.5m faultstop=7.5m
+ faultmethod=leadtime faultleadtime=0.1m
```

```
linear tran start=0 stop=12e-3 faultstart=0.5m faultstep=0.5m +faultstop=7.5m
```

```
maxiters_rampstep tran start=0 stop=12e-3 faultstart=0.5m faultstep=0.5m
+faultstop=7.5m faultmethod=maxiters faulttrampsteps=10
```

```
onestep tran start=0 stop=12e-3 faultstart=0.5m faultstep=0.5m faultstop=7.5m +
faultmethod=onestep
```

the following four tables, corresponding to the four transient statements are generated in the `out_test` directory.



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```
tfa_test_fault.leadtime.table
tfa_test_fault.linear.table
tfa_test_fault.maxiters_rampstep.table
tfa_test_fault.onestep.table
```

## ***Post-Processing of Table File for Detection Matrix***

Spectre installation contains an executable file `spectre_ddmrpt` that evaluates the fault table file and generates the defect detection matrix. `spectre_ddmrpt` reads the fault result and compares the data with the nominal value. A fault is detected when the difference is greater than the tolerance. The criteria are set based on the relative (`-r`) and absolute (`-a`) tolerance in the command parameters.

The simplified use model is shown below.

```
spectre_ddmrpt [-h] [-t TIMEPTS] [-s SIGNALS] [-a ABSTOL] [-r RELTOL]
 [-m MERGE [MERGE ...]] [-o OUTPUT] [-p] [-cl CL] [-q]
 [--ct] [--ce] [--cd CSVDET] [--cs CSVSOL] [--xd XLSXDET]
 [--xs XLSXSOL] [--sd SQLDET] [--ss SQLSOL] [--td TXTDET]
 [--ts TXTSOL] [-D DET] [-G UNDET] [-N ERRFAULT]
 [-A AUTOSTOP] [-oe OCEAN] [-rf RESULTS_FILE]
 [-cf CALC_FILE] [-vf VAR_FILE] [-raw RAW_DIR] [--er ELEMREPORT]
 [--du DEFECTUNIV] [-O OCEAN_OUTPUT_FILE] [-P OUTDIR]
 FILES [FILES ...]
```

The following criteria are used to determine whether the fault is detected. The default value for `ABSTOL` is 0.005 and `RELTOL` is 5%.

```
delta(fault_result - nominal_result) >= ABSTOL (5m) + RELTOL (5%) * nominal_result
```

The values 0 and 1 for the iterations have a special meaning in the table file. All the signals are marked as `N` for the value 0 if the simulation fails due to convergence issues or is terminated. The signals are marked as `D` for the value 1 if the simulation is autostopped due to assert violation.

The untestable signal saved as `N` is not counted in the detection coverage rate. If there is a need to include it, use the option `--coverr`, as shown below.

```
.../bin/spectre_ddmrpt --coverr out_ddm_tfa/tfa.leadtime.table -o report_ddm
```

To generate the defect coverage based on hierarchy or design scope in the netlist, you can apply the scope parameters `-i` to include or `-x` to exclude a subset of the fault list that belongs to the specified subcircuit instances.

```
spectre_ddmrpt inp.table --inst "X1 Xa*"
spectre_ddmrpt inp.table --xinst "X1.X*"
```

Report of defect coverage can be generated by a subset of faults whose names start with the specified prefix or matching the specified wildcard string.

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```
%../bin/spectre_ddmrpt top.table -b "bridgeFaults*" -o myreport_block.txt
```

You can generate the defect detection matrix report automatically right after the fault simulation. You can define any option for running `spectre_ddmrpt` in a file, for example, `ddm_options.txt` and set `faultddm=ddm_options.txt`. Once the fault simulation is performed, `spectre_ddmrpt` is started automatically to generate the report with the options.

In `ddm_options.txt` file, the following are defined where the absolute value of 0.04V and relative value of 5% are used for generating the report.

```
-a 0.04 -r 0.05
```

In the end of the Spectre log file, the command to run the defect detection report is shown as the following messages.

```
Processing fault analysis data:
```

```
../bin/spectre_ddmrpt fault_sim/myOPAMP.tranFault.table -a 0.04 -r 0.05
-o fault_sim/myOPAMP.tranFault.ddmrpt -q
```

The report name is generated in the format `[Netlist].[TranName].ddmrpt`.

`spectre_ddmrpt` also performs the following tasks:

- Output or save the detection matrix into `csv`, `xls`, or `sql` format for every test port, when the detection limit has the simple form as percentage difference from nominal (golden) solution
- Compares the detection accuracy of several simulations saved in the table files and outputs the fault detection summary for a given test port, when the detection limit has the simple form as percentage difference from nominal (golden) solution
- Transform the table data into `csv`, `xls`, or `sql` format (similar to the `faultddb` parameter in a transient statement)

You can use the following command to find the description of all the available options:

```
%../bin/spectre_ddmrpt -h
```

Below are some examples of the usage of `spectre_ddmrpt`.

**Note:** It is assumed that the transient fault simulation has been performed and the `tfa_test_fault.linear.table` file exists.

1. `%../bin/spectre_ddmrpt tfa_test_fault.linear.table --cs SOL -s d`

The above command processes the `tfa_test_fault.linear.table` file and saves all solutions for signal `d` into a `SOL.csv` file with the following annotations:

```
Time Points: 0.0005, 0.0045, 0.0075
```

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Signals: d

Detection Matrix:

|          | 0.0005/d | 0.0045/d | 0.0075/d | Total  |
|----------|----------|----------|----------|--------|
| bridge_1 | D        | G        | G        | D      |
| bridge_2 | G        | G        | G        | G      |
| bridge_3 | D        | G        | D        | D      |
| open_1   | G        | D        | G        | D      |
| open_2   | D        | G        | G        | D      |
| open_3   | D        | G        | G        | D      |
| Coverage | 66.67%   | 16.67%   | 16.67%   | 83.33% |

Solution Matrix:

|          | 0.0005/d | 0.0045/d   | 0.0075/d |
|----------|----------|------------|----------|
| nominal  | 4.45     | 1.6e-07    | 4.874    |
| bridge_1 | 4.907    | -3.857e-07 | 5.058    |
| bridge_2 | 4.45     | 1.6e-07    | 4.874    |
| bridge_3 | 3.85     | 3.186e-09  | 4.274    |
| open_1   | 4.456    | -1.391e-06 | 4.876    |
| open_2   | 4.908    | -3.874e-07 | 5.063    |
| open_3   | 4.907    | -3.856e-07 | 5.059    |

Legend:

- G - Good, measurement consistent with fault-free circuit within error bound
- D - Detected with violations of error bound
- N - Not testable (error occurred during analysis, e.g. non-convergence)
- - Unevaluated

Solution matrix saved to SOL.csv.

The new SOL.csv file can be used to apply more advanced detection rules using Excel features.

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If you have two or more table files (for example, `tfa_test_fault.tmezero.table`, `tfa_test_fault.linear.table`, and `tfa_test_fault.onestep.table`) that result from several fault simulations under the same conditions (same fault times and test ports) but with different methods, or different set of simulation parameters, you can compare the detection accuracy by taking the first table file as reference.

2. `%.../bin/spectre_ddmrpt tfa_test_fault.timezero.table tfa_test_fault.linear.table tfa_test_fault.onestep.table -s g -t 1.5e-3 -r 5`

This command compares the detection with 5% limit for signal `g` and testpoint at `1.5e-3`, and generates the following output:

Files: `test_fault.leadtime.table` (Golden), `test_fault.onestep.table` (Measured-1), `test_fault.maxiters_rampstep.table` (Measured-2)

\*\*\* Analysis 1 Time Point: 0.0015 Signal: g \*\*\*

Summary:

|              | Measured-1   | Measured-2   |
|--------------|--------------|--------------|
| Matched      | 6 (100.00% ) | 6 (100.00% ) |
| Missed       | 0 ( 0.00% )  | 0 ( 0.00% )  |
| False Detect | 0 ( 0.00% )  | 0 ( 0.00% )  |

Detection Matrix:

|          | Golden | Measured-1 | Matching-1 | Measured-2 | Matching-2 |
|----------|--------|------------|------------|------------|------------|
| bridge_1 | G      | G          | Matched    | G          | Matched    |
| bridge_2 | G      | G          | Matched    | G          | Matched    |
| bridge_3 | G      | G          | Matched    | G          | Matched    |
| open_1   | G      | G          | Matched    | G          | Matched    |
| open_2   | G      | G          | Matched    | G          | Matched    |
| open_3   | G      | G          | Matched    | G          | Matched    |

Legend:

G - Good, measurement consistent with fault-free circuit within error bound

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|   |                                                                       |
|---|-----------------------------------------------------------------------|
| D | - Detected with violations of error bound                             |
| N | - Not testable (error occurred during analysis, e.g. non-convergence) |
| - | - Unevaluated                                                         |

Here, `Matched` confirms that the detection status is similar to the reference (the first column). `Missed` means that this particular defect was not detected during the simulation unlike the reference data. `False_Detect` is set to mark the false detection, when the defect was detected despite not being in reference.

Using the file format options in the command line, you can save the matching data and solutions into `csv`, `xlsx`, or `sql` files. The file with the solutions can be used to compare the results with more realistic detection limits applying Excel or SQL functionality.

### ***Merging the Defect Detection Report***

When the detection criteria are different for different signals saved in the table file, you can post-process the signal subsets based on the same criterion, and then merge the partial reports with the same fault list. The final report will contain the coverage rate re-calculated for all signals under consideration. To merge the reports, each partial report should be generated in one of `csv`, `xlsx`, or `sql (db)` formats.

```
.../spectre_ddmrpt noSampling.tran.table -s IDDOUT -t 2.3e-6 -a 1e-6 \
--xd report_ddmrpt_1 -o text_ddmrpt_1.txt

.../spectre_ddmrpt noSampling.tran.table -s DELAY -t 2.3e-6 -a 5e-8 \
--xd report_ddmrpt_2 -o text_ddmrpt_2.txt
```

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```
.../spectre_ddmrpt report_ddmrpt_1.xlsx report_ddmrpt_2.xlsx \
-o report_ddmrpt_final.txt
```

Time Points: 2.3e-06  
 Signals: IDDOUT  
 Detection absolute tolerance: 1e-6  
 Total Defects: 30  
 Simulated: 10

Detection Matrix:

|                       | 2.3e-06/IDDOUT | Total  | Likelihood |
|-----------------------|----------------|--------|------------|
| OPAMP1_bsim_bridge_1  | G              | G      | 0.0728914  |
| OPAMP1_bsim_bridge_4  | D              | D      | 0.116626   |
| OPAMP1_bsim_bridge_7  | G              | G      | 0.0831902  |
| OPAMP1_bsim_bridge_8  | G              | G      | 0.0728914  |
| OPAMP1_bsim_bridge_9  | G              | G      | 0.029277   |
| OPAMP1_bsim_bridge_15 | D              | D      | 0.0265662  |
| OPAMP1_bsim_bridge_17 | D              | D      | 0.116626   |
| OPAMP1_bsim_bridge_22 | G              | G      | 0.160901   |
| OPAMP1_bsim_bridge_27 | G              | G      | 0.029277   |
| OPAMP1_bsim_bridge_28 | G              | G      | 0.00975901 |
| Weighted Coverage     | 36.19%         | 36.19% | 0.718005   |

Time Points: 2.3e-06  
 Signals: DELAY  
 Detection absolute tolerance: 5e-8  
 Total Defects: 30  
 Simulated: 10

Detection Matrix:

|                       | 2.3e-06/DELAY | Total  | Likelihood |
|-----------------------|---------------|--------|------------|
| OPAMP1_bsim_bridge_1  | D             | D      | 0.0728914  |
| OPAMP1_bsim_bridge_4  | D             | D      | 0.116626   |
| OPAMP1_bsim_bridge_7  | D             | D      | 0.0831902  |
| OPAMP1_bsim_bridge_8  | D             | D      | 0.0728914  |
| OPAMP1_bsim_bridge_9  | D             | D      | 0.029277   |
| OPAMP1_bsim_bridge_15 | G             | G      | 0.0265662  |
| OPAMP1_bsim_bridge_17 | G             | G      | 0.116626   |
| OPAMP1_bsim_bridge_22 | D             | D      | 0.160901   |
| OPAMP1_bsim_bridge_27 | D             | D      | 0.029277   |
| OPAMP1_bsim_bridge_28 | G             | G      | 0.00975901 |
| Weighted Coverage     | 78.70%        | 78.70% | 0.718005   |

|    | Defects               | 2.3e-06/IDDOUT | 2.3e-06/DELAY | Total  | Likelihood |
|----|-----------------------|----------------|---------------|--------|------------|
| 0  | OPAMP1_bsim_bridge_1  | G              | D             | D      | 0.072891   |
| 1  | OPAMP1_bsim_bridge_4  | D              | D             | D      | 0.116626   |
| 2  | OPAMP1_bsim_bridge_7  | G              | D             | D      | 0.083190   |
| 3  | OPAMP1_bsim_bridge_8  | G              | D             | D      | 0.072891   |
| 4  | OPAMP1_bsim_bridge_9  | G              | D             | D      | 0.029277   |
| 5  | OPAMP1_bsim_bridge_15 | D              | G             | D      | 0.026566   |
| 6  | OPAMP1_bsim_bridge_17 | D              | G             | D      | 0.116626   |
| 7  | OPAMP1_bsim_bridge_22 | G              | D             | D      | 0.160901   |
| 8  | OPAMP1_bsim_bridge_27 | G              | D             | D      | 0.029277   |
| 9  | OPAMP1_bsim_bridge_28 | G              | G             | G      | 0.009759   |
| 10 | Weighted Coverage     | 36.19%         | 78.70%        | 98.64% | 0.718005   |

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**Note:** Reports based on random sampling are not compatible with report merging.

Another possibility to combine multiple reports is that reports are generated based on the fault simulation with the same design and detection limit but different fault lists.

```
.../spectre_ddmrpt test_tfa_faultlist1/report_tfa_1.leadtime.table \
-s d -t 7.5e-3 --xd report_ddmrpt_f1 -o text_ddmrpt_f1.txt
.../spectre_ddmrpt test_tfa_faultlist2/report_tfa_2.leadtime.table \
-s d -t 7.5e-3 --xd report_ddmrpt_f2 -o text_ddmrpt_f2.txt
.../spectre_ddmrpt report_ddmrpt_f1.xlsx report_ddmrpt_f2.xlsx \
-o report_ddmrpt_fullList.txt
```

Time Points: 0.0075  
Signals: d  
Detection absolute tolerance: 1e-06  
Total Defects: 10

Detection Matrix:

|                         |   | 0.0075/d | Total     | Likelihood |
|-------------------------|---|----------|-----------|------------|
| fault_bridges_bridge_1  | G | G        | 0.0833333 |            |
| fault_bridges_bridge_2  | G | G        | 0.0833333 |            |
| fault_bridges_bridge_3  | D | D        | 0.0833333 |            |
| fault_bridges_bridge_4  | G | G        | 0.166667  |            |
| fault_bridges_bridge_5  | G | G        | 0.166667  |            |
| fault_bridges_bridge_6  | G | G        | 0.0833333 |            |
| fault_bridges_bridge_7  | D | D        | 0.0833333 |            |
| fault_bridges_bridge_8  | D | D        | 0.0833333 |            |
| fault_bridges_bridge_9  | D | D        | 0.0833333 |            |
| fault_bridges_bridge_10 | G | G        | 0.0833333 |            |
| Weighted Coverage       |   | 33.33%   | 33.33%    | 1          |

Time Points: 0.0075  
Signals: d  
Detection absolute tolerance: 1e-06  
Total Defects: 8

Detection Matrix:

|                    |   | 0.0075/d | Total     | Likelihood |
|--------------------|---|----------|-----------|------------|
| fault_opens_open_1 | G | G        | 0.0833333 |            |
| fault_opens_open_2 | D | D        | 0.166667  |            |
| fault_opens_open_3 | G | G        | 0.166667  |            |
| fault_opens_open_4 | D | D        | 0.166667  |            |
| fault_opens_open_5 | G | G        | 0.166667  |            |
| fault_opens_open_6 | G | G        | 0.0833333 |            |
| fault_opens_open_7 | D | D        | 0.0833333 |            |
| fault_opens_open_8 | G | G        | 0.0833333 |            |
| Weighted Coverage  |   | 41.67%   | 41.67%    | 1          |

|    | Defects                 | 0.0075/d | Total  | Likelihood |
|----|-------------------------|----------|--------|------------|
| 0  | fault_bridges_bridge_1  | G        | G      | 0.0833333  |
| 1  | fault_bridges_bridge_2  | G        | G      | 0.0833333  |
| 2  | fault_bridges_bridge_3  | D        | D      | 0.0833333  |
| 3  | fault_bridges_bridge_4  | G        | G      | 0.166667   |
| 4  | fault_bridges_bridge_5  | G        | G      | 0.166667   |
| 5  | fault_bridges_bridge_6  | G        | G      | 0.0833333  |
| 6  | fault_bridges_bridge_7  | D        | D      | 0.0833333  |
| 7  | fault_bridges_bridge_8  | D        | D      | 0.0833333  |
| 8  | fault_bridges_bridge_9  | D        | D      | 0.0833333  |
| 9  | fault_bridges_bridge_10 | G        | G      | 0.0833333  |
| 10 | fault_opens_open_1      | G        | G      | 0.0833333  |
| 11 | fault_opens_open_2      | D        | D      | 0.166667   |
| 12 | fault_opens_open_3      | G        | G      | 0.166667   |
| 13 | fault_opens_open_4      | D        | D      | 0.166667   |
| 14 | fault_opens_open_5      | G        | G      | 0.166667   |
| 15 | fault_opens_open_6      | G        | G      | 0.0833333  |
| 16 | fault_opens_open_7      | D        | D      | 0.0833333  |
| 17 | fault_opens_open_8      | G        | G      | 0.0833333  |
| 18 | Weighted Coverage       | 37.50%   | 37.50% | 2          |

There may also be a situation in which you run the fault simulation for a long fault list, and some of them fail while most of them finish successfully. After making the change for the setup, you will need to rerun these failed faults and the updated fault detection can overwrite those in the existing report. The commands below show how it works. In addition, an example

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is available in the workshop under the installation. An alternative solution is to specify the faults in original netlist with `faultsid=[...]` to rerun.

First generate the detection report with following commands.

```
%spectre +aps input_tfa_leadtime.scs -o out_tfa_org/
%spectre_ddmrpt out_tfa_org/input_tfa_leadtime.tran.table -s VOUT \
-t 0.009 --cd cd_tfa_wiFail > report_tfa_wiFail.txt
```

Review the result and generate the faults that are not testable to be included for rerun.

```
%spectre_ddmrpt out_tfa_fail/input_tfa_leadtime_fakeN.tran.table -s VOUT \
-t 0.009 -N fault_notestable.scs --cd cd_tfa_wiFail >
report_tfa_wiFail_cd.txt
```

Once the fault simulation is done, the detection report is generated only for the faults that are rerun.

```
%spectre_ddmrpt out_tfa_rerun/input_tfa_leadtime_rerun.tran.table -s VOUT
-t 0.009 --cd cd_tfa_rerunInclu > report_tfa_rerunInclu_cd.txt
```

Merge the rerun detection in csv format into the original report to get the final detection report.

```
%spectre_ddmrpt cd_tfa_wiFail.csv cd_tfa_rerunInclu.csv >
report_tfa_final_cd_inclu.txt
```

### **Defect Detection Report According to IEEE P2427 Standard**

IEEE committee has proposed a standard for some typical devices. For example, the bridge faults take place at terminals of drain, gate, source for MOS device. Spectre provides you the flexibility to choose what terminal you want to select for bridges generation with parameter `faultterminals=[...]`.

In defect detection report (ddm report), Spectre follows the standard to list the coverage rate at the top of the report and separates the coverage rate for each type of the faults, shorts, opens and customs.

IEEE P2427 Summary:

| Defect Type | Defect Model | Detected | Undetected | Undetectable | Detectable Coverage | Weighting Function | Test Conditions |
|-------------|--------------|----------|------------|--------------|---------------------|--------------------|-----------------|
| Short       | 100hm        | 27       | 3          | -            | 90.00%              | w*1                |                 |
| Open        | 1G0hm        | 13       | 1          | -            | 92.86%              | w*1                |                 |
| Custom      | custom       | 0        | 0          | -            | 0                   | -                  |                 |



## Performing Autostop in Transient Fault Analysis

To enable the autostop feature in transient fault analysis, you have to define assert checking, as shown below.

```
LOAD_CAP2 assert safecheck=check expr="v(gg,g)" min=-8e-8 max=2.501 message="Load
Cap2_limit exceeded"
```

```
leadtime tran start=0 stop=12e-3 errpreset=conservative maxiters=5
```

```
+ faulttimes=[5m 6.5m] faultautostop=check
```

```
+ faultmethod=leadtime faultleadtime=0.1m faultsave=all
```

Once the assert violation is triggered, fault simulation is stopped automatically. The following messages are printed in the log file.

```

leadtime: time = 301.5 us (2.51 %), step = 6.612 us (55.1 m%)
leadtime: time = 980.6 us (8.17 %), step = 90.28 us (752 m%)
leadtime: time = 1.581 ms (13.2 %), step = 120 us (1 %)
leadtime: time = 2.181 ms (18.2 %), step = 120 us (1 %)
 Transient fault analysis started at fault time 2.5 ms.
 Fault analysis for fault_bridges_bridge_1 : 6 time steps

 Fault fault_bridges_bridge_6 detected with assert. Analysis terminated due to autostop at
 2.400390625 ms.

 Fault analysis for fault_bridges_bridge_7 : 13 time steps

 Fault fault_opens_open_7 detected with assert. Analysis terminated due to autostop at 2.400390625
 ms.

 Fault analysis for fault_opens_open_9 : 13 time steps
 Fault analysis for fault_opens_open_10 : 13 time steps
 Transient fault analysis finished at time 2.5 ms : 6 (100.00%) simulations succeeded.

```

Note that in the above report, both bridge\_6 and bridge\_7 are stopped automatically due to assert detection.

When the fault simulation is terminated due to `faultautostop=all`, the detection status and solution are annotated as unevaluated (-) when the test point is set later than the autostop time for the signal saved. However, the asserts keep the values for all the test points despite the autostop time because the violation has a continuous meaning.

The following report shows that autostop is triggered at 60us.

|                   | 5e-05/Iddq_pd | 0.0001/Iddq_pd | 0.00015/Iddq_pd | 0.0002/Iddq_pd | 0.00025/Iddq_pd |
|-------------------|---------------|----------------|-----------------|----------------|-----------------|
| func_s_bridge_1   | G             | G              | -               | -              | -               |
| func_s_bridge_2   | D             | D              | D               | D              | D               |
| func_s_bridge_3   | G             | G              | -               | -              | -               |
| func_s_bridge_4   | G             | G              | G               | G              | G               |
| func_s_bridge_5   | G             | G              | -               | -              | -               |
| Weighted Coverage | 16.67%        | 16.67%         | 16.67%          | 16.67%         | 16.67%          |

## Assert Compatibility

The assert violation results are saved in the fault table file, which is used to store the signals and currents specified in the `save` statement.

The following figure shows the fault result with asserts saved in the fault table file. The value 1 denotes that the fault is detected with the assert.

|                                         |           |           |           |            |          |          |           |            |            |
|-----------------------------------------|-----------|-----------|-----------|------------|----------|----------|-----------|------------|------------|
| parameters:nominal=0                    |           |           |           |            |          |          |           |            |            |
| Test_Points                             | g         | d         | gg        | s          | DEV_BIAS | LOAD_CAP | LOAD_CAP2 | resistance | iterations |
| 3.600000E-03                            | 6.250E-01 | 2.480E+00 | 1.250E+00 | 1.967E-03  | 0        | 0        | 0         | 1.602e+38  | 2          |
| 6.500000E-03                            | 2.500E+00 | 3.548E+00 | 5.000E+00 | 1.452E-01  | 0        | 0        | 0         | 1.602e+38  | 2          |
| 7.800000E-03                            | 7.648E-08 | 5.000E+00 | 3.553E-15 | -4.841E-10 | 0        | 1        | 0         | 1.602e+38  | 2          |
| 1: fault_bridges_bridge_1 ( 0 dd ) r=10 |           |           |           |            |          |          |           |            |            |
| 3.600000E-03                            | 6.250E-01 | 2.480E+00 | 1.250E+00 | 1.967E-03  | 0        | 0        | 0         | 10         | 2          |
| 6.500000E-03                            | 2.500E+00 | 3.548E+00 | 5.000E+00 | 1.452E-01  | 0        | 0        | 0         | 10         | 2          |
| 7.800000E-03                            | 7.647E-08 | 5.000E+00 | 3.553E-15 | -4.838E-10 | 0        | 0        | 0         | 10         | 2          |
| 2: fault_bridges_bridge_6 ( 0 g ) r=10  |           |           |           |            |          |          |           |            |            |
| 3.600000E-03                            | 1.225E-02 | 2.500E+00 | 1.250E+00 | 5.382E-10  | 0        | 0        | 0         | 10         | 2          |
| 6.500000E-03                            | 4.916E-02 | 4.995E+00 | 5.000E+00 | -7.037E-04 | 0        | 0        | 1         | 10         | 1          |
| 7.800000E-03                            | 2.896E-01 | 5.000E+00 | 5.792E-01 | 2.370E-06  | 0        | 0        | 0         | 10         | 1          |

For the `timezero` method, transient fault analysis evaluates the asserts with `safecheck` throughout the simulation.

For the `leadtime` method, transient fault analysis evaluates the asserts with `safecheck` within the leadtime interval in the simulation.

For `linear`, `maxiters`, and `onestep` methods, transient fault analysis evaluates the asserts with `safecheck` only at the fault times. In other words, for any given method, asserts with `safecheck` are evaluated at the same time point or for the same duration as the fault injection time point or duration for that method.

## Accuracy and Performance

Spectre transient fault analysis provides a wide range of methods and parameters to perform defect-oriented test simulation. The choice of an appropriate method depends on the size or simulation time of the nominal design, number of defects taken into consideration, accuracy pre-requirements, and CPU resources available. Other factors, such as high circuit sensitivity to some defects, may affect convergence significantly and slow down performance, and, as a result, force changing the method for fault analysis.

### ***Linear method***

`faultmethod=linear` is the default simulation method in Spectre. The simulation time in this case is comparable with the nominal simulation, and only for huge fault lists, it may affect performance.

The `linear` method is recommended for the initial evaluation of performance and defect detection. This is just a sensitivity approach, where the simulator provides the initial response of the circuit to a particular defect rather than the real solutions and waveforms. As a result, the linear method has the best performance and the worst accuracy.

The linear method always reports “0% fault failed” during simulation at each fault time.

### ***Timezero method***

If the simulation time for the nominal netlist is relatively short, or the number of defects is small, `faultmethod=timezero` method can be used. This method provides the best accuracy. Therefore, you can avoid the experimentation related to the choice of a proper method for the given design. However, the `timezero` method is the slowest and cannot be recommended for every case.

The status of simulation during `timezero` method is annotated by message “Fault analysis for bridge\_1:32 time steps”.

Some of the defects can change the functionality of the circuit dramatically. For instance, oscillations can be triggered and simulation time may increase manifold. The `timezero` method monitors the number of time steps taken and terminates the simulation when the step count becomes huge in comparison to the nominal simulation. Such situation is annotated by the warning message “Transient fault simulation is too slow for bridge\_1 and was terminated at time 800us”. You can collect the names of the failed faults and rerun the simulation within a separate analysis using the same fault list but specifying `faultsname=[bridge_1]`, or `faultsid=[1]` in the new analysis statement.

### ***Maxiters method***

The rest of the fault methods represent a variety of choices for accuracy versus performance in between `linear` and `timezero` methods.

`faultmethod=maxiters` is also a sensitivity method. However, unlike `linear`, it provides better accuracy. The `maxiters` method can be useful when the dynamic response of the circuit is not very important.

You can use several options to control the quality of simulation results.

The transient analysis parameter `faultmaxiters` enables you to specify the maximum limit for the Newton iteration count while performing the simulation step, after a fault injection. The default value is 50. Decreasing this number may improve performance but degrade accuracy for some faults.

The `faultrampsteps` parameter can be used with `maxiters` to improve convergence and reduce the number of iterations required. The recommended value is 10. It represents the maximum number steps allowed in the R-stepping algorithm, when the resistance of the injected bridge is changing gradually from a large value (solution is close to nominal case) to a value specified in the fault list.

The quality of `maxiters` method can be monitored from the annotations. The faults that have convergence issues generate warnings "Fault simulation failed for bridge\_884". The failure means that the convergence criteria was not satisfied for the fault simulation with the given parameters. The mentioned voltages are the solution values for the nominal design before the fault was injected. The big difference may just serve as a confirmation of the fact that shorting these nodes can result in numerical difficulties.

When `faultrampsteps` is specified and a failure occurs, Spectre generates an extended version of this message, that is, "Fault simulation failed for bridge\_44: 3.5V and 0V shorted. (Last converged fault with R=4.604e+03 Ohm)".

The ending of fault simulation at each fault time is annotated as "Fault sensitivity analysis finished at time 2.000000e-04: 92 (7.99%) faults failed." The high percentage of failures indicates that either the simulation parameters have to be adjusted (`faultmaxiters`, `faultrampsteps`, `faultlimiting`), or the fault method `maxiters` is not appropriate for this design.

### ***Onestep method***

When the dynamic response of a circuit is important, or the `maxiters` method does not provide the required accuracy, `faultmethod=onestep` can be used. This method performs as `maxiters` initially. If no convergence is achieved, it reduces the time step and continues the iterations until convergence requirements are satisfied. Therefore, there can be multiple time steps taken until a solution is found at the fault time for every defect. This may affect the simulation performance significantly. You can adjust the simulation parameters (`faultmaxiters`, `faultrampsteps`, `faultlimiting`) to optimize performance.

### ***Leadtime method***

In some situations, the `onestep` method cannot provide the solution while the time step gets reduced to the minimum possible value. The simulation for such defect is considered as failed

and is terminated. The final solution is based on the `maxiters` method. A warning similar to the `maxiters` method is also generated.

If the design under test (DUT) is time-sensitive, `faultmethod=leadtime` can be a better choice than the `onestep` method. The difference between these two methods is only the time where a defect gets injected during the simulation process. The `leadtime` method requires a mandatory parameter `leadtime` to specify the time interval to inject the fault. The `onestep` method takes the defect into consideration at a previous time point, right before the fault time. `leadtime` uses the same parameters as `onestep` and `maxiters`, and supports similar annotations.

The choice of `leadtime` value is limited by the distance between the fault times. The time interval `[testpoint-leadtime, testpoint]` cannot contain any other fault times. The operating frequency or a few clock periods may be considered as a choice of value for `leadtime`. You can use the parameter `faultstrobe=yes` with Spectre strobing options to save the multiple measurements to a table file within the lead time interval. As a result, the restriction of overlapping lead times can be avoided.

In many situations, the `leadtime` method has an advantage over `onestep`. As soon as the defect is taken into consideration ahead of time, it may improve the accuracy of results as well convergence. It is not unusual if `leadtime` takes less time steps than `onestep` for the same fault simulation.

You can use the optional parameter `faultic` to use the dc solution instead of nominal when fault is injected using the `leadtime` method. The possible values are `no`, `bridge`, `open`, `custom`, `param`, and `all`.

### Comparing Accuracy and Performance of Various Methods

For accuracy evaluation of fault methods and performance estimation of Spectre transient fault analysis, direct simulation with the fault injected is required as a reference. In many cases, the direct approach is not realistic for a very long simulation time. To start, it is recommended to select a representative small-to-medium sized design with the fault list that can be simulated within reasonable time using the fault method `timezero`, or by the direct approach (changing netlist for each defect).

As an alternative, Spectre provides the `faultsinst` parameter that can be used in the transient statement. `faultsinst` allows you to select the faults for simulation from one or several blocks in the circuit, without modification of the original fault list. With the limited number of injected faults, the `timezero` method can produce the reference data within reasonable time.

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After performing the simulation for several methods, you can compare the accuracy by means of detection matching using the `spectre_ddmrpt` Spectre binary that is located in the `<installation>/bin` directory.

### Job Distribution in Transient Fault Analysis

Like direct fault analysis, transient fault analysis also supports job distribution. The command to submit transient fault analysis jobs is the same as direct fault analysis. However, transient fault analysis does not save the fault result over the full transient time but only at the test points specified in `faulttimes` vector. Fault simulation results are saved in the raw file and the fault table file.

To submit the jobs on farm machine, you can specify the following:

```
%bsub -R "(OSNAME==Linux)" "spectre +aps -mt +mp=3 tran_fault.scs -outdir fullpath/out_tfa_mp/"
```

To run the distribution on one machine, you may use the following command with a single thread.

```
%spectre +aps -mt +mp=3 tran_fault.scs -outdir out_tfa_mp/
```

Due to the unique fault injection for the transient fault analysis, the data for different jobs need to be combined after the simulation is done in distributed mode. With Virtuoso Visualization and Analysis tool, the data saved for the test points are shown with the job ID in the format `tranName-jobID#_faults-tran`. You can load the waveforms by selecting the data manually.

```
leadtime-001_faults-tran
leadtime-002_faults-tran
leadtime-003_faults-tran
```

### PostProcessing with MDL

You can use MDL to postprocess fault data saved in the table file for transient fault analysis. It applies to fault methods `timezero`, `leadtime`, `onestep`, `maxiters` and `linear` with fault times defined using `faultstart`, `faultstep`, and `faultstop`. With transient fault analysis `leadtime` method, you can also use `faultstrobe=yes` with `strobestart`, `strobestep`, and `strobestop` to output the extra fault data points without injecting the faults at fault times.

For example, the following transient fault analysis statement inserts the fault at 16m, 21m, 26m and 31m with 5m preleading fault interval and saves the extra test points starting at 12m with 0.1m step.

```
leadtime tran stop=51m faultmethod=leadtime faulttimes=[16m 21m 26m 31m] \
```

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```
faultleadtime=[5m] faultstrobe=yes strobestart=[12m] strobestop= 31m \
strobestep=1m
```

The result is saved in the fault table, as shown below.

```
title: Fault analysis
analysis: transient
undefined: 1.60000E+38
```

```
parameters:nominal=0
Test_Points VOUT resistance iterations
1.200000E-02 1.815E+00 1.602e+38 2
1.300000E-02 1.821E+00 1.602e+38 2
1.400000E-02 1.828E+00 1.602e+38 2
1.500000E-02 1.840E+00 1.602e+38 2
1.600000E-02 1.840E+00 1.602e+38 2
1.700000E-02 1.840E+00 1.602e+38 2
1.800000E-02 1.840E+00 1.602e+38 2
1.900000E-02 1.840E+00 1.602e+38 2
2.000000E-02 1.840E+00 1.602e+38 2
2.100000E-02 1.833E+00 1.602e+38 2
2.200000E-02 1.828E+00 1.602e+38 2
2.300000E-02 1.824E+00 1.602e+38 2
2.400000E-02 1.821E+00 1.602e+38 2
2.500000E-02 1.818E+00 1.602e+38 2
2.600000E-02 1.818E+00 1.602e+38 2
2.700000E-02 1.818E+00 1.602e+38 2
2.800000E-02 1.818E+00 1.602e+38 2
2.900000E-02 1.818E+00 1.602e+38 2
3.000000E-02 1.818E+00 1.602e+38 2
3.100000E-02 1.818E+00 1.602e+38 2
```

The measurement of fault result can only be postprocessed with MDL. By running MDL postprocessing, the measurements are added as extended columns in the fault table file.

The transient statement and measurements are defined in `tfa.mdl` as shown below.

```
alias measurement tran1 {
 run leadtime
export real a01=max(V(g))
export real a02=min(V(g))
}
run tran1
```

You can run either of the following commands to generate the fault table file that includes the measurements.

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```
%spectre +mdlpost -faults -b tfa.mdl -r tfarun.raw
%spectre +mdlpost -faults -b tfa.mdl -r tfarun.raw -tablein tfa.tran.table \
 -tableout tfa.new.table
```

MDL postprocessing generates the measurement data file for all the faults according to the PSF data, as shown below.

Exported variables from results directory: ./out\_TFA/myinput\_TFA.raw

```
date : 11:55:23 AM, Thur Jul 2, 2020
design : // Point Netlist Generated on: Mar 5 16:16:42 2020
simulator : spectre
version : 19.1.0.418
```

```
Measurement Name : tran1
Analysis Type : tran
Fault bridge name : func_bridges_bridge_1
out_max.func_bridges_bridge_1 = 0.709153
out_min.func_bridges_bridge_1 = 0.634413
```

```
Measurement Name : tran1
Analysis Type : tran
Fault bridge name : func_bridges_bridge_2
out_max.func_bridges_bridge_2 = 1.84641
out_min.func_bridges_bridge_2 = 1.81887
```

```
Measurement Name : tran1
Analysis Type : tran
Fault bridge name : func_bridges_bridge_3
out_max.func_bridges_bridge_3 = 1.84641
out_min.func_bridges_bridge_3 = 1.81887
```

### Using Calculator Expression with Ocean

You can also use Ocean expression to perform calculation on the fault result saved in the table file. You need the option `savetainseparatedir=yes` in direct fault analysis to save the data in a separate directory.

You can specify the calculation function in a file, for example, `my_calculate.txt`, as shown below.

```
out_max=ymin(v("VOUT"))
out_min=ymin(v("VOUT"))
avg = (out_max + out_min)/2.0
```

Next, run `spectre_ddmrpt` to save the calculated result to a new file.



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The `spectre_ddmrpt` script for direct fault analysis is slightly different from the one for transient fault analysis.

```
% spectre_ddmrpt dfa.tran.table -raw dfa.raw -cf my_calculate.txt -rf \
dfa.final.table
```

For transient fault analysis, you do not have to specify the raw result, as shown below.

```
% spectre_ddmrpt tfa.tran.table -cf calc.txt -rf tfa.final.table
```

The signals `out_max`, `out_min`, and `avg` are saved in addition to the existing signals in the final table file. You can then include the measurement of `avg` in the defect coverage by running the `spectre_ddmrpt` script.

```
parameters:nominal=0
Test_Points VOUT avg out_max out_min resistance iterations
1.100000e-02 1.810e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
1.200000e-02 1.815e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
1.300000e-02 1.821e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
1.400000e-02 1.828e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
1.500000e-02 1.840e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
1.600000e-02 1.840e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
1.700000e-02 1.840e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
1.800000e-02 1.840e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
1.900000e-02 1.840e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
2.000000e-02 1.840e+00 1.822e+00 1.840e+00 1.805e+00 1.602e+38 2
```

## spectre\_ddmrpt Command-Line Options

```
spectre_ddmrpt [-h] [-t TIMEPTS] [-s SIGNALS] [-a ABSTOL] [-r RELTOL]
 [-m MERGE [MERGE ...]] [-o OUTPUT] [-p] [-e] [-cl CL]
 [-cr {CP,W}] [-i INST] [-x XINST] [-g GROUPNAME] [--hs HIERSTART]
 [--hd HIERDEPTH] [--hst HIERSORT] [--er ELEMREPORT] [--du DEFECTUNIV]
 [-q] [--ct] [--ce] [--ne] [--cd CSVDET] [--cs CSVSOL] [--xd XLSXDET]
 [--xs XLSXSOL] [--sd SQLDET] [--ss SQLSOL] [--td TXTDET] [--ts TXTSOL]
 [-D DET] [-G UNDET] [-N ERRFAULT] [-A AUTOSTOP]
 [-oe OCEAN] [-rf RESULTS_FILE] [-cf CALC_FILE]
 [-vf VAR_FILE] [-raw RAW_DIR] [-O OCEAN_OUTPUT_FILE]
 [-P OUTDIR] FILES [FILES ...]
```

### Positional arguments

**FILES** Specifies table files to be analyzed.

Input one file to print detection matrix (detection statistics) and solution matrix (simulation solutions).

Input multiple files to compare their detection matrices with the first file being the reference.

### Optional arguments

**-h, --help** Specifies the help message and exits.

**-t TIMEPTS** Specifies the time points to test the signal; repeat this option or use ' , ' between time points for multiple inputs.

**-s SIGNALS** Specify signals to analyze fault detection; repeat this option or use ',' between signals for multiple inputs. Wildcards '\*' and '?' are also supported. Enclose the expression in quotes to avoid Linux glob expansion.

#### Example:

```
spectre_ddmrpt -s 'testbenc?.*' ~/
spiceModels.leadtime.table | head -n 5
```

**-a ABSTOL** Specifies the absolute tolerance in expression  $\text{reitol} * \text{abs}(\text{nominal}) + \text{abstol}$  used for fault detection ( $\text{abstol}=1\text{e-}6$ ,  $\text{reitol}=0.05$  by default).

Repeat this option or use ' , ' between numbers to set up different tolerances for corresponding time points.

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|                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>-r RELTOL</code>            | <p>Specifies the relative tolerance in expression <math>\text{reltol} * \text{abs}(\text{nominal}) + \text{abstol}</math> used for fault detection (<math>\text{abstol}=1\text{e-}6</math>, <math>\text{reltol}=0.05</math> by default);</p> <p>Repeat this option or use ' , ' between numbers to set up different tolerances for corresponding time points.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <code>-m MERGE [MERGE ...]</code> | <p>Merges multiple table files.</p> <p>Usage:</p> <pre>%spectre_ddmrpt table1 -m table2 [table3 ...] -rf table</pre> <p>Example:</p> <pre>spectre_ddmrpt 1.table -m 2.table 3.table -rf 123.table</pre> <p>If the data in the input tables is based on the same test points and signals, and the faults from <i>table2</i> are a subset of the faults from <i>table1</i>, the final table includes all data from <i>table1</i> with updates according to <i>table2</i>. Merging is not allowed when the faults from <i>table1</i> are a subset of <i>table2</i>.</p> <p>If the data in the input tables is based on the same test points and signals, but the fault lists in <i>table1</i> and <i>table2</i> are different, the final table includes the concatenated data from all tables.</p> <p>If the input table data are based on the same fault lists, but the test points in <i>table1</i> and <i>table2</i> are different, the final table includes concatenated data for all test points from all tables.</p> |
| <code>-o OUTPUT</code>            | <p>Saves the report in a file.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>-p, --p2427</code>          | <p>Prints IEEE 2427 summary.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>-e, --estim</code>          | <p>Print estimated coverage confidence interval evaluation. Default is 0.95.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>-cl CL</code>               | <p>Sets confidence level for fault coverage confidence interval evaluation. Default is 0.95.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>-cr {CP,W}</code>           | <p>Choice of confidence interval formula: Clopper-Pearson, or Wald. Default is CP.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <code>-i INST, --inst INST</code> | <p>Report includes a subset of the fault list that belongs to the specified subcircuit instances.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

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|                                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>-x XINST</code><br><code>--xinst XINST</code>                                   | Report excludes a subset of the fault list that belongs to the specified subcircuit instances.                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>-g GROUPNAME, --group GROUPNAME</code>                                          | Report defect coverage only for a subset of faults whose names start with the specified prefix or match the specified wildcard string.                                                                                                                                                                                                                                                                                                                                             |
| <code>--hs HIERSTART,</code><br><code>--hierstart HIERSTART</code>                    | Print defect coverage according to design hierarchy starting from HIERSTART subcircuit.                                                                                                                                                                                                                                                                                                                                                                                            |
| <code>--hd HIERDEPTH,</code><br><code>--hierdepth HIERDEPTH</code>                    | Report defect coverage for specified number of levels below HIERSTART. Default is all levels.                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>--er ELEMREPORT,</code><br><code>--elemreport</code><br><code>ELEMREPORT</code> | Specify elements to show defect coverage report; repeat this option or use ',' between element for multiple inputs. Wildcards like '*' and '?' are supported when the expression enclosed in quotes. Use 'all' to include all elements. One of extra mandatory parameters is required: <code>-f</code> to provide the original fault list(s) included in simulation and <code>sim.table</code> , or <code>--du</code> defect universe details db related to simulated fault lists. |
| <code>--du DEFECTUNIV,</code><br><code>--defectuniv</code><br><code>DEFECTUNIV</code> | Specify the defect universe details db related to simulated fault lists.                                                                                                                                                                                                                                                                                                                                                                                                           |
| <code>-q, --quiet</code>                                                              | Does not print to stdout.                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

### Matrix Saving Options

|                             |                                                                                                                                                                 |
|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>--ct, --covtop</code> | Prints defect coverage as the first row in detection matrix.                                                                                                    |
| <code>--ce, --coverr</code> | Prints defect coverage including simulation with errors (marked "N") as detected.                                                                               |
| <code>--ne, --nomerr</code> | Propagates nominal solution at last simulated test point as a golden for later test points when nominal simulation auto-stopped earlier, or failed to converge. |
| <code>--cd CSVDET</code>    | Specifies the name of CSV file to save detection matrix (" <code>.csv</code> " will be added to the end).                                                       |
| <code>--cs CSVSOL</code>    | Specifies the name of CSV file to save solution matrix (" <code>.csv</code> " will be added to the end).                                                        |
| <code>--xd XLSXDET</code>   | Specifies the name of Excel file to save detection matrix (" <code>.xlsx</code> " will be added to the end).                                                    |

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|                           |                                                                                                             |
|---------------------------|-------------------------------------------------------------------------------------------------------------|
| <code>--xs XLSXSOL</code> | Specifies the name of Excel file to save solution matrix (" <code>.xlsx</code> " will be added to the end). |
| <code>--sd SQLDET</code>  | Specifies the name of SQL file to save detection matrix (" <code>.db</code> " will be added to the end).    |
| <code>--ss SQLSOL</code>  | Specifies the name of SQL file to save solution matrix. (" <code>.db</code> " will be added to the end)     |
| <code>--td TXTDET</code>  | Specifies the name of ASCII file to save detection matrix (" <code>.txt</code> " will be added to the end). |
| <code>--ts TXTSOL</code>  | Specifies the name of ASCII file to save solution matrix. (" <code>.txt</code> " will be added to the end). |

### Fault List Saving Options

|                          |                                             |
|--------------------------|---------------------------------------------|
| <code>-D DET</code>      | Prints the detected faults into a file.     |
| <code>-G UNDET</code>    | Prints the undetected faults into a file.   |
| <code>-N ERRFAULT</code> | Prints the not testable faults into a file. |
| <code>-A AUTOSTOP</code> | Prints the autostopped faults into a file.  |

### ADE Expression Compatibility Options

|                                                                     |                                                                                                                                                 |
|---------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>-oe OCEAN</code>                                              | Ocean executable (may include path) and command line args.<br><br>Default value = ' <code>ocean -nograph</code> '.                              |
| <code>-rf RESULTS_FILE, --<br/>results_file<br/>RESULTS_FILE</code> | Output table file containing signal values augmented with ADE calculator expression results.<br><br>Default value = <code>output.table</code> . |
| <code>-cf CALC_FILE, --<br/>calc_exprfile<br/>CALC_FILE</code>      | Input file containing calculator expressions, ocean-evaluable SKILL code, etc.                                                                  |
| <code>-vf VAR_FILE, --<br/>VAR_file VAR_FILE</code>                 | Input file containing values for ADE VAR("<xyz>") expressions,<br><br>Default value = <code>None</code>                                         |

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|                                                                          |                                                                                                                                                                 |
|--------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>-raw RAW_DIR, --raw_dir RAW_DIR</code>                             | Name of the DFA raw directory to process calculator expressions.                                                                                                |
| <code>-O OCEAN_OUTPUT_FILE, --ocean_output_file OCEAN_OUTPUT_FILE</code> | Files in which the raw ocean output for debug is to be saved.<br>Default value = <code>ocean_out.txt</code>                                                     |
| <code>-P OUTDIR, --psf_dir OUTDIR</code>                                 | Root of directory tree in which PSF (ASCII) files corresponding to data in <code>-t/--table_file</code> are to be dumped.<br>Default value = <code>OCEAN</code> |

## spectre\_fsrpt Command-Line Options

### Usage

```
spectre_fsrpt [-h] [-e] [-f FAULTFILE] [-o OUTPUT] [-s] [-p PRIORITY]
 [-r] [-cl CL] [-cr {CP,W}] [-i INST] [-x XINST] [-g GROUPNAME] [-s SIGNALS]
 [-SU FILENAME] [-SD FILENAME] [-DD FILENAME] [-DU FILENAME]
 [-safe FILENAME] [-dang FILENAME] [-det FILENAME]
 [-undet FILENAME] [-N FILENAME] [-A FILENAME]
 [-FMID FAILURE_MODE_ID] [-FM FAILURE_MODE_TYPE]
 [-ft {text,text-usf}] FILE [FILE ...]
```

### Positional Arguments

**FILE**

To generate a report from Spectre Fault Analysis, input a Spectre/Xcelium log file.

If the analysis was distributed, input the main log file.

For example: `spectre_fsrpt spectre.log`

To merge multiple report files saved by this script, input the files to be merged.

For example: `spectre_fsrpt fs.rpt fs2.rpt`

### Optional Arguments

**-h, --help** Display the help message to exit.

**-e, --ignore** Ignore asserts that have error definition when generating a report.

**-f FAULTFILE, --faultfile FAULTFILE**

Specifies fault list file generated by Spectre info analysis to print fault device info in the report.

For example: `spectre_fsrpt spectre.log -f fault_bridges.scs -f fault_opens.scs`

**-o OUTPUT, --output OUTPUT**

Saves the report in file.

For example: `spectre_fsrpt spectre.log -o fs.rpt`

**-s, --short** Enables short annotation for measurements in detection matrix.

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`-p PRIORITY, --priority PRIORITY`

Specifies the priority.

When combining multiple reports with the same fault list, `spectre_fsrpt` will pick up the fault classification based on the specified priority.

Default value is 'DD>DU>SD>SU'.

Example: `spectre_fsrpt spectre.log -p 'DD>DU>SD>SU'`

`-r, --incredund`

Include redundant faults with different IDs into the combined report when merging several report files. By default, such faults are included only once.

`-cl CL, --conflevel CL`

Set confidence level for fault coverage confidence interval evaluation.

Default value is 0.95.

`-cr {CP,W}, --confrule {CP,W}`

Choice of confidence interval formula: Clopper-Pearson, or Wald.

Default value is CP.

`-i INST, --inst INST`

Report includes the subset of the fault list which belongs to the specified subcircuit instances.

`-x XINST, --xinst XINST`

Excludes the subset of the fault list which belongs to the specified subcircuit instances.

`-g GROUPNAME --group GROUPNAME`

Report defect coverage only for a subset of faults whose names start with the specified prefix or match the specified wildcard string.

`-s SIGNALS --signals SIGNALS`

Specify signals (asserts) to generate report; repeat this option or use ',' between signals for multiple inputs. Wildcards like '\*' and '?' are supported when the expression is enclosed in quotes.



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|                                               |                                                                                   |
|-----------------------------------------------|-----------------------------------------------------------------------------------|
| <code>-SU FILENAME</code>                     | Prints Safe_undetected (C1) faults into file.                                     |
| <code>-SD FILENAME</code>                     | Prints Safe_detected (C2) faults into file.                                       |
| <code>-DD FILENAME</code>                     | Prints Dangerous_detected (C3) faults into file.                                  |
| <code>-DU FILENAME</code>                     | Prints Dangerous_undetected (C4) faults into file.                                |
| <code>-safe FILENAME</code>                   | Prints Safe faults into file.                                                     |
| <code>-dang FILENAME</code>                   | Prints Dangerous faults into file.                                                |
| <code>-det FILENAME</code>                    | Print Detected faults into file.                                                  |
| <code>-undet FILENAME</code>                  | Print Undetected faults into file.                                                |
| <code>-N FILENAME, --errfault FILENAME</code> | Prints not testable faults into file.                                             |
| <code>-A FILENAME, --autostop FILENAME</code> | Print autostopped faults into file.                                               |
| <code>-FMID FAILURE_MODE_ID</code>            | Failure mode ID.<br>Default value is 000.                                         |
| <code>-FM FAILURE_MODE_TYPE</code>            | Failure mode type, including SPF/LF/LFP/LFC, default is SPF.                      |
| <code>-ft, --format {text,text-usf}</code>    | Choice of output format for functional safety report.<br>Default value is 'text'. |

## Pole Zero Analysis

The pole zero analysis linearizes the circuit about the DC operating point and computes the poles and zeros of the linearized network. The analysis generates a finite number of poles and zeros, each being a complex number. If you sweep a parameter, the parameter values corresponding to the current iteration are printed.

The pole zero analysis dense method works best on small to medium sized circuits (circuits with less than a thousand equations). You can use the arnoldi method (iterative sparse solver) on large circuits for better performance.

If you run a pole zero analysis on a frequency dependent component (element whose AC equivalent varies with frequency, such as transmission line or BJT with excess phases), the Spectre circuit simulator approximates the component as AC equivalent conductance and evaluates conductance at 1Hz.

You can set up and run a pole zero analysis through the Analog Design Environment. For more information, see the *ADE Explorer User Guide*.

## Syntax

```
analysisName [(pnode nnode)] pz [method=arnoldi numpoles=0 numzeros=0 sigmar=0.1
 sigmai=0.0 ...]
```

where

|                       |                                                                                                                                                                                                                                                                                          |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>analysisName</i>   | Name of analysis.                                                                                                                                                                                                                                                                        |
| <i>pnode nnode</i>    | Nodes in the circuit whose difference is the output of the transfer function for which zeroes are to be calculated.                                                                                                                                                                      |
| <i>method=arnoldi</i> | Specifies that the method to be used for calculating poles and zeroes is arnoldi. Default value is <i>qz</i> (dense method).                                                                                                                                                             |
| <i>numpoles=0</i>     | Limits the maximum number of poles in the arnoldi method to the specified value. Default value is 0, which indicates that the limit is the circuit size.                                                                                                                                 |
| <i>numzeros=0</i>     | Limits the maximum number of zeroes in the arnoldi method to the specified value. Default value is 0, which indicates that the limit is the circuit size.                                                                                                                                |
| <i>sigmar=0.1</i>     | Specifies the root finding control parameter for the arnoldi method. If the interesting poles or zeros are around the value <i>z</i> , $z=x+jy$ , setting <i>sigmar</i> to <i>x</i> and <i>sigmai</i> to <i>y</i> helps Spectre find the solution more accurately. Default value is 0.1. |

`sigmai=0.0`

Specifies the root finding control parameter for the arnoldi method. If the interesting poles or zeros are around the value  $z$ ,  $z=x+jy$ , setting `sigmar` to  $x$  and `sigmai` to  $y$  helps Spectre find the solution more accurately. Default value is 0.

If you do not specify the input source, the Spectre circuit simulator performs only the pole analysis. For a detailed description of the parameters, see `spectre -h pz`.

## Example 1

`myPZ1 pz`

Performs pole analysis.

## Example 2

`myPZ2 pz method=arnoldi`

Performs pole analysis with the arnoldi method.

## Example 3

`mypz2 (n1 n2) pz iprobe=VIN`

Performs pole zero analysis for a circuit whose input is `VIN` and output is the voltage difference between nodes `n1` and `n2`.

## Example 4

`mypz3 (n1 n2) pz iprobe=I1 param=temp start=25 stop=100 step=25`

Performs pole zero analysis for a circuit whose input is `I1` and output is the voltage difference between nodes `n1` and `n2`.

## Output Log File

The output log file contains the following information:

- Complex numbers for poles
- Complex numbers for zeroes
- Gain for zeroes

- Quality factor Q, which can be defined as:

$$Qfactor = (sign)^{0.5} \left( \left( \frac{im}{re} \right)^2 + 1 \right)^{0.5}$$

where *sign* is 1 if *real*<0 and *sign* is -1 if *real*>0. When *real* is 0, Qfactor is not defined.

If the output of the pole zero analysis contains positive real part poles indicating an unstable circuit, the label **\*\*RHP** is appended to those poles. An example is shown below:

```

PZ Analysis 'mypz'

```

| Poles (Hertz) |             |           |       |         |
|---------------|-------------|-----------|-------|---------|
|               | Real        | Imaginary |       | Qfactor |
| 1             | 4.5694e+10  | 0         | **RHP | -0.5    |
| 2             | 4.2613e+10  | 0         | **RHP | -0.5    |
| 3             | 1.4969e+10  | 0         | **RHP | -0.5    |
| 4             | 1.4925e+10  | 0         | **RHP | -0.5    |
| 5             | 1.0167e+10  | 0         | **RHP | -0.5    |
| 6             | 1.0165e+10  | 0         | **RHP | -0.5    |
| 7             | 7.3469e+09  | 0         | **RHP | -0.5    |
| 8             | 7.3469e+09  | 0         | **RHP | -0.5    |
| 9             | -1.0061e+09 | 0         |       | 0.5     |
| 10            | -1.0061e+09 | 0         |       | 0.5     |
| 11            | -1.0235e+09 | 0         |       | 0.5     |

## Loopfinder Analysis

The loopfinder (**lf**) analysis linearizes the circuit about the DC operating point and identifies the loops that may potentially cause stability problems. The analysis does not require the identification of loops or the use of probes.

The analysis computes the impedance of the nodes at a frequency that is equal to the magnitude of the pole and identifies the high impedance nodes. It displays the impedance of all the high impedance nodes within a loop, sorted by the impedance value.

The loopfinder analysis, by default, uses the direct method to detect the suspected poles. However, this method is computationally intensive and works best on small-to-medium sized circuits. You can use the **krylov** method (iterative sparse solver) on large circuits for better performance.

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Use the `dampmax` parameter to control the filtering of suspected poles. Setting the value of `dampmax` to 1 results in the inclusion of all poles. The default value of the `dampmax` parameter is 0.7. Use the `zmin` parameter to control the number of nodes in the output. A higher `zmin` value means that fewer nodes will be displayed in the output for a given loop.

For more information on loopfinder analysis, see [LoopFinder Analysis](#) in the Spectre Circuit Simulator Reference manual.

### Syntax

```
analysisName lf <parameter=value>
```

#### Example1

```
mylf lf
```

Performs loopfinder analysis and computes the impedance of all nodes.

#### Example 2

```
mylf lf solver_method=krylov
```

Performs loopfinder analysis using the krylov method for pole detection.

#### Example 3

```
mylf lf dev=R0 param=r start=100 stop=300 step=1
```

In the above example, loopfinder analysis is performed by sweeping the device parameter `r` of the device `R0` from 100 to 300 at an increment of 1.

### Output of the Loopfinder Analysis

Following is a sample output of the loopfinder analysis:

```
Important complex poles - natural frequency and damping factor
1.11e+03 MHz 0.00175
```

```
*****node impedance @wn*****
Natural Frequencies 1.11e+03M
net015 589.
net23 1.31e+03
net022 1.31e+03
net14 589.
```

```
net20 5.37e+03
Vout 5.37e+03
```

```
*****Loop1*****
```

```
Natural Frequency = 1.11e+03 MHz
```

```
Damping Factor = 0.00175
```

| Node Name | Impedance@wn |
|-----------|--------------|
| Vout      | 5.37e+03     |
| net20     | 5.37e+03     |
| net022    | 1.31e+03     |
| net23     | 1.31e+03     |
| net015    | 589.         |
| net14     | 589.         |

## Other Analyses (sens, fourier, dcmatch, and stb)

There are four analyses in this category: `sens`, `fourier`, `dcmatch`, and `stb`.

### Sensitivity Analysis

You can supplement the analysis information you automatically receive with the AC and DC analyses by placing `sens` statements in the netlist. Output for the `sens` command is sent to the rawfile or to an ASCII file that you can specify with the `+sensdata <filename>` option of the `spectre` command.

- If you set `senstype=partial`, Spectre calculates partial sensitivity. This determines the sensitivity of output variables to input design parameters. Results are expressed as a ratio of the change in an output analysis variable to the change in an input design parameter. For example, if  $V$  is the output value, and  $P$  is the input design parameter, sensitivity is computed as follows:

$$S_{V,P} = \frac{dV}{dP}$$

- If you set `senstype=normalized`, Spectre calculates normalized sensitivity, which removes the dependence of results on the magnitude of the output variable and input design parameters. Normalized sensitivity is computed as follows:

$$S_{V,P} = \frac{PdV}{VdP}$$

$$S_{V,P} = P \frac{dV}{dP} \text{ if } V=0$$

$$S_{V,P} = \frac{1}{V} \frac{dV}{dP} \text{ if } P=0$$

When both P and V are zero, partial sensitivity is used.

## Formatting the sens Command

You format the `sens` command, as follows:

```
sens [(output_variables_list)] [to
(design_parameters_list)] [for (analyses_list)]
```

where:

```
output_variables_list = ovar1 ovar2 ...
design_parameters_list = dpar1 dpar2 ...
analyses_list = ana1 ana2 ...
```

The `ovari` are the output variables whose sensitivities are calculated. These are normally node names, deviceInstance:parameter or modelName:parameter specifications. Examples are 5, n1, and Qout:betadc.

The `dparj` are the design parameters to which the output variables are sensitive. You can specify them in a format similar to `ovari`. However, they must be input parameters that you can specify (for example, R1:r). You can use wildcard (\*) for device instances and models (for example, \*:r) in which case, sensitivity information of the output variables is computed with respect to the specified parameters for all device instances and models.

If you do not specify a `to` clause, sensitivities of output variables are calculated with respect to all available instance and model parameters.

**Note:** The method for specifying design parameters and output variables is described in more detail in the documentation for the `save` statement in [Chapter 9, “Specifying Output Options.”](#)

The following table shows you the types of design and output parameters that are normally used for both AC and DC analyses:

|                   | AC Analysis         | DC Analysis                         |
|-------------------|---------------------|-------------------------------------|
| Design parameters | Instance parameters | Instance parameters                 |
|                   | Model parameters    | Model parameters                    |
| Output parameters | Node voltages       | Node voltages                       |
|                   | Branch currents     | Branch currents                     |
|                   |                     | Instance operating-point parameters |

You can also specify device instances or models as design parameters without further specifying parameters, but this approach might result in a number of error messages. The Spectre simulator attempts sensitivity analysis for every device parameter and sends an error message for each parameter that cannot be varied. The Spectre simulator does, however, perform the requested sensitivity analysis for appropriate parameters.

The  $ana_k$  are the analyses for which sensitivities are calculated. These can be analysis instance names (for example, `opBegin` and `ac2`) or analysis type names (for example, `DC` and `AC`).

## Examples of the `sens` Command

The following examples illustrate `sens` command format:

```
sens (q1:betadc 2 Out) to (vcc:dc nbjt1:rb) for (analDC)
```

This command computes DC sensitivities of the `betadc` operating-point parameter of transistor `q1` and of nodes `2` and `Out` to the `dc` voltage level of voltage source `vcc` and to the model parameter `rb` of `nbtj1`. The values are computed for DC analysis `analDC`. The results are stored in the files `analDC.vcc:dc` and `analDC.nbtj1:rb`.

```
sens (1 n2 7) to (q1:area nbjt1:rb) for (analAC)
```

This command computes AC sensitivities of nodes `1`, `n2`, and `7` to the `area` parameter of transistor `q1` and to the model parameter `rb` of `nbtj1`. The values are computed for each frequency of the AC analysis `analAC`. The results are stored in the files `analAC.q1:area` and `analAC.nbtj1:rb`.



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```
sens (vbb:p q1:int_c q1:gm 7) to (q1:area nbjt1:rb) for (analDC1)
```

This command computes DC sensitivities of the branch current `vbb:p`, the operating-point parameter `gm` of transistor `q1`, the internal collector voltage `q1:int_c`, and the node 7 voltage to the instance parameter `q1:area` and the model parameter `nbtj:1:rb`. The values are computed for analysis `analDC1`.

```
sens (1 n2 7) to (*:area) for (analAC)
```

This command computes the AC sensitivities of nodes 1, n2, and 7 to the `area` parameter of all device instances and models.

```
sens (1 n2 7) for (analAC)
```

This command computes the AC sensitivities of nodes 1, n2, and 7 to all available device and model parameters.

**Note:** This can result in a lot of information.

### Sensitivity analysis for binned model in subckt

To support sensitivity analysis for binned model defined in `subckt`, use the option `sensbinparam`.

*sensbinparam=no*: default; feature disabled.

*sensbinparam=uncorrelated*: uncorrelated method.

*sensbinparam=correlated*: fully-correlated method.

### Example:

```
model nch bsim3v3
```

```
{
1: type=n vth0=0.59 lmin=3.5e-7 lmax=8.0e-7 wmin=4.0e-7 wmax=8.0e-7
xl=8.66e-8
xw=-2.1e-8
2: type=n vth0=0.51 +lmin=8.0e-7 lmax=1.2e-6 wmin=4.0e-7 wmax=8.0e-7
xl=8.66e-8
xw=-2.1e-8
}
```

both bins are used by different instances in the netlist. Inside spectre, the model bin name will be `nch_1` and `nch_2`.

Assuming you want the sensitivity of *out* (output signal) vs *vth0* in the model group, the two methods produce results in the following manner:

### ***Uncorrelated***

Considering *nch\_1* and *nch\_2* are two totally independent uncorrelated models, Spectre treats *nch\_1* and *nch\_2* as two separated models.

Spectre perturbs *nch\_1:vth0*, *nch\_2:vth0* parameter values separately.

The sensitivity report will have

*out vs nch\_1:vth0*

*out vs nch\_2:vth0*

### ***Correlated***

Considering *nch\_1* and *nch\_2* are 100% correlated, Spectre perturbs *nch\_1:vth0* and *nch\_2:vth0* simultaneously, the sensitivity report will just have one *out vs nch:vth0*.

## **Fourier Analysis**

The ratiometric Fourier analyzer measures the Fourier coefficients of two different signals at a specified fundamental frequency without loading the circuit. The algorithm used is based on the Fourier integral rather than the discrete Fourier transform and therefore is not subject to aliasing. Even on broad-band signals, it computes a small number of Fourier coefficients accurately and efficiently. Therefore, this Fourier analyzer is suitable on clocked sinusoids generated by sigma-delta converters, pulse-width modulators, digital-to-analog converters, sample-and-holds, and switched-capacitor filters as well as on the traditional low-distortion sinusoids produced by amplifiers or filters.

The analyzer is active only during a transient analysis. For each signal, the analyzer prints the magnitude and phase of the harmonics along with the total harmonic distortion at the end of the transient analysis. The total harmonic distortion is found by summing the power in all of the computed harmonics except DC and the fundamental. Consequently, the distortion is not accurate if you request an insufficient number of harmonics. The Fourier analyzer also prints the ratio of the spectrum of the first signal to the fundamental of the second, so you can use the analyzer to compute large signal gains and immittances directly.

If you are concerned about accuracy, perform an additional Fourier transform on a pure sinusoid generated by an independent source. Because both transforms use the same time

points, the relative errors measured with the known pure sinusoid are representative of the errors in the other transforms. In practice, this second Fourier transform is performed on the reference signal. To increase the accuracy of the Fourier transform, use the `points` parameter to increase the number of points. Tightening `reltol` and setting `errpreset=conservative` are two other measures to consider.

The accuracy of the magnitude and phase for each harmonic is independent of the number of harmonics computed. Thus, increasing the number of harmonics (while keeping `points` constant) does not change the magnitude and phase of the low order harmonics, but it does improve the accuracy of the total harmonic distortion computation. However, if you do not specify `points`, you can increase accuracy by requesting more harmonics, which creates more points.

The large number of points required for accurate results is not a result of aliasing. Many points are needed because a quadratic polynomial interpolates the waveform between the time points. If you use too few time points, the polynomials deviate slightly from the true waveform between time points and all of the computed Fourier coefficients are slightly in error. The algorithm that computes the Fourier integral does accept unevenly spaced time points, but because it uses quadratic interpolation, it is usually more accurate using time steps that are small and nearly evenly spaced.

This device is not supported within `altergroup`.

### Instance Definition

```
Name [p] [n] [pr] [nr] ModelName parameter=value ...
Name [p] [n] [pr] [nr] fourier parameter=value ...
```

The signal between terminals `p` and `n` is the test or numerator signal. The signal between terminals `pr` and `nr` is the reference or denominator signal. Fourier analysis is performed on terminal currents by specifying the `term` or `refterm` parameters. If both `term` and `p` or `n` are specified, then the terminal current becomes the numerator and the node voltages become the denominator. By mixing voltages and currents, it is possible to compute large signal immittances.

### Model Definition

```
model modelName fourier parameter=value ...
```

## DC Match Analysis

The DCMATCH analysis performs DC device matching analysis for a given output. It computes the deviation in the DC operating point of the circuit due to processing or

environmental variation in modeled devices. If `method=standard` is specified, a set of `dcmatch` parameters in the model cards are required for each supported device contributing to the deviation. The analysis applies device mismatch models to construct equivalent mismatch current sources to all the devices that are modeled. These current sources will have zero mean and some variance. The variance of the current sources are computed according to device match models. It then computes the 3-sigma variance of dc voltages or currents at user specified outputs due to the mismatch current sources. The simulation results displays the devices rank ordered by their contributions to the outputs.

In addition, for MOSFET devices, it displays threshold voltage mismatch, current factor mismatch, gate voltage mismatch, and drain current mismatch. For bipolar devices, it displays base-emitter junction voltage mismatch. For resistors, it displays resistor mismatches.

The analysis replaces multiple simulation runs by circuit designers for accuracy vs. size analysis. It automatically identifies the set of critical matched components during circuit design. For example, when there are matched pairs in the circuit, the contribution of two matched transistors will be equal in magnitude and opposite in sign. Typical usage are to simulate the output offset voltage of operational amplifiers, estimate the variation in bandgap voltages, and predict the accuracy of current steering DACs.

For `method=standard`, `DCMATCH` analysis is available for BSIM3V3, BSIM4, BSIMSOI, EKV, PSP102, PSP103, BJT, VBIC, BHT, RESISTOR, PHY\_RES, R3, and resistor-type `bsource`. If `method=statistics` is specified, a statistics block is required to list the parameters that are considered as randomly varying. By default, all statistics parameters found in the statistics block are considered in the computation, unless option `variations` is specified. In this case, device matching models are not used and `dcmatch` model parameters are not required.

### Model Definition

```
name [pnode nnode] dcmatch parameter=value ...
```

### Examples of the `dcmatch` command

The following example investigates the 3-sigma dc variation at the output of the current flowing through the device `vd`, which is a voltage source in the circuit netlist. `dcmm1` is the name of the analysis, `dcmatch` is a keyword indicating the dc mismatch analysis, and the parameter settings `oprobe=vd` and `port1=1` specify that the output current is measured at the first port of `vd`. Device mismatch contributions less than 0.1% of the maximum contribution of all mismatch devices to the output are not reported, as specified by the parameter `meth`. The mismatch (that is the equivalent mismatch current sources in parallel to all the devices that use model `n1`) is modeled by the model parameters `mvtw1`, `mvtw12`, `mvtt0`, `mbew1`, and `mbe0`.

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```
dcmm1 dcmatch mth=1e-3 oprobe=vd porti=1
model n1 bsim3v3 type=n ...
+ mvtwl=6.15e-9 mvtwl2=2.5e-12 mvt0=0.0 mbewl=16.5e-9 mbe0=0.0
```

The output of the analysis is displayed on the screen/logfile:

```
DC Device Matching Analysis 'mismatch1' at vd
Local Variation = 3-sigma random device variation
sigmaOut sigmaVth sigmaBeta sigmaVg sigmaIds
-13.8 uA 2.21 mV 357 m% 2.26 mV 1.71 % mp6
-6.99 uA 1.63 mV 269 m% 1.68 mV 1.08 % m01
-2.71 uA 1.11 mV 187 m% 1.16 mV 648 m% m02
-999 nA 769 uV 131 m% 807 uV 428 m% m04x4_4
-999 nA 769 uV 131 m% 807 uV 428 m% m04x4_3
-999 nA 769 uV 131 m% 807 uV 428 m% m04x4_2
-999 nA 769 uV 131 m% 807 uV 428 m% m04x4_1
-999 nA 769 uV 131 m% 807 uV 428 m% m04
-718 nA 1.09 mV 185 m% 1.15 mV 599 m% m40x04
-520 nA 1.55 mV 263 m% 1.63 mV 835 m% m20x04
-378 nA 2.21 mV 376 m% 2.34 mV 1.16 % m10x04
-363 nA 539 uV 92 m% 567 uV 293 m% m08
-131 nA 379 uV 64.9 m% 400 uV 203 m% m16
-46.7 nA 267 uV 45.9 m% 283 uV 142 m% m32
vd =-3.477 mA +/- 15.91 uA (3-sigma variation)
```

This says that the 3-sigma variation at  $i(vd)$  due to the mismatch models is  $-3.477\text{ mA} \pm 15.91\text{ }\mu\text{A}$ . The  $-3.477\text{ mA}$  is the dc operating value of  $i(vdd)$ , and  $15.91\text{ }\mu\text{A}$  is the 3-sigma variation due to the device mismatches. The device mp6 contributes the most to the output variation at  $-13.8\text{ }\mu\text{A}$  followed by m01 which contributes  $-6.99\text{ }\mu\text{A}$ . The equivalent 3-sigma Vth variation of mp6 is 2.21 mV. The relative 3-sigma beta (current factor) variation of mp6 is 0.357%. The equivalent 3-sigma gate voltage variation is 2.26 mV. The relative 3-sigma Ids variation of mp6 is 1.71%.

The output can also be written in psf, and you can view the table using Analog Design Environment.

The following statement investigates the 3-sigma dc variation on output  $v(n1, n2)$ . The result of the analysis is printed in a psf file and the cpu statistics of the analysis are generated.

```
dcmm2 n1 n2 dcmatch mth=1e-3 where=rawfile
```

In the following example, the output is the voltage drop across the 1st port of r3.

```
dcmm3 dcmatch mth=1e-3 oprobe=r3 portv=1
```

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For the following statement, the output of the analysis is printed to a file `circuitName.info.what`.

```
dcmm4 n3 0 dcmatch mth=1e-3 where=file file="%C:r.info.what"
```

You can use sweep parameters on the dcmatch analysis to perform sweeps of temperature, parameters, model/instance/subcircuit parameters etc.

In the following example, the device parameter `w` of the device `x1.mp2` is swept from  $15\mu\text{m}$  to  $20\mu\text{m}$  at each increment of  $1\mu\text{m}$ .

```
dcmm6 n3 0 dcmatch mth=0.01 dev=x1.mp2 param=w
+ start=15e-6 stop=20e-6 step=1e-6 where=rawfile
```

In the following example, a set of analyses is performed on output `v(n3,0)` by sweeping the device parameter `w` of the device `mp6` from  $80\mu\text{m}$  to  $90\mu\text{m}$  at each increment of  $2\mu\text{m}$ .

```
sweep1 sweep dev=mp6 param=w start=80e-6 stop=90e-6 step=2e-6 {
dcmm5 n3 0 dcmatch mth=1e-3 where=rawfile
}
```

In the following example, temperature is swept from  $25^{\circ}\text{C}$  to  $100^{\circ}\text{C}$  at increment of  $25^{\circ}\text{C}$ .

```
dcmm7 n3 0 dcmatch mth=0.01 param=temp
+ start=25 stop=100 step=25
```

For more information on the dcmatch parameters, see the *Spectre Circuit Simulator Reference*.

If you run the dcmatch analysis in Analog Design Environment, you can access the output through the Results menu and create a table of mismatch contributors.

### DC Match Theory

Statistical variation of drain current in a MOSFET is modeled by

$$I_{ds} = I_{ds_o} + \Delta I_{ds}$$

where

$I_{ds}$  is the total drain to source,

$I_{ds_o}$  is the nominal current, and

$\Delta I_{ds}$  is the variation in drain to source current due to local device variation.

If  $V_{out}$  is the output signal of interest, then the variance of  $V_{out}$  due to the  $i^{th}$  MOSFET is approximated by

$$\sigma^2(V_{out})_i = \left( \frac{\partial}{\partial \Delta I_{ds_i}} V_{out} \right)^2 \bigg|_{I_{ds_o}} \sigma^2(\Delta I_{ds_i})$$

The term

$$\frac{\partial}{\partial \Delta I_{ds_i}} V_{out}$$

in the equation above is the sensitivity of the output to the drain to source current and can be efficiently obtained by the dcmatch analysis.

### **Mismatch Models**

The term  $\sigma^2(\Delta I_{ds_i})$  is the variance of the mismatch current in MOSFET transistors. The mismatch in the current is assumed to be due to a mismatch in the threshold voltage ( $V_{th}$ ) and the mismatch in the width to length ratio ( $\beta$ ). When `version=0/2`, it is approximated as:

$$\frac{\sigma^2(\Delta I_{ds})}{(I_{ds_0})^2} = \frac{g_{m_o}^2}{(I_{ds_0})^2} \sigma^2(\Delta V_{th}) + \frac{\sigma^2(\Delta \beta)}{\beta_o^2}$$

where

$$g_{m_o} = \frac{\partial I_{ds}}{\partial V_{th}} \bigg|_{I_{ds_o}}$$

$$\sigma^2(\Delta V_{th}) = \frac{mvtwI^2}{WL} + \frac{mvtwl^2}{WL^2} + mvt0^2$$

$$\frac{\sigma^2(\Delta \beta)}{(\beta_0)^2} = \frac{mbewI^2}{WL} + mbe0^2$$

Note that  $g_{m_o}$  is computed at the DC bias solution from the device model equations, the values a, b, c, d and e are the mismatch parameters while  $W$  and  $L$  are device parameters.

$$\sigma^2 \Delta V_g = \frac{\sigma^2(\Delta I_{ds})}{g_{m_0}^2}$$

There are several parameters that affect the mismatch model.

- `mismatchmod` specifies the equations to be used for the mismatch model
- `mismatchdist` is the mismatch distance
- `mismatchvec1` specifies the mismatch  $V_{th}$  width and length parameters
- `mismatchvec2` specifies the mismatch Beta width and length parameters
- `mismatchvec3` specifies the mismatch  $V_{th}$  distance parameter
- `mismatchvec4` is the mismatch Beta distance parameter

When `mismatchmod=0`, the default mismatch equations are used.

$$\sigma^2(\Delta V_{th}) = \frac{mvtwl^2}{WL} + \frac{mvtwl^2}{WL^2} + mvt0^2$$

$$\frac{\sigma^2(\Delta\beta)}{(\beta_0)^2} = \frac{mbewl^2}{WL} + mbe0^2$$

When `mismatchmod=1`, the unified mismatch equations are used.

$$\sigma^2(\Delta V_{th}) = \frac{A_1}{W^{B_1} L^{C_1}} + \frac{A_2}{W^{B_2} L^{C_2}} + A_3$$

$$\frac{\sigma^2(\Delta\beta)}{(\beta_0)^2} = \frac{X_1}{W^{Y_1} L^{Z_1}} + \frac{X_2}{W^{Y_2} L^{Z_2}} + X_3$$

`mismatchvec1= [A1, B1, C1, A2, B2, C2, A3 ]`

`mismatchvec2= [X1, Y1, Z1, X2, Y2, Z2, X3 ]`

When `mismatchmod=2`, the Pelgrow's Law mismatch equations are used.

$$\sigma(\Delta V_{th}) = \frac{A}{\sqrt{WL}} + B$$

$$\frac{\sigma(\Delta\beta)}{(\beta_0)} = \frac{X}{\sqrt{WL}} + Y$$

`mismatchvec1= [A, B ]`

`mismatchvec2= [X, Y ]`



When `mismatchmod=3`, the universal mismatch equations are used.

$$\sigma^2(\Delta V_{th}) = \sum_{i=0}^n \frac{A_i}{W_i L C_i} + \sum_{j=0}^r E_j D_j^F$$

$$\frac{\sigma^2(\Delta \beta)}{\beta_0^2} = \sum_{i=0}^m \frac{X_i}{W_i Y_i L Z_i} + \sum_{j=0}^s G_j D_j^H$$

`mismatchvec1= [N, A1, B1, C1, ..., An, Bn, Cn ]`

`mismatchvec2= [M, X1, Y1, Z1, ..., Xm, Ym, Zm ]`

`mismatchvec3= [R, E1, F1, ..., Er, Fr]`

`mismatchvec4= [S, G1, H1, ..., Gs, Hs]`

The bipolar  $\sigma^2(\Delta I_c)$  and the resistor  $\sigma^2(\Delta I_r)$  are computed for each device provided that the device size, bias point, and mismatch parameters are known.

$$\frac{\sigma^2(\Delta I_r)}{I_r^2} = mr + \frac{mrl}{L^{mrlp}} + \frac{mrw}{W^{mrwp}} + \frac{mrlw1}{(LW)^{mrlw1p}} + \frac{mrlw2}{(LW)^{mrlw2p}}$$

$$\frac{\sigma^2(\Delta I_c)}{(I_{c0})^2} = \frac{(gm_0)^2}{(I_{c0})^2} \cdot (mvt0)^2$$

where  $gm_0$  is  $\frac{\partial}{\partial V_{BE}} I_c$ ,  $I_{c0}$  is the nominal collector current, and  $\Delta V_{be} = mvt0 / \sqrt{2}$ .

### **Modified MOSFET Mismatch Models**

When `version=1/3`, the following DC mismatch model is used for BSIM models:

$$\frac{\sigma^2(\Delta I_{ds})}{(I_{ds0})^2} = \frac{\left(\frac{\partial}{\partial V_{th0}} I_{ds}\right)^2}{(I_{ds0})^2} \sigma^2(\Delta V_{th}) + \left(\frac{u0}{I_{ds0}}\right)^2 \left(\frac{\partial}{\partial u0} I_{ds}\right)^2 \frac{\sigma^2(\Delta u0)}{u0^2}$$

where  $v_{th0}$  and  $u0$  are BSIM model parameters.

## New Method to Perform DC Match Analysis

The existing DC Match analysis simulates the statistical mismatch based on device mismatch models and only supports resistor, BJT, and MOSFET devices.

Starting with the MMSIM 12.1.1 release, a new parameter `method` with possible values of `standard` and `statistics` has been added in `dcmatch` analysis. When `method` is set to `statistics`, Spectre computes the statistical variation by:

1. Computing the sensitivity of the output signal to any parameters.
2. Considering the statistical definitions and computing the `sigmaOut` as results.

The syntax for the new `method` is as follows:

```
analysis_name [(output_node_name)] dcmatch method=statistics | standard ...
```

The DC Match analysis prints the sensitivity and sigma output for each statistics parameter, and then prints the one sigma variation for output node `OUT`.

```

DC Device Matching Analysis `dcmm' at V(OUT,0)

DC simulation time: CPU = 1 ms, elapsed = 998.974 us.
SigmaOut Sensitivity DesignParameter Contribution
16.52 uV 1.168e-05 n_p1_sigma
9.866 uV 6.97615e-06 n_p2_sigma
6.776 uV 4.79167e-06 p_p1_sigma
858.6 nV -6.07093e-07 p_p2_sigma
```

There are four parameters that contribute zero (or below `thresh_mth`) sensitivity to the output.

```
V(OUT,0) = 1.649 V +/- 20.42 uV (1-sigma total variation)
```

## ACMatch Analysis

ACMatch analysis linearizes the circuit about the DC operating point and computes the variations of AC responses due to statistical parameters defined in statistics blocks. Only mismatch parameters are considered. The analysis skips the process parameters.

ACMatch takes each parameter defined in the statistics blocks and applies variation one at a time to compute the sensitivity of the output signal with respect to the statistical parameter. Based on the sensitivities computed by this procedure, the total variation of the output is computed by adding the variation contributions from each statistical parameter, assuming that the parameters are mutually independent.

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The output result is sorted based on the real part of the output sigma of each parameter (or instance).

You can specify two or less than two nodes with the ACMatch analysis. If you specify one node, the analysis outputs the AC response on that node. If you specify two nodes, the analysis outputs the difference in AC response between the two nodes.

## Model Definition

```
name node1 [node2] acmatch parameter=value...
```

## Examples of Analysis

```
acmm OUTP acmatch start=1k stop=100G dec=1 where=rawfile groupby=inst
```

The following statement investigates the 1-sigma ac variation on output `v(OUTP)`. The sweep points have been specified at 1k and 100G and the total sigma of each contributor is grouped by instance name. The results are saved in a psf file.

Following is the output generated by the ACMatch analysis:

| Real               | Imag    | Real        | Imag        | Mag                                                            | Phase   | Mag         | Phase       | Contributor | ➡ Header                                  |                                 |
|--------------------|---------|-------------|-------------|----------------------------------------------------------------|---------|-------------|-------------|-------------|-------------------------------------------|---------------------------------|
| 1-Sigma            | 1-Sigma | Variance(%) | Variance(%) | 1-Sigma                                                        | 1-Sigma | Variance(%) | Variance(%) |             |                                           |                                 |
| frequency = 1 kHz  |         |             |             |                                                                |         |             |             |             |                                           |                                 |
| 7.55 V             | 6.64 mV | 56.3        | 41.8        | 7.55 V                                                         | 5.71 u  | 56.3        | 12.2        | IO.M8       | ➡ Contribution of each mismatch parameter |                                 |
| 3.8 V              | 899 uV  | 14.3        | 765 n       | 3.8 V                                                          | 6.4 u   | 14.3        | 15.3        | IO.M6       |                                           |                                 |
| 3.71 V             | 7.55 mV | 13.6        | 54          | 3.71 V                                                         | 12.2 u  | 13.6        | 55.4        | IO.M7       |                                           |                                 |
| 2.69 V             | 608 uV  | 7.14        | 350 n       | 2.69 V                                                         | 4.47 u  | 7.14        | 7.48        | IO.M9       |                                           |                                 |
| 2.64 V             | 599 uV  | 6.91        | 339 n       | 2.64 V                                                         | 4.4 u   | 6.91        | 7.24        | IO.M10      |                                           |                                 |
| 1.1 V              | 1.06 mV | 1.2         | 1.06        | 1.1 V                                                          | 1.05 u  | 1.2         | 416 n       | IO.M5       |                                           |                                 |
| 496 mV             | 964 uV  | 244 m       | 880 n       | 496 mV                                                         | 1.54 u  | 244 m       | 884 n       | IO.M3       |                                           |                                 |
| 445 mV             | 877 uV  | 196 m       | 728 n       | 445 mV                                                         | 1.44 u  | 196 m       | 772 n       | IO.M4       |                                           |                                 |
| 186 mV             | 342 uV  | 34.3 m      | 111 n       | 186 mV                                                         | 758 n   | 34.3 m      | 215 n       | IO.M2       |                                           |                                 |
| Real               | Imag    | Mag         | Phase       | (ac solution)<br>(1-sigma total)<br>(coefficient of variation) |         |             |             |             |                                           | ➡ Total contribution @frequency |
| 457 V              | -245 mV | 457 V       | -30.6 m     |                                                                |         |             |             |             |                                           |                                 |
| 10.1 V             | 10.3 mV | 10.1 V      | 936 u       |                                                                |         |             |             |             |                                           |                                 |
| 2.2 %              | 4.2 %   | 2.2 %       | 3.06 %      |                                                                |         |             |             |             |                                           |                                 |
| frequency = 10 kHz |         |             |             |                                                                |         |             |             |             |                                           |                                 |
| 7.55 V             | 66.5 mV | 56.3        | 41.8        | 7.55 V                                                         | 57.1 u  | 56.3        | 12.2        | IO.M8       | ➡ Next frequency                          |                                 |
| 3.8 V              | 8.99 mV | 14.3        | 764 n       | 3.8 V                                                          | 64 u    | 14.3        | 15.3        | IO.M6       |                                           |                                 |
| 3.71 V             | 75.5 mV | 13.6        | 54          | 3.71 V                                                         | 122 u   | 13.6        | 55.4        | IO.M7       |                                           |                                 |
| 2.69 V             | 6.08 mV | 7.14        | 350 n       | 2.69 V                                                         | 44.7 u  | 7.14        | 7.47        | IO.M9       |                                           |                                 |
| 2.64 V             | 5.98 mV | 6.91        | 339 n       | 2.64 V                                                         | 44 u    | 6.91        | 7.24        | IO.M10      |                                           |                                 |
| 1.1 V              | 10.6 mV | 1.2         | 1.06        | 1.1 V                                                          | 10.5 u  | 1.2         | 416 n       | IO.M5       |                                           |                                 |
| 496 mV             | 9.64 mV | 244 m       | 880 n       | 496 mV                                                         | 15.4 u  | 244 m       | 884 n       | IO.M3       |                                           |                                 |
| 445 mV             | 8.77 mV | 196 m       | 727 n       | 445 mV                                                         | 14.4 u  | 196 m       | 772 n       | IO.M4       |                                           |                                 |
| 186 mV             | 3.42 mV | 34.3 m      | 111 n       | 186 mV                                                         | 7.58 u  | 34.3 m      | 215 n       | IO.M2       |                                           |                                 |
| Real               | Imag    | Mag         | Phase       | (ac solution)<br>(1-sigma total)<br>(coefficient of variation) |         |             |             |             |                                           |                                 |
| 457 V              | -2.45 V | 457 V       | -306 m      |                                                                |         |             |             |             |                                           |                                 |
| 10.1 V             | 103 mV  | 10.1 V      | 9.36 m      |                                                                |         |             |             |             |                                           |                                 |
| 2.2 %              | 4.2 %   | 2.2 %       | 3.06 %      |                                                                |         |             |             |             |                                           |                                 |

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Following is the output generated by ACMatch analysis, grouped by parameter names:

| Real<br>1-Sigma    | Imag<br>1-Sigma | Real<br>Variance(%) | Imag<br>Variance(%) | Mag<br>1-Sigma             | Phase<br>1-Sigma | Mag<br>Variance(%) | Phase<br>Variance(%) | Parameter<br>Name |
|--------------------|-----------------|---------------------|---------------------|----------------------------|------------------|--------------------|----------------------|-------------------|
| frequency = 1 kHz  |                 |                     |                     |                            |                  |                    |                      |                   |
| 7.37 V             | 6.49 mV         | 53.8                | 39.9                | 7.37 V                     | 5.57 u           | 53.8               | 11.6                 | IO.M8:m_dvthn     |
| 3.71 V             | 878 uV          | 13.6                | 729 m               | 3.71 V                     | 6.25 u           | 13.6               | 14.6                 | IO.M6:m_dvthn     |
| 3.63 V             | 7.38 mV         | 13                  | 51.5                | 3.63 V                     | 11.9 u           | 13                 | 52.9                 | IO.M7:m_dvthn     |
| 2.3 V              | 521 uV          | 5.23                | 257 m               | 2.3 V                      | 3.83 u           | 5.23               | 5.48                 | IO.M9:m_dvthp     |
| 2.27 V             | 513 uV          | 5.08                | 249 m               | 2.27 V                     | 3.77 u           | 5.08               | 5.32                 | IO.M10:m_dvth     |
| 1.61 V             | 1.42 mV         | 2.58                | 1.91                | 1.61 V                     | 1.22 u           | 2.58               | 559 m                | IO.M8:m_u0n       |
| 1.39 V             | 314 uV          | 1.9                 | 93.4 m              | 1.39 V                     | 2.31 u           | 1.9                | 1.99                 | IO.M9:m_u0p       |
| 1.36 V             | 308 uV          | 1.83                | 89.7 m              | 1.36 V                     | 2.26 u           | 1.83               | 1.92                 | IO.M10:m_u0p      |
| 898 mV             | 939 uV          | 799 m               | 834 m               | 898 mV                     | 1 u              | 799 m              | 376 m                | IO.M5:m_dvthp     |
| 813 mV             | 194 uV          | 654 m               | 35.7 m              | 813 mV                     | 1.37 u           | 654 m              | 708 m                | IO.M6:m_u0n       |
| 793 mV             | 1.62 mV         | 622 m               | 2.47                | 793 mV                     | 2.6 u            | 622 m              | 2.54                 | IO.M7:m_u0n       |
| 639 mV             | 491 uV          | 404 m               | 228 m               | 639 mV                     | 3.26 u           | 404 m              | 39.9 m               | IO.M5:m_u0p       |
| 461 mV             | 833 uV          | 210 m               | 656 m               | 461 mV                     | 1.28 u           | 210 m              | 615 m                | IO.M3:m_dvthp     |
| 445 mV             | 819 uV          | 196 m               | 635 m               | 445 mV                     | 1.27 u           | 196 m              | 605 m                | IO.M4:m_dvthp     |
| 184 mV             | 486 uV          | 33.5 m              | 223 m               | 184 mV                     | 847 n            | 33.5 m             | 269 m                | IO.M3:m_u0p       |
| 124 mV             | 231 uV          | 15.2 m              | 58.7 m              | 124 mV                     | 651 n            | 15.2 m             | 159 m                | IO.M2:m_u0n       |
| 13 mV              | 312 uV          | 167 u               | 92.2 m              | 13 mV                      | 667 n            | 167 u              | 167 m                | IO.M4:m_u0p       |
| Real               | Imag            | Mag                 | Phase               |                            |                  |                    |                      |                   |
| 457 V              | -245 mV         | 457 V               | -38.6 m             | (ac solution)              |                  |                    |                      |                   |
| 10.1 V             | 10.1 mV         | 10.1 V              | 936 u               | (1-sigma total)            |                  |                    |                      |                   |
| 2.2 %              | 4.2 %           | 2.2 %               | 3.86 %              | (coefficient of variation) |                  |                    |                      |                   |
| frequency = 10 kHz |                 |                     |                     |                            |                  |                    |                      |                   |
| 7.37 V             | 64.9 mV         | 53.8                | 39.9                | 7.37 V                     | 55.7 u           | 53.8               | 11.6                 | IO.M8:m_dvthn     |
| 3.71 V             | 8.77 mV         | 13.6                | 728 m               | 3.71 V                     | 62.5 u           | 13.6               | 14.6                 | IO.M6:m_dvthn     |
| 3.63 V             | 73.8 mV         | 13                  | 51.5                | 3.63 V                     | 119 u            | 13                 | 52.9                 | IO.M7:m_dvthn     |
| 2.3 V              | 5.2 mV          | 5.23                | 256 m               | 2.3 V                      | 38.3 u           | 5.23               | 5.48                 | IO.M9:m_dvthp     |
| 2.27 V             | 5.13 mV         | 5.08                | 249 m               | 2.27 V                     | 37.7 u           | 5.08               | 5.32                 | IO.M10:m_dvth     |
| 1.61 V             | 14.2 mV         | 2.58                | 1.91                | 1.61 V                     | 12.2 u           | 2.58               | 559 m                | IO.M8:m_u0n       |
| 1.39 V             | 3.14 mV         | 1.9                 | 93.3 m              | 1.39 V                     | 23.1 u           | 1.9                | 1.99                 | IO.M9:m_u0p       |
| 1.36 V             | 3.08 mV         | 1.83                | 89.6 m              | 1.36 V                     | 22.6 u           | 1.83               | 1.91                 | IO.M10:m_u0p      |
| 898 mV             | 9.39 mV         | 799 m               | 834 m               | 898 mV                     | 10 u             | 799 m              | 376 m                | IO.M5:m_dvthp     |
| 813 mV             | 1.94 mV         | 654 m               | 35.6 m              | 813 mV                     | 13.7 u           | 654 m              | 708 m                | IO.M6:m_u0n       |
| 793 mV             | 16.2 mV         | 622 m               | 2.47                | 793 mV                     | 26 u             | 622 m              | 2.54                 | IO.M7:m_u0n       |
| 639 mV             | 4.91 mV         | 404 m               | 228 m               | 639 mV                     | 3.26 u           | 404 m              | 39.9 m               | IO.M5:m_u0p       |
| 461 mV             | 8.33 mV         | 210 m               | 656 m               | 461 mV                     | 12.8 u           | 210 m              | 615 m                | IO.M3:m_dvthp     |
| 445 mV             | 8.19 mV         | 196 m               | 635 m               | 445 mV                     | 12.7 u           | 196 m              | 605 m                | IO.M4:m_dvthp     |
| 184 mV             | 4.86 mV         | 33.4 m              | 223 m               | 184 mV                     | 8.47 u           | 33.4 m             | 269 m                | IO.M3:m_u0p       |

For more information on ACMatch Analysis, refer to the [ACMatch Analysis](#) section in the *Spectre Circuit Simulator Reference manual*

## Stability Analysis

The loop-based and device-based algorithms are available in the Spectre circuit simulator for small-signal stability analysis. Both are based on the calculation of Bode's return ratio. The analysis output are loop gain waveform, gain margin, and phase margin.

### Model Definition

```
name stb parameter=value ...
```

### Examples of the stb command

```
stbloop stb start=1.0 stop=1e12 dec=10 probe=Iprobe
stbdev stb start=1.0 stop=1e12 dec=10 probe=mos1
```

The analysis parameters are similar to the small-signal ac analysis except for the `probe` parameter, which must be specified to perform stability analysis. When the `probe` parameter points to a current probe or voltage source instance, the loop based algorithm will be invoked; when it points to a supported active device instance, the device based algorithm will be invoked.

The gain margin and phase margin are automatically determined from the loop gain waveform by detecting zero-crossing in the gain plot and phase plot. If margins cannot be determined for a particular stability analysis, a log file displays the corresponding reason.

### Loop-Based Algorithm

The loop-based algorithm is based on considering the feedback loop as a lumped model with normal and reverse loop transmission. It calculates the true loop gain, which consists of normal loop gain and reverse loop gain. Stability analysis approaches for low-frequency applications assume that signal flows unilaterally through the feedback loop, and they use the normal loop gain to assess the stability of the design. However, the true loop gain provides more accurate stability information for applications involving significant reverse transmission.

You can place a probe component (current probe or zero-DC-valued voltage source) on the feedback loop to identify the loop of interest. The probe component does not change any of the circuit characteristics, and there is no special requirement on the polarity configuration of the probe component.

The loop-based algorithm provides accurate stability information for single-loop circuits and multi-loop circuits in which a probe component can be placed on a critical wire to break all loops. For a multi-loop circuit in which such a wire may not be available, the loop based algorithm can be performed only on individual feedback loops to ensure they are stable. Although the stability of all feedback loops is only a necessary condition for the whole circuit to be stable, the multi-loop circuit tends to be stable if all individual loops are associated with reasonable stability margins.

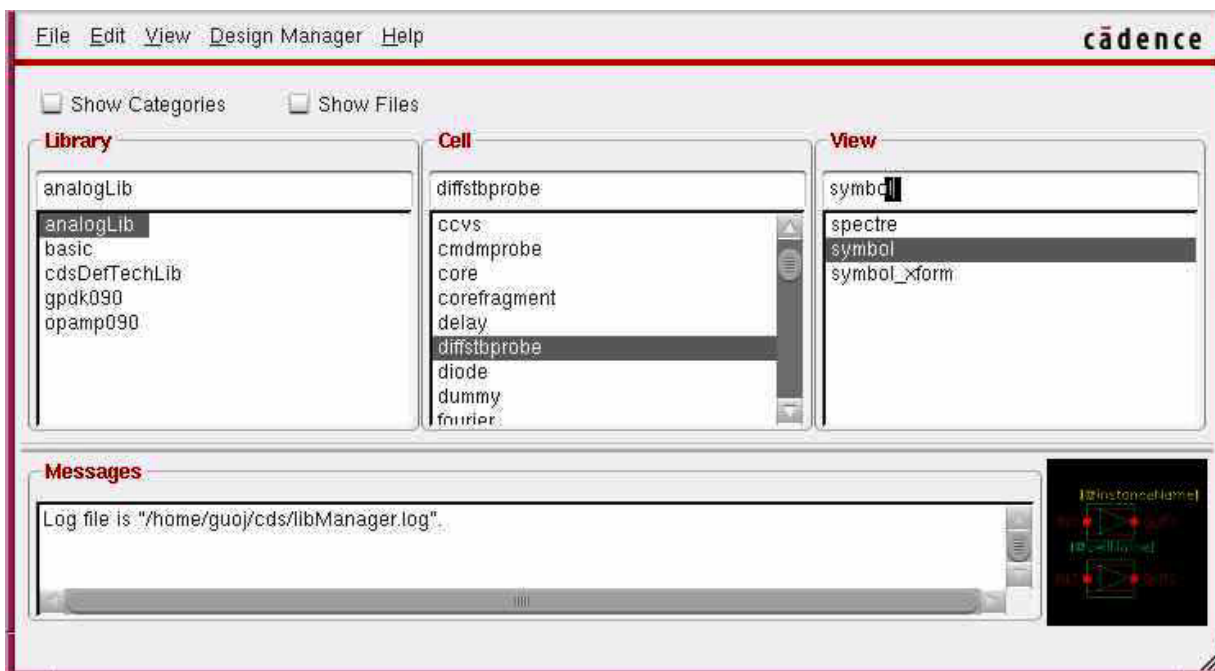
### Stability Analysis of Differential Circuit with Loop-based Algorithm

For the multi-loop circuits, such as differential feedback circuit, a differential stability probe (`diffstbprobe`) should be inserted to perform the stability analysis by breaking all the feedback loops.

**Note:** It is recommended to use `diffstbprobe` instead of `cmdmprobe` for multi-loop circuits.

In ADE schematic, you can select the differential probe named as `diffstbprobe` in `analogLib`, see Figure [11-1](#).

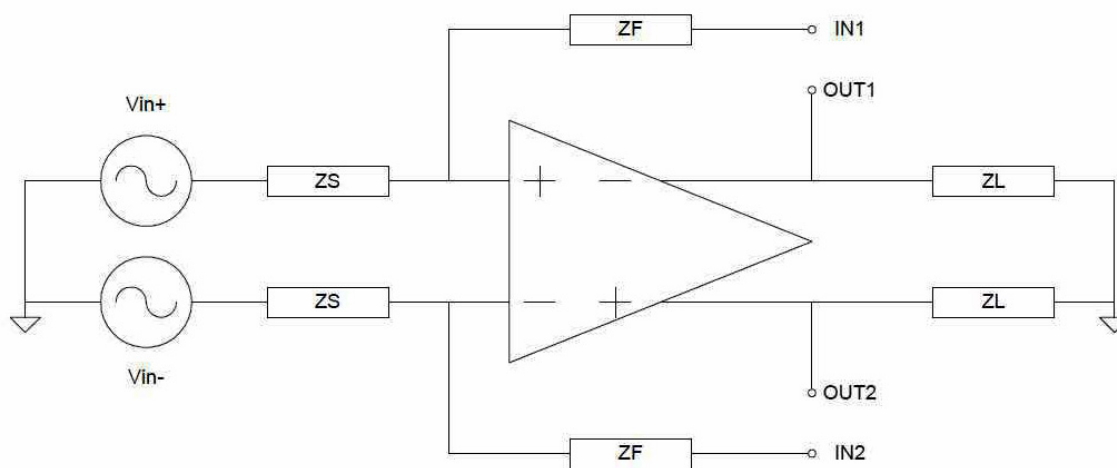
**Figure 11-1 Differential stb probe in analogLib**



With that component of diffstbprobe, there are four nodes defined as  
 Istbprobe (IN1 IN2 OUT1 OUT2) diffstbprobe

Figure 11-2 shows how to connect the probe to the differential circuit.

**Figure 11-2 Differential feedback circuit**



## ***Example of differential mode:***

```
stbloop stb start=1 stop=10G probe= Istbprobe.IPRB_DM
```

The analysis parameter of probe has to specify as IPRB\_DM of a probe instance for differential circuit.

## **Device Based Algorithm**

The device-based algorithm produces accurate stability information for circuits in which a critical active device can be identified such that nulling the dominant gain source of this device renders the whole network to be passive. Examples are multistage amplifier, single-transistor circuit, and S-parameter characterized microwave component.

This algorithm is often applied to assess the stability of circuit design in which local feedback loops cannot be neglected; the loop-based algorithm cannot be performed for these applications because the local feedback loops are inside the devices and are not accessible from the schematic level or netlist level to insert the probe component.

The supported active device and its dominant gain source are summarized in the table below.

| <b>Component</b> | <b>Dominant Controlled Source</b> | <b>Description</b>              |
|------------------|-----------------------------------|---------------------------------|
| b3soipd          | gm                                | Common-source transconductance  |
| bjt              | gm                                | Common-emitter transconductance |
| bsim1,2,3,3v3    | gm                                | Common-source transconductance  |
| btasoi           | gm                                | Common-source transconductance  |
| cccs             | gain                              | Current gain                    |
| ccvs             | rm                                | Transresistance                 |
| ekv              | gm                                | Common-source transconductance  |
| gaas             | gm                                | Common-source transconductance  |
| hbt              | dice_dvbe                         | Intrinsic dlce/dVbe             |
| hvmos            | gm                                | Common-source transconductance  |
| jfet             | gm                                | Common-source transconductance  |
| mos0,1,2,3       | gm                                | Common-source transconductance  |
| tom2             | gm                                | Common-source transconductance  |
| vbic             | dic_dvbe                          | Intrinsic dlc/dVbe              |
| vccs             | gm                                | Transconductance                |

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| Component | Dominant Controlled Source | Description  |
|-----------|----------------------------|--------------|
| vcvs      | gain                       | Voltage gain |

In general, the stability information produced by the device-based algorithm can be used to assess the stability of that particular device. Most often, a feedback network consists of a global feedback loop and numerous nested local loops around individual transistors. The loop-based algorithm can determine the stability of the whole network as long as all nested loops are stable, while the device-based algorithm can be used to ensure all local loops are stable.

For more information on the stability analysis parameters, see the *Spectre Circuit Simulator Reference*.



## Sweep Analysis

The `sweep` analysis sweeps a parameter processing a list of analyses (or multiple analyses) for each value of the parameter.

The sweeps can be linear or logarithmic. Swept parameters return to their original values after the analysis. However, certain other analyses also allow you to sweep a parameter while performing that analysis. For more details, check `spectre -h` for each of the following analyses. The following table shows you which parameters you can sweep with different analyses.

|                                                                | Time | TEMP | FREQ | A component<br>instance<br>parameter | A component<br>model<br>parameter | A netlist<br>parameter |
|----------------------------------------------------------------|------|------|------|--------------------------------------|-----------------------------------|------------------------|
| DC analysis ( <code>dc</code> )                                |      | •    |      | •                                    | •                                 | •                      |
| AC analysis ( <code>ac</code> )                                |      | •    | •    | •                                    | •                                 | •                      |
| Noise analysis<br>( <code>noise</code> )                       |      | •    | •    | •                                    | •                                 | •                      |
| S-parameter<br>analysis ( <code>sp</code> )                    |      | •    | •    | •                                    | •                                 | •                      |
| Transfer function<br>analysis ( <code>xf</code> )              |      | •    | •    | •                                    | •                                 | •                      |
| Transient analysis<br>( <code>tran</code> )                    | •    |      |      |                                      |                                   |                        |
| Time-domain<br>reflectometer<br>analysis ( <code>tdr</code> )  | •    |      |      |                                      |                                   |                        |
| Periodic steady<br>state analysis ( <code>pss</code> )         | •    |      |      |                                      |                                   |                        |
| Periodic AC<br>analysis ( <code>pac</code> )                   |      |      | •    |                                      |                                   |                        |
| Periodic transfer<br>function analysis<br>( <code>pxf</code> ) |      |      | •    |                                      |                                   |                        |
| Periodic noise<br>analysis ( <code>pnoise</code> )             |      |      | •    |                                      |                                   |                        |

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|                                              | Time | TEMP | FREQ | A component instance parameter | A component model parameter | A netlist parameter |
|----------------------------------------------|------|------|------|--------------------------------|-----------------------------|---------------------|
| Envelope-following analysis ( <i>envlp</i> ) | •    |      |      |                                |                             |                     |
| Sweep analysis ( <i>sweep</i> )              |      | •    |      | •                              | •                           | •                   |
| DC Match Analysis ( <i>dcmatch</i> )         |      | •    |      | •                              | •                           | •                   |
| Stability Analysis ( <i>stb</i> )            |      | •    | •    | •                              | •                           | •                   |

**Note:** To generate transfer curves with the DC analysis, specify a parameter and a sweep range. If you specify the `oppoint` parameter for a DC analysis, the Spectre simulator computes the linearized model for each nonlinear component. If you specify both a DC sweep and an operating point, the operating point information is generated for the last point in the sweep.

## Setting Up Parameter Sweeps

To specify a parameter sweep, you must identify the component or circuit parameter you want to sweep and the sweep limits in an analysis statement. A parameter you sweep can be circuit temperature, a device instance parameter, a device model parameter, a netlist parameter, or a subcircuit parameter for a particular subcircuit instance.

Within the `sweep` analysis only, you specify child analyses statements. These statements must be bound with braces. The opening brace is required at the end of the line defining the sweep.

## Specifying the Parameter You Want to Sweep

You specify the components and parameters you want to sweep with the following parameters:

| Parameter        | Description                                                     |
|------------------|-----------------------------------------------------------------|
| <code>dev</code> | The name of an instance whose parameter value you want to sweep |

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| Parameter             | Description                                                                                                                                                                                                                                           |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>sub</code>      | The name of the subcircuit instance whose parameter value you want to sweep                                                                                                                                                                           |
| <code>mod</code>      | The name of a model whose parameter value you want to sweep                                                                                                                                                                                           |
| <code>param</code>    | The name of the component parameter you want to sweep                                                                                                                                                                                                 |
| <code>freq</code>     | For analyses that normally sweep frequency (small-signal analyses such as <code>ac</code> ), if you sweep some parameter other than frequency, you must still specify a fixed frequency value for that analysis using the <code>freq</code> parameter |
| <code>paramset</code> | For the <code>sweep</code> analysis only; allows sweeping of multiple parameters defined by the <code>paramset</code> statement                                                                                                                       |

For all analyses that support sweeping, to sweep the circuit temperature, use `param=temp` with no `dev`, `mod`, or `sub` parameter. You can sweep a top-level netlist parameter by giving the parameter name with no `dev`, `mod`, or `sub` parameter. You can sweep a subcircuit parameter for a particular subcircuit instance by specifying the subcircuit instance name with the `sub` parameter and the subcircuit parameter name with the `param` parameter. You can do the same thing for a particular device instance by using `dev` for the device instance name or for a particular model by using `mod` for the device model name.

**Note:** If frequency is a sweep option for an analysis, the Spectre simulator sweeps frequency if you leave `dev`, `mod`, and `param` unspecified. That is, frequency is the default swept parameter for that analysis.

### Specifying Parameter Sets You Want to Sweep

For the `sweep` analysis only, the `paramset` statement allows you to specify a list of parameters and their values. This can be referred by a `sweep` analysis to sweep the set of parameters over the values specified. For each iteration of the sweep, the netlist parameters are set to the values specified by a row. The values have to be numbers, and the parameters' names have to be defined in the input file (netlist) before they are used. The `paramset` statement is allowed only in the top level of the input file.

The following is the syntax for the `paramset` statement:

```
Name paramset {
 list of netlist parameters
 list of values foreach netlist parameter
 list of values foreach netlist parameter ...
}
```

Here is an example of the `paramset` statement:

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```
parameters p1=1 p2=2 p3=3
data paramset {
 p1 p2 p3
 5 5 5
 4 3 2
}
```

Combining the `paramset` statement with the `sweep` analysis allows you to sweep multiple parameters simultaneously, for example, power supply voltage and temperature.

### Setting Sweep Limits

For all analyses that support sweeping, you specify the sweep limits with the parameters in the following table:

| Parameter           | Value                                                  | Comments                                                                             |
|---------------------|--------------------------------------------------------|--------------------------------------------------------------------------------------|
| <code>start</code>  | Start of sweep value (Default=0)                       | <code>start</code> and <code>stop</code> are used together to specify sweep limits.  |
| <code>stop</code>   | End of sweep value                                     |                                                                                      |
| <code>center</code> | Center value of sweep                                  | <code>center</code> and <code>span</code> are used together to specify sweep limits. |
| <code>span</code>   | Span of sweep (Default=0)                              |                                                                                      |
| <code>step</code>   | Step size for linear sweeps                            | <code>step</code> and <code>lin</code> are used to specify linear sweeps.            |
| <code>lin</code>    | Number of steps for linear sweeps (Default is 50)      |                                                                                      |
| <code>dec</code>    | Number of points per decade for log sweeps             | <code>dec</code> and <code>log</code> are used to specify logarithmic sweeps.        |
| <code>log</code>    | Number of steps for logarithmic sweeps (default is 50) |                                                                                      |
| <code>values</code> | Array of sweep values                                  | <code>values</code> specifies each sweep value with a vector of values.              |

If you do not specify the step size, the sweep is linear when the ratio of the stop to the start values is less than 10 and logarithmic when this ratio is 10 or greater. If you specify sweep limits and a `values` array, the points for both are merged and sorted.

### Examples of Parameter Sweep Requests

This `sweep` statement uses braces to bound the child analyses statements.

```
swp sweep param=temp values=[-50 0 50 100 125] {
 oppoint dc oppoint=logfile
}
```

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This statement specifies a linear sweep of frequencies from 0 to 0.3 MHz with 100 steps.

```
Sparams sp stop=0.3MHz lin=100
```

The previous statement could be written like this and achieve the same result.

```
Sparams sp center=0.15MHz span=0.3MHz lin=100
```

This statement specifies a logarithmic sweep of frequencies from 1 kHz through 1 GHz with 10 steps per decade.

```
cmLoopGain ac start=1k stop=1G dec=10
```

This statement is identical to the previous one except that the number of steps is set to 55.

```
cmLoopGain ac start=1k stop=1G log=55
```

This statement specifies a linear sweep of temperatures from 0 to 50 degrees in 1-degree steps. The frequency for the analysis is 1 kHz.

```
XferVsTemp xf start=0 stop=50 step=1 probe=Rload param=temp freq=1kHz
```

This statement uses a vector to specify sweep values for device `VCC`. The values specified for the sweep are 0, 2, 6, 7, 8 and 10.

```
SwpVccDC dc dev=Vcc values=[0 2 6 7 8 10]
```

### Distributed Sweep

You can use the `distribute` option with the sweep statement to distribute a sweep analysis to further speed up the run time for sweep analysis by using more computer cores across multiple computers. You can use the `distribute` option with possible values of `fork`, `rsh`, `ssh`, `lsf`, and `sge` to specify the method to be used to launch the child processes. In addition, you can use the `numprocesses` option to specify the number of child processes to be launched for each job.

In distributed sweep analysis, the master process splits the job into the number of tasks specified using the `numprocesses` option. Each subtask is simulated into its own child subprocess. Once a child process is completed, the results are returned and the master process merges the results including the raw files.

For `rsh` and `ssh` methods, you also need to specify the list of hosts to be used for the subprocesses using the `+hosts` command-line option.

For LSF and SGE methods, you need to use the `bsub` and `qsub` options respectively, to submit the job requests.

If any of the child process fails and you still want to have a scalar file by combining the distributed sweep results, you can set the following environment variable:

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```
setenv CDS_MMSIM_DISTRIBUTED_SWEEP_MERGE_RESULTS_ONLY
```

If a sweep analysis is defined in the netlist and the `+mp <numprocesses>` command-line option is used, Spectre automatically detects the farm environment (LSF, SGE, RTDA, or Network Computer) and distributes the sweep analysis to the specified number of child processes. If a farm environment is not detected, Spectre uses the `fork` option to distribute a sweep analysis by creating multiple jobs on a single system.

## Monte Carlo Analysis

The `montecarlo` analysis is a swept analysis with associated child analyses similar to the sweep analysis (see `spectre -h sweep`). The Monte Carlo analysis refers to “statistics blocks” where statistical distributions and correlations of netlist parameters are specified. (Detailed information on statistics blocks is given in [Specifying Parameter Distributions Using Statistics Blocks](#).) For each iteration of the Monte Carlo analysis, new pseudorandom values are generated for the specified netlist parameters (according to their specified distributions) and the list of child analyses are then executed.

The Cadence design environment Monte Carlo option allows for scalar measurements to be linked with the Monte Carlo analysis. Calculator expressions are specified that can be used to measure circuit output or performance values (such as the slew rate of an operational amplifier). During a Monte Carlo analysis, these measurement statement results vary as the netlist parameters vary for each Monte Carlo iteration and are stored in a scalar data file for post processing. By varying the netlist parameters and evaluating these measurement statements, the Monte Carlo analysis becomes a tool that allows you to examine and predict circuit performance variations that affect yield.

The statistics blocks allow you to specify batch-to-batch (process) and per- instance (mismatch) variations for netlist parameters. These statistically varying netlist parameters can be referenced by models or instances in the main netlist and can represent IC manufacturing process variation or component variations for board-level designs. The following description gives a simplified example of the Monte Carlo analysis flow:

```
perform nominal run if requested
if any errors in nominal run then stop
for each Monte Carlo iteration {
 if process variations specified then
 apply "process" variation to parameters
 if mismatch variations specified then
 for each subcircuit instance {
 apply "mismatch" variation to parameters
 }
 for each child analysis {
 run child analysis
 evaluate any export statements and
 store results in a scalar data file
 }
}
```

The following is the syntax for the Monte Carlo analysis:

```
Name montecarlo parameter=value ... {
 analysis statements ...
 export statements ...
}
```

The Monte Carlo analysis

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- Refers to the statistics block(s) for how and which netlist parameters to vary
- Generates statistical variation (random numbers according to the specified distributions)
- Runs the specified child analyses (similar to the Spectre nested sweep analysis), where the child analyses are either
  - Multiple data-producing child analyses (such as DC or AC analyses)
  - A single sweep child analysis, which itself has child analyses

- Calculates the export quantities

Each Monte Carlo run processes `export` statements that implicitly refer to the result of the child analyses. These statements calculate scalar circuit output values for performance characteristics, such as slew rate.

- Organizes the export data appropriately

Scalar data, such as bandwidth or slew rate, is calculated from an `export` statement and saved to an ASCII file, which can be used later for plotting a histogram or scattergram.

- After the Monte Carlo analysis is complete, all parameters are returned to their original values.

### Monte Carlo Analysis Parameters

You use the following parameters for Monte Carlo analysis.

#### Analysis Parameters

---

| Parameter                    | Description                                                                                                                                                                                                                                                                                                 |
|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>numruns=100</code>     | Number of Monte Carlo iterations to perform (not including nominal).                                                                                                                                                                                                                                        |
| <code>firstrun=1</code>      | Starting iteration number.                                                                                                                                                                                                                                                                                  |
| <code>runpoints=[...]</code> | Specifies the iteration indices to be simulated. Two types of settings are accepted; integers and ranges. For example, <code>runpoints=[10 range(15, 18) 20]</code> is an acceptable setting. It specifies that simulation needs to be performed for the 10th, 15th, 16th, 17th, 18th, and 20th iterations. |



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| Parameter                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>saverunpointsfile</code>  | Saves the file that contains the actual run points (iteration indices).                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>loadrunpointsfile</code>  | Loads the file that contains the run points (iteration indices) to be simulated.                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <code>variations=process</code> | Level of statistical variation to apply. Possible values are <code>process</code> , <code>mismatch</code> , or <code>all</code> .                                                                                                                                                                                                                                                                                                                                                                                                           |
| <code>sampling=standard</code>  | Method of statistical sampling to apply. Possible values are <code>standard</code> , <code>lhs</code> , and <code>lds</code> .                                                                                                                                                                                                                                                                                                                                                                                                              |
| <code>numbins=0</code>          | Number of bins for <code>lhs</code> (latin-hypercube) method. The number is checked against <code>numruns + firstrun - 1</code> , and <code>Max( numbins, numruns + firstrun - 1 )</code> is used for the <code>lhs</code> .                                                                                                                                                                                                                                                                                                                |
| <code>seed</code>               | Optional starting seed for random number generator.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <code>config</code>             | Specifies a <code>yaml</code> file to set up the monte carlo configurations.                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <code>scalarfile</code>         | Output file that will contain output scalar data.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <code>paramfile</code>          | Output file that will contain output scalar data labels.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <code>dut=[...]</code>          | If set, then the specified subcircuit or device instances will have process and mismatch variations applied, the unspecified instances will only have process variations applied. All subcircuits or devices instantiated under this instance will also have process and mismatch variations enabled. By default, mismatch variation is applied to all subcircuit or device instances in the design and process is applied globally. This parameter allows the testbench to change and not affect the variations seen by the actual design. |
| <code>ignore=[...]</code>       | If set, no variation is applied to the specified subcircuit or device instance(s). All subcircuits or devices instantiated under this instance will also have no variation enabled. By default, mismatch is applied to all subcircuit or device instances in the design and process is applied globally.                                                                                                                                                                                                                                    |
| <code>dutparams=[...]</code>    | If set, only the specified statistical parameters have process and mismatch variations applied.                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <code>ignoreparams=[...]</code> | If set, the specified statistical parameters are excluded from applying process and mismatch variation.                                                                                                                                                                                                                                                                                                                                                                                                                                     |

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| Parameter                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>json</code>                  | Output a json file containing the variation and analysis settings. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>no</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <code>accuracyaware=summary</code> | <p>Specifies the mode of runtime monitoring and early termination of a Monte Carlo simulation. Possible values are:</p> <p><code>summary</code> - Prints the summary statistics in the Spectre log file only at the end of Monte Carlo simulation.</p> <p><code>iteration</code> - Prints the statistics of measurements in the Spectre log file after each step of the Monte Carlo analysis.</p> <p><code>autostop</code> - Terminates the simulation based on the criteria specified using the <code>minmaxpairs</code> and <code>smooththresh</code> options.</p> <p>When you specify <code>accuracyaware=autostop</code>, you must also specify the <code>minmaxpairs [ x1_min x1_max....]</code> option, which defines pairs of values that correspond to <code>oceanEval</code> expression defined in the Monte Carlo statement.</p> |
| <code>minmaxpairs [...]</code>     | Pairs of values that are used to specify the <code>min</code> and <code>max</code> measurements defined in ocean expressions. The simulation is terminated when the current iteration generates a measurement that resides outside the region of <code>[min max]</code> . It is not necessary that the number of pairs is equal to the number of measurements. However, each pair must be aligned with the corresponding ocean measurement. Extra number of pairs are ignored when the simulation is terminated. This parameter is active only when the <code>accuracyaware</code> parameter is set to <code>autostop</code> .                                                                                                                                                                                                             |
| <code>smooththresh=0.0</code>      | Specifies the smoothness threshold of an ocean measurement. The average takes place within consecutive non-overlapping 200 iteration windows. The recommended value is 1e-4 for a reasonably converged signal average. This parameter is active only when the <code>accuracyaware</code> parameter is set to <code>autostop</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

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| Parameter                    | Description                                                                                                                                                                                                                                               |
|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>method=standard</code> | Method used to run the Monte Carlo analysis. Possible values are:<br><br><code>standard</code> : Runs the standard Monte Carlo analysis.<br><br><code>VADE</code> : Runs Monte Carlo analysis on a variation-aware design with varying device parameters. |

### Saving Process Parameters

| Parameter                         | Description                                                                                                                                             |
|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>saveprocessparams</code>    | Whether or not to save scalar data for statistically varying process parameters which are subject to process variation. Possible values are no or yes.  |
| <code>processscalarfile</code>    | Output file that will contain process parameter scalar data.                                                                                            |
| <code>processparamfile</code>     | Output file that will contain process parameter scalar data labels.                                                                                     |
| <code>saveprocessvec=[...]</code> | Array of statistically varying process parameters (which are subject to process variation) to save as scalar data in <code>`processscalarfile'</code> . |

### Saving Mismatch Parameters

| Parameter                          | Description                                                                                                                                                                             |
|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>savemismatchparams=no</code> | Whether or not to save scalar data for statistically varying mismatch parameters which are subject to mismatch variation. Possible values are no or yes. Possible values are no or yes. |
| <code>mismatchscalarfile</code>    | Output file that will contain mismatch parameter scalar data.                                                                                                                           |
| <code>mismatchparamfile</code>     | Output file that will contain mismatch parameter scalar data labels.                                                                                                                    |
| <code>dumpdependency</code>        | Whether or not to save the dependency map. Possible values are <code>none</code> and <code>mismatch</code> .                                                                            |

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|                                   |                                                                                                                        |
|-----------------------------------|------------------------------------------------------------------------------------------------------------------------|
| <code>dependencymapfile</code>    | Output file that contains a dependency map that indicates the pairing of mismatch parameters and subcircuit instances. |
| <code>dependencyscalarfile</code> | Output random numbers to a file that are used by mismatch parameters.                                                  |
| <code>dependencyparamfile</code>  | Output the mapping from the mismatch parameters to the corresponding subcircuit instances to a file.                   |

---

### Flags

| Parameter                              | Description                                                                                                                                                                                                                                                                                                                   |
|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>donominal=yes</code>             | Whether or not to perform nominal run. Possible values are no or yes.                                                                                                                                                                                                                                                         |
| <code>addnominalresults=no</code>      | Whether or not to add nominal run results to MC run results. Possible values are no or yes.                                                                                                                                                                                                                                   |
| <code>paramdumpmode=no</code>          | Whether or not to full dump process/mismatch parameters information. Possible values are no or yes.                                                                                                                                                                                                                           |
| <code>dumpseed=no</code>               | Whether or not to dump seed parameters information. Possible values are no or yes.                                                                                                                                                                                                                                            |
| <code>nullmfactorcorrelation=no</code> | Controls the mismatch variation correlation of parallel devices defined by m-factor. If set to <code>yes</code> , devices are assumed to get uncorrelated mismatch variations. If set to <code>no</code> , devices are assumed to get the same mismatch variation. Possible values are <code>no</code> and <code>yes</code> . |
| <code>appendsd=no</code>               | Whether or not to append scalar data. Possible values are no or yes.                                                                                                                                                                                                                                                          |
| <code>savefamilyplots=no</code>        | Whether or not to save data for family plots. If <code>yes</code> , this could require a lot of disk space. Possible values are no or yes.                                                                                                                                                                                    |
| <code>savedatainseparatedir=no</code>  | Whether or not to save data for an each plot in a separate directory. Possible values are <code>no</code> or <code>yes</code> .<br><br><b>Note:</b> Setting this parameter to <code>yes</code> may require a lot of disk space.                                                                                               |

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| Parameter          | Description                                                                                                                                                                                                                                                                                         |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| evaluationmode=no  | If set to <code>yes</code> , dumps random numbers used in montecarlo analysis without running any enclosed analyses. Possible values are <code>no</code> and <code>yes</code> .                                                                                                                     |
| diskstorage=no     | If set to <code>yes</code> , mismatch data is stored on hard drive instead of memory while running a monte carlo analysis. Possible values are <code>no</code> and <code>yes</code> .                                                                                                               |
| wfseparation=no    | If set to <code>yes</code> , a separate directory for nominal run is created by the name <code>nom</code> and the directory names of individual iterations are simplified by removing the leading analysis names. Possible values are <code>no</code> and <code>yes</code> .                        |
| seedscramble=no    | If set to <code>yes</code> , a scrambling procedure is applied to the seed value to generate a better random number sequence in the sense of randomness. Possible values are <code>no</code> and <code>yes</code> .                                                                                 |
| distribute         | Distributes a montecarlo analysis to reduce simulation time by using more computer cores across multiple computers. Possible values are <code>no</code> , <code>fork</code> , <code>rsh</code> , <code>ssh</code> , <code>lsf</code> , <code>sge</code> , <code>nc</code> , and <code>auto</code> . |
| numprocesses       | Specifies the number of jobs in distributed mode.                                                                                                                                                                                                                                                   |
| usesamesequence=no | If set to <code>yes</code> , the random sequence is maintained for a seed even if there is an empty dut/ignore list. Possible values are <code>no</code> or <code>yes</code> .                                                                                                                      |
| rngversion         | Version of random number generator. Possible values are <code>default</code> and <code>v151</code> .                                                                                                                                                                                                |

### Annotation Parameters

| Parameter      | Description                                                                                                                    |
|----------------|--------------------------------------------------------------------------------------------------------------------------------|
| annotate=sweep | Degree of annotation. Possible values are <code>no</code> , <code>title</code> , <code>sweep</code> , or <code>status</code> . |
| title          | Analysis title.                                                                                                                |

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| Parameter                      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>ignoremode</code>        | <p>Controls the type of variation that is applied to ignored devices when variations = all. By default, the variation seen by ignored devices depends on whether the dut or ignore parameter is used.</p> <p>If dut is used, then all non-DUT devices will get process variation.</p> <p>If the ignore parameter is used, then devices in the ignore list will use nominal values, that means the devices have no variation.</p> <p>When <code>ignoremode = nominal   process</code>, the behavior is consistent for both dut and ignore.</p> <p>If <code>ignoremode = nominal</code>, then all devices in the ignore list or devices that are not in the dut list will use nominal values.</p> <p>If <code>ignoremode = process</code>, all devices in the ignore list or devices that are not in the dut list have process variation.</p> <p>Possible values are <code>default</code>, <code>nominal</code>, <code>process</code> and <code>both</code>.</p> |
| <code>stdscale</code>          | <p>Scale the standard deviation by the specified value. The default value is 1.0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <code>process_stdscale</code>  | <p>Scale the standard deviation of process variation parameters by the specified value. The default value is 1.0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <code>mismatch_stdscale</code> | <p>Scale the standard deviation of mismatch variation parameters by the specified value. The default value is 1.0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <code>dist=default</code>      | <p>Force all MonteCarlo random variation distributions to the specified type. Possible values are <code>default</code>, <code>unif</code>, <code>gauss</code> and <code>gamma</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>ignore_type=[...]</code> | <p>If set, no variation is applied to the specified types. The default value is <code>none</code>. Possible values are <code>none</code> and <code>memcell</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <code>iterprevic</code>        | <p>Specifies whether the MC iterations use the previous IC solutions. Possible values are <code>none</code> and <code>nominal</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>dumpvop</code>           | <p>Specifies whether to dump process/mismatch with the new order. Possible values are <code>no</code> and <code>yes</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

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| Parameter                      | Description                                                                                                                                                                                                                                                                           |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>processdist=none</code>  | Set all MonteCarlo process variation distributions to be the specified type. The default type is none.<br><br>Possible values are <code>none</code> , <code>gauss</code> , <code>lnorm</code> , <code>unif</code> , <code>sunif</code> , <code>lunif</code> and <code>gamma</code> .  |
| <code>mismatchdist=none</code> | Set all MonteCarlo mismatch variation distributions to be the specified type. The default type is none.<br><br>Possible values are <code>none</code> , <code>gauss</code> , <code>lnorm</code> , <code>unif</code> , <code>sunif</code> , <code>lunif</code> and <code>gamma</code> . |
| <code>loadvariationfile</code> | Load file in csv format that contains the variation (iteration indices) to be simulated.                                                                                                                                                                                              |

### Specifying the First Iteration Number

The advantages of using the `firstrun` parameter to specify the first iteration number are as follows:

- You can reproduce a particular run from a previous experiment when you know the starting seed and run number but not the corresponding seed.
- If you are a standalone Spectre user, you can run a Monte Carlo analysis of 100 runs, analyze the results, decide they are acceptable, and then decide to do a second analysis of 100 runs to give a total of 200 runs. By specifying the `firstrun=101` for the second analysis, the Spectre simulator retains the data for the first 100 runs and runs only the second 100 runs. This gives the same results and random sequence as if you ran just a single Monte Carlo analysis of 200 runs.

### Sample Monte Carlo Analyses

For a Monte Carlo analysis, the Spectre simulator performs a nominal run first, if requested, calculating the specified outputs. If there is any error in the nominal run or in evaluating the `export` statements after the nominal run, the Monte Carlo analysis stops.

If the nominal run is successful, then, depending on how the `variations` parameter is set, the Spectre simulator applies process variations to the specified parameters and mismatch variations (if specified) to those parameters for each subcircuit instance. If the `export` statements are specified, the corresponding performance measurements are saved as a new file or appended to an existing file.

The following Monte Carlo analysis statement specifies (using the default) that a nominal analysis is performed first. The `sweep` analysis (and all child analyses) are performed, and `export` statements are evaluated. If the nominal analysis fails, the Spectre simulator gives an error message and will not perform the Monte Carlo analysis. If the nominal analysis succeeds, the Spectre simulator immediately starts the Monte Carlo analysis. The `variations` parameter specifies that only process variations (`variations=process`) are applied; this is useful for looking at absolute performance spreads. There is a single child sweep analysis (`sw1`) so that for each Monte Carlo run, the Spectre simulator sweeps the temperature, performs the dc and transient analyses, and calculates the slew rate. The output of the slew rate calculation is saved in the scalar data file.

```
mc1 montecarlo variations=process seed=1234 numruns=200 {
 sw1 sweep param=temp values=[-50 27 100] {
 dcop1 dc // a "child" analysis
 tran1 tran start=0 stop=1u// another "child" analysis
 // export calculations are sent to the scalar data file
 export slewrate=oceanEval("slewRate(v(\"vout\"),10n,t,30n,t,10,90)")
 }
}
```

The following Monte Carlo analysis statement applies only mismatch variations, which are useful for detecting spreads in differential circuit applications. It does not perform a nominal run.

**Note:** No temperature sweep is performed.

```
mc2 montecarlo donominal=no variations=mismatch seed=1234 numruns=200 {
 dcop2 dc
 tran2 tran start=0 stop=1u
 export slewrate=oceanEval("slewRate(v(\"vout\"),10n,t,30n,t,10,90)")
}
```

The following Monte Carlo analysis statement applies both process and mismatch variations:

```
mc3 montecarlo saveprocessparams=yes variations=all numruns=200 {
 dcop3 dc
 tran3 tran start=0 stop=1u
 export slewrate=oceanEval("slewRate(v(\"vout\"),10n,t,30n,t,10,90)")
}
```

### Specifying Parameter Distributions Using Statistics Blocks

The statistics blocks are used to specify the input statistical variations for a Monte Carlo analysis. A statistics block can contain one or more process blocks (which represent batch-to-batch type variations) and/or one or more mismatch blocks (which represent on-chip or device mismatch variations), in which the distributions for parameters are specified. Statistics blocks can also contain one or more correlation statements to specify the correlations between specified process parameters and/or to specify correlated device instances (such as matched pairs). Statistics blocks can also contain a `truncate` statement that can be used for generating truncated distributions.



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The statistics block contains the distributions for parameters:

- Distributions specified in the process block are sampled once per Monte Carlo run, are applied at global scope, and are used typically to represent batch-to-batch (process) variations.
- Distributions specified in the mismatch block are applied on a per-subcircuit instance basis, are sampled once per subcircuit instance, and are used typically to represent device-to-device (on chip) mismatch for devices on the same chip.

When the same parameter is subject to both process and mismatch variations, the sampled process value becomes the mean for the mismatch random number generator for that particular parameter.

**Note:** Statistics blocks can be specified using combinations of the Spectre keywords `statistics`, `process`, `mismatch`, `vary`, `truncate`, and `correlate`. Braces (`{}`) are used to delimit blocks.

The following example shows some sample statistics blocks, which are discussed after the example along with syntax requirements.

```
// define some netlist parameters to represent process parameters
// such as sheet resistance and mismatch factors
parameters rshsp=200 rshpi=5k rshpi_std=0.4K xisn=1 xisp=1 xxx=20000 uuu=200

// define statistical variations, to be used
// with a MonteCarlo analysis.
statistics {
 process { // process: generate random number once per MC run
 vary rshsp dist=gauss std=12 percent=yes
 vary rshpi dist=gauss std=rshpi_std // rshpi_std is a parameter
 vary xxx dist=lnorm std=12
 vary uuu dist=unif N=10 percent=yes
 ...
 }
 mismatch { // mismatch: generate a random number per instance
 vary rshsp dist=gauss std=2
 vary xisn dist=gauss std=0.5
 vary xisp dist=gauss std=0.5
 }
 // some process parameters are correlated
 correlate param=[rshsp rshpi] cc=0.6
 // specify a global distribution truncation factor
 truncate tr=6.0 // +/- 6 sigma
}

// a separate statistics block to specify correlated (i.e. matched)
// components
// where m1 and m2 are subckt instances.
statistics {
 correlate dev=[m1 m2] param=[xisn xisp] cc=0.8
}

// a separate statistics block to specify correlation with wildcard, where
// 'I*.M3' matches multiple subckt instances, for examples, I1.M3, I2.M3, I3.M3,
```

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```
etc..
// Only the asterisk (*) is recognized as a valid wildcard symbol.
statistics {
 correlate dev=[I*.M3] param=[misx mixy] cc=0.8
}
```

**Note:** You can specify the same parameter (for example, `rshsp`) for both process and mismatch variations.

In the process block, the process parameter `rshsp` is varied with a Gaussian distribution, where the standard deviation is 12 percent of the nominal value (`percent=yes`). When `percent` is set to `yes`, the value for the standard deviation (`std`) is a percentage of the nominal value. When `percent` is set to `no`, the specified standard deviation is an absolute number. This means that parameter `rshsp` should be varied with a normal distribution, where the standard deviation is 12 percent of the nominal value of `rshsp`. The nominal or mean value for such a distribution is the current value of the parameter just before the Monte Carlo analysis starts. If the nominal value of the parameter `rshsp` was 200, the preceding example specifies a process distribution for this parameter with a Gaussian distribution with a mean value of 200 and a standard deviation of 24 (12 percent of 200). The parameter `rshpi` (sheet resistance) varies about its nominal value with a standard deviation of 0.4 K-ohms/square.

In the mismatch block, the parameter `rshsp` is then subject to *further* statistical variation on a per-subcircuit instance basis for on-chip variation. Here, it varies a little for each subcircuit instance, this time with a standard deviation of 2. For the first Monte Carlo run, if there are multiple instances of a subcircuit that references parameter `rshsp`, then (assuming `variations=all`) it might get a process random value of 210, and then the different instances might get random values of 209.4, 211.2, 210.6, and so on. The parameter `xisn` also varies on a per-instance basis, with a standard deviation of 0.5. In addition, the parameters `rshsp` and `rshpi` are correlated with a correlation coefficient (`cc`) of 0.6.

The `.mcdat` file, by default, displays the following statistics parameters in the Statistics section: `max`, `min`, `mean`, `variance`, `stddev`, `avgdev`, `avgdev`, and `failedtimes`. You can set the `mc_stat_list` option parameter to `all` to output all statistical parameters in the file.

The following is an example of the `.mcdat` file. The parameters in blue are added when you set the value of `mc_stat_list` to `all`.

Statistics:

|          |             |    |             |
|----------|-------------|----|-------------|
| max      | 1.68571e-08 | 27 | 4.42243e-09 |
| min      | 1.39394e-08 | 27 | 4.03428e-09 |
| mean     | 1.55027e-08 | 27 | 4.19754e-09 |
| variance | 3.36186e-19 | 0  | 7.31927e-21 |
| stddev   | 5.79816e-10 | 0  | 8.55527e-11 |

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|                 |             |     |             |
|-----------------|-------------|-----|-------------|
| avgdev          | 4.67287e-10 | 0   | 6.99047e-11 |
| skewness        | 0.0611099   | NaN | 0.260798    |
| kurtosis        | -0.213995   | NaN | -0.403713   |
| Q1              | 1.50883e-08 | 27  | 4.13173e-09 |
| median          | 1.55056e-08 | 27  | 4.19708e-09 |
| Q3              | 1.58615e-08 | 27  | 4.25678e-09 |
| CI_mean_2.5%    | 1.53877e-08 | 27  | 4.18057e-09 |
| CI_mean_97.5%   | 1.56178e-08 | 27  | 4.21452e-09 |
| CI_stddev_2.5%  | 5.09082e-10 | 0   | 7.51159e-11 |
| CI_stddev_97.5% | 6.73558e-10 | 0   | 9.93845e-11 |
| failedtimes     | 0           | 0   | 0           |

### Multiple Statistics Blocks

You can use multiple statistics blocks, which accumulate or overlay each other. Typically, process variations, mismatch variations, and correlations between process parameters are specified in a single statistics block. This statistics block can be included in a “process” include file, such as the ones shown in the example in [“Process Modeling Using Inline Subcircuits”](#) on page 110. A second statistics block can be specified in the main netlist where actual device instance correlations are specified as matched pairs.

The following statistics block can be used to specify the correlations between matched pairs of devices and probably is placed or included into the main netlist by the designer. These statistics are used in addition to those specified in the statistics block in the preceding section so that the statistics blocks “overlay” or “accumulate.”

```
// define correlations for "matched" devices q1 and q2
statistics {
 correlate dev=[q1 q2] param=[XISN...] cc=0.75
}
```

**Note:** You can use a single statistics block containing both sets of statements; however, it is often more convenient to keep the topology-specific information separate from the process-specific information.

## Specifying Distributions

Parameter variations are specified using the following syntax:

```
vary PAR_NAME dist=type {std=<value> | N=<value>} {percent=yes|no}
```

Four types of parameter distributions are available: Gaussian, log normal, and uniform, corresponding to the *type* keywords `gauss`, `lnorm`, `gamma`, and `unif`, respectively. For both `gauss` and `lnorm` distributions, you specify a standard deviation using the `std` keyword.

**Note:** You can also specify a global parameter as a value for `dist`. For example:

```
parameters DIST_snd=gauss
statistics {
 process {
 vary AGIDL_snd dist=DIST_snd std=1
 }
}
```

The following distributions (and associated parameters) are supported:

### ■ Gaussian

This distribution is specified using `dist=gauss`. For the Gaussian distribution, the mean value is taken as the current value of the parameter being varied, giving a distribution denoted by Normal(mean,std). Using the example in [“Specifying Parameter Distributions Using Statistics Blocks.”](#) parameter `rshpi` is varied with a distribution of Normal (5k,0.4k). The nominal value for the Gaussian distribution is the value of the parameter before the Monte Carlo analysis is run. The standard deviation can be specified using the `std` parameter. If you do not specify the `percent` parameter, the standard deviation you specify is taken as an absolute value. If you specify `percent=yes`, the standard deviation is calculated from the value of the `std` parameter multiplied by the nominal value and divided by 100; that is, the value of the `std` parameter specifies the standard deviation as that percentage of the nominal value.

**Note:** If `std=0` or `std=<param_name>=0` is found in the statistics block, Spectre generates an error. You can specify the `ignorezerovar=yes` parameter in the `options` statement to bypass this check.

### ■ Log normal

This distribution is specified using `dist=lnorm`. The log normal distribution is denoted by

$$\log(x) = \text{Normal}(\log(\text{mean}), \text{std})$$

where  $x$  is the parameter being specified as having a log normal distribution.

**Note:** `log()` is the natural logarithm function. For parameter `xxx` in the example in [Specifying Parameter Distributions Using Statistics Blocks](#), the process variation is according to

```
log(xxx) = Normal(log(20000), 12)
```

The nominal value for the log normal distribution is the value of the parameter before the Monte Carlo analysis is run. If you specify a normal distribution for a parameter `P1` whose value is 5000 and you specify a standard deviation of 100, the actual distribution is produced such that

```
log(P1) = N(log(5000), 100)
```

### ■ Uniform

This distribution is specified using `dist=unif`. The uniform distribution for parameter `x` is generated according to

```
x = unif(mean-N, mean+N)
```

such that the mean value is the nominal value of the parameter `x`, and the parameter is varied about the mean with a range of  $\pm N$ . The standard deviation is not specified for the uniform distribution, but its value can be calculated from the formula `std=N/sqrt(3)`. The nominal value for the uniform distribution is the value of the parameter before the Monte Carlo analysis is run. The uniform interval is specified using the parameter `N`. For example, specifying `dist=unif N=5` for a parameter whose value is 200 results in a uniform distribution in the range  $200 \pm N$ , that is, from 195 to 205. You can also specify `percent=yes`, in which case, the range is  $200 \pm N\%$ , that is, from 190 to 210.

If the parameters `max` and `min` are specified, the nominal value is calculated as  $(\text{max} + \text{min}) / 2$  and the uniform interval is calculated as  $(\text{max} - \text{min}) / 2$ .

### ■ Log uniform

This distribution is specified using `dist=lunif`. The log uniform distribution is denoted by

```
log(x) = (log(nominal_value) - N, log(nominal_value) + N)
```

Here, `x` is the parameter being specified as having a log uniform distribution. The nominal value (`nominal_value`) is defined as  $\text{min} * \sqrt{\text{max} / \text{min}}$  and the value of `N` is specified as  $\log(\sqrt{\text{max} / \text{min}})$ . The parameters `max` and `min` specify the distribution range.

### ■ Gamma

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Derived parameters that have their default values specified as expressions of other parameters cannot have distributions specified for them. Only parameters that have numeric values specified in their declaration can be subjected to statistical variation.

Parameters that are specified as correlated must have had an appropriate variation specified for them in the statistics block.

For example, if you have the parameters

```
XISN=XIS+XIB
```

you cannot specify distribution for `XISN` or a correlation of this parameter with another.

The `percent` flag indicates whether the standard deviation `std` or uniform range `N` are specified in absolute terms (`percent=no`) or as a percentage of the mean value (`percent=yes`). For parameter `uuu` in the example in [“Specifying Parameter Distributions Using Statistics Blocks,”](#) the mean value is 200, and the variation is  $200 \pm 10\% \cdot (200)$ , that is,  $200 \pm 20$ . For parameter `rshsp`, the process variation is given by `Normal( 200, 12%*(200) )`, that is, `Normal(200, 24)`. Cadence recommends that you do not use the `percent=yes` with the log normal distribution.

### Changing Parameter Distributions at Runtime

At times, you might want to reproduce the design failures with less MonteCarlo iterations and check the design robustness quickly. You can use the `dist=default|unif|gauss` parameter to force all parameter distributions to a specified type. In addition, you can use the `stdscale` parameter scale the deviation by a specified value.

The following examples show how to use `stdscale` and `dist` options to force a parameter distribution to the specified type.

#### ■ `stdscale=k`

Consider a scenario where you have the following in the statistics block:

```
statistics {
 mismatch {
 vary mymismatch1 dist=gauss std=1
 }
}
```

If you specify `stdscale=k` in the MonteCarlo statement, `std=1` of all random variables will be multiplied by `k`. For example, if you specify the following in the Montecarlo statement:

```
mcl montecarlo firstrun=1 numruns=5000 dist=unif stdscale=2 {
dc dc
```

```
}
```

the statistics block will change to:

```
statistics {
 mismatch {
 vary mymismatch1 dist=gauss std=1*k
 }
}
```

### ■ `dist=unif|gauss`

When you specify `dist=unif` or `dist=gauss`, distribution of all random variables is converted to `unif` or `gauss`.

Consider a scenario where you have the following in the statistics block:

```
statistics {
 mymismatch1 = p
 mismatch {
 vary mymismatch1 dist=gauss std=a
 }
}
```

If you specify the following MonteCarlo statement:

```
mcl montecarlo numruns=100 variations=mismatch seed=12345 stdscale=k dist=unif
```

the statistics block will change to:

```
statistics {
 mymismatch1 = p
 mismatch {
 vary mymismatch1 dist=unif N=a*sqrt(3)*k
 }
}
```

**Note:** When `stdscale=k` and `dist=unif`, is specified and if one parameter follows `gauss`, `std=a`, `mean=b`, Spectre automatically converts it into uniform distribution with `mean=b`, `unif(b-sqrt(3)*a*k, b+sqrt(3)*a*k)`.

**Note:** By transforming the Gaussian distribution to Uniform, you can identify the design failure at high sigma-corner with small number of samples. However, you cannot predict the yield of the design with this approach.

## Truncation Factor

The default truncation factor for Gaussian distributions (and for the Gaussian distribution underlying the log normal distribution) is 4.0 sigma. Randomly generated values that are outside the range of mean  $\pm$  4.0 sigma are automatically rejected and regenerated until they fall inside the range. If the truncation factor is less than 0, Spectre does not generate truncated distributions and generates a warning. If the truncation factor is specified as 0, then Spectre generates an error.

You can change the truncation factor using the `truncate` statement. The following is the syntax:

```
truncate tr=value
```

The value of the truncation factor can be a constant or an expression. In addition, you can specify the truncation factor in the process and mismatch blocks. However, if the truncation factor is not specified in the process or mismatch block, then the truncation factor in the statistics block is considered.

**Note:** Parameter correlations can be affected by using small truncation factors.

## Correlation Statements

There are two types of correlation statements that you can use:

### ■ Process parameter correlation statements

The following is the syntax of the process parameter correlation statement:

```
correlate param=[list of parameters] cc=value
```

This allows you to specify a correlation coefficient between multiple process parameters. You can specify multiple process parameter correlation statements in a statistics block to build a matrix of process parameter correlations. During a Monte Carlo analysis, process parameter values are randomly generated according to the specified distributions and correlations.

### ■ Instance or mismatch correlation statements (matched devices)

The following is the syntax of the instance or mismatch correlation statement:

```
correlate dev=[list of subckt instances] {param=[list of parameters]}
cc=value
```

```
correlate dev=[<wildcard expr>] {param=[list of parameters]} cc=<value>
```

where the device or subcircuit instances to be matched are listed in *list of subckt instances*, or regular expressions with asterisk (\*) and *list of parameters* specifies exactly which parameters with mismatch variations are to be correlated. Use the instance mismatch correlation statement to specify correlations for particular



subcircuit instances. If a subcircuit contains a device, you can effectively use the instance correlation statements to specify that certain devices are correlated (matched) and give the correlation coefficient. You can optionally specify exactly which parameters are to be correlated by giving a list of parameters (each of which must have had distributions specified for it in a mismatch block) or by specifying no parameter list, in which case all parameters with mismatch statistics specified are correlated with the given correlation coefficient. The correlation coefficients are specified in the `<value>` field and must be between  $\pm 1.0$ .

**Note:** Correlation coefficients can be constants or expressions, as can `std` and `N` when specifying distributions.

### Characterization and Modeling

The following statistics blocks can be used with the example in “[Process Modeling Using Inline Subcircuits](#)” on page 110 if they are included in the main netlist, anywhere below the main `parameters` statement. These statistics blocks are meant to be used in conjunction with the modeling and characterization equations in the inline subcircuit example, for a Monte Carlo analysis only.

```
statistics {
 process {
 vary RSHSP dist=gauss std=5
 vary RSHPI dist=lnorm std=0.15
 vary SPDW dist=gauss std=0.25
 vary SNDW dist=gauss std=0.25
 }
 correlate param=[RSHSP RSHPI] cc=0.6
 mismatch {
 vary XISN dist=gauss std=1
 vary XBFN dist=gauss std=1
 vary XRSP dist=gauss std=1
 }
}

statistics {
 correlate dev=[R1 R2] cc=0.75
 correlate dev=[TNSA1 TNSA2] cc=0.75
}
```

### Creating same variation for same block in different simulations

At times, it may be necessary to use the same variation of a design in different simulations. This can be achieved by using identical subcircuit and instance definitions for the design in both simulations, and by ordering the netlist with the `options` statement, as shown below.

```
opt1 options sortinstance=yes
```

### Applying the Same Variation on an Instance or a Subset of an Instance

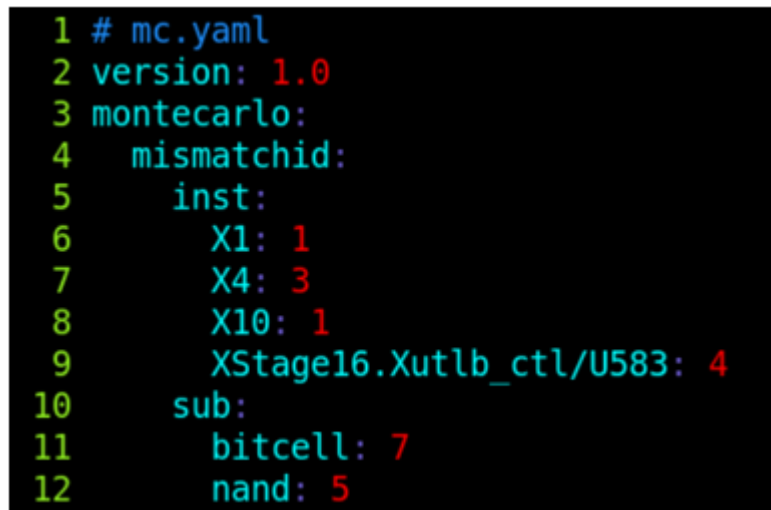
You can apply the same variation to an instance regardless of the testbench or the design hierarchy. In addition, if multiple instances of a cell are present in a design, you can set up the simulation such that all the instances or a subset of those instances get the same variation.

To do this, you can add a mismatch id to the instance in the design. If the mismatch id is consistent across all designs, the instance or the subsets of the instance will always have the same mismatch variation, assuming that the MC seed itself is also the same.

You can add the mismatch id in a file in YAML file format and add the YAML file in the monte carlo statement using the `config` parameter, as shown below.

```
mc1 montecarlo seed=123345 config="mc.yaml" {
 tr1 tran ...
}
```

The following is a sample YAML file.



```
1 # mc.yaml
2 version: 1.0
3 montecarlo:
4 mismatchid:
5 inst:
6 X1: 1
7 X4: 3
8 X10: 1
9 XStage16.Xutlb_ctl/U583: 4
10 sub:
11 bitcell: 7
12 nand: 5
```

In the above YAML file, there are two entries in the `mismatchid` block; one for instances and the other for subcircuits. All the instances of the subcircuit `bitcell` have a mismatch id 7, while the instances of `nand` have an id of 5. Instances `X1` and `X10` have the same mismatch id of 1, instance `X4` has an id of 3, while `XStage16.Xutlb_ctl/U583` has an id of 4.

Each mismatch id defines an independent mismatch variation sequence; instances with the same mismatch id share the same mismatch variations. This also applies to multiple netlists, that is, if we have an instance `X1` in `netlist1` that shares the same mismatch id with an instance `X11` in `netlist2`, and both monte carlo analyses have the same seed, then `X1` and `X11` will share the same mismatch variations even though they are in different runs and have different hierarchical names.

**Note:** The mismatch id feature works only with `sampling=standard`.

## Filtering the Variables Generated from the Monte Carlo Analysis

Spectre provides a plugin that you can use to filter the random variables generated from a Monte Carlo run to perform statistical simulation. The plugin accepts or rejects a variable generated from a monte carlo run based on its validity. If a sample is rejected, Spectre generates another sample to replace the rejected sample. The simulation starts only when all the samples are generated. The following is the plugin script:

```
struct mcRandomVariable {
 enum Type {
 normal = 0,
 uniform = 1,
 lognormal = 2
 };
 mcRandomVariable(const void *ptr) : dataPtr(ptr) {}
 const char *getInstName();
 const char *getParamName();
 Type getType();
 double getMean();
 double getStd();
 bool isProcess()
 {
 return strlen(getInstName()) == 0;
 }
private:
 const void *dataPtr;
};

class mciSampleFilter
{
public:
 virtual bool begin(std::vector<mcRandomVariable> &rVariables) = 0;
 virtual bool filter(std::vector<double> &rValues) = 0;
 virtual bool end() = 0;
};

extern "C" {
 int mciRegisterSampleFilter(mciSampleFilter *pFilter);
}
```

You can define your own filter class derived from the base class `mciSampleFilter`.

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- The `begin` method is called by Spectre at the beginning of the monte carlo analysis, with the vector of all random variables. It must return true to indicate that the plugin is ready to proceed.
- Next, Spectre calls the `filter` method multiple times with the vector of generated random values. It should return a true or false to indicate the values are accepted or rejected.
- The `end` is called by Spectre at the end of the monte carlo analysis.

You also need to add the following function to the plugin code. Spectre will then load the plugin and call this function. The function then registers the filter object using the `mciRegisterSampleFilter` function.

```
extern "C"
{
void
mciInstall(void)
{
 mySampleFilter *pFilter = new mySampleFilter;
 mciRegisterSampleFilter(pFilter);
}
}
```

Once the code is compiled into a shared library you can load the plugins into Spectre as follows:

### Using environment variable

```
export CDS_MMSIM_PLUGINS=${PATH_TO_MC_PLUGIN}/%O/lib/%B/libmcfilter.so
```

### On the command line

```
$ spectre -plugin ${PATH_TO_MC_PLUGIN}/%O/lib/%B/libmcfilter.so input.scs
```

**Note:** Currently, the filter plugin works only when `sampling=standard` or `sampling=lds`. In addition, the plugin currently does not support the MDL and MP flows.

## Distributed Monte Carlo Analysis

You can use the `distribute` option with the `montecarlo` statement to distribute a Monte Carlo analysis to further speed up the run time for the analysis by using more computer cores across multiple computers. The `distribute` option with possible values of `lsf`, `sge`, `rsh`, `ssh`, `fork`, `nc`, and `auto` is used to specify the method to be used to launch the child processes. You can use the `numprocesses` option to specify the number of child processes to be launched for each job.

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In distributed Monte Carlo analysis, the master process splits the job into the number of tasks specified using the `numprocesses` option. Each subtask is simulated in its own child subprocess. Once a child process is completed, it returns the results to the master process and the master process merges the results into a single file; including the scalar measurement files.

For `lsf` and `sgc` methods, you need to use the `bsub` and `qsub` options respectively, to submit the initial master run. The master process uses the same settings to split the job into child processes.

In general, the master and child processes run on the same queue. You can use the `CDS_MMSIM_MP_QUEUE` environment variable to direct the master to run the child processes in alternative queues.

For `rsh` and `ssh` methods, you need to specify the list of hosts to be used for the subprocess using the `+hosts` command-line option.

You can use the `fork` option to create multiple jobs on a single system.

The following example runs a 2000 point Monte Carlo analysis by splitting the run points into 20 subprocesses. The master process is launched using `bsub` with four cores reserved. Each child process is launched by the master using the same `bsub` command arguments.

```
mcl montecarlo numruns = 2000 distribute=lsf numprocesses=20
% bsub -R "(OSNAME==Linux) span[hosts=1]" -n 4 "spectre +aps input.scs"
```

The following example runs a 2000 point Monte Carlo analysis by splitting the run points into 20 subprocesses onto remote systems. The subprocesses are launched using the `rsh` method on three machines `host-1`, `host-2`, and `host-3`. Each subprocess uses one core.

```
mcl montecarlo numruns = 2000 distribute=rsh numprocesses=20
% spectre +aps -mt +hosts='host-1 host-2 host-3' input.scs
```

The following example is similar to the examples above, however, here, the master splits the 20 subprocesses on the same local machine. Each subprocess uses one core.

```
mcl montecarlo numruns = 2000 distribute=fork numprocesses=20
% spectre +aps -mt input.scs
```

If any of the child process fails and you still want to have a scalar file by combining the distributed Monte Carlo results, you can set the following environment variable:

```
setenv CDS_MMSIM_DISTRIBUTED_MONTECARLO_MERGE_RESULTS_ONLY
```

If a Monte Carlo analysis is defined in the netlist and the `+mp <numprocesses>` command-line option is used, Spectre automatically detects the farm environment (LSF, SGE, RTDA, or Network Computer) and distributes the montecarlo analysis to the specified number of child

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processes. If a farm environment is not detected, Spectre uses the `fork` option to distribute a Monte Carlo analysis by creating multiple jobs on a single system.

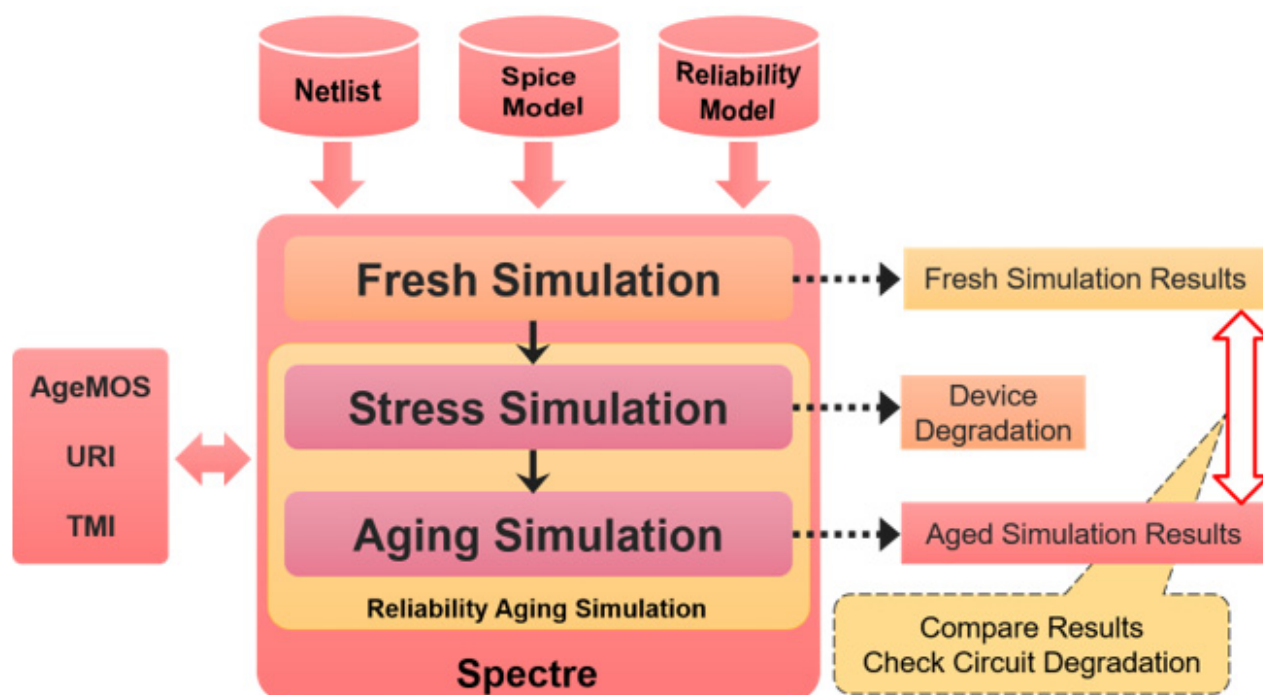
**Note:** Spectre APS supports distribution of Monte Carlo and Sweep analyses; however, any subset analysis defined within the Monte Carlo or Sweep analysis is not distributed.

**Note:** You cannot use relative path (such as `scalarfile=../monteCarlo/mcdata`) to specify the location of file in distributed montecarlo. This is because distributed results are saved in the root directory. If you use a relative path to specify the location, all child processes will refer to the same directory.

## Spectre Reliability Analysis

Spectre reliability analysis for HCI, NBTI, and/or PBTI is a two-phase simulation flow. The first phase, fresh and stress simulation, calculates the device age or degradation. The second phase, post-stress or aging simulation, simulates the degradation effect on the circuit performance based on the device degradation information obtained during the first phase of stress simulation.

The following figure shows the reliability simulation flow in Spectre:



### Reliability Simulation Block

Reliability simulation in Spectre is specified by using a reliability block, which is similar to the block statement that is used for Monte Carlo simulation.

A reliability block contains the following control statements:

- Reliability Control Statements
- Stress Statements
- Aging/Post-Stress Statements

## ■ Additional Notes

The following example shows how these statements should be specified within a reliability block:

```
reliability_run_name reliability [global_options]{
reliability control statements
stress statements
aging/post-stress statements
}
```

Any fresh simulation settings are provided before the reliability block statements. The reliability block then provides the stress and post-stress simulation.

**Note:** DC sweep is not supported inside the reliability block. If you add a DC sweep statement in the reliability block, Spectre generates an error during simulation.

**Note:** Starting with SPECTRE 19.1 ISR2, all Spectre X preset modes (cx, ax, mx, lx, and vx) support native reliability aging analysis.

## Reliability Control Statements

The reliability control statements control the reliability simulation. The RelXpert control statement syntax is also supported in the reliability block. For detailed information on the reliability control statements, see the [Reliability Control Statements Reference](#) section.

**Note:** Spectre XPS supports native reliability analysis. The Spectre XPS native reliability analysis supports the following control statements:

- age
- report\_model\_param
- relx\_tran
- maskdev
- agelevel\_only

Currently, only the agemos model is supported.

## Stress Statements

The stress statements specify or change the stress conditions, and run the stress simulation. Stress statements can be categorized as stress testbench/vectors and simulation statements. Stress testbench statements specify the stress conditions during the stress



simulation phase. This is done through `alter` statements. Stress testbench statements are optional. Stress simulation is performed through another transient statement. A transient statement is required for running stress simulation.

**Note:** Only transient analysis is supported with the stress statement.

### Aging/Post-Stress Statements

The aging statements specify or change the post-stress or end-of-life simulation conditions, and run the aging simulation. Similar to stress statements, the end-of-life conditions are specified through `alter` statements and run with another transient simulation. You can use the `aging_analysis_name` reliability control statement to specify dc, ac, noise, info, stb, S-parameter, hb, hbnoise, pss, pnoise, pac, or pxf analysis in addition to transient analysis.

**Note:** When you use the `simmode` reliability control statement, the `aging_analysis_name` control statement is ignored. In addition, for `simmode type=stress`, all analyses are considered as fresh analyses, and for `simmode type=aging`, all analyses are considered as aging analyses. This means that all analysis statements from the specified aging analysis to the end of the reliability block are considered as aging analysis with degradation.

**Note:** The aging transient conditions can be different from the stress transient conditions.

### Additional Notes

- The reliability feature only supports `bsim4`, `bsim3v3`, `psp103`, `bsimsoi`, `bsimcmg`, `bsimimg`, HiCUM (`bht`), `bsim6` (`bsimbulk`), BJT, and URI models.
- The reliability feature supports SpectreRF HB, PSS, P Noise, Pole Zero, DC Match, and HB Noise analyses.
- The two parameters `age` and `deltad` must be specified in the reliability block.

### Examples of Reliability Block Setup

#### Example 1

```
rel reliability {
 age time = [10y]
 deltax value = 0.1
 tran_stress tran start = 0.0n step = 1n stop = 10n
 change1 alter param = temp value = 25
 tran_aged tran start = 0.0n step = 1n stop = 10n
}
```

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The above example runs the stress simulation at the same fresh condition. Then, the aged simulation is run with temp=25C.

### Example 2

```
rel1 reliability {
 /* control statements */
 age time = [100h]
 deltad value=0.1
 /* stress testbench */
 Change0 alter param=temp value=125
 Change1 alter dev=VDD1 value=1.5 /* change VDD condition to 1.5V during stress */

 /* stress simulation */
 tran_stress tran start=0 stop=1us
 /* aging testbench */
 Change2 alter dev=VDD1 value=1.2 /* change VDD condition in EOL simulation */
 change3 alter param=temp value=25 /* change temp value in EOL simulation */
 /* aging simulation */
 tran_age tran start=0.5u stop=1us
}
```

In the above example, reliability simulation is carried with stressing devices for 100h with VDD at 1.5V and temp at 125C. After stress, end of life simulation (aging) is done with VDD at 1.2V and temperature at 25C.

### Example 3

```
rel reliability {
 age time=[8y]
 gradual_aging_agepoint points=[1y 5y 10y]
 tran_stress ...
 tran_aged ...
}
```

The above example:

- Runs the stress simulation for 1 year, calculates the device age, and updates the models.
- Continues to run the stress simulation using the updated models for 4 years, calculates the device age, and updates the model again.

- Continues to run the stress simulation using the updated models for 5 years (for total of 10 years), calculates the device age, and updates the model again. Next, runs `tran_aged` to generate the waveform.

**Note:** `age time=[8y]` is not used if `gradual_aging_agepoint` is used.

### Example 4

```
rel reliability {
age time=[8y]
gradual_aging_agemstep type=log start=1y stop=10y total_step=5
tran_stress ...
tran_aged ...
}
```

The above example:

- Calculates the time step using the formula  $(\log(\text{stop\_time}) - \log(\text{start\_time})) / (\text{total\_step} - 1)$ .
- Runs stress simulation for time step=2.25 years, calculates device age, and updates models.
- Checks if the `total_step` number is reached. If not, runs stress simulation again.
- If `total_step` number is reached, runs aging transient using the last updated model and generates the degraded waveform.

**Note:** `age time=[8y]` is not used if `gradual_aging_agemstep` is used.

### Example 5

```
param=VDD value=3.5
param=temp value=125
rel reliability
{
// reliability control statements
age time = [10y]
deltad value = 0.1
gradual_aging_agepoint points = [1y, 3y, 5y, 10y]
gradual_aging_alter time=3y param=VDD value=2.5
gradual_aging_alter time=3y param=TEMP value=100
// fresh/stress simulation.
tran_fresh tran start = 0 step = 1us stop = 10us
// aging testbench statements.
```

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```
//change1 alter param=rel_temp value=125
// aging simulation statements.
tran_aged tran start = 0 step = 1us stop = 10us }
```

The above example:

- Supports multiple transient statements. Whenever a gradual aging statement is reached, it sets the stress time for the following transient statement.
- Runs stress simulation for first 3 years at VDD=3.5V and temp=125, and updates the model.
- Runs stress simulation with updated model for next 7 years at VDD=2.5V and temp=100, and updates the model.
- Runs aging with updated model and generates degraded waveform.

### Example 6

```
rel reliability {
 age time = [10yr]
 uri_lib file="$OUTPATH/libURI.so"
 report_model_param value = yes
 aging_analysis_name value="hb_age"

 hb_fresh hb oversample=[1] funds=["FLO"] maxharms=[20]
 + errpreset=moderate annotate=status
 hbnoise_fresh (IFp IFn) hbnoise start=1K stop=10M maxsideband=20
 + annotate=status

 tran_stress tran step=1ns stop=100ns

 hb_age hb oversample=[1] funds=["FLO"] maxharms=[20]
 + errpreset=moderate annotate=status
 hbnoise_age (IFp IFn) hbnoise start=1K stop=10M maxsideband=20
 + annotate=status
 tran_aged tran start = 0 step = 1us stop = 10us }
```

The fresh RF analysis can be added inside the reliability block or before it.

For aged RF analysis, you must specify the aging analysis name using the `aging_analysis_name` control statement. This implies that from the specified aging analysis to the end of the reliability block, all included analyses are considered as aging

analysis with degradation. In the above example, the aging analysis name is `hb_age`. As a result, `hb_age` and `hbnoise_age` will be considered as aging analysis.

**Note:** In the reliability block, the last transient statement should always be `tran_aged`, which generates the aging waveform.

## Example 7

```
rel reliability {
 enable_ade_process value=yes
 age time=[10.0000y]
 accuracy level=2
 aging_analysis_name value="sp_age"
 uri_lib file="./relexpert/URILIB.so" debug=0 uri_mode=appendage

 tran_stress tran stop=1n errpreset=conservative write="spectre.ic" \
 writefinal="spectre.fc" annotate=status maxiters=5

 sp_age sp ports=[PORTIN PORTOUT] start=1G stop=1.2G step=0.1G annotate=status
 // export E_T=oceanEval("1")
 tran_aged tran start = 0 step = 1us stop = 10us
}
```

## Reliability Analysis with Spectre X Distributed Simulation

Use the `+xdp` option to run reliability analysis with Spectre X distributed simulation. This lets you use more computer cores across multiple computer hosts to further speed up run time of large to very large, mainly postlayout circuits. A circuit is considered as large when there are at least 500,000 nodes.

## Reliability Parameters Supported with Spectre X Distributed Simulation

Spectre X distributed simulation supports the following reliability parameters.

| Parameter                | Description                                                                                                                                                 |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| age time                 | The time in future when the transistor degradation and degraded SPICE model parameters are to be calculated.                                                |
| report_model_param value | Specifies whether to print the stress and aged parameters in the <code>.bm#</code> file.<br><br>Possible values are <code>no</code> and <code>yes</code> .  |
| accuracy level           | Specifies the methods used in the reliability simulation when performing integration and substrate current calculation.<br><br>Possible values are 1 and 2. |

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| Parameter                              | Description                                                                                                                                                                                                                                                                                                                               |
|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>minage value</code>              | Specifies the smallest age value for which degraded SPICE model parameters are calculated.                                                                                                                                                                                                                                                |
| <code>enable_negative_age value</code> | Enables negative age value.<br>Possible values are <code>no</code> and <code>yes</code> .                                                                                                                                                                                                                                                 |
| <code>enable_ade_process value</code>  | Enables reliability analysis in ADE Explorer or ADE Assembler.<br>Possible values are <code>no</code> and <code>yes</code> .                                                                                                                                                                                                              |
| <code>rel_mod type</code>              | Specifies the analysis type used for obtaining the device reliability values.<br>Possible values are <code>aging</code> , <code>she</code> , <code>all</code> , <code>aging_she</code> and <code>aging_thermal</code> .                                                                                                                   |
| <code>urilib file</code>               | Specifies URI library file name.                                                                                                                                                                                                                                                                                                          |
| <code>urilib uri_mode</code>           | Specifies the method to be used for performing aging simulation.<br>Possible values are <code>agemos</code> , <code>scaleparam</code> , <code>appendage</code> , <code>new_appendage</code> , <code>appendage2</code> and <code>appendage1</code> .                                                                                       |
| <code>urilib debug</code>              | Specifies the debug mode for URI library. The value can be either <code>0</code> or a positive value. When specified, a flag is added to the URI library indicating whether to print the debug information. If <code>debugMode</code> is not set to <code>0</code> , the debug messages are printed.<br>Default value is <code>0</code> . |
| <code>urilib scale_mode</code>         | Specifies parameter scale mode for URI library. The value can be <code>original</code> or <code>effective</code> . If value is <code>original</code> , send original parameter value to URI for param scale, else send effective value.<br>Possible values are <code>original</code> and <code>effective</code> .                         |
| <code>combine_deg</code>               | Determines whether to combine the external URI results with internal URI results in <code>bo0</code> file.<br>Possible values are <code>no</code> and <code>yes</code> .                                                                                                                                                                  |
| <code>output_she_power value</code>    | Set output device power in SHE flow.<br>Possible values are <code>no</code> and <code>yes</code> .                                                                                                                                                                                                                                        |

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| Parameter                        | Description                                                                                                                         |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| <code>desgort value</code>       | Specifies to enable to sort degradation data in decreasing order.<br><br>Possible values are <code>no</code> and <code>yes</code> . |
| <code>preset age</code>          | Specifies age value for preset.                                                                                                     |
| <code>agelevel_only value</code> | Sets the level for reliability analysis, which is essentially the age level number of the reliability analysis to be performed.     |
| <code>deltad value</code>        | The time in future when the transistor degradation and degraded SPICE model parameters are to be calculated.                        |

### Reliability Models Supported with Spectre X Distributed Simulation

Spectre X distributed simulation supports the following reliability models:

- Agebsim4
- Agebsim3v3
- Agebsimsoi
- Agepsp102
- Agehisim2
- Agehisim\_hv
- Agebsimcmg
- Ageumos3
- Ageumos4
- Ageumos5
- Ageumos6
- Agepsp103
- Agepsp1020
- Agepsp1021
- Agepsp102e
- Agebsimimg



- Ageutsoi
- Ageutsoi2
- Agelutsoi
- Agebsim6
- Agebsimbulk
- Agehisimhv\_va
- Agemos195
- Agesisim2\_va

## **Reliability Control Statements Reference**

- accuracy ( \*relxpert: .accuracy ) on page 480
- age ( \*relxpert: .age ) on page 481
- agelevel only ( \*relxpert: .agelevel only ) on page 482
- check\_neg\_aging ( \*relxpert: .check\_neg\_aging ) on page 484
- degradation\_check ( \*relxpert: .degradation\_check ) on page 485
- degradation\_check\_exception ( \*relxpert: .degradation\_check\_exception ) on page 487
- degradation\_check\_output ( \*relxpert: .degradation\_check\_output ) on page 488
- degsort ( \*relxpert: .degsort ) on page 489
- deg\_ratio ( \*relxpert: .deg\_ratio ) on page 491
- deltad ( \*relxpert: .deltad ) on page 493
- dumpagemodel ( \*relxpert: .dumpagemodel ) on page 495
- enable\_negative\_age ( \*relxpert .enable\_negative\_age ) on page 497
- enable\_tmi\_uri on page 498
- gradual\_aging\_agepoint ( \*relxpert: .agepoint ) on page 499
- gradual\_aging\_agestep ( \*relxpert: .agestep ) on page 500
- idmethod ( \*relxpert: .idmethod ) on page 501
- igatemethod ( \*relxpert: .igatemethod ) on page 502
- isubmethod ( \*relxpert: .isubmethod ) on page 503
- macrodevice ( \*relxpert: .macrodevice ) on page 504
- maskdev ( \*relxpert: .maskdev ) on page 505
- minage ( \*relxpert: .minage ) on page 506
- opmethod ( \*relxpert: .opmethod ) on page 507
- output\_device\_degrad ( \*relxpert: .output\_device\_degrad ) on page 511
- output\_subckt\_degrad on page 514
- relx\_tran ( \*relxpert: .relx\_tran ) on page 519

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- report\_model\_param (\*relxpert: .report\_model\_param ) on page 520
- simmode on page 521
- tmi\_aging\_mode (\*relxpert: .tmi\_aging\_mode) on page 522
- uri\_lib ( \*relxpert: .uri\_lib ) on page 524
- vdsmethod on page 526
- User-Defined Reliability Models on page 530

## **accuracy ( \*relxpert: .accuracy )**

`accuracy level={1 | 2}`

### **Description**

Specifies methods used in the reliability simulation when performing integration and substrate current calculation.

### **Arguments**

`level={1 | 2}`

Specifies trapezoidal integration when performing integrations and calculates  $I_{sub}$  for  $V_{gs} < V_{th}$ . When `level` is set to 1, the software uses backward Euler integration and sets  $I_{sub}=0$  when  $V_{gs} < V_{th}$ . When `level` is set to 2, the software uses trapezoidal integration and calculates  $I_{sub}$  when  $V_{gs} < V_{th}$ . Setting `accuracy` to 2 is more accurate, but increases simulation time when compared to when `accuracy` is set to 1.

Default: 1

### **Example**

```
accuracy level = 2
*relxpert: accuracy 2
```

Specifies that trapezoidal integration will be used and  $I_{sub}$  will be calculated when  $V_{gs} < V_{th}$ .

## **age ( \*relxpert: .age )**

```
age time = { value [value1 value2...]}
```

### **Description**

Specifies the time at which the transistor degradation and degraded SPICE model parameters are calculated.

### **Arguments**

*value*

The duration in the future at which the transistor degradation and degraded SPICE model parameters are to be calculated. Attach the suffix y (year), h (hour) or m (minute).

There should be no space between the number and suffix. For example, 10m, 1e-5sec.

### **Example**

```
age time = [10y]
*relxpert: age 10y
```

Specifies the age time as 10 years.

## agelevel\_only ( \*relxpert: .agelevel\_only )

```
agelevel_only value=[(level_value model_name) (level_value model_name) ...]
 type=include|exclude
```

### Description

Specifies the age level for performing reliability analysis on the specified model(s). You can specify different age levels for different set of models.

**Note:** This option also supports the URI defined `agelevel` statement.

If *model\_name* is not specified, the simulation is performed on all of the devices at the specified age level.

### Arguments

|                    |                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>level_value</i> | <p>Sets the level for reliability analysis, which is essentially the age level number of the reliability analysis is to be performed.</p> <p>The following levels can be used to specify Cadence internal ageMOS models:</p> <ul style="list-style-type: none"><li>■ 0: Specifies HCI reliability analysis.</li><li>■ 1: Specifies NBTI reliability analysis.</li><li>■ 2: Specifies PBTI reliability analysis.</li></ul> |
| <i>model_name</i>  | <p>Lists the models at one age level to perform reliability analysis.</p>                                                                                                                                                                                                                                                                                                                                                 |
| <i>type</i>        | <p>Includes or excludes the specified aging levels. The default value is <code>include</code>.</p>                                                                                                                                                                                                                                                                                                                        |

### Example

```
agelevel_only value=[(101 pmos1 pmos2) (112 pmos1 pmos2)]
```

Runs reliability analysis on `pmos1` and `pmos2` models with age levels 101 and 112.

## **aging\_analysis\_name**

`aging_analysis_name value=analysis_name`

### **Description**

Specifies the name of the analysis that needs to be used as aging analysis instead of transient analysis. You cannot specify a stress transient analysis as aging analysis in the reliability block.

**Note:** Currently, `aging_analysis_name` supports only ac and dc analyses.

### **Arguments**

|              |                                                                                                                |
|--------------|----------------------------------------------------------------------------------------------------------------|
| <i>value</i> | Name of the analysis to be used in aging simulation. Possible values are <code>ac</code> and <code>dc</code> . |
|--------------|----------------------------------------------------------------------------------------------------------------|

### **Example**

`aging_analysis_name value=ac`

## **check\_neg\_aging (\*relxpert: .check\_neg\_aging)**

`check_neg_aging type={warn|error|ignore} clamp={yes|no}`

### **Description**

Reports the negative degradation values for a model.

### **Arguments**

|              |                                                                                                                                                                                                                                                                 |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>type</i>  | Specifies the type of message to be generated when negative aging occurs. Possible values are <code>error</code> and <code>warn</code> . The default value is <code>error</code> .                                                                              |
| <i>clamp</i> | Specifies whether or not to clamp the degradation values for negative aging. Default is <code>no</code> . If set to <code>yes</code> , Spectre clamps the degradation values to be the same as fresh values and generates a warning message for negative aging. |

### **Example**

```
check_neg_aging type=warn clamp=yes
```



## degradation\_check (\*relxpert: .degradation\_check)

```
degradation_check type=[warn | error] parameter=[deltad | dvth | didlin | didsat |
 did | dgm | dgds] value=<degradation_value> {agelevel=agelevel_number}
 {sub=[sub1 sub2 sub3 ...] | mod=[mod1 mod2 mod3...] | dev=[inst1 inst2
 inst3...]} [error=filename]
```

### Description

Checks for device degradation and issues a warning or error if the device's degradation value (in `bo0` output) or `vth`, `idlin`, `idsat`, `gm`, and/or `gds` degradation (in `bt0` output) is greater than the value specified by the `value` argument.

You can also use reliability warning/error model parameters, such as `warn_dvth`, `error_dvth` and so on, to check for device degradation. However, if warning/error model parameters are also specified along with the `degradation_check` control statement, the `degradation_check` control statement takes precedence over the model parameters.

You can output the degradation check results to a file using the `degradation_check_output filename` reliability control statement. You can use the `degradation_check_exception filename` control statement to specify the devices for which degradation check needs to be skipped.

### Arguments

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>type</i>      | Specifies the message type. Possible values are <code>error</code> or <code>warning</code> . For <code>type=warning</code> , only the first five warning messages are reported. For <code>type=error</code> , Spectre terminates with the error message.                                                                                                                                                                                                                                                                                                                                                                                    |
| <i>parameter</i> | Specifies the model parameters for the device. Possible values are <code>deltad</code> , <code>dvth</code> , <code>didlin</code> , <code>didsat</code> , <code>did</code> , <code>dgm</code> , or <code>dgds</code> . <code>deltad</code> refers to the degradation value in the <code>bo0</code> output. <code>dvth</code> , <code>didlin</code> , <code>didsat</code> , <code>did</code> , <code>dgm</code> , <code>dgds</code> refer to <code>Vth</code> , <code>Idlin</code> , <code>Idsat</code> , either <code>Idlin</code> or <code>Idsat</code> , <code>Gm</code> , or <code>Gds</code> degradation in the <code>bt0</code> output. |
| <i>value</i>     | Specifies the degradation value for the model. An error or warning is issued if the degradation for the specified parameter is greater than the degradation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <i>agelevel</i>  | Specifies the age level for the model.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <i>sub</i>       | Specifies the name of the subcircuit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

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|                 |                                                      |
|-----------------|------------------------------------------------------|
| <i>mod</i>      | Specifies the list of models.                        |
| <i>dev</i>      | Specifies the name of the instances.                 |
| <i>filename</i> | Name of the file to which the error will be written. |

- You can specify only one of the `sub`, `mod`, or `dev` arguments in the control statement. A combination is not allowed. If none of these arguments is specified, then all devices are checked for degradation.
- The `agelevel` argument can be specified only for the `deltad` parameter. In addition, if `agelevel` is specified for the `deltad` parameter, then degradation check is performed only at that `agelevel`.
- Only one `degradation_check` control statement is allowed. If multiple statements are specified, only the last statement is considered by the simulator.

### Example

```
degradation_check type=warn parameter=deltad value=0.25
```

The above statement issues a warning if any device's total `deltad` in `bo0` is greater than 0.25.

```
degradation_check type=error parameter=dvth value=0.7 mod=[nmos]
```

Issues an error if any device with model `nmos` has `d_Vth` value greater than 0.7 in `bt0`.

## **degradation\_check\_exception (\*relxpert: .degradation\_check\_exception)**

`degradation_check_exception file=filename`

### **Description**

Excludes the devices specified in the file from degradation check.

### **Arguments**

|                 |                                                                                      |
|-----------------|--------------------------------------------------------------------------------------|
| <i>filename</i> | Name of the file containing devices that need to be excluded from degradation check. |
|-----------------|--------------------------------------------------------------------------------------|

## **degradation\_check\_output (\*relxpert: .degradation\_check\_output)**

`degradation_check_output file = filename`

### **Description**

Outputs the device degradation errors and warnings generated by the `degradation_check` control statement or the reliability model parameters for degradation check to a specified file. The file contains the degradation information in the following format:

| <b>Device</b> | <b>Type</b> | <b>Degradation_Value</b> | <b>Limit_Value</b> | <b>AgeLevel</b> |
|---------------|-------------|--------------------------|--------------------|-----------------|
| X1.m1         | warning     | d_vth=0.3                | warn_dvth=0.2      | agelevel=0      |
| X1.m2         | error       | d_idsat=0.004            | error_didsat=0.003 | agelevel=2      |

### **Arguments**

|                 |                                                        |
|-----------------|--------------------------------------------------------|
| <i>filename</i> | Name of the file where the output needs to be written. |
|-----------------|--------------------------------------------------------|

## degsort (\*relxpert: .degsort)

```
degsort {threshold = value | number = value } [phys = value] [item = value]
 [value=yes|no]
```

### Description

Prints MOS transistors based on the threshold and number settings. The results are sorted in the descending order of degradation.

**Note:** The `threshold` and `number` arguments are mutually exclusive. Therefore, only one of them can be specified with `degsort` to print the sorted device degradation results.

### Arguments

|                                     |                                                                                                                                                                                                                                                                                      |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>threshold=<i>value</i></code> | Prints the transistors having degradation values greater than <code>threshold</code> value. <i>value</i> can be in decimal notation (xx.xx) or in engineering notation (x.xxe+xx).                                                                                                   |
| <code>number=<i>value</i></code>    | Prints only the first <i>value</i> transistors having the highest degradations. For example, if <code>number=100</code> , the software will print the first 100 transistors with highest degradations.                                                                               |
| <code>phys</code>                   | Reliability effect to be used for sorting. This parameter is available only for TMI aging flow.<br>Possible values are <code>hci_bti</code> , <code>hci</code> , and <code>bti</code> .                                                                                              |
| <code>item</code>                   | Reliability item is used for sorting. It is only available for TMI aging flow. This parameter is available only for TMI aging flow.<br>Possible values are 0 (or <code>didsat</code> ), 1 (or <code>didlin</code> ), 2 (or <code>dvtlin</code> ), and 3 (or <code>lifetime</code> ). |
| <code>value</code>                  | Prints the transistors having degradation values sorted in decreasing order. It cannot be used for TMI aging model. The default value is <code>yes</code> .                                                                                                                          |

**Note:** If the parameters `threshold` | `number`, or `item` are specified, the value is set to `yes` by default.

### Example

```
degsort threshold = 0.1
*relxpert: degsort -threshold 0.1
```

Prints all MOS transistors that have degradation value greater than 0.1.

## **deg\_ratio (\*relxpert: .deg\_ratio)**

```
deg_ratio type = { [include | exclude] [hci = hci_ratio_value nbti =
 nbti_ratio_value pbti = pbti_ratio_value bti = bti_ratio_value hcin =
 nmos_hci_ratio_value hcip = pmos_hci_ratio_value btin = nmos_bti_ratio_value
 btip = pmos_bti_ratio_value]
dev = [inst1 inst2 inst3...] }
```

### **Description**

Specifies the HCI, NBTI, and PBTI degradation weighting ratio for devices in a Spectre simulation. The HCI, NBTI, and PBTI ratio values are specified by using the *hci\_ratio\_value*, *nbti\_ratio\_value*, *pbti\_ratio\_value*, respectively. The HCI ratio values for nmos and pmos are specified using *nmos\_hci\_ratio\_value* and *pmos\_hci\_ratio\_value*, respectively. The BTI ratio values for nmos and pmos are specified using *nmos\_bti\_ratio\_value* and *pmos\_bti\_ratio\_value*, respectively. The new degradation values for the specified devices is obtained by multiplying the original degradation value.

**Note:** Specifying *nbti=nbti\_ratio\_value* is the same as specifying *btip=pmos\_bti\_ratio\_value* and specifying *pbti=pbti\_ratio\_value* is the same as specifying *btin=nmos\_bti\_ratio\_value*. If *hci* and *hcip/hcin* are specified, *hcip/hcin* will take precedence over *hci*.

### **Arguments**

|                           |                                                                                                                                                     |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>type=include</code> | Include the specified devices during TMI aging simulation flow.                                                                                     |
| <code>type=exclude</code> | Exclude the specified devices during TMI aging simulation flow.                                                                                     |
| <code>hci</code>          | Specifies the HCI degradation weighting ratio in total degradation. The specified value should be greater than 0.0. The default value is 1.0.       |
| <code>nbti</code>         | Specifies the NBTI degradation weighting ratio in total degradation. The specified value should be greater than 0.0. The default value is 1.0.      |
| <code>pbti</code>         | Specifies the PBTI degradation weighting ratio in total degradation. The specified value should be greater than 0.0. The default value is 1.0.      |
| <code>bti</code>          | Specifies the NBTI/PBTI degradation weighting ratio in total degradation. The specified value should be greater than 0.0. The default value is 1.0. |

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|      |                                                                                                                                                         |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| hcin | Specifies the HCI degradation weighting ratio for nmos in total degradation. The specified value should be greater than 0.0. The default value is 1.0.  |
| hcip | Specifies the HCI degradation weighting ratio for pmos in total degradation. The specified value should be greater than 0.0. The default value is 1.0.  |
| btin | Specifies the PBTI degradation weighting ratio for nmos in total degradation. The specified value should be greater than 0.0. The default value is 1.0. |
| btip | Specifies the NBTI degradation weighting ratio for pmos in total degradation. The specified value should be greater than 0.0. The default value is 0.   |
| dev  | Specify the instances that need to be included or excluded for degradation ratio during TMI aging simulation flow                                       |

### Example

```
deg_ratio type=include [hci = 0.5 nbti = 0.3 pbti = 0.2] dev = [I1]
```



## deltad ( \*relxpert: .deltad )

```
deltad value = deltad_value [model_name1|agelevel<val1> agelevel<val2>
[model_name2|agelevel<val3>]...] [item = value]
```

### Description

Requests the calculation of lifetime for each transistor under the circuit operating conditions. You can use multiple `deltad` statements for different types of transistors.

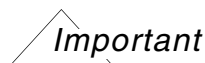
### Arguments

*value=deltad\_value*

The degradation value can be transconductance ( $\Delta g_m / g_m$ ), linear or saturation drain current degradation ( $\Delta I_d / I_d$ ), threshold voltage shift ( $\Delta V_t$ ), or any other degradation monitor, depending on the definitions of the lifetime parameters  $H$  and  $m$ . *deltad\_value* can be in decimal notation (xx.xx) or in engineering notation (x.xxe+xx).

*model\_name*

Name of a specific model whose lifetime is calculated. The model name must be the same as specified in the `.model` card.



Currently, specifying the model name is not supported.

*agelevel*

Specifies the agelevel values for HCI, PBTI, and NBTI modeling. You must specify the agelevel values using the keyword `agelevel`, for example, `agelevel103`, `agelevel103` and so on. In addition, you cannot combine the agelevel value with the model name in one `deltad` statement.

*item*

Name of electrical parameter for lifetime estimation. This parameter is available only for TMI aging flow. Possible values are 0 (or `didsat`), 1 (or `didlin`), 2 (or `dvtlin`), and 3 (or `lifetime`).

### Example

```
deltad value=["0.1 pmos"]
```

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Specifies that the lifetime calculation will be done under the circuit operating conditions for pmos transistors.

```
deltad value=["0.1 agelevel101 agelevel102" "50 agelevel103"]
```

## **dumpagemodel (\*relxpert: .dumpagemodel)**

```
dumpagemodel file = filename dev = [devicelist]
```

### **Description**

Outputs the model card information for aged devices into the specified file.

### **Arguments**

|                   |                                                                                                                                                                                                                 |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>file</code> | Specifies the file name to which the model card information for the aged devices will be written.                                                                                                               |
| <code>dev</code>  | Specifies the devices whose model card information will be output to the file. If <code>dev</code> is not specified, then the model card information for all the devices will be written to the specified file. |

### **Example**

```
dumpagemodel file = "agedModelFile"
```

Specifies that the model card information for all the devices be written to the `agedModelFile` file.

## **enable\_bias\_runaway (\*relxpert .enable\_bias\_runaway)**

```
enable_bias_runaway = { yes | no }
```

### **Description**

Enables the bias runaway detecting flow. This flow checks for positive feedback between the device degradation and stress over the device which might result in an exponential increase in device degradation and failure.

### **Arguments**

|                    |                                                                     |
|--------------------|---------------------------------------------------------------------|
| <code>value</code> | Specifies whether or not to enable the bias runaway detecting flow. |
|                    | The default value is <code>no</code> .                              |

### **Example**

```
enable_bias_runaway value = yes
```

## **enable\_negative\_age (\*relxpert .enable\_negative\_age)**

```
enable_negative_age value = { yes | no }
```

### **Description**

Enables the negative age value for customer URI output. For internal agelevel, the negative age values cannot be negative. If this option is not specified, all negative age values are set to 0.0.

### **Arguments**

|       |                                                                                                                               |
|-------|-------------------------------------------------------------------------------------------------------------------------------|
| value | Specifies whether or not to enable the negative age value for the customer URI output. The default value is <code>no</code> . |
|-------|-------------------------------------------------------------------------------------------------------------------------------|

### **Example**

```
enable_negative_age value = yes
```

## enable\_tmi\_uri

`enable_tmi_uri value={yes|no} [tmishe=yes|no]`

### Description

Enables the TMI and URI flow. By default (`value=no` and `tmishe=no`), Spectre only supports the TMI flow if the TMI library is present, otherwise, it supports the URI flow.

If both TMI or URI libraries are present and you want to enable both TMI and URI flow models (for example, TMI for normal SPICE and URI for aging calculation), you can set the value to `yes` to enable both calculations. If you want to also enable the TMI self-heating flow, set the value of the `tmishe` parameter to `yes`. Then, Spectre passes the TMI `dtemp` value to URI for reliability calculation.

### Arguments

|                         |                                                                                                                                                                                                                  |
|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>yes</code>        | Enable the TMI and URI flow.                                                                                                                                                                                     |
| <code>no</code>         | Support the TMI flow if TMI library is present.                                                                                                                                                                  |
| <code>tmishe=yes</code> | Enable the self-heating flow and pass the <code>dtemp</code> value to URI for reliability calculation. This option sets the values of the TMI aging parameters <code>tmiage</code> and <code>tmishe</code> to 1. |
| <code>tmishe=no</code>  | Do not perform TMI self heating.                                                                                                                                                                                 |

### Example

```
enable_tmi_uri value=yes tmishe=yes
```

## **gradual\_aging\_agepoint (\*relxpert: .agepoint)**

`gradual_aging_agepoint points=[age_point_list] profile=[yes|no]`

### **Description**

Specifies the agepoint method for the gradual aging flow. Use this option to define the selected age points to perform reliability simulation or run the simulation independent of the aging points. The results files for each step are suffixed with age point values.

### **Arguments**

|                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>age_point_list</i> | Specifies the age point list. Note that the point's value should be more than 0. The value in the list should be arranged in ascending order and no negative value should be specified.                                                                                                                                                                                                                                                                                                                                                                                  |
| <i>profile</i>        | Specifies that the simulation be run independent of the aging point list. When <code>profile=yes</code> , the age calculation for the age point during gradual aging steps is independent of the previous age point. The aging calculation for all the aging steps is based on the fresh condition and the final aging value is the sum of the age value for every aging step. As a result, the immediate gradual aging points or the gradual aging steps do not affect the final aging value. Only the final age time in the gradual aging affects the final age value. |

### **Example**

`gradual_aging_agepoint points=[1y 3y 5y 8y]`

Specifies that the simulation be run for age points 1y, 3y, 5y, and 8y.

## **gradual\_aging\_agestep (\*relxpert: .agestep)**

```
gradual_aging_agestep type=[log|lin] start=start_time stop=stop_time
total_step=total_step_num
```

### **Description**

Specifies the agestep method for gradual aging flow. Use this option to define the reliability simulation from the start time to the stop time. The total steps of reliability simulation are specified by *total\_step\_num*. Two age step types, linear and logarithm, can be specified.

### **Arguments**

|                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>type</code>       | <p>Specifies the type of agestep, linear (<code>lin</code>) or logarithm (<code>log</code>). The default type is <code>lin</code>. When you specify <code>lin</code>, the time step is calculated using the following formula:</p> $(\text{stop\_time} - \text{start\_time}) / \text{total\_step}$ <p>When you specify <code>log</code>, the time step is calculated using the following formula:</p> $[\log(\text{stop\_time}) - \log(\text{start\_time})] / \text{total\_step}$ |
| <code>start</code>      | <p>The start time of reliability simulation. Default is 0.0 for linear type and 1.0 for logarithm.</p> <p><b>Note:</b> The time unit can be set as y(year), d(day), h(hour), m(minute) and s(second).</p>                                                                                                                                                                                                                                                                         |
| <code>stop</code>       | <p>The stop time for reliability simulation.</p> <p><b>Note:</b> The time unit can be set as y(year), d(day), h(hour), m(minute) and s(second).</p>                                                                                                                                                                                                                                                                                                                               |
| <code>total_step</code> | <p>The total number of steps for reliability simulation. The value should be more than 1.</p>                                                                                                                                                                                                                                                                                                                                                                                     |

### **Example**

```
gradual_aging_agestep type=log start=1y stop=10y total_step=6
```

Specifies that the agestep method will be used for the gradual aging flow where the type of agestep is logarithm, the start and stop time for simulation is 1 year and 10 years, respectively, and the total steps for reliability simulation is 6.



## idmethod ( \*relxpert: .idmethod )

```
idmethod type = { ids | idrain | idstatic }
```

### Description

Specifies how the simulator obtains the drain current ( $I_d$ ) to perform reliability calculations. The following types of drain currents, which are available from SPICE, are supported by reliability analysis:

- Dynamic drain current (also called AC drain current) - this is the current that flows in to the drain node.
- Static drain current (also called channel drain current, DC drain current, or  $I_{ds}$ ).

**Note:** The value for this control statement must be as specified by the foundry.

### Arguments

|                            |                                                                               |
|----------------------------|-------------------------------------------------------------------------------|
| <code>type=ids</code>      | Instructs the reliability simulator to use $I_{ds}$ static current (Default). |
| <code>type=idrain</code>   | Instructs the reliability simulator to use dynamic drain current.             |
| <code>type=idstatic</code> | Instructs the reliability simulator to use the terminal static current.       |

### Example

```
idmethod type=idrain (new format)
*relxpert: idmethod idrain
```

Specifies the reliability simulator to print dynamic drain current.

## **igatemethod (\*relxpert: .igatemethod)**

```
igatemethod type={calc | spice}
```

### **Description**

Specifies the method used for obtaining the gate terminal current of a MOSFET.

During MOSFET HCI simulation, the gate terminal current is required for calculating the degradation value. The simulator can either calculate this value using internal Igate model, or obtain it from the built-in SPICE model such as BSIM4 or PSP Igate model.

If this command is not used, the simulator calculates the gate terminal current using internal Igate model.

**Note:** The value for this control statement must be as specified by the foundry.

### **Arguments**

|                    |                                                                                |
|--------------------|--------------------------------------------------------------------------------|
| <code>calc</code>  | Calculates the gate terminal current using the internal Igate model (Default). |
| <code>spice</code> | Obtains the gate terminal current value using built-in SPICE model.            |

### **Example**

```
igatemethod type=spice
*relxpert: igatemethod spice
```

Specifies that the gate terminal current value should be from built-in SPICE model.

## **isubmethod (\*relxpert: .isubmethod)**

```
isubmethod type={ calc | spice }
```

### **Description**

Specifies the method used for obtaining substrate terminal current of a MOSFET.

During MOSFET HCI simulation, the substrate terminal current is required for calculating the degradation value. The simulator can either calculate this value using internal Isub model, or obtain it from the built-in SPICE model such as BSIM4 or PSP Isub model.

If this command is not used, the simulator calculates the substrate terminal current using internal Isub model.

**Note:** The value for this control statement must be as specified by the foundry.

### **Arguments**

|                    |                                                                                    |
|--------------------|------------------------------------------------------------------------------------|
| <code>calc</code>  | Calculates the substrate terminal current using the internal Isub model (Default). |
| <code>spice</code> | Obtains the substrate terminal current value using built-in SPICE model            |

### **Example**

```
isubmethod type=spice
*relxpert: isubmethod spice
```

Specifies that the substrate terminal current value should be obtained from the built-in SPICE model.

## **macrodevice (\*relxpert: .macrodevice)**

```
macrodevice type=[appendparams|agemos] sub = [sub1 sub2 sub3 ...]
```

### **Description**

Identifies the subcircuits in the netlist that are actually macro devices and therefore require special handling. You must specify at least one subcircuit.

### **Arguments**

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| type | <p>Specifies the method to handle macro devices. Possible values are <code>appendparams</code> (default) and <code>agemos</code>. For <code>type=appendparams</code>, there is no change in SPICE model parameters and the degradation value is appended to the related macro device. You can specify the subcircuit instance parameters to be scaled using <code>scaled_params []</code> in the aging model card.</p> <p>For <code>type=agemos</code>, Spectre performs degradation of SPICE model parameters for the related macro device.</p> |
| sub  | <p>Specifies the subcircuit name.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### **Example**

```
macrodevice type=appendparams sub=[inv]
```

## maskdev ( \*relxpert: .maskdev )

```
maskdev type={include | exclude} { sub = [sub1 sub2 sub3 ...] mod = [mod1 mod2 mod3 ...] dev = [inst1 inst2 inst3 ...] }
```

### Description

Includes or excludes:

- instances which belong to the subcircuit listed in the subckt list
- devices which belong to the model listed in the model list
- devices which are listed in the instance list

### Arguments

|              |                                                                                                                                                                   |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| type=include | Performs reliability simulation on the specified devices, or the models that belong to the listed subcircuit, or devices that belong to the listed model only.    |
| type=exclude | Excludes the listed devices, or the models that belong to the listed subcircuit, or the devices that belong to the specified model during reliability simulation. |
| sub          | Specifies the subcircuit(s) for which the related instances should be included or excluded while performing reliability analysis.                                 |
| mod          | Specifies the models for which the related devices should be included or excluded while performing reliability analysis.                                          |
| dev          | Specifies the instances to be included or excluded during reliability analysis.                                                                                   |

### Example

```
maskdev type=include sub=[inv] mod=[nmos pmos] dev=[I1 I2 I3 I4]
*relxpert: maskdev include subckt = [inv] model=[nmos pmos] instance=[I1 I2 I3 I4]
```

Includes the models that belong to the `inv` subcircuit and the `pmos` and `nmos` models. In addition, it includes the `I1`, `I2`, `I3`, and `I4` devices.

## **minage ( \*relxpert: .minage )**

`minage value = minage_value`

### **Description**

Sets the smallest Age value for which degraded SPICE model parameters are calculated. This statement speeds up aging calculation by using fresh SPICE model parameters if the transistor Age value is smaller than the specified *minage\_value*.

### **Arguments**

`value=minage_value` Specifies the smallest Age value for which degraded SPICE model parameters are calculated. *minage\_value* can be in decimal notation (xx.xx) or in engineering notation (x.xxe+xx).

### **Example**

```
minage value = 0.001
*relxpert: minage 0.001
```

Specifies that the smallest Age value, 0.001, for which degraded SPICE model parameters are calculated.

## **opmethod (\*relxpert: .opmethod )**

```
opmethod type = { calc | spice }
```

### **Description**

Specifies whether the *Igate* or *Isub* value should be obtained from the SPICE models (for example, BSIM3 or BSIM4) or the internal *Igate* or *Isub* equation should be used.

**Note:** The value for this control statement must be as specified by the foundry.

### **Arguments**

|                    |                                                                                                                              |
|--------------------|------------------------------------------------------------------------------------------------------------------------------|
| <code>calc</code>  | Calculates the gate and substrate terminal current using the Cadence <i>Igate</i> and <i>Isub</i> model equations (Default). |
| <code>spice</code> | Obtains the gate and substrate terminal current value from the SPICE model.                                                  |

### **Example**

```
opmethod type=spice
*relxpert: opmethod spice
```

Specifies that the gate and substrate terminal current value should be obtained from the SPICE model.

## **output\_inst\_param (\*relxpert: .output\_inst\_param)**

```
output_inst_param list=[param1 param2...]
```

### **Description**

Specify the names of the instance parameters, defined in URI shared library, to be output into bo0 or psf file.

### **Arguments**

|                   |                                                                              |
|-------------------|------------------------------------------------------------------------------|
| <code>list</code> | Names of the URI instance parameters that need to be added to the bo0 table. |
|-------------------|------------------------------------------------------------------------------|

**Note:** URI instance parameters must be specified, otherwise, Spectre generates a warning.

### **Example**

```
output_inst_param list=[dtemp leff]
```

The above statement adds the URI instance parameters `dtemp` and `leff` to the bo0 file.



## **output\_she\_power (\*relxpert: .output\_she\_power)**

`output_she_power value=yes|no`

### **Description**

Output the device power in the self-heating (SHE) flow. You must set the `rel_mode` reliability control statement to `she` or `all` for this control statement to work.

The device power is calculated using the `calcPower()` URI function and stored in the `.bw0` file.

### **Argument**

|                    |                                                                                                                           |
|--------------------|---------------------------------------------------------------------------------------------------------------------------|
| <code>value</code> | If set to <code>yes</code> , outputs the device power in the self-heating flow.<br>The default value is <code>no</code> . |
|--------------------|---------------------------------------------------------------------------------------------------------------------------|

### **Example**

```
output_she_power value=yes
```

## reset\_analysis\_param

```
reset_analysis_param type = { tran | dc | ac }
```

### Description

Replaces the stress and aging analysis parameters defined in the reliability analysis block with the specified analysis.

### Arguments

|                   |                                                                                                                     |
|-------------------|---------------------------------------------------------------------------------------------------------------------|
| <code>type</code> | Specifies the type of analysis that will replace the stress and aging parameters in the reliability analysis block. |
|-------------------|---------------------------------------------------------------------------------------------------------------------|

**Note:** Currently, only the `tran` option is supported.

### Example

```
reset_analysis_param type=tran
```

## **output\_device\_degrad ( \*relxpert: .output\_device\_degrad )**

```
output_device_degrad { vdd = "vdd_value1 [model_list...] ["vdd_value2
 [model_list...]"]... } [vdlin = vdlin_value1 [model_list...] [vdlin_value2
 [model_list...]...] [vgsat = vgsat_value1 [model_list...] [vgsat_value2
 [model_list...]...] [vglin = vglin_value1 [model_list...] [vglin_value2
 [model_list...]...] [output_bias_voltage=yes|no] [correct_bias_voltage =
 no|yes] [keep_zero_result =no|yes] tmi_lib_inc = file_path file = file_path
```

### **Description**

Outputs the device degradation (gm, gds, Idlin, Idsat, Vth degradation) information to a .bt0 file.

The device degradation calculation is based on following fixed bias conditions:

#### **NMOSFET**

- Idsat:  $V_{ds}=V_{dd}$ ,  $V_{gs}=V_{gsat}$  if  $V_{gsat}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .
- Idlin:  $V_{ds}=V_{dlin}$  if  $V_{dlin}$  is specified for the target model, otherwise  $V_{ds}=0.05V$ ;  $V_{gs}=V_{glin}$  if  $V_{glin}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .
- gm:  $V_{ds}=V_{dlin}$  if  $V_{dlin}$  is specified for the target model, otherwise  $V_{ds}=0.05V$ ;  $V_{gs}=V_{glin}$  if  $V_{glin}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .
- Vth:  $V_{ds}=V_{dlin}$  if  $V_{dlin}$  is specified for the target model, otherwise  $V_{ds}=0.05V$ ;  $V_{gs}=V_{glin}$  if  $V_{glin}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .
- Gds:  $V_{ds}=V_{dlin}$  if  $V_{dlin}$  is specified for the target model, otherwise  $V_{ds}=0.05V$ ;  $V_{gs}=V_{glin}$  if  $V_{glin}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .

#### **PMOSFET**

- Idsat:  $V_{ds}=V_{dd}$ ,  $V_{gs}=V_{gsat}$  if  $V_{gsat}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .
- Idlin:  $V_{ds}=V_{dlin}$  if  $V_{dlin}$  is specified for the target model, otherwise  $V_{ds}=-0.05V$ ;  $V_{gs}=V_{glin}$  if  $V_{glin}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .
- gm:  $V_{ds}=V_{dlin}$  if  $V_{dlin}$  is specified for the target model, otherwise  $V_{ds}=-0.05V$ ;  $V_{gs}=V_{glin}$  if  $V_{glin}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .
- Vth:  $V_{ds}=V_{dlin}$  if  $V_{dlin}$  is specified for the target model, otherwise  $V_{ds}=-0.05V$ ;  $V_{gs}=V_{glin}$  if  $V_{glin}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .

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- **Gds:**  $V_{ds}=V_{dlin}$  if  $V_{dlin}$  is specified for the target model, otherwise  $V_{ds}=-0.05V$ ;  $V_{gs}=V_{glin}$  if  $V_{glin}$  is specified for the target model, otherwise  $V_{gs}=V_{dd}$ .

### Arguments

|                                   |                                                                                                                                                                                                                                                                              |
|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>vdd</code>                  | Sets the bias voltage for the device to obtain <code>gm</code> , <code>gds</code> , <code>Idlin</code> , <code>Idsat</code> , and <code>Vth</code> degradation for the TMI aging flow. This argument is mandatory.                                                           |
| <code>vdlin</code>                | $V_{ds}$ value for <code>Idlin</code> / <code>Vt</code> / <code>Gm</code> measurement.                                                                                                                                                                                       |
| <code>vgsat</code>                | $V_{gs}$ value for <code>Idsat</code> measurement                                                                                                                                                                                                                            |
| <code>vglin</code>                | $V_{gs}$ value for <code>Idlin</code> / <code>Vt</code> / <code>Gm</code> measurement.                                                                                                                                                                                       |
| <code>tmi_lib_inc</code>          | <p>Specifies the path to the file containing TMI library path and include section. The following is the syntax of the file:</p> <p>TMI include path [include section]</p> <p>It is mandatory to specify the TMI include path. The include section is optional.</p>           |
| <code>file</code>                 | <p>Specifies the path of the include file.</p> <p>The <code>output_device_degrad</code> options can be specified in the included file.</p>                                                                                                                                   |
| <code>output_bias_voltage</code>  | Specifies whether to print the model names and bias conditions for the specified devices in the <code>.bt0</code> and <code>,dpl</code> files. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>no</code> .                             |
| <code>correct_bias_voltage</code> | Specifies whether to correct the bias voltage of the specified devices. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>yes</code> .                                                                                                   |
| <code>keep_zero_result</code>     | Specifies whether to print the zero degradation results in the <code>.bt0</code> file. By default, zero degradation results are not printed in the <code>.bt0</code> file. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>no</code> . |

### Example

```
output_device_degrad vdd=["1.2 nch1 nch2" "1.1 pch1 pch2"] tmi_lib_inc="./
model_bmg_1/BSIMCMG_TMI_Model_1_usage.1"
```

The above example sets the bias voltage for models `nch1` and `nch2` to `1.2`, and the bias voltage for models `pch1` and `pch2` to `1.1`.'

## **output\_subckt\_degrad**

```
output_subckt_degrad { sub= sub1 [sub2]...} { vdd = "vdd_value1 [subckt_list...]"
 ["vdd_value2 [subckt_list...]"]...} [vdlin = vdlin_value1 [subckt_list...]
 [vdlin_value2 [subckt_list...]...] [vgsat = vgsat_value1 [subckt_list...] [vgsat_value2 [subckt_list...]...] [vglin = vglin_value1 [subckt_list...] [vglin_value2 [subckt_list...]...] { node = node_name1 [node1_terminals] [node2_name [node2_terminals]]... } { correct_bias_voltage = no|yes } {ivth = "value1 model1" ["value2 model2"]...} ivthn = value ivthp = value file = file_path
```

### **Description**

Outputs the subcircuit degradation (Idlin, Idsat, Vth degradation) information to a .bt0 file. Since a subcircuit is treated as a MOSFET device, it should have at least four terminals which map to drain (D), source (S), gate (G), and bulk (B) of the MOSFET.

The subcircuit degradation calculation is based on following fixed bias conditions:

#### **NMOSFET**

- Idsat: Vds=Vdd, Vgs=Vgsat if Vgsat is specified for the target subcircuit, otherwise Vgs=Vdd.
- Idlin: Vds=Vdlin if Vdlin is specified for the target subcircuit, otherwise Vds=0.05V; Vgs=Vglin if Vglin is specified for the target subcircuit, otherwise Vgs=0.05.
- Vth: Vds=Vdlin if Vdlin is specified for the target subcircuit, otherwise Vds=0.05V; Vgs=Vglin if Vglin is specified for the target subcircuit, otherwise Vgs=0.05.

#### **PMOSFET**

Idsat: Vds=Vdd, Vgs=Vgsat if Vgsat is specified for the target subcircuit, otherwise Vgs=Vdd.

Idlin: Vds=Vdlin if Vdlin is specified for the target subcircuit, otherwise Vds=-0.05V; Vgs=Vglin if Vglin is specified for the target subcircuit, otherwise Vgs=0.05.

Vth: Vds=Vdlin if Vdlin is specified for the target subcircuit, otherwise Vds=-0.05V; Vgs=Vglin if Vglin is specified for the target subcircuit, otherwise Vgs=0.05.

## Arguments

|                    |                                                                                                                                                                                                                        |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>sub</code>   | List of subcircuits for which degradation needs to be performed. This argument is mandatory.                                                                                                                           |
| <code>vdd</code>   | Sets the bias voltage for the subcircuit to obtain <code>gm</code> , <code>gds</code> , <code>Idlin</code> , <code>Idsat</code> , and <code>Vth</code> degradation for the TMI aging flow. This argument is mandatory. |
| <code>vdlin</code> | Vds value for <code>Idlin</code> / <code>Vt</code> measurement.                                                                                                                                                        |
| <code>vgsat</code> | Vgs value for <code>Idsat</code> measurement.                                                                                                                                                                          |
| <code>vglin</code> | Vgs value for <code>Idlin</code> / <code>Vt</code> measurement.                                                                                                                                                        |
| <code>node</code>  | Specifies the four-terminal node name in the order D G S B for each subcircuit. If a node is not specified, the first four terminals of the subcircuit are taken as D G S B by default.                                |
| <code>ivth</code>  | Specifies the constant current value for the specified model.                                                                                                                                                          |
| <code>ivthn</code> | Specifies the constant current value for NMOS.                                                                                                                                                                         |
| <code>ivthp</code> | Specifies the constant current value for PMOS.                                                                                                                                                                         |
| <code>file</code>  | Specifies the path of the include file.                                                                                                                                                                                |

**Note:** The `output_subckt_degrad` options can be specified in the included file.

`correct_bias_voltage`

Specifies whether to correct the bias voltage of the specified devices. Possible values are `no` and `yes`. The default value is `yes`.

## Example

```
output_device_degrad sub = [sub1 sub2] vdd=["1.2 sub1" "1.1 sub2"] tmi_lib_inc="./
model_bmg_1/BSIMCMG_TMI_Model_1_usage.1"
```

The above example sets the bias voltage for subcircuit `sub1` to 1.2 and for subcircuit `sub2` to 1.1.

## preset (\*relxpert: .preset)

```
preset {age|deg|lifetime} [agelevel=integer] mod=[mod1 mod2...] dev=[dev1 dev2...]
```

**Note:** The Spectre syntax for `preset` is currently not compatible with RelXpert.

### Description

This statement is used to preset the total `age`, `deg` (degradation), or `lifetime` values of devices in the netlist file. If `preset` is set, Spectre uses the values directly, but does not calculate them. The `preset` statement is useful if you already know the `age|degradation|lifetime` of blocks or devices, and want to preset the values in order to speed up the calculation.

If the `preset` is `age`, the simulator does not perform age calculation for the specified devices, models, or blocks. Lifetime or degradation calculations are based on the preset `age` value. If the `preset` is `lifetime` or `deg`, the simulator derives the age from the preset lifetime or degradation values to calculate degradation or lifetime for the specified devices, models, or blocks.

**Note:** In the current release, the `preset` reliability option works only for aging analysis in the appendage flow.

### Arguments

|                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>age</code>      | The age value of the device, model, or block.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <code>deg</code>      | The degradation value of the device, model, or block.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <code>lifetime</code> | The lifetime value of the device, model, or block.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <code>agelevel</code> | Defined for Hot-Carrier injection (HCI), negative bias temperature instability (NBTI), or positive bias temperature instability (PBTI) modeling. The following <code>agelevel</code> values are assigned for different modeling types: <ul style="list-style-type: none"><li>■ HCI: <code>agelevel=0</code></li><li>■ NBTI: <code>agelevel=1</code></li><li>■ PBTI: <code>agelevel=2</code></li></ul> The default behavior is to calculate both HCI and NBTI, or both HCI and PBTI. |
| <code>mod</code>      | The list of models. Wildcard (*) is supported.                                                                                                                                                                                                                                                                                                                                                                                                                                      |



`dev` The list of devices. Wildcard (\*) is supported.

### Examples

The following example

```
preset age=1.0001e-5 agelevel=1 dev=x1.mp1
```

tells the simulator to set the device `x1.mp1` NBTI age value to `1.001e-5`.

The following example

```
preset deg=1.01e-02 mod=PMOS
```

tells the simulator to set the degradation value to `1.01e-02` for all devices which use the `PMOS` model.

The following example

```
preset lifetime=10y agelevel=0 dev=X2*mp1
```

tells the simulator to set the `lifetime` value to 10 years for all devices or for devices with hierarchical names that begin with the `X2` prefix and end with the `mp1` suffix (for example, `X2.mp1`, `X21.mp1`, and `X2.X22.mp1`).

## rel\_mode (\*relxpert: .rel\_mode)

```
rel_mode type=[aging|she|all]
```

### Description

Specifies the type of analysis to be used for obtaining the reliability values of MOSFETs.

For `type=she` and `type=all`, the specified device power and temperature rise are calculated using the `calcDeltaPower()`, `calcPower()`, and `calcTrise()` URI functions and stored in the `.bw0` and `.bh0` files.

You can output the device power (`.bw0`) in the self-heating flow by using the output\_she\_power (\*relxpert: .output\_she\_power) control statement.

The URI library can be added using the uri\_lib (\*relxpert: .uri\_lib) control statement.

**Note:** For self-heating calculation, you can use URI or the internal self-heating model (`agelevel=3`). When using URI, ensure that a standalone `agelevel` is used for self-heating calculation. Do not use URI and the internal self-heating model for self-heating calculation at the same time.

### Arguments

|                         |                                                                                 |
|-------------------------|---------------------------------------------------------------------------------|
| <code>type=she</code>   | Uses the self-heating flow to obtain the reliability values.                    |
| <code>type=aging</code> | Uses the aging flow to obtain the reliability values. This is the default flow. |
| <code>type=all</code>   | Use both self-heating and aging flows to obtain the reliability values.         |

### Example

```
rel_mode type=all
```

## **relx\_tran ( \*relxpert: .relx\_tran )**

```
relx_tran start=start_time stop=stop_time mult_win [start_time1 stop_time1
start_time2 stop_time2...]
```

### **Description**

Specifies the start and stop time for reliability simulation during transient simulation.

### **Arguments**

|                               |                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>start=start_time</code> | Specifies the start time of reliability analysis during transient simulation.                                                                                                                                                                                                                                                                                                                        |
| <code>stop=stop_time</code>   | Specifies the stop time of reliability analysis during transient simulation.<br><br>Default: If <code>stop_time</code> is not specified, the software stops in <code>.tran</code> statement.                                                                                                                                                                                                         |
| <code>mult_win</code>         | Specifies multiple time windows for reliability analysis during transient simulation. In the argument, <code>start_time</code> and <code>stop_time</code> values must be specified in pairs. The <code>start</code> and <code>stop</code> arguments and the <code>multi_win</code> argument are mutually exclusive and cannot be used together. If you specify them together, an error is generated. |

### **Example**

```
relx_tran start = 1n stop = 10n
*relxpert: relx_tran 1n 10n
```

Specifies that the start time for reliability simulation during transient simulation is 1n and the stop time for reliability simulation during transient simulation is 10n.

```
relx_tran start=100u stop=500n mult_win =[100n 200n 300n 400n 450n 500n]
```

Perform reliability analysis in the following time windows during transient simulation:

(100n 200n), (300n 400n), and (450 500n).

## **report\_model\_param (\*relxpert: .report\_model\_param )**

`report_model_param value = {yes | no}`

### **Description**

Determines whether to print the fresh and aged parameters in the `.bm#` file. When set to `yes`, the fresh and aged parameters are printed to the `.bm#` file.

### **Arguments**

|                        |                                                                                 |
|------------------------|---------------------------------------------------------------------------------|
| <code>value=yes</code> | Prints the fresh and aged parameters in the <code>.bm#</code> files.            |
| <code>value=no</code>  | Skips printing of the fresh and aged parameters in the <code>.bm#</code> files. |

### **Example**

```
report_model_param value = yes
*relxpert: report_model_param yes
```

Prints the fresh and aged parameters in the `.bm#` file.

## simmode

```
simmode { type = [stress | aging | all] } file = filename [tmifile=filename]
```

## Description

Normally, reliability simulation includes stress and aging transient analysis. This option enables you to choose which transient analysis to run in the reliability simulation. The default value is `all` and runs both stress and aging transient analysis.

## Arguments

|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>type=stress</code> | Runs only the stress transient analysis in reliability simulation.                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <code>type=aging</code>  | Runs only the aging transient analysis in reliability simulation.                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>type=all</code>    | Runs both stress and aging transient analyses in reliability simulation.                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <code>file</code>        | Specifies the file name to which the scaled model parameter names and values will be saved. If the file name is not specified the results are saved in the default file <code>*.bs0</code> .                                                                                                                                                                                                                                                                                                                          |
| <code>tmifile</code>     | Specifies the file to which the scaled model parameter names and values will be saved in the TMI aging flow. If <code>type=stress</code> or <code>all</code> , the behavior of <code>tmifile</code> is the same as the <code>tmioutput</code> option in the TMI aging flow and the default value is <code>*_tmioutput</code> . If <code>type=aging</code> , the behavior of <code>tmifile</code> is the same as <code>tmiinput</code> option in the TMI aging flow and the default value is <code>*_tmiinput</code> . |

## Example

```
simmode type = aging file= input.bs0
```

Specifies that the aging transient simulation be run and the results be saved in the file `input.bs0`.

## **tmi\_aging\_mode (\*relxpert: .tmi\_aging\_mode)**

`tmi_aging_mode type=[aging|she|all]`

### **Description**

This option is used to specify the TMI self-heating or aging mode for the TMI aging flow.

### **Arguments**

|                         |                                                      |
|-------------------------|------------------------------------------------------|
| <code>type=aging</code> | Enable only the TMI aging mode. This is the default. |
| <code>type=she</code>   | Enable only the TMI self-heating mode.               |
| <code>type=all</code>   | Enable both TMI aging and self-heating modes.        |

### **Example**

```
tmi_aging_mode type=all
```

## **tmi\_she\_mindtemp (\*relxpert: .tmi\_she\_mindtemp)**

`tmi_she_mindtemp value=value`

### **Description**

Sets the minimum delta temperature induced by self-heating for transistor devices. If the temperature change for a transistor is less than the minimum delta temperature value, the second self-heating run is not required.

**Note:** This option works only in the TMI self-heating flow.

### **Arguments**

|                    |                                                                                                |
|--------------------|------------------------------------------------------------------------------------------------|
| <code>value</code> | Sets the minimum delta temperature value. The default value is 0.0 and the unit is in celsius. |
|--------------------|------------------------------------------------------------------------------------------------|

### **Example**

```
tmi_she_mindtemp value=10
*relxpert: .tmi_she_mindtemp value=10
```

## uri\_lib ( \*relxpert: .uri\_lib )

```
uri_lib file = { "uri_lib_name" } uri_mode= [scaleparam | appendage | appendage1
| appendage2] debug = [0 | 1] scale_mode = [original | effective]
```

### Description

Loads the Unified Reliability interface (URI) shared library.

**Note:** For more information on the URI functions, see the *Unified Reliability Interface Functions* section in the *Spectre® Unified Reliability Interface Reference*.

### Arguments

`file=uri_lib_name`

Specifies the shared library name.

`uri_mode`

Specifies which method should be used to perform aging simulation. Possible values are `scaleparam` (default), `appendage`, `appendage1`, and `appendage2`.

**Note:** The `appendage` method is not supported in the MMSIM11.1 and earlier releases.

**Note:** `uri_mode=appendage1` is equivalent to `uri_mode=appendage` in releases prior to SPECTRE18.1ISR3.

**Note:** In Spectre18.1ISR3, the `appendage` method has been replaced by the `appendage2` method. Therefore, if you specify `uri_mode=appendage`, it is equivalent to `uri_mode=appendage2`. The `appendage1` method can be used for backward compatibility with earlier releases.

For the `appendage2` method, you are required to run the stress and aging simulations in a separate netlist. First, you need to run a stress simulation using the `simmode` option and then run the aging simulation using the intermediate file that is generated during the stress simulation.

`debug`

Specifies whether to print the debug information. The default value is 0.



`scale_mode` Specifies the parameter scaling mode for URI library. If `scale_mode=effective` is specified, the effective parameter is passed to URI for scaling. If `scale_mode=original` is specified, the original parameter is passed to URI for scaling.

## Example

```
uri_lib file = "./libURI.so" uri_mode = scaleparam debug =1
*relxpert: uri_lib "./libURI.so" uri_mode = scaleparam debug=1
```

Specifies the `libURI.so` URI library and the `agemos` URI mode. In addition, requests the debug information to be generated.

**Note:** You can also use the `RELXPERT_URI_LIBS` environment variable to set the URI library. If you use both the `RELXPERT_URI_LIBS` environment variable and the `uri_lib` control statement, the `RELXPERT_URI_LIBS` environment variable takes higher precedence over the `uri_lib` control statement.

## Example2

The following is an example of using the `appendage2` method:

```
//Reliability block setting for stress simulation
rel reliability {
 age time =[10yr]
 uri_lib file="uriLib.so" uri_mode=appendage2
 simmode type=stress
 tran_stress tran stop=10n
}
//Reliability block setting for aging only netlist
rel reliability {
 age time =[10yr]
 uri_lib file="uriLib.so" uri_mode=appendage2
 simmode type=aging file="input.bs0" //input.bs0 is intermediate file generated
 in stress)

 tran_stress tran stop=10n
```

## vdsmethod

`vdsmethod type = [internal | external]`

### Description

Specifies how the simulator would use the `vds` values for reliability calculations. When set to `internal`, reliability simulation sets `vds` to use the internal value. If set to `external`, reliability simulation sets `vds` to use the external value.

### Arguments

|                            |                                                                          |
|----------------------------|--------------------------------------------------------------------------|
| <code>type=internal</code> | Use the internal value for <code>vds</code> .                            |
| <code>type=external</code> | Use the external value for <code>vds</code> . This is the default value. |

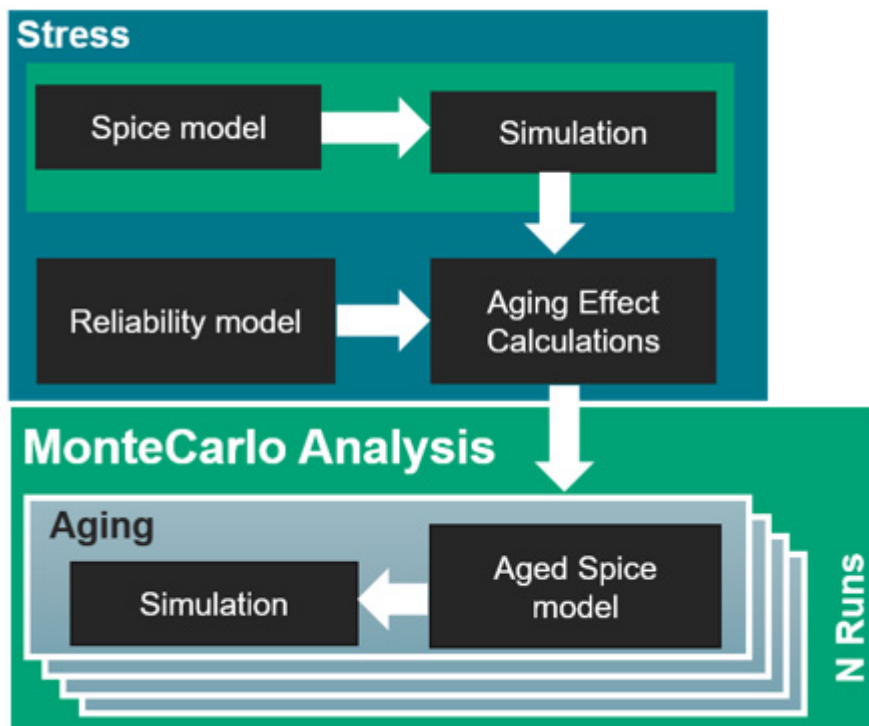
### Example

```
vdsmethod type=internal
```

## Aging Monte Carlo Analysis

Spectre reliability analysis supports the following two flows to perform aging MonteCarlo analysis for the agemos and appendage flow:

- **1+N method:** In this method, a nominal stress analysis is run first. Next, MonteCarlo analysis is performed on the aging analysis. No variations are performed on the stress analysis.



The following is an example of a reliability block for the stress simulation:

```
rel reliability {
 // reliability control statements
 age time = [10y]
 deltax value = 0.1
 report_model_param value=yes
 simmode type=stress

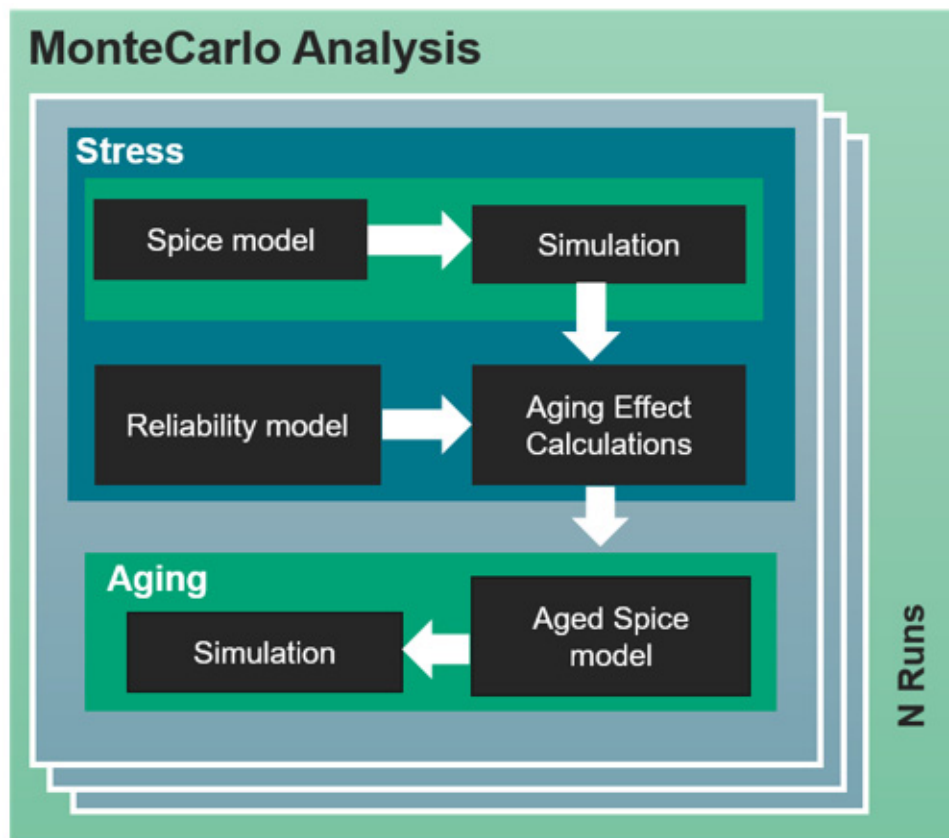
 // fresh/stress simulation.
 tran_stress tran start = 0 step = 1u stop = 10u
}
```

The following is an example of a reliability block for the aging Monte Carlo simulation:

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```
mcl montecarlo numruns=100 seed=12345 variations=all sampling=standard \
savedatainseparatedir=yes savefamilyplots=yes {
 rel reliability {
 // reliability control statements
 age time = [10y]
 deltad value = 0.1
 report_model_param value=yes
 // fresh/stress simulation.
 simmode type=aging file="stress.bs0"
 // aging simulation statements.
 tran_aged tran start = 0 step = 1us stop = 10us
 }
}
```

- **N+N method:** In this method, Monte Carlo analysis is performed on both stress and aging simulations. This method can be run on a single netlist or separate netlist.



The following is an example of running stress and aging analyses in the same netlist:

```
mcl montecarlo numruns=100 seed=12345 variations=all sampling=standard
```

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---

```
savadatainseparatedir=yes savefamilyplots=yes {
rel reliability {
 // reliability control statements
 age time = [10y]
 deltad value = 0.1
 report_model_param value=yes
 // fresh/stress simulation.
 tran_stress tran start = 0 step = 1u stop = 10u
 // aging simulation statements.
 tran_aged tran start = 0 step = 1us stop = 10us
}
}
```

The following is an example of running stress and aging analyses in separate netlists:

```
mcl montecarlo numruns=100 seed=12345 variations=all sampling=standard
savadatainseparatedir=yes savefamilyplots=yes {
rel reliability {
 // reliability control statements
 age time = [10y]
 deltad value = 0.1
 uri_lib file="libURI.so" uri_mode=appendage
 report_model_param value=yes
 simmode type=stress
 // fresh/stress simulation.
 tran_stress tran start = 0 step = 1u stop = 10u
}
}

mcl montecarlo numruns=100 seed=12345 variations=all sampling=standard
savadatainseparatedir=yes savefamilyplots=yes {
rel reliability {
 // reliability control statements
 age time = [10y]
 deltad value = 0.1
 report_model_param value=yes
 uri_lib file="libURI.so" uri_mode=appendage
 // fresh/stress simulation.
 simmode type=aging file="stress.bs0"
 // aging simulation statements.
 tran_aged tran start = 0 step = 1us stop =10us
}
}
```

## User-Defined Reliability Models

Cadence provides a unified reliability interface (URI) to allow you to implement customized models for running reliability simulation. Contact Cadence support or refer to URI document for more information.

## Measuring the Reliability Analysis

To measure the reliability analysis that is defined in the reliability block, you need to specify the `.measure` MDL statement right before or after the reliability block. For example:

```
rel reliability {

// reliability control statements
age time = [10y]
deltad value = 0.1
report_model_param value=yes

// fresh/stress simulation.
tran_stress tran start = 0 step = 1u stop = 10u // Need add the one parameter for
identify the fresh tran.

// aging simulation statements.
tran_aged tran start = 0 step = 1us stop = 10us // Need add the one parameter for
identify the aged tran.
}

simulator lang = spice
.measure tran nmos_width PARAM='(1e6)*wn'
```

In the above example, the `.measure` statement will work for the `tran_aged` transient analysis.

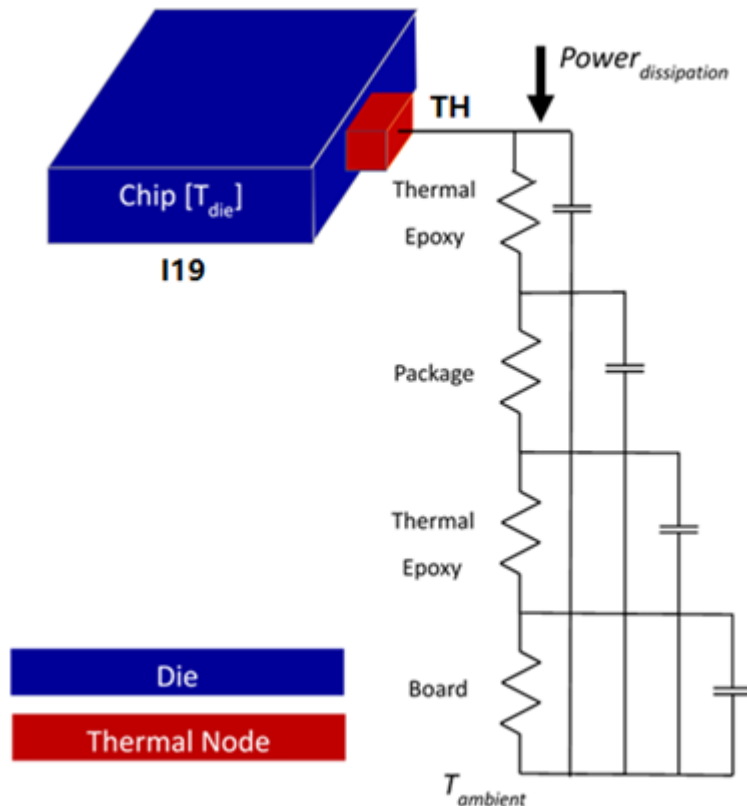
## **Thermal Nodes**

You can define the thermal nodes in the Spectre netlists. Thermal nodes provide you the ability to dynamically analyze the effect of temperature on the electrical behavior of the design during simulation. In the past, you could perform thermal analysis by changing the simulation ambient temperature directly or using dynamic parameters to change the ambient temperature during transient analysis. Dynamic parameters change the temperature during simulation, however, the temperature is independent of the circuit's electrical behavior. The Spectre thermal node enables you to couple the temperature and power of a subcircuit or a device model. The thermal node is connected to a thermal impedance to simulate the effect of temperature on the electrical behavior of the design during simulation. You can use it as:

- an external point of connection, for example, simulating the effect of packaging on a circuit's electrical performance
- or
- an internal node, for example, to model device self-heating effect

## External Thermal Node

The following figure displays an external thermal node:



You can use the Spectre `temnode` statement to create thermal nodes. In the following example, a thermal node `TH` is created for the subcircuit instance `I19` and is connected to the ambient through the JEDEC package modeled by the subcircuit `JEDEC_package`:

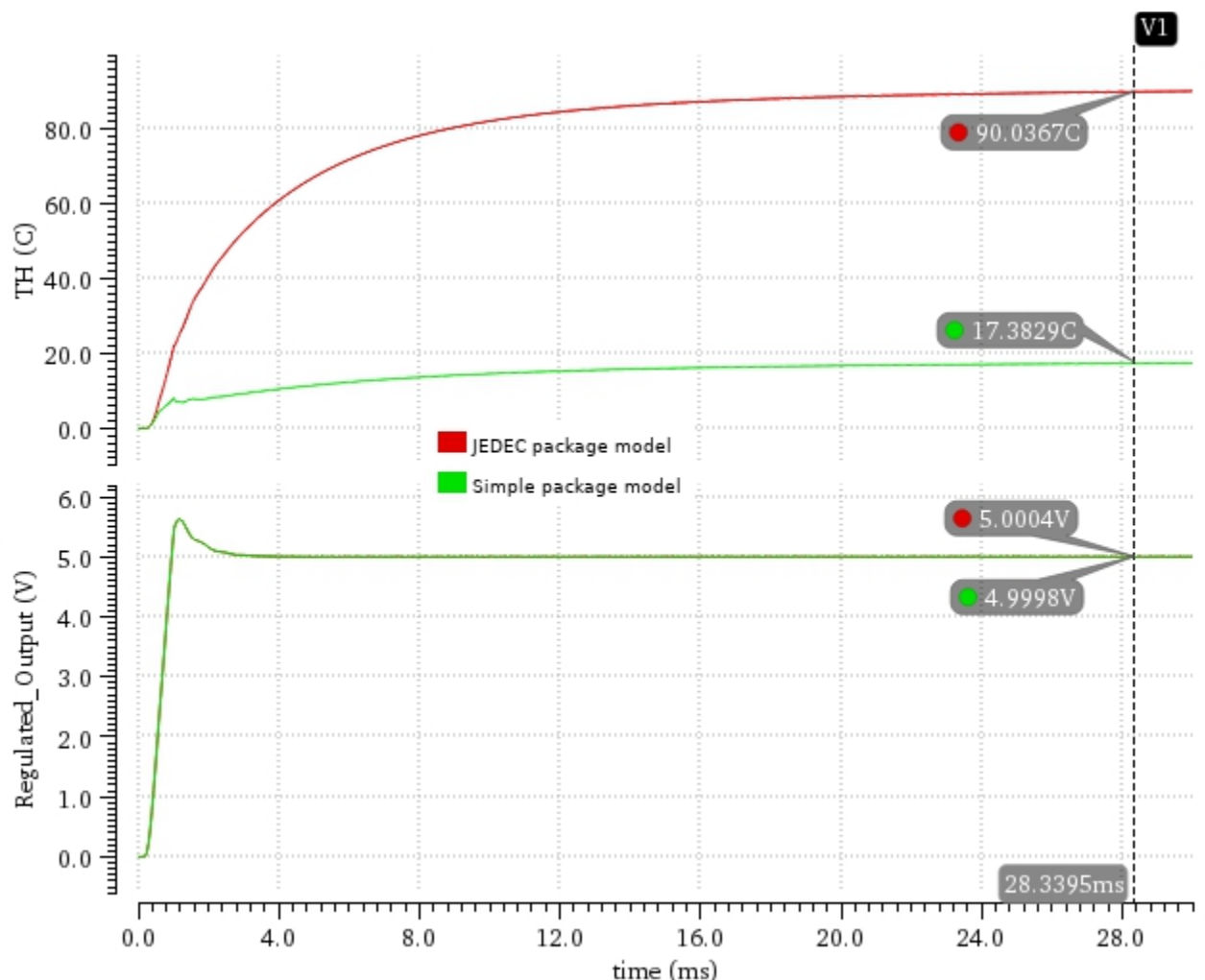
```
subckt dc2dc_updated_core_1 VDD Switcher VSS Vfb Vosc Vref inh_bulk_n

ends dc2dc_updated_core_1
subckt JEDEC_package JUNCTION AMBIENT

ends JEDEC_package
tn1 (TH) temnode sub=I19
I16 (TH 0) JEDEC_package
I19 (net070 Switcher_Out 0 net051 net026 net021 0) dc2dc_updated_core_1
```



The following figure displays the simulation results for the external thermal node:



During simulation, the power dissipated within the subcircuit `I19` is output at the thermal node defined by the `tempnode` statement (`sub=I19`). It is applied to the thermal package model and the result is the temperature rise from the ambient temperature of the subcircuit `I19`. The temperature at `TH` is applied to the `dTemp` instance properties of all the instances in the subcircuit `I19`. You can save the simulation results by adding the thermal node `TH` to the Spectre `save` statement:

```
save TH
```

Spectre also supports the Spice syntax for thermal node creation. The Spice equivalent of the above Spectre `tempnode` statement is shown below.

```
.tempnode TH sub=I1s9
```

The simulation example shows the simulation results for a DC-to-DC Converter with two different package models. The simple model is a shunt `R [1 Ohm] || C [1 mF]` to represent the package. The JEDEC model is more complex with longer thermal time constants. In this simulation, the electrical characteristics are not greatly affected by the 20C temperature rise due to the packaging.

### Internal Thermal Node

Thermal nodes can also be created at nodes within a subcircuit or a device model to allow modeling simulation of the self-heating effect.

In the following example, a thermal node `TH` is created inside a subcircuit `test` by adding the `tempnode` statement. However, unlike the external thermal node example, the `sub` keyword is not used, therefore, the temperature at `TH` will modify the `dTemp` value of all the instances inside the subcircuit. As a result, the resistor `ra` will now operate at a temperature of ambient temperature, `tnom`, + temperature rise, `dTemp`, where `dTemp` is the product of the resistor power and thermal self-impedance (`rthn || cthn`).

```
subckt test a b
 ra (a b) resistor r=1k tc1=0.1
 tn1 (TH) tempnode
 rthn (TH 0) resistor r=10
 cthn (TH 0) capacitor c=0.1
ends test
x1 (a b) test
```

Spectre recognizes `rthn` and `cth` as thermal elements because they are connected to the thermal node. They are treated as thermal elements, not as electrical elements. Thermal elements are described in terms of power and temperature instead of current and voltage.

## **SpectreThermal Analysis**

Spectre APS thermal analysis, Spectre Thermal, performs electrothermal simulation using Cadence® Thermal Extractor and delivers true electrothermal co-simulation. In the Spectre thermal analysis flow, the thermal extractor is used to extract a thermal model of the die, based on the chip structure and thermal properties of the die stack.

Spectre thermal analysis is different from self-heating (SHE) analysis because it considers the thermal interactions between devices. In addition, it considers all the power sources in the chip, including transistors, resistors, and other devices.

This section discusses the following topics:

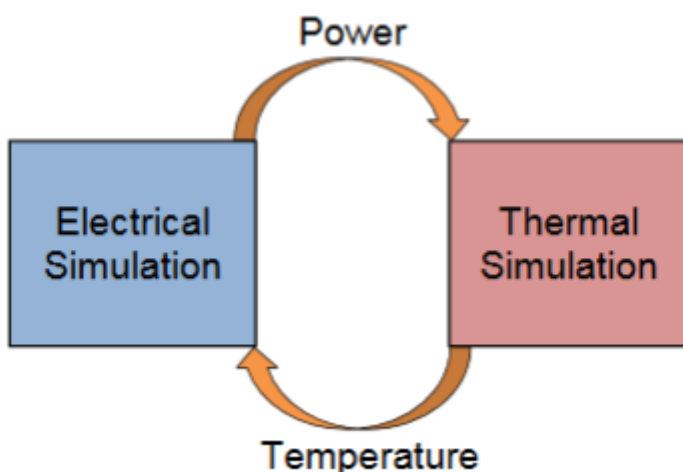
- [Spectre Thermal Analysis Technology, Product, and Flow Overview](#) on page 536
- [Thermal Control Files](#) on page 545
- [Getting Started with Spectre Thermal Analysis](#) on page 553

## Spectre Thermal Analysis Technology, Product, and Flow Overview

### Technology Overview

In the Spectre thermal analysis flow, the first step is to generate a thermal model, which is a description of the thermal characteristics of a design. The thermal model is created using the chip structure, physical design and die stack, and thermal conductivity of materials. It is a thermal equivalent circuit of the die. Spectre thermal analysis uses the electrical and thermal descriptions of the circuit, the netlist, and the thermal model to perform electrothermal simulation.

Spectre thermal analysis starts with an electrical simulation and uses the instance power to drive a thermal solution to calculate the temperature of the instances on the die. If the temperatures converge, the simulation is complete. If not, the thermal and electrical simulation process continues until the results converge to a stable solution that satisfies both the circuit electrical power and the circuit temperature condition. This process is called electrothermal co-simulation or electrothermal simulation.



The Spectre thermal analysis flow requires a complete testbench including stimuli, device models, and all files required for a regular Spectre simulation. The circuit information is included in the DSPF file (with instances and/or parasitic sections). To enable Spectre thermal analysis, add the testbench netlist in the `reliability` block using the thermal analysis statement, as shown below.

```
rel reliability
{
 myThermal thermal config "thermal.conf" <options>
```

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---

```
{
 tran_thermal tran stop=100n
}
```

Most of the thermal analysis control settings are specified as options in the `thermal` analysis statement. A `config` option is required to further specify the location of the thermal technology file and the location of the thermal package file.

Spectre thermal analysis supports both steady state and dynamic thermal analysis, which is controlled by the `method` option.

You can use the following options to specify the control settings for the Spectre thermal analysis. These options may be relevant to the steady state thermal analysis, dynamic thermal analysis, or both.

| Option                     | Description                                                                                                                                                                                                                 | Default Value            |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
| <code>title</code>         | Analysis title                                                                                                                                                                                                              |                          |
| <code>annotate</code>      | Specifies the degree of annotation. Possible values are <code>no</code> , <code>title</code> , <code>sweep</code> and <code>status</code> .                                                                                 | <code>sweep</code>       |
| <code>config</code>        | Specify the location of the thermal configuration file. This option is mandatory.                                                                                                                                           | <code>None</code>        |
| <code>sort</code>          | Sort the instances in steady state thermal analysis reports by <code>Trise</code> ( <code>trise</code> ) or power ( <code>pwr</code> ).                                                                                     | <code>trise</code>       |
| <code>maxinst</code>       | Specify the number of instances to be included in steady state thermal analysis reports                                                                                                                                     | <code>all</code>         |
| <code>method</code>        | Select the thermal analysis mode, the options are either steady state ( <code>steadystate</code> ) or dynamic ( <code>dynamic</code> ) thermal analysis.                                                                    | <code>steadystate</code> |
| <code>numiter</code>       | Number of steady-state electrothermal iterations to be performed.                                                                                                                                                           | <code>2</code>           |
| <code>res_trise_rpt</code> | Include resistor temperature for thermal reports. Possible values are <code>yes</code> , <code>no</code> , and <code>laststep</code> . Only instance temperatures are reported when this option is set to <code>no</code> . | <code>no</code>          |
| <code>save_inst</code>     | List of instance names for which temperature and power are to be included in dynamic thermal analysis reports.                                                                                                              | <code>Empty</code>       |

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|                        |                                                                                                                                                                                                                                       |                                   |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| dbg_output             | Generate .dbg_trise_iter* and .thermal_pwr.iter* files in the raw file directory for steady state thermal analysis.                                                                                                                   | 0                                 |
| dbg_output_sort        | Device sorting order in debug reports (.dbg_trise_iter* and .thermal_pwr.iter*) for steady state thermal analysis. Possible values are index, trise, and power.                                                                       | trise                             |
| probe_output_format    |                                                                                                                                                                                                                                       |                                   |
|                        | Specifies the format of the output by the probe. Possible values are binary, txt, and both.                                                                                                                                           | binary                            |
| chip_bbox              | A vector of four numbers [llx lly urx ury] representing a user-defined chip bounding box. By default, the chip bounding box is calculated from the device geometries so that a tight bounding box containing all the devices is used. | Calculated from device geometries |
| frame_freq             | Specify the time step interval for thermal trise data output                                                                                                                                                                          | 3                                 |
| trise_lowerlmt         | Specify the lower limit for Trise.                                                                                                                                                                                                    | 0                                 |
| trise_lmt              | Limit the value of Trise used for updating the device temperatures. This helps to prevent device temperatures from going out of valid range during electrical simulation. Unit is degree centigrade.                                  | 300                               |
| thermal_ignore_para_rc |                                                                                                                                                                                                                                       |                                   |
|                        | Select whether ignore parasitic RC for thermal analysis. Possible values are no, yes and pwrOnly.                                                                                                                                     | no                                |
| check_inst_overlapped  |                                                                                                                                                                                                                                       |                                   |
|                        | Check overlapped instances. Possible values are no and yes.                                                                                                                                                                           | no                                |
| keep_ori_cap           | Keep original cap value from tdb file or not. Possible values are no and yes.                                                                                                                                                         | no                                |
| keep_pkg_grid          | Keep package grid from tdb file or not. Possible values are no and yes.                                                                                                                                                               | no                                |
| saveonlylaststepdata   |                                                                                                                                                                                                                                       |                                   |

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|                                  |                                                                                                                                                   |                     |
|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
|                                  | Dump the waveform files in a separate directory for steady-state. Possible values are <code>no</code> and <code>yes</code> .                      | <code>no</code>     |
| <code>save_channelonly</code>    |                                                                                                                                                   |                     |
|                                  | Select the output layer for thermal trise data output. Possible values are <code>no</code> and <code>yes</code> .                                 | <code>no</code>     |
| <code>save_layer</code>          | List of layer names for which <code>trise</code> will be reported in the thermal <code>.temp_grid</code> file.                                    | All layers          |
| <code>save_timepoints</code>     | Save temperature file at specific time points.                                                                                                    | All layers          |
| <code>save_timewindows</code>    |                                                                                                                                                   |                     |
|                                  | Save temperature file during specific time interval.                                                                                              | All layers          |
| <code>trise_lowerlmt</code>      | Specifies the minimum Trise.                                                                                                                      | 0.0C                |
| <code>trise_db_type</code>       | Select thermal data output format. Possible values are <code>binary</code> and <code>txt</code> .                                                 | <code>binary</code> |
| <code>thermal_data_format</code> |                                                                                                                                                   |                     |
|                                  | Select trise data output format. Possible values are <code>none</code> , <code>binary</code> and <code>txt</code> .                               | <code>binary</code> |
| <code>thermal_flushpoints</code> |                                                                                                                                                   |                     |
|                                  | Specify the flush points number for thermal data output.                                                                                          | -1                  |
| <code>thermal_flushtime</code>   |                                                                                                                                                   |                     |
|                                  | Specify the flush interval for thermal data output.                                                                                               | -1                  |
| <code>thermal_step</code>        | Specifies the thermal time step (seconds) for dynamic thermal solver. Set this parameter to 0 to get identical electrical and thermal time steps. | 0.0                 |
| <code>thermal_step_ratio</code>  |                                                                                                                                                   |                     |
|                                  | If ratio is X, it means that do thermal solver once every X tran steps.                                                                           | 1                   |
| <code>thermal_trise_step</code>  |                                                                                                                                                   |                     |
|                                  | Trise threshold for using thermal solver.                                                                                                         | 0.0                 |

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Once the reliability block is set up in the input netlist, Spectre thermal analysis is automatically invoked when running Spectre APS simulation. For example, if the name of the input netlist is `input.scs`, you can use the following command to invoke Spectre thermal analysis:

```
% spectre -64 +aps input.scs
```

### Product Overview and Spectre Thermal Analysis Flow

The Spectre thermal analysis consists of the following three components:

- Spectre APS for electrical simulation

Spectre APS is used for electrical simulation, which computes the power of each power dissipating instances in the circuit: MOS transistors, resistors, diodes, and bipolar transistors.

- Cadence® Thermal Extractor

Cadence® Thermal Extractor is called internally by Spectre APS to perform thermal extraction of the die and to create the thermal model used in electrothermal simulation.

- Spectre APS for thermal simulation

Spectre APS is used for thermal simulation. It calculates the instance temperatures based on the power consumption of the instances. The thermal solver is built into the electrothermal simulation and is not available as a standalone offering.

In addition to these components, Spectre thermal analysis also includes enhancement to Spectre APS for electrothermal simulation. Spectre APS automatically maps the information from the electrical simulator, power, to the thermal solver and maps the information from the thermal solver, temperature, back to the electrical simulator. After defining where the data is stored and how to perform the simulation, the electrothermal simulation runs automatically until completion.

### ***Spectre Steady State Analysis Flow***

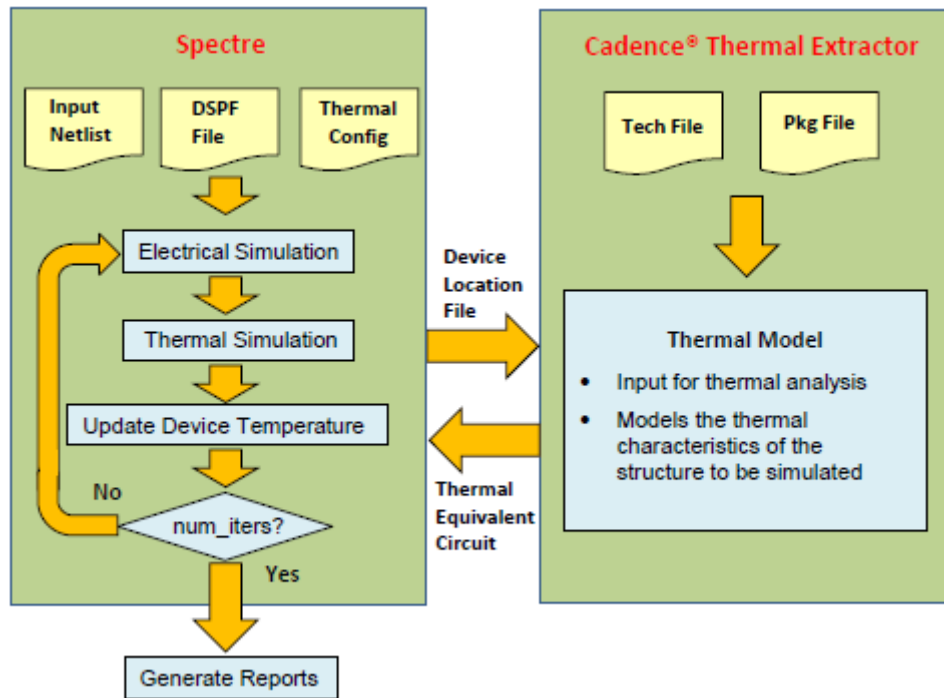
For steady-state thermal simulation, electrothermal simulation starts with an electrical simulation with the device temperatures initially set to the ambient value.

Upon completion of the electrical simulation, the average power of all the devices is computed and sent to the thermal solver to compute the temperature rise for each device as a result of the steady-state instance power. The calculated instance temperatures are then used to update the instance temperatures for the next iteration of the electrothermal simulation. The process continues until the user-specified iteration count is reached. The output of the



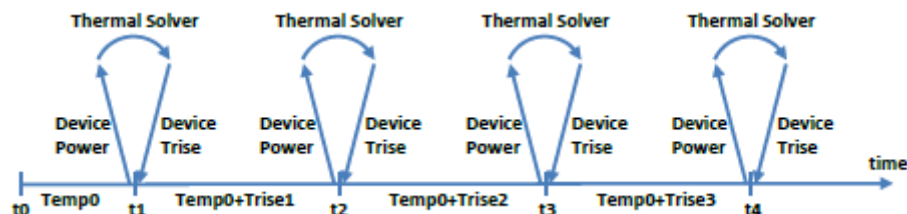
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steady-state thermal simulation is a text report, which lists the temperature rise and the average power of each device in the DSPF netlist.



### ***Spectre Dynamic Thermal Analysis Flow***

Dynamic thermal analysis is run by performing thermal solving at each time step of the Spectre transient analysis. Because thermal variation is usually much slower than electrical variation, it is assumed that convergence of electrothermal co-simulation is always achieved with just one iteration at each time step. Therefore, no iterations are needed for the electrothermal co-simulation during dynamic thermal analysis. This greatly increases the efficiency of the dynamic thermal analysis algorithm without introducing significant errors.



## **DSPF Requirements**

The Spectre thermal analysis flow is based on using DSPF. A DSPF file is required to include all electrical and geometric information needed for thermal analysis. The following figure

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shows a representative DSPF netlist with all important information for thermal model generation being marked in color.

```
*|DSPF 1.5
*
*|DATE "Wed May 16 21:53:06 2018"
*|VENDOR "Cadence Design Systems"
*|PROGRAM "Cadence Quantus QRC Extraction"
*|VERSION "18.1.0 Linux 64 bit - (Thu Apr 5 16:57:32 PDT 2018)"
*|DESIGN "powermos_4m"
*|DIVIDER /
*|DELIMITER #
*|DeviceFingerDelim "@"
*|BUSBIT []** caps2d version: 10
*
.SUBCKT ldo_bist_att_1v2 ibias vss byp out ena vdd1v8
*
*Net Section
*
*|GROUND_NET VSS
*
*|LAYER_MAP
*0 none
*1 active
*2 poly_conn
*3 metall_conn
*4 metal2_conn

*|NET S1 0
*|P (S1 X 0 74.1400 -10.4200) // $llx=74.1400 $lly=-10.4200 $urx=74.1400 $ury=-10.4200 $lvl=3
*|I (MM0#d MM0 d X 0 3.7460 9.8750) // $llx=3.7460 $lly=9.8750 $urx=3.7460 $ury=9.8750 $lvl=4
*|S (S1#118743 63.6315 -10.2050) // $llx=63.6315 $lly=-10.2050 $urx=63.6315 $ury=-10.2050 $lvl=1
*|S (S1#118745 63.1840 -10.2050) // $llx=63.1840 $lly=-10.2050 $urx=63.1840 $ury=-10.2050 $lvl=1
*|S (S1#118746 62.5665 -10.2050) // $llx=62.5665 $lly=-10.2050 $urx=62.5665 $ury=-10.2050 $lvl=1
C1 S1#118743 VSS 4.90442e-14 $X=65.0175 $Y=54.885
C2 S1#118745 VSS 4.66118e-14 $X=64.8125 $Y=54.874
C3 S1#118746 VSS 4.66123e-14 $X=64.6075 $Y=54.873
Rh1 S1 S1#118743 0.058419 TC1=0.002278 TC2=-4.02e-07 $L=13.3585 $W=10.06 $LLX=63.631500
+ $LLY=-15.235000 $URX=76.990000 $URY=-5.175000 $X=68.8855 $Y=-10.205 $lvl=3
Rh2 S1#118743 S1#118745 0.001994 TC1=0.002278 TC2=-4.02e-07 $L=0.3585 $W=10.06
+ $LLX=63.184000 $LLY=-15.235000 $URX=63.543000 $URY=-5.175000 $X=63.3635 $Y=-10.205 $lvl=3
Rh3 S1#118745 S1#118746 0.003433 TC1=0.002278 TC2=-4.02e-07 $L=0.617 $W=10.06
+ $LLX=62.258000 $LLY=-15.235000 $URX=63.493000 $URY=-5.175000 $X=62.8755 $Y=-10.205 $lvl=3
*
*Instance Section
*
MNM0 MNM0#d MNM0#g MNM0#s S1 g45n1svt L=4.5e-08 W=0.0001
+ AD=1.4e-11 AS=1.6e-11 PD=0.00020028 PS=0.00020032
+ sa=1.4e-07 sb=2e-06 sca=1.93368 scb=7.47405e-05 scc=2.77238e-09
+ $X=3.723 $Y=54.8755
MNM0@1 MNM0@1#d MNM0@1#g MNM0@1#s S1 g45n1svt L=4.5e-08 W=0.0001
+ AD=1.6e-11 AS=1.6e-11 PD=0.00020032 PS=0.00020032
+ sa=3.45e-07 sb=2e-06 sca=1.93368 scb=7.47405e-05 scc=2.77238e-09
+ $X=3.928 $Y=54.8755
MNM0@2 MNM0@2#d MNM0@2#g MNM0@2#s S1 g45n1svt L=4.5e-08 W=0.0001
+ AD=1.6e-11 AS=1.6e-11 PD=0.00020032 PS=0.00020032
+ sa=5.5e-07 sb=2e-06 sca=1.93368 scb=7.47405e-05 scc=2.77238e-09
+ $X=4.133 $Y=54.8755
```

Important info for thermal solver:

- Subckt definition
- Layer information
- Bounding boxes of resistors
- Location and dimension of transistors or resistors

The location and dimension of parasitic resistors can be defined by one or both of the following two sets of data:

- Bounding box (\$LLX, \$LLY, \$URX, \$URY)
- Box center location (\$X, \$Y) and dimension \$L (length) and \$W (width)

For thermal simulation, the bounding box information is usually more accurate than location/dimension information because the dimension data often contains scaling factors that are intended for electrical modeling/computation and are not relevant for thermal modeling. Therefore, when both sets of information is provided in the DSPF file for parasitic resistors, the bounding box information is used and the location/dimension information is ignored. It is recommended that when generating DSPF files for Spectre thermal simulation, proper control switches are turned on so that bounding boxes are created for parasitic resistors. If Quantus QRC is used for DSPF netlist extraction, you can use the following options for the generation of parasitic resistor bounding boxes:

- `include_parasitic_res_bonding_box`
- `include_parasitic_res_via_array_bounding_box`
- `include_parasitic_res_counductor_bounding_box`

## **Thermal Control Files**

Electrothermal analysis is performed based on the information contained in the `reliability` block of the testbench. The `reliability` block must contain a thermal statement that defines the thermal configuration file as well as other information, such as the `tran` analysis statement.

### **Thermal Configuration File**

The thermal configuration file consists of two parts, the location of the data files required for thermal analysis, and additional options. The following two files are required for thermal analysis:

- Thermal technology file
- Thermal package file

The thermal technology file is defined with the keyword `tech_file` in the thermal configuration file and describes the die stack. It is the thermal equivalent of the ICT file and contains the thickness and the thermal properties of the materials of the die stack.

The thermal package file is defined with the keyword `package_file` in the thermal configuration file and describes the thermal characteristics of the package, which define the boundary conditions for thermal analysis. The following is the content of a sample thermal configuration file, where the location of the thermal technology and thermal package files are specified:

```
thermal tech_file = "tech.txt"
thermal package_file = "pkg.txt"
```

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In addition to the technology file and package file, the thermal configuration file can also include other options, as shown in the following table:

| Keyword | Options       | Description                                                                                                  | Default Value |
|---------|---------------|--------------------------------------------------------------------------------------------------------------|---------------|
| thermal | tech_file     | Location of technology file (required).                                                                      | None          |
|         | package_file  | Location of package file (required).                                                                         | None          |
| spf     | geounit       | Scaling factor for $L$ and $W$ of transistor instances to convert the unit into meter.                       | 1.0           |
|         | geounit_xy    | Scaling factor for $\$X$ and $\$Y$ of the transistor instances and resistors to convert the unit into meter. | 1.0e-6        |
|         | geounit_wl    | Scaling factor for $\$L$ and $\$W$ of resistors to convert the unit into meter.                              | 1.0e-6        |
| etsopt  | solver_preset | Accuracy setting for the thermal solver.                                                                     | mx            |

### ***Setting the values for geounit, geounit\_xy, and geounit\_wl***

Normally, the device dimensions in the DSPF file are expected to be provided in the following units:

| Parameters                             | Units |
|----------------------------------------|-------|
| $L, W$ for MOSFET devices              | m     |
| $\$X, \$Y$ for resistors and instances | um    |
| $\$L, \$W$ for resistors               | um    |

If the device geometries in the DSPF file are provided in the above units, using the default setting for `geounit`, `geounit_xy`, and `geounit_wl` is sufficient without any overrides for the default.

If the units in the DSPF file are different from the above, the default setting needs to be overwritten to convert the geometry values into the correct units. The following table lists a few scenarios of the geometry units in the DSPF file and the corresponding overrides for

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geounit, geounit\_xy, or geounit\_wl, that will convert the geometry values into the correct units:

| L, W Unit (instances) | \$X, \$Y unit (instances & resistors) | \$L, \$W unit (resistors) | geounit, geounit_xy, and geounit_wl setting |
|-----------------------|---------------------------------------|---------------------------|---------------------------------------------|
| m                     | um                                    | um                        | Use default setting                         |
| um                    | um                                    | um                        | geounit = 1.0e-6                            |
| m                     | nm                                    | um                        | geounit_xy = 1.0e-9                         |

## Thermal Technology File

The thermal technology file is defined by the `tech_file` keyword in the thermal configuration file. It contains the chip stackup and the corresponding thermal materials. The following is an example of the thermal technology file (`tech.txt`):

```
*Thermal_Layers
Substrate 804.5 (silicon 148 1658960)
Channel 0.33 (silicon 148 1658960)
poly_conn 0.10 (silicon 148 1658960) (oxide 12.4 2440000)
cont_poly 0.05 (copper 390 3439205) (oxide 2.4 440000)
cont_ndiff_conn 10 (copper 390 3439205) (oxide 2.4 440000)
cont_pdiff_conn 10 (copper 390 3439205) (oxide 2.4 440000)
metal1_conn 0.15 (copper 390 3439205) (oxide 2.4 440000)
Via1 0.03 (copper 390 3439205) (oxide 2.4 440000)
metal2_conn 0.15 (copper 390 3439205) (oxide 2.4 440000)
Via2 0.15 (copper 390 3439205) (oxide 2.4 2440000)
metal3_conn 0.40 (copper 390 3439205) (oxide 2.4 440000)
Via3 0.15 (copper 390 3439205) (oxide 2.4 440000)
metal4_conn 0.15 (copper 390 3439205) (oxide 2.4 440000)
Via4 0.30 (copper 390 3439205) (oxide 2.4 2440000)
metal5_conn 0.15 (copper 390 3439205) (oxide 2.4 440000)
```

The definition of each layer, such as the following line is:

```
poly_conn 0.10 (silicon 148 1658960) (oxide 12.4 2440000)
```

1. conductor layer name (name of the layer in which a device resides)
2. conductor layer thickness (um)
3. conductor layer material name

4. conductor layer thermal conductivity W / (m \* K)
5. conductor layer mass\_density \* specific\_heat kg/m3 \* J / (kg \* K)
6. dielectric layer name
7. dielectric layer thermal conductivity W / (m \* K)
8. dielectric layer mass\_density \* specific\_heat kg/m3 \* J / (kg\*K)

## Thermal Package File

The thermal package file is defined by the `package_file` keyword in the thermal configuration file. The thermal package file contains the thermal boundary conditions between the die and the ambient. The following is an example of a thermal package file with thermal boundary conditions specified:

```
CUSTOM_IC_THERMAL_SIMULATION_SETUP
TR_bottom 1
TR_top 1000
TR_left 530000
TR_right 530000
TR_back 200000
TR_front 200000
END_CUSTOM_IC_THERMAL_SIMULATION_SETUP
```

In this example, the heat flows vertically into the die attach since the sidewall thermal resistances are much higher than the die attach thermal resistance on the top and bottom. The file starts with the keyword, `CUSTOM_IC_THERMAL_SIMULATION_SETUP`, and ends with the keyword, `END_CUSTOM_IC_THERMAL_SIMULATION_SETUP`. Each line of the file contains a keyword and a thermal resistance value. The boundary conditions are expressed as thermal resistance connected between the ambient temperature and one of the six sides of the die. In addition to the six boundary conditions, additional parameters can be specified in the package file. The following table lists supported parameters and their descriptions:

---

| Parameter Name | Unit | Description                                            | Default Value |
|----------------|------|--------------------------------------------------------|---------------|
| TR_top         | C/W  | Thermal resistance between top surface and ambient.    | infinity      |
| TR_bottom      | C/W  | Thermal resistance between bottom surface and ambient. | infinity      |



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| Parameter Name | Unit | Description                                                         | Default Value |
|----------------|------|---------------------------------------------------------------------|---------------|
| TR_left        | C/W  | Thermal resistance between left surface and ambient.                | infinity      |
| TR_right       | C/W  | Thermal resistance between right surface and ambient.               | infinity      |
| TR_front       | C/W  | Thermal resistance between front surface and ambient.               | infinity      |
| TR_back        | C/W  | Thermal resistance between back surface and ambient.                | infinity      |
| TC_top         | J/C  | Thermal capacitance between top surface and ambient.                | 1e-12         |
| TC_bottom      | J/C  | Thermal capacitance between bottom surface and ambient.             | 1e-12         |
| TC_left        | J/C  | Thermal capacitance between left surface and ambient.               | 1e-12         |
| TC_right       | J/C  | Thermal capacitance between right surface and ambient.              | 1e-12         |
| TC_front       | J/C  | Thermal capacitance between front surface and ambient.              | 1e-12         |
| TC_back        | J/C  | Thermal capacitance between back surface and ambient.               | 1e-12         |
| Tamb_top       | C    | Ambient temperature for the top surface.                            | 0             |
| Tamb_bottom    | C    | Ambient temperature for the bottom surface.                         | 0             |
| Tamb_left      | C    | Ambient temperature for the left surface.                           | 0             |
| Tamb_right     | C    | Ambient temperature for the right surface.                          | 0             |
| Tamb_front     | C    | Ambient temperature for the front surface.                          | 0             |
| Tamb_back      | C    | Ambient temperature for the back surface.                           | 0             |
| NX             | None | Number of width grid elements on the die used for thermal modeling. | 20            |
| NY             | None | Number of depth grid elements on the die used for thermal modeling. | 20            |

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| Parameter Name    | Unit | Description                                                                                                                                                              | Default Value |
|-------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| NZ_Substrate      | None | Number of substrate thickness grid elements, not including the metal/via layers, on the die used for thermal modeling.                                                   | 5             |
| IGNORE_PARASITICS | None | Selection of approximation used for thermal modeling of heat sources due to parasitics.<br><br>0: No approximation<br><br>1: Ignore heat source due to parasitic devices | 0             |

### Trench Structure Support

Trench structures can be specified in the package file using the following syntax:

```
trench x0 y0 delta_x delta_y depth (trench material properties)
```

Here:

`trench` is the keyword to specify the trench structure

`x0` and `y0` are the coordinates of lower-left corner of the rectangular shape (the coordinates use DSPF coordinates as reference)

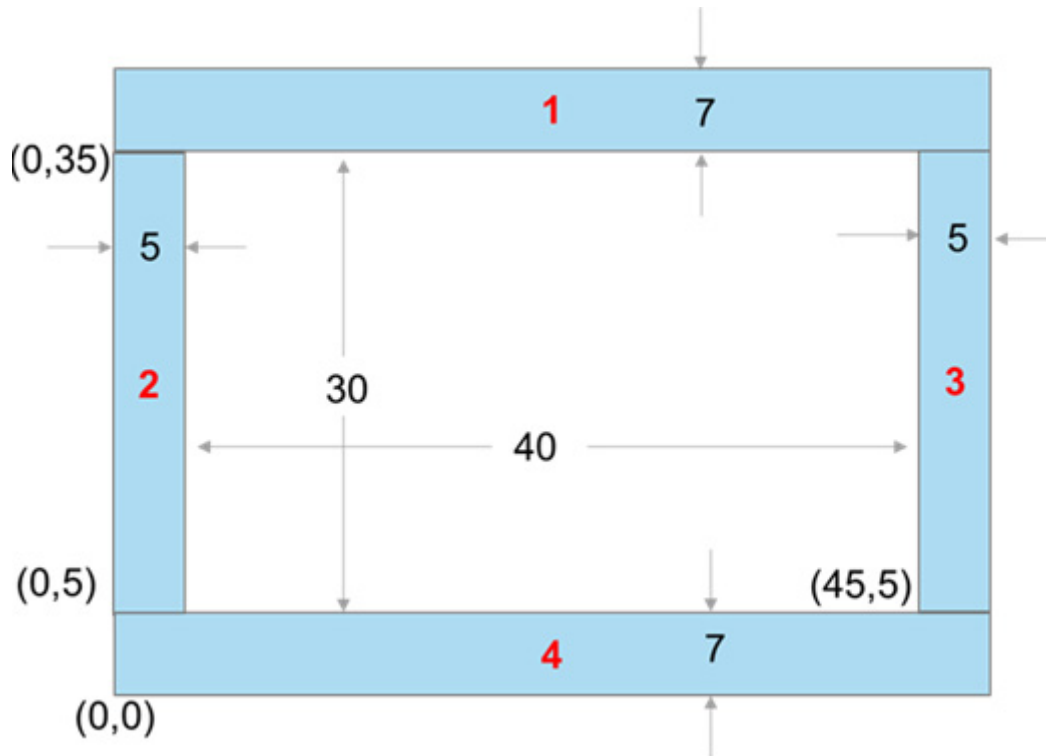
`delta_x` specifies the length of the trench in the X direction

`delta_y` specifies the length of the trench in the Y direction

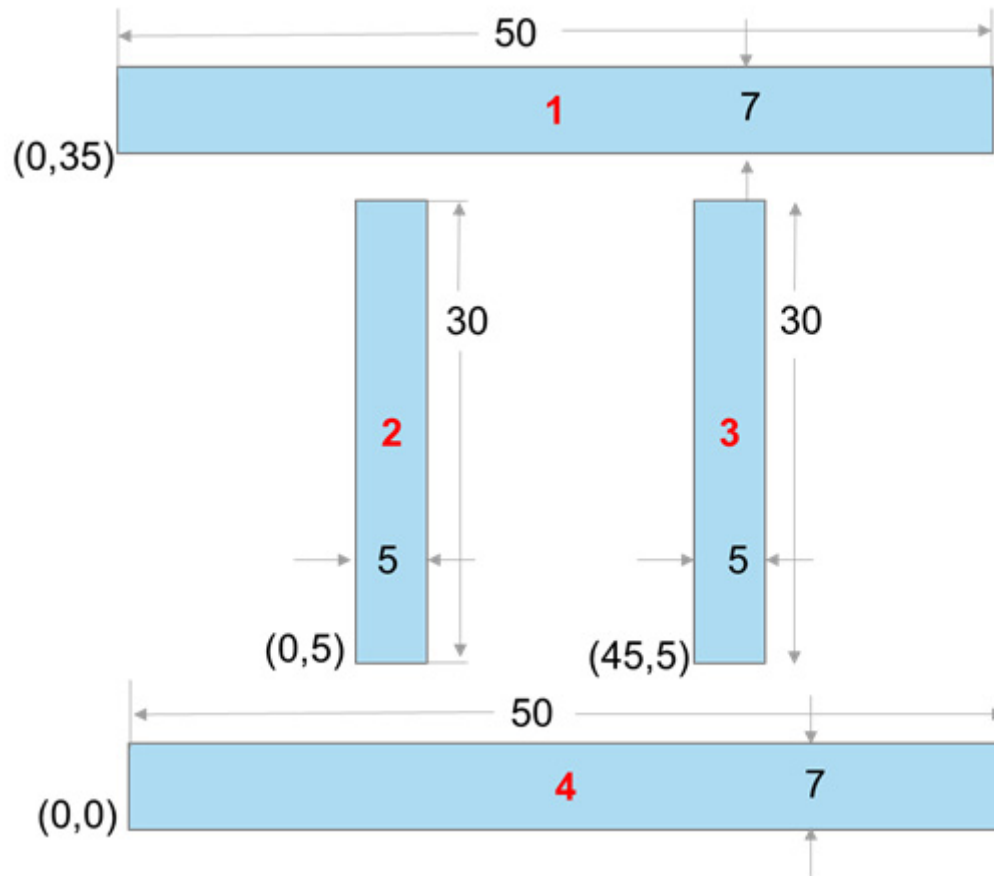
`depth` specifies the thickness of the trench

`trench material properties` specify the properties of the trench material, such as material name, thermal conductivity, mass density \* specific heat.

A trench structure is usually made up of several rectangular shaped pieces, each of which can be specified with the above syntax.



The above trench structure can be broken into the following rectangular pieces:



Given that the trench walls are 10um in depth, you can specify the trench structure in the package file, as shown below:

```
trench 0 35 50 7 10 (siliconoxide 148 1658960)
trench 0 5 5 30 10 (siliconoxide 148 1658960)
trench 45 5 5 30 10 (siliconoxide 148 1658960)
trench 0 0 50 7 10 (siliconoxide 148 1658960)
```

## Cauer and Foster Model Support in Package File

You can specify Cauer and Foster models for chip packages by using the `TOP_MODEL` or `BOTTOM_MODEL` parameter in the package file, as shown in the following example.

```
CUSTOM_IC_THERMAL_SIMULATION_SETUP
TOP_MODEL model_file.txt
NX 100
NY 100
NZ_Substrate 10
END_CUSTOM_IC_THERMAL_SIMULATION_SETUP
```

In the example above, the `TOP_MODEL` parameter specifies a file name `model_file.txt`, which in turn contains the Cauer or Foster model of the package, as shown below.

---

| Cauer Model                          | Foster Model                          |
|--------------------------------------|---------------------------------------|
| <code>.SUBCKT cauer_model 1 0</code> | <code>.SUBCKT foster_model 1 0</code> |
| <code>R0 1 2 100</code>              | <code>R0 1 2 100</code>               |
| <code>C0 1 0 0.0001</code>           | <code>C0 1 2 0.0135</code>            |
| <code>R1 2 3 200</code>              | <code>R1 2 3 200</code>               |
| <code>C1 2 0 0.0003</code>           | <code>C1 2 3 0.0135</code>            |
| <code>R2 3 4 250</code>              | <code>R2 3 4 250</code>               |
| <code>C2 3 0 0.0005</code>           | <code>C2 3 4 0.0135</code>            |
| <code>R3 4 5 300</code>              | <code>R3 4 5 300</code>               |
| <code>C3 4 0 0.0008</code>           | <code>C3 4 5 0.0135</code>            |
| <code>R4 5 0 150</code>              | <code>R4 5 0 150</code>               |
| <code>C4 5 0 0.001</code>            | <code>C4 5 0 0.0135</code>            |
| <code>.ENDS cauer_model</code>       | <code>.ENDS foster_model</code>       |

---

## Getting Started with Spectre Thermal Analysis

To perform Spectre thermal analysis, the first step is to prepare the simulation testbench including the postlayout data of the design, and the DSPF files with device location and dimension information for the transistors, resistors, diodes, and so on, in the instance section.

A `dspf_include` statement is required in the Spectre thermal analysis flow to identify the DSPF data.

```
dspf_include "sram.spf" (Spectre syntax)
.dspf_include "sram.spf" (SPICE syntax)
```

`dspf_include` provides special features for reading the DSPF format data, for example, port order adjustments, or handling of duplicated subcircuits. Do not use the `include/` `.include` commands to read the DSPF format data because these commands do not have the special functions of the `dspf_include/.dspf_include` command.

After setting up the testbench, you should perform a regular (non-electrothermal) postlayout simulation with the `spectre` command to ensure that the testbench contains no error, and the circuit behaves as expected.

```
% spectre +aps input.scs (Spectre test bench)
```

To perform electrothermal simulation on the same design, to add a reliability block containing the thermal analysis statement which defines the thermal configuration file (see [Technology Overview](#) on page 536) and invoke the Spectre command the same way as a regular postlayout simulation:

```
% spectre +aps input.scs (electrothermal analysis)
```

The electrothermal analysis is enabled by the presence of the `reliability` block. All electrothermal related options are defined either as options to the thermal analysis statement or in the thermal configuration file.

### Following the Progress of Spectre Steady-State Thermal Analysis

As the simulation runs, Spectre outputs messages to the screen and the simulation log file that shows the progress of the simulation and provides statistical information. The following sections describe the information that may be significant to you when using the steady-state thermal analysis flow.

#### ***Hardware Configuration and Run-Time Machine Loading***

At the beginning of a simulation session, Spectre prints the hardware configuration (physical memory, CPU core specification) and runtime machine status (available memory, CPU core operating frequency, CPU loading). When running electrothermal analysis on large designs, ensure there is sufficient memory available, with CPU operating at full speed (not in power saving mode), and the machine loading is light.

```
User: abc Host: xspeneh8c-1 HostID: 14AC0820 PID: 1920
Memory available: 88.2909 GB physical: 202.6861 GB
Linux : Red Hat Enterprise Linux Client release 5.8 (Tikanga)
```

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---

```
CPU Type: Intel(R) Xeon(R) CPU X5680 @ 3.33GHz
All processors running at 3333.6 MHz
Socket: Processors
0: 0, 1, 2, 3, 4, 5
1: 6, 7, 8, 9, 10, 11
System load averages (1min, 5min, 15min) : 7.8 %, 7.5 %, 9.3 %
```

## ***Reading the Thermal Configuration File***

Spectre reads the thermal configuration file before processing the circuit being analyzed. All valid options are reported in the following summary:

```
Reading THERMAL configuration file: ../thermal.conf
~~~~~
THERMAL Analysis Configuration
~~~~~
Thermal tech_file = "tech.txt"
Thermal package_file = "pkg.txt"
```

If one of the specified thermal configuration options is not displayed in the summary, check the related warnings and correct the syntax.

## ***Processing the DSPF Files***

Spectre processes the DSPF files and prepares a reduced circuit to be simulated if there are RC parasitics. This often includes identifying the power nets and reducing them to only include parasitic capacitors, as well as identifying the signal nets and reducing the parasitic resistors and capacitors according to accuracy requirement.

```
Time for Processing DSPF file: CPU = 9.31258 s, elapsed = 10.6095 s.
Time accumulated: CPU = 9.32858 s, elapsed = 10.6095 s.
Peak resident memory used = 320 Mbytes.
Time for Creating Parasitic Database: CPU = 3.62345 s, elapsed = 3.61969 s.
Time accumulated: CPU = 12.952 s, elapsed = 14.2293 s.
Peak resident memory used = 586 Mbytes.
```

## ***Running Electrical Simulation to Produce Device Power Values***

At this point, Spectre is ready to perform electrical simulation to produce device power values required for electrothermal simulation. This step is simply a regular circuit simulation, where Spectre first parses the circuit, reports circuit inventory, initiates a DC analysis, and finishes the step with a transient analysis.

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```


Transient Analysis `myThermal-000_runThermal-001_tran_thermal': time = (0 s -> 1
ns)

.....
.....9.....8.....7.....6.....5.....4.....3.....2.....1.....0
Number of accepted tran steps = 635
.....
Initial condition solution time: CPU = 1.32797 ks, elapsed = 670.625 s.
Intrinsic tran analysis time: CPU = 103.104 s, elapsed = 35.0529 s.
```

The resulting device power values are stored in a file with the extension `.thermal_rpt1` in the output directory, and used as an input for the subsequent thermal simulation.

This step of the electrothermal simulation is fully multi-threaded. It uses the number of cores specified using `+mt` on the Spectre command line.

### ***Calling Cadence® Thermal Extractor to Generate Thermal Model***

During the first iteration, Cadence® Thermal Extractor is invoked to build the thermal model of the structure being analyzed using the device location information extracted from the DSPF file and the material and boundary conditions defined in the thermal technology and package files. Spectre reports the chip bounding box information and the thermal package file content as the information is read into Cadence® Thermal Extractor, as well as the time spent building the thermal model:

```
Initializing data base for thermal solver of electrical-thermal co-simulation...
Die size in x, y and z direction: 7um 8um 101um
HTC value at right(xmax) bounadry: 2335.14W/m^2-K 530000K/W 40
HTC value at left(xmin) boundary: 2335.14W/m^2-K 530000K/W 40
HTC value at back(ymax) boundary: 2668.73W/m^2-K 530000K/W 40
HTC value at front(ymin) boundary: 2668.73W/m^2-K 530000K/W 40
HTC value at top surface of layer channel: 41528.2W/m^2-K 430000K/W 200
HTC value at bottom surface of layer substrate: 357143W/m^2-K 50000K/W 200
Wave3D engine finished normally.
Time for initiating and create thermal database: CPU = 149.8s (0h 2m 29s),
elapsed = 166.0s (0h 2m 46s).
```

This step of the electrothermal simulation is executed only once during the first iteration of the run. The resulting thermal model is reused for subsequent iterations of the thermal solver.



### ***Running Thermal Simulation to get the Temperature Rise on Devices***

Once the thermal model is built, Spectre performs thermal simulation using the thermal model generated by Cadence® Thermal Extractor:

```
Solving for temperature in electrical-thermal co-simulation...
Time for solving thermal: CPU = 3.6s (0h 0m 3s), elapsed = 3.6s (0h 0m 3s).
```

The resulting temperature rise on each device is then used to set the device temperature on each device for the next iteration of the electrothermal simulation.

At the end of each iteration, Spectre reports the runtime statistics, such as total and accumulated run times and memory usage. These are important measures when optimizing performance:

```
Total time required for tran analysis
`myThermal-000_runThermal-000_tran_thermal': CPU = 1.48324 ks (24m 43.2s),
elapsed = 879.193 s (14m 39.2s).
Time accumulated: CPU = 1.87758 ks (31m 17.6s), elapsed = 1.28742 ks (21m 27.4s).
Peak resident memory used = 13.2 Gbytes.
```

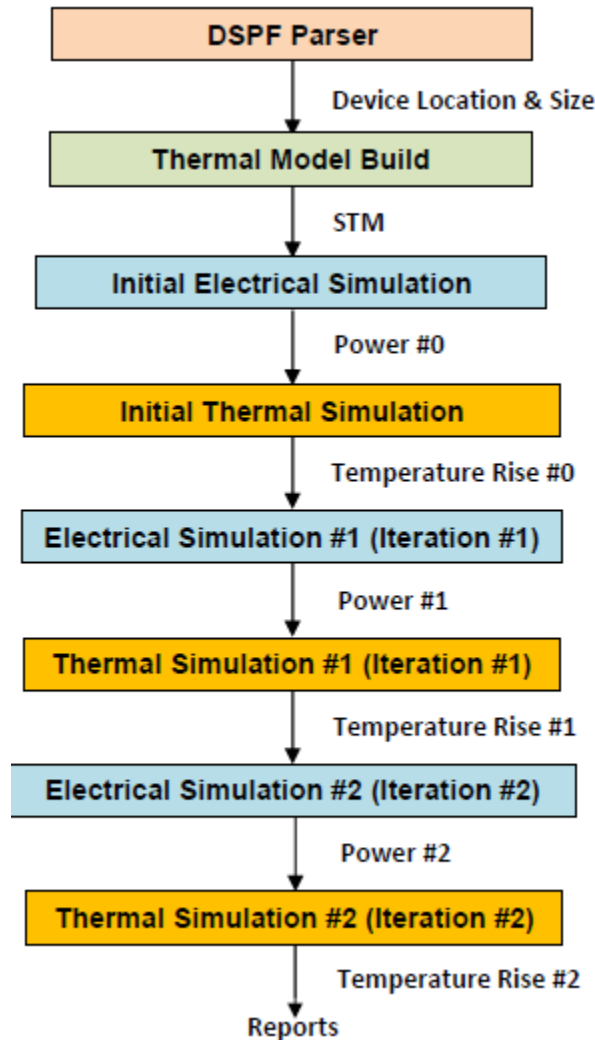
### **Spectre Steady-State Thermal Analysis Data Flow**

The following figure shows the flow of a two-iteration run of electrothermal simulation with the number of iterations defined in the thermal analysis options as `numiter=2`. Note that the number of iterations is defined as the number of electrothermal simulations after the initial

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round of simulation. Therefore, with `numiter=2`, the total number of both electrical and thermal simulations is three.



Three copies of thermal report are generated in the `raw` file directory, each corresponding to the result from one iteration, with the initial iteration number in the file name suffix being `0`.

### Spectre Steady-State Thermal Analysis Output Reports

Spectre thermal analysis generates a report file with the extension `.thermal_rpt` and the iteration count in the `raw` file directory after each iteration. It reports the temperature rise and

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power value on each device in the DSPF file. The last of these reports can be used as the final result of the electrothermal analysis. The following is a sample report that is generated:

## Table Legends:

Device : Name of Device.  
Trise (Cent): Temperature changes due to thermal analysis.  
Pwr (Watt): Average Power.  
Trise\_range(Cent): Minimum and Maximum of Trise.  
Pwr\_range (Watt): Minimum and Maximum of Power.  
Total\_Pwr : Sum of the Power for all of devices.  
Number\_of\_Devices: The number of devices display.  
Sorting : The order of devices are sorted by Trise or Pwr.

-----+

Trise\_range = [ 7.917030e+01 ~ 7.922372e+01 ]  
Pwr\_range = [ 1.261553e-15 ~ 2.110023e-04 ]  
Total\_Pwr = 3.394335e-03  
Number\_of\_Devices = 3094  
Sorting = Trise

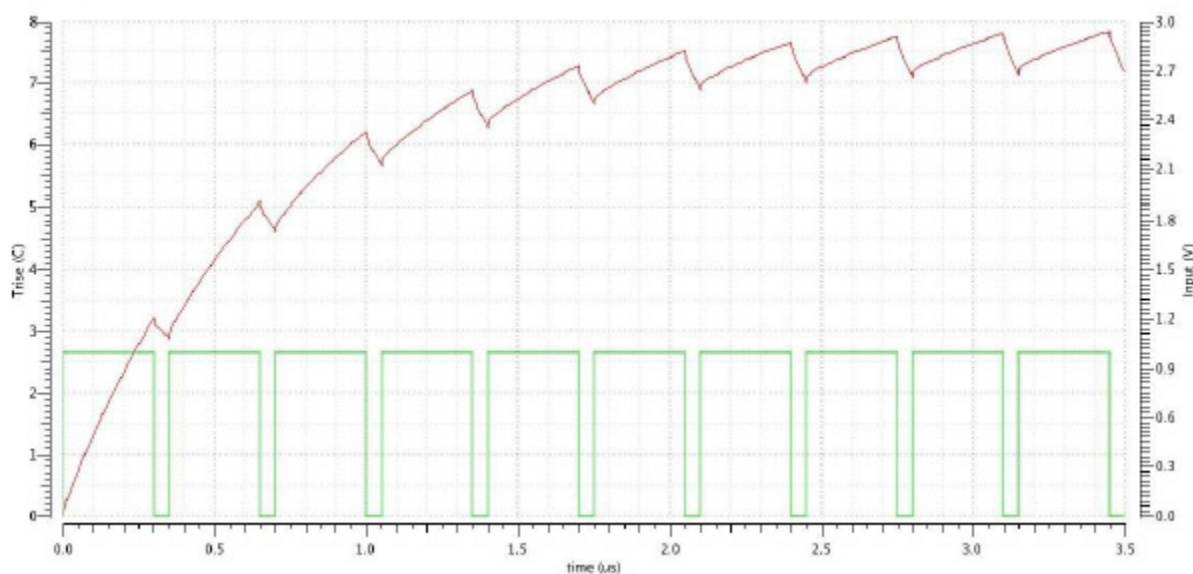
| Device           | Trise        | Pwr          |
|------------------|--------------|--------------|
| I0.MMN_cap@15.m1 | 7.922372e+01 | 4.719894e-13 |
| I0.MMN_cap@16.m1 | 7.922372e+01 | 4.719641e-13 |
| I0.MMN_cap@17.m1 | 7.922371e+01 | 5.043528e-13 |
| I0.MMP_out.m1    | 7.922292e+01 | 2.047078e-04 |
| I0.MMP_out@10.m1 | 7.922292e+01 | 2.047007e-04 |
| I0.MMP_out@11.m1 | 7.922292e+01 | 2.046164e-04 |
| I0.MMP_out@12.m1 | 7.922292e+01 | 2.047996e-04 |
| I0.MMP_out@13.m1 | 7.922292e+01 | 2.051595e-04 |
| I0.MMP_out@14.m1 | 7.922292e+01 | 2.059644e-04 |
| I0.MMP_out@7.m1  | 7.922292e+01 | 2.043795e-04 |
| I0.MMP_out@8.m1  | 7.922292e+01 | 2.044011e-04 |
| I0.MMP_out@9.m1  | 7.922292e+01 | 2.046469e-04 |
| I0.MMP_out@15.m1 | 7.922281e+01 | 2.110023e-04 |
| I0.MMN_cap.m1    | 7.922237e+01 | 4.719401e-13 |
| I0.MMN_cap@14.m1 | 7.922237e+01 | 4.719389e-13 |
| I0.rrpo413       | 7.922227e+01 | 9.889157e-20 |
| I0.rrpo885       | 7.922227e+01 | 2.679198e-15 |
| I0.rrpog_1_972   | 7.922227e+01 | 1.541470e-15 |
| I0.rrpo2090      | 7.922227e+01 | 1.286555e-14 |
| I0.rrpog_1_2145  | 7.922227e+01 | 1.286552e-15 |
| I0.rrpo2051      | 7.922222e+01 | 1.261556e-14 |
| I0.rrpog_1_2110  | 7.922222e+01 | 1.261553e-15 |
| I0.rrpo2050      | 7.922222e+01 | 2.543516e-14 |
| I0.rrpog_1_2109  | 7.922222e+01 | 2.543509e-15 |

.....

## Spectre Dynamic Thermal Analysis Output

With Spectre dynamic thermal analysis, the transient temperature waveforms on the designated instances are saved in a file in the `raw` file directory with the extension

`.temp_probe.tran.tran`. The instances for which the temperature waveforms are desired are defined with the `save_inst` option to the thermal analysis statement in the testbench. Along with the temperature waveform, the instantaneous power waveform of the designated instances is also saved in the same file. Without providing a list of instances with the `save_inst` option, no instance temperature and power waveforms are saved. However, Spectre always save the minimum or maximum instance temperature rise and the total power of the entire design in the `.temp_probe.tran.tran` file regardless of whether any instance is provided in the `save_inst` option. The following is a temperature waveform of a device in a design plotted along with the input signal waveform:



## Generating the Thermal Analysis Database and Plotting the Results

When you run the Spectre thermal analysis, a thermal analysis database is created that is similar to the simulation waveform data. The thermal database consists of the thermal database (`.tdb`) and temperature (`.temp_grid`) files. The Virtuoso ADE heat map viewer can read these `.tdb` and `.temp_grid` files to generate a thermal map of the thermal simulation results.

The following is the syntax to generate the thermal database file (`.tdb`):

```
rel reliability {
 mythermal thermal config=./thermal.conf method=<method>
 thermal_db_type=<type> thermal_data_format=<format> frame_freq=<value>
}
```

|                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                       |                     |
|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| <code>thermal_db_type</code>     | <p>Specifies the format for the thermal data output. When you select <code>binary</code>, the thermal database file is created in binary format. The binary thermal database file is used by the thermal plot tool.</p> <p>When you select <code>txt</code>, the thermal database file is created in both binary and text formats.</p> <p>Possible values are <code>binary</code> and <code>txt</code>.</p>                           | <code>binary</code> |
| <code>thermal_data_format</code> |                                                                                                                                                                                                                                                                                                                                                                                                                                       |                     |
|                                  | <p>Specifies the format for trise data output. When you select <code>binary</code>, the trise file is created in binary format. The binary trise file is used by the thermal plot tool.</p> <p>When you select <code>txt</code>, the trise file is generated in text format. The text format file is used by ADE for heatmap generation.</p> <p>Possible values are <code>none</code>, <code>binary</code>, and <code>txt</code>.</p> | <code>binary</code> |
| <code>frame_freq</code>          | Specifies the time step interval for the thermal rise data output. Specify 1 to save the thermal rise data output for all the times steps.                                                                                                                                                                                                                                                                                            | 3                   |

You can specify `save_channelonly=yes` to save the temperature of only the channel layer in the generated temperature file. By default, Spectre saves the temperature of all layers.

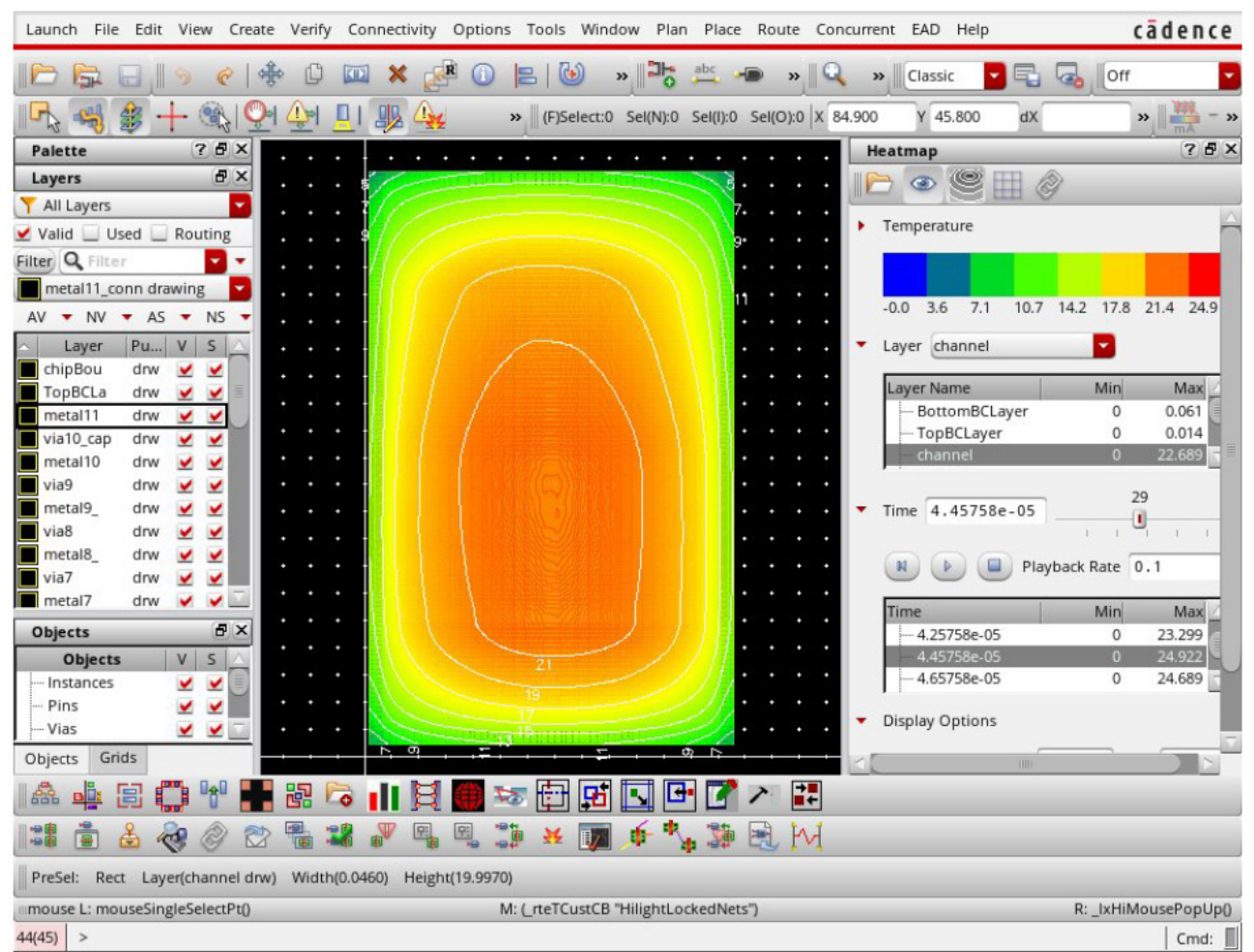
## Plotting the Thermal Map Results

The Virtuoso ADE thermal map viewer supports the following capabilities:

- Temperature distribution for each layer and layer switching
- Overlay of thermal map on top of device shapes and chip bounding box
- Zoom in and out to check the details or overview of the temperature distribution
- Isotherm lines
- Animation of dynamic analysis simulation result

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The ADE thermal map viewer enables you to view and interactively navigate through the thermal results.



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## Control Statements

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The Spectre<sup>®</sup> circuit simulator lets you place a sequence of control statements in the netlist. You can use the same control statement more than once. Different Spectre control statements are discussed throughout this manual. The following are control statements:

- [The alter and altergroup Statements on page 564](#)
- [The ic and nodeset Statements on page 566](#)
- [The info Statement on page 572](#)
- [The options Statement on page 583](#)
- [The paramset Statement on page 589](#)
- [The save Statement on page 591](#)
- [The print Statement on page 611](#)
- [The set Statement on page 612](#)
- [The shell Statement on page 613](#)
- [The statistics Statement on page 613](#)

## The alter and altergroup Statements

You modify individual parameters for devices, models, circuit, and subcircuit parameters during a simulation with the `alter` statement. The modifications apply to all analyses that follow the `alter` statement in your netlist until you request another parameter modification. You also use the `alter` statement to change the following `options` statement temperature parameters and scaling factors:

- `temp`
- `tnom`
- `scale`
- `scalem`

You can use the `altergroup` statement to respecify device, model, and circuit parameter statements that you want to change for subsequent analyses. You can also change subcircuits if you do not change the topology.

## Changing Parameter Values for Components

To change a parameter value for a component device or model, you specify the device or model name, the parameter name, and the new parameter value in the `alter` statement. You can modify only one parameter with each `alter` statement, but you can put any number of `alter` statements in a netlist. The following example demonstrates `alter` statement syntax:

```
SetMag alter dev=Vt1 param=mag value=1
```

- `SetMag` is the unique netlist name for this `alter` statement. (Like many Spectre statements, each `alter` statement must have a unique name.)
- The keyword `alter` is the primitive name for the `alter` statement.
- `dev=Vt1` identifies `Vt1` as the netlist name for the component statement you want to modify. You identify an instance statement with `dev` and a `model` statement with `mod`. When you use the `alter` statement to modify a circuit parameter, you leave both `dev` and `mod` unspecified.
- `param=mag` identifies `mag` as the parameter you are modifying. If you omit this parameter, the Spectre simulator uses the first parameter listed for each component in the Spectre online help as the default.
- `value=1` identifies `1` as the new value for the `mag` parameter. If you leave `value` unspecified, it is set to the default for the parameter.



## Changing Parameter Values for Models

To change a parameter value for model files with the `altergroup` statement, you list the device, model, and circuit parameter statements as you would in the main netlist. Within an alter group, each model is first defaulted and then the model parameters are updated. You cannot nest alter groups. You cannot change from a model to a model group and vice versa. The following example demonstrates `altergroup` statement syntax:

```
agl altergroup {
 parameters p1=1
 model myres resistor r1=1e3 af=p1
 model mybsim bsim3v3 lmax=p1 lmin=3.5e-7
}
```

The following example shows the full replacement of models using the `altergroup` statement:

```
ff_25 altergroup {
 include "../models/corner_ff"
}
```

For each model or device being altered, the parameters are first defaulted and then set to the new values. The parameter dependencies are updated and maintained.

You can include files into the alter group and can use the `simulator lang=spice` command to switch language mode. For more details on the `include` command, see the Spectre online help (`spectre -h include`). A model defined in the netlist has to have the same model name and primitive type (such as `bsim2`, `bsim3`, or `bjt`) in the alter group. For model groups, you can change the number of models in the group. You cannot change from a model to a model group and vice versa. For details on model groups, see the Spectre online help (`spectre -h bsim3v3`).

If you include a file containing multiple corners using `altergroup`, you can use the `+mp <numprocesses>` command-line option to distribute the simulation across multiple machines. Spectre automatically detects the farm environment (LSF, SGE, RTDA, or Network Computer) and distributes the simulation statements to the specified number of child processes. If a farm environment is not detected, Spectre uses the `fork` option to distribute the corner simulation by creating multiple jobs on a single system.

## Further Examples of Changing Component Parameter Values

This example changes the `is` parameter of a model named `SH3` to the value `1e-15`:

```
modify2 alter mod=SH3 param=is value=1e-15
```

The following examples show how to use the `param` default in an `alter` statement. The first parameter listed for resistors in the Spectre online help is the default. For resistors, this is the resistance parameter `r`.

Consequently, if `R1` is a resistor, the following two `alter` statements are equivalent:

```
change1 alter dev=R1 param=r value=50
change1 alter dev=R1 value=50
```

## Changing Parameter Values for Circuits

When you change a circuit parameter, you use the same syntax as when you change a device or model parameter except that you do not enter a `dev` or a `mod` parameter.

This example changes the ambient temperature to 0°C:

```
change2 alter param=temp value=0
```

The following table describes the circuit parameters you can change with the `alter` statement:

---

| Parameter           | Description                                              |
|---------------------|----------------------------------------------------------|
| <code>temp</code>   | Ambient temperature                                      |
| <code>tnom</code>   | Default measurement temperature for component parameters |
| <code>scalem</code> | Component model scaling factor                           |
| <code>scale</code>  | Component instance scaling factor                        |

---

**Note:** If you change `temp` or `tnom` using an `alter` statement, all expressions with `temp` or `tnom` are reevaluated.

## The `ic` and `nodeset` Statements

The Spectre simulator lets you provide state information to the DC and transient analyses. You can specify two kinds of state information:

### ■ Initial conditions

The `ic` statement lets you specify values for the starting point of a transient analysis. The values you can specify are voltages on nodes and capacitors, and currents on inductors.

### ■ Nodesets

Nodesets are estimates of the solution you provide for the DC or transient analyses. Unlike initial conditions, their values have no effect on the final results. Nodesets usually act only as aids in speeding convergence, but if a circuit has more than one solution, as with a latch, nodesets can bias the solution to the one closest to the nodeset values.

### Setting Initial Conditions for All Transient Analyses

You can specify initial conditions that apply to all transient analyses in a simulation or to a single transient analysis. The `ic` statement and the `ic` parameter described in this section set initial conditions for all transient analyses in the netlist. In general, you use the `ic` parameter of individual components to specify initial conditions for those components, and you use the `ic` statement to specify initial conditions for nodes. You can specify initial conditions for inductors with either method. Specifying `cmin` for a transient analysis does not satisfy the condition that a node has a capacitive path to ground.

**Note:** Do not confuse the `ic` parameter for individual components with the `ic` parameter of the transient analysis. The latter lets you select from among different initial conditions specifications for a given transient analysis.

### Specifying Initial Conditions for Components

You can specify initial conditions in the instance statements of capacitors, inductors, and windings for magnetic cores. The `ic` parameter specifies initial voltage values for capacitors and current values for inductors and windings. In the following example, the initial condition voltage on capacitor `Cap13` is set to two volts:

```
Cap13 11 9 capacitor c=10n ic=2
```

### Specifying Initial Conditions for Nodes

You use the `ic` statement to specify initial conditions for nodes or initial currents for inductors. The nodes can be inside a subcircuit or internal nodes to a component.

The following is the format for the `ic` statement:

```
ic signalName=value ...
```

The format for specifying signals with the `ic` statement is similar to that used by the `save` statement. This method is described in detail in [Saving Main Circuit Signals](#) on page 591. Consult this discussion if you need further clarification about the following example.

```
ic Voff=0 X3.7=2.5 M1:int_d=3.5 L1:1=1u
```

This example sets the following initial conditions:

- The voltage of node `Voff` is set to 0.
- Node 7 of subcircuit `X3` is set to 2.5 V.
- The internal drain node of component `M1` is set to 3.5 V. (See the following table for more information about specifying internal nodes.)
- The current for inductor `L1` is set to 1 $\mu$ .

Specifying initial node voltages requires some additional discussion. The following table tells you the internal voltages you can specify with different components.

| Component                     | Internal Node Specifications                                                      |
|-------------------------------|-----------------------------------------------------------------------------------|
| BJT                           | <code>int_c</code> , <code>int_b</code> , <code>int_e</code>                      |
| BSIM                          | <code>int_d</code> , <code>int_s</code>                                           |
| MOSFET                        | <code>int_d</code> , <code>int_s</code>                                           |
| GaAs MESFET                   | <code>int_d</code> , <code>int_s</code> , <code>int_g</code>                      |
| JFET                          | <code>int_d</code> , <code>int_s</code> , <code>int_g</code> , <code>int_b</code> |
| Winding for Magnetic Core     | <code>int_Rw</code>                                                               |
| Magnetic Core with Hysteresis | <code>flux</code>                                                                 |

## Supplying Solution Estimates to Increase Speed

You use the `nodeset` statement to supply estimates of solutions that aid convergence or bias the simulation towards a given solution. You can use nodesets for all DC and initial transient analysis solutions in the netlist. The `nodeset` statement has the following format:

```
nodeset signalName=value ...
```

Values you can supply with the `nodeset` statement include voltages on topological nodes, including internal nodes, and currents through voltage sources, inductors, switches, transformers, N-ports, and transmission lines.

The format for specifying signals with the `nodeset` statement is similar to that used by the `save` statement. This method is described in detail in [Saving Main Circuit Signals](#) on page 591. Consult this discussion if you need further clarification about the following example.

```
nodeset Voff=0 X3.7=2.5 M1:int_d=3.5 L1:l=1u
```

This example sets the following solution estimates:

- The voltage of node `voff` is set to 0.
- Node 7 of subcircuit X3 is set to 2.5 V.
- The internal drain node of component M1 is set to 3.5 V. (See the table in the [ic statements](#) section of this chapter for more information about specifying internal nodes.)
- The current for inductor `L1` is set to 1 $\mu$ .

### Specifying State Information for Individual Analyses

You can specify state information for individual analyses in two ways:

- You can use the `ic` parameter of the transient analysis to choose which previous specifications are used.
- You can create a state file that is read by an individual analysis.

### Choosing Which Initial Conditions Specifications Are Used for a Transient Analysis

The `ic` parameter in the transient analysis lets you select among several options for which initial conditions to use. You can choose the following settings:

---

| Parameter Setting | Action Taken                                                                                                                                                                 |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>dc</code>   | Initial conditions specifiers are ignored, and the existing DC solution is used.                                                                                             |
| <code>node</code> | The <code>ic</code> statements are used, and the <code>ic</code> parameter settings on the capacitors and inductors are ignored.                                             |
| <code>dev</code>  | The <code>ic</code> parameter settings on the capacitors and inductors are used, and the <code>ic</code> statements are ignored.                                             |
| <code>all</code>  | Both the <code>ic</code> statements and the <code>ic</code> parameters are used. If specifications conflict, <code>ic</code> parameters override <code>ic</code> statements. |

---

### Specifying State Information with State Files

You can also specify initial conditions and estimate solutions by creating a state file that is read by the appropriate analysis. You can create a state file in two ways:

- You can instruct the Spectre simulator to create a state file in a previous analysis for future use.

- You can create a state file manually in a text editor.

## Telling the Spectre Simulator to Create a State File

You can instruct the Spectre simulator to create a state file from either the initial point or the final point in an analysis. To write a state file from the initial point in an analysis, use the `write` parameter. To write a state file from the final point, use the `writefinal` parameter. Each of the following two examples writes a state file named `ua741.dc`. The first example writes the state file from the initial point in the DC sweep, and the second example writes the state file from the final point in the DC sweep.

```
Drift dc param=temp start=0 stop=50.0 step=1 readns="ua741.dc" write="ua741.dc"
Drift dc param=temp start=0 stop=50.0 step=1 readns="ua741.dc"
writefinal="ua741.dc"
```

## Creating a State File Manually

The syntax for creating a state file in a text editor is simple. Each line contains a signal name and a signal value. Anything after a pound sign (#) is ignored as a comment. The following is an example of a simple state file:

```
State file generated by Spectre from circuit file 'wilson'
during 'stepresponse' at 5:39:38 PM, jan 21, 1992.
1 .588793510612534
2 1.17406247989272
3 14.9900516233357
pwr 15
vcc:p -9.9483766642647e-06
```

## Reading State Files

To read a state file as an initial condition, use the `readic` transient analysis parameter. To read a state file as a nodeset, use the `readns` parameter. This example reads the file `intCond` as initial conditions:

```
DoTran_z12 tran start=0 stop=0.003 \
 step=0.00015 maxstep=6e-06 readic="intCond"
```

This second example reads the file `soluEst` as a nodeset.

```
DoTran_z12 tran start=0 stop=0.003 \
 step=0.00015 maxstep=6e-06 readns="soluEst"
```

## Special Uses for State Files

State files can be useful for the following reasons:

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- You can save state files and use them in later simulations. For example, you can save the solution at the final point of a transient analysis and then continue the analysis in a later simulation by using the state file as the starting point for another transient analysis.
- You can use state files to create automatic updates of initial conditions and nodesets.

The following example demonstrates the usefulness of state files:

```
altTemp alter param=temp value=0
Drift dc param=temp start=0 stop=50.0 step=1 readns="ua741.dc0" write="ua741.dc0"
XferVsTemp xf param=temp start=0 stop=50.0 step=1 load freq=1kHz
readns="ua741.dc0"
```

The first analysis computes the DC solution at T=0C, saves it to a file called `ua741.dc0`, and then sweeps the temperature to T=50C. The transfer function analysis (`xf`) resets the temperature to zero. Because of the temperature change, the DC solution must be recomputed. Without the use of state files, this computation might slow the simulation because the only available estimate of the DC solution would be that computed at T=50C, the final point in the DC sweep. However, by using a state file to preserve the initial DC solution at T=0C, you can enable the Spectre simulator to compute the new DC solution quickly. The computation is fast because the Spectre simulator can use the DC solution computed at T=0C to estimate the new solution. You can also make future simulations of this circuit start quickly by using the state file to estimate the DC solution. Even if you have altered a circuit, it is usually faster to start the DC analysis from a previous solution than to start from the beginning.

### Setting IC Priority Order

By default, if you specify an initial condition file with the `readic` parameter, initial conditions from the file are used, and the `ic` statements specified in the netlist are ignored. You can set the `options` statement parameter `icpriority` to `netlist`, (`icpriority=netlist`) to enable the simulator give precedence to the `ic` statements specified in the netlist. Similarly, if you specify the nodesets in a file using `readns`, and the `icpriority` parameter is set to `netlist`, then the nodeset statements in the netlist get higher priority.

Following is the order of precedence (from highest to lowest) when the `icpriority` parameter is set to `netlist`:

- `ic` statements in the netlist file
- `readic`
- `nodeset` statements specified in the netlist file
- `readns`

Following is the order of precedence (from highest to lowest) when the `icpriority` parameter is set to `file`:

- `readic`
- `ic` statements in the netlist file
- `readns`
- `nodeset` statements specified in the netlist file

## The info Statement

You can generate lists of component parameter values with the `info` statement. With this statement, you can access the values of input, output, and operating-point parameters and print the node capacitance table. These parameter types are defined as follows:

- **Input parameters**  
Input parameters are those you specify in the netlist, such as the given length of a MOSFET or the saturation current of a bipolar resistor.
- **Output parameters**  
Output parameters are those the simulator computes, such as temperature-dependent parameters and the effective length of a MOSFET after scaling.
- **Operating-point parameters**  
Operating-point parameters are those that depend on the operating point.
- **Node Capacitance Table**  
The node capacitance table displays the capacitance between the nodes of a circuit.



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You can also list the minimum and maximum values for the input, output, and operating-point parameters, along with the names of the components that have those values.

---

| Parameter Setting                  | Action Taken                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>what=oppooint</code>         | Prints the oppooint parameters. Other possible values are <code>none</code> , <code>inst</code> , <code>models</code> , <code>input</code> , <code>output</code> , <code>nodes</code> , <code>all</code> , <code>terminals</code> , <code>captab</code> , <code>parameters</code> , <code>primitives</code> , <code>subckts</code> , <code>assert</code> , <code>allparameters</code> , <code>netlist</code> , <code>options</code> , <code>dumpall</code> , <code>bridges</code> , <code>opens</code> , <code>allcaps</code> , <code>customreplace</code> , <code>custominsert</code> , <code>customopen</code> , <code>netcap</code> , and <code>moscap</code> . |
| <code>where=logfile</code>         | Prints the parameters to the logfile. Other possible values are <code>nowhere</code> , <code>screen</code> , <code>file</code> , and <code>rawfile</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>file="%C:r.info.what"</code> | File name when <code>where=file</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <code>save=all</code>              | Saves all signals to output. Other possible values are <code>lvl</code> , <code>allpub</code> , <code>lvlpub</code> , <code>selected</code> , and <code>none</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <code>nestlvl</code>               | Specifies levels of subcircuits to report. The default value is <code>infinity</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <code>extremes=yes</code>          | Prints minimum and maximum values. Other possible values are <code>no</code> and <code>only</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <code>title=test</code>            | Prints <code>test</code> as the title of the analysis in the output file.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

---

## Specifying the Parameters You Want to Save

You specify parameters you want to save with the `info` statement `what` parameter. You can give this parameter the following settings:

---

| Setting                    | Action                                                                                                                                                                                |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>none</code>          | Lists no parameters                                                                                                                                                                   |
| <code>inst</code>          | Lists input parameters for instances of all components                                                                                                                                |
| <code>models</code>        | Lists input parameters for models of all components                                                                                                                                   |
| <code>input</code>         | Lists input parameters for instances and models of all components                                                                                                                     |
| <code>output</code>        | Lists effective and temperature-dependent parameter values                                                                                                                            |
| <code>nodes</code>         | The output is a terminal-to-node map                                                                                                                                                  |
| <code>all</code>           | Lists input and output parameter values                                                                                                                                               |
| <code>oppoint</code>       | Lists operating-point parameters                                                                                                                                                      |
| <code>terminals</code>     | The output is a node-to-terminal mapping                                                                                                                                              |
| <code>captab</code>        | Prints node-to-node capacitance                                                                                                                                                       |
| <code>parameters</code>    | Lists top level circuit parameters and their values.                                                                                                                                  |
| <code>primitives</code>    | Lists model parameters, oppoint parameters, output parameters, instance parameters, region parameters, and terminal names of a primitive. No parameter values are printed.            |
| <code>subckts</code>       | Lists subcircuit parameters and terminal names.                                                                                                                                       |
| <code>allparameters</code> | Lists top level circuit and subcircuit parameters and their values.                                                                                                                   |
| <code>netcap</code>        | Prints the capacitance values per net. For each net, capacitance contribution from the extracted view (DSPF, SPEF), design capacitor, and MOSFET terminal capacitances are displayed. |
| <code>moscap</code>        | Prints the capacitance values per MOSFET.                                                                                                                                             |
| <code>allcap</code>        | Prints the netcap and moscap reports.                                                                                                                                                 |
| <code>bridges</code>       | Prints information about bridge faults.                                                                                                                                               |
| <code>opens</code>         | Prints information about open faults                                                                                                                                                  |
| <code>customreplace</code> | Prints information about custom replace faults                                                                                                                                        |
| <code>customopen</code>    | Prints information about custom open faults                                                                                                                                           |

| Setting                   | Action                                        |
|---------------------------|-----------------------------------------------|
| <code>custominsert</code> | Prints information about custom insert faults |

The difference between `moscap` and `oppoint` setting is in the junction capacitances for drain-bulk and source-bulk. `moscap` is used to calculate the capacitance of a single mosfet. A diagonal capacitor equals to the sum of all `moscap` capacitances connected to the terminal, so it includes junction capacitances. The following table shows how `moscap` is calculated in terms of `oppoint`:

| <code>moscap</code> | Expression by <code>oppoint</code> |
|---------------------|------------------------------------|
| <code>cdd</code>    | <code>cdd+cjd</code>               |
| <code>css</code>    | <code>css+cjs</code>               |
| <code>cbb</code>    | <code>cbb+cjd+cjs</code>           |
| <code>cdb</code>    | <code>cdb-cjd</code>               |
| <code>cbd</code>    | <code>cbd-cjd</code>               |
| <code>csb</code>    | <code>csb-cjs</code>               |
| <code>cbs</code>    | <code>cbs-cjs</code>               |

The `info` statement gives you some additional settings. You can use the `save` parameter of the `info` statement to specify groups of signals whose values you want to list. For more information about `save` parameter options, refer to [Saving Groups of Signals](#). Finally, you can generate a summary of maximum and minimum parameter values with the `extremes` option.

## Specifying the Output Destination

You can choose among several output destination options for the parameters you list with the `info` statement. With the `info` statement `where` parameter, you can

- Display the parameters on a screen
- Send the parameters to a log file, to the raw file, or to a file you create

When the `info` statement is called from a transient analysis or used inside of a sweep, the name of the `info` analysis is prepended by the parent analysis. If the `file` option is used to save the results, use the `%A` percent code (described in [Description of Spectre Predefined Percent Codes](#)) in the filename to prevent the file from being overwritten.

For example, the following `info` statement

```
tempSweep sweep param=temp start=27 stop=127 step=10 {dcl dc dcInfo info
what=oppooint where=file file="infodata.%A"}
```

produces

```
infodata.tempSweep-000_dcInfo
infodata.tempSweep-001_dcInfo
infodata.tempSweep-002_dcInfo
infodata.tempSweep-003_dcInfo
```

and so on...

### Examples of the `info` Statement

You format the `info` statement as follows:

```
StatementName info parameter=value
```

The following example tells the Spectre simulator to send the maximum and minimum input parameters for all models to a log file:

```
Inparams info what=models where=logfile extremes=only
```

For a complete description of the parameters available with the `info` statement, consult the lists of analysis and control statement parameters in the Spectre online help (`spectre -h`).

### Printing the Node Capacitance Table

The Spectre simulator allows you to print node capacitance to an output file. This can help you in identifying possible causes of circuit performance problems due to capacitive loading.

The capacitance between nodes  $x$  and  $y$  is defined as

$$C_{xy} = - \frac{\partial q_x}{\partial v_y}$$

where  $q_x$  is the sum of all charges in the terminal connected to node  $x$ , and  $v_y$  is the voltage at node  $y$ .

The total capacitance at node  $x$  is defined as

$$C_{xx} = \frac{\partial q_x}{\partial v_x}$$

where charge  $q_x$  and voltage  $v_x$  are at the same node  $x$ .

Use the `captab` analysis to display the capacitance between the nodes in your circuit. This is an option in the `info` statement. Here is an example of the `info` settings you would set to perform a `captab` analysis:

| Parameter Setting          | Action Taken                                                                                                                                                                                                                            |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>what=captab</code>   | Performs <code>captab</code> analysis. The default value is <code>oppoint</code> .                                                                                                                                                      |
| <code>where=logfile</code> | Prints the parameters to a logfile. Other possible values are <code>nowhere</code> , <code>screen</code> , and <code>file</code> . The value <code>rawfile</code> is not supported for node capacitance.                                |
| <code>title=captab</code>  | Prints <code>captab</code> as the title of the analysis in the output file.                                                                                                                                                             |
| <code>threshold=0</code>   | Specifies the threshold capacitance value. The nodes for which the total node capacitance is below the threshold value will not be printed in the output table.                                                                         |
| <code>detail=node</code>   | Prints the capacitance for only the specified node. Other possible values are<br><br><code>nodetoground</code> : Prints the capacitance only for node-to-ground.<br><br><code>nodetonode</code> : Prints the capacitance for all nodes. |
| <code>filter=rc</code>     | Filters the internal RC nodes and reports only the pre-layout nodes. Possible values are <code>rc</code> and <code>none</code> .                                                                                                        |
| <code>sort=name</code>     | Defines how to sort the node capacitance table. Possible values are <code>name</code> and <code>value</code> .                                                                                                                          |

For a complete list of `captab` parameters and values, consult the Spectre online help (`spectre -h`).

Use the `infotimes` option of the transient analysis when you bind the `captab` analysis to a transient analysis. This runs the `captab` analysis at specified time intervals. The syntax for the `infotimes` option is

```
infotimes=[x1, x2...]
```

where `x1` and `x2` are time points for which the `info` analysis should be performed. The following is an example of binding a `captab` analysis to a transient analysis.

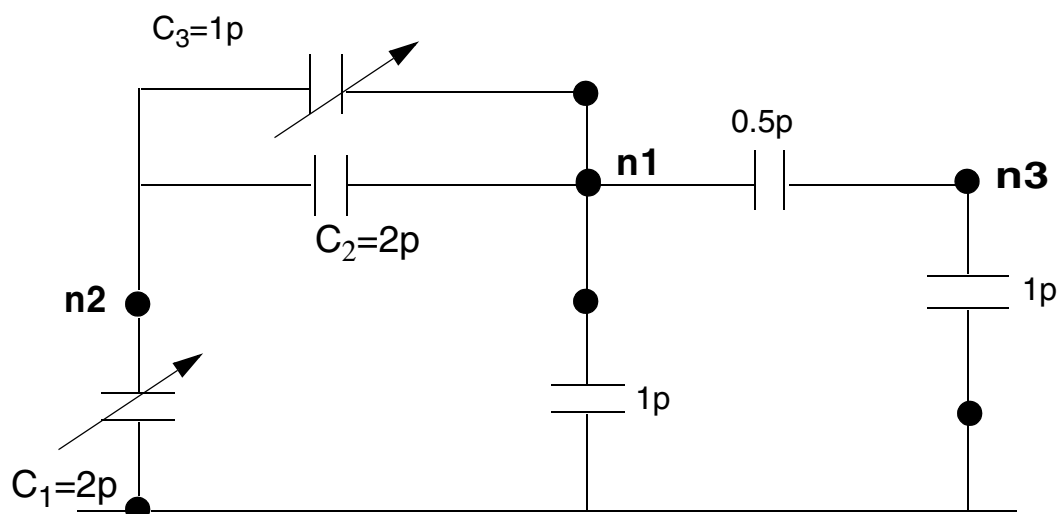
```
tran1 tran stop=1μ infotimes=[0.1μ 0.5μ] infoname=capInfo
capInfo info what=captab where=file file='capNodes'detail=nodetonode
```

## Output Table

The output for the captab analysis is printed in the following format:

- The first column displays the names of the two nodes (From\_node:To\_Node).
- The second column displays the fixed (linear) capacitance between the two nodes.
- The third column is the variable (non-linear) capacitance between the two nodes.
- The last column displays the total capacitance between the nodes.

**Table 12-1** Displays the output for the circuit below when `detail=nodetonode`:



In this circuit, the total capacitance at node 2 (n2:n2 in the table) is

$$C_1 + C_2 + C_3 = 5p$$

The total capacitance between node 2 and node 1 (n2:n1) is

$$C_2 (\text{Linear}) + C_3 (\text{Non-Linear}) = 3p$$

**Table 12-2 Node Capacitance Table Sorted by Value**

|       |            |             |          |
|-------|------------|-------------|----------|
| n2:n2 | Fixed=2p   | Variable=3p | Sum=5p   |
| n2:n1 | Fixed=2p   | Variable=1p | Sum=3p   |
| n1:n1 | Fixed=3.5p | Variable=1p | Sum=4.5p |
| n1:0  | Fixed=1p   | Variable=0  | Sum=1p   |
| n1:n2 | Fixed=2p   | Variable=1p | Sum=3p   |
| n1:n3 | Fixed=0.5p | Variable=0  | Sum=0.5p |
| n3:n3 | Fixed=1.5p | Variable=0  | Sum=1.5p |
| n3:0  | Fixed=1p   | Variable=0  | Sum=1p   |
| n3:n1 | Fixed=0.5p | Variable=0  | Sum=0.5p |

The total node capacitance at nodes 1, 2, and 3 is represented by the rows `n1:n1`, `n2:n2`, and `n3:n3` respectively.

There is no entry for `n3:n2`, which means there is no capacitance between these two nodes.

Table 7-1 is sorted by value. The rows are first grouped according to node names – the rows with the same `From_Node` are kept in a group. The row depicting the total capacitance at each node is always displayed first in the group, and the row displaying the node-to-ground capacitance is second. The remaining rows within each group are sorted in descending order of the `Sum` value.

**Note:** If the threshold is set to 2p (`thresh=2p`), the row `n1:n3` will not be printed because the capacitance between the nodes is less than the threshold. The row `n1:0` will be printed since the node-to-ground capacitance is always printed. The group `n3:n3`, `n3:0`, and `n3:n1` will not be printed because the total node capacitance at node 3 (`n3:n3`) is less than the threshold.

If you sort the table by name (`sort=name`), it would look as follows:

**Table 12-3 Node Capacitance Table Sorted by Name**

|       |            |             |          |
|-------|------------|-------------|----------|
| n1:n1 | Fixed=3.5p | Variable=1p | Sum=4.5p |
| n1:0  | Fixed=1p   | Variable=0  | Sum=1p   |

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|       |            |             |          |
|-------|------------|-------------|----------|
| n1:n2 | Fixed=2p   | Variable=1p | Sum=3p   |
| n1:n3 | Fixed=0.5p | Variable=0  | Sum=0.5p |
| n2:n2 | Fixed=2p   | Variable=3p | Sum=5p   |
| n2:0  | Fixed=0    | Variable=2p | Sum=2p   |
| n2:n1 | Fixed=2p   | Variable=1p | Sum=3p   |
| n3:n3 | Fixed=1.5p | Variable=0  | Sum=1.5p |
| n3:n0 | Fixed=1p   | Variable=0  | Sum=1p   |
| n3:n1 | Fixed=0.5p | Variable=0  | Sum=0.5p |

In this case, the `From_Node:To_Node` column is sorted alpha-numerically. However, the row depicting the total capacitance at each node is always displayed first in the group, and the row displaying the node-to-ground capacitance is second.

### Filtering RC Nodes Within an RC Net in XPS FastSPICE Mode

To filter the RC nodes and only report the pre-layout nodes, use the `filter=rc` option. For example:

```
simulator lang=spectre
capnode info what=captab where=file file="%C:r.info.captab" sort=value filter=rc
```

The above statement will generate the following:

```
XTOP.GPDWN : XTOP.GPDWN fixed=43.7231 f , variable=3.06673 f , sum=46.7898 f.
```

#### XPS

| Node Name           | Type | Value   | Unit |
|---------------------|------|---------|------|
| XTOP.GPDWN:13329855 | sum  | 2.64506 | f    |
| XTOP.GPDWN:13329857 | sum  | 2.33274 | f    |
| XTOP.GPDWN:13332058 | sum  | 1.75921 | f    |
| XTOP.GPDWN:13332698 | sum  | 2.18223 | f    |
| XTOP.GPDWN:13332699 | sum  | 1.92519 | f    |



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|                     |       |         |      |
|---------------------|-------|---------|------|
| XTOP.GPDWN:13808847 | sum   | 2.57183 | f    |
| XTOP.GPDWN:13811191 | sum   | 2.46744 | f    |
| -----               | ----- | ----    | ---- |
| -----               | ----- | ----    | ---- |
|                     | Total | 46.7898 | f    |

Here, the `fixed` value stands for the device/wire parasitic capacitance and the `variable` value stands for coupling and voltage-dependent capacitance.

The result of `captab` analysis includes all nodes and the output is located in `outdir` under `./XPS_result/top_netlist.info.captab`.

**Printing the Capacitance Values of Nets**

The Spectre simulator allows you to print the capacitance values for each net. For each net, capacitance contribution from extracted view (DSPF, SPEF), design capacitor, and MOSFET-terminal capacitances are shown. To do this, use the `netcap` analysis, as shown below.

```
info1 info what=netcap where=file file=netlist.info.netcap
```

Here, `netlist` is the name of the netlist.

The output of the `netcap` analysis is printed in the file `netlist.info.netcap` in `ascii` format. The following is an example:

Net Capacitance Table

| NetName  | NetType    | Cextracted | Cdesign | Cestimated | Cinterconnect | Cdrain | Cgate    | Csource | Cbulk | Ctotal    |
|----------|------------|------------|---------|------------|---------------|--------|----------|---------|-------|-----------|
| net89    | schematic  | 0          | 0       | 0          | 0             | 52.19f | 0        | 0       | 0     | 52.19f    |
| net90    | mixed      | 0          | 0       | 0          | 0             | 92.51f | 0        | 0       | 0     | 92.51f    |
| I0.SIDDQ | postlayout | 47.9422f   | 0       | 0          | 47.9422f      | 0      | 434.497f | 0       | 0     | 482.4392f |
| ----     |            |            |         |            |               |        |          |         |       |           |
| ----     |            |            |         |            |               |        |          |         |       |           |

In the table:

- `NetType` is the type of net. `schematic` means that the net exists only in the design (pre-layout). `postlayout` means that the net exists only inside the extracted view (DSPF). `mixed` means that the net exists in both pre-layout and postlayout.
- `Cextracted` is the capacitance contribution from the extracted view (DSPF, SPEF).

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- `Cdesign` is the capacitance contribution from the design (pre-layout) capacitors.
- `Cestimated` is the capacitance contribution from capacitors with special formats.
- `Cinterconnect` is the sum of `Cextracted`, `Cdesign` and `Cestimated`.
- `Cdrain` is the capacitance contribution from the MOSFET drain.
- `Cgate` is the capacitance contribution from the MOSFET gate.
- `Csource` is the capacitance contribution from the MOSFET source.
- `Cbulk` is the capacitance contribution from the MOSFET bulk.
- `Ctotal` is the sum of `Cinterconnect`, `Cdrain`, `Cgate`, `Csource`, and `Cbulk`.

## Printing the Terminal Capacitance Values of MOSFETs

You can also print the terminal capacitance values for MOSFETs. To do this, use the `moscap` analysis, as shown below.

```
info1 info what=moscap where=file file=<netlist>.info.moscap
```

Here, `netlist` is the name of the netlist.

The output of the `moscap` analysis is printed in the file `<netlist>.info.moscap` in ascii format. The following is an example:

| Device Instance | Device Location | cdd          | cdg          | cds          | cdb          | cgd          | cgg          | cgs          | cgb          | csd          |
|-----------------|-----------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| I1.MC4          | postlayout      | 4.22609e-13  | -1.80386e-13 | -1.84819e-13 | -5.74042e-14 | -1.76082e-13 | 3.61447e-13  | -1.83272e-13 | -2.09200e-15 | -3.19123e-13 |
| I1.MC4@1        | postlayout      | 5.57294e-13  | -1.80380e-13 | -3.19448e-13 | -5.74659e-14 | -1.83277e-13 | 3.61434e-13  | -1.76062e-13 | -2.09537e-15 | -1.84945e-13 |
| I33.PM13        | schematic       | 3.63888e-13  | -1.54401e-13 | -1.54162e-13 | -5.53258e-14 | -1.64203e-13 | -1.43472e-13 | -1.43472e-13 | -2.37197e-15 | -2.72274e-13 |
| csg             | css             | csb          | cbd          | cbg          | cbs          | cbb          |              |              |              |              |
| -1.80386e-13    | 5.56913e-13     | -5.74042e-14 | 7.25957e-14  | -6.73838e-16 | -1.88822e-13 | 1.16900e-13  |              |              |              |              |
| -1.80380e-13    | 4.22791e-13     | -5.74659e-14 | -1.89072e-13 | -6.73683e-16 | 7.27184e-14  | 1.17027e-13  |              |              |              |              |
| -1.54401e-13    | 4.93469e-13     | -6.67947e-14 | 7.25894e-14  | -1.24624e-15 | -1.95836e-13 | 1.24492e-13  |              |              |              |              |

In the table:

- Device Location shows whether the MOSFET exists in postlayout (DSPF) or schematic (pre-layout)
- Four terminals of MOSFET allows 16 capacitors.

## The options Statement

To enter initial parameters for your simulation that you do not specify in your environment variables or on your command line, you use the `options` statement. You can control parameters in a number of areas with the `options` statement:

- Parameters that specify tolerances for accuracy
- Parameters that control temperature
- Parameters that select output data
- Parameters that help solve convergence difficulties
- Parameters that control error handling and annotation
- Parameters that control method of threshold voltage (`vth`) computation for MOS device. For BSIM3v3, BSIM4, PSP102 PSP103, and BSIMCMG. Spectre supports `vth` from model equation (`std`) or constant current `vth` (`vthcc`). Otherwise, Spectre only supports 'std' computation.
- Parameters that specify the process options including `tnom`, `scale`, and `scalem`. When these process parameters are specified in a subcircuit in the MTS mode, they are locally scoped to that subcircuit only.

For a complete list of the parameters you can set with the `options` statement, consult the Spectre online help (`spectre -h`).

### options Statement Format

The `options` statement format is

```
Name options parameter=value ...
```

where

*Name*

The unique name you give to the `options` statement. The Spectre simulator uses this name to identify this statement in error or annotation messages

*options*

Primitive name for this control statement.

*Parameter=value*

Value you choose for the parameter. You can enter any number of parameter specifications with a single `options` statement.

## options Statement Example

```
Examp options rawfmt=psfbin audit=brief temp=30 \
 save=lvlpub nestlvl=3 rawfile=%C:r.raw useprobes=no
```

The example sets the `rawfmt`, `audit`, `temp`, `save`, `nestlvl`, `rawfile`, and `useprobes` parameters for an `options` statement named `Examp`. The backslash (\) at the end of the first line is a line continuation character. Nonnumerical parameter values are chosen from the possible values listed in the Spectre online help (`spectre -h`).

## Performing Parasitic Reduction

You can use the `parasitics` option or the `+parasitics` command-line option to set the parasitics for RC reduction globally, as shown below.

```
Opt options parasitics=on
```

or

```
spectre +aps +parasitics input.scs
```

If you specify both the `parasitics` option and the `+parasitics` command-line option, the `+parasitics` command-line option takes higher precedence.

You can also perform parasitic reduction of instances and subcircuits with the scope specified for MTS. For example:

```
Opt options parasitics=off
Opt1 options parasitics=on inst=[x1]
Opt2 options parasitics=on subckt=[subckt1]
```

In the above example, parasitic RC reduction is disabled globally, however, parasitic RC reduction is performed for subcircuit instance `x1` and subcircuit `subckt1`. So, if there are three subcircuit instances in the netlist, for example, `x1`, `x2`, and `x3`, and the following is specified, the parasitics RC reduction takes effect on `x1`, and not on `x2` and `x3`:

```
Opt options parasitics=on inst=[x1]
```

In the following example, parasitic RC reduction is performed globally, however, it is not performed for the subcircuit instance `x1` and subcircuit `sub1`:

```
opt1 options parasitics=on
opt2 options parasitics=off inst=[x1]
opt2 options parasitics=off sub=sub1
```

To perform parasitic reduction of instances and subcircuits with the scope specified for MTS, you need to specify `+mts` at the command line, as shown below.

```
% spectre +aps +mts....
```

When the above is specified, and you also use the `+parasitics` command-line option, the `parasitics` option takes higher precedence over the `+parasitics` command-line option. However, if `parasitics` is specified as a global option, then the `+parasitics` command-line option has the higher priority.

## Setting Tolerances

You need to set tolerances if the Spectre simulator's default settings do not suit your needs. This section tells you how to make the needed adjustments. If you need to examine default tolerances for any Spectre parameters, you can find them in the Spectre online help (`spectre -h`).

### Setting Tolerances with the options Statement

The following `options` statement parameters control error tolerances:

|                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>reltol</code>                           | One of the Spectre simulator's convergence criteria is that the difference between solutions in the last two iterations for a given time must be sufficiently small. With <code>reltol</code> , you set the maximum relative tolerance for values computed in the last two iterations. The default for <code>reltol</code> is 0.001.                                                                                                    |
| <code>iabstol</code> and <code>vabstol</code> | These parameters set absolute, as opposed to relative, tolerances for differences in the computed values of voltages and currents in the last two iterations. These parameter values are added to the tolerances specified by <code>reltol</code> . They let the Spectre simulator converge when the differences accepted by <code>reltol</code> approach zero. You can also set these values with the <code>quantity</code> statement. |

## Specifying Hierarchical Delimiters

You can use the `hier_delimiter` option to specify a hierarchical delimiter to represent the nodes inside a subcircuit hierarchy in your netlist. If you do not specify the `hier_delimiter` option, `.` is taken as the default hierarchical delimiter. The following is the syntax to specify the `hier_delimiter` option:

### Spectre Syntax

```
Opt options hier_delimiter="%"
```

### SPICE Syntax

```
.option hier_delimiter="%"
```

To specify " or \ as the hierarchical delimiter, the Escape symbol is required if you use double quotes (for example, `hier_delimiter="\ \"`).

**Note:** The `hier_delimiter` option has to be set as the first line in the top-level input netlist file.

### Additional options Statement Settings You Might Need to Adjust

This section provides some explanation of commonly used `options` statement parameters. It is not a complete listing of `options` statement parameters. For a complete list, consult the Spectre online help (`spectre -h`).

|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>tempeffects</code> | <p>This parameter defines how temperature affects the built-in primitive components. It takes the following three values:</p> <p><code>vt</code>—Only the thermal voltage <math>V_t = \frac{kT}{q}</math> is allowed to vary with temperature.</p> <p><code>tc</code>—The component temperature coefficient parameters (parameters that start with <code>tc</code>, such as <code>tc1</code>, and <code>tc2</code>) are active as well as the thermal voltage. You use this setting when you want to disable the temperature effects for nonlinear devices.</p> <p><code>all</code>—All built-in temperature models are enabled.</p> |
| <code>compatible</code>  | <p>This parameter changes some of the device models to be more consistent with the models in other simulators. See the <code>options</code> statement parameter listings in the Spectre online help (<code>spectre -h</code>) for more information.</p>                                                                                                                                                                                                                                                                                                                                                                              |

### Simulation Config file Support

Spectre supports simulation configuration file (`spectre.cfg`) that can be loaded to set the default options for the simulator.

This file is located and read from the following locations:

1. From the installation directory `<install_dir>/spectre/etc/configs`. This file is always read.

2. From the path specified using the `+config` command-line option. This file is always read. If you specify multiple files using the `+config` command-line option, all files are read by Spectre.
3. From one of the following locations, in the given order of precedence:
  - ☐ CSF search path, if `csfLookUpConfig` is specified

**Note:** You can use the `-csf` command-line option to disable the CSF mechanism.

  - ☐ Working directory
  - ☐ Home directory

**Note:** For example, if a config file is located in the CSF search path, working directory, and home directory, Spectre will only read the config file from CSF and ignore the config files located in the home and working directories.

Therefore, if a configuration file exists at all the above locations, Spectre will read at least three configuration files.

## Computing the Constant Current

Spectre supports the following options to compute the constant current ( $V_{th}$ ):

| Option Name              | Description                                                                                                                                                                                                                                           | Default Value      |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| <code>ivthn</code>       | NMOS $V_{th}$ current parameter                                                                                                                                                                                                                       | 0.0A               |
| <code>ivthp</code>       | PMOS $V_{th}$ current parameter                                                                                                                                                                                                                       | 0.0A               |
| <code>ivthw</code>       | Width offset for the constant current $V_{th}$                                                                                                                                                                                                        | 0.0m               |
| <code>ivthl</code>       | Length offset for the constant current $V_{th}$                                                                                                                                                                                                       | 0.0m               |
| <code>ivth_vdsmin</code> | The minimum $V_{ds}$ in constant current $V_{th}$ calculation                                                                                                                                                                                         | 0.05V              |
| <code>vthmod</code>      | $V_{th}$ output selector. This option is used to switch the output of the $V_{th}$ between the model equation $V_{th}$ and constant current $V_{th}$ definitions. This is an enum with two possible values, <code>std</code> and <code>vthcc</code> . | <code>vthcc</code> |

The following model parameters are added to the models that support constant current threshold ( $V_{th}$ ) calculation:

| Parameter Name           | Description                                                                                                                                            |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>ivth</code>        | $V_{th}$ current parameter. The default value is taken from the options <code>ivthn</code> or <code>ivthp</code> , depending on the type of the model. |
| <code>ivthw</code>       | Width offset for the constant current $V_{th}$                                                                                                         |
| <code>ivthl</code>       | Length offset for the constant current $V_{th}$                                                                                                        |
| <code>ivth_vdsmin</code> | The minimum $V_{ds}$ in constant current $V_{th}$ calculation                                                                                          |
| <code>vthmod</code>      | $V_{th}$ output selector                                                                                                                               |

**Note:** The model parameters have higher priority over the options. The options are used as default values for the model parameters. It is recommended not to use the constant current  $V_{th}$  method because it may impact simulation performance.

### Computing the Drain Saturation Voltage Based on Output Conductance

Spectre supports the following options to compute the drain saturation voltage ( $V_{dsat}$ ) based on output conductance ( $g_{ds}$ ):

| Option Name            | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Default Value |
|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| <code>vdsatmod</code>  | $V_{dsat}$ output selector. Possible values are: <code>std</code> , <code>gds</code> , <code>std</code> and <code>slow_gds</code> .<br><br>When <code>vdsatmod=std</code> , $v_{dsat}$ outputs SPICE model $v_{dsat}$ . When <code>vdsatmod=gds</code> , $g_{ds}$ -based $v_{dsat}$ is output. When <code>vdsatmod=slow_gds</code> , $v_{dsat}$ outputs an accurate $g_{ds}$ -based $v_{dsat}$ . However, it can be slow and is not recommended for dc sweep or transient analysis. |               |
| <code>vdsat_c</code>   | Coefficient for $V_{dsat}$ . The value of <code>vdsat_c</code> should be greater than 0. This option is used by both PMOS and NMOS.                                                                                                                                                                                                                                                                                                                                                 | 0.08          |
| <code>vdsat_vdl</code> | $V_{ds}$ coefficient for $V_{dsat}$ . The value of <code>vdsat_vdl</code> should be greater than 0. This option is used by both PMOS and NMOS.                                                                                                                                                                                                                                                                                                                                      | 0.3           |



`vdsat_vadj` Vds adjustment for vdsat. The value of `vdsat_vdaj` 0.0 should be greater than or equal to 0. This option is used by both PMOS and NMOS.

The following model parameters are added to the BSIMIMG and BSIMCMG models that support drain saturation voltage calculation:

| Parameter Name          | Description                                          |
|-------------------------|------------------------------------------------------|
| <code>vdsat_c</code>    | Coefficient for Vdsat. The default value is 0.8.     |
| <code>vdsat_vdl</code>  | Vds coefficient for Vdsat. The default value is 0.3. |
| <code>vdsat_vadj</code> | Vds adjustment for Vdsat. The default value is 0.0.  |

**Note:** The model parameters have higher priority over the options.

## The paramset Statement

For the `sweep` analysis only, the `paramset` statement allows you to specify a list of parameters and their values. This can be referred by a `sweep` analysis to sweep the set of parameters over the values specified. For each iteration of the sweep, the netlist parameters are set to the values specified by a row. The values have to be numbers, and the parameters' names have to be defined in the input file (netlist) before they are used. The `paramset` statement is allowed only in the top level of the input file.

The syntax is

```
Name paramset {
 list of netlist parameters
 list of values foreach netlist parameter
 list of values foreach netlist parameter ...
}
```

Here is an example of the `paramset` statement:

```
parameters p1=1 p2=2 p3=3
data paramset {
 p1 p2 p3
 5 5 5
 4 3 2
}
```

The `paramset` statement also supports subcircuit parameters, as shown in the following example:

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---

```
inline subckt rmod (g d s b)
parameters pert_fms=1 rx=1
rmod(d s) res
model res resistor l=100+pert_fms w=200+temp r=pert_fms+rx
ends

subckt rSubS A Y supply gnd
rp(Y A supply supply) rmod
rn(Y A gnd gnd) rmod rx=2
ends

XS (in output supply 0) rSubS
dataSub paramset {
 XS.rn:pert_fms XS.rn:rx
 3 514
 13 503
}
```

You can also specify the time, triggered by an event in the `paramset` statement, as shown below.

```
paramSet1 paramset {
 time temp reltol
 @(assert_1 0) 125 1e-3
}
```

The above statement means that whenever an event specified by the `assert_1` happens, the temperature should be set to 125 and the value of `reltol` should be set to `1e-3`.

Combining the `paramset` statement with the `sweep` analysis allows you to sweep multiple parameters simultaneously; for example, power supply voltage and temperature.

## The save Statement

You can save signals for individual nodes and components or save groups of signals.

### Saving Signals for Individual Nodes and Components

You can include signals for individual nodes and components in the save list by placing `save` statements (not to be confused with the `save` parameter) in your netlist. When you specify signals in a `save` statement, the Spectre simulator sends these signals to the output raw file, as long as the `nestlvl` setting does not filter them.

**Note:** When multiple `save` statements are specified in the netlist file, they are executed in the order they appear in the netlist.

In this section, you will learn how to save the following:

- Voltages for individual nodes
- Charge on a node
- All signals for an individual component
- Selected signals for an individual component
- Parameters of Stacked-FET

The syntax for the `save` statement varies slightly, depending on whether the requested data is from the main circuit or a subcircuit.

### Saving Main Circuit Signals

The `save` statement general syntax has the following arguments. You can specify more than one argument with a single `save` statement, and you can mix the types of arguments in a single statement.

```
save signalName...
save signalName:q | dynamic
save compName...
save compName:modifier...
save subcircuitName:terminalIndex...
```

- *signalName* is generally the netlist name of a node whose voltage you want to save. If the specified node name is not unique (an instance in the netlist has the same name), the Spectre circuit simulator saves the node. If the signal name is specified with the modifier *q* or *dynamic*, it saves the charge on the node instead of the voltage. For

example `save 7:q` or `save 7:dynamic` saves the charge for the node named 7. Wildcards are supported in node names. For example, `save *:q`.

- *compName* is the netlist name of a component whose signals you want to save. Wildcards are supported in component names.
- *modifier* specifies signals you want to save for a particular component. It can have the following types of values:

- A terminal name

Terminal names for components are the names for nodes in component instance definitions. You can find instance definitions for each component in the component parameter listings in the Spectre online help (`spectre -h`). For example, the following is the instance definition of a microstrip line. The terminal names are `t1`, `b1`, `t2`, and `b2`. Wildcards are supported.

```
Name t1 b1 t2 b2 msline parameter=value...
```

- A terminal index

The terminal index is a number that indicates where a terminal is in the instance definition. You give the first terminal a terminal index of 1, the second a terminal index of 2, and so on. In this example, the terminal indexes are 1 for `sink` and 2 for `src`.

```
Name sink src isource parameter=value...
```

- A name of an operating-point parameter (from the lists of parameters for each component in the Spectre online help). Wildcards are supported.
- The name of a Verilog<sup>®</sup>-A internal variable.
- One of the following keywords:

|                           |                                                              |
|---------------------------|--------------------------------------------------------------|
| <code>currents</code>     | To save all currents of the device                           |
| <code>static</code>       | To save resistive currents of the device                     |
| <code>displacement</code> | To save capacitive currents of the device                    |
| <code>dynamic</code>      | To save charge or flux of the device                         |
| <code>oppoint</code>      | To save the operating points of the device                   |
| <code>probe</code>        | To measure current of the device with a probe                |
| <code>pwr</code>          | To save power dissipated on a circuit, subcircuit, or device |
| <code>total_pwr</code>    | To save the total power of all the devices.                  |

`all`                      To save all signals of the device

- *subcircuitName* is the instance name of a subcircuit call. Saving terminal currents for subcircuit calls is the same as saving terminal currents for other instance statements except that you must identify individual terminal currents you want to save by the terminal index.

**Note:** To save all terminal currents for subcircuit calls, you use a `save` statement or specify the `subcktprobelv1` parameter in an `options` statement. The `currents=all` option of the `options` statement saves currents only for devices.

**Saving Subcircuit Signals**

To save a subcircuit,

- Give a full path to the subcircuit name. Start with the highest level subcircuit and identify the signals you want to save at the end of the path. Separate each name with a period.

**Examples of the save Statement**

The following table shows you examples of `save` statement syntax. When you specify node names, the Spectre simulator saves node voltages. Currents are identified by the terminal node name or the index number.

**Exception:** Currents through probes take the name of the probe.

---

| save Statement                | Action                                                                                                                                         |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>save 7</code>           | Saves voltage for a node named 7.                                                                                                              |
| <code>save 7:q</code>         | Saves the charge on the node named 7.                                                                                                          |
| <code>save *:q</code>         | Saves the charge on all nodes.                                                                                                                 |
| <code>save Q4:currents</code> | Saves all terminal currents associated with component Q4.                                                                                      |
| <code>save Q4:c:static</code> | Saves resistive terminal currents associated with component Q4.                                                                                |
| <code>save D8:cap</code>      | Saves the junction capacitance for component D8.<br>(Assumes D8 is a diode, and, therefore, <code>cap</code> is an operating-point parameter.) |

| save Statement          | Action                                                                                                                                                             |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| save Q5 D9:oppoint      | Saves all signal information for component Q5 and the operating-point parameters for component D9.                                                                 |
| save Q1:c               | Saves the collector current for component Q1. (Example assumes Q1 is a BJT, and, therefore, c is a terminal name.)                                                 |
| save Q1:1               | Same effect as the previous statement. Saves the collector current for component Q1. Identifies the terminal with its terminal index instead of its terminal name. |
| save M2:d:displacement  | Saves capacitive current associated with the drain terminal of component M2. (Example assumes M2 is a MOSFET, so d is a terminal name.)                            |
| save Q3:currents M1:all | Saves all currents for component Q3 and all signals for component M1.                                                                                              |
| save F4.S1.BJT3:oppoint | Saves operating-point parameters for device BJT3. BJT3 is in subcircuit S1. Subcircuit S1 is nested within subcircuit F4.                                          |

### Saving Individual Currents with Current Probes

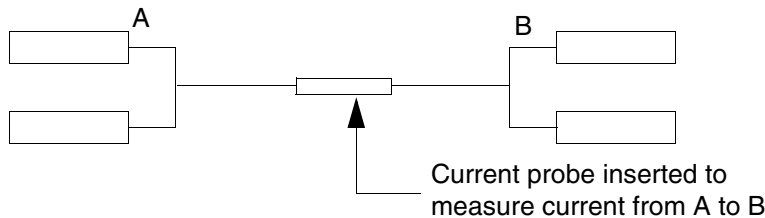
A current probe is a component that measures the current passing between two nodes. Its effect is like placing an amp meter on two points of a circuit. It creates a new branch in the circuit between the two nodes, forces the voltages on the two nodes to be equal, and then measures the flow of current.

#### ***When to Use Current Probes***

Use a probe instead of a `save` statement under the following circumstances:

- If you want increased flexibility for giving currents descriptive names  
With a current probe, you can name the current anything you want. With a `save` statement, the name of the current must have a `:name` suffix.
- If you are saving measurements for current-controlled components
- If you are saving currents for an AC analysis
- If you are saving measurements for a current that passes between two parts of a circuit but not through a terminal

The following example inserts a current probe to measure the current flowing between A and B. Because there is no component between A and B, there is no other way to measure this current except to insert a current probe that has an identical current to the one you want to measure.



**Example**

`Name in out iprobe`

|        |                                                                                                        |
|--------|--------------------------------------------------------------------------------------------------------|
| Name   | The unique netlist name for the current probe component. The measured current also receives this name. |
| in     | Input node of the probe.                                                                               |
| out    | Output node of the probe.                                                                              |
| iprobe | Primitive name of the component.                                                                       |

In the following example, the current probe measures the current between nodes `src` and `in`, names the measured current `Iin`, and saves `Iin` to the raw file.

`Iin src in iprobe`

**Note:** You can also direct the Spectre simulator to save currents with probes with a `save` statement option. For further information, see the description of [save statement keywords](#) in this chapter.

**Saving Power**

To save power dissipated on a circuit, subcircuit, or device, you use the `pwr` parameter. Power is calculated only during DC and transient analyses. The results are saved as a waveform, representing the instantaneous power dissipated in the circuit, subcircuit, or device.

**Formatting the pwr Parameter**

The syntax for the `pwr` parameter is illustrated by the following examples.

To save the power dissipated on a device or instance of a subcircuit, the syntax is

```
save instance_name:pwr
```

To save the total power, the syntax is

```
save :pwr
```

You can explicitly save particular power variables. For example:

```
save :pwr x1:pwr x1.x2.m1:pwr
```

This statement saves three power signals:

- total power dissipated (`:pwr`)
- power dissipated in the `x1` subcircuit instance (`x1:pwr`)
- power dissipated in the `x1.x2.m1` MOSFET

**Power Options**

The `pwr` parameter in the `options` statement can also be used to save power. The following table shows the five possible settings for the `pwr` option:

---

| Setting              | Action                                                                                                      |
|----------------------|-------------------------------------------------------------------------------------------------------------|
| <code>all</code>     | The total power, the power dissipated in each subcircuit, and the power dissipated in each device is saved. |
| <code>subckts</code> | The total power and the power dissipated in each subcircuit is saved.                                       |
| <code>devices</code> | The total power and the power dissipated in each device is saved.                                           |
| <code>total</code>   | The total power dissipated in the circuit is calculated and saved.                                          |
| <code>none</code>    | No power variable is calculated or saved. This is the default setting.                                      |

---

For example:

```
opts options pwr=total
save x1:pwr
```

This creates two power signals, `:pwr` (generated by the `options` statement) and `x1:pwr` (generated by the `save` statement).



## **Saving Groups of Signals**

To save groups of signals as results, use the `save` and `nestlvl` parameters. Specify which signals you want to save with the `save` parameter. Use the `nestlvl` parameter when you save signals in subcircuits. The `nestlvl` parameter specifies how many levels deep into the subcircuit hierarchy you want to save signals. The `save` parameter only saves the node voltages and the source terminal currents. It does not save device currents and subcircuit terminal currents.

You can set these parameters as follows:

- In `options` statements

If you set the `save` and `nestlvl` parameters with an `options` statement, the setting applies to signal data from all analyses that follow that statement in the netlist.

- In most analysis statements

If you set the `save` and `nestlvl` parameters with an analysis statement, the setting applies to that analysis only. It overrides any previous `save` or `nestlvl` settings.

## **Formatting the `save` and `nestlvl` Parameters**

The syntax for both the `save` and `nestlvl` parameters is illustrated by the following `options` statement:

```
setting1 options save=lvlpub nestlvl=2
```

## **The `save` Parameter Options**

The following table shows the possible settings for the `save` parameter:

| Setting               | Action                                                                                                                                                                                                                                                                           |
|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>none</code>     | Does not save any data (currently does save one node chosen at random).                                                                                                                                                                                                          |
| <code>selected</code> | Saves only the signals specified with <code>save</code> statements. This is the default setting.                                                                                                                                                                                 |
| <code>lvlpub</code>   | Saves all signals that are normally useful up to <code>nestlvl</code> deep in the subcircuit hierarchy. This option is equivalent to <code>allpub</code> for subcircuits. Normally useful signals include shared node voltages and currents through voltage sources and iprobes. |

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| Setting               | Action                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>lvl</code>      | Saves all signals up to <code>nestlvl</code> deep in the subcircuit hierarchy. This option is relevant for subcircuits.                                                                                                                                                                                                                                                                                        |
| <code>allpub</code>   | <p>Saves only signals that are normally useful, which include:</p> <ul style="list-style-type: none"><li>■ Voltages from nodes in the design</li><li>■ Current from voltage source in the design</li><li>■ Current from inductor in the design</li></ul> <p>The <code>allpub</code> option excludes the voltage of the nodes that are not seen in the design or netlist, but are created by the simulator.</p> |
| <code>all</code>      | <p>Saves all signals, which include:</p> <ul style="list-style-type: none"><li>■ Voltages from nodes in the design</li><li>■ Current from voltage source in the design</li><li>■ Current from inductor in the design</li><li>■ Voltage from an internal node in the device model or a Verilog-A module.</li></ul>                                                                                              |
| <code>nooutput</code> | Does not output any simulation results including node voltages, <code>vsource</code> currents, device currents, and <code>subckt</code> currents. For the <code>nooutput</code> option to have effect, it needs to be defined globally.                                                                                                                                                                        |

Use `lvl` or `all` (instead of `lvlpub` or `allpub`) to include internal node voltages and currents through other components that compute current.

Use `lvlpub` or `allpub` to exclude signals at internal nodes on devices (the internal collector, base, emitter on a BJT, the internal drain and source on a FET, etc). `lvlpub` and `allpub` also exclude the currents through inductors, controlled sources, transmission lines, transformers, etc.

**Note:** Setting the `save` parameter value to `selected` without any `save` statements in the netlist is not equivalent to specifying no output. Currently, the Spectre simulator automatically sets the `save` parameter to `allpub`.

If you specify the `save` parameter in a `tran` statement, Spectre, by default, saves all the data in the design. If you specify a parameter as a value to the `save` parameter, then Spectre rounds off the value to the nearest integer, assigns it to an enum type, and generates a warning message. For example:

```
simulator lang=spectre insensitive=yes
R1 1 2 resistor r=1k
```

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---

```
R2 2 0 resistor r=1k
V1 1 0 vsource dc=1
tran tran stop=1u save=tttotal
simulator lang=spice
.probe v(2)
.param tttotal=1.1ns
simulator lang=spectre
```

In the above example, `tttotal` has been specified as a value to the `save` parameter. Spectre will round off 1.1ns to 1, assign it to enum type `lv1` and generate a warning message.

The following table displays how Spectre will round off the values and assign them to various enum types:

| Specified Value | Rounded Off Value           | Enum Type Assigned          |
|-----------------|-----------------------------|-----------------------------|
| 0-0.4           | 0                           | <code>all</code>            |
| 0.5-1.4         | 1                           | <code>lv1</code>            |
| 1.5-2.4         | 2                           | <code>allpub</code>         |
| 2.5-3.4         | 3                           | <code>lv1pub</code>         |
| 3.5-4.4         | 4                           | <code>selected</code>       |
| 4.5-5.4         | 5                           | <code>none</code>           |
| 5.5-6.4         | 6                           | <code>nooutput</code>       |
| >6.5            | Invalid enumeration, ignore | Invalid enumeration, ignore |

### Saving Subcircuit Signals

To save groups of signals for subcircuits, you must adjust two parameter settings:

- Set the `save` parameter to either `lv1` or `lv1pub`.
- Set the `nestlv1` parameter to the number of levels in the hierarchy you want to save. The default setting for `nestlv1` is infinity, which saves all levels.

### Saving Groups of Currents

The `currents` parameter of the `options` statement computes and saves the device and source terminal currents and the inline subcircuit currents. You use it to create settings for currents that apply to all terminals in the netlist.

For two-terminal components, the Spectre simulator saves only the first terminal (entering) currents. You must use a `save` statement or set the values of the global `redundant_currents` and `useprobes` parameters of the `options` statement to `yes` to save data for the second terminal of a two-terminal component. For more information about the `save` statement, see [Saving Signals for Individual Nodes and Components](#) on page 591.

### ***Setting the currents Parameter***

The `currents` parameter has the following options:

| Setting                | Action                                                                                                                                                                                                                                                               |
|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>selected</code>  | Saves only currents that you specifically request with <code>save</code> statements or <code>save</code> parameters. Also saves naturally computed “branch” currents (currents through current probes, voltage sources, and inductors). This is the default setting. |
| <code>nonlinear</code> | Saves all terminal currents for nonlinear devices, naturally computed “branch” currents (currents through current probes, voltage sources, and inductors), and currents you specify with <code>save</code> statements. Can significantly increase simulation time.   |
| <code>all</code>       | Saves all inline device and subcircuit terminal currents and currents available from <code>selected</code> settings to the raw file. Can significantly increase simulation time.                                                                                     |
| <code>none</code>      | Does not save any device terminal currents.                                                                                                                                                                                                                          |

**Note:** Currently, if you set the `currents` parameter value to `nonlinear` or `all` and do not specify any node voltage and `vsource` current in the `save` statement, the Spectre simulator saves allpub signals as well as the currents you requested. This might change in future releases of the Spectre simulator.

### ***Examples of the currents Parameter***

You use the following syntax for the `currents` parameter in the `options` statement. For more information about the `options` statement, see the parameter listings in the Spectre online help (`spectre -h`).

- The Spectre simulator saves all terminal currents for nonlinear components, currents specified with the `save` statement, and routinely computed currents.

```
opt1 options currents=nonlinear
```

- The Spectre simulator saves all terminal currents.

```
opt2 options currents=all
```

### ***Setting Multiple Current Probes***

Sometimes you might need to set a large number of current probes. This could happen, for example, if you need to save a number of ACs. (Current probes can find such small signal currents when they are not normally computed.) You can specify that all currents be calculated with current probes by placing `useprobes=yes` in an `options` statement.

Setting multiple current probes can greatly increase the DC and transient analysis simulation times. Consequently, this method is typically used only for small circuits and AC analysis.

#### ***Important***

Adding probes to circuits that are sensitive to numerical noise might affect the solution. In such cases, an accurate solution might be obtained by reducing `reltol`.

### ***Saving Subcircuit Terminal Currents***

Use the `subcktprobelvl` parameter to control the calculation of terminal currents for subcircuits and inline subcircuits. Current probes are added to the terminals of each subcircuit, up to `subcktprobelvl` deep.

**Note:** If you use the `subcktprobelvl` parameter to compute the terminal currents for inline subcircuits, ensure that the `useprobes` option is set to `no`, otherwise, the device terminal currents are not plotted in ADE automatically.

### ***Saving Inline Subcircuit Terminal Currents***

Use the `inlinesubcktcurrent` parameter to control the calculation of inline subcircuit terminal currents. When either `currents` or `subcktprobelvl` parameter is applied on the inline subcircuit terminal, or the inline subcircuit terminal is specified in the `save` statement, the `inlinesubcktcurrent` parameter controls whether the current is from an inline device or subcircuit. Possible values for the `inlinesubcktcurrent` parameter are `device` and `subckt`. The default value is `subckt`.

## Hierarchical Current Probing

You can use the `save` statement to probe terminal currents hierarchically at a specified depth. You can specify the depth using the `probelvl` option to obtain the terminal current for all terminals connected to the specified terminal at that depth. The following is the syntax for obtaining the terminal currents:

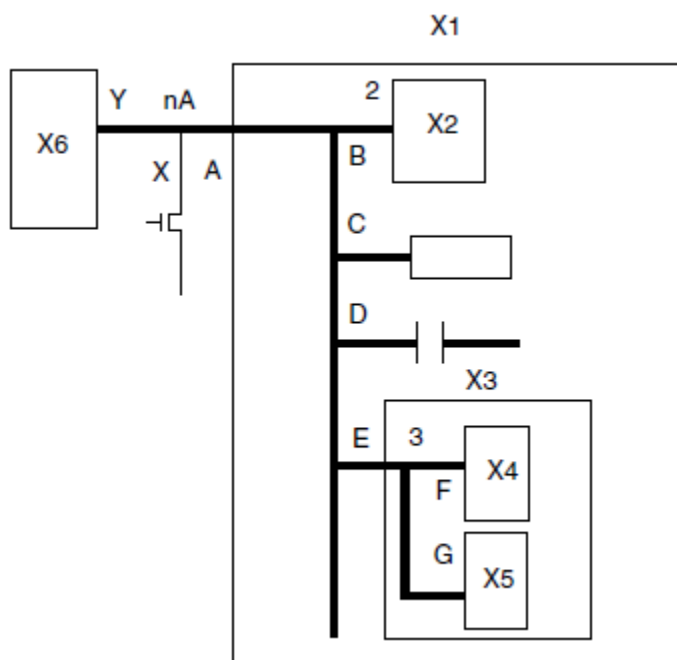
```
save X:terminal probelvl=value
```

Here, X is the subcircuit name, terminal is the subcircuit terminal, and value is the depth of the terminal that is connected to the subcircuit terminal.

You can also save the currents of all terminals that are connected to a node by specifying the node name, as shown below.

```
save nodeName:currents probelvl=value
```

Consider a scenario where terminal A is connected to terminals B, C, D, and E. In addition, terminal E is connected to terminals F and G, as shown in the following figure:



To probe all terminal currents that are connected to terminal A till the third-level depth, you can specify the following:

```
save X1:A probelvl=3
```

To save the currents of all terminals that are connected to node nA, you can use the following `save` statement:

```
save nA:currents probelvl=2
```

The above statement will save the currents of all terminals connected to node nA, that is, A, X, Y, B, C, D, and E.

### Using the `subcktiprobes` Parameter

You can save subcircuit terminal currents by using any of the following two methods:

- `save` statement. For example, `save X1:1`
- `subcktprobervl` parameter in the `options` statement. For example, `opt options subcktprobervl=1`

No matter which method you choose to save the subcircuit terminal currents, the simulator calculates the current by using any of the following two methods:

- Accumulating the current of devices inside the subcircuit.
- Inserting a current probe between the subcircuit terminal and the connection outside the subcircuit, and obtaining the current from the current probe.

The second method (current probe method) is more accurate than the first one.

You can use the `subcktiprobes` parameter in the `options` statement to choose the method to save the subcircuit terminal currents. The `subcktiprobes` parameter accepts the following values:

`no`: does not insert a current probe for the `save` statement or the `subcktprobervl` parameter.

`save`: inserts a current probe for the `save` statement but not for the `subcktprobervl` parameter.

`all`: inserts a current probe for both `subcktprobervl` parameter and `save` statement.

`yes`: (Default) If used with baseline Spectre, the behavior is equivalent to `subcktiprobes=all`; however, if used with Spectre APS, the behavior is equivalent to `subcktiprobes=save`.

### Measuring Stacked-FET Parameters

Stacked-FET is a mechanism that creates longer devices by using fixed length (L) FinFETs. Spectre treats stacked FETs as subcircuits containing multiple MOSFETs connected serially. The subcircuit must contain at least one MOSFET. In addition, the subcircuit should contain a minimum of four or a maximum of five terminals, and the first four terminals should be defined as drain, gate, source, and bulk. Extra terminals are ignored.

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To enable stacked-FET measurement, set the global option `subcktoppoint` to `yes`, as shown below.

```
Opt1 options subcktoppoint=yes
```

You can use the `save` statement to measure the parameters of stacked-FETs including term voltage, current, capacitance, conductance, and `vth`. All devices in the subcircuit can also be probed.

```
save inst_name:param_name
```

Here, `inst_name` is the subcircuit instance name and `param_name` is the name of the stacked FET parameter that needs to be measured. Wildcards are supported.

Following parameters are supported:

|                   |                                    |
|-------------------|------------------------------------|
| <code>vbd</code>  | Body-to-drain voltage              |
| <code>vbs</code>  | Body-to-source voltage             |
| <code>vgs</code>  | Gate-to-source voltage             |
| <code>vds</code>  | Drain-to-source voltage            |
| <code>vdg</code>  | Drain-to-gate voltage              |
| <code>id</code>   | Current flow in drain              |
| <code>ig</code>   | Current flow in gate               |
| <code>is</code>   | Current flow in source             |
| <code>ib</code>   | Current flow in bulk               |
| <code>gm</code>   | Gate transconductance              |
| <code>gds</code>  | Drain conductance                  |
| <code>gmbs</code> | Body transconductance              |
| <code>vth</code>  | Constant current threshold voltage |
| <code>cgg</code>  | Gate capacitance                   |
| <code>cgd</code>  | Gate-drain capacitance             |
| <code>cgs</code>  | Gate-source capacitance            |
| <code>cdd</code>  | Drain capacitance                  |
| <code>cds</code>  | Drain-source capacitance           |
| <code>cdg</code>  | Drain-gate capacitance             |



|         |                                          |
|---------|------------------------------------------|
| cbg     | Body-gate capacitance                    |
| cbd     | Body-drain capacitance                   |
| cbs     | Body-source capacitance                  |
| region  | Estimated operating region               |
| oppoint | All supported operating point parameters |

For example:

```
save I1:vth I1:vgS I1:vds
save *:oppoint devtype=subckt depth=3
save I0.*:oppoint devtype=subckt
```

You can use the `subcktopfreq` parameter in the `options` statement to set the frequency used in subcircuit operating point parameter calculation. The default value of `subcktopfreq` is  $1/(2\pi)$  Hz.

Stacked-FET measurement is supported in `dc`, `info`, and `tran` analyses. In `tran` analysis, you need to specify the time point by using `infotimes=[...]`.

| Analysis Name | Example                                                                                    |
|---------------|--------------------------------------------------------------------------------------------|
| dc            | dc dc<br>save X1:vth X1:gds                                                                |
| tran          | save X1:vth X1:gds<br>tran1 tran infoname=info1 infotimes=[...]<br>info1 info what=oppoint |
| info          | save X1:vth X1:gds<br>info1 info what=oppoint                                              |

Using Wildcards in the Save Statement

Wildcards provide a way to specify a pattern of a set of names without having to know all the names themselves. For example, the pattern `X1.X2.*` can match all node voltages in the subcircuit `X1.X2`.

You can use wildcards in Spectre for saving signals selectively and thus reducing runtime, memory usage, and disk space.

The syntax for using wildcards is:

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```
save {X[:param] [depth=depth] [sigtype=node|subckt|dev|all] [devtype=devicetype]
 [subckt=subname1] [xsubckt=subname2]
 [exclude=exclude] [compression=yes|no] [ports=yes|no] [filter=none|rc|colon]
 [logic=yes] [vlth=value] [vhth=value] [probelvl=value] [time_window= start1
 stop1 start2 stop2...]}
```

where

|                    |                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>X</i>           | Hierarchical name of a node/device/subcircuit.                                                                                                                                                                                                                                                                                                                                                                                       |
| <i>param</i>       | Device operating point parameter or a device or subcircuit terminal current.                                                                                                                                                                                                                                                                                                                                                         |
| <i>depth</i>       | Depth of expression matching, i.e. if <i>X:param</i> is a wildcard expression, $\text{depth}(X:param) = \text{depth}(X) = (\text{number of } . \text{ in } X) + 1$ .                                                                                                                                                                                                                                                                 |
| <i>sigtype</i>     | Type of the hierarchical name <i>x</i> in the wildcard expression <i>X:param</i> . Default: <i>node</i>                                                                                                                                                                                                                                                                                                                              |
| <i>devicetype</i>  | Type of device for which signals are to be saved.                                                                                                                                                                                                                                                                                                                                                                                    |
| <i>subname1</i>    | The subcircuit this save statement applies to. Setting this parameter is equivalent to defining the statement within the subcircuit declaration. Only one subcircuit name is allowed in a save statement. To declare more than one subcircuit, put them into separate save statements using the <i>subckt</i> parameter. You cannot use wildcards or brackets when using the <i>subckt</i> parameter to specify the subcircuit name. |
| <i>subname2</i>    | The subcircuit name that needs to be excluded from the save statement. For example, <code>save * xsubckt=sub1</code> . Wildcards are supported.                                                                                                                                                                                                                                                                                      |
| <i>exclude</i>     | Node or element names to be excluded from the save statement. You can use wildcards and brackets when using the <i>exclude</i> parameter to specify the node or element names.                                                                                                                                                                                                                                                       |
| <i>compression</i> | Define whether the signals need to be compressed. Default is <i>no</i> .                                                                                                                                                                                                                                                                                                                                                             |
| <i>ports</i>       | Output port information for the specified subcircuits. For example, <code>save x1* subckt=sub1 ports=yes</code> . Default is <i>no</i> .                                                                                                                                                                                                                                                                                             |
| <i>filter</i>      | Filter out the nodes that are connected only to parasitic elements from the output signal list. Wildcards are allowed.                                                                                                                                                                                                                                                                                                               |

|                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>logic</i>          | Sets up a logic probe on nodes for the specified quantity. The results are stored in a waveform output file. The <code>logic</code> argument only applies to node voltages and is ignored for all other signal types.                                                                                                                                                                                                                           |
| <code>vlth</code>     | Low voltage threshold ( <code>vlth</code> ) specifies the voltage threshold for the logic 0 (zero) state. The 0 (logic <code>vlth</code> ) state is probed if the node voltage is less than or equal to <code>vlth</code> . If the node voltage is between <code>vlth</code> and <code>vhth</code> , the X state is probed. If either <code>vlth</code> or <code>vhth</code> is not specified, then the <code>save</code> statement is ignored. |
| <code>vhth</code>     | High voltage threshold ( <code>vhth</code> ) specifies the voltage threshold for the logic 1 (one) state. The 1 (logic <code>vhth</code> ) state is probed if the node voltage is greater than or equal to <code>vhth</code> . If the node voltage is between <code>vlth</code> and <code>vhth</code> , the X state is probed.                                                                                                                  |
| <code>probelvl</code> | Saves the terminal current for all terminals connected to the specified terminal at a specified depth.                                                                                                                                                                                                                                                                                                                                          |

`time_window`

Specifies the time window for which the waveform data needs to be saved. You can specify multiple time windows using a single `save` statement. If multiple time windows are specified, the following rules apply:

1. For multiple time windows with same signal, union is used.
2. If a signal is saved twice, the statement containing the `time_window` option is honored.

You can specify `compression=yes` to turn on waveform compression. All output formats, such as `psf`, `psfbin`, `psfxl`, `fsdb`, `sst2`, and so on are supported.

The `time_window` option uses the next time step point after the start time and the last time step before the end time. It does not introduce a new breakpoint or step into the simulation.

You can also use the global `save_time_window` option to specify the time windows for which the waveform data needs to be saved. The `save_time_window` option applies to all `save` statements in the netlist and also to global `save` statements, such as `save=all` and `currents=all`.

However, if the `time_window` option is also specified with the `save` statement, the global `save_time_window` option is ignored.

## Example

```
save N1 time_window=[1u 2u 4u 5u]
save N2
opt1 options save_time_window=[6u 7u]
```

In the above example, node `N1` is saved from `1u` to `2u` and from `4u` to `5u`. In addition, node `N2` is saved from `6u` to `7u`.

Spectre supports the following wildcard pattern matching characters:

\* – matches any string including the empty string and the hierarchical delimiter ``.'`

? – matches any character including ``.'`

For a wildcard expression `X:param`, `*` and `?` is supported in the hierarchical name `X` and `*` is supported for `param`.



**Caution**

***Be careful when using wildcards in the save statement since saving too much data can degrade Spectre performance or cause out-of-memory problems.***

## **Examples of the Save Statement with Wildcard Patterns**

### **Save Statement with Wildcard Pattern    Action**

|                                        |                                                                                                                                                                                                             |
|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>save x*</code>                   | Saves the voltages of all nodes whose name starts with <code>x</code> , e.g. <code>xout</code> , <code>x10.n1</code> , <code>x1.x2.x3.n31</code> .                                                          |
| <code>save x*.*1</code>                | Saves the voltages of all nodes from level 2 and above (where 1 is the top level) whose name starts with <code>x</code> and ends in 1, e.g. <code>x1.n1</code> , <code>x1.x2.x3.n31</code> .                |
| <code>save *</code>                    | Saves all node voltages from all hierarchical levels, e.g. <code>xout</code> , <code>x10.n1</code> , <code>x1.x2.x3.n31</code> .                                                                            |
| <code>save xinv1:vdd*</code>           | Saves the port currents of all ports matching <code>vdd *</code> of subcircuit <code>xinv</code> .                                                                                                          |
| <code>save *:vdd*</code>               | Saves the port currents of all ports matching <code>vdd*</code> of all subcircuits.                                                                                                                         |
| <code>save *:1 sigtype=dev</code>      | Saves all currents through the first terminal of the devices.                                                                                                                                               |
| <code>save x*.*1 depth=5</code>        | Saves the voltages of all nodes from level 2 to level 5 whose name starts with <code>x</code> and ends in 1, e.g. <code>x1.n1</code> , <code>x1.x2.x3.x4.n31</code> but not <code>x1.x2.x3.x4.x5.n41</code> |
| <code>save x*.*1 depth=1</code>        | Saves nothing.                                                                                                                                                                                              |
| <code>save x*.*1 sigtype=subckt</code> | Saves all terminal currents of subcircuits from level 2 and above whose name starts with <code>x</code> and ends in 1', e.g. <code>x1.x21:2</code> , <code>x1.x2.x31:3</code>                               |

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|                                                     |                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>save x*.*1 sigtype=dev</code>                 | Saves all available device information including the terminal currents and the operating point parameters for devices from level 2 and above whose name starts with <code>x</code> and ends in <code>1</code> , e.g. <code>x1.x2.m1:1</code> , <code>x1.x2.x3.m31:oppoint</code> .                                                                                                    |
| <code>save * sigtype=all</code>                     | Saves all node voltages, subcircuit terminal currents and all available device information including terminal currents and operating point parameters.                                                                                                                                                                                                                                |
| <code>save *:c devtype=bjt</code>                   | Saves all collector currents.                                                                                                                                                                                                                                                                                                                                                         |
| <code>save x1*:vds devtype=bsim3v3</code>           | Saves <code>vds</code> of all <code>bsim3v3</code> devices whose name starts with <code>x1</code> .                                                                                                                                                                                                                                                                                   |
| <code>save I3.I*.M*:oppoint devtype=m0903</code>    | Saves the operating point parameters of all <code>m0903</code> devices from level 3 and above (where 1 is the top level) whose name matches the pattern.                                                                                                                                                                                                                              |
| <code>save * sigtype=node subckt=osc</code>         | Saves node voltages for all instances of the subcircuit <code>osc</code> , but no node voltage is saved outside these instances including the top level.                                                                                                                                                                                                                              |
| <code>save x* sigtype=node xsubckt=osc</code>       | Saves node voltages of all nodes whose name starts with <code>x</code> , except for node voltages of subckt <code>osc</code> .                                                                                                                                                                                                                                                        |
| <code>save m* sigtype=dev subckt=inv</code>         | Saves information for all devices <code>m*</code> contained in the instances of the subcircuit <code>inv</code> . For example, <code>I1.m1:1</code> is saved but not <code>I1.v1:p</code> and <code>mos1:d</code> .                                                                                                                                                                   |
| <code>save * exclude=[I1* I2*]</code>               | Saves voltages for all nodes except the nodes whose hierarchical path starts with <code>I1</code> and <code>I2</code> . For example, <code>net5</code> , <code>I3.out</code> , and <code>I5.I1.osc</code> are saved, but <code>I1.net5</code> , <code>I2.net9</code> , and <code>I100</code> are not saved.                                                                           |
| <code>save * exclude=[v*] subckt=mem depth=1</code> | Saves voltages for all nodes except the nodes <code>v*</code> in all the instances of subckt <code>mem</code> . Hierarchy levels saved are the top level of subcircuit <code>mem</code> and one level below. For example, if <code>I1.I2</code> is an instance of <code>mem</code> , <code>I1.I2.net5</code> is saved, but not <code>I1.I2.v1</code> and <code>I1.I2.I3.net8</code> . |

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|                                                                                                                              |                                                                                                                                                                                                                              |
|------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>save X1:A probelvl=3</code>                                                                                            | Saves all terminal currents that are connected to terminal A of subcircuit X1, till the third-level depth.                                                                                                                   |
| <code>save x*.*1 depth=3 time_window=[1m 2m 3m 4m]</code>                                                                    | Saves the voltages of all nodes from level 2 to level 3 whose names starts with x and ends in 1 from 1ms to 2ms and 3ms to 4ms.                                                                                              |
| <code>save N*</code><br><code>save N1 time_window=[1m 2m 3m 4m]</code>                                                       | Saves all nodes starting with N for entire simulation time, except N1 which is only saved from 1ms to 2ms.                                                                                                                   |
| <code>save N* time_window=[1m 3m]</code><br><code>save N1 time_window=[4m 5m]</code>                                         | <b>Note:</b> If a signal is saved twice, the statement containing the <code>time_window</code> option is honored.<br><br>Save all the nodes starting with N from 1ms to 3ms. In addition, saves node N1 from 4ms to 5ms.     |
| <code>save N* time_window=[1m 3m]</code><br><code>save N1 time_window=[2m 4m]</code>                                         | Saves all nodes starting with N from 1ms to 2 ms and saves node N1 from 1ms to 4ms.<br><br><b>Note:</b> If overlapping values are specified in multiple <code>time_window</code> options for the same signal, union is used. |
| <code>save N1 time_window=[1u 2u 4u 5u]</code><br><code>save N2</code><br><code>opt1 options save_time_window=[6u 7u]</code> | Saves node N1 from 1u to 2u and from 4u to 5u. In addition, saves node N2 from 6u to 7u.                                                                                                                                     |

## The print Statement

You can print signal and instance data to an output file by using the `print` statement. You can use the `print` statement for AC, DC, transient, noise, and sweep analyses.

You format the print statement as follows:

```
print item ... [,item] ,name=mytran {to="filename" | addto="filename"}
[precision="%15g"]
```

where

*item*  $V(node1[, node2])$  |  $I(terminal)$  | *Param* | *Expression*  
 $V(node1[, node2])$  Node voltage to be printed.

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|                                 |                                                                                          |
|---------------------------------|------------------------------------------------------------------------------------------|
| <code>I(<i>terminal</i>)</code> | Terminal current to be printed.                                                          |
| <code>Param</code>              | Parameter value to be printed.                                                           |
| <code>Expression</code>         | Expression to be printed.                                                                |
| <code>name</code>               | Analysis to be printed.                                                                  |
| <code>to</code>                 | Name of the output file. This file will overwrite any existing files with the same name. |
| <code>addto</code>              | Name of the file to which output is to be appended.                                      |
| <code>precision</code>          | Precision of the numerical values to be printed.                                         |

Use the following syntax to access noise parameters:

```
<noise_analysis_name>:<parameter_name>
```

where

`parameter_name` can be `out` (output noise), `in` (input noise), `F` (noise factor), or `NF` (noise figure).

### Examples

```
print im(I(vd1)),im(I(vd2)),im(I(vd3)), name=ac1 to="ac.out"
```

prints the imaginary parts of the current.

```
print I(vd), name=dc1 to="dc.out" precision="%15g"
```

prints the current.

```
print noise:out, name=noise to="noise.out"
```

prints the output noise.

## The set Statement

Except for temperature parameters and scaling factors, you use the `set` statement to modify any `options` statement parameters you set at the beginning of the netlist. The new settings apply to all analyses that follow the `set` statement in the netlist.

You can change the initial settings for the state of the simulator by placing a `set` statement in the netlist. The `set` statement is similar to the `options` statement that sets the state of the simulator, but it is queued with the analysis statements in the order you place them in the netlist.



You use the `set` statement to change previous `options` or `set` statement specifications. The modifications apply to all analyses that follow the `set` statement in the netlist until you request another parameter modification. The `set` and `options` statements have many identical parameters, but the `set` statement cannot modify all `options` statement parameters. The parameter listings in the Spectre online help tell you which parameters you can reset with the `set` statement.

The following example demonstrates the `set` statement syntax. This example turns off several annotation parameters.

```
Quiet set narrate=no error=no info=no
```

- `Quiet` is the unique name you give to the `set` statement.
- The keyword `set` is the primitive name for the `set` statement.
- `narrate`, `error`, and `info` are the parameters you are changing.

**Note:** If you want to change `temp` or `tnom`, use the `alter` statement.

## The shell Statement

The shell analysis passes a command to the operating system command interpreter given in the `SHELL` environment variable. The command behaves as if it were typed into the Command Interpreter Window, except that any `%X` codes in the command are expanded first.

The default action of the shell analysis is to terminate the simulation.

The following is the syntax for the shell statement:

```
Name shell parameter=value ...
```

## The statistics Statement

The statistics blocks allow you to specify batch-to-batch (process) and per- instance (mismatch) variations for netlist parameters. These statistically varying netlist parameters can be referenced by models or instances in the main netlist and can represent IC manufacturing process variation or component variations for board-level designs. For more information about the `statistics` statement, see [“Specifying Parameter Distributions Using Statistics Blocks”](#).



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## Specifying Output Options

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This chapter discusses the following topics:

- [Signals as Output](#) on page 616
- [Listing Parameter Values as Output](#) on page 616
- [Preparing Output for Viewing](#) on page 618
- [Accessing Output Files](#) on page 621

## Signals as Output

Signals are quantities that the simulator must determine to solve the network equations formulated to represent the circuit. The signals must be known before other output data can be computed.

Signals are mainly the physically meaningful quantities of interest to the user, such as the voltages on the topological nodes and naturally computed branch currents (such as those for inductors and voltage sources).

Other examples of signals are the voltages at the internal nodes of components and the terminal currents computed by using current probes at device or subcircuit terminals.

**Note:** If there are more than four terminals on a device (such as `vbic`, `hbt`, or `bta_soi`), the fifth and higher terminals do not return actual currents but return 0.0.

You can save signals and include them as simulation results. Signals you can save include the following:

- Voltages at topological nodes
- All currents
- Other quantities that the Spectre® circuit simulator computes to determine the operating point and other analysis data

For more information on saving signals, see [“The save Statement”](#) on page 255.

## Saving all AHDL Variables

If you want to save all the ahdl variables belonging to all the ahdl instances in the design, set the `saveahdlvars` option to `all` using a Spectre `options` command. For example:

```
Saveahdl options saveahdlvars=all
```

## Listing Parameter Values as Output

You can generate lists of component parameter values with the `info` statement. With this statement, you can access the values of input, output, and operating-point parameters. These parameter types are defined as follows:

- Input parameters

Input parameters are those you specify in the netlist, such as the given length of a MOSFET or the saturation current of a bipolar resistor.

### ■ Output parameters

Output parameters are those the simulator computes, such as temperature-dependent parameters and the effective length of a MOSFET after scaling.

### ■ Operating-point parameters

Operating-point parameters are those that depend on the operating point.

You can also list the minimum and maximum values for the input, output, and operating-point parameters, along with the names of the components that have those values.

## Specifying the Parameters You Want to Save

You specify parameters you want to save with the `info` statement `what` parameter. You can give this parameter the following settings:

---

| Setting                | Action                                                             |
|------------------------|--------------------------------------------------------------------|
| <code>none</code>      | Lists no parameters.                                               |
| <code>inst</code>      | Lists input parameters for instances of all components.            |
| <code>models</code>    | Lists input parameters for models of all components.               |
| <code>input</code>     | Lists input parameters for instances and models of all components. |
| <code>output</code>    | Lists effective and temperature-dependent parameter values.        |
| <code>all</code>       | Lists input and output parameter values.                           |
| <code>oppoint</code>   | Lists operating-point parameters.                                  |
| <code>terminals</code> | The output is a node-to-terminal map.                              |
| <code>nodes</code>     | The output is a terminal-to-node map.                              |

---

The `info` statement gives you some additional options. You can use the `save` parameter of the `info` statement to specify groups of signals whose values you want to list. For more information about `save` parameter options, consult [“Saving Groups of Signals”](#) on page 261. Finally, you can generate a summary of maximum and minimum parameter values with the `extremes` option.

## Specifying the Output Destination

You can choose among several output destination options for the parameters you list with the `info` statement. With the `info` statement `where` parameter, you can

- Display the parameters on a screen
- Send the parameters to a log file, to the raw file, or to a file you create

## Examples of the `info` Statement

You format the `info` statement as follows:

```
StatementName info parameter=value..
```

The following example tells the Spectre simulator to send the maximum and minimum input parameters for all models to a log file:

```
Inparams info what=models where=logfile extremes=only
```

For a complete description of the parameters available with the `info` statement, consult the lists of analysis and control statement parameters in the Spectre online help (`spectre -h`).

## Preparing Output for Viewing

In this section, you will learn how to format output data files so you can view them with a postprocessor.

## Output Formats Supported by the Spectre Simulator

You can choose from among the following format settings for output data files or directories. The default setting is `psfx1`. In the MMSIM 6.1 and succeeding releases, the Spectre simulator can create PSF files of unlimited size for all analyses.

---

| Option                  | Format                                                                                                                              |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| <code>fsdb/fsdb5</code> | Fast Signal Database format. This format is supported for transient analyses only. This format can be viewed in nWave and Sandwork. |
| <code>nutascii</code>   | Nutmeg–ASCII (SPICE3 standard output)                                                                                               |
| <code>nutbin</code>     | Nutmeg–binary (SPICE3 standard output)                                                                                              |
| <code>psfascii</code>   | Cadence parameter storage format (PSF)–ASCII                                                                                        |

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| Option                | Format                                                                                                                                                                    |
|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>psfbin</code>   | Cadence parameter storage format (PSF)–binary                                                                                                                             |
| <code>psfbinf</code>  | Cadence lowered precision parameter storage format                                                                                                                        |
| <code>psfxl</code>    | Cadence parameter storage XL format.                                                                                                                                      |
| <code>sst2</code>     | Signal Scan Turbo2 format. This format is supported for transient analyses only. This format can be viewed in Simvision and the Virtuoso Visualization and Analysis tool. |
| <code>tr0ascii</code> | TR0 ASCII format                                                                                                                                                          |
| <code>uwi</code>      | Unified Waveform Interface format. This format is supported for transient, ac, noise, DC, info, montecarlo, sweep, and RF analyses.                                       |
| <code>wdf</code>      | Waveform Data format. This format is supported for transient analyses only.                                                                                               |

For `psfbin`, and `psfascii` formats, the Spectre circuit simulator creates output files with extension `.tran` in the raw directory. The Spectre simulator overwrites existing files and directories with the same extension.

For `sst2`, `fsdb`, and `wdf` formats, the Spectre simulator creates output files with extensions `.trn`, `.fsdb`, and `.wdf` respectively.

PSF XL is a new Cadence waveform format which provides a high compression rate for large circuit designs. PSF XL is supported by the Virtuoso® Visualization and Analysis tool (available in the IC 6.1.7 and later releases).

The waveform files generated by the default `psfxl` format (`psfversion="1.1"`) are compressed and are much smaller in size. To generate the waveform files using the old `psfxl` format, use the option `psfversion="1.0"` in the `options` statement, as shown below.

```
spectre -format psfxl +aps input.scs
opt options psfversion="1.0"
```

**Note:** It is recommended to specify the value in double quotation marks.

RTSF is a PSF extension that can plot extremely large datasets (where signals have a large number of data points, for example 10 million) within seconds. RTSF is applicable to the `psfbin`, `psfbinf`, and `psfxl` formats, and is available with the visualization tool in IC 6.1.2 and later releases. You can enable RTSF by using the `+rtsf` option.

If the Spectre simulator cannot open files or create the necessary directories, it stops.

For further information about the Nutmeg format, consult the *Nutmeg Users' Manual* (available from the University of California, Berkeley).

You can use nWave or Sandwork to view outputs in the `fsdb` and `wdf` formats. For all other formats, you can use any waveform viewer in the Cadence IC flow.

### Defining Output File Formats

You can redefine the output file format in two ways:

- With a `spectre` command you type from the command line or place in an environment variable
- With an `options` statement you put in the netlist

You use the `options` statement in the netlist to override an environment default setting, and you use the `spectre` command at run time to override any settings in the netlist. The parameter values you enter are the same for either method.

### Example Using the `spectre` Command

The following example shows you how to set `format` options with the `spectre` command. This statement, which you type at the command line or place in an environment variable, directs the Spectre simulator to run a simulation on a circuit named `circuitfile` and format the results in binary Nutmeg.

```
spectre -format nutbin circuitfile
```

The following statement shows you how to specify the `uwi` format with the `spectre` command. This statement directs the Spectre circuit simulator to run the simulation on the circuit named `in.ckt` and write the output in the user-defined format `saf`. The library path is specified as `/hm/mtzakova/libUWI.so`.

```
spectre -format uwi -uwifmt saf -uwilib /hm/mtzakova/libUWI.so in.ckt
```

The following statement specifies multiple output formats simultaneously.

```
spectre -f uwi -uwifmt saf:wdf:fsdb -uwilib /hm/user1/libUWI.so in.ckt
```

### Example Using the `options` Statement

You set format options with the `rawfmt` parameter of the `options` statement as shown in the following example. This statement, which you place in the netlist, instructs the Spectre simulator to create an output file in binary Nutmeg. For more information about the `options` statement, see the parameter listings in the Spectre online help (`spectre -h`).



Settings options rawfmt=nutbin

## Accessing Output Files

After you run a simulation, you will want access to results of the various analyses you specified. To access these results, you need to know the names of the files and directories where the Spectre simulator stores these results. In this section, you will learn how the Spectre simulator names its output directories and files and how you can change these naming conventions to fit your needs. The information in this section applies to `psf` and `wsf` formats.

### How the Spectre Simulator Creates Names for Output Directories and Files

When you create a netlist, you give the netlist a filename. When you simulate the circuit, the Spectre simulator adds the suffix `.raw` to this filename to create the name of the output directory for the simulation. For example, results from the simulation of a file named `input.scs` are stored in a directory named `input.raw`.

In the output directory, results from each analysis you specify are stored in separate files. The root of each filename is the name you gave the analysis in the netlist, and the suffix for each filename is the type of analysis you specified. For example, if you run the following analysis, the Spectre simulator stores the results in a file named `Sparams.sp`:

```
Sparams sp start=100M stop=100G dec=100
```

For the `sweep` and `montecarlo` analyses, the names of the filenames are a concatenation of the parent analysis name, the iteration number, and the child analysis name. For example,

```
sweep1 sweep param=temp values=[-25 50]{
 dcOp dc
}
```

creates `sweep1_000_dcOp.dc` and `sweep1_001_dcOp.dc`.

The following example contains a number of analysis statements from a netlist. It shows the name of the output file the Spectre simulator creates for each analysis. In some cases, the Spectre simulator creates more than one output file for an analysis. This is because the

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analysis statement contains a parameter that specifies that certain output information be sent to a file.

```

// ANALYSES
OpPoint.info
OpPoint.dc → // DC operating point
 OpPoint dc print=yes oppoint=rawfile readns="ua741.dc"
 \
Drift.dc → write="ua741.dc"
 Drift dc start=0 stop=50.0 step=1 param=temp \
XferVsTemp.xf → nestlvl=0
 XferVsTemp xf start=0 stop=50 step=1 probe=Rload \
 param=temp freq=1k

// Gain
LoopGain.ac → please1 alter dev=Vfb param=mag value=1 annotate=no
 LoopGain ac start=1 stop=10M dec=10 nestlvl=0
 please2 alter dev=Vfb param=mag value=0 annotate=no

XferVsFreq.xf → // XF
 XferVsFreq xf start=1 stop=10M dec=10 probe=Rload
StepResponse.tran → // Transient
 StepResponse.info
 StepResponse tran stop=250u oppoint=rawfile
 SineResponse tran stop=150u errpreset=moderate \
 method=trap
SineResponse.tran
```

---

| Results File      | Description                                        |
|-------------------|----------------------------------------------------|
| logFile           | Log file (identifies output file format)           |
| OpPoint.info      | Nonlinear device DC operating-point file           |
| OpPoint.dc        | Node voltages at the operating point               |
| Drift.dc          | DC sweep                                           |
| XferVsTemp.xf     | Transfer function versus temperature               |
| LoopGain.ac       | AC analysis                                        |
| XferVsFreq.xf     | Transfer function versus frequency                 |
| StepResponse.tran | Transient analysis                                 |
| StepResponse.info | Operating-point information for transient analysis |
| SineResponse.tran | Transient analysis                                 |

---

## Filename for SPICE Input Files

If you specify analyses with standard SPICE syntax, the name of the output file for the first instance of each type of analysis is the same as the name shown in the following table:

| SPICE Analysis | Output Filename   |
|----------------|-------------------|
| .OP            | opBegin.dc        |
| .AC            | frequencySweep.ac |
| .DC            | srcSweep.dc       |
| .TRAN          | timeSweep.tran    |

**Note:** These names have special significance to the Cadence analog design environment.

If you request multiple unnamed analyses using SPICE syntax, the names are constructed by appending a sequence integer to the name of the analysis type and further adding the dot extension that is appropriate for the analysis. For example, multiple AC analyses would generate this sequence of files: `frequencySweep.ac`, `ac2.ac`, `ac3.ac`, `ac4.ac`, and so on.

## Specifying Your Own Names for Directories

You might want to specify a name for an output directory that is different from the name of your netlist. (For example, if you use the same netlist in more than one simulation, you probably want different names for the output files.) You can specify names in two ways:

- You can specify your directory name from the command line or in an environment variable with the `spectre` command `-raw` option. For example, if you want your output directory to be named `test.circuit.raw`, you start your simulation as follows:

```
spectre -raw test.circuit inputFile
```

- You can set the `rawfile` parameter of the `options` statement. For example, the following `options` statement creates an output directory named `test.circuit.raw`:

```
Setup options rawfile="test.circuit"
```

**Note:** The Spectre simulator has some additional features that help you manage data by letting you systematically specify or modify filenames. For more information about these features, see [Chapter 13, “Managing Files.”](#)



---

## Running a Simulation

---

This chapter discusses the following topics:

- [Running Spectre in 64-Bit](#) on page 626
- [Starting Simulations](#) on page 627
- [Checking Simulation Status](#) on page 630
- [Interrupting a Simulation](#) on page 630
- [Recovering from Transient Analysis Terminations](#) on page 631
- [Controlling Command Line Defaults](#) on page 634

## Running Spectre in 64-Bit

You can run 64-bit software using any of the following two methods:

- [Using the -64 Command Line Option](#) on page 626
- [Using the CDS\\_AUTO\\_64BIT Environment Variable](#) on page 626

### Important

Before you run 64-bit software, verify that all required patches are installed by running the *System Configuration Checking Tool* script, `checkSysConf`. This script is in your local installation of Cadence software, at the following location:

```
your_install_dir/bin/checkSysConf MMSIM19.1
```

`MMSIM19.1` is a parameter expected by the script.

The *System Configuration Checking Tool* is also available on the Cadence Online Support system. All required patches must be installed for the 64-bit executables to work correctly.

### Using the -64 Command Line Option

For example, run Spectre using the following command:

```
your_install_dir/bin/spectre -64 mem.scs
```

### Using the CDS\_AUTO\_64BIT Environment Variable

Do the following:

1. Set the environment variable `CDS_AUTO_64BIT {ALL|NONE|"list" | INCLUDE: "list" | EXCLUDE: "list" }` to select 64-bit executables.

|                 |                                                                                                                                                                                               |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ALL             | Runs all applications as 64-bit, where available. The list of applications available is in:<br><code>your_install_dir/bin/64bit</code>                                                        |
| NONE            | Runs all applications as 32-bit.                                                                                                                                                              |
| "list"          | Runs only the executables included in the list, where available, as 64-bit. <code>list</code> is a list of case-sensitive executable names delimited by comma(,), semi-colon(;), or colon(:). |
| INCLUDE: "list" | Runs all applications in the list as 64-bit, where available.                                                                                                                                 |

`EXCLUDE: "list"` Runs all applications as 64-bit, where available, except the applications in the list.

## Examples:

```
setenv CDS_AUTO_64BIT spectre
setenv CDS_AUTO_64BIT EXCLUDE:"si"
```

## 2. Run Spectre using the following command:

```
your_install_dir/bin/spectre
```

## Starting Simulations

To start a simulation, you type the `spectre` command at the command line with the following syntax:

```
spectre +spice options inputfile
```

The `spectre` command starts a simulation of *inputfile*. The simulation includes any options you request. For a given simulation, the `spectre` command options override any settings in default environment variables or `options` statement specifications.

The `+spice` option ensures that Spectre is invoked with the SPICE-compatible parser. In addition, it also

- sets `tnom` and `temp` to 25C
- sets parameter inheritance to global rather than the Spectre default of local. This means that global parameter definitions override local ones.
- sets flags on all device models to be SPICE compatible.
- enforces `.IC` statements and initial conditions on elements for DC and OP analyses. By default, Spectre only forces initial conditions if the DC analysis `force` option is set.

The following example starts a simulation of the input file `test1`.

```
spectre +spice test1
```

## Specifying Simulation Options

Many simulation runs require more complicated instructions than the previous example. Spectre® circuit-simulator-run options can be specified in two ways. Which method you use depends on the run option.

- You specify some Spectre options by typing a minus (-) in front of the option. The (-V) in the following example specifies that version information be printed for the simulation of circuit `test1`.

```
spectre -V test1
```

- You activate some Spectre options by typing a plus (+) before the option. You deactivate these options by typing a minus (-) before the option. For example, the following `spectre` command starts a simulation run for circuit `test1`. In this simulation, the Spectre simulator sets checkpoints but does not print error messages:

```
spectre +checkpoint -error test1
```

Some Spectre options have abbreviations. You can find these abbreviations in [Chapter 2, “Spectre Command Options,”](#) of the *Spectre Circuit Simulator Reference* manual. For example, you can type the previous command as follows:

```
spectre +cp -error test1
```

Specific `spectre` command options are discussed throughout this guide. For a complete list of options and formats, see [Chapter 2, “Spectre Command Options,”](#) of the *Spectre Circuit Simulator Reference* manual.

## Using License Queuing

You can turn on license queuing by using the `lqtimeout` command line option:

```
spectre +lqtimeout time
```

If a license is not available when you begin a simulation job, the Spectre circuit simulator waits in queue for a license for the specified time. If you specify the value 0 for this option, the Spectre circuit simulator waits indefinitely for a license. The `lqtimeout` option has no default value for the standalone Spectre circuit simulator. If you invoke Spectre through the Analog Design Environment, the default value for `lqtimeout` is 900 seconds.

You can use the `lqsleep` option to specify the interval (in seconds) at which the Spectre circuit simulator should check for license availability. The default value for `lqsleep` is 30 seconds.

```
spectre +lqsleep interval
```

For more information on any of the above options, see `spectre -h`.

## Suspending a Simulation Automatically When Disk Space is Low

You can use the `+disk_check` command-line option to suspend a simulation when the disk space is lower than the specified threshold. When Spectre finds the available disk space to



be less than the specified threshold value, it immediately suspends the simulation and generates a warning message. You can free up the disk space and type `kill -s CONT <pid>` at the command line to resume the simulation. However, if you set the option `disk_check_autoresume=yes` in the `options` statement, the simulation is resumed automatically once you free up the disk space.

The threshold value can also be set using the `disk_check_thresh` option in the `options` statement, as follows:

```
Opts options disk_check_thresh=1E9
```

The above statement sets the disk space threshold value to 1 gigabytes. The default value for the option `disk_check_thresh` is 1M.

## Suspending and Resuming Licenses

You can direct Spectre to release licenses when suspending a simulation job. This feature is aimed for users of simulation farms, where the licenses in use by a group of lower priority jobs may be needed for a group of higher priority jobs. To enable this feature, simply start Spectre with the `+lsuspend` command line option. Press `ctrl+z` to suspend the simulation run and release the Spectre license. All licenses are checked in. To resume simulation, press `fg`. These keystrokes may not work if you have changed the default key bindings.

You can also use the `kill` command to suspend and resume the simulation. You can suspend a simulation with `kill -s TSTP <pid>`. To resume the simulation, type `kill -s CONT <pid>`.

In Virtuoso® Analog Design Environment, the `lqtimeout` and `lqsleep` options are controlled by the following options:

```
spectre.envOpts lsuspend boolean t
spectre.envOpts licQueueTimeOut string "900"
spectre.envOpts licQueueSleep string "30"
```

## Determining Whether a Simulation Was Successful

When the Spectre simulator finishes a simulation, it sets the shell status variable to one of the following values:

- 0 If the Spectre simulator completed the simulation normally
- 1 If the Spectre simulator stopped any analysis because of an error

- 2 If the Spectre simulator stopped the simulation early because of a Spectre error condition
- 3 If a Spectre simulation was stopped by you or by the operating system

## Checking Simulation Status

If you want to check the status of a simulation during a run, type the following UNIX command:

```
% kill -USR1 PID
```

*PID* is the Spectre process identification number, which you can find by activating the UNIX `ps` utility.

The Spectre simulator displays the status information on the screen or sends it to standard output if it cannot write to the screen. If you check the status from a remote terminal, the Spectre simulator also writes the status to the `SpectreStatus` file in the directory from which the Spectre simulator was called. The Spectre simulator deletes this file at termination of the run.

**Note:** You can also give Spectre netlist instructions to display some status information. For more information, consult the Spectre online help about the `sweep` and `steps` options for the `annotate` parameter. You can set the `annotate` parameter for most Spectre analyses.

## Interrupting a Simulation

If you want to stop the Spectre simulator while a simulation is running, do one of the following:

- Send an INT signal with your interrupt character.

The interrupt character is usually `Control-c`. You can get information about the interrupt character for your system with the UNIX `stty` utility.

- Send the INT signal with a `kill(1)` command.

When you use either of these commands, the Spectre simulator prepares the incomplete output data file for reading by the postprocessor and then stops the simulation.



***Do not stop the Spectre simulator with a `kill -9` command. This command stops the simulation before the Spectre simulator can prepare the output files for reading by the postprocessor.***

## Recovering from Transient Analysis Terminations

If a transient analysis ends before a successful conclusion, you can recover the work that is completed and restart the analysis. The Spectre simulator needs saved state or checkpoint files to perform this recovery. State files save the current state of the simulation whereas checkpoint files save only the circuit operating point and simulation time at the specified point during the simulation. When re-starting an aborted simulation with a saved state file, convergence issues, glitches, and potential inaccuracies associated with the checkpoint mechanism are prevented.

You can change the netlist parameters (global, subcircuit, instance), temperature, simulation tolerances, and stop time between savestate and restart. You cannot change the topology and the platform you are running the simulation on.

This section tells you how to create saved state and checkpoint files. It also tells you how to restart a simulation after a transient analysis termination.

### Creating Saved State Files

You can save the current state of the system periodically during a simulation, so that if the simulation is interrupted, you can re-run the simulation from the last saved point. You can also use the save state feature to run a simulation up to a point, and then re-run the last portion of the simulation several times to investigate how the circuit responds to different stimuli. You can try various accuracy settings for different time periods to get the best performance for your simulation.

To create a saved state file,

1. Enable save state by typing `+savestate` as a command line argument to the `spectre` command that starts the simulation. Savestate is enabled by default.
2. Specify the time points and file to save the state to:

```
analysisName tran stop=stoptime [[saveperiod=time] | [savetime=[time1
time2...]] | [saveclock=clock_time]] [savefile=filename.srf]
```

where

#### If you specify

`saveperiod=time`

#### Spectre

generates a saved state file at the specified transient simulation time interval. Only the last generated saved state file is kept.

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|                                            |                                                                                                                                                                                                                                                                                     |
|--------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>savetime=[time1<br/>time2...]</code> | generates a saved state file at each specified time point and suffixes ascending numbers to the file name ( <code>filename.srf#</code> ) where <code>#=0, 1, 2...</code>                                                                                                            |
| <code>saveclock=clock_time</code>          | generates a saved state file at the specified real time interval. Default value is 30 minutes for Spectre. Spectre APS does not have any time limit for the <code>saveclock</code> period.                                                                                          |
| <code>savefile=filename.srf</code>         | saves the state to the specified file. Default name is <code>%C.%A.srf</code> where <code>%C</code> is the input circuit file name and <code>%A</code> is the analysis name.                                                                                                        |
| <code>savefile=filename</code>             | saves the state to file <code>filename@time1</code> , <code>filename@time2</code> and so on.<br><br>Default name is <code>%C.%A.srf_@time1</code> , <code>%C.%A.srf_@time2...</code> where <code>%C</code> is the input circuit file name and <code>%A</code> is the analysis name. |

If more than one time point parameter is specified, the Spectre circuit simulator utilizes the parameters in the order as given in the table above – i.e., `saveperiod`, `savetime`, and then `saveclock`.

By default, the Spectre simulator creates checkpoint files every 30 minutes during a transient analysis. In the case of Spectre APS, the `saveclock` period is set to infinity due to which, checkpoint files are not created unless `saveclock` is specifically set to a smaller value. The Spectre simulator deletes the savestate files when the simulation ends successfully.

The Spectre simulator attempts to save the state file after QUIT, TERM, INT, or HUP interrupts. After other interrupt signals, the Spectre simulator might be unable to save the state file.

### Creating checkpoint Files

This section talks about the following ways to create checkpoint files:

- Automatically, with defaults and `options` statement settings
- From the command line during a simulation
- For specific analyses with netlist instructions

This section also tells you how to restart a simulation after a transient analysis termination.

## Reactivating Automatic Recovery for a Single Simulation

If you have deactivated the default setting (by putting the `-checkpoint` setting in an environment variable), you can reactivate the default value for a given simulation run with the following procedure:

- Type `+checkpoint` as a command line argument to the `spectre` command that starts the simulation.

## Determining How Often the Spectre Simulator Creates Recovery Files

If you want to change how often the Spectre simulator creates checkpoint files for a particular simulation, or if you want your checkpoint files saved after a successful completion, you should set the `ckptclock` parameter of the `options` statement. For more information about the `options` statement, consult the parameter listings in the Spectre online help (`spectre -h`).

The following `options` statement tells the Spectre simulator to create checkpoint files every 3 1/2 minutes for all transient analyses in a simulation. (You indicate parameters for `ckptclock` in seconds.)

```
SetCkptInterval options ckptclock=210
```

## Creating Recovery Files from the Command Line

You can create a checkpoint file when a transient analysis is running with a UNIX interrupt signal from the command line.

- To create a checkpoint file from the command line, send a `USR2` signal with a UNIX `kill` command.

```
kill -USR2 PID
```

(You find the necessary process identification number by running the UNIX `ps` utility.)

The Spectre simulator also attempts to write a checkpoint file after `QUIT`, `TERM`, `INT`, or `HUP` interrupts. After other interrupt signals, the Spectre simulator might be unable to write a checkpoint file.

## Setting Recovery File Specifications for a Single Analysis

When you specify a transient analysis, you can also create periodic checkpoint files for that analysis.

- To create periodic checkpoint files for a transient analysis, set the `ckptperiod` parameter in the transient analysis statement.

The following example creates a checkpoint every 20 seconds during the transient analysis `SineResponse`:

```
SineResponse tran stop=150u ckptperiod=20
```

### Restarting a Transient Analysis

You can restart a transient analysis from the last saved state file or checkpoint file.

To restart a transient analysis from the last saved state file, do one of the following,

- Add the `+recover=[filename]` argument to the `spectre` command line
- Add the `recover` argument to the `tran` statement as follows:

```
analysisName tran recover=filename
```

To restart a transient analysis from the last checkpoint file,

- Add the `+recover` argument to the `spectre` command line

### Output Directory after Recovery

A new raw directory is created when recovering a saved state. The raw directory name is the same as the run directory name with an index number added, such as `*.raw#` where `#` is 0, 1, 2,...

For example, if the raw directory in the first run is `input.raw`, the recovered raw directory is `input.raw0`. The next recovered raw directory is named `input.raw1` and so on.

### Controlling Command Line Defaults

There are many run options you can specify with either the `spectre` command or the `options` statement. The Spectre simulator provides defaults for many of these options, so you can avoid the inconvenience of specifying many options for each simulation. Spectre defaults are satisfactory for most situations, but, if you have specialized needs, you can also set your own defaults. Spectre command line defaults control the following general areas:

- Messages from the Spectre simulator
- Destination and format of results

- Default values for the C preprocessor
- Default values for percent codes
- Creating checkpoints and initiating recoveries
- Screen display
- Name of the simulator
- Simulation environment (such as `opus`, `edge`, and so on)

### Examining the Spectre Simulator Defaults

You can identify the various Spectre defaults by consulting the detailed description of `spectre` command options in the *Spectre Circuit Simulator Reference* manual.

### Setting Your Own Defaults

You can set your own defaults by setting the UNIX environment variables `%S_DEFAULTS` or `SPECTRE_DEFAULTS`. In `%S_DEFAULTS`, `%S` is replaced by the name of the simulator, so this variable is typically `SPECTRE_DEFAULTS`. However, the name created by the `%S` substitution is different if you move the executable to a file with a different name or if you call the program with a symbolic or hard link with a different name. Consequently, you can create multiple sets of defaults, which you identify with different `%S` substitutions. Initially, the Spectre simulator looks for defaults settings in `%S_DEFAULTS`. If this variable does not exist, it looks for default settings in `SPECTRE_DEFAULTS`.

To set these environment variables, use the following procedure.

- In an appropriate file, such as `.cshrc` or `.login`, use the appropriate UNIX command to create settings for the environment variables `%S_DEFAULTS` or `SPECTRE_DEFAULTS`. Format the new default settings like `spectre` command line arguments and place them in quotation marks.

The following example changes the default output format from `psfbin` to `psfxl`. It also sets an option that is normally deactivated. It sends all messages from the Spectre simulator to a `%C:r.log` file.

For `csh`:

```
setenv SPECTRE_DEFAULTS "-format psfxl +log %C:r.log "
```

For `sh` or `ksh`:

```
SPECTRE_DEFAULTS="-format psfxl +log %C:r.log "
```

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EXPORT SPECTRE\_DEFAULTS

## Video

To view a demonstration on controlling the Spectre output, see [\*Controlling Spectre Outputs Using the Environment Variable Setting\*](#) video.

**Note:** Access to this video will depend on the availability of a web browser and a Cadence Online Support account.

This second example, a typical use of the SPECTRE\_DEFAULTS environment variable, tells the Spectre simulator to do the following:

- Write a log file named `cktfile.out`, where `cktfile` is the name of the input file minus any dot extension.
- Use the parameter soft limits file in the Cadence® software hierarchy.

```
setenv SPECTRE_DEFAULTS "+log %C:r.out +param /cds/etc/spectre/range.lmts"
```

You can use the default settings to specify alternative conditions for running the Spectre simulator. Suppose you create the following environment variables:

```
setenv SPECTRE_DEFAULTS "+param range.lmts +log %C:r.o -E"
setenv SPECSIM_DEFAULTS "+param corner.lmts =log %C:r.log \
-f psfbin"
```

If `spectre` and `specsim` are both links to the Spectre executable, and you run the executable as `spectre`, the Spectre simulator does the following:

- Reads the file `range.lmts` for the parameter limits
- Directs all messages to the screen *and* to a log file named after the circuit file with `.o` appended (see [Chapter 13, “Managing Files,”](#) for more information about specifying filenames)
- Runs the C preprocessor

Running the executable as `specsim` causes the Spectre simulator to select a different set of defaults and to do the following:

- Read the range limits from the file `corner.lmts`
- Direct log messages to a file named after the circuit file with `.log` appended (the `=log` specification suppresses the log output to the screen)
- Format output files in binary parameter storage format (PSF)



## References for Additional Information about Specific Defaults

In some cases, you need to consult other sections of this book before you can set defaults.

- If you want to set default limits for warning messages about parameter values, consult [Chapter 21, “Identifying Problems and Troubleshooting.”](#) to find information about installing Cadence defaults or creating your own range limits file if you need to customize defaults.
- You can find additional information about percent code defaults in [Description of Spectre Predefined Percent Codes](#) on page 951.

## Overriding Defaults

You can override defaults in the UNIX environment variables for a given simulation with either `spectre` command-line arguments or `options` statement specifications. The `spectre` command-line arguments also override `options` statement specifications.

### Video

To view the demonstration on overriding the defaults, see [\*Controlling Spectre Outputs during Run Time\*](#) video.

**Note:** Access to this video will depend on the availability of a web browser and a Cadence Online Support account.



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## AHDL Linter Checks

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This chapter contains the following topics:

- [About the AHDL Linter Feature](#) on page 640
- [Using the AHDL Linter Feature](#) on page 640
- [Identifying AHDL Linter Messages](#) on page 643
- [Filtering AHDL Linter Messages](#) on page 644
- [Using the ahdhelp Utility](#) on page 645

## About the AHDL Linter Feature

The AHDL Linter technology offers a powerful set of capabilities for upfront identification of issues that worry designers even well beyond the model creation stage. The AHDL Linter feature helps identify complex design modeling issues and can be used on block simulation or SOC verifications performed just before tape out. Early warnings enable designers to avoid expensive design iterations, and meeting quality and time-to-market goals.

You can use the AHDL Linter feature to analyze Spectre, Spectre APS and Spectre XPS test cases containing Verilog-A models.

AHDL Linter checks each behavioral model in the design and suggests which line should be improved to:

- Avoid potential convergence or performance problems
- Improve model accuracy, reusability, and portability

AHDL linter consists of static and dynamic lint checks. Static lint checks are performed at compilation stage. Dynamic lint checks are performed during analysis for dynamic modeling issues that may cause convergence or performance problems during simulation.

## Using the AHDL Linter Feature

The AHDL Linter feature is activated in Spectre, Spectre APS, and Spectre XPS using the following command-line options:

```
% spectre -ahdllint netlist.scs
% spectre +aps -ahdllint netlist.scs
% spectre +xps +cktpreset=sram -ahdllint netlist.scs
```

where `netlist.scs` is written using Spectre, SPICE, or eSpice syntax and includes one or more Verilog-A models.

You can perform static lint checks on a netlist file that includes one or more Verilog-A models, as follows:

```
spectre +aps -ahdllint=static test.scs // test.scs includes the Verilog-A files
```

Spectre, in this case, performs only lint checks on all Verilog-A files and does not run the simulation.

You can also perform static lint checks on a Verilog-A file directly without specifying the top-level netlist file (`.scs`), as follows:

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```
spectre +aps -ahdllint=static test.va //perform static lint check on test.va
```

The `-ahdllint` option accepts the following arguments:

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>no</code>     | Disables lint checks. There is no change in the existing compilation or simulation error messages.                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <code>warn</code>   | (default) Turns on the static lint and dynamic lint checks. Except the models with attribute <code>(* ahdllint = "no" *)</code> , the static lint checks all models, continues the simulation, and then performs dynamic lint checks.                                                                                                                                                                                                                                                                                                                          |
| <code>error</code>  | Turns on the static lint check. Dynamic lint checks are performed only when static lint issues are not detected. Except the models with attribute <code>(* ahdllint = "no" *)</code> , the static lint checks all models. The simulator generates an error and exits if there is any static lint warning reported after compiling all the models of the circuit. If there are no static lint warnings, the simulator continues the simulation and performs dynamic lint checks. However, in the case of dynamic lint issues, the simulator does not error out. |
| <code>force</code>  | Similar to <code>warn</code> , but this option overrides the model attribute <code>(* ahdllint = "no" *)</code> , and forces to check all models, continue the simulation, and perform dynamic lint checks.                                                                                                                                                                                                                                                                                                                                                    |
| <code>static</code> | Performs static lint checks on a Verilog-A file directly.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Note:** The `-ahdllint` option can be used without any argument, which is equivalent to specifying `-ahdllint=warn`. You can also set the `-ahdllint` option as default by setting the `SPECTRE_DEFAULTS` environment variable, as follows:

```
setenv SPECTRE_DEFAULTS "-ahdllint=warn"
```

You can use the `-ahdllint_maxwarn =n` command-line option to control the maximum number of static and dynamic warnings. The default value is 5.

You can also control the maximum number of warnings by using the environment variable `SPECTRE_DEFAULTS`, as show below.

```
setenv SPECTRE_DEFAULTS "-ahdllint -ahllint_maxwarn=10"
```

You can use the `-ahdllint_warn_id=<ID>` option to control the warning messages for a specific message ID. `ID` should be a positive integer value between 5001 and 6000 or 8001 and 9999. In addition, the `-ahdllint_warn_id` option should always be used with the `-ahdllint_maxwarn` option and should be directly specified after it in the command line, otherwise, the option will be ignored. For example:

```
spectre +aps -ahdllint -ahdllint_maxwarn=2 -ahdllint_warn_id=5001 input.scs
```

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In the above example, Spectre will display only two warning messages related to the message ID 5001.

You can specify the `-ahdllint_maxwarn` and `-ahdllint_warn_id` options multiple times at the command line. For example:

```
spectre +aps -ahdllint -ahdllint_maxwarn=1 -ahdllint_warn_id=5001 -
ahdllint_maxwarn=3 -ahdllint_warn_id=8001 input.scs
```

In the above example, only one warning message related to the message ID 5001 will be displayed. In addition, three warning messages related to the message ID 8001 will be displayed.

You can also specify multiple IDs with the `-ahdllint_warn_id` option. However, the IDs must be specified using double quotes with a space between them. For example:

```
spectre +aps -ahdllint -ahdllint_maxwarn=2 -ahdllint_warn_id="5001 5003 5005"
input.scs
```

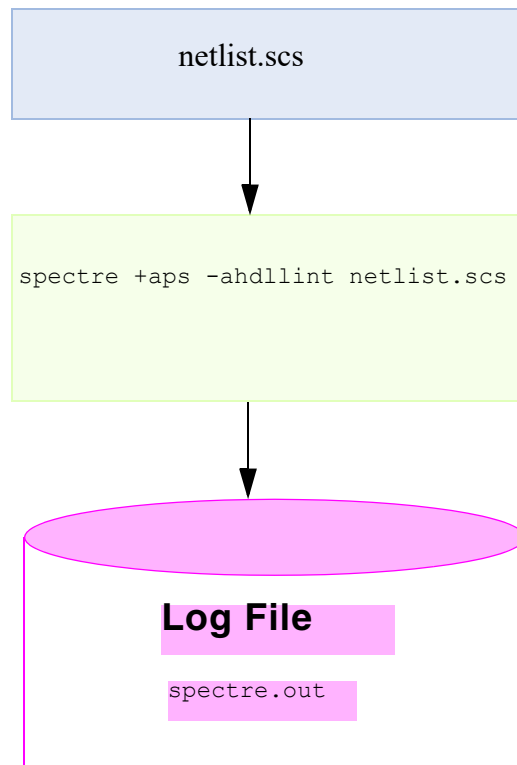
Use the `-ahdllint_minstep=value` command-line option to set the minimal time step size boundary that will trigger an AHDL Linter warning, when the step size imposed by a Verilog-AMS filter or function, such as `transition`, `cross`, `above`, `$bound_step`, and `timer` is smaller than `value`. The default value is `1e-12`.

You can use the `-ahdllint_summary_maxentries=<value>` command-line option to control the maximum number of messages to be displayed in dynamic lint summary. The default value is 25. For example:

```
spectre -ahdllint_summary_maxentries=20 input.scs
```

By default, the static and dynamic lint warnings and the dynamic lint summary output are sent to the simulation log file. You can use the `-ahdllint_log=file` command-line option to output all the information to a specified file instead of the output log file.

The following figure displays the AHDL Linter usage summary with Spectre APS.

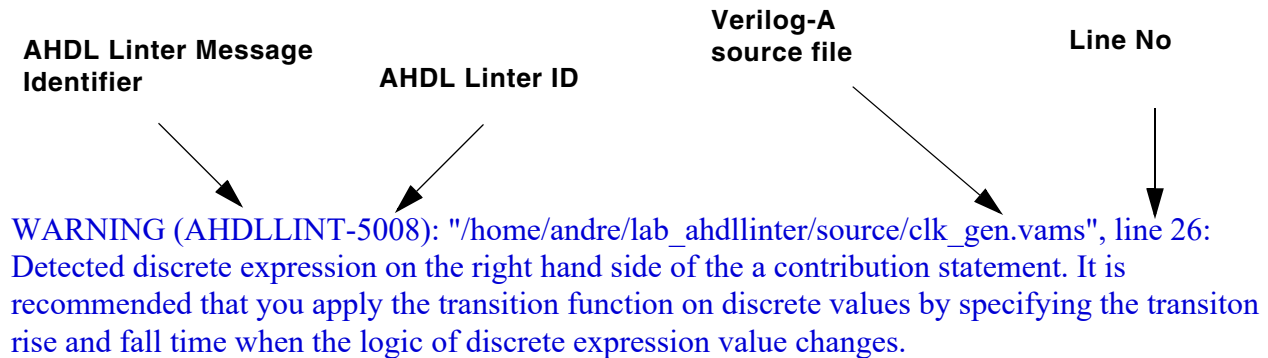


## Identifying AHDL Linter Messages

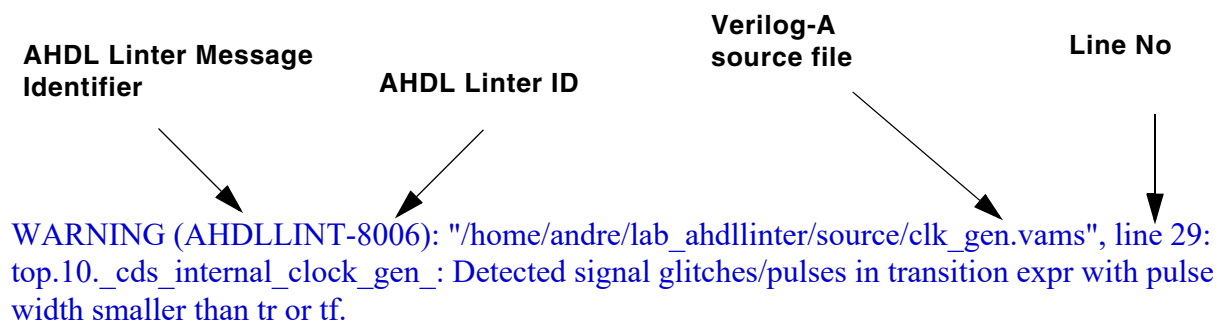
The messages generated from AHDL Linter (static or dynamic) have the AHDL Linter message identifier `AHDL LINT` at the beginning of the message followed by the message id.

The following examples show the static and dynamic AHDL linter messages generated by Spectre, Spectre APS, and Spectre XPS:

## Static AHDL Linter Message



## Dynamic AHDL Linter Message



## Filtering AHDL Linter Messages

You can filter the AHDL Linter messages using the `options` control statement, as follows:

```
Name options warning_limit=num warning_id=id
```

where:

`warning_limit` specifies the number of messages to be printed.

`warning_id` specifies the message id that needs to be printed.

### Example1



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```
myoptions options warning_limit=0 warning_id=[AHDLLINT-8004 AHDLLINT-8005]
```

In the above example, Spectre, Spectre APS, or Spectre XPS will not print any message with the id AHDLLINT-8004 and AHDLLINT-8005.

### Example2

```
myoptions2 options warning_limit=1 warning_id=[AHDLLINT-8005]
```

In the above example, Spectre, Spectre APS, or Spectre XPS will print only one message with the id AHDLLINT-8005.

For more information about the `options` control statement, see [The options Statement](#) on page 583.

## Using the ahdhelp Utility

You can use the `ahdhelp` utility to view the extended help on various messages reported by AHD Linter. To view the extended help, you need to provide the AHD Linter id number as an argument, as shown below.

```
% ahdhelp 8005
```

The following is an example of the `ahdhelp` utility:

```
% ahdhelp 5012
```

```
AHDLLINT-5012: Detected $abstime in an equality expression inside a conditional.
Analog simulations select timepoints using a variable timestep size algorithm based
on accuracy considerations, so the value of "time" only changes between discrete
real values. In order to perform an event at a particular time, the @(timer)
construct must be used to tell the simulator to step to a particular timepoint and
execute the desired code when that event actually occurs.
```

example:

```
if ($abstime==50n) xval=2;
```

solution:

```
@(timer(50n)) xval=2;
```



---

## Device and Circuit Checks

---

This chapter contains the following topics:

- Device Checks on page 648
  - ❑ The assert Statement on page 648
  - ❑ The check Statement on page 661
  - ❑ The checklimit Statement on page 662
  - ❑ Global Options on page 668
- Circuit Checks on page 677
  - ❑ Dynamic Checks on page 682
  - ❑ Static Checks on page 751

## Device Checks

The Spectre `assert` statement enables you to perform checks on design parameters, node voltages, element currents, model parameters, operating point parameters, and expressions. Use of wildcards and subcircuit scoping are supported.

When multiple `assert` checks are used, the `check` and `checklimit` statements enable you to manage which check is active during which analysis.

**Note:** The `assert`, `check`, and `checklimit` statements are supported only in Spectre, Spectre APS, Spectre X, Spectre XPS-SPICE, and Spectre XPS-MS. Spectre XPS-SRAM, Spectre XPS-FLASH and Spectre XPS-DRAM do not support this functionality.

The following topics provide more details:

[The `assert` Statement](#)

[The `check` Statement](#)

[The `checklimit` Statement](#)

[Global Options](#)

## The `assert` Statement

With the `assert` statement, you can set custom characterization checks to specify the safe operating conditions for your circuit. The Spectre circuit simulator then issues messages telling you when parameters move outside the safe operating area and, conversely, when the parameters return to the safe area, peak value and duration of violations. When a variable changes from an above-max value directly to a below-min value in one simulation step (that is, no stay within bounds), the Spectre simulator uses a middle bound solution  $(\text{min} + \text{max}) / 2$  to report the peak value and the duration of violations.

By default, Spectre reports the margin value as `value - boundValue`. However, if the `ASSERT_PEAKMARGIN` environment variable is set to 1, Spectre reports the margin value as `peakValue - boundValue`.

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The four types of checks that are supported in the device checking flow are described below.

| Check                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Initial setup check    | <p>Includes checks on constant parameters only, such as constant global, model or instance parameters that are independent of the operating points.</p> <p>This check is done only once before any analysis (including <code>checklimit</code>) is run. This check is also repeated once if any constant parameter is altered.</p> <p><b>Note:</b> The initial setup check cannot be disabled and the error level cannot be changed by the <code>checklimit</code> statement.</p> |
| Operating point check  | <p>Includes checks on MDL expressions and instance operating point parameters.</p> <p>This check is done for each analysis.</p>                                                                                                                                                                                                                                                                                                                                                   |
| Time domain check      | Check done during transient analysis.                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Frequency domain check | Check done during AC analysis.                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

Assert statements, which you specify in the netlist, are supported for transient, AC, DC, DC sweep, noise, pz, sp, and pss analyses.

You can set checks for any of the following:

- Top-level netlist parameter
- Model parameter
- Instance parameter
- Operating point parameter
- Expressions

The syntax for defining a check is

```
Name assert [sub=subcircuit_master] [subs=subcircuit_masters]
 { primitive=primitive | mod=model | dev=instance }
 { param=param | modelparam=mod_param | expr="[var_list;] mdl_expr" }
 [min=value] [max=value]
 [duration=independentvar_limit]
 [message="message"]
 [level= none | notice | warning | error | fatal]
```

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```
[info= yes | no]
[values=[enum_list]]
[boolean=true | false]
[anal_types=[analysis_list]]
[check_windows=[start1 stop1 start2 stop2...]]
[maxvio_perinst= value]
[maxvio_all= value]
[extreme=yes|no]
[safecheck=none|func|check]
[skip_dev_inside_subckt]
[min_peak=value]
[max_peak=value]
```

where

|                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>Name</i>                    | Name of the check statement. The name must not start with a number or contain invalid characters like space, dot, comma, slash, etc.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <i>sub=subcircuit_master</i>   | Subcircuit over which the check is to be applied.<br>An <code>assert</code> on a subcircuit type applies the check hierarchically to the lowest leaf-level instances. For example, If you define an <code>assert</code> statement with <code>sub</code> and <code>mod</code> , all device instances of the specified model type over all instances of the specified subcircuit type are checked. If the subcircuit type or master instantiates another subcircuit, the devices and models in that instance will be checked as well. Wildcards are supported. Double quotation marks are required with wildcards. For example, <code>sub="n*"</code> . |
| <i>subs=subcircuit_masters</i> | The subcircuits over which the check is to be applied.<br><br>Wildcards are supported. For example,<br><code>subs=[nmos? pmos*]</code><br><br><b>Note:</b> Enclose the subcircuit names within square brackets as shown in the above example.                                                                                                                                                                                                                                                                                                                                                                                                         |
| <i>primitive=primitive</i>     | Primitive whose model or instance parameter is to be checked. For a complete list of primitives, see <code>spectre -h components</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

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|                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>mod=model</code>                       | Model type whose model or instance parameter is to be checked. If the parameter to be checked is an instance parameter (specified using the <code>param</code> parameter), all instances of the specified model are checked. If the parameter to be checked is a model parameter (specified using the <code>modelparam</code> parameter), only the specified model is checked.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <code>dev=instance</code>                    | <p>Device or subcircuit instance whose instance parameter is to be checked. A name is first looked up as a subcircuit instance and then as a device instance. If an inline subcircuit and inline device inherits the same hierarchical name, the assert is applied to the subcircuit instance. If, however, the parameter specified is a device instance parameter, the assert is applied to the device instance. Wildcards are supported.</p> <p><b>Note:</b> In the case of stacked FETs, Spectre supports asserts to check for a violating device.</p>                                                                                                                                                                                                                                                                                                                                            |
| <code>param=param</code>                     | Device instance parameter, netlist parameter, operating point parameter, subcircuit parameter, node voltage or device terminal current to be checked. It is checked within the scope of the specified <code>sub</code> , <code>subs</code> , <code>dev</code> , <code>mod</code> or <code>primitive</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <code>modelparam=mod_param</code>            | Model parameter to be checked.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <code>expr="[var_list;]<br/>mdl_expr"</code> | <p>MDL expression to be checked.</p> <p>The <code>var_list</code> is optional and allows the Spectre simulator to return the value of specified variables. For example,<br/><code>expr="v_ds=v(d,s); len=1; v(d,s)&lt;3    1&gt;0.4u"</code></p> <p>An MDL expression can contain instance parameters, operating point parameters, netlist parameters, subcircuit parameters, node voltages, device terminal currents, or boolean expressions. The expression is checked within the scope of the specified <code>sub</code>, <code>subs</code>, <code>primitive</code>, <code>mod</code> or <code>dev</code>.</p> <p>The Spectre circuit simulator displays an error message when a boolean expression is true (by default) or when a non-boolean expression crosses the maximum or minimum value. You do not need to specify the <code>max</code> or <code>min</code> for a boolean expression.</p> |
| <code>min=value</code>                       | <p>Lower limit of the parameter to be checked.</p> <p>Default value: <math>-\infty</math></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

`max=value`

Upper limit of the parameter to be checked.

Default value:  $+\infty$

Note the following:

- The expression of constants is allowed to be used in `min` and `max` parameters. However, MDL expressions with variables, such as `V()` and `I()` are not allowed. (See [Example 4](#) on page 658)
- The `min` and `max` parameters are ignored for boolean expression checks.

`duration=independentva  
r_limit`

Time period over which the check has to be violated before a warning is displayed. Applicable to transient analyses only.

`message="message"`

Message to be printed if the check fails.

`level= none | notice  
| warning | error |  
fatal`

Severity level of the message if the check fails.

If the severity level is `notice` or `warning`, simulation continues after the message is displayed.

If the severity level is `error`, the Spectre circuit simulator aborts the analysis when the first error-level violation occurs. If the severity level is `fatal`, the Spectre circuit simulator aborts the simulation when the first fatal-level violation occurs.

Default value: `warning`

`info= yes | no`

When `yes`, the parameter will not be checked against `min`/`max`; only its value will be printed.

Default: `no`

`values=[enum_list]`

List of values of enumeration type parameters. By default, violations are reported when an enumeration parameter has a value inside `enum_list` and getting outside of `enum_list`. If the `boolean=false` parameter is set, violations are reported when an enumeration parameter has a value outside `enum_list`.

Example: `param=region values=[triode sat]`

Note the following:

- Without specifying values, an enumeration type parameter check will be ignored.
- There is no need to specify the `min` or `max` parameter for enumeration type parameter checks.



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|                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>boolean= true   false</code>      | <p>This is used to choose report style for boolean violations. When set to <code>true</code> (default), the violation is printed when the expression changes from <code>false</code> to <code>true</code>. When set to <code>false</code>, the violation is printed when the expression changes from <code>true</code> to <code>false</code>.</p>                                                                                                                                                                                       |
| <code>anal_types=[analysis_list]</code> | <p>The list of analysis types for which the check is to be applied. By default, the check is applied to all the analyses specified in the netlist. Possible values are <code>ac</code>, <code>dc</code>, <code>noise</code>, <code>pz</code>, <code>sp</code>, <code>tran</code>, and <code>pss</code>.</p> <p>Example: <code>anal_types=[dc tran]</code></p> <p><b>Note:</b> The <code>anal_types</code> parameter is ignored if an invalid analysis type is specified.</p>                                                            |
| <code>check_windows</code>              | <p>The time windows within which the assert is to be enabled or disabled. Sweep windows are not supported. Therefore, this parameter should not be used with sweep analysis.</p> <p><b>Note:</b> If the <code>check_windows</code> parameter is defined in both <code>assert</code> and <code>checklimit</code> statements, the <code>check_windows</code> parameter in the <code>assert</code> statement takes higher precedence over the <code>check_windows</code> parameter specified in the <code>checklimit</code> statement.</p> |
| <code>maxvio_perinst</code>             | <p>Limit the violation number to a specified value <i>&lt;value&gt;</i> for each particular checked instance. This means that if the violation count reaches the number specified by <i>&lt;value&gt;</i> then that instance is not checked during the remaining steps of the analysis.</p>                                                                                                                                                                                                                                             |
| <code>maxvio_all</code>                 | <p>Limit the violation number to a specified value <i>&lt;value&gt;</i> for all the checked instances during the analysis.</p>                                                                                                                                                                                                                                                                                                                                                                                                          |
| <code>group</code>                      | <p>Specify the group to which the assert belongs to. The default value is <code>default</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>extreme</code>                    | <p>When <code>extreme=yes</code>, it reports the extreme value of the boolean check assert. Possible values are <code>yes</code> and <code>no</code>. The default value is <code>no</code>.</p>                                                                                                                                                                                                                                                                                                                                         |

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|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>safecheck</code>              | <p>Specify the assert type for fault detection. When <code>safecheck=func</code>, it checks the functional module. <code>safecheck=check</code> checks the diagnostic module (checker). A functional safety report is generated for both <code>func</code> and <code>check</code> asserts. Set the value of the <code>safecheck</code> to <code>none</code> to perform regular assert checking. Possible values are <code>none</code>, <code>func</code>, and <code>check</code>. See <a href="#">Fault Analysis</a> for more information on Spectre fault analysis.</p> |
| <code>skip_dev_inside_subckt</code> | <p>Skips subcircuits or device instances inside the subcircuit. For example, <code>skip_dev_inside_subckt=[pll.M1 pll.inv1]</code> will not perform assert check on the device model instance <code>M1</code> and the subckt instance <code>inv1</code> inside the subckt definition of <code>pll</code>.</p>                                                                                                                                                                                                                                                            |
| <code>max_peak</code>               | <p>Specify the maximum threshold based on which the violation is reported.</p> <p><b>Note:</b> <code>max_peak</code> does not impact the assertion check. It only limits the assert output report and reports only the violations that violate the assert and cross the <code>max_peak</code> limit.</p>                                                                                                                                                                                                                                                                 |
| <code>min_peak</code>               | <p>Specify the minimum threshold based on which the violation is reported.</p> <p><b>Note:</b> <code>min_peak</code> does not impact the assertion check. It only limits the assert output report and reports only the violations that violate the assert and cross the <code>min_peak</code> limit.</p>                                                                                                                                                                                                                                                                 |

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The following table displays some ways to use the `assert` parameters.

| # | Assert parameters                                                                            | Description                                                                                                                                                                                                                                         | Applies to                                                                                             |
|---|----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| 1 | <code>dev=device or subckt instance</code><br><code>param=paramname</code>                   | <code>paramname</code> can be an:<br>- Instance parameter<br>- Operating point parameter<br>- Netlist parameter<br>- Node voltage or device terminal current<br><br>For subcircuit instances, <code>paramname</code> can be a subcircuit parameter. | The specified instance.                                                                                |
| 2 | <code>mod=model</code><br><code>param=paramname</code>                                       | <code>paramname</code> can be an:<br>- Instance parameter<br>- Operating point parameter                                                                                                                                                            | All instances of the specified model.                                                                  |
| 3 | <code>mod=model</code><br><code>modelparam=paramname</code>                                  | <code>paramname</code> must be a model parameter.                                                                                                                                                                                                   | The specified model.                                                                                   |
| 4 | <code>primitive=primitive</code><br><code>param=paramname</code>                             | <code>paramname</code> can be an:<br>- Instance parameter.<br>- Operating point parameter                                                                                                                                                           | All instances of the specified primitive type.                                                         |
| 5 | <code>primitive=primitive</code><br><code>modelparam=paramname</code>                        | <code>paramname</code> must be a model parameter.                                                                                                                                                                                                   | All models of the specified primitive type.                                                            |
| 6 | <code>sub=subcircuit_master</code><br><code>dev=X1</code><br><code>param=paramname</code>    |                                                                                                                                                                                                                                                     | Device X1 over all instances of the specified subcircuit.<br>Same as row 1.                            |
| 7 | <code>sub=subcircuit_master</code><br><code>mod=model</code><br><code>param=paramname</code> |                                                                                                                                                                                                                                                     | All instances of the specified model over all instances of the specified subcircuit.<br>Same as row 2. |

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| #  | Assert parameters                                                                                           | Description                                                                                        | Applies to                                                                                                   |
|----|-------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|
| 8  | <code>sub=subcircuit_master</code><br><code>mod=model</code><br><code>modelparam=paramname</code>           |                                                                                                    | The specified model over all instances of the specified subcircuit.<br>Same as row 3.                        |
| 9  | <code>sub=subcircuit_master</code><br><code>primitive=primitive</code><br><code>param=paramname</code>      |                                                                                                    | All instances of the specified primitive over all instances of the specified subcircuit<br>Same as row 4.    |
| 10 | <code>sub=subcircuit_master</code><br><code>primitive=primitive</code><br><code>modelparam=paramname</code> |                                                                                                    | All models of the specified primitive type over all instances of the specified subcircuit.<br>Same as row 5. |
| 11 | <code>sub=subcircuit_master</code><br><code>param=paramname</code>                                          | <code>paramname</code> is a subcircuit parameter.                                                  | All instances of the subcircuit.                                                                             |
| 12 | <code>expr=mdl_expr</code>                                                                                  | Valid conditional expression or combination of operating points.                                   | Expression-specific instances, node voltages etc.                                                            |
| 13 | <code>expr="mdl_expr"</code><br><code>min=value</code><br><code>max=value</code>                            | The expression is evaluated and compared against the <code>min</code> and <code>max</code> values. | Expression-specific instances, node voltages etc.                                                            |

If you define an `assert` statement within a subcircuit block without the `sub` parameter, the check is applied to that block only. If you use the `sub` parameter, the specified subcircuit master must be defined within the block.

You can use the `defwave` parameter to define a new waveform by relating previously defined waveforms and nodes and also specify the parameter in the `assert` statement as an expression. For example:

```
defwave comp1=v(1)-v(2)
defwave comp2=m1:vds + m1:vds + comp1
assert1 assert expr="comp1>0" info=yes level=warning message="v(1)>v(2) out of bound."
testdev22 assert expr="comp2 - m3:vds" min=0.0 max=1.0
```

The name of `defwave` should be different from instance parameters, model parameters, operating point parameters, netlist parameters, or subcircuit parameters. For example, consider M1 as an instance of an inline subcircuit `mos_r`, as shown below.

```
inline subckt mos_r (d g s b)
parameters p1=1u p2=2u
mos_r (dp g sp b) mos_mod l=p1 w=p2// "inline" component
rd (d dp) resistor r=10 // series drain resistance
rs (s sp) resistor r=10 // series source resistance
ends mos_r
```

In addition, consider the following assert statement:

```
defwave vds=v(d) - v(s)
assert2 assert expr="vds" sub=mos_r min=0.0 max=1.0
```

Here, `assert2` will check the opoint parameter `vds` of `mos_r` that is different from terminal voltages (`v(d) - v(s)`) for subcircuit `mos_r`.

Violations are reported at the following three stages:

- At initial setup stage.
- On the occurrence of a violation when the assert is evaluated.
- At the end of an analysis.

All `assert` statement violations are written to the Spectre log file by default, irrespective of the `maxwarnstologfile` and `maxnotestologfile` parameter settings. You can use the `checklimitfile` option to write the violations to a dedicated file. A message during simulation indicates where the violations are being written. For more information, see `spectre -h options`.

### Examples of the assert Statement

#### **Example 1**

```
vtho_check assert primitive=bsim3 modelparam=vtho min=-0.2 max=0.2
message="vtho exceeds bound" level=warning
```

Checks for model parameter `vtho` over all device instances of the primitive type BSIM3 and prints a warning `vtho exceeds bound` if the value of `vtho` is less than -0.2 and higher than 0.2.

## Example 2

```
mlvgs_check assert sub=inv dev=m1 param=vgs min=0.0 max=2.5
 message="vgs exceeds bound" level=notice
```

Checks for operating point `vgs` in the device `m1` over all instances of the subcircuit type `inv` in the netlist and prints a notice `vgs exceeds bound` if the value of `vgs` is less than 0 and higher than 2.5.

## Example 3

Netlist:

```
subckt mysubckt a b c
parameters adNum=0.0
.....//contents of the subcircuit
ends mysubckt
```

Check defined for the above netlist:

```
adNum_check assert dev=X1 param=adNum min=0.0 max=5.0
 message="Drain parasitic resistor is too high" level=warning
```

Checks the parameter `adNum` in the subcircuit instance `X1` and prints a warning `Drain parasitic resistor is too high` if the value of `adNum` is higher than 5.0.

## Example 4

```
Parameters p1=0.8
...
M1_powercheck assert expr="(max(m1:ids*m1:vds))" max=(p1*0.5e-3)
 message="power of M1 exceeds expected load power"
```

Checks that `(max(m1:ids*m1:vds))` is less than `(p1*0.5e-3)`. If not, it prints the warning `power of M1 exceeds expected load power`.

## Example 5

```
MAX_powercheck assert expr="max(m1:pwr) < max(abs(vin:dc*I(r1)))"
 message="power of M1 exceeds expected load power" boolean=false
```

Checks that maximum power `max(m1:pwr)` is less than `max(abs(vin:dc*I(r1)))`. If not, it prints the warning `power of M1 exceeds expected load power`.

## Example 6

```
voltage_check assert subs=[inv? dff*] dev=m1 expr="V(d,s)" min=0.0 max=2.5
```

Checks for voltage across terminals *d* and *s* of device *m1* in all instances of subcircuits: whose names match *dff\** or *inv?* and prints a warning when the value of  $V(d, s)$  is less than 0 or higher than 2.5.

### Example 7

```
Op_check assert mod=nch dev=m1 expr="vds" min=0.0 max=2.5 anal_types=[dc]
```

Checks for the operating point drain-source voltage in all instances of the model *nch* for DC and DC sweep analyses only, and prints a warning when the value of *vds* is less than 0 or higher than 2.5.

### Example 8

```
boolean_check assert dev=I0 expr="Id=I(d); len=l; (I(d) >=2m) || (l > 1u)"
anal_types=[dc tran]
```

Checks for the boolean expressions  $I(d) \geq 2m$  or  $length > 1u$  in the instance *I0* for DC, DC sweep and transient analyses only, prints a warning when the boolean expression is true, and returns the value of *Id* and *len*.

### Example 9

```
cap_voltage_check assert primitive=capacitor expr="V(1)-V(2)" max=1
```

Checks for the voltage difference across the terminals of all capacitors and prints a notice if the value of  $V(1) - V(2)$  is higher than 1.

### Example 10

```
current_check assert expr="I(I2:1)" max=1m message="test current!"
```

Checks for the current flowing through terminal *I2:1* and prints a notice *test current!* if the value is larger than 1mA.

### Example 11

```
Parameters bvca=9.1
...
Not_chk assert sub=in1 expr="!(V(d,s) > (bvca-0.5))" level=notice message =
"Testing Not!"
```

Checks the voltage across terminals *d* and *s* in the instances of subcircuit *in1*, and prints a notice *Testing Not!* when  $V(d, s)$  is not greater than  $(bvca - 0.5)$ .

## Example 12

```
sub res n1 n2 n3
assert_i assert sub=res expr="V(index(2), index(1))" min=-1 max=1 level=warning
```

The above example checks index 2 - index 1 for subckt res which is equivalent to  $n2 - n1$ .

## Example 13

```
subckt mysubckt1 D G S B
 MN0 (net5 G S B) my_nch w=(120n) l=45n
 MN1 (D G net7 B) my_nch w=(120n) l=45n
 MN2 (net7 G net6 B) my_nch w=(120n) l=45n
 MN3 (net6 G net5 B) my_nch w=(120n) l=45n
ends mysubckt1
I1 (D G S B) mysubckt1
```

```
stacked_device assert dev=I3 param=id max=-100
```

For the case with stacked FETs, Spectre now supports asserts to check for a violating device.

## Example 14

```
assertAbsTime assert expr="abstime()" max=-1 info=yes
```

The above example checks the transient time and prints the value if it is greater than -1. For example, the above statement will print the following:

```
Warning from spectre at time = 4.122041315 ns during transient analysis 'trans'.
 WARNING (SPECTRE-4107): assertAbsTime: Instance, Expression 'abstime()' has
value 4.122041315e-09
Warning from spectre at time = 7.596470186 ns during transient analysis 'trans'.
 WARNING (SPECTRE-4107): assertAbsTime: Instance, Expression 'abstime()' has
value 7.596470186e-09
Warning from spectre at time = 11.7083856 ns during transient analysis 'trans'.
 WARNING (SPECTRE-4107): assertAbsTime: Instance, Expression 'abstime()' has
value 11.7083856e-09
Warning from spectre at time = 19.92157532 ns during transient analysis 'trans'.
 WARNING (SPECTRE-4107): assertAbsTime: Instance, Expression 'abstime()' has
value 19.92157532e-09
```

## Example 15

```
tran tran step=1e-12 pstep=1e-12 stop=2e-08
```



```
check_full_simu_tim assert message="CHECK_FULL_SIMU_TIME"
expr="full_simu_time=stoptime(); full_simu_time>10n"
```

The above example checks the transient stop time and prints a warning if it is greater than 10n. For example, the above statement will print the following:

```
Warning from spectre during transient analysis 'tran'.
WARNING (SPECTRE-4056): check_full_simu time: CHECK_FULL_SIMU_TIME.
Expression 'full_simu_time=stoptime(); full_simu_time>10n' is getting true where
full_simu_time=20e-09. Total duration of overshoot was 19.999e-09.
```

The check Statement

You can perform a check analysis by adding the check statement after the analysis statement in your netlist. The check analysis checks the values of the component parameters to be sure that the values of component parameters are reasonable. You can perform checks on input, output, or operating-point parameters. The Spectre simulator checks parameter values against parameter soft limits. For information on the default soft limits, see [Customizing Error and Warning Messages](#) on page 332.

To use the check analysis, you must also enter the +param command line argument with the spectre command to specify a file that contains the soft limits.

The following example illustrates the syntax of the check statement. It tells the Spectre simulator to check the parameter values for instance statements.

```
ParamChk check what=inst
```

- ParamChk is your unique name for this check statement.
- The keyword check is the component keyword for the statement.
- The what parameter tells the Spectre simulator which parameters to check.

The what parameter of the check statement gives you the following options:

| Option | Action                                                              |
|--------|---------------------------------------------------------------------|
| none   | Disables parameter checking                                         |
| models | Checks input parameters for all models only                         |
| inst   | Checks input parameters for all instances only                      |
| input  | Checks input parameters for all models and all instances            |
| output | Checks output parameters for all models and all instances           |
| all    | Checks input and output parameters for all models and all instances |

| Option  | Action                                                             |
|---------|--------------------------------------------------------------------|
| oppoint | Checks operating-point parameters for all models and all instances |

## The checklimit Statement

You can enable or disable an assert or a group of asserts with the `checklimit` statement. You can define one or more `checklimit` statements in the netlist, each enabling or disabling individual asserts. The statement is applied to subsequent transient, DC, and DC sweep analyses until the next `checklimit` statement appears.

If there is no `checklimit` statement before all the analyses, a default `checklimit` statement enabling all asserts is added. In other words, by default, all asserts are enabled. The first `checklimit` statement that specifically enables asserts also disables the remaining asserts. The `checklimit` statements are cumulative in effect except when the `checkallasserts` parameter is specified. The subsequent `checklimit` statements disable the asserts specified in the `disable` parameter and then enable the asserts specified in the `enable` parameter based on the first `checklimit` statement. Note that you cannot disable the check on constant parameters that Spectre runs during initial setup.

When multiple `checklimit` statements refer to the same assert, the last `checklimit` statement overrides the previous statements.

The syntax for a `checklimit` statement is

```
Name checklimit [enable=["check1" "check2" ... "checkn"]]
[disable=["check1" "check2" ... "checkn"]]
[start=value] [stop=value]
[check_windows=[start1 stop1 start2 stop2 ...]]
[boundary_type= time | sweep]
[severity= none | notice | warning | error | fatal]
[checkallasserts= yes | no]
[asserts=[assert1 assert2...]
[param= name[
[value= value]]
[filter= none | progressive | extreme]
```

where

[illegible]

```
enable=["check1" "check2" ... "checkn"]
```

Specifies the checks to be enabled. By default, all the checks are enabled. Wildcards are supported.

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`disable=[ "check1" "check2" ... "checkn" ]]`

Specifies the checks to be disabled. By default, none of the checks are disabled. Wildcards are supported.

`start=value`

The beginning point at which the specified check is to be enabled or disabled.

`stop=value`

The end point at which the specified check is to be enabled or disabled.

`check_windows=[ start1 stop1 start2 stop2 ...]`

Time or sweep windows within which the assert is to be enabled or disabled. The `boundary_type` parameter determines whether the `start` and `stop` values apply to time or sweep.

**Note:** Ensure that the array has an even number of values.

`boundary_type= time | sweep`

Determines whether the start and stop values for the `check_windows` parameter applies to time (used for transient analyses) or sweep (used for DC sweep and AC analyses).

Default: `time`

`severity=none | notice | warning | error | fatal ]`

Severity level of the message if the check fails. This overrides the severity levels specified for individual assert checks. If you set the severity to `none`, the severity level depends on the assert settings.

Default: `none`

**Note:** The specified severity level cannot change the violation level for the checks done during the initial setup stage because no checklimit analysis is done during the initial setup stage.

`checkallasserts=yes | no`

Enables or disables all the assert checks in the netlist. This parameter is ignored if both the `enable` and `disable` parameters are specified.

`asserts`

Specify a group of asserts whose parameters (specified using the `param` parameter) and values (specified using the `value` parameter) need to be changed.

`param`

Specifies the parameter setting for an individual assert or a group of asserts specified using the `asserts` parameter.

**Note:** If an assert has its own parameter setting, then its own setting is effective, otherwise, it uses the global parameter setting. See Example 2 below.

You can use the `param` parameter to change the value of the following parameters of the `assert` statement: `max`, `min`, `check_windows`, `maxvio_perinst`, `maxvio_all`, `duration`, `level`, `extreme`, and `skip_dev_inside_subckt`. Other assert parameters are not supported.

`value`

Specifies the value of the parameter (specified using the `param` parameter) for the assert (specified using the `asserts` parameter) that needs to be changed.

`filter`

Reduces the number of violations generated from an assert to the most significant ones. Possible values are `none`, `progressive`, and `extreme`. The default value is `none`.

When `filter=none` is specified, all violations are reported.

When `filter=progressive` is specified, a violation is generated for a given assert on a design instance, if any of the following condition is met:

- its duration is longer than any previous duration
- its absolute overshoot/undershoot is larger than any previous overshoot/undershoot
- its area estimate (area estimate=duration\*(overshoot/undershoot)) is greater than any previous area estimate

**Note:** The `filter=progressive` parameter only applies to simple asserts (for example, `vgs>...`) and not complex asserts (for example, `vgs >... & vds>...`).

When `filter=extreme` is specified, then, for a given assert on a design instance, the following is reported:

- the top peak violation, the top duration violation, and the top area violation
- For a one-sided assert (min or max), a maximum of three violations are reported
- For a two-sided assert (min and max checking), a maximum of six violations are reported
- If one violation has a max in peak and area, peak and duration, or area and duration, then, fewer violations are reported

For information on defining asserts, see [The assert Statement](#).

## Examples of checklimit Statement

### Example1

This section displays the cumulative effect of the checklimit statements. By default, all asserts are enabled.

```
//assert1, assert2, assert3, assert4, and
//Mychecklimit1 appear in include file "model1"
//assert5, assert6, and assert7, and Mychecklimit2
//appear in include file "model2"
//Mychecklimit3 and Mychecklimit4 appear in the netlist containing
//include files "model1" and "model2"

Mychecklimit1 checklimit disable=["assert2" "assert5"]
```

disables assert2 and assert5 and keeps assert1, assert3, assert4, assert6, and assert7 enabled. This condition remains in effect until the next checklimit statement is found.

```
Mychecklimit2 checklimit enable=["assert2" "assert6"] disable=["assert7"]
start=1ns stop=5ns severity=warning
```

specifically enables assert2 and assert6 thereby disabling all the other asserts. assert2 and assert6 are run within 1ns and 5ns, and a warning is displayed if the asserts are violated.

```
Mychecklimit3 checklimit disable =["assert2"] start=5ns stop=10ns severity=none
dcOp dc
```

Now assert6 is checked within 5ns and 10ns. The severity level is disabled in this checklimit statement, so assert6 determines the severity level if this check is violated. The simulator runs the DC analysis and checks only assert6. Since this is a DC analysis, the start and stop parameters are ignored.

```
Mychecklimit4 checklimit checkallasserts=yes disable =["assert1"]
start=1ns stop=10ns
tran1 tran stop=10ns
```

enables all asserts except assert1 and checks them within 1ns and 10ns.

```
Mychecklimit5 checklimit checkallasserts=no enable=["assert7"] check_windows=[1
3 5 7 9 10] boundary_type=sweep
dcswp dc param=vdc start=1 stop=10 step=1
```

checks assert7 when the netlist parameter vdc is varied from 1 to 3, 5 to 7, 9 to 10 for the DC sweep analysis.

```
Mychecklimit6 checklimit checkallasserts=no enable=["assert3" "assert4"]
check_windows=[1n 3n 5n 7n 9n 10n] boundary_type=time
tran1 tran stop=10ns
```

checks assert3 and assert4 from 1ns to 3ns, 5ns to 7ns, 9ns to 10ns for the transient analysis with stop time at 10ns.

### **Example2**

```
set1 checklimit asserts=[assert1 assert2 assert3] param=check_windows value=[0 20n]
set2 checklimit asserts=[assert3 assert4 assert5] param=check_windows value=[20n 40n]
set3 checklimit checkallasserts=yes check_windows=[0n 30n]
set4 checklimit checkallasserts=yes check_windows=[10n 30n]
```

In the above example, the `set1 checklimit` statement sets the `check_windows` parameter for the asserts `assert1`, `assert2`, and `assert3` to `[0 20n]`. The `set2 checklimit` statement sets the `check_windows` parameter for the asserts `assert3`, `assert4`, and `assert5` to `[20n 20n]`. Note that the `set2 checklimit` statement will override the value of `assert3` specified in the `set1 checklimit` statement. Therefore, the value of `check_windows` for `assert3` will be `[20n 40n]`.

The `set3 checklimit` statement sets the `check_windows` parameter for all asserts to `[0n 30n]` but the `set4 checklimit` statement overrides the `set3` statement and sets the `check_windows` parameter for all asserts to `[10n 30n]`.

If all the above `checklimit` statements are specified together, the `check_windows` setting for `assert1` and `assert2` will be `[0 20n]` and the `check_windows` setting for `assert3`, `assert4`, and `assert5` will be `[20n 40n]`. The `check_windows` setting for all other asserts would be `[10n 30n]`.

## Global Options

You can customize the behavior of the `assert`, `check`, and `checklimit` statements by setting the following options in the `options` statement:

- `asserts_silent_init`
- `checklimit_skip_insts`
- `checklimit_skip_insts_file`
- `checklimitdest`
- `devcheck_stat`
- `expr_reltol`
- `mod_assert_expand_sub`
- `wfdebug`

### **`asserts_silent_init`**

Enables or disables printing of warning messages during initialization in the log file. You can selectively enable or disable warnings for different types of asserts.

For example, you can disable warnings from PDK assert when a PDK subckt is not placed in the schematic and enable the warnings for custom asserts.

Asserts in PDK (subckt) generate the following warnings whenever a PDK subckt is NOT placed in the schematic:

```
WARNING (SPECTRE-16460): assert_PDK:Specified subcircuit master `xxx was not found.
WARNING (SPECTRE-16462): assert_PDK>Error in specification of subcircuit master.
Assert is ignored.
```

There can be thousands of such warning messages in the log file. You can disable these warnings from PDK assert by using this global option along with an assert name or a group name.

When multiple types of asserts are used, use the group parameter to distinguish PDK asserts from custom asserts.

The default value of group is `default`. Therefore, assert `assert_PDK` in the following example belongs to a group called `default`.

```
assert_PDK assert sub=xxx expr="v(1,0) >2.5" message="<<<<< PDK assert >>>>>"
level=warning
```



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The following example adds the `assert_custom` assert to a group called `custom` and enables warning messages.

```
assert_custom assert group=custom sub=res expr="V(in) >2.5" message="<<<<< custom
assert >>>>>" level=warning
assert_1 assert group=pdk other sub=inv expr="V(out) >2.5" message="<<<<<
group=default assert >>>>>" level=warning
assert_2 assert group=pdk other sub=inv expr="V(out) >2.5" message="<<<<<
group=default assert >>>>>" level=warning
```

The global option `asserts_silent_init` can be used to the disable warning messages by group name or assert name. The following example disables warnings from `assert_PDK` and `assert_1` during initialization.

```
opts options asserts_silent_init=["group=default" assert_1]
```

**Note:** When using the group option, the value must be specified within double quotes because `=` is a meta character.

## checklimit\_skip\_insts

Specifies the subcircuit instances that need to be skipped from assert verification. This option supports wildcards.

The following example skips subcircuit instance `XINV1` during assert checking.

```
assertopt options checklimit_skip_insts=[XINV1]
```

## checklimit\_skip\_insts\_file

Specifies the name of the file that contains the names of the subcircuit instances to be skipped during assert checking. This option supports wildcards.

Example:

```
assertopt1 options checklimit_skip_insts_file=assert_skip.txt
```

## checklimitdest

Specifies the destination where violations are to be written in the raw directory.

```
checklimitdest=file | psf | sqldb | both
```

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The values for the `checklimitdest` option are described below.

| Value              | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>file</code>  | <p>Writes the violations information to a file. You can use the <code>checklimitfile</code> option to specify the dedicated file name. If the <code>checklimitfile</code> option is not specified, by default, the violations are written to the Spectre log file.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>psf</code>   | <p>Writes the detailed violations information for each analysis type into the <code>.violations</code> and <code>.sqldb</code> files in the raw directory.</p> <p>For example, the violations information for a transient analysis run is written to a <code>tranViolations.violations</code> file in the raw directory, DC analysis runs to a <code>dcOpViolations.violations</code> file, DC sweep analysis runs to a <code>dcViolations.violations</code> file, AC analysis run to a <code>acViolations.violations</code> file, and so on. For more information about the format of violations in the <code>.violations</code> file, see <a href="#">Format of Violations in the .violations File</a>.</p> <p><b>Note:</b> By default, the <code>.violations</code> file is created in the PSF binary format. Use the <code>rawfmt=psfascii</code> option to create the file in ASCII format.</p> <p><b>Note:</b> Support for the <code>psf</code> option will be discontinued in a future release.</p> |
| <code>both</code>  | <p>Writes the violations information to both file and <code>.sqldb</code> file in the raw directory.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <code>sqldb</code> | <p>Writes the detailed violations information for each analysis type into a <code>.sqldb</code> file in the raw directory.</p> <p>The default value for the <code>checklimitdest</code> option is <code>sqldb</code>.</p> <p>For more information about the format of violations in the <code>sqldb</code> file, see <a href="#">Format of Violations in the sqldb File</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Note:** For assert level `none`, `notice`, or `warning`, the violations are written according to value specified for the `checklimitdest` option. However, for assert level `error` and `fatal`, the violation information is always written to a file regardless of the setting of the `checklimitdest` option.

## ***Format of Violations in the .violations File***

The following example of a violation written in the .violations file describes how you can find the instance name for which the violation is reported, the violation start value, margin value, violation start point, violation end point and violation status. Click on the links next to each line in the example for more information:

```
"check6.I1.Q0.violation1" "violation" <-- Violation name
-4.955361033925568e-02 <-- Violation Start Value
4.955361033925568e-02 <-- Margin
1.237567063989001e-08 <-- Violation Start Point
1.588944803644453e-08 <-- Violation End Point
4.744540579920873e-02 <-- Violation End Value
1.237567063989001e-08 <-- Peak Step Value
-4.955361033925568e-02 <-- Peak Value
3.513777396554524e-09 <-- Duration Value
0.000000000000000e+00 <-- Minimum Bound Value
NaN <-- Maximum Bound Value
-4.955361033925568e-02 <-- Average Value

) PROP (
"assert" "check6"
"instance" "I1.Q0" <-- Instance name
"model" ""
"severity" "warning"
"status" "failed" <-- Violation status
```

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The description of the violation is given below.

| Value                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Violation Name        | <p>Name of the violation.</p> <p>The violation name is written in the following format:</p> <pre>&lt;assertName&gt;.&lt;instName&gt;.violation&lt;localNumber&gt;</pre> <p>For example, in the violation name <code>check1.M1.violation2</code>,</p> <ul style="list-style-type: none"><li>■ <code>check1</code> is assert name defined in the netlist.</li><li>■ <code>M1</code> is the instance that violates the check.</li><li>■ <code>violation2</code> is the second violation reported for <code>check1</code> on instance <code>M1</code>.</li></ul> |
| Violation Start Value | The start value of a violation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Margin                | <p>The difference between the violation start value and the <code>min</code> or <code>max</code> parameter values.</p> <p><b>Note:</b> The margin value for a violation reported for a boolean expression assert will be <code>NaN</code> because the <code>min</code> and <code>max</code> parameters are ignored for boolean expression asserts.</p>                                                                                                                                                                                                       |
| Violation Start Point | The abscissa of violation start value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Violation End Point   | The abscissa of violation end value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Violation End Value   | The end value of a violation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Peak Step Value       | Time step during the peak value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Peak Value            | Peak value of the violation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Duration Value        | Time period of the violation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Minimum Bound Value   | Lower limit of the parameter value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Maximum Bound Value   | Upper limit of the parameter value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Average Value         | Average value of the violation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Instance Name         | The name of the instance that violates the check.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

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| Value            | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Violation Status | Violations with the <code>failed</code> status are written to the <code>.violations</code> file. A violation has a failed status if it violates the current analysis or is not processed because the <code>level</code> parameter in the <code>assert</code> statement or the <code>severity</code> parameter in the <code>checklimit</code> statement has the value <code>error</code> or <code>fatal</code> . |

### Format of Violations in the `sqldb` File

The following example of a violation written in the `.sqldb` file describes how you can find the instance name for which the violation is reported, the violation start time, violation start value, duration, end value, and violation end time.

```
% sqlite3 input.sqldb
% select * from assert_0View;
```

|               |                      |                                                                        |
|---------------|----------------------|------------------------------------------------------------------------|
| ID            | = 1                  | ID of the assert violation                                             |
| Checker Name  | = check6             | Name of the assert                                                     |
| Instance      | = I1.Q0              | Name of the instance                                                   |
| Model=nch     | = nch                | Model name of the device                                               |
| Start Value   | = -4.95536103392e-02 | Start value of the violation                                           |
| Margin=       | = 4.95536103392e-02  | Margin                                                                 |
| StartTime (s) | = 1.23756706398e-08  | Start time of the violation                                            |
| Duration (s)  | = 3.51377739655e-09  | Duration of the violation                                              |
| EndTime (s)   | = 1.58894480364e-08  | End time of the violation                                              |
| EndValue      | = 4.74454057992e-02  | End value of the violation                                             |
| AvgValue      | = -4.9553610339e-02  | Average value of the violation                                         |
| ViolationType | = upper              | upper when max value is violated and lower when min value is violated. |
| PeakStep      | = 1.23756706398e-0   | Time step at peak value                                                |
| PeakValue     | = -4.9553610339e-02  | Peak value                                                             |
| Dissatisfied  |                      | Contains part of the boolean assert expression which was dissatisfied  |

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The detailed schema can be found at the following location:

```
<MMSIM_install_dir>/tools.lnx86/spectre/etc/ade/mmSQLSchema.sql
```

## devcheck\_stat

Specifies whether to display device-checking statistics on the terminal and added to the log file. By default, this option is set to `none` and statistics messages are not displayed. Set this option to `inst` or `sub` to display statistics messages while keeping the checks on.

Possible values for this option are:

- `none`: Does not print any information related to asserts on the screen or in the log file.
- `inst`: Displays the asserts on an instance basis. In addition, information related to whether an assert is on or off is also printed on the screen and in the log file.
- `sub`: Displays the number of enabled asserts only per subcircuit per assert name. For asserts outside the subcircuit, only the assert name is printed. For asserts inside the subcircuit, the name of the subcircuit, followed by the assert name, and the number of occurrences of the enabled assert are printed. For asserts inside a nested subcircuit, the subcircuit hierarchy is prefixed before the assert name.

For example, when `devcheck_stat=inst`, Spectre displays the following device-checking statistics before the analysis:

```
The following asserts will be enabled for all subsequent analyses until the next
checklimit analysis statement is found:
```

```
assert1 : ON
X1.assert2 : ON
X1.assert3 : ON
X2.assert2 : ON
X2.assert3 : ON
```

Consider X1 and X2 are instance of subckt sub1. When `devcheck_stat=sub`, the following statistics will be printed:

```
The following asserts will be enabled for all subsequent analyses until the next
checklimit analysis statement is found:
```

```
assert1 : ON
X1.X2:assert2 : ON
```

You can disable the display of these statistics by setting devcheck\_stat to `none`.

## **expr\_reltol**

Defines the relative tolerance for expressions. The default value of `expr_reltol` is `1e-12`. Set this option in scenarios when the evaluation of equations that compare numbers may generate wrong results because the simulator introduces numerical noise.

For example, the following assert statement checks for the device length `l` of `6nm`. However, if `l` is stored with the value `5.99999999999` in the simulator database, the assert is not be triggered.

```
check_l assert primitive=nmos expr="(l==6n)" level=warning
```

Example:

```
opt1 options expr_reltol=1e-12
```

## **mod\_assert\_expand\_sub**

Specifies whether to automatically detect the `mod` or `sub` usage for the model card and subcircuit.

Spectre asserts use the `mod=nch` parameter to apply asserts to devices with the device model name `nch`. By default, the `mod` parameter does not apply to device model subcircuit or inline subcircuit names. You can set the value of the `mod_assert_expand_sub` netlist option to `yes` so that Spectre assert automatically detects the `mod` or `sub` usage for the model card and subcircuit.

```
opt1 options mod_assert_expand_sub=yes
```

With the `mod_assert_expand_sub` option set to `yes`, the `mod` parameter is applied to the device model or inline subcircuit names if no model statement with the specified name is found.

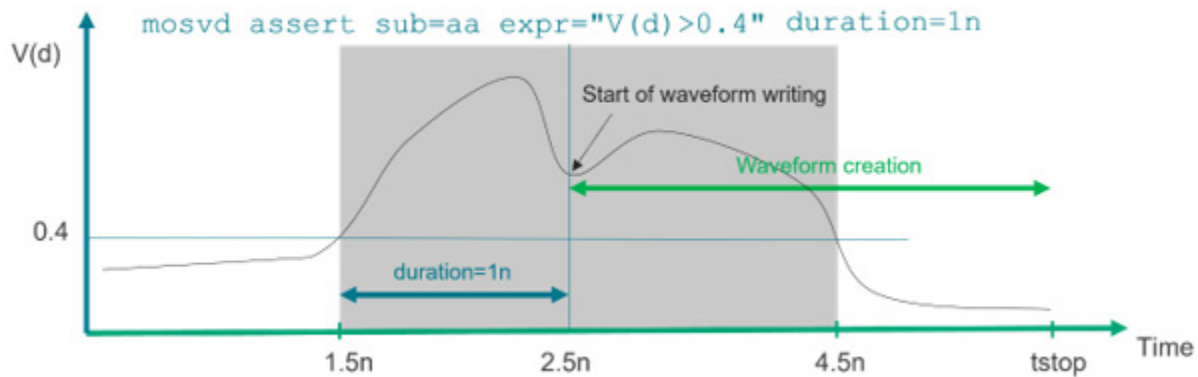
```
assert_mod mod=nch expr="V(inm)" max=-100
```

A warning is generated if `nch` is not a model or a subcircuit name.

## **wfdebug**

Specifies whether to store all time-varying current (`R1:in`) and voltage (`M1:d`) waveforms used in an assert expression. Differential voltages like `V(d,s)` used in asserts are saved as individual voltage signals `V(d)` and `V(s)`.

Spectre starts saving a waveform only when the assert criteria is satisfied.



When the waveform writing is enabled, it remains enabled till the simulation ends. For any assert without violation, no waveform is saved. For large designs and many asserts, the `wfdebug=assert` option may save a large number of waveforms, which may significantly degrade Spectre performance.

Any expression using the `avg()` and `rms()` functions will only be triggered at the end of transient analysis. There is no violation during transient analysis. Therefore, the related signal will not be saved because `wfdebug` will not know until at the end of transient analysis if violation criteria is satisfied or not.

For example:

```
assertopt options wfdebug=assert
```



## Circuit Checks

Circuit checks enable you to analyze typical design problems, such as high impedance nodes, leakage paths between power supplies, timing errors, power issues, connectivity problems, or extreme rise and fall times. They can be separated into dynamic and static checks. Dynamic checks are performed during transient analysis. Static checks are topology checks which do not require any simulation.

### Circuit Check Scoping

Most circuit checks can be applied either globally to the entire design, or locally to specific blocks of a design. The scoping options are available to define the scope of each circuit check. The circuit checks can be applied to a specific subcircuit instance (`inst`), or to all instances of a subcircuit definition (`subckt`). Exclusion of a specific subcircuit instance (`xinst`), or all instances of a subcircuit (`xsubckt`) is supported. All scoping options support wildcards, and the hierarchy level of the scope can be defined by the `depth` option.

|                      |                                                                                                                                  |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>    | Non-hierarchical node name. Default is <code>none</code> .                                                                       |
| <code>net</code>     | Hierarchical node names between which leakage path is checked. Wildcards are not supported. Default is <code>none</code> .       |
| <code>dev</code>     | Non-hierarchical element name. Default is <code>none</code> .                                                                    |
| <code>model</code>   | Non-hierarchical model name. Default is <code>none</code> .                                                                      |
| <code>inst</code>    | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                       |
| <code>xinst</code>   | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                    |
| <code>subckt</code>  | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                |
| <code>xsubckt</code> | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                 |
| <code>depth</code>   | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8. |

**Note:** The `inst` and `xinst` arguments can only be used to specify subcircuit instances, and not device instances.

Combination of `inst/xinst` and `subckt/xsubckt` is not allowed.

Following wild cards are allowed for `node`, `dev`, `model`, `inst`, `xinst`, `subckt`, and `xsubckt`:

- \* – matches any character including an empty string and . (dot)
- ? – matches any single character including space and . (dot)

## Depth and inst/subckt Scoping

When using a combination of the `inst/subckt` scoping with wildcarding and the `depth` option, the following rules apply:

- Depth is applied first.

The number defined in `depth` (`depth=n`) defines the number of maximum dots in the selected net or element names. Basically, the top level and `n` additional levels are selected. For example, for `depth=3`:

- Nets selected
  - Top level: `net5`
  - three levels below: `x1.net2`, `x1.x2.net4`, `x1.x2.x3.net8`

- `inst` (or `subckt`) scope is applied second

- if `inst=x1.x2` then
  - Nets selected: `x1.x2.net4`, `x1.x2.x3.net8`
  - Nets not selected: `net5`, `x1.net2`, `x1.x2.x3.x4.net6`

## Circuit Check Scoping Examples

```
...node=[*] inst=[*] depth=3
```

Matches any node on the top four hierarchy levels of the design (top + 3 levels)

```
...node=[*] inst=[x1]
```

Matches any node inside the subcircuit instance `x1` and its child instances

```
...node=[*] inst=[x1.*]
```

Matches any node which is part of the child instances of `x1`, but not nodes inside `x1` itself

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|                                                              |                                                                                                                                                                                           |
|--------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>...node=[n1*] inst=[x1.x2]<br/>xinst=[x1.x2.x3]</code> | Matches <code>x1.x2.n11</code> , <code>x1.x2.x4.n12</code> ,<br><code>x1.x2.x4.x5.x6.n15</code><br><br>Does not match <code>x1.x2.x3.n12</code> , <code>x1.n1</code>                      |
| <code>...dev=[R*] inst=[x1 x2.x3] depth=3</code>             | Matches <code>x1.R5</code> , <code>x1.x2.R19</code> ,<br><code>x1.x2.x3.R88</code><br><br>Does not match <code>R15</code> ,<br><code>x1.x2.x3.x4.R12</code> , <code>x2.x3.x5.x6.R9</code> |
| <code>...model=[nf pf] inst=[x1.x2]</code>                   | Matches any model instantiation of <code>nf</code><br>and <code>pf</code> inside <code>x1.x2</code> .                                                                                     |
| <code>...node=[*] subckt=[pll] xsubckt=[vco]</code>          | Matches all nodes inside all instances of<br>the <code>pll</code> subcircuit, except the nodes<br>inside the instances of the <code>vco</code><br>subcircuit.                             |
| <code>...node=[*] inst=[x1.x2] subckt=[vco]</code>           | Combination of <code>inst</code> and <code>subckt</code> is not<br>allowed.                                                                                                               |
| <code>...node=[*] inst=[x1.x2] xsubckt=[vco]</code>          | Combination of <code>inst/xsubckt</code> , or<br>combination of <code>subckt/xinst</code> is not<br>allowed.                                                                              |

## Specifying the Output Format for the Checker Violation Report

To specify the output format for the checker violation reports:

- ➔ Set the `check_format` parameter of the `options` statement

Possible values of the `check_format` parameter are:

- ☐ `sql`: Saves the report in `sqldb` format that is saved in a file with extension `.sqldb`.
- ☐ `xml`: Saves the report in both `sql` and XML formats. The report in the XML format is saved in a file with extension `.xml`. This the default value of the `check_format` parameter.
- ☐ `text`: Saves the report in both `sql` and text formats. The report in the text format is saved in a file with extension `.rpt`.
- ☐ `all`: Saves the report in all formats: `sqldb`, text, and XML

All the reports are saved in the `raw` directory.

Examples:

Spectre syntax to specify the output format:

```
opt options check_format=text
```

SPICE syntax to specify the output format:

```
.option check_format=text
```

## Circuit Check SpiceVision PRO Integration

The dynamic and static circuit checks report design errors on circuit nodes, devices, and elements. A SpiceVision PRO integration is available that enables you to quickly browse the schematic for nodes, devices, and elements reported in the design check error report. SpiceVision PRO, a product of Concept Engineering GmbH, reads the SPICE or Spectre netlists and generates clean, easy-to-read transistor-level schematics, and circuit fragments to speed up circuit debugging. Use the workshop database located under `<MMSIM>/tools.lnx86/SpiceVision` to learn more about the integration. The integration requires a SpiceVision PRO license which can be obtained from Concept Engineering GmbH.

## MonteCarlo Sweep and Alter Support in Dynamic Checks

Dynamic design checks support multiple simulations due to MonteCarlo, sweep, and alter. The design check is applied to each individual MonteCarlo, sweep, and alter simulation. Following are the limitations:

- Altering the design check parameters between (MC, altered, or swept) simulations is not supported.
- While the text report shows the individual run that caused the check error, the XML report does not report the individual run.

## Changing Default Value of Parameters

Most circuit check parameters have an associated default value. To change the default value, you need to specify a different value for the parameter in the circuit check statement. However, if you want to use a different default value for a parameter every time you run a circuit check, specify the value in a file and use the `+paramdefault <filename>` command-line option to enable Spectre to read and apply the default values from the specified file.

Here, `<filename>` is the name of the file containing the default value of parameters. The file should only contain the primitive circuit check name, parameter name, and the parameter value in one line. For example:

```
dyn_floatdcpath ith 1n
static_highz vnth 0.3
```

For more information, see [Specifying Parameter Defaults in a File](#) on page 253.

## Circuit Check Syntax

All circuit checks follow Spectre syntax and can be written only in Spectre syntax (not SPICE syntax). Therefore, you must follow the syntax rules that apply to Spectre (see [Basic Syntax Rules](#) on page 139). If using design checks in a SPICE format netlist, you must specify `simulator lang=spectre` before any circuit check statement (see [Spectre Language Modes](#) on page 139). For example, the following is the syntax for the `dyn_highz` check in Spectre format with line continuation:

```
simulator lang=spectre
chk1 dyn_highz node=[*] inst=[alpha beta gamma pll]
```

A mathematical expression can be used by encapsulating the expression in round brackets ([Expressions](#)). You can also use `.PARAM` in the mathematical statements. For example:

```
simulator lang=spice
.param PER = 50n
simulator lang=spectre
parameter NUM = 10
dcpath1 dyn_dcpath duration=(1n+PER/2) time_window=[0n (NUM*PER/2)] ...
```

The rules of referencing SPICE syntax in the circuit check statements are the same as referencing SPICE syntax in Spectre `save` statement. For example:

```
simulator lang=spice
r1 node<1> node[2] 1k

simulator lang=spectre
save node\<1\>
save node\[2\]
chk1 dyn_highz node=[node\<1\>] ...
Chk2 dyn_subckpwr port=[AD\[1\]] ...
```

## Dynamic Checks

Dynamic checks are performed during transient simulation and are dependent on the stimuli. The checks use the `dyn_` prefix as part of the circuit check keyword, and write the report into a file with the extension `.dynamic.xml`. The xml file can be viewed with any Web browser.

The following table lists the checks that are supported in Spectre®, Spectre® APS, Spectre X, Spectre® XPS SPICE mode, Spectre® XPS FastSPICE mode, and Spectre® MS mode (see [Chapter 4, “The Spectre XPS Circuit Simulator”](#)):

**Table 16-1 Dynamic Checks Supported in Various Modes**

| Name                                                             | Spectre,<br>Spectre APS,<br>Spectre X                                                           | Spectre<br>XPS<br>SPICE | Spectre<br>XPS<br>FastSPICE<br>(SRAM,<br>DRAM,<br>Flash) | Spectre<br>MS |
|------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|-------------------------|----------------------------------------------------------|---------------|
| <a href="#">Dynamic High Impedance Node Check</a>                | Yes                                                                                             | Yes                     | Yes                                                      | Yes           |
| <a href="#">Dynamic DC Leakage Current Path Check</a>            | Two approaches. See <a href="#">Transient and Leakage Analysis Based Approaches</a> on page 689 |                         |                                                          |               |
| <a href="#">Dynamic Floating Gate Induced Leakage Path Check</a> | Two approaches. See <a href="#">Transient and Leakage Analysis Based Approaches</a> on page 694 |                         |                                                          |               |
| <a href="#">Dynamic MOSFET Voltage Check</a>                     | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Resistor Voltage Check</a>                   | No                                                                                              | No                      | Yes                                                      | No            |
| <a href="#">Dynamic Capacitor Voltage Check</a>                  | No                                                                                              | No                      | Yes                                                      | No            |
| <a href="#">Dynamic Diode Voltage Check</a>                      | No                                                                                              | No                      | Yes                                                      | No            |
| <a href="#">Dynamic Excessive Element Current Check</a>          | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Excessive Rise and Fall Time Check</a>       | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Glitch Check</a>                             | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Setup and Hold Check</a>                     | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Noisy Node Check</a>                         | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Node Capacitance Check</a>                   | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Subcircuit Port Power Check</a>              | Yes                                                                                             | Yes                     | Yes                                                      | Yes           |
| <a href="#">Dynamic Pulse Width Check</a>                        | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Power Density Check</a>                      | Yes                                                                                             | Yes                     | Yes                                                      | No            |
| <a href="#">Dynamic Active Node Check</a>                        | Yes                                                                                             | Yes                     | Yes                                                      | No            |

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| Name                                                 | Spectre,<br>Spectre APS,<br>Spectre X | Spectre<br>XPS<br>SPICE | Spectre<br>XPS<br>FastSPICE<br>(SRAM,<br>DRAM,<br>Flash) | Spectre<br>MS |
|------------------------------------------------------|---------------------------------------|-------------------------|----------------------------------------------------------|---------------|
| <u>Dynamic Subcircuit Instance Activity Check</u>    | No                                    | No                      | Yes                                                      | No            |
| <u>Dynamic Subcircuit Port Voltage/Current Check</u> | No                                    | No                      | Yes                                                      | No            |
| <u>Dynamic Delay Check</u>                           | Yes                                   | Yes                     | Yes                                                      | No            |
| <u>Dynamic Floating Node Statistical Check</u>       | Yes                                   | No                      | No                                                       | No            |
| <u>Dynamic Uninitialized Check</u>                   | No                                    | No                      | Yes                                                      | No            |

## Dynamic High Impedance Node Check

### Syntax

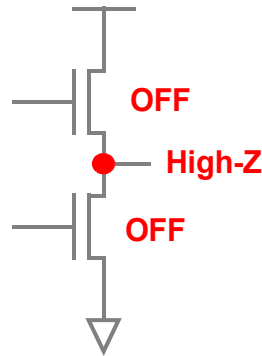
```

title dyn_highz node=[n1 n2 ...] duration=<value> time_window=[start1 stop1
 start2 stop2] <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]>
 <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> <depth=n>
 error_limit=<value> rest_th_va=<value> res_th=<value> isource_ith=<value>
 bjt_vbe=<value> bjt_ith=<value> diode_vth=<value> <inverse=no|yes>
 <sort=no|duration>
 <fanout=all|gate|bulk|gate_has_driver_no_moscap|gate_no_moscap>
 <filter=[no|rc]> <xnode=[node1 node2...]> xnode_file=<value>
 <nonconducting_subckt=[subckt1 subckt2...]> <conducting_subckt=[subckt1
 subckt2...]> <debug_net=[net1 net2...]> <debug_time=[t1 t2...]>
 <debug_format=txt|sql|both> <debug_report=lowz|highz|both>

```

## **Description**

Reports the nodes that are in high impedance state (also known as floating) for a duration longer than the user-defined threshold. A high impedance state occurs when there is no conducting path from the node to any power supply or ground.



The following device conditions are used:

- MOSFET is conducting if `region` is either `triode` or `saturation`.
- Resistors, controlled resistors, `phy_res`, `relay`, and inductors are conducting if `R <= res_th`.
- BJT is conducting if `vbe > bjt_vbe` or `ic > bjt_ith`.
- Diode is considered to be conducting if `v > diode_vth`.
- `Vsource` and `iprobes` are conducting.
- `Isource`, `VCCS`, and `CCCS` are conducting if `i > isource_ith`.
- JFET is considered to be conducting.
- Mutual inductor and controlled capacitors are considered to be non conducting.
- Verilog-A: Conducting path depends on the module details.

The results are written to the `dynamic.xml` file, which can be viewed in a Web browser.

## **Arguments**

### **Design Check Parameters**



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|             |                                                                                                                                                                                                                                                                           |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| node        | A space-separated list of names of the nodes to which the check is applied. Default is <code>none</code> . Wildcards are supported.                                                                                                                                       |
| xnode       | A space-separated list of names of the hierarchical nodes to be excluded from the check. Default is <code>none</code> . Wildcards are supported.                                                                                                                          |
| xnode_file  | File containing the names of the hierarchical nodes that need to be excluded from the check. Wildcards are not supported. Default is <code>none</code> .                                                                                                                  |
| duration    | HighZ states with a duration longer than value are reported (default is <code>5ns</code> ).                                                                                                                                                                               |
| bjt_vbe     | BJT vbe conducting threshold. Default is <code>0.4V</code> .                                                                                                                                                                                                              |
| bjt_ith     | BJT ith conducting threshold. Default is <code>50nA</code> .                                                                                                                                                                                                              |
| res_th_va   | Verilog-A resistor conducting threshold for high impedance node detection. This parameter is applicable only on AMS <code>ie</code> element, and on one or two-port AHD module. Default is <code>10 MOhms</code> .                                                        |
| res_th      | Resistor conducting threshold. Default is <code>1TOhms</code> .                                                                                                                                                                                                           |
| isource_ith | Current source conducting threshold. Default is <code>1pA</code> .                                                                                                                                                                                                        |
| diode_vth   | Diode voltage conducting threshold. Default is <code>0.6V</code> .                                                                                                                                                                                                        |
| inverse     | If set to <code>no</code> , reports all nodes that are in highz state. If set to <code>yes</code> , reports all nodes that are not in highz state. Possible values are <code>no</code> and <code>yes</code> . Default is <code>no</code> .                                |
| sort        | Sort the violations. If set to <code>no</code> , no sorting is performed. If set to <code>duration</code> , violations are sorted based on <code>duration</code> . Possible values are <code>no</code> and <code>duration</code> . The default value is <code>no</code> . |
| debug_net   | Hierarchical nets to debug. Wildcard is not allowed. Default is <code>none</code> .<br><br><b>Note:</b> This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre XPS SPICE mode.                                                                     |
| debug_time  | Time points at which the debug report is generated. Default is <code>none</code> .<br><br><b>Note:</b> This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre XPS SPICE mode.                                                                      |

|              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| debug_format | <p>When debug_format=txt, the report is written to the &lt;netlistName&gt;_&lt;checkName&gt;_&lt;debug_time&gt;.report.log file in text format. The report contains all conducting paths from a debug net to ground causing the debug net to be a lowz node. The report also contains information about all devices that are off causing a debug net to be highz.</p> <p>When debug_format=sql, the report is written in xml/sql format. The report, in this case, only contains all conducting paths from a debug net to ground causing the debug net to be a lowz node.</p> <p>When debug_format=both, the report is written in all formats. Possible values are sql, txt, and both. Default is txt.</p> <p><b>Note:</b> This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre XPS SPICE mode.</p> |
| debug_report | <p>When debug_report=lowz, only lowz nodes are reported and the report contains all conducting paths from debug_net to ground, causing debug_net to be a lowz node.</p> <p>When debug_report=highz only highz nodes are reported and the report contains all devices that are off, causing debug_net to be highz.</p> <p>When debug_format=both, both lowz and highz nodes are reported.</p> <p>Possible values are lowz, highz, and both. The default value is both.</p> <p><b>Note:</b> This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre XPS SPICE mode.</p>                                                                                                                                                                                                                                  |

### Filtering Parameters

|             |                                                                                                                                           |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| time_window | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to tend. |
| error_limit | Maximum number of errors to be reported. Default is 10000.                                                                                |

`fanout` Fanout setting to filter node with specified connection. When `fanout=gate_has_driver_no_moscap`, floating nodes only connecting to MOSCAPs will not be checked. When `fanout=gate_no_moscap`, gates only connecting to MOSCAPs will not be checked. Possible values are `all`, `gate`, `bulk`, `gate_has_driver_no_moscap`, and `gate_no_moscap`. Default is `all`.

`filter` If set to `no`, filtering is not performed. If set to `rc`, `dyn_highz` checks only one node in the same parasitic sub. This option is supported only in Spectre XPS FastSPICE mode. Possible values are `no` and `rc`. The default value is `no`.

## Wildcard Scoping

`inst` Subcircuit instances to which the circuit check is applied. Default is `inst=*`.

`xinst` Subcircuit instances that are excluded from the circuit check. Default is `none`.

`subckt` Instances of the specified subcircuit to which the circuit checks are applied. Default is `subckt=*`.

`xsubckt` Instances of the specified subcircuit which are excluded from the circuit checks. Default is `none`.

`depth` Hierarchy level (from top level) to be checked. `depth=3` reports errors on top level plus 3 sublevels. Default is 8.

`nonconducting_subckt`

All instances of specified subcircuit are considered non-conducting during the floating node detection. All devices inside the subcircuit are considered non-conducting during the floating node detection. Wildcard is supported. Default is `none`.

**Note:** This option is supported only in Spectre, Spectre APS, and Spectre X.

`conducting_subckt`

All instances of specified subcircuit are considered conducting during the floating node detection. All devices inside the subcircuit are considered conducting during the floating node detection. Wildcard is supported. Default is `none`.

**Note:** This option is supported only in Spectre, Spectre APS, and Spectre X.

```
nonconducting_primitive=[...]
```

All instances of specified primitive or VerilogA modules are considered non-conducting during the floating node detection. Wildcard is supported. Default is none.

## Example

```
hz1 dyn_highz node=["*"] duration=2e-09 time_window=[1e-09 1e-08]
```

The above command will report all nodes that were in a high impedance state for a duration longer than  $2e-09s$  within the time window between  $1e-09s$  and  $1e-08s$ . The following is an example of the report that is displayed in the Web browser:

### Dynamic HighZ Node Check Violations

#### dyn\_highz: hz1

- hz1 dyn\_highz node=["\*"] duration=2e-09 time\_window=[1e-09 1e-08]
- Violation Count: 1

| Title | Node Name | Start(s)     | Duration(s)  |
|-------|-----------|--------------|--------------|
| hz1   | out       | 1.000000e-09 | 9.000000e-09 |

## Dynamic DC Leakage Current Path Check

### Syntax

```
title dyn_dcpath net=[n1 n2 ...] duration=<value> ith=<value> time_window=[start1
 stop1 start2 stop2 ...] <leaki_times=[t1 t2 ...]> <xinst=[xinst1 xinst2...]>
 error_limit=<value> <sort=no|current>
```

### Description

Reports the conductance paths between user-specified nets. This check can be used in two ways. One is based on transient-analysis and the other is based on leakage analysis. The check based on transient analysis reports qualifying paths carrying an absolute current higher than the parameter `ith` for a duration longer than the specified `duration`, within the specified `time_window`. The check based on leakage analysis reports qualifying paths carrying an absolute current higher than the parameter `ith` at specified `leaki_times`. `leaki_times` should be carefully selected in standby or power-down mode (see [XPS SRAM Leakage Current Simulation](#) on page 99). Both methods cannot be used in one check statement. If you specify both methods in one check statement, then leakage analysis gets higher priority than transient analysis.

The following table shows the Spectre modes in which the two methods are supported.

**Table 16-2 Transient and Leakage Analysis Based Approaches**

| Method                                                          | Spectre,<br>Spectre APS,<br>Spectre X | Spectre<br>XPS<br>SPICE | Spectre<br>XPS<br>FastSPICE<br>(SRAM,<br>DRAM,<br>Flash) | Spectre<br>MS |
|-----------------------------------------------------------------|---------------------------------------|-------------------------|----------------------------------------------------------|---------------|
| DC Leakage Current Path<br>Check based on transient<br>analysis | Yes                                   | Yes                     | Yes                                                      | Yes           |
| DC Leakage Current Path<br>Check based on leakage<br>analysis   | Yes                                   | Yes                     | Yes                                                      | No            |

If more than two nets are specified, Spectre checks the leakage path between each net combination. For example, if `net=[vdc1 vdc2 0]` is specified, then the conducting path between `vdc1` and `vdc2`, `vdc1` and `0`, and `vdc2` and `0` is checked.

High accuracy settings are recommended when using the Spectre XPS FastSPICE solver (`+cktpreset=sram_pwr`).

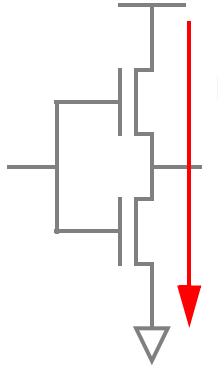
The results are written to a file with the extension `dynamic.xml`.

**Note:** The `dyn_dcpath` report can also list the iprobes added by the simulator. You can set the global option `check_dcpath_igniprobes=yes` to include the iprobes in the report. Only the iprobes added by the simulator (through `save` statement or `options` statement) are controlled by the `check_dcpath_igniprobes` option.

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By default, bulk current through the MOSFET is not traced. You can set the global option `dcpath_bulk_current=yes` to trace the bulk current.



## Arguments

|                          |                                                                                                                                                                                                                                        |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>net</code>         | Hierarchical node names between which the leakage path is checked. Wildcarding is not allowed. All combination of nets are checked. Default is none.                                                                                   |
| <code>duration</code>    | Leakage paths with a duration longer than specified value are reported (default is 5ns).                                                                                                                                               |
| <code>sort</code>        | If set to <code>no</code> , sorting is not performed. If set to <code>current</code> , the violations are sorted by max current. Possible values are <code>no</code> and <code>current</code> . The default value is <code>no</code> . |
| <code>ith</code>         | Leakage paths with absolute current higher than the specified value are reported (default is 50uA).                                                                                                                                    |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> .                                                                                |
| <code>leaki_times</code> | Defines the times at which the check is performed. This option is supported only in Spectre, Spectre APS, Spectre X, Spectre XPS SPICE, and Spectre XPS FastSPICE. It is not supported in Spectre MS.                                  |
| <code>xinst</code>       | Subcircuit instances to be excluded from the check. Default is none.<br><br><b>Note:</b> This parameter is supported only in Spectre XPS FastSPICE mode.                                                                               |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                                                                                                             |

# Spectre Classic Simulator, Spectre APS, Spectre X, Spectre XPS, Spectre FMC Analysis, and Legato Reliability Solution User Guide

## Example 1

```
dcpath1 dyn_dcpath ith=200u net=[vdd 0] duration=1n time_window=[1n 20n]
```

The above command will report the DC conductance path between `vdd` and `0`. The command will report the paths that carry current higher than `200u` for a duration longer than `1n` within the time window between `1n` and `20n`. The following is an example of the report that is displayed in the Web browser:

### Dynamic DC Leakage Path Check Violations

#### `dyn_dcpath: dcpath1`

```
dcpath1 dyn_dcpath ith=0.0002 duration=1e-09 net=["vdd" "0"] time_window=[1e-09 2e-08]
```

Violation Count: 1

#### Dynamic dcpath check based on transient analysis - Violation

| Title                | Path Id | From Net | To Net | Start(s)     | Duration(s)  |
|----------------------|---------|----------|--------|--------------|--------------|
| <code>dcpath1</code> | 0       | vdd      | 0      | 1.033403e-08 | 4.944546e-09 |

Dcpath datas: size=2

| Instance | Current(A)   |
|----------|--------------|
| MP1      | 2.944546e-04 |
| MN1      | 2.363355e-04 |

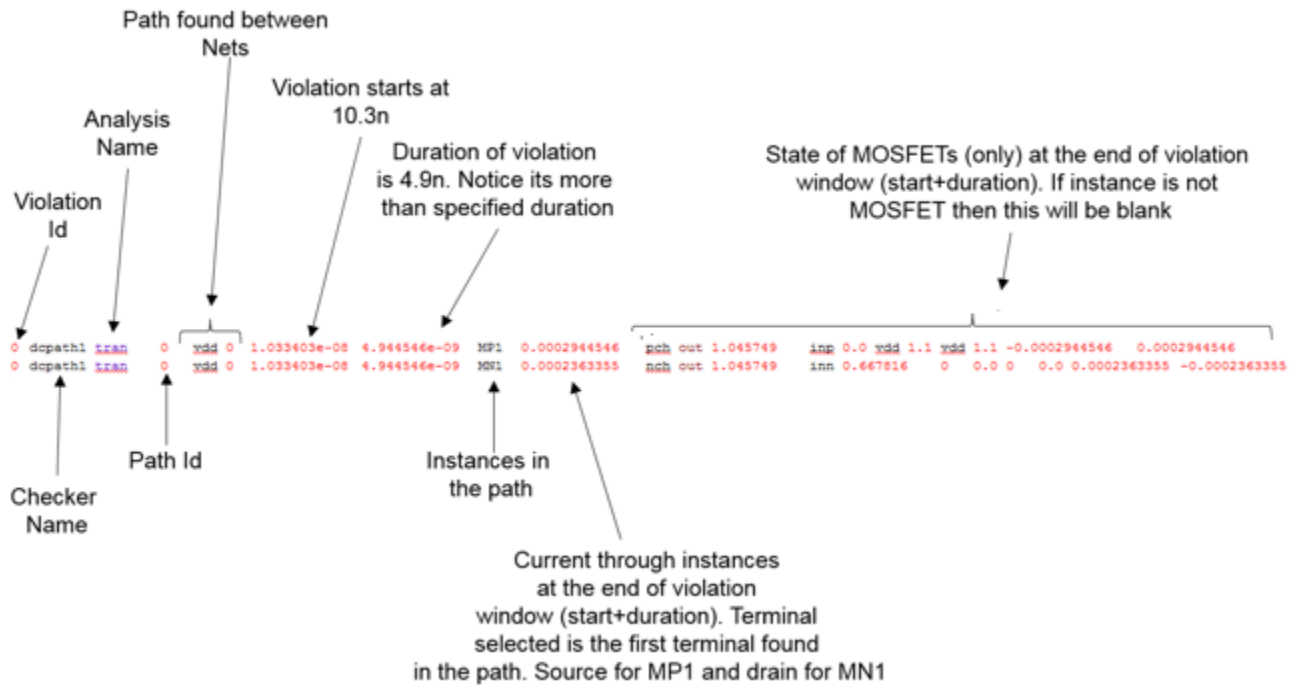
Elemstate datas: size=2

| Instance Name | Model | Drain Name | Drain Volt(V) | Gate Name | Gate Volt(V) | Source Name | Source Volt (V) | Bulk Name | Bulk Volt(V) | Drain Current (A) | Source Current(A) |
|---------------|-------|------------|---------------|-----------|--------------|-------------|-----------------|-----------|--------------|-------------------|-------------------|
| MP1           | pch   | out        | 1.045749e+00  | inp       | 0.000000e+00 | vdd         | 1.100000e+00    | vdd       | 1.100000e+00 | -2.944546e-04     | 2.944546e-04      |
| MN1           | nch   | out        | 1.045749e+00  | inn       | 6.678160e-01 | 0           | 0.000000e+00    | 0         | 0.000000e+00 | 2.363355e-04      | -2.363355e-04     |

The path report has three sections. Each section is explained below.

- The first section shows that a path is found starting from net `vdd` to net `0`. Since this is a check based on transient-analysis, the name of the table is *Dynamic dcpath check based on transient analysis*.
- The second section shows the actual instances in the path. The first column *Instance* contains instances in the path. The second column contains the current through the instances. The current is taken at the end of violation, that is, at  $1.52e-8$  seconds (start + duration =  $1.03e-8 + 4.94e-9$ ).
- The third section shows the state of MOSFETs in the path. It does not report anything other than MOSFETs. The first column *Instance Name* is the MOSFET name. The second column is the model name. The following columns are the terminal names and voltages. The last two columns show the drain and source terminal currents. The values are taken at the end of violation.

Similar to xml report, the text report is shown below:



Example 2

```
dcpath2 dyn_dcpath ith=200u net=[vdd 0] leaki_times=[12.5n]
```

The above command will report the DC conductance path between `vdd` and `0`. The command will report the paths that carry current higher than `200u` based on the leakage analysis done at time `12.5ns`. In the report, *Total Current* is the summation of all branch currents exiting



from the net `vdd`. The following is an example of the report that is displayed in the Web browser:

## Dynamic DC Leakage Path Check Violations

### dyn\_dcpath: dcpath2

dcpath2 dyn\_dcpath ith=0.0002 net=["vdd" "0"] leaki\_times=[1.25e-08]

Violation Count: 1

#### Dynamic dcpath check based on leaki analysis - Violation

| Title                   | Path Id | From Net | To Net | Violation Time (s) | Total Current (A) |
|-------------------------|---------|----------|--------|--------------------|-------------------|
| <a href="#">dcpath2</a> | 0       | vdd      | 0      | 1.250000e-08       | -9.548904e-04     |

#### Dcpath datas: size=2

| Instance | Current(A)    |
|----------|---------------|
| MP1      | -9.548903e-04 |
| MN1      | 9.548903e-04  |

Since this check is based on leakage analysis, the name of table is *Dynamic dcpath check based on leaki analysis*.

## Dynamic Floating Gate Induced Leakage Path Check

### Syntax

```
title dyn_floatdcpath net=[n1 n2 ...] node=[n1 n2...] xnode=[n1 n2...]
 <leaki_times=[t1 t2 ...]> duration=<value> error_limit=<value>
 time_window=[start1 stop1 start2 stop2 ...] res_th_va=<value>
 res_th=<value> isource_ith=<value> bjt_vbe=<value> bjt_ith=<value>
 diode_vth=<value> <floatgate=[yes|no|gate_has_driver_no_cap]>
 <filter=[no|rc]> <detailed_path=[yes|per_fm|per_fn]> <sort=[no|current]>
 numprocesses=<value> <distributed=[no|fork]> ith=<value>
 <sweep=[no|single|all|all_once] points=<value> vmin=<value> vmax=<value>
 rforce=<value> time_window=[start1 stop1 start2 stop2 ...] <inst=[inst1
 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2...]>
 <xsubckt=[xsubckt1 xsubckt2...]> <nonconducting_subckt=[subckt1
 subckt2...]> <conducting_subckt=[subckt1 subckt2...]> <float_vpn=[vpn1
 vpn2...]> <debug_net=[net1 net2...]>
```

## Description

Reports the DC leakage paths that are caused by floating gate. This check can be used in two ways. One is based on transient analysis and the other is based on leakage analysis. Both methods cannot be used in one check statement. If you specify both methods in one check statement, then, leakage analysis gets higher priority than transient analysis.

The following table shows the Spectre modes in which the two methods are supported:

**Table 16-3 Transient and Leakage Analysis Based Approaches**

| Method                                                                  | Spectre,<br>Spectre APS,<br>Spectre X | Spectre<br>XPS<br>SPICE | Spectre<br>XPS<br>FastSPICE<br>(SRAM,<br>DRAM,<br>Flash) | Spectre<br>MS |
|-------------------------------------------------------------------------|---------------------------------------|-------------------------|----------------------------------------------------------|---------------|
| Dynamic Floating Gate Induced Leakage Check based on transient analysis | Yes                                   | Yes                     | No                                                       | No            |
| Dynamic Floating Gate Induced Leakage Check based on leakage analysis   | Yes                                   | Yes                     | Yes                                                      | Yes           |

The two methods are explained below.

## Transient-based Method

The check based on transient analysis is evoked when parameters `time_window` or/and `duration` are specified. It reports the qualifying paths carrying an absolute current higher than the parameter `ith` for a duration longer than the specified duration (`duration`), within the specified time window (`time_window`). This qualifying path must also have a MOSFET with gate floating for duration longer than the specified duration (`duration`), within the specified time window (`time_window`). The violations are a union of `dyn_highz` and `dyn_dcpath`, if you use the same setting. This methodology does not generate the worst case leakage path. If the settings of `dyn_dcpath` and `dyn_floatdcpath` are same, the violations of `dyn_floatdcpath` will be a subset of `dyn_dcpath`. The following parameters are irrelevant: `vmin`, `vmax`, `points`, `rforce`, `leaki_times`, `sweep`, `floatgate`, `detailed_report`, `debug_net`, `distribute`, and `numprocesses`. The floating node detection is similar to `dyn_highz` and the path detection is similar to `dyn_dcpath`.

## ***Leakage Analysis-based Method***

The check based on leakage analysis is evoked when parameter `leaki_times` is specified. `leaki_times` should be carefully selected in standby or power-down mode (see [XPS SRAM Leakage Current Simulation](#)). The check is performed at specified times (`leaki_times`) of a transient simulation. Floating nodes and MOSFET devices with floating gates are detected. Potential leakage paths (`sweep=no`) or worst leakage paths (`sweep=all|single|all_once`) caused by floating gate MOSFET devices are reported. The leakage paths are checked between the specified power supply nodes (`net`). The floating node detection and path detection in the leakage analysis based method are explained below:

### **Floating node detection (`leaki_times`)**

A node is considered floating (or in high impedance state) if it has no conducting path to a power supply or ground. A report of all MOSFETs with floating gates can be printed by using the parameter `floatgate`. The following device conducting rules are used for floating node detection:

- MOSFET is considered to be conducting if `region` is either `triode` or `saturation`.
- Resistors, controlled resistors, `phy_res`, relay, and inductors are considered to be conducting if  
`R <= res_th`.
- BJT is considered to be conducting if `vbe > bjt_vbe` or `ic > bjt_ith`.
- Diode is considered to be conducting if `v > diode_vth`.
- `Vsource`, and `iprobe`s are considered to be conducting.
- `Isource`s, `VCCS`, and `CCCS` are considered to be conducting if `i > isource_ith`.
- JFET is considered to be conducting.
- Mutual inductors and controlled capacitors are considered to be non-conducting.
- Verilog-A: conducting path depends on the module details

### **Path detection (`leaki_times`)**

Once the floating nodes are identified, the leakage paths caused by the floating nodes need to be detected. You can use the current-based method or the conducting-rule-based method to detect the leakage path.

When the `sweep` parameter is set to `single`, `all`, or `all_once`, the leakage path detection is based on current. In the current-based path detection method, floating node voltage is

swept, and the current in the path is measured. After the measurement, the current-based method reports the qualifying paths carrying an absolute current higher than the parameter `ith`. Either all floating nodes are swept at once (`sweep=all`), or each floating node is swept individually (`sweep=single`). The following parameters are relevant to the current-based path detection method: `vmin`, `vmax`, `points`, and `rforce`.

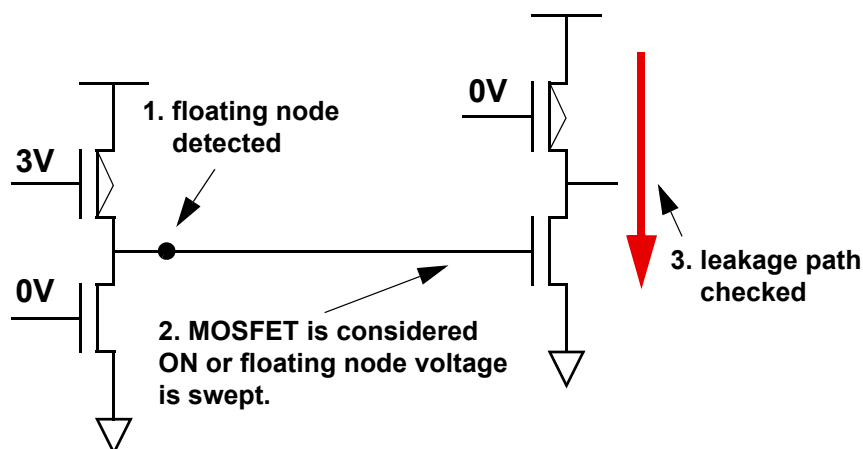
When the `sweep` parameter is set to `no`, the leakage path detection is based on following conducting rules:

- MOSFET devices with floating gates are always considered to be conducting.
- Resistors, controlled resistors, and inductors are considered to be conducting if `R <= res_th`
- BJT is considered to be conducting if `vbe > bjt_vbe` or `ic > bjt_ith`.
- Diode is considered to be conducting if `v > diode_vth`.
- Vsources is considered to be conducting if `v=0`; otherwise, it is not conducting.
- Iprobes are considered to be conducting.
- Isources, VCCS, and CCCS are considered to be conducting if `i > isource_ith`.
- VerilogA: conducting path depends on the module details

The following parameters are irrelevant with `sweep=no`: `vmin`, `vmax`, `points`, and `rforce`.

If more than two nets are specified, then Spectre checks the leakage path between each pair of nets. For example, if `net=[vdc1 vdc2 0]` is specified, then the conducting path between `vdc1` and `vdc2`, `vdc1` and `0`, and `vdc2` and `0` is checked.

Higher accuracy settings are recommended when using the Spectre XPS FastSPICE solver (+cktpreset=sram\_pwr).



For Spectre MS mode, the results of the check are written to a file with the extension `dynamic.leaki_<leaki>.xml`, where `<leaki>` is the `leaki_times` specified in the check statements. For example, for `leak_times=[7.5n]`, two files will be generated; a regular file with the extension `dynamic.xml` and a `dyn_floatdcpath` file with extension the extension `dynamic.leaki_7.5e-9.xml`.

For Spectre, Spectre APS, Spectre X, Spectre XPS SPICE, and Spectre XPS FastSPICE, the results of the check are written to a single file with the extension `dynamic.xml`.

**Note:** The `dyn_floatdcpath` report can also list the iprobes added by the simulator. You can set the global option `check_dcpath_igniprobes=yes` to include the iprobes in the report. Only the iprobes added by the simulator (through `save` statement or `options` statement) are controlled by the `check_dcpath_igniprobes` option.

By default, bulk current through the MOSFET is not traced. You can set the global option `dcpath_bulk_current=yes` to trace the bulk current.

## Arguments

|                          |                                                                                                   |
|--------------------------|---------------------------------------------------------------------------------------------------|
| <code>leaki_times</code> | Defines the times at which the check is performed.                                                |
| <code>duration</code>    | Leakage paths with a duration longer than the specified value are reported. Default value is 5ns. |

**Note:** This option is supported only in Spectre, Spectre APS, and Spectre X.

`time_window` The time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to tend.

`error_limit` Maximum number of errors to be reported. Default is 10000.

### **Floating node detection parameters**

`bjt_vbe` BJT vbe conducting threshold for high impedance node detection. BJT is conducting if  $i > bjt\_ith$  or  $vbe > bjt\_vbe$ . Default is 0.4V.

`bjt_ith` BJT ith conducting threshold for high impedance node detection. BJT is conducting if  $i > bjt\_ith$  or  $vbe > bjt\_vbe$ . Default is 50nA.

`res_th_va` Verilog-A resistor conducting threshold for high impedance node detection. This parameter is applicable only on AMS `ie` element, and on one or two-port AHD module. Default is 10 MOhms.

`res_th` Resistor conducting threshold for high impedance node detection. Resistor is conducting if  $R < res\_th$ . Default is 1TOhms.

`diode_vth` Diode voltage conducting threshold for high impedance node detection. Diode is conducting if  $v > diode\_vth$ . Default is 0.6V.

`isource_ith` Current source conducting threshold for floating node detection. Current sources are conducting if  $i > isource\_ith$ . Default is 1pA.

`mos_conduct_rule` The conducting rule to decide whether a MOSFET is conducting or not.

Possible Values:

- `tri_sat`: Specifies that a MOSFET is conducting when region is either triode or saturation.
- `tri_sat_sub`: Specifies that a MOSFET is conducting when region is either triode, saturation, or subthreshold.
- `ids_gds`: Specifies that a MOSFET is conducting when  $ids > mos\_ith$  or  $gds > mos\_gds$ , where `mos_ith` and `mos_gds` are check parameters.
- `vgs`: Specifies that a MOSFET is conducting when  $vgs > vth$  (Only supported in XPS Fastspice).

The region, `ids`, `gds` and `vgs` are oppoint parameters of MOSFET.

Default is `tri_sat`.

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`debug_net` Hierarchical nets to debug. Wildcard is not allowed. Default is none. The debug report is generated at `leaki_times`.

`nonconducting_subckt`

All instances of specified subcircuit are considered non-conducting during the floating node detection. All devices inside the subcircuit are considered non-conducting during the floating node detection. Wildcard is supported. Default is none.

**Note:** This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre MS.

`conducting_subckt`

All instances of specified subcircuit are considered conducting during the floating node detection. All devices inside the subcircuit are considered conducting during the floating node detection. Wildcard is supported. Default is none.

**Note:** This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre MS.

`nonconducting_primitive=[...]`

All instances of specified primitive or VerilogA modules are considered non-conducting during the floating node detection. Wildcard is supported. Default is none.

`nonfloat_vpn=[...]` All specified vpn(s) will be marked as non-floating nodes during floating node detection. Wildcard is not allowed. Wildcard is not allowed. Default is none.

**Note:** This option is supported only in Spectre XPS FastSPICE mode.

`float_vpn`

All channel connections of the specified VPN or VPNs are marked as floating nodes during floating node detection. Wildcard is not allowed. Default is none.

**Note:** This option is supported only in Spectre XPS FastSPICE mode.

### Floating node detection filtering parameters

|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>floatgate</code> | Specifies whether to report all MOSFETs with floating gate at specified <code>leaki_times</code> . If set to <code>gate_has_driver_no_moscap</code> , floating MOSCAPs are not reported. The value <code>gate_has_driver_no_moscap</code> is supported only in Spectre XPS FastSPICE mode. If set to <code>yes</code> , all MOSFETs with floating gates at the specified <code>leaki_times</code> are reported. If set to <code>no</code> , then the report is not generated. Default value is <code>no</code> . Possible values are: <code>no</code> , <code>yes</code> , and <code>gate_has_driver_no_moscap</code> . |
| <code>filter</code>    | If set to <code>no</code> , filtering is not performed. If set to <code>rc</code> , <code>dyn_floatdcpath</code> checks only one node in the same parasitic sub. This option is supported only in Spectre XPS FastSPICE mode. Possible values are <code>no</code> and <code>rc</code> .                                                                                                                                                                                                                                                                                                                                 |
| <code>node</code>      | Nodes to which the floating node detection is applied. This parameter is not supported in Spectre XPS FastSPICE. Default is all ( <code>node=*</code> ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <code>xnode</code>     | Nodes that are excluded from floating node detection. This parameter is not supported in Spectre XPS FastSPICE. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>inst</code>      | Subcircuit instances to which the floating node detection is applied. This parameter is not supported in Spectre XPS FastSPICE. Default includes all instances ( <code>inst=*</code> ).                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>xinst</code>     | Subcircuit instances to be excluded from the floating node detection. This parameter is not supported in Spectre XPS FastSPICE. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>subckt</code>    | The instances of the specified subcircuit to which the floating node detection is applied. This parameter is not supported in Spectre XPS FastSPICE. Default includes all subcircuits ( <code>subckt=*</code> ).                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>xsubckt</code>   | The instances of the specified subcircuits that are excluded from the floating node detection. This parameter is not supported in Spectre XPS FastSPICE. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                               |

## Path detection parameters

|                  |                                                                                                                                                      |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>net</code> | Hierarchical node names between which the leakage path is checked. Wildcarding is not allowed. All combination of nets are checked. Default is none. |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|



|        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| sweep  | <p>If set to <code>no</code>, no DC sweep is performed and leakage path is based on conducting rules. If set to <code>single</code>, each floating node is swept one at a time and the leakage paths more than <code>ith</code> are reported. If set to <code>all</code>, all floating nodes are swept together and the leakage paths more than <code>ith</code> are reported. If set to <code>all_once</code>, voltage of gates connected to NMOS is set to <code>VDD</code>, voltage of gates connected to PMOS is set to <code>0</code>, voltage of gates connected to both NMOS and PMOS is set to <code>VDD/2</code>, and leakage paths more than <code>ith</code> are reported.</p> <p>The default is <code>all</code> in Spectre, Spectre APS, Spectre X, Spectre XPS Spice and Spectre MS and <code>no</code> in Spectre XPS FastSPICE. The option <code>all_once</code> is supported only in Spectre XPS FastSPICE. The option <code>single</code> is not supported in Spectre XPS FastSPICE.</p> |
| ith    | <p>Leakage paths more than <code>ith</code> will be reported. This option is applicable only with <code>sweep=single</code>, <code>sweep=all</code>, and <code>sweep=all_once</code>. The default value is 50uA. This option is supported only in Spectre, Spectre APS, and Spectre X.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| points | <p>Number of sweep points, applicable to both <code>sweep=single</code> and <code>sweep=all</code>. The default value is 3.</p> <p><b>Note:</b> This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre MS.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| vmin   | <p>Minimum voltage for <code>sweep=single</code> and <code>sweep=all</code>. If specified, the voltage sweep will start from the specified <code>vmin</code> voltage. If not specified, minimum voltage in the design will be used. Default is <code>none</code>.</p> <p><b>Note:</b> This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre MS.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| vmax   | <p>Maximum voltage for <code>sweep=single</code> and <code>sweep=all</code>. If specified, the voltage sweep will stop at the specified <code>vmax</code> voltage. If not specified, maximum voltage in the design will be used. Default is <code>none</code>.</p> <p><b>Note:</b> This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre MS.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

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|                           |                                                                                                                                                                                                                                       |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>rforce</code>       | Change the <code>rforce</code> value only for <code>sweep=single</code> and <code>sweep=all</code> . The default value is 500M.<br><br><b>Note:</b> This option is supported only in Spectre, Spectre APS, Spectre X, and Spectre MS. |
| <code>numprocesses</code> | Number of processes to use for distributed analysis.                                                                                                                                                                                  |
| <code>distribute</code>   | Distribute method to use. Currently, it is supported only for <code>sweep=single</code> . Possible values are <code>no</code> , <code>fork</code> , <code>lsf</code> , and <code>sge</code> .                                         |

### Path detection filtering parameters

|                            |                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>detailed_path</code> | If set to <code>yes</code> , prints the detailed path. Default is <code>per_fm</code> , which prints one path per floating MOSFET. If set to <code>per_fn</code> , print one path per floating node. Possible values are <code>per_fm</code> , <code>yes</code> , and <code>per_fn</code> . The <code>per_fn</code> value is not supported in Spectre XPS FastSPICE. |
| <code>sort</code>          | Sort the violations. If set to <code>no</code> , sorting is not performed. If set to <code>current</code> , <code>dyn_floatdcpath</code> sorts the violations based on maximum current. Possible values are <code>no</code> and <code>current</code> . Default value is <code>no</code> .                                                                            |

### Example 1

```
dyn1 dyn_floatdcpath net=[vdd 0] leaki_times=[7.5n]
```

The above command will report the high impedance node induced DC leakage paths between the nets `vdd` and `0` at the specified leaki times (based on leakage analysis). The following is an example of the report that is displayed in the Web browser:

## Dynamic Floating Node Induced DC Leakage Path Check Violations

### dyn\_floatdcpath: dyn1

- dyn1 dyn\_floatdcpath net=["vdd" "0"] leaki\_times=[7.5e-09]
- Violation Count: 1

#### Dynamic Floating Node Induced DC Leakage Path Check - DC Path Violations

| Title                | From Net | To Net | Violation Time(s) |
|----------------------|----------|--------|-------------------|
| <a href="#">dyn1</a> | vdd      | 0      | 7.500000e-09      |

#### Fdcpath datas: size=3

| Instance | Current(A)    | Floating Gate Node | Floating Gate Node Volt(V) |
|----------|---------------|--------------------|----------------------------|
| MP2      | -5.033521e-04 | N/A                | 0.000000e+00               |
| MN2      | 5.033526e-04  | out1               | 1.045099e+00               |
| MN3      | 5.033502e-04  | N/A                | 0.000000e+00               |

#### Mosinfo datas: size=3

| Device | Model | Drain Name | Drain Volt(V) | Gate Name | Gate Volt(V) | Source Name | Source Volt(V) | Bulk Name | Bulk Volt(V) |
|--------|-------|------------|---------------|-----------|--------------|-------------|----------------|-----------|--------------|
| MP2    | pch   | out2       | 9.455211e-01  | 0         | 0.000000e+00 | vdd         | 1.100000e+00   | vdd       | 1.100000e+00 |
| MN2    | nch   | out2       | 9.455211e-01  | out1      | 1.045099e+00 | out3        | 1.592441e-01   | 0         | 0.000000e+00 |
| MN3    | nch   | out3       | 1.592441e-01  | vdd       | 1.100000e+00 | 0           | 0.000000e+00   | 0         | 0.000000e+00 |

This path report contains the following three sections:

- The first section shows the path that is found starting *From Net* `vdd` *To Net* `0`.
- The second section shows the actual instances in the path. The first column *Instance* contains instances in the path. The second column contains the current through the instances. The third column establishes the link between the floating node and MOSFET. The third column may contain either a node name or N/A. If it contains a node name, it means that the corresponding element is a MOSFET whose gate is floating. The fourth column shows the voltage of the floating gate.
- The third section shows the state of MOSFETs in the path. It does not report anything other than MOSFET. The first column *Device* is the MOSFET name. The second column is the model name. The following columns show the terminal names and voltages.

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## Example 2

```
dyn3 dyn_floatdcpath net=[vdd2 0] duration=1n ith=1u time_window=[0n 20n]
```

The above command will report the high impedance node induced DC leakage paths between the nets `vdd2` and `0`. The command will report the paths that carry current higher than `200u` for a duration longer than `1n` within the time window between `1n` and `20n`. The following is an example of the report that is displayed in the Web browser:

### Dynamic Floating Node Induced DC Leakage Path Check Violations

#### **dyn\_floatdcpath: dyn3**

- dyn3 dyn\_floatdcpath net=["vdd2" "0"] duration=1e-09 ith=1e-06 time\_window=[0 2e-08]
- Violation Count: 2

#### Dynamic Floating Node Induced DC Leakage Path Check based on transient analysis - DC Path Violations

| Title                | From Net | To Net | Start(s)     | Duration(s)  |
|----------------------|----------|--------|--------------|--------------|
| <a href="#">dyn3</a> | vdd2     | 0      | 5.293002e-09 | 4.838801e-09 |

#### Fdcpath datas: size=2

| Instance | Current(A)    | Floating Gate Node | Floating Gate Node Volt(V) |
|----------|---------------|--------------------|----------------------------|
| MP2      | -1.090717e-05 | out1               | 4.519859e-01               |
| MN2      | 1.016297e-05  | out1               | 4.519859e-01               |

#### Mosinfo datas: size=2

| Device | Model | Drain Name | Drain Volt(V) | Gate Name | Gate Volt(V) | Source Name | Source Volt(V) | Bulk Name | Bulk Volt(V) |
|--------|-------|------------|---------------|-----------|--------------|-------------|----------------|-----------|--------------|
| MN2    | nch   | out2       | 1.087655e+00  | out1      | 4.519859e-01 | 0           | 0.000000e+00   | 0         | 0.000000e+00 |
| MP2    | pch   | out2       | 1.087655e+00  | out1      | 4.519859e-01 | vdd2        | 1.100000e+00   | vdd2      | 1.100000e+00 |

Since this check is based on transient analysis, the name of table is Dynamic Floating Node Induced DC Leakage Path Check based on transient analysis.

## Dynamic MOSFET Voltage Check

### Syntax

```
title dyn_mosv model=[m1 m2 ...] cond=<expression> <sample=extreme|start>
duration=<value> <sort=[no|duration]> time_window=[start1 stop1 start2
stop2] <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]>
<subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> <depth=n>
error_limit=<value>
```

### Description

Reports MOSFET devices fulfilling the conditional expression on device voltages and device size (`w`, `l`) for a duration longer than the user-defined duration threshold (`duration`).

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Supported MOSFET variables are:  $v(g,s)$ ,  $v(g,d)$ ,  $v(g,b)$ ,  $v(d,s)$ ,  $v(d,b)$ ,  $v(s,b)$ ,  $v(g)$ ,  $v(d)$ ,  $v(s)$ ,  $v(b)$ ,  $l$ , and  $w$ .

Supported operators are:  $+$ ,  $-$ ,  $*$ ,  $/$ ,  $==$ ,  $!=$ ,  $<$ ,  $<=$ ,  $>$ ,  $>=$ ,  $||$ ,  $\&\&$ , and  $!$ .

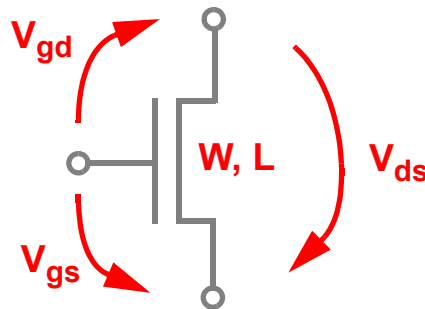
When `sample` is set to `extreme`, the extreme value of voltage function is reported. If the expression contains  $>$  or  $>=$ , the max value is reported as the extreme value. If the expression contains  $<$  or  $<=$  the min value is reported as the extreme value. Expressions having voltage function to the right and left of the comparison operator such as  $v(g) > v(s)$  are not supported. However,  $v(g,s) > 0$  is supported.

In Spectre, Spectre APS, Spectre X, and Spectre XPS SPICE, the expression specified in `cond` can have multiple key-expressions. For example, `cond="v(g,s)>0.4 && v(d,s)>0.4"`.

In Spectre XPS FastSPICE, the expression specified in `cond` should contain only one key-expression. For example, `cond="v(g,s)>0.4"`.

The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.

**Note:** This design check is supported only in Spectre, Spectre APS, Spectre X, Spectre XPS SPICE, and Spectre XPS FastSPICE mode. It is not supported in Spectre MS mode (see [Chapter 4, “The Spectre XPS Circuit Simulator”](#)). For Spectre, Spectre XPS SPICE, and Spectre MS modes, use of device check is recommended (see [Device Checks](#)).



### Arguments

|                    |                                                          |
|--------------------|----------------------------------------------------------|
| <code>model</code> | MOSFET device model names to be checked.                 |
| <code>cond</code>  | Condition to be checked (default is <code>none</code> ). |

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|                          |                                                                                                                                                                                                                                                             |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>sample</code>      | Report the extreme value or the start point. Possible values are <code>extreme</code> and <code>start</code> .                                                                                                                                              |
| <code>sort</code>        | Sort the violations. If set to <code>no</code> , no sorting is performed. If set to <code>duration</code> , violations are sorted based on duration. Possible values are <code>no</code> and <code>duration</code> . The default value is <code>no</code> . |
| <code>duration</code>    | Conditions with duration longer than the specified value are reported (default is <code>5ns</code> ).                                                                                                                                                       |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is <code>0</code> to <code>tend</code> .                                                                                        |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                                                                                                                  |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                                                                                                               |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                                                                                                           |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                                                                                                            |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is <code>8</code> .                                                                                                              |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is <code>10000</code> .                                                                                                                                                                                    |

### **Example**

```
mos1 dyn_mosv model=[nmos] cond=" v(g,s)>1.9" duration=2n
```

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The above command will report a MOSFET instance of NMOS that fulfills the condition  $v(g, s) > 1.9$  for a duration longer than  $2n$ . The following is an example of the report that is displayed in the Web browser:

## Dynamic MOSFET Voltage Check Violations

### dyn\_mosv: mos1

mos1 dyn\_mosv model=["nmos"] cond="v(g,s)>1.9" duration=2e-09

Violation Count: 2

#### Dynamic mosv check - Violation

| Title                | Instance Name | Start(s)     | Model Name | Drain Name | Gate Name | Source Name | Bulk Name | Duration(s)  | Dissatisfied  | Violating Value        | Check Time(s) |
|----------------------|---------------|--------------|------------|------------|-----------|-------------|-----------|--------------|---------------|------------------------|---------------|
| <a href="#">mos1</a> | x1.mn2        | 1.058000e-09 | nmos       | mid        | in        | gnd         | gnd       | 3.984000e-09 | (v(g, s)>1.9) | v(g, s)=1.914000000000 | 1.058000e-09  |
| <a href="#">mos1</a> | x2.mn2        | 5.187000e-09 | nmos       | out        | mid       | gnd         | gnd       | 4.813000e-09 | (v(g, s)>1.9) | v(g, s)=1.909126953081 | 5.187000e-09  |

## Dynamic Resistor Voltage Check

### Syntax

```
title dyn_resv cond=<expression> duration=<value> time_window=[start1 stop1
start2 stop2] <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]>
<subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> <depth=n>
error_limit=<value>
```

### Description

Reports resistor elements fulfilling the conditional expression on element voltages for a duration longer than the user-defined duration threshold (`duration`).

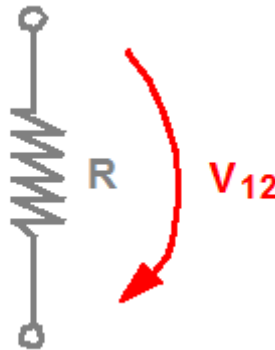
Supported resistor variables are:  $V(1, 2)$ ,  $V(1)$ , and  $V(2)$ .

Supported operators are: +, -, \*, /, ==, !=, <, <=, >, >=, ||, &&, and !.

The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.

**Note:** This design check is supported only in Spectre XPS FastSPICE mode. It is not supported in Spectre, Spectre APS, Spectre X, Spectre XPS SPICE, and Spectre MS modes (see [Chapter 4, “The Spectre XPS Circuit Simulator”](#)). For Spectre, Spectre APS, Spectre

XPS SPICE, and Spectre MS modes, use of device check is recommended (see [Device Checks](#)).



### **Arguments**

|                          |                                                                                                                                                         |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>cond</code>        | Condition to be checked (default is <code>none</code> ).                                                                                                |
| <code>duration</code>    | Conditions with duration longer than the specified value are reported (default is <code>5ns</code> ).                                                   |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is <code>0 to tend</code> . |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                              |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                           |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                       |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                        |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is <code>8</code> .          |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is <code>10000</code> .                                                                                |

### **Example**

```
resv dyn_resv cond="V(1,2)>0.2" duration=5n
```



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The above command will report the resistor elements that fulfill the condition  $V(1,2) > 0.2V$  for a duration longer than  $5e-10s$ . The following is an example of the report that is displayed in the Web browser:

## Dynamic Resistor Voltage Check Violations

### dyn\_resv: resv1

resv1 dyn\_resv cond="v(1,2)>0.2" duration=5e-10

Violation Count: 1

| Title | Instance Name | Start(s)     | Model Name | Term1 Name | Term2 Name | Duration(s)  | Dissatisfied        | Violating Value  | Check Time(s) |
|-------|---------------|--------------|------------|------------|------------|--------------|---------------------|------------------|---------------|
| resv1 | r1            | 1.011000e-09 | resistor   | in         | in1        | 6.850000e-10 | ( v(1, 2) > (0.2) ) | v(1, 2)=0.206731 | 1.011000e-09  |

## Dynamic Capacitor Voltage Check

### Syntax

```
title dyn_capv cond=<expression> duration=<value> time_window=[start1 stop1
start2 stop2] <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]>
<subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> <depth=n>
error_limit=<value>
```

### Description

Reports capacitor elements fulfilling the conditional expression on element voltages for a duration longer than the user-defined duration threshold (*duration*).

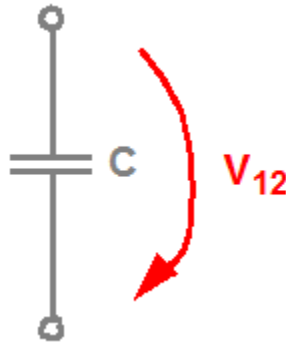
Supported capacitor variables are:  $V(1,2)$ ,  $V(1)$ , and  $V(2)$ .

Supported operators are: +, -, \*, /, ==, !=, <, <=, >, >=, ||, &&, and !.

The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.

**Note:** This design check is supported only in Spectre XPS FastSPICE mode. It is not supported in Spectre, Spectre APS, Spectre X, Spectre XPS SPICE, and Spectre MS modes (see [Chapter 4, “The Spectre XPS Circuit Simulator”](#)). For Spectre, Spectre APS, Spectre

XPS SPICE, and Spectre MS modes, use of device check is recommended (see [Device Checks](#)).



## Arguments

|                          |                                                                                                                                                         |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>cond</code>        | Condition to be checked (default is <code>none</code> ).                                                                                                |
| <code>duration</code>    | Conditions with duration longer than the specified value are reported (default is <code>5ns</code> ).                                                   |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> . |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                              |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                           |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                       |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                        |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.                        |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                              |

## Example

```
capv dyn_capv cond="V(1, 2)>0.2 duration=0.5n
```

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The above command will report the capacitor elements that fulfill the condition  $V(1,2) > 0.2V$  for a duration longer than  $5e-10s$ . The following is an example of the report that is displayed in the Web browser:

## Dynamic Capacitor Voltage Check Violations

### dyn\_capv: capv2

capv2 dyn\_capv cond="v(1,2)>0.2" duration=5e-10

Violation Count: 1

| Title | Instance Name | Start(s)     | Model Name | Term1 Name | Term2 Name | Duration(s)  | Dissatisfied        | Violating Value  | Check Time(s) |
|-------|---------------|--------------|------------|------------|------------|--------------|---------------------|------------------|---------------|
| capv2 | c1            | 1.011000e-09 | capacitor  | in         | in1        | 6.850000e-10 | ( v(1, 2) > (0.2) ) | v(1, 2)=0.206731 | 1.011000e-09  |

## Dynamic Diode Voltage Check

### Syntax

```
title dyn_diodev model=[m1 m2 ...] cond=<expression> duration=<value>
time_window=[start1 stop1 start2 stop2] <inst=[inst1 inst2...]>
<xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1
xsubckt2....]> <depth=n> error_limit=<value>
```

### Description

Reports diode devices fulfilling the conditional expression on device voltages for a duration longer than the user-defined duration threshold (*duration*).

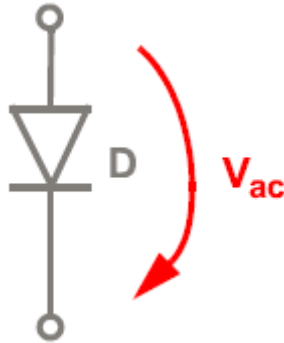
Supported diode variables are:  $v(a,c)$ ,  $v(a)$ , and  $v(c)$ .

Supported operators are: +, -, \*, /, ==, !=, <, <=, >, >=, ||, &&, and !.

The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.

**Note:** This design check is supported only in Spectre XPS FastSPICE mode. It is not supported in Spectre, Spectre APS, Spectre X, Spectre XPS SPICE, and Spectre MS modes (see [Chapter 4, “The Spectre XPS Circuit Simulator”](#)). For Spectre, Spectre APS, Spectre

XPS SPICE, and Spectre MS modes, use of device check is recommended (see [Device Checks](#)).



### **Arguments**

|                          |                                                                                                                                                         |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>model</code>       | Diode device model names to be checked.                                                                                                                 |
| <code>cond</code>        | Condition to be checked (default is <code>none</code> ).                                                                                                |
| <code>duration</code>    | Conditions with duration longer than the specified value are reported (default is <code>5ns</code> ).                                                   |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> . |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                              |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                           |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                       |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                        |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.                        |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                              |

Example

```
dv1 dyn_diodev model=["diode1"] cond="v(a,c)>0.5" duration=2.5e-08
```

The above command will report the instances of `diode1` that fulfill the condition  $v(a, c) > 0.5$  for a duration longer than 25n. The following is an example of the report that is displayed in the Web browser:

Dynamic Diode Voltage Check Violations

**dyn\_diodev: dv1**

dv1 dyn\_diodev model=["diode1"] cond="v(a,c)>0.5" duration=2.5e-08

Violation Count: 2

| Title               | Instance Name | Start(s)     | Model Name | Anode Name | Cathode Name | Duration(s)  | Dissatisfied        | Violating Value  | Check Time(s) |
|---------------------|---------------|--------------|------------|------------|--------------|--------------|---------------------|------------------|---------------|
| <a href="#">dv1</a> | d2            | 3.968000e-09 | diode1     | mid        | vdd          | 4.638400e-08 | ( v(a, c) > (0.5) ) | v(a, c)=0.535796 | 3.968000e-09  |
| <a href="#">dv1</a> | d1            | 5.169600e-08 | diode1     | 0          | mid          | 5.288000e-08 | ( v(a, c) > (0.5) ) | v(a, c)=0.510379 | 5.169600e-08  |

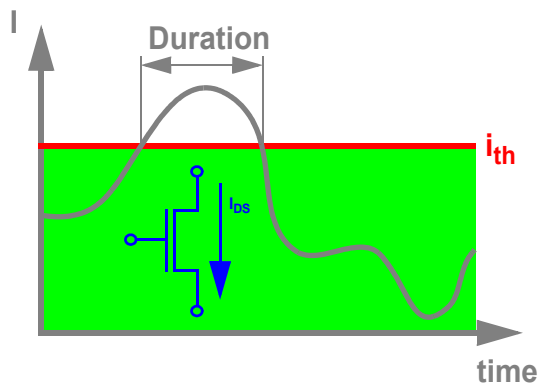
Dynamic Excessive Element Current Check

Syntax

```
title dyn_exi dev=[d1 d2 ...] duration=<value> ith=<value> <inst=[inst1 inst2...]>
 <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2...]> <xsubckt=[xsubckt1
 xsubckt2...]> <depth=n> error_limit=<value> time_window=[start1 stop1
 start2 stop2 ...]
```

Description

Reports elements and devices carrying currents (absolute value) above a threshold specified by `ith` for a time longer than the duration threshold specified by `duration`. The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.



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This design check is not supported in Spectre MS mode. See [Spectre Mixed-Signal Design Simulation](#) on page 68.

### Arguments

|                          |                                                                                                                                                         |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>dev</code>         | Device (MOSFET, R, C, and so on) instance names to be checked (default is <code>none</code> ).                                                          |
| <code>duration</code>    | Excessive currents with a duration longer than value are reported (default is <code>5ns</code> ).                                                       |
| <code>ith</code>         | Elements with current higher than the specified value are reported (default is <code>none</code> ).                                                     |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                              |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                           |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                       |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                        |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.                        |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                              |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> . |

### Example

```
exi dyn_exi dev=["*"] ith=1e-06 duration=1e-09
```

The above command will report all device instances that carry excessive currents higher than  $1e-06$  for a duration longer than  $1e-09s$ . The following is an example of the report that is displayed in the Web browser:

Dynamic Excessive Element Current Check Violations

dyn\_exi: exi1

- exi1 dyn\_exi dev=["\*"] ith=1e-06 duration=1e-09
- Violation Count: 2

| Title                | Instance Name | Start(s)     | Duration(s)  | Max Current(A) |
|----------------------|---------------|--------------|--------------|----------------|
| <a href="#">exi1</a> | x1.mn1        | 4.923000e-09 | 5.077000e-09 | 2.320818e-03   |
| <a href="#">exi1</a> | x2.r1         | 1.280000e-10 | 9.872000e-09 | 3.000000e-03   |

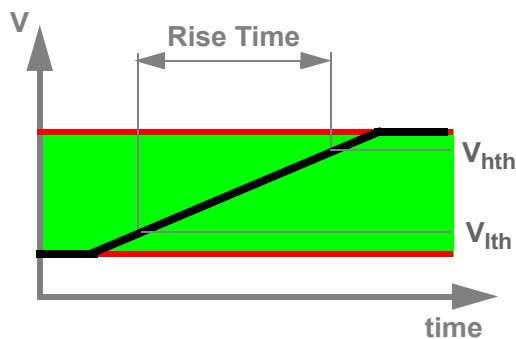
Dynamic Excessive Rise and Fall Time Check

Syntax

```
title dyn_exrf node=[n1 n2 ...] rise=<value> fall=<value> utime=<value>
 vlth=<value> vpth=<value> time_window=[start1 stop1 start2 stop2]
 <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1
 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]>
 <fanout=all|gate|bulk|gate_has_driver_no_moscap|gate_no_moscap>
 <filter=[no|rc]> <inverse=[no|yes]> <sort=[no|duration]> <depth=n>
 error_limit=<value>
```

Description

Reports nodes with excessive rise and fall times, or nodes with an undefined state. The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.



## Spectre Classic Simulator, Spectre APS, Spectre X, Spectre XPS, Spectre FMC Analysis, and Legato Reliability Solution User Guide

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This design check is not supported in Spectre MS mode. See [Spectre Mixed-Signal Design Simulation](#) on page 68.

### Arguments

|                          |                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>        | Nodes to be checked. Default is <code>none</code> .                                                                                                                                                                                                                                                                                                                                        |
| <code>rise</code>        | Rise times longer than specified value are reported (default is <code>none</code> ). The rise time is measured between low ( <code>vlth</code> ) and high ( <code>vhth</code> ) voltage thresholds.                                                                                                                                                                                        |
| <code>fall</code>        | Fall times longer than specified value are reported (default is <code>none</code> ). The fall time is measured between low ( <code>vlth</code> ) and high ( <code>vhth</code> ) voltage thresholds.                                                                                                                                                                                        |
| <code>utime</code>       | Undefined time threshold. Undefined state is defined by node voltages between the low and high voltage thresholds.                                                                                                                                                                                                                                                                         |
| <code>vlth</code>        | Low voltage threshold for <code>rise</code> , <code>fall</code> , and <code>utime</code> measurements (default is <code>none</code> ).                                                                                                                                                                                                                                                     |
| <code>vhth</code>        | High voltage threshold for <code>rise</code> , <code>fall</code> , and <code>utime</code> measurements (default is <code>none</code> ).                                                                                                                                                                                                                                                    |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> .                                                                                                                                                                                                                                    |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code> .                                                                                                                                                                                                                                                                                               |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                                                                                                                                                                                                                                              |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                                                                                                                                                                                                                                          |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                                                                                                                                                                                                                                           |
| <code>fanout</code>      | Fanout setting to filter node with specified connection. When <code>fanout=gate_no_moscap</code> , gates connecting only to MOSCAPs will not be checked. This option is supported only in Spectre XPS. Possible values are <code>all</code> , <code>gate</code> , <code>bulk</code> , <code>gate_has_driver_no_moscap</code> , <code>gate_no_moscap</code> . Default is <code>all</code> . |



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|                          |                                                                                                                                                                                                                                                                                         |
|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>filter</code>      | If set to <code>no</code> , filtering is not performed. If set to <code>rc</code> , <code>dyn_exrf</code> checks only one node in the same parasitic sub. This option is supported only in Spectre XPS FastSPICE. Possible values are <code>no</code> and <code>rc</code> .             |
| <code>inverse</code>     | If set to <code>no</code> , reports rise times and fall times longer than the specified value. If set to <code>yes</code> , reports rise times and fall times smaller than the specified value. Possible values are <code>no</code> and <code>yes</code> . Default is <code>no</code> . |
| <code>sort</code>        | Sort the violations. If set to <code>no</code> , no sorting is performed. If set to <code>duration</code> , violations are sorted based on duration. Possible values are <code>no</code> and <code>duration</code> . The default value is <code>no</code> .                             |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.                                                                                                                                                        |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                                                                                                                                                              |

## Example

```
exrf1 dyn_exrf node=["*"] rise=5e-10 fall=5e-10 utime=1e-09 vlth=0.3 vhth=2.7
time_window=[1e-09 9e-09]
```

The above command will report nodes with rise and fall times larger than  $5e-10s$  and nodes with undefined states longer than  $1e-09s$ . Measurements are performed between the voltage thresholds  $0.3V$  and  $2.7V$  and within the time window between  $1e-09s$  and  $9e-09s$ . The following is an example of the report that is displayed in the Web browser:

### Dynamic Excessive Rise, Fall, Undefined State Time Check Violations

#### **dyn\_exrf: exrf1**

- exrf1 dyn\_exrf node=["\*"] rise=5e-10 fall=5e-10 utime=1e-09 vlth=0.3 vhth=2.7 time\_window=[1e-09 9e-09]
- Violation Count: 5

| Title                 | Node Name | Type  | Start(s)     | Duration(s)  |
|-----------------------|-----------|-------|--------------|--------------|
| <a href="#">exrf1</a> | out       | fall  | 1.390000e-09 | 1.288000e-09 |
| <a href="#">exrf1</a> | out1      | utime | 1.440000e-09 | 7.560000e-09 |
| <a href="#">exrf1</a> | t1        | rise  | 4.838000e-09 | 8.270000e-10 |
| <a href="#">exrf1</a> | t2        | fall  | 5.596000e-09 | 8.870000e-10 |
| <a href="#">exrf1</a> | out       | rise  | 6.374000e-09 | 1.336000e-09 |

## Dynamic Glitch Check

### Syntax

```
title dyn_glitch node=[n1 n2 ...] duration=<value> min_duration=<value>
max_duration=<value> time_window=[start1 stop1 start2 stop2]
high=<value> low=<value> mid=<value> <inst=[inst1 inst2...]> <xinst=[xinst1
xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]>
<fanout=all|gate|bulk> <depth=n> error_limit=<value>
```

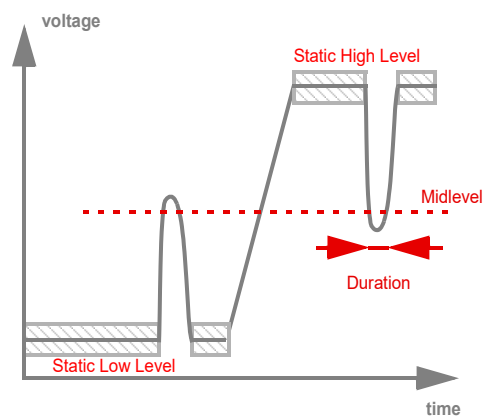
### Description

A glitch occurs when:

- A low signal goes above the mid level, and crosses the mid level again in a time less than the user-defined duration.
- A high signal goes below mid level, and crosses the mid level again in a time less than the user-defined duration.

The check applies only to blocks with single and constant power supply.

The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.



This design check is not supported in Spectre MS mode. See [Spectre Mixed-Signal Design Simulation](#) on page 68.

## Arguments

|                           |                                                                                                                                                                                                                                        |
|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>         | Nodes to which the check is applied. Default is <code>none</code> .                                                                                                                                                                    |
| <code>duration</code>     | Duration threshold of a glitch (default is <code>5ns</code> ).                                                                                                                                                                         |
| <code>min_duration</code> | Minimum glitch duration threshold. Default is <code>0 sec</code> .                                                                                                                                                                     |
| <code>max_duration</code> | Maximum glitch duration threshold Default is <code>5ns</code> .                                                                                                                                                                        |
| <code>time_window</code>  | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is <code>0 to tend</code> .                                                                                |
| <code>high</code>         | High voltage level (default is <code>none</code> ).                                                                                                                                                                                    |
| <code>low</code>          | Low voltage level (default is <code>0V</code> ).                                                                                                                                                                                       |
| <code>mid</code>          | Mid voltage level (default is <code>0.5*(high+low)</code> ).                                                                                                                                                                           |
| <code>inst</code>         | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                                                                                             |
| <code>xinst</code>        | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                                                                                          |
| <code>subckt</code>       | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                                                                                      |
| <code>xsubckt</code>      | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                                                                                       |
| <code>fanout</code>       | Fanout setting to filter node with specified connection. Possible values are <code>all</code> , <code>gate</code> , and <code>bulk</code> . Default is <code>all</code> . This option is supported only in Spectre XPS FastSPICE mode. |
| <code>depth</code>        | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is <code>8</code> .                                                                                         |
| <code>error_limit</code>  | Maximum number of errors to be reported. Default is <code>10000</code> .                                                                                                                                                               |

## Example

```
dyn_glitch1 dyn_glitch node=["*"] duration=1e-09 high=1.2
```

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The above command will report all nodes with glitches. The glitch duration is defined to be smaller than 1ns. The high voltage level is 1.2V. The following is an example of the report that is displayed in the Web browser:

## Dynamic Glitch Check Violations

### `dyn_glitch: dyn_glitch1`

- `dyn_glitch1 dyn_glitch node=[*] duration=1e-09 high=1.2`
- Violation Count: 4

| Title                       | Node Name | Start(s)     | Duration(s)  | Peak Value(V) | Static Voltage(V) |
|-----------------------------|-----------|--------------|--------------|---------------|-------------------|
| <a href="#">dyn_glitch1</a> | XIL6.A1   | 2.064000e-09 | 2.940000e-10 | -1.588217e-03 | 1.200000e+00      |
| <a href="#">dyn_glitch1</a> | OUT       | 2.089000e-09 | 3.050000e-10 | 1.197951e+00  | 0.000000e+00      |
| <a href="#">dyn_glitch1</a> | XIL6.A1   | 1.207800e-08 | 1.330000e-10 | 1.162371e+00  | 0.000000e+00      |
| <a href="#">dyn_glitch1</a> | OUT       | 1.210600e-08 | 1.320000e-10 | -6.177051e-03 | 1.200000e+00      |

## Dynamic Setup and Hold Check

### Syntax

```
title dyn_setuphold node=[node] ref_node=[node] setup_time=<value>
 hold_time=<value> setup_chk_time=<value> setup_hold_time=<value>
 delay=<value> edge=[rise|fall|both] ref_edge=[rise|fall|both] vlth=<value>
 ref_vlth=<value> vhth=<value> ref_vhth=<value> time_window=[start1 stop1
 start2 stop2] margin_stats=[yes|no] <subckt=[subckt1 subckt2....]>
 <fanout=all|gate|bulk> error_limit=<value> report=[violation|all]
```

### Description

Measures the timing of a signal net in comparison to a referenced (clock) net. It reports the setup or hold timing errors if the signal net transition happens within the specified violation window.

The violation window of the setup timing check is `refTime + delay - setup_time` and `refTime + delay`. The violation window for the hold timing check is `refTime + delay` and `refTime + delay + hold_time`. `refTime` is the transition time of the reference net.

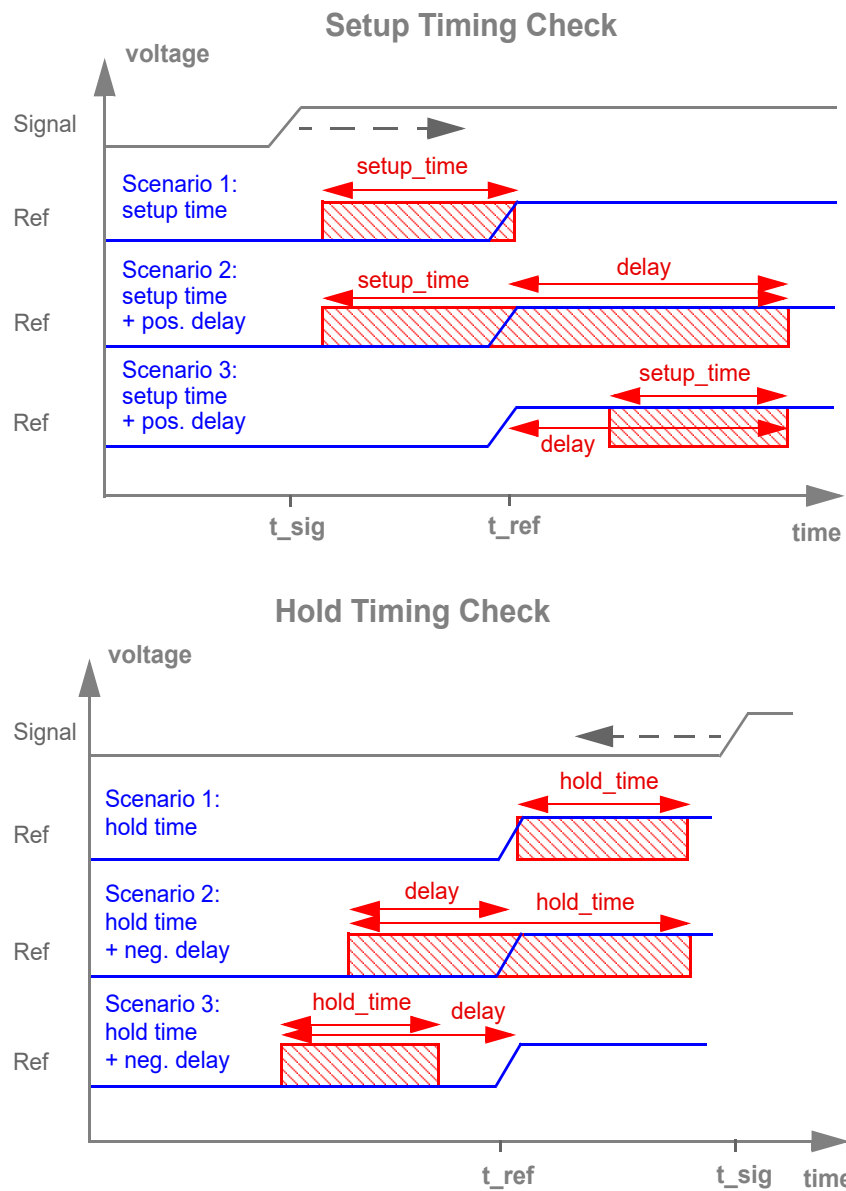
`ref_vhth` and `vhth` parameters trigger the rising edge measurements, whereas `ref_vlth` and `vlth` parameters trigger the falling edge measurements.

If subcircuit parameter (`subckt`) is specified then the node (`node`) and reference node (`ref_node`) are considered local nodes to that subcircuit. That is, the nodes and reference nodes will belong to the instances of the specified subcircuit. Only one `subckt` value can be specified per check, with no wildcard.

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If the `subckt` parameter is not specified then `node` and `ref_node` are considered as global nodes with hierarchical names starting from the top level.

The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.



In the figure above, a setup or hold error is reported if the signal net transition occurs in the red marked area.

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This design check is not supported in Spectre MS mode. See [Spectre Mixed-Signal Design Simulation](#) on page 68.

### Arguments

|                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>           | Node to which the check is applied. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                       |
| <code>ref_node</code>       | Name of the referenced clock (net). Wildcards are not supported.                                                                                                                                                                                                                                                                                                                                                                                           |
| <code>setup_time</code>     | Setup time violation window. If specified, setup check is enabled. Default is 0.0 sec.                                                                                                                                                                                                                                                                                                                                                                     |
| <code>hold_time</code>      | Hold time violation window. If specified, hold check is enabled. Default is 0.0 sec.                                                                                                                                                                                                                                                                                                                                                                       |
| <code>delay</code>          | Delay time of the referenced signal. Default is 0.0 sec.                                                                                                                                                                                                                                                                                                                                                                                                   |
| <code>edge</code>           | Edge type of the signal net. Possible values are <code>rise</code> , <code>fall</code> , or <code>both</code> . Default is <code>rise</code> .                                                                                                                                                                                                                                                                                                             |
| <code>ref_edge</code>       | Edge type of the referenced signal net. Possible values are <code>rise</code> , <code>fall</code> , or <code>both</code> . Default is <code>rise</code> .                                                                                                                                                                                                                                                                                                  |
| <code>setup_chk_time</code> | Specifies the setup time checking window. Spectre only checks the signal states within <code>refTime+delay-setup_chk_time</code> and <code>refTime+delay</code> window. Signal states outside the window are ignored. This argument is enabled only when setup check is enabled and the value of <code>report</code> is <code>all</code> . The specified value must be greater than <code>setup_time</code> . Default value is <code>2*setup_time</code> . |
| <code>hold_chk_time</code>  | Specifies the hold time checking window. Spectre only checks the signal states within <code>refTime+delay+hold_chk_time</code> and <code>refTime+delay</code> window. Signal states outside the window are ignored. This argument is enabled only when hold check is enabled and the value of <code>report</code> is <code>all</code> . The specified value must be greater than <code>hold_time</code> . Default value is <code>2*hold_time</code> .      |
| <code>vlth</code>           | Low voltage threshold for the signal net. Default is 0.2v.                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>ref_vlth</code>       | Low voltage threshold for the referenced net. Default is 0.2v                                                                                                                                                                                                                                                                                                                                                                                              |
| <code>vhth</code>           | High voltage threshold for the signal net. Default is 0.8v                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>ref_vhth</code>       | High voltage threshold for the referenced net. Default is 0.8v.                                                                                                                                                                                                                                                                                                                                                                                            |

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|                           |                                                                                                                                                                                                                                        |
|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>time_window</code>  | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> .                                                                                |
| <code>margin_stats</code> | Specifies whether or not to print the margin statistics. By default, margin statistics are not printed. Possible values are <code>no</code> and <code>yes</code> . The default value is <code>no</code> .                              |
| <code>error_limit</code>  | Maximum number of errors to be reported. Default is 10000.                                                                                                                                                                             |
| <code>subckt</code>       | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>none</code> .                                                                                                                          |
| <code>fanout</code>       | Fanout setting to filter node with specified connection. Possible values are <code>all</code> , <code>gate</code> , and <code>bulk</code> . Default is <code>all</code> . This option is supported only in Spectre XPS FastSPICE mode. |
| <code>report</code>       | Reports all checks or violations only. Possible values are <code>all</code> and <code>violation</code> . Default value is <code>violation</code> .                                                                                     |

## Example 1

```
s4 dyn_setuphold node=["*"] edge=rise ref_node="I9.I1.clk" ref_edge=rise
 setup_time=5e-11 vth=0.5 ref_vth=0.5
```

The above command reports any transition of signal node in the time window between 0.5ns before the signal `clk` rises.

Since `subckt` parameter is not specified, it will compare all nodes with `ref_node` `I9.I1.sig_2` and report any violations.

The following is an example of the report that is displayed on the Web browser.

- s4 dyn\_setuphold node=["\*"] edge=rise ref\_node="I9.I1.clk" ref\_edge=rise setup\_time=5e-11 vth=0.5 ref\_vth=0.5
- Violation Count: 3

| Title              | Ref Node Name | Node Name   | Type  | Edge | Ref Edge | Time(s)      | Reference Time(s) | Violation Window Start(s) | Violation Window End(s) |
|--------------------|---------------|-------------|-------|------|----------|--------------|-------------------|---------------------------|-------------------------|
| <a href="#">s4</a> | I9.I1.clk     | signal_2    | setup | rise | rise     | 1.800000e-10 | 2.197383e-10      | 1.697383e-10              | 2.197383e-10            |
| <a href="#">s4</a> | I9.I1.clk     | signal_4    | setup | rise | rise     | 1.900000e-10 | 2.197383e-10      | 1.697383e-10              | 2.197383e-10            |
| <a href="#">s4</a> | I9.I1.clk     | I9.I1.sig_1 | setup | rise | rise     | 2.099673e-10 | 2.197383e-10      | 1.697383e-10              | 2.197383e-10            |

## Example 2

```
s1 dyn_setuphold node=["*"] edge=rise ref_node="clk" ref_edge=rise setup_time=5e-11
 vhth=0.5 ref_vhth=0.5 subckt=ckt1
```

The above command reports any transition of the signal data in the time window between 0.5ns before the signal `clk` rises.

Since `subckt=ckt1` is specified, it will compare all nodes in subckt `ckt1` with `ref_node sig_2` and report any violations. Note that `node` and `ref_node` belongs to same subckt `ckt1`.

The following is an example of the report that is displayed on the Web browser.

- s1 dyn\_setuphold node=["\*"] edge=rise ref\_node="clk" ref\_edge=rise setup\_time=5e-11 vhth=0.5 ref\_vhth=0.5 subckt=["ckt1"]
- Violation Count: 2

| Title              | Ref Node Name | Node Name   | Type  | Edge | Ref Edge | Time(s)      | Reference Time(s) | Violation Window Start(s) | Violation Window End(s) |
|--------------------|---------------|-------------|-------|------|----------|--------------|-------------------|---------------------------|-------------------------|
| <a href="#">s1</a> | I9.I1.clk     | I9.I1.sig_1 | setup | rise | rise     | 2.099673e-10 | 2.197383e-10      | 1.697383e-10              | 2.197383e-10            |
| <a href="#">s1</a> | I9.I0.clk     | I9.I0.sig_1 | setup | rise | rise     | 2.497238e-10 | 2.593195e-10      | 2.093195e-10              | 2.593195e-10            |

## Dynamic Noisy Node Check

### Syntax

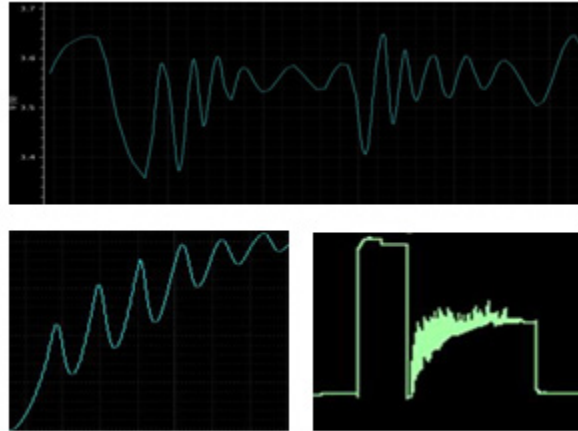
```
title dyn_noisynode node=[node] time_window=[start1 stop1 start2 stop2]
 duration=<value> <inst=[inst1 inst2...]> skip =<value> e1=<value> e2=<value>
 <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2...]> <xsubckt=[xsubckt1
 xsubckt2...]> <fanout=all|gate|bulk> <depth=n> error_limit=<value>
```

### Description

Identifies the nodes with unstable or noisy node conditions. A node is considered unstable or noisy if its voltage fulfills the condition  $\text{abs}(dV/dt) > e1$  and  $\text{abs}(d(dV/dt)dt) > e2$  for a



time longer than `duration`. Stable periods shorter than `skip` are ignored. The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.



This design check is not supported in Spectre MS mode. See [Spectre Mixed-Signal Design Simulation](#) on page 68.

## Arguments

|                          |                                                                                                                                                         |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>        | Node to which the check is applied. Default is none.                                                                                                    |
| <code>duration</code>    | Duration threshold. Default is 5.00e-07.                                                                                                                |
| <code>e1</code>          | First derivative threshold. Default is 5.00e04.                                                                                                         |
| <code>e2</code>          | Second derivative threshold. Default is 2.00e16.                                                                                                        |
| <code>skip</code>        | Stable periods less than <code>skip</code> are ignored. Default is 50.0e-09                                                                             |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> . |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                              |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                              |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is none.                                                                         |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                       |

|         |                                                                                                                                                                                |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| xsubckt | Instances of the specified subcircuit which are excluded from the circuit check. Default is none.                                                                              |
| fanout  | Fanout setting to filter node with specified connection. Possible values are all, gate, and bulk. Default is all. This option is supported only in Spectre XPS FastSPICE mode. |
| depth   | Hierarchy level (from top level) to be checked. depth=3 reports errors on top level plus 3 sublevels. Default is 8.                                                            |

Example

```
u1 dyn_noisynode node=["*"] duration=1e-08 skip=1.5e-10 time_window=[0 20n]
```

The above command reports all nodes with unstable or noisy node conditions for a duration longer than 1e-08 seconds. Stable periods shorter than 1.5e-10 are ignored. The circuit check is active between 0 and 20ns.

The following is an example of the report that is displayed on the Web browser.

Dynamic Noisy Node Check Violations

dyn\_noisynode: u1

- u1 dyn\_noisynode node=["\*"] duration=1e-08 skip=1.5e-10
- Violation Count: 5

| Title              | Node Name | Start(s)     | Duration(s)  |
|--------------------|-----------|--------------|--------------|
| <a href="#">u1</a> | 2         | 8.333333e-12 | 1.998472e-08 |
| <a href="#">u1</a> | 3         | 8.333333e-12 | 1.998472e-08 |

Dynamic Node Capacitance Check

Syntax

```
title dyn_nodecap <node=[node1 node2...]> <time=[t1 t2...]> <inst=[inst1
inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]>
<xsubckt=[xsubckt1 xsubckt2....]> <fanout=all|gate|bulk> <depth=n>
error_limit=<value><intrinsic_cap_merge=no|yes>
```

### Description

Reports the node capacitance at specified times (`time`) of a transient simulation. Device capacitances, voltage dependent capacitances, grounded and coupling caps are combined into one value. The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.

This design check is not supported in Spectre MS mode. See [Spectre Mixed-Signal Design Simulation](#) on page 68.

### Arguments

|                                  |                                                                                                                                                                                                                                            |
|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>                | Nodes for which the capacitance needs to be checked. Default value is <code>none</code> .                                                                                                                                                  |
| <code>time</code>                | Time point(s) at which the check needs to be performed.                                                                                                                                                                                    |
| <code>inst</code>                | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                                                                                                 |
| <code>xinst</code>               | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                                                                                              |
| <code>subckt</code>              | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                                                                                          |
| <code>xsubckt</code>             | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                                                                                           |
| <code>intrinsic_cap_merge</code> | <p>Merge the internal captab node with the external node. Possible values are <code>yes</code> and <code>no</code>. The default value is <code>no</code>.</p> <p>This option is supported only in Spectre, Spectre APS, and Spectre X.</p> |
| <code>fanout</code>              | Fanout setting to filter node with specified connection. Possible values are <code>all</code> , <code>gate</code> , and <code>bulk</code> . Default is <code>all</code> . This option is supported only in Spectre XPS FastSPICE mode.     |
| <code>depth</code>               | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.                                                                                                           |
| <code>error_limit</code>         | Maximum number of errors to be reported. Default is 10000.                                                                                                                                                                                 |

## Example

```
n1 dyn_nodecap node=[*] time=[0 3n 7n]
```

The above command will report the node capacitance for all nodes at times 0, 3ns and 7ns.

The following is an example of the report that is displayed in the Web browser:

## Dynamic Node Capacitance Check Violations

### dyn\_nodecap: n1

```
n1 dyn_nodecap node=["*"] time=[0 3e-09 7e-09]
```

Violation Count: 6

| Title              | Node Name | Time(s)      | Capacitance(F) |
|--------------------|-----------|--------------|----------------|
| <a href="#">n1</a> | mid       | 0.000000e+00 | 3.239651e-13   |
| <a href="#">n1</a> | out       | 0.000000e+00 | 1.035941e-13   |
| <a href="#">n1</a> | mid       | 3.000000e-09 | 2.545755e-13   |
| <a href="#">n1</a> | out       | 3.000000e-09 | 1.982198e-13   |
| <a href="#">n1</a> | mid       | 7.000000e-09 | 3.234888e-13   |
| <a href="#">n1</a> | out       | 7.000000e-09 | 1.035941e-13   |

## Dynamic Subcircuit Port Power Check

### Syntax

```
title dyn_subcktpwr <port=[port1 port2...]> <inst=[inst1 inst2...]> <net=[n1
n2...]> <power=[on|off]> error_limit=<value> time_window=[start1 stop1
start2 stop2] <depth=n> filter=[none|gates] ith=<value>
```

### Description

Reports port currents, port powers, and subcircuit powers.

The port current is positive when the current is going into a subcircuit. This check will report average, RMS, and maximum values of the current entering a port.

This check can be used in two ways. One is tree-based and other is instance-based. Both methods cannot be combined in one check statement. If you specify both methods in one

check statement, then the tree-based method gets higher priority than the instance-based method.

In the tree-based method, the root of a tree is selected by the parameter `net`. From this root, port current is traced down the hierarchy until `depth` or device is reached. The `port`, `inst`, and `power` parameters are irrelevant in tree-based approach.

In the instance-based method, any port name matching `inst` and `port` parameters are reported.

Power analysis can be done by using the parameter `power`. This parameter is supported only in the instance-based method. When the parameter `power` is set to `on`, then two additional sections are generated. The first section reports the average, RMS and the maximum power entering the ports, specified using the parameter `port`. The second section reports the average, RMS, and the maximum power consumed by each instance of a subcircuit, specified using the parameter `inst`.

**Note:** The wildcard in `port` parameter only considers the ports defined in the subcircuit definition. For global nodes, you need to add the ports manually.

### Arguments

|                          |                                                                                                                                                         |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>port</code>        | The ports that need to be analyzed. Default value is <code>none</code> .                                                                                |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                              |
| <code>net</code>         | Specify the root for the tree-based method. This argument is supported only in Spectre, Spectre APS, and Spectre X.                                     |
| <code>power</code>       | If set to <code>off</code> (default), report only port currents. If set to <code>on</code> , report port currents, and power of ports and subcircuits.  |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is <code>none</code> .       |
| <code>filter</code>      | If set to <code>none</code> (default), all gates are checked. If set to <code>gates</code> , ports connected to MOSFET gates are skipped.               |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                              |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> . |

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`ith` If all the `abs (AVG)`, `RMS` and `abs (MAX)` values are below `ith`, the values will be filtered out.

## Example

```
chk1 dyn_subcktpwr inst=[*] port=[*] depth=1 time_window=[0 10m] power=on
```

The above command reports the port current for all ports of all instances in the time window between 0 and 10ms. The report includes the current and power information for all subcircuit instances one level down the hierarchy.

The following is an example of the report that is displayed in the Web browser:

### dyn\_subcktpwr: chk1

- `chk1 dyn_subcktpwr inst=["*"] port=["*"] depth=1 time_window=[0 0.01] power=on`
- Violation Count: 5

#### Dynamic Subckt Port Power Check - Port Current Report

| Title                | Port Name | Avg(A)        | RMS(A)       | Max(A)        | Max Time(s)  | From(s)      | To(s)        |
|----------------------|-----------|---------------|--------------|---------------|--------------|--------------|--------------|
| <a href="#">chk1</a> | x_top.A   | 8.000015e-04  | 1.260086e-03 | 2.000004e-03  | 1.100000e-03 | 0.000000e+00 | 1.000000e-02 |
| <a href="#">chk1</a> | x_top.B   | -8.000015e-04 | 1.260086e-03 | -2.000004e-03 | 1.100000e-03 | 0.000000e+00 | 1.000000e-02 |

#### Dynamic Subckt Port Power Check - Port Power Report

| Title                | Port Name | Avg(W)       | RMS(W)       | Max(W)       | Max Time(s)  | From(s)      | To(s)        |
|----------------------|-----------|--------------|--------------|--------------|--------------|--------------|--------------|
| <a href="#">chk1</a> | x_top.A   | 7.939066e-04 | 1.255858e-03 | 2.000004e-03 | 1.100000e-03 | 0.000000e+00 | 1.000000e-02 |
| <a href="#">chk1</a> | x_top.B   | 7.939066e-04 | 1.255858e-03 | 2.000004e-03 | 1.100000e-03 | 0.000000e+00 | 1.000000e-02 |

#### Dynamic Subckt Port Power Check - Sum of Port Powers by Instance

| Title                | Instance Name | Avg(W)       | RMS(W)       | Max(W)       | Max Time(s)  | From(s)      | To(s)        |
|----------------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|
| <a href="#">chk1</a> | x_top         | 1.587813e-03 | 2.511717e-03 | 4.000008e-03 | 1.100000e-03 | 0.000000e+00 | 1.000000e-02 |

## Dynamic Pulse Width Check

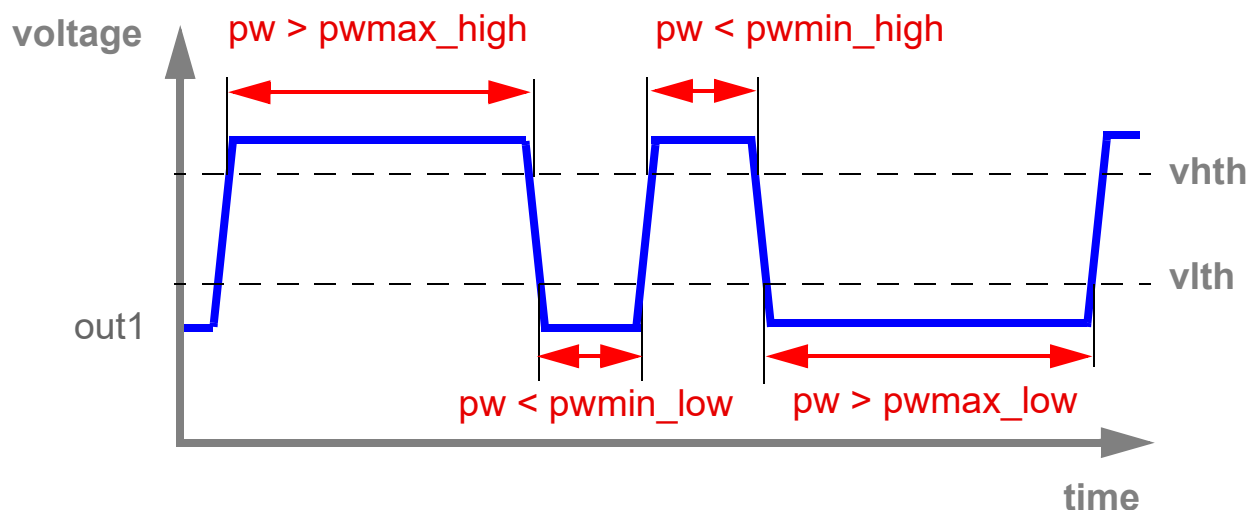
### Syntax

```
title dyn_pulsewidth node=[n1 n2 ...] pwmin_low=<value> pwmax_low=<value>
 pwmin_high=<value> pwmax_high=<value> vlth=<value> vhth=<value>
 time_window=[start1 stop1 start2 stop2] <inst=[inst1 inst2...]>
 <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1
 xsubckt2....]> <fanout=all|gate|bulk> <depth=n> error_limit=<value>
```

### Description

The pulse width of a logic low state signal is the duration between which the signal crosses the low voltage threshold ( $vlth$ ) while falling and again crosses  $vlth$  while rising. If this duration is outside the range specified using the `pwmin_low` and `pwmax_low` parameters, the `dyn_pulsewidth` check reports the pulse width of such signals.

Similarly, the pulse width of a logic high state signal is the duration between which the signal crosses the high voltage threshold ( $vhth$ ) while rising and again crosses  $vhth$  while falling. If this duration is outside the range of `pwmin_high` and `pwmax_high` parameters, the `dyn_pulsewidth` check reports the pulse width of such signals.



The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.

This design check is not supported in Spectre MS mode. See [Spectre Mixed-Signal Design Simulation](#) on page 68.

## Arguments

|                          |                                                                                                                                                                                                                                        |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>        | Nodes to which the check is applied. Default is none.                                                                                                                                                                                  |
| <code>pwmin_low</code>   | Minimum value of the pulse width in logic low state. Default is 0.0 sec.                                                                                                                                                               |
| <code>pymax_low</code>   | Maximum value of the pulse width in logic low state. Default is infinity sec.                                                                                                                                                          |
| <code>pwmin_high</code>  | Minimum value of the pulse width in logic high state. Default is 0.0 sec.                                                                                                                                                              |
| <code>pymax_high</code>  | Maximum value of the pulse width in logic high state. Default is infinity sec.                                                                                                                                                         |
| <code>vlth</code>        | Low voltage threshold for the signal net. Default is 0.2v.                                                                                                                                                                             |
| <code>vhth</code>        | High voltage threshold for the signal net. Default is 0.8v.                                                                                                                                                                            |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to tend.                                                                                              |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                                                                                                             |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                                                                                             |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is none.                                                                                                                                                        |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                                                                                      |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is none.                                                                                                                                     |
| <code>fanout</code>      | Fanout setting to filter node with specified connection. Possible values are <code>all</code> , <code>gate</code> , and <code>bulk</code> . Default is <code>all</code> . This option is supported only in Spectre XPS FastSPICE mode. |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.                                                                                                       |

## Example

```
chk1 dyn_pulsewidth node=[*] pwmin_low=20n pyrax_low=40n pwmin_high=20n
pymax_high=40n vlth=0.2 vhth=1.0
```



The above command reports all nodes that specify either of the following conditions:

- The pulse width in logic low state is outside the range of parameters `pwmin_low` (20n) and `pwmax_low` (40n).
- The pulse width in logic high state is outside the range of parameters `pwmin_high` (20n) and `pwmax_high` (40n).

The following is an example of the report that is displayed in the Web browser.

### Dynamic Pulse Width Check Violations

#### **dyn\_pulsewidth: chk1**

chk1 dyn\_pulsewidth node=["\*"] pwmin\_low=2e-08 pwmax\_low=4e-08  
pwmin\_high=2e-08 pwmax\_high=4e-08 vlth=0.2 vhth=1

Violation Count: 4

| Title                | Node Name | Type | Time(s)      | Pulse Width(s) |
|----------------------|-----------|------|--------------|----------------|
| <a href="#">chk1</a> | out1      | low  | 1.039700e-08 | 9.843000e-09   |
| <a href="#">chk1</a> | out1      | high | 2.035600e-08 | 4.994700e-08   |
| <a href="#">chk1</a> | out1      | high | 1.003570e-07 | 9.946000e-09   |
| <a href="#">chk1</a> | out1      | low  | 1.103970e-07 | 4.984300e-08   |

## Dynamic Power Density Check

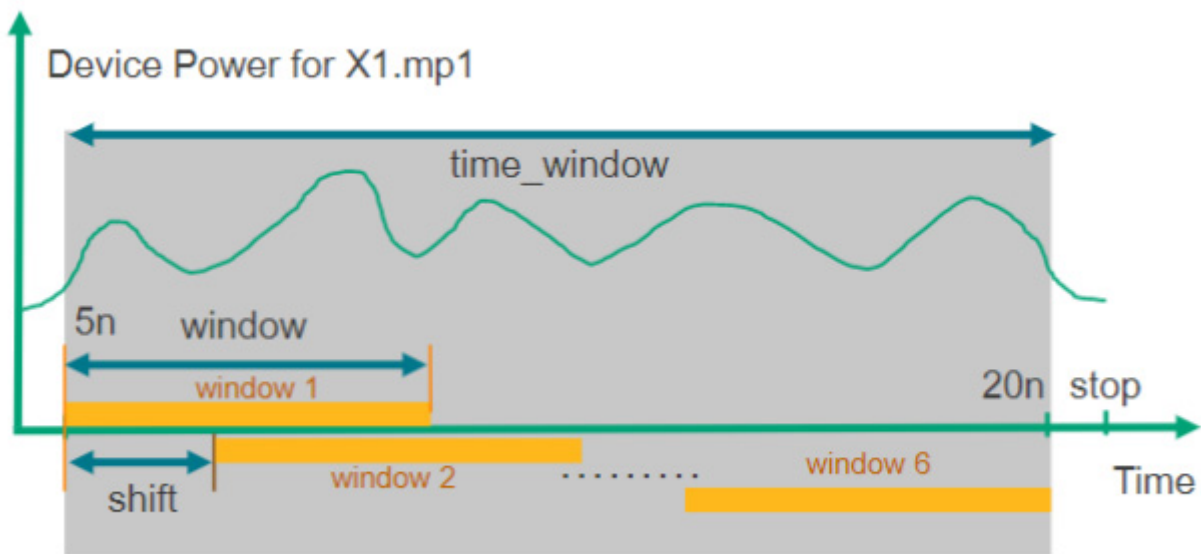
### Syntax

```
title dyn_powerdensity time_window=[start1 stop1 start2 stop2] window=<value>
 shift=<value> <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]>
 <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> <depth=n>
```

### Description

Device and circuit reliability heavily depend on how much power is consumed by the individual MOSFET devices and how much heat is generated in a short period of time. To ensure improved reliability and lifetime, circuit designers need to optimize the power consumption of devices in the given design.

The power density check reports the average window with the highest power consumption for each MOSFET. It is based on shifting the measuring window over the operating time window.



The results are written to a file with the extension `dynamic.xml`, which can be viewed with a Web browser.

**Parameters**

Filtering parameters

|                          |                                     |                                                                                                                                                                                                                                              |
|--------------------------|-------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>time_window</code> | <code>[tstart, tstop]</code><br>sec | The time window during which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to tend.                                                                                            |
| <code>window</code>      | <code>10e-9</code><br>sec           | Width of a measuring window for average power calculation. These measuring window will be inside the <code>time_window</code> . If not specified, there will be only one measuring window and it will be equal to <code>time_window</code> . |
| <code>shift</code>       | <code>5.00E-09</code><br>sec        | Time shift between two measuring window. Default is 5.00E-09 sec.                                                                                                                                                                            |

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|                          |       |                                                      |
|--------------------------|-------|------------------------------------------------------|
| <code>error_limit</code> | 10000 | Maximum number of errors reported. Default is 10000. |
|--------------------------|-------|------------------------------------------------------|

### Wildcard scoping

|                      |       |                                                                                                                                      |
|----------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| <code>inst</code>    | [...] | Subcircuit instances to which the check is applied. Default includes all instances ( <code>inst=*</code> ).                          |
| <code>xinst</code>   | [...] | Subcircuit instances to be excluded from the check. Default is none.                                                                 |
| <code>subckt</code>  | [...] | The instances of the specified subcircuit to which the check is applied. Default includes all subcircuits ( <code>subckt=*</code> ). |
| <code>xsubckt</code> | [...] | The instances of the specified subcircuits that are excluded from the check. Default is none.                                        |
| <code>depth</code>   | 8     | Hierarchy levels (starting from top, instance, or subcircuit scope) to be checked. Default is 8.                                     |

### Example

The following statement reports the average window with the highest power consumption for each MOSFET. The power consumption will be checked in 6n seconds average windows, shifted by 2n seconds.

```
chk1 dyn_powerdensity shift=2n window=6n
```

The report of this example is displayed in the Web browser, as shown below.

## Dynamic Power Density Check Violations

### dyn\_powerdensity: chk1

- chk1 dyn\_powerdensity shift=2e-09 window=6e-09
- Violation Count: 2

| Title                | Instance Name | Model Name | Avg window                   | Max Avg Power(W) | Width(m)     |
|----------------------|---------------|------------|------------------------------|------------------|--------------|
| <a href="#">chk1</a> | MN1           | nch        | [3.000000e-08, 3.600000e-08] | 1.999364e-03     | 2.000000e-06 |
| <a href="#">chk1</a> | MP1           | pch        | [1.000000e-08, 1.600000e-08] | 3.647913e-04     | 4.000000e-06 |

## Dynamic Active Node Check

### Syntax

```
title dyn_actnode node=[n1 n2 ...] dv=<value> type=<value> time_window=[start1
stop1 start2 stop2] <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]>
<subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]>
<fanout=all|gate|bulk> <depth=n> error_limit=<value>
```

### Description

The dynamic active node check detects nodes with voltage changes that exceed the user-defined threshold `dv`. The voltage change is defined as peak-to-peak voltage ( $V_{pp}$ ) within a time window.

The results are written to the `dynamic.xml` file, which can be viewed in a Web browser.

**Note:** This design check is supported in Spectre, Spectre APS, Spectre X, Spectre XPS Spice, and Spectre XPS FastSPICE modes. It is not supported in Spectre MS mode.

### Arguments

|                   |                                                                                                                              |
|-------------------|------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code> | Nodes to which the check is applied. Default is none.                                                                        |
| <code>dv</code>   | Voltage change threshold for the active nodes. Default is 0.1 volt.                                                          |
| <code>type</code> | Report inactive or active nodes or both. Possible values are <code>act</code> , <code>inact</code> , and <code>both</code> . |

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|                          |                                                                                                                                                                                                                                        |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> .                                                                                |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                                                                                                             |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                                                                                             |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                                                                                          |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                                                                                      |
| <code>fanout</code>      | Fanout setting to filter node with specified connection. Possible values are <code>all</code> , <code>gate</code> , and <code>bulk</code> . Default is <code>all</code> . This option is supported only in Spectre XPS FastSPICE mode. |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                                                                                       |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.                                                                                                       |

### Example

```
chk2 dyn_actnode node=[*] dv=4 type=act time_window=[0 3e-07]
```

The above command reports all nodes that are active. These active nodes will have peak-to-peak voltage above 4V between 0s to 300ns. In addition, the command prints a summary report that lists the percentage of active nodes having peak-to-peak voltage above 4V between 0s to 300ns.

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The following is an example of the report that is displayed on the Web browser.

## dyn\_actnode: chk1

- chk1 dyn\_actnode node=["\*"] dv=4 type=act time\_window=[0 3e-07]
- Violation Count: 7

### Dynamic Active Node Check - Summary

| Title                | Percentage of active nodes | From(s)      | To(s)        |
|----------------------|----------------------------|--------------|--------------|
| <a href="#">chk1</a> | 7.792%                     | 0.000000e+00 | 3.000000e-07 |

### Dynamic Active Node Check - Active Nodes

| Title                | Node Name  | Vpp(V)       | From(s)      | To(s)        |
|----------------------|------------|--------------|--------------|--------------|
| <a href="#">chk1</a> | X5.N2N1484 | 4.125149e+00 | 0.000000e+00 | 3.000000e-07 |
| <a href="#">chk1</a> | X5.N2N1485 | 5.344194e+00 | 0.000000e+00 | 3.000000e-07 |
| <a href="#">chk1</a> | X5.N2N1486 | 5.016927e+00 | 0.000000e+00 | 3.000000e-07 |
| <a href="#">chk1</a> | X5.N2N1489 | 4.030851e+00 | 0.000000e+00 | 3.000000e-07 |
| <a href="#">chk1</a> | X5.NA      | 4.235771e+00 | 0.000000e+00 | 3.000000e-07 |
| <a href="#">chk1</a> | X5.ND      | 4.161615e+00 | 0.000000e+00 | 3.000000e-07 |

## Dynamic Subcircuit Instance Activity Check

### Syntax

```
title dyn_activity min_activity=<value> time_window=[start1 stop1 start2 stop2...]
 <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1
 subckt2...]> <xsubckt=[xsubckt1 xsubckt2...]> <depth=n> error_limit=<value>
```

### Description

This check reports the activity percentage of an instance relative to a circuit. The activity percentage is the ratio of events in the instance versus the events in the entire circuit.

The check reports the activity for instances specified using the `inst` parameter and all its child instances.

The results are written to the `dynamic.xml` file, which can be viewed in a Web browser.

**Note:** This design check is supported only in Spectre XPS FastSPICE mode. It is not supported in Spectre, Spectre APS, Spectre X, Spectre XPS SPICE, and Spectre MS modes (see [Chapter 4, “The Spectre XPS Circuit Simulator”](#)).

### Arguments

|                           |                                                                                                                                                           |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>min_activity</code> | Any block activity below the minimum activity value is not be reported. The value can be between 0 and 1. Default is 0.                                   |
| <code>time_window</code>  | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> .   |
| <code>inst</code>         | Instances of the subcircuit to which the check is applied. Default is <code>none</code> .                                                                 |
| <code>inst</code>         | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                |
| <code>xinst</code>        | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                             |
| <code>subckt</code>       | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                         |
| <code>xsubckt</code>      | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                          |
| <code>depth</code>        | Hierarchy level (from top, instance, or subcircuit scope) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8. |
| <code>error_limit</code>  | Maximum number of errors to be reported. Default is 10000.                                                                                                |

### Example

```
chk1 dyn_activity inst=[x1 x2] time_window=[0n 20n] min_activity=0
```

The above command will check the activity percentage of instances X1 and X2. The events start recording between the specified time window of 0ns and 20ns.

The following is an example of the report that is displayed on the Web browser:

## Dynamic Subckt Activity Check Violations

### dyn\_activity: chk1

chk1 dyn\_activity inst=["x1" "x2"] time\_window=[0 2e-08] min\_activity=0

Violation Count: 10

| Title                | Instance Name | Activity | Subckt      | From(s)      | To(s)        |
|----------------------|---------------|----------|-------------|--------------|--------------|
| <a href="#">chk1</a> | x1            | 11.358%  | logic_gates | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x1.x_d1       | 3.580%   | nand        | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x1.x_d2       | 3.126%   | nand        | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x1.x_r1       | 3.669%   | nor         | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x1.x_t2       | 0.983%   | inv         | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x2            | 88.642%  | logic_gates | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x2.x_d1       | 31.813%  | nand        | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x2.x_d2       | 20.177%  | nand        | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x2.x_r1       | 33.956%  | nor         | 0.000000e+00 | 2.000000e-08 |
| <a href="#">chk1</a> | x2.x_t2       | 2.696%   | inv         | 0.000000e+00 | 2.000000e-08 |

## Dynamic Subcircuit Port Voltage/Current Check

### Syntax

```
title dyn_subcktport cond=<expression> duration=<value> time_window=[start1 stop1
start2 stop2...] subckt=<value> error_limit=<value>
```

### Description

Reports instances of the user-specified `subckt` fulfilling the conditional expression on port voltages and port currents for a time longer than the user-specified `duration`. Only one subcircuit is allowed per statement.

Voltages and currents of a port can be referenced by the port name of a subcircuit. For example, consider the subcircuit definition `.subckt INV port_A port_B`. Here, supported port names are: `v(port_A)`, `v(port_B)`, `v(port_A,port_B)`, `i(port_A)`, and `i(port_B)`. The port current is positive when the current is flowing into a subcircuit.

Supported operators are: `+`, `-`, `*`, `/`, `==`, `!=`, `<`, `<=`, `>`, `>=`, `|`, `&&`, and `!`.



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All design instances of the subcircuit specified using `subckt` are checked.

The results are written to the `dynamic.xml` file, which can be viewed in a Web browser.

**Note:** This design check is supported only in Spectre XPS FastSPICE mode. See [Chapter 4, “The Spectre XPS Circuit Simulator”](#).

### Arguments

|                          |                                                                                                                                                         |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>cond</code>        | Conditional expression to be fulfilled. Default is none.                                                                                                |
| <code>time_window</code> | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> . |
| <code>duration</code>    | Duration threshold. Default is 5.00E-09 sec.                                                                                                            |
| <code>error_limit</code> | Maximum number of errors reported. Default is 10000.                                                                                                    |
| <code>subckt</code>      | Instances of the specified subcircuit to which the check is applied. Wildcard is not supported. Default is none.                                        |

### Example

```
vol1 dyn_subcktport subckt="decwl64b" cond="v(inh_VDD)>1.7" duration=10n
```

The above command will report all instances of subcircuit `decwl64b` satisfying the condition `v(inh_VDD)>1.7` for a duration longer than 10n.

The following is an example of the report that is displayed on the Web browser:

- `vol1 dyn_subcktport subckt="decwl64b" cond="v(inh_VDD)>1.7" duration=1e-08`
- Violation Count: 4

| Title                | Instance Name ▾ | From(s)      | To(s)        | Dissatisfied           | Violating Value |
|----------------------|-----------------|--------------|--------------|------------------------|-----------------|
| <a href="#">vol1</a> | XTOP.XPOST0     | 0.000000e+00 | 1.000000e-07 | ( v(inh_VDD) > (1.7) ) | v(inh_VDD)=1.8  |

## Dynamic Delay Check

### Syntax

```
title dyn_delay node=[node] ref_node=[node] min_time=<value> max_time=<value>
 edge=[rise|fall|both] ref_edge=[rise|fall|both] vlth=<value>
 ref_vlth=<value> vhth=<value> ref_vhth=<value> time_window=[start1 stop1
 start2 stop2] <subckt=[subckt1]> <fanout=all|gate|bulk>
 error_limit=<value>
```

### Description

Checks timing delays between two signals and reports nodes with edge delay errors.

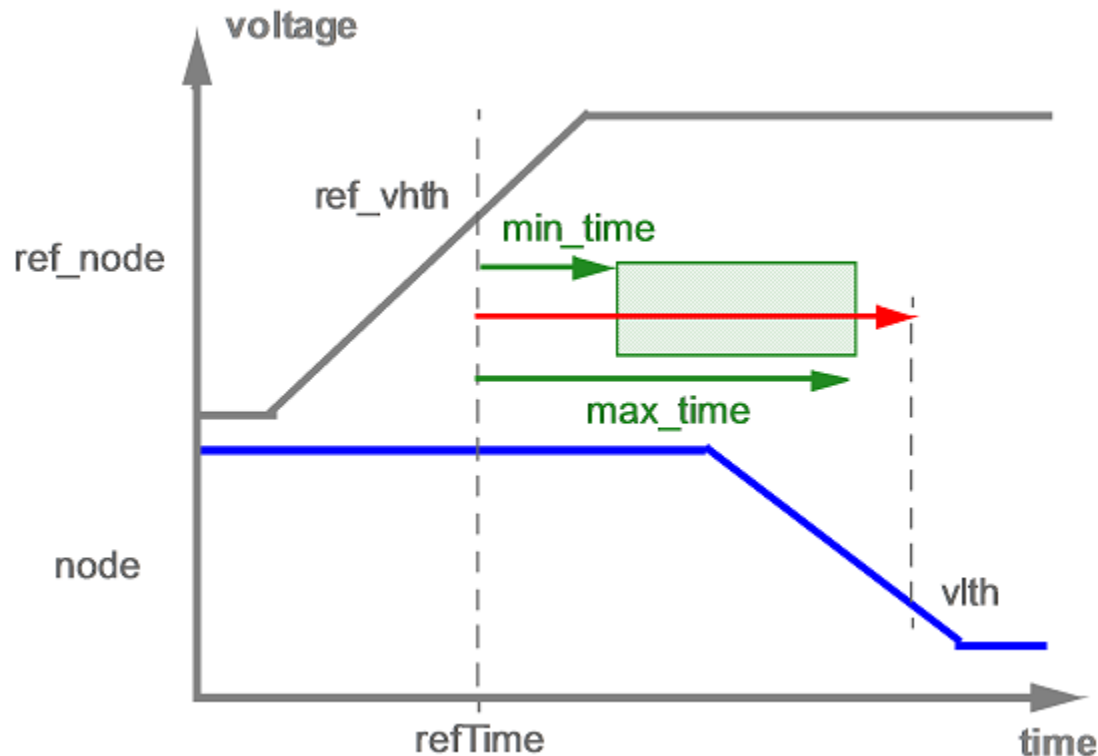
The delay is measured between user-specified nodes and a reference node. A timing delay error occurs when the transition time of a signal falls outside the range of `refTime + min_time` and `refTime + max_time`, where `refTime` is the transition time of the reference signal. In other words, a timing delay error occurs when the delay between the signal and the reference signal is outside the range of `min_time` and `max_time`.

The `ref_vhth` and `vhth` parameters are used for triggering rising edge measurements, while `ref_vlth` and `vlth` parameters are used for triggering falling edge measurements. For example, a delay measurement from a rising reference signal to a falling signal includes measuring the delay from the time the reference signal crosses `ref_vhth` to the time the signal crosses `vlth`.

If the `subckt` parameter is specified, then `node` and `ref_node` are considered as local nodes to the specified subcircuit. In other words, `node` and `ref_node` belong to the instances of the specified subcircuit. Only one `subckt` value can be specified per check, with no wildcard.

If the `subckt` parameter is not specified, `node` and `ref_node` are considered as global nodes with hierarchical names starting from the top level.

The results are written to the `dynamic.xml` file, which can be viewed in a Web browser.



In the figure above, an error is reported if the signal net transition occurs outside the green marked area.

**Note:** This design check is not supported in Spectre MS mode. See [Spectre Mixed-Signal Design Simulation](#) on page 68.

**Arguments**

|          |                                                                                                                                                       |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| node     | Nodes to which the check is applied. Default is none.                                                                                                 |
| ref_node | Name of the referenced node. Wildcards are not supported.                                                                                             |
| min_time | Minimum time delay between the signal and the reference signal transition. The specified value can be negative, 0, or positive.                       |
| max_time | Maximum time delay between the signal and the reference signal transition. The specified value can be negative, 0, or positive.                       |
| edge     | Edge type of the signal net. Possible values are <code>rise</code> , <code>fall</code> , and <code>both</code> . Default value is <code>rise</code> . |

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|             |                                                                                                                                                             |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ref_edge    | Edge type of the reference signal. Possible values are <code>rise</code> , <code>fall</code> , and <code>both</code> . Default value is <code>rise</code> . |
| vlth        | Low voltage threshold for the signal net.                                                                                                                   |
| ref_vlth    | Low voltage threshold for the referenced net.                                                                                                               |
| vhth        | High voltage threshold for the signal net.                                                                                                                  |
| ref_vhth    | High voltage threshold for the referenced net.                                                                                                              |
| time_window | Time window to which the circuit check is applied. Multiple non-overlapping time windows are supported. Default time window is 0 to <code>tend</code> .     |
| error_limit | Maximum number of errors reported. Default is 10000.                                                                                                        |
| subckt      | Instances of the specified subcircuit to which the check is applied. Default is none.                                                                       |

### Example

```
d1 dyn_delay ref_node=out8 node=out1 ref_edge=rise edge=fall min_time=100p
max_time=5n time_window=[115n 200n]
```

The above command reports any transition of signal data having delay of more than 5n seconds or having delay of less than 100p seconds. The delay is evaluated from the rising edge of `out8` node to the falling edge of `out1` node.

If the `subckt` parameter is not specified, then `node` and `ref_node` are considered as global nodes with the hierarchical names starting from the top level.

The following is an example of the report that is displayed on the Web browser:

### Dynamic Delay Check Violations

#### **dyn\_delay: d1**

- d1 dyn\_delay ref\_node="out8" node=["out1"] ref\_edge=rise edge=fall min\_time=1e-10 max\_time=5e-09 time\_window=[1.15e-07 2e-07]
- Violation Count: 1

| Title              | Ref Node Name | Node Name | Ref Edge | Edge | Reference Time(s) | Time(s)      | Delay(s)     |
|--------------------|---------------|-----------|----------|------|-------------------|--------------|--------------|
| <a href="#">d1</a> | out8          | out1      | rise     | fall | 1.195470e-07      | 1.911900e-07 | 7.164300e-08 |

## Dynamic Floating Node Statistical Check

### Syntax

```
title dyn_float_tran_stat domains=[domain_pair_1 domain_pair_2...]
 ping_start=<value> ping_count=<value> ping_duration=<value>
 ping_ibias=<value> ping_iabsthresh=<value> ping_iabsthresh_ramp=<value>
 ping_irelthresh=<value> seed=<value> domain_voltage_thresh=<value>
 save=[no|all|ping] distribute=[no|fork] numprocesses=<value>
 report_top_current=<value> ping_resistor_max=<value>
 ping_duration_max=<value> ping_resistor_min=<value> time_constant=<value>
 node=[node1 node2...] xnode=[node1 node2...] <inst=[inst1 inst2...]>
 <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1
 xsubckt2....]> ping_voltage_thresh=<value> ping_index =[value1 value2 ...]
 domain_detection_voltage_atol=<value>
```

### Description

The `dyn_float_tran_stat` check reports leaky MOSFETs/BJTs caused by floating nodes. It also detects floating nodes caused by other floating nodes.

The check deploys a statistical method of forcing (pinging) different voltages on the gate of MOSFET and the base of BJT. Ping refers to randomly forcing a node to 0 or VDD, or ramping from 0 to VDD. Only MOSFET gates or BJT base nodes are pinged. Ping is realized by applying a voltage source in series with a large resistor (`ping_resistor`) on each node. The strength of a ping is weaker (because of large `ping_resistor`) than other drivers on each node.

### *dyn\_float\_tran\_stat* Algorithm

- Transient simulation is run till `ping_start`.
- Qualified nodes are identified to exercise pings according to domains
- For each qualified node, `domain_voltage` is evaluated
- Pings are created randomly using seed value. One third of the qualified nodes are selected for HIGH. One third of qualified nodes are selected for LOW. One third of qualified nodes are selected for RAMP.
- `ping_duration` and `ping_resistor` are evaluated
- Pings are applied sequentially at `ping_start`.
- For each ping:

- ❑ All MOSFET drain currents and BJT collector currents are stored as reference current ( $I_{ref}$ ) right before applying the ping
- ❑ For the first half of `ping_duration`:
  - HIGH/LOW to each node is forced through a resistor with `ping_resistor` value.
  - Device current ( $I_{ping}$ ) is checked at 0.95 of 0.5\*`ping_duration`. A fail is detected if:
 
$$|I_{ref} - I_{ping}| > \max(\text{ping\_iabsthresh}, \text{ping\_irelthresh} * \min(|I_{ref}|, |I_{ping}|))$$
- ❑ For the second half of `ping_duration`:
  - The RAMP is forced to each node through a resistor with the `ping_resistor` value and the maximum ( $I_{ping,max}$ ) and minimum ( $I_{ping,min}$ ) device current is checked during the RAMP. A fail is detected in any of the following cases:
 
$$|I_{ref} - I_{ping,max}| > \max(\text{ping\_iabsthresh\_ramp}, \text{ping\_irelthresh} * \min(|I_{ref}|, |I_{ping,max}|))$$

$$|I_{ref} - I_{ping,min}| > \max(\text{ping\_iabsthresh\_ramp}, \text{ping\_irelthresh} * \min(|I_{ref}|, |I_{ping,min}|))$$

The results are written to the `dynamic.xml` file, which can be viewed in a Web browser.

## Arguments

|                            |                                                                                                                                                                                                                                                                                               |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>domains</code>       | Pairs of power-supply domains in which the floating nodes are checked. For example, <code>domains=[VDD VSS VPP VSS]</code> . The domain also defines the domain voltage ( <code>domain_voltage</code> ) value for forcing node voltages. Default value is none. Wildcarding is not supported. |
| <code>ping_start</code>    | The time at which the check is initiated.                                                                                                                                                                                                                                                     |
| <code>ping_count</code>    | The number of statistical periods being used. The default value is 300. If the <code>ping_index</code> argument is also specified, <code>ping_count</code> is ignored.                                                                                                                        |
| <code>ping_duration</code> | <p>The duration of a ping. A ping consists of the following two phases</p> <ul style="list-style-type: none"> <li>■ high/low forcing phase</li> <li>■ ramp up forcing phase</li> </ul> <p>The length of each phase is half the ping duration. Default value is none.</p>                      |

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|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>ping_ibias</code>            | Lowest bias current in the design. It is recommended to set this parameter to 10% of bias current in the design. The default value is none. If specified, then <code>ping_resistor</code> is evaluated to be equal to <code>domain_voltage/ping_ibias</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <code>ping_iabsthresh</code>       | The current threshold for floating node detection during high/low forcing. The default value is <code>domain_voltage/ping_resistor</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <code>ping_iabsthresh_ramp</code>  | The current threshold for floating node detection during ramp forcing. The default value is <code>100 * domain_voltage/ping_resistor</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <code>ping_irelthresh</code>       | The relative threshold for floating node detection for both high/low and ramp forcing. The default value is 1000.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>seed</code>                  | The seed value for random number generation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <code>domain_voltage_thresh</code> | The lowest threshold for domain voltage. If a node has voltage less than <code>domain_voltage_thresh</code> , it is excluded from the ping. The default value is 0.0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <code>save</code>                  | <p>Probes the gate voltage of MOSFETs, base voltage of BJTs, drain current of MOSFETs, and collector current of BJTs. If the value is set to <code>ping</code>, <code>netlist</code>, or <code>all</code>, a new waveform file is written in the raw directory. The format of the waveform file is <code>&lt;CheckName&gt;_&lt;PingStart&gt;.tran.tran</code>, where <i>CheckName</i> is the name of the check and <i>PingStart</i> is time from <i>PingStart</i> up to the time the ping simulation is finished. If the value is set to <code>ping</code>, only ping voltages and MOS/BJT currents are saved. If the value is set to <code>netlist</code>, the signals mentioned in the netlist are saved. If set to <code>all</code>, both the signals in the <code>save=ping</code> and the ones saved in the netlist are saved.</p> <p>The default value is <code>no</code>. Possible values are <code>ping</code>, <code>no</code>, <code>all</code>, and <code>netlist</code>.</p> |
| <code>distribute</code>            | The distributed processing method. Possible values are <code>lsf</code> , <code>no</code> and <code>fork</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>numprocesses</code>          | The number of processes for distributed processing.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>report_top_current</code>    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

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The number of top  $n$  devices with the largest leakage current to be reported. If the value is set to 0, the report contains all the devices.

`ping_duration_max`

The maximum value of the applied `ping_duration`. The default value is `none`.

`ping_resistor_max`

The maximum value of the applied `ping_resistor`. The default value is 10G.

`ping_resistor_min`

The minimum value of the applied `ping_resistor`. The default value is 100M.

`time_constant`

Time constant. The default value is 6.

`node`

Node to which the check is applied. Default is `none`.

`xnode`

Nodes to be excluded from the check. Default is `none`.

`inst`

Subcircuit instances to which the circuit check is applied. Default is `inst=*`

`xinst`

Subcircuit instances that are excluded from the circuit check. Default is `none`.

`subckt`

Instances of the specified subcircuit to which the circuit checks are applied. Default is `subckt=*`.

`xsubckt`

Instances of the specified subcircuit which are excluded from the circuit checks. Default is `none`.

`ping_voltage_thresh`

The threshold for the ping voltage. The default value is 0.

`ping_index`

Selectively re-ping a circuit with a list of pings. The default value is `none`.

`domain_detection_voltage_atol`



The voltage tolerance for voltage-based domain detection. When finding the nodes connected to VDD, the next node is marked if its voltage minus the value specified using the `domain_detection_voltage_ultol` argument is less than the voltage of the current node. Similarly, when finding the nodes connected to VSS, the next node is marked if its voltage plus the value specified using the `domain_detection_voltage_ultol` argument is greater than the voltage of the current node.

The default value is 1e-20.

## Example

```
dynSta1 dyn_float tran_stat domains=["vdd" "vss"] ping_start=[5n] ping_count=27
ping_duration=6e-06 ping_ibias=1.1e-07 ping_iabsthresh=1e-07
ping_iabsthresh_ramp=1e-07 ping_irelthresh=1000 save=all
```

The above command statistically forces (ping) certain voltages on all MOSFET gates in vdd-vss domain. If there is current difference before (Ref Current) and after (Current at Failure) the application of ping, then it is considered as violation.

The following is an example of the report that is displayed on the Web browser:

### Dynamic Statistical High Impedance Node based on FORCE transient analysis

| Title                   | Ping Index | Start Time(s) |
|-------------------------|------------|---------------|
| <a href="#">dynSta1</a> | 1          | 5.000000e-09  |

### Eleminfo datas: size=2

| Instance | Ref Current(A) | Current at Failure(A) | Voltage at Failure(V) | Time of Failure(s) | Gate Base Node | Ping Applied |
|----------|----------------|-----------------------|-----------------------|--------------------|----------------|--------------|
| MP1      | -2.019650e-10  | -2.702495e-05         | 5.356743e-01          | 4.606799e-06       | N1             | RAMPUP       |
| MN1      | 1.004048e-10   | 2.706917e-05          | 5.356743e-01          | 4.606799e-06       | N1             | RAMPUP       |

## Dynamic Uninitialized Check

### Syntax

```
title dyn_uninilatch_check node=[node1 node2...] <inst=[inst1 inst2...]>
 <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2...]> <xsubckt=[xsubckt1
 xsubckt2...]> error_limit=<value>
```

## Description

The `dyn_uninilatch` check detects the uninitialized latch nodes that have more than one DC solution. The check reports all nodes in a potential loop.

The results are written to the `dynamic.xml` file, which can be viewed in a Web browser.

The `dyn_uninilatch` check is supported only in Spectre XPS FastSPICE. See [Chapter 4, “The Spectre XPS Circuit Simulator”](#).

## Arguments

|                          |                                                                                                                   |
|--------------------------|-------------------------------------------------------------------------------------------------------------------|
| <code>node</code>        | Nodes to which the check is applied. Default is <code>none</code> .                                               |
| <code>inst</code>        | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                        |
| <code>xinst</code>       | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                     |
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> . |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .  |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                        |

## Example

```
chk2 dyn_uninilatch node=[*] inst=[x1 x2] time_window=[0n 20n]
```

## Static Checks

Static checks are performed after parsing, using the topology information and voltage propagation. They apply to digital and SRAM circuits only and do not require a transient simulation. Static checks use the `static_` keyword prefix and write the results into a file with the extension `.static.xml`. The xml file can be viewed with any Web browser.

**Note:** Static checks are supported only in Spectre APS, Spectre X, Spectre XPS SPICE, Spectre XPS FastSPICE, and Spectre MS. These static circuit checks are not supported in Spectre.

- [Static High Impedance Node Check](#) on page 752
- [Static DC Leakage Path Check](#) on page 754
- [Static NMOS/PMOS Forward Bias Bulk Check \(NMOS, PMOS\)](#) on page 757
- [Static Voltage Domain Device Check](#) on page 760
- [Static Transmission Gate Check](#) on page 764
- [Static Always Conducting NMOS/PMOS Check \(NMOS, PMOS\)](#) on page 765
- [Static MOSFET Voltage Check](#) on page 768
- [Static Resistor Voltage Check](#) on page 771
- [Static Capacitor Voltage Check](#) on page 774
- [Static Diode Voltage Check](#) on page 777
- [Static Resistor Check](#) on page 780
- [Static Capacitor Check](#) on page 782
- [Static ERC Check](#) on page 784
- [Static RC Delay Check](#) on page 787
- [Static Subcircuit Port Voltage Check](#) on page 790
- [Static Stack Count](#) on page 793
- [Static Coupling Impact Check](#) on page 795
- [Static PMOS to GND Count Check](#) on page 798
- [Static NMOS to VDD Count Check](#) on page 800
- [Static Highfanout Check](#) on page 803

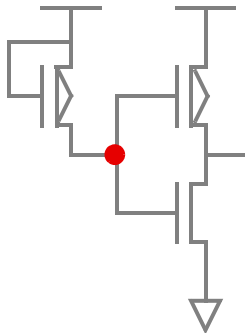
## Static High Impedance Node Check

### Syntax

```
title static_highz node=[n1 n2 ...] vnth=<value> vpth=<value>
 vsrctnodefile=[[subckt]...] "NV_FILE1" [subckt2 "NV_FILE2" subckt3 "NV_FILE3"
 ...]] <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1
 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]>
 <fanout=all|gate|bulk|gate_has_driver_no_moscap|bulkgate_no_moscap>
 pw1_time=<value> <depth=n> error_limit=<value>
 <rpt_node=no|all|top|selected>
```

### Description

Reports nodes without a possible conducting path to a DC power supply or ground. The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



### Arguments

|        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| node   | Nodes to be checked for the highz state. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                |
| fanout | Fanout setting to filter node with specified connection. When set to <code>gate_has_driver_no_moscap</code> , floating nodes only connecting to MOSCAPs will not be checked. When set to <code>gate_no_moscap</code> , gates only connecting to MOSCAPs will not be checked. Possible values are <code>all</code> , <code>gate</code> , <code>bulk</code> , <code>gate_has_driver_no_moscap</code> , and <code>bulkgate_no_moscap</code> . Default is <code>all</code> . |

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|                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>rpt_node</code>     | <p>Report node voltages. If set to <code>no</code>, no node voltages are reported. If set to <code>all</code>, all node voltages are reported. If set to <code>top</code>, voltages of only the top-level nodes are reported. If set to <code>selected</code>, voltages of only the specified nodes are reported. The report is written to a file named <code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code>.</p> <p>Possible values are <code>no</code>, <code>all</code>, <code>top</code>, and <code>selected</code>. The default value is <code>no</code>.</p>                                                                                                                                                                               |
| <code>vpth</code>         | <p>PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (the default value is -0.4 v).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>vnth</code>         | <p>NMOS threshold voltage. This value is used to calculate the voltage drop across a NMOS channel during voltage propagation (the default value is 0.5 v).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>vsrncodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrncodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these <code>vsrncodefile</code> node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrncodefile=["NV_FILE0"]</code></p> <p>Default is <code>" [...]"</code>.</p> |
| <code>pwl_time</code>     | <p>If specified, all <code>pwl</code> sources are considered constant sources with a value equal to the voltage of the <code>pwl</code> source at <code>pwl_time</code>. Default is infinity.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <code>error_limit</code>  | <p>Maximum number of errors to be reported. Default is 10000.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <code>inst</code>         | <p>Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <code>xinst</code>        | <p>Subcircuit instances that are excluded from the circuit check. Default is <code>none</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>subckt</code>       | <p>Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <code>xsubckt</code>      | <p>Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

depth                      Hierarchy level (from top level) to be checked. depth=3 reports errors on top level plus 3 sublevels. Default is 8.

**Example**

```
static_hz1 static_highz node=["*"]
```

The above command will report all possible high impedance nodes. The following is an example of the report that is displayed in the Web browser:

Static HighZ Node Check Violations

static\_highz: static\_hz1

static\_hz1 static\_highz node=["\*"]

Violation Count: 1

Static HighZ Node Check - Violation

| Title                      | Node Name |
|----------------------------|-----------|
| <a href="#">static_hz1</a> | inp       |

**Static DC Leakage Path Check**

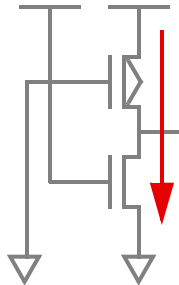
**Syntax**

```
title static_dcpath net=[n1 n2 ...] vnth=<value> vpth=<value>
vsrnodefile=[[subckt]...] pwl_time=<value> error_limit=<value>
<rpt_node=no|all|top|selected>
```

**Description**

Reports the always conducting paths between the power supply nodes. If more than two nets are specified, Spectre checks the leakage path between each net combination. For example, if net=[vdc1 vdc2 0] is specified, then the conducting path between vdc1 and vdc2, vdc1 and 0, and vdc2 and 0 is checked.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



## Arguments

|                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>net</code>          | Hierarchical node names between which the leakage path is checked. Wildcarding is not allowed. All combination of nets are checked. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>vnth</code>         | NMOS threshold voltage. This value is used to calculate the voltage drop across a NMOS channel during voltage propagation (the default value is 0.5 v).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <code>vpth</code>         | PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (the default value is -0.4 v).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>pwl_time</code>     | If specified, all pwl sources are considered constant sources with a value equal to the voltage of the pwl source at <code>pwl_time</code> . Default is infinity.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>vsrncodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrncodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these <code>vsrncodefile</code> node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrncodefile=["NV_FILE0"]</code></p> <p>Default is " [... ] ".</p> |

`rpt_node` Report node voltages. If set to `no`, no node voltages are reported. If set to `all`, all node voltages are reported. If set to `top`, voltages of only the top-level nodes are reported. If set to `selected`, voltages of only the specified nodes are reported. The report is written to a file named `<netlist_name>.<check_name>.nv`.

Possible values are `no`, `all`, `top`, and `selected`. The default value is `no`.

`error_limit` Maximum number of errors to be reported. Default is 10000.

**Example**

```
dc1 static_dcpath net=["vdd 0"]
```

The above command will report potential DC leakage paths between the power supply nodes `vdd` and `0` . The following is an example of the report that is displayed in the Web browser:

Static DC Leakage Path Check Violations

static\_dcpath: dc1

```
dc1 static_dcpath net=["vdd" "0"]
```

Violation Count: 1

Static DC Leakage Path Check - Violation

| Title               | From Net | To Net |
|---------------------|----------|--------|
| <a href="#">dc1</a> | vdd      | 0      |

Path Elements:

mp1

mn2



## **Static NMOS/PMOS Forward Bias Bulk Check (NMOS, PMOS)**

### **Syntax**

```
title static_nmosb model=[m1 m2 ...] mode=[definite|possible] vt=<value>
 vnth=<value> vpth=<value> <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]>
 <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]>
 pwl_time=<value> vsrcnodefile=[[subckt]...] <depth=n>
 <rpt_node=no|all|top|selected> error_limit=<value>

title static_pmosb model=[m1 m2 ...] mode=[definite|possible] vt=<value>
 vnth=<value> vpth=<value> <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]>
 <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]>
 pwl_time=<value> vsrcnodefile=[[subckt]...] <depth=n>
 <rpt_node=no|all|top|selected> error_limit=<value>
```

### **Description**

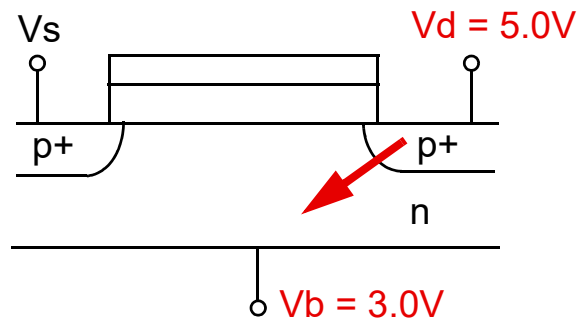
Reports MOSFET devices with forward biased bulk condition. The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser. A violation is generated when the bulk bias voltage meets the following conditions:

For NMOS:

- When mode=definite:  $\min(V_b) \geq \min(V_d, V_s) + \text{abs}(v_t)$
- When mode=possible:  $\max(V_b) \geq \min(V_d, V_s) + \text{abs}(v_t)$

For PMOS:

- When mode=definite:  $\max(V_b) \leq \max(V_d, V_s) - \text{abs}(v_t)$
- When mode=possible:  $\min(V_b) \leq \max(V_d, V_s) - \text{abs}(v_t)$



## ***Arguments***

|                       |                                                                                                                                                                                                |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>model</code>    | Model(s) to which the forward bias bulk condition is applied.<br>Default is <code>none</code> .                                                                                                |
| <code>mode</code>     | When <code>mode=possible</code> , all possible violations are reported.<br>When <code>mode=definite</code> , definite violations are reported. The<br>default value is <code>definite</code> . |
| <code>vt</code>       | Threshold voltage for p-n junction being checked (the default<br>value is 0.3 v)                                                                                                               |
| <code>vnth</code>     | NMOS threshold voltage. This value is used to calculate the<br>voltage drop across a NMOS channel during voltage propagation<br>(the default value is 0.5 v).                                  |
| <code>vpth</code>     | PMOS threshold voltage. This value is used to calculate the<br>voltage drop across a PMOS channel during voltage propagation<br>(the default value is -0.4 v).                                 |
| <code>inst</code>     | Subcircuit instances to which the circuit check is applied. Default<br>is <code>inst=*</code>                                                                                                  |
| <code>xinst</code>    | Subcircuit instances that are excluded from the circuit check.<br>Default is <code>none</code> .                                                                                               |
| <code>subckt</code>   | Instances of the specified subcircuit to which the circuit checks<br>are applied. Default is <code>subckt=*</code> .                                                                           |
| <code>xsubckt</code>  | Instances of the specified subcircuit which are excluded from the<br>circuit checks. Default is <code>none</code> .                                                                            |
| <code>pwl_time</code> | If specified, all pwl sources are considered constant sources with<br>a value equal to the voltage of the pwl source at <code>pwl_time</code> .<br>Default is infinity.                        |

|                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>vsrncodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrncodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these <code>vsrncodefile</code> node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrncodefile=["NV_FILE0"]</code>.</p> <p>Default is " [...] ".</p> |
| <code>depth</code>        | <p>Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <code>rpt_node</code>     | <p>Report node voltages. If set to <code>no</code>, no node voltages are reported. If set to <code>all</code>, all node voltages are reported. If set to <code>top</code>, voltages of only the top-level nodes are reported. If set to <code>selected</code>, voltages of only the specified nodes are reported. The report is written to a file named</p> <p><code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code>.</p> <p>Possible values are <code>no</code>, <code>all</code>, <code>top</code>, and <code>selected</code>. The default value is <code>no</code>.</p>                                                                                                                                                             |
| <code>error_limit</code>  | <p>Maximum number of errors to be reported. Default is 10000.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### **Example**

```
nmosb1 static_nmosb model=["nmos"]
```

The above command will report all instances of the `nmos` model with potential forward bias bulk conditions. The following is an example of the report that is displayed in the Web browser:

### Static Forward Bias Bulk Check Violations

#### static\_nmosb: nmosb1

```
nmosb1 static_nmosb model=["nmos"]
```

Violation Count: 1

#### Static Forward Bias Bulk Check - Violation

| Title                  | Instance Name | Model Name | Sub Name | Vd       | Vg       | Vs       | Vb       |
|------------------------|---------------|------------|----------|----------|----------|----------|----------|
| <a href="#">nmosb1</a> | x1.mn1        | nmos       | inv      | ( 0, 3 ) | ( 0, 3 ) | ( 0, 0 ) | ( 3, 3 ) |

### Static Voltage Domain Device Check

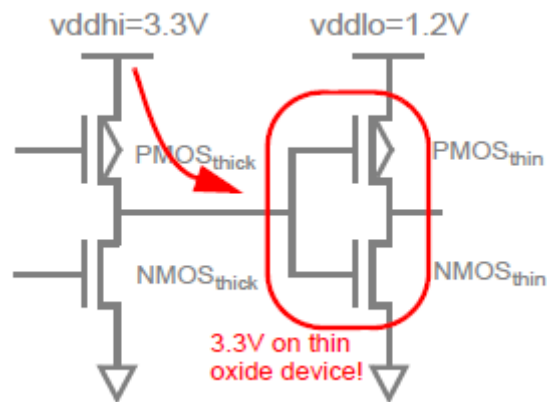
#### Syntax

```
title static_voltdomain model=[m1 m2 ...] <inst=[inst1 inst2...]> <xinst=[xinst1
xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]>
pwl_time=<value> vsrnodefile=[[subckt]...] <depth=n>
<rpt_node=no|all|top|selected> error_limit=<value>
```

#### Description

Reports high voltage driving the low-voltage MOSFETS and low voltage driving the high-voltage MOSFETS.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



## Arguments

|                       |                                                                                                                                                                   |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>model</code>    | MOSFET device model names to be checked. By default, all types of MOSFETs are checked.                                                                            |
| <code>inst</code>     | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                        |
| <code>xinst</code>    | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                     |
| <code>subckt</code>   | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                 |
| <code>xsubckt</code>  | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                  |
| <code>pwl_time</code> | If specified, all pwl sources are considered constant sources with a value equal to the voltage of the pwl source at <code>pwl_time</code> . Default is infinity. |

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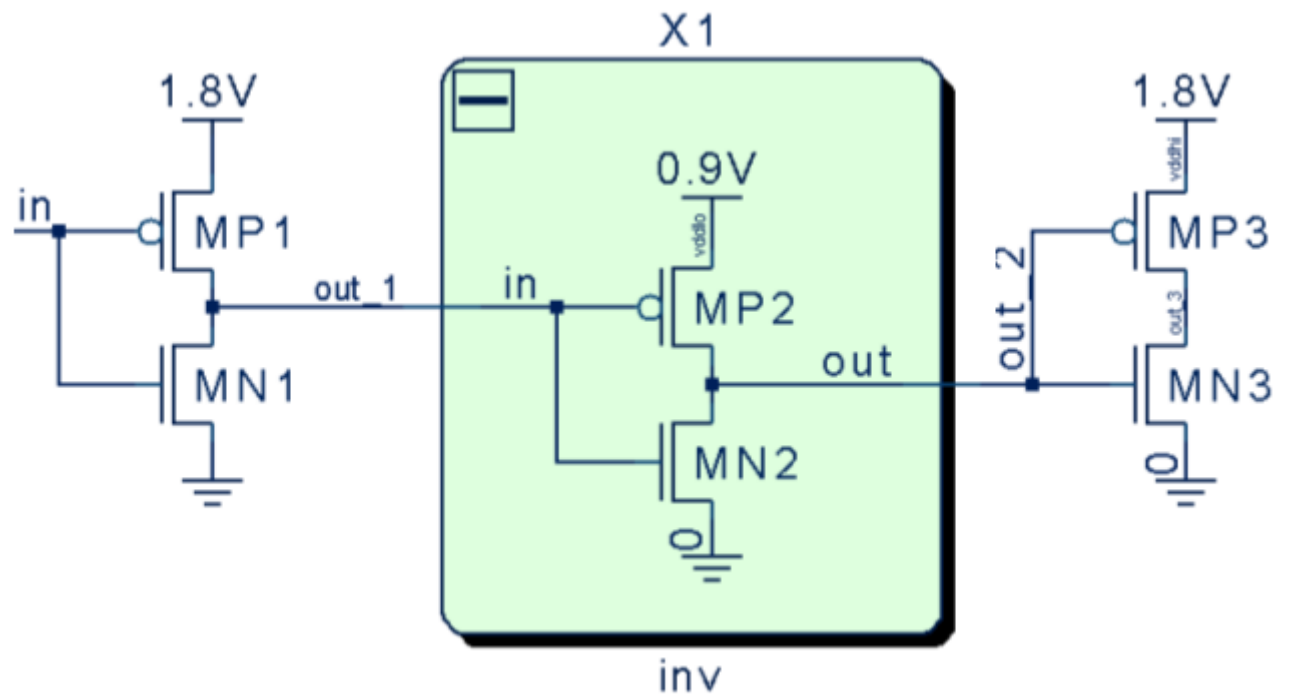
|                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>vsrncodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrncodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these <code>vsrncodefile</code> node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrncodefile=["NV_FILE0"]</code>.</p> <p>Default is " [...] ".</p> |
| <code>depth</code>        | <p>Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <code>rpt_node</code>     | <p>Report node voltages. If set to <code>no</code>, no node voltages are reported. If set to <code>all</code>, all node voltages are reported. If set to <code>top</code>, voltages of only the top-level nodes are reported. If set to <code>selected</code>, voltages of only the specified nodes are reported. The report is written to a file named</p> <p><code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code>.</p> <p>Possible values are <code>no</code>, <code>all</code>, <code>top</code>, and <code>selected</code>. The default value is <code>no</code>.</p>                                                                                                                                                             |
| <code>error_limit</code>  | <p>Maximum number of errors to be reported. Default is 10000.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### Example

```
chk1 static_voltdomain model=[*]
```

The above command will check all instances of MOSFETS. The *HighV Driving LowV* table reports MOSFETs whose gate voltage is higher than the drain/source voltage. The *LowV*

*Driving HighV* table reports MOSFETs whose gate voltage is lower than the drain/source voltage.



The following is an example of the report that is displayed in the Web browser:

Static Voltage Domain Device Check - HighV Driving LowV

| Title                | Gate Name | Instance Name | Subckt Name | Vd         | Vg         | Vs           | Vb           |
|----------------------|-----------|---------------|-------------|------------|------------|--------------|--------------|
| <a href="#">chk1</a> | out_1     | X1.MN2        | inv         | ( 0, 0.9 ) | ( 0, 1.8 ) | ( 0, 0 )     | ( 0, 0 )     |
| <a href="#">chk1</a> | out_1     | X1.MP2        | inv         | ( 0, 0.9 ) | ( 0, 1.8 ) | ( 0.9, 0.9 ) | ( 0.9, 0.9 ) |

Static Voltage Domain Device Check - LowV Driving HighV

| Title                | Gate Name | Instance Name | Subckt Name | Vd         | Vg         | Vs           | Vb           |
|----------------------|-----------|---------------|-------------|------------|------------|--------------|--------------|
| <a href="#">chk1</a> | in        | MN1           | N/A         | ( 0, 1.8 ) | ( 0, 0.9 ) | ( 0, 0 )     | ( 0, 0 )     |
| <a href="#">chk1</a> | out_2     | MN3           | N/A         | ( 0, 1.8 ) | ( 0, 0.9 ) | ( 0, 0 )     | ( 0, 0 )     |
| <a href="#">chk1</a> | in        | MP1           | N/A         | ( 0, 1.8 ) | ( 0, 0.9 ) | ( 1.8, 1.8 ) | ( 1.8, 1.8 ) |
| <a href="#">chk1</a> | out_2     | MP3           | N/A         | ( 0, 1.8 ) | ( 0, 0.9 ) | ( 1.8, 1.8 ) | ( 1.8, 1.8 ) |

Note that the *Subckt Name* is the name of subcircuit containing the instance `X1 . MN2`. This helps in locating level-shifters. If an instance is at the top-level then *Subckt Name* will show N/A.

## Static Transmission Gate Check

### Syntax

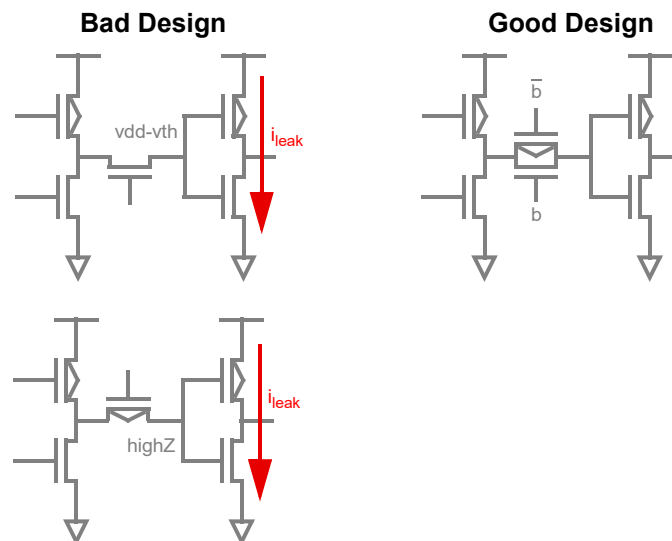
```
title static_tgate node=[n1 n2 ...] <inst=[inst1 inst2...]> <xinst=[xinst1
 xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]>
 <depth=n> error_limit=<value>
```

### Description

Reports transmission gates which may cause potential leakage currents between power supplies. Such gates can be characterized by their node connectivity, based on the following:

- Nodes which connect to gate and NMOS drain/source terminals, but not to PMOS drain/source terminals
- Nodes which connect to gate and PMOS drain/source terminals, but not to NMOS drain/source terminals

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



### Arguments

`node` Nodes to be checked. Default is none.



|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| inst        | Subcircuit instances to which the circuit check is applied. Default is inst=*                                       |
| xinst       | Subcircuit instances that are excluded from the circuit check. Default is none.                                     |
| subckt      | Instances of the specified subcircuit to which the circuit checks are applied. Default is subckt=*                  |
| xsubckt     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is none.                  |
| depth       | Hierarchy level (from top level) to be checked. depth=3 reports errors on top level plus 3 sublevels. Default is 8. |
| error_limit | Maximum number of errors to be reported. Default is 10000.                                                          |

Example

```
tgate1 static_tgate node=["*"]
```

The above command will report all nodes connecting to transmission gates that may cause design problems like leakage currents. The following is an example of the report that is displayed in the Web browser:

Static Transfer Gate Check Violations

static\_tgate: tgate1

- tgate1 static\_tgate node=["\*"]
- Violation Count: 2

| Title                  | Node Name |
|------------------------|-----------|
| <a href="#">tgate1</a> | in2       |
| <a href="#">tgate1</a> | in4       |

Static Always Conducting NMOS/PMOS Check (NMOS, PMOS)

Syntax

```
title static_nmosvgs model=[m1 m2 ...] vnth=<value> vpth=<value> vt=<value>
 <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1
 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> pwl_time=<value>
 vsrnodefile=[[subckt]...] <depth=n> <rpt_node=no|all|top|selected>
 error_limit=<value>
```

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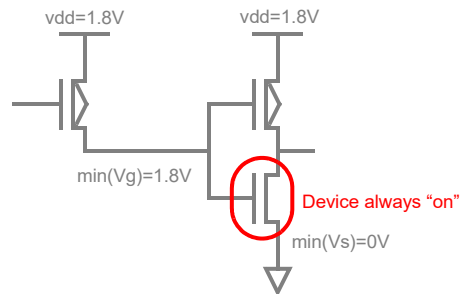
```
title static_pmosvgs model=[m1 m2 ...] vnth=<value> vpth=<value> vt=<value>
 <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1
 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> pwl_time=<value>
 vsrcnodefile=[[subckt]...] <depth=n> <rpt_node=no|all|top|selected>
 error_limit=<value>
```

## Description

Reports MOSFET devices potentially always conducting due to connectivity problems. The following conditions are checked, and an error is reported if they are fulfilled:

- NMOS:  $\min(V_g) > \min(V_s/V_d) + \text{abs}(v_t)$
- PMOS:  $\max(V_g) < \max(V_s/V_d) - \text{abs}(v_t)$

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



## Arguments

|       |                                                                                                                                                          |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| model | MOSFET device model names to be checked. Default is <code>none</code> .                                                                                  |
| vnth  | NMOS threshold voltage. This value is used to calculate the voltage drop across a NMOS channel during voltage propagation (the default value is 0.5 v).  |
| vpth  | PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (the default value is -0.4 v). |
| vt    | MOSFET threshold voltage. Default is 0V.                                                                                                                 |
| inst  | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                               |
| xinst | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                            |

## Spectre Classic Simulator, Spectre APS, Spectre X, Spectre XPS, Spectre FMC Analysis, and Legato Reliability Solution User Guide

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|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>subckt</code>      | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>xsubckt</code>     | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <code>pwl_time</code>    | If specified, all pwl sources are considered constant sources with a value equal to the voltage of the pwl source at <code>pwl_time</code> . Default is infinity.                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>rpt_node</code>    | Report node voltages. If set to <code>no</code> , no node voltages are reported. If set to <code>all</code> , all node voltages are reported. If set to <code>top</code> , voltages of only the top-level nodes are reported. If set to <code>selected</code> , voltages of only the specified nodes are reported. The report is written to a file named <code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code> .<br><br>Possible values are <code>no</code> , <code>all</code> , <code>top</code> , and <code>selected</code> . The default value is <code>no</code> . |
| <code>depth</code>       | Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <code>error_limit</code> | Maximum number of errors to be reported. Default is 10000.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

### Example

```
mos1 static_nmosvgs model="nmos" vt=0.5
```

The above command will check all instances of the nmos device for a potential "always on" state. The NMOS `vt` is defined with 500mV.

The following is an example of the report that is displayed in the Web browser:

## Static Always Conducting MOSFET Check Violations

### static\_nmosvgs: mos1

mos1 static\_nmosvgs model=["nmos"] vt=0.5

Violation Count: 1

#### Static Always Conducting MOSFET Check - Violation

| Title                | Instance Name | Model Name | Sub Name | Vd       | Vg           | Vs       | Vb       |
|----------------------|---------------|------------|----------|----------|--------------|----------|----------|
| <a href="#">mos1</a> | x2.mn2        | nmos       | inv      | ( 0, 0 ) | ( 1.8, 1.8 ) | ( 0, 0 ) | ( 0, 0 ) |

## Static MOSFET Voltage Check

### Syntax

```
title static_mosv model=[m1 m2 ...] cond=<expression>
 <rpt_node=no|all|top|selected> vnth=<value> vpth=<value> pwl_time=<value>
 vsrnodefile=[[subckt]...] vsrnodefile=[[subckt1] "NV_FILE1" [subckt2
 "NV_FILE2" subckt3 "NV_FILE3" ...]] error_limit=<value> <inst=[inst1
 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]>
 <xsubckt=[xsubckt1 xsubckt2....]> <depth=n>
```

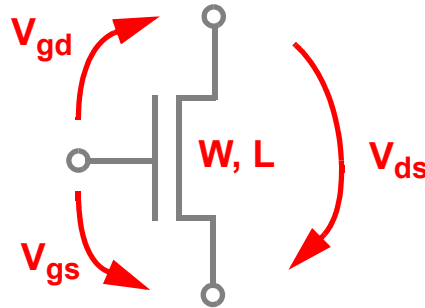
### Description

Reports MOSFET devices fulfilling the conditional expression on device voltages and device size (w, l).

Supported MOSFET variables are:  $v(g,s)$ ,  $v(g,d)$ ,  $v(g,b)$ ,  $v(d,s)$ ,  $v(d,b)$ ,  $v(s,b)$ ,  $v(g)$ ,  $v(d)$ ,  $v(s)$ ,  $v(b)$ , l, and w.

Supported operators are: +, -, \*, /, ==, !=, <, <=, >, >=, ||, &&, and !.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



## Design Check Parameters

|                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>model</code>    | MOSFET device model names to be checked.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>cond</code>     | Condition to be checked                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>rpt_node</code> | <p>Report node voltages. If set to <code>no</code>, no node voltages are reported. If set to <code>all</code>, all node voltages are reported. If set to <code>top</code>, voltages of only the top-level nodes are reported. If set to <code>selected</code>, voltages of only the specified nodes are reported. The report is written to a file named</p> <p><code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code>.</p> <p>Possible values are <code>no</code>, <code>all</code>, <code>top</code>, and <code>selected</code>. The default value is <code>no</code>.</p> |

## Digitize Parameters

|                       |                                                                                                                                                                         |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>vnth</code>     | NMOS threshold voltage. This value is used to calculate the voltage drop across a NMOS channel during voltage propagation (the default value is 0.5 v).                 |
| <code>vpth</code>     | PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (the default value is -0.4 v).                |
| <code>pwl_time</code> | <p>If specified, all pwl sources are considered constant sources with a value equal to the voltage of the pwl source at <code>pwl_time</code>. Default is infinity.</p> |

`vsrncodefile` Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a `vsrncodefile` file with the `rpt_node` feature, then you can reuse these `vsrncodefile` node voltages.

The subcircuit name and the related `NV_FILE` need to be specified in pairs. The node voltages from the `NV_FILE` are applied to the nodes inside the given subcircuit. If the first `NV_FILE` is given without a subcircuit name, then it is applied to the top level. For example, `vsrncodefile=["NV_FILE0"]`.

Default is " [ . . . ] ".

## Filtering Parameters

`error_limit` Maximum number of errors to be reported. Default is 10000.

## Wildcard Scoping

`inst` Subcircuit instances to which the circuit check is applied. Default is `inst=*`

`xinst` Subcircuit instances that are excluded from the circuit check. Default is `none`.

`subckt` Instances of the specified subcircuit to which the circuit checks are applied. Default is `subckt=*`.

`xsubckt` Instances of the specified subcircuit which are excluded from the circuit checks. Default is `none`.

`depth` Hierarchy level (from top level) to be checked. `depth=3` reports errors on top level plus 3 sublevels. Default is 8.

## Example

```
mos1 static_mosv model="nmos" cond="v(g,s)>1.9"
```

The above command will report the instances of `nmos` that fulfill the condition `v(g,s)>1.9`.

The following is an example of the report that is displayed in the Web browser:

## Static MOSFET Voltage Check Violations

### static\_mosv: mos1

mos1 static\_mosv model=["nmos"] cond="v(g,s)>1.9"

Violation Count: 2

#### Static MOSFET Voltage Check - Violation

| Title                | Instance Name | Model Name | Sub Name | Vd         | Vg         | Vs       | Vb       |
|----------------------|---------------|------------|----------|------------|------------|----------|----------|
| <a href="#">mos1</a> | x1.mn2        | nmos       | invhi    | ( 0, 3.3 ) | ( 0, 3.3 ) | ( 0, 0 ) | ( 0, 0 ) |
| <a href="#">mos1</a> | x2.mn2        | nmos       | inv      | ( 0, 1.8 ) | ( 0, 3.3 ) | ( 0, 0 ) | ( 0, 0 ) |

## Static Resistor Voltage Check

### Syntax

```
title static_resv cond=<expression> <inst=[inst1 inst2...]> vnth=<value>
 vpth=<value> <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]>
 <xsubckt=[xsubckt1 xsubckt2....]> pwl_time=<value>
 vsrnodefile=[[subckt]...] <depth=n> <rpt_node=no|all|top|selected>
 error_limit=<value>
```

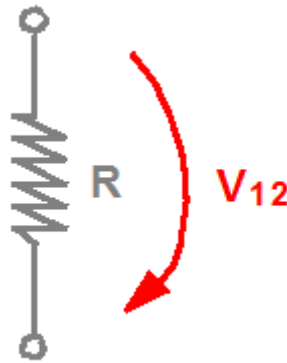
### Description

Reports resistor elements fulfilling the conditional expression on device voltages.

Supported resistor variables are:  $v(1,2)$ ,  $v(1)$ , and  $v(2)$ .

Supported operators are: +, -, \*, /, ==, !=, <, <=, >, >=, ||, &&, and !.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



### Arguments

|                       |                                                                                                                                                                   |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>cond</code>     | Condition to be checked                                                                                                                                           |
| <code>vnth</code>     | NMOS threshold voltage. This value is used to calculate the voltage drop across a NMOS channel during voltage propagation (the default value is 0.5 v).           |
| <code>vpth</code>     | PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (the default value is -0.4 v).          |
| <code>inst</code>     | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                        |
| <code>xinst</code>    | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                     |
| <code>subckt</code>   | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                 |
| <code>xsubckt</code>  | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                  |
| <code>pwl_time</code> | If specified, all pwl sources are considered constant sources with a value equal to the voltage of the pwl source at <code>pwl_time</code> . Default is infinity. |



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|                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>vsrncodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrncodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these <code>vsrncodefile</code> node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrncodefile=["NV_FILE0"]</code>.</p> <p>Default is " [...] ".</p> |
| <code>depth</code>        | <p>Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <code>rpt_node</code>     | <p>Report node voltages. If set to <code>no</code>, no node voltages are reported. If set to <code>all</code>, all node voltages are reported. If set to <code>top</code>, voltages of only the top-level nodes are reported. If set to <code>selected</code>, voltages of only the specified nodes are reported. The report is written to a file named</p> <p><code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code>.</p> <p>Possible values are <code>no</code>, <code>all</code>, <code>top</code>, and <code>selected</code>. The default value is <code>no</code>.</p>                                                                                                                                                             |
| <code>error_limit</code>  | <p>Maximum number of errors to be reported. Default is 10000.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### Example

```
resv1 static_resv cond="v(1,2)>0
```

The above command will report the resistor elements that fulfill the condition `v(1,2)>0`.

The following is an example of the report that is displayed in the Web browser:

## Static Resistor Voltage Check Violations

### static\_resv: resv1

resv1 static\_resv cond="v(1,2)>0"

Violation Count: 1

#### Static Resistor Voltage Check - Violation

| Title                 | Instance Name | Model Name | Sub Name | V1         | V2         |
|-----------------------|---------------|------------|----------|------------|------------|
| <a href="#">resv1</a> | r1            | resistor   | -        | ( 0, 3.3 ) | ( 0, 3.3 ) |

## Static Capacitor Voltage Check

### Syntax

```
title static_capv cond=<expression> <inst=[inst1 inst2...]> vnth=<value>
 vpth=<value> <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]>
 <xsubckt=[xsubckt1 xsubckt2....]> pwl_time=<value>
 vsrnodefile=[[subckt]...] <depth=n> <rpt_node=no|all|top|selected>
 error_limit=<value>
```

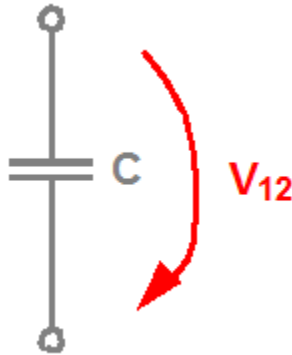
### Description

Reports capacitor elements fulfilling the conditional expression on device voltages.

Supported capacitor variables are:  $v(1,2)$ ,  $v(1)$ , and  $v(2)$ .

Supported operators are: +, -, \*, /, ==, !=, <, <=, >, >=, ||, &&, and !.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



## Arguments

|                       |                                                                                                                                                                   |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>cond</code>     | Condition to be checked                                                                                                                                           |
| <code>vnth</code>     | NMOS threshold voltage. This value is used to calculate the voltage drop across a NMOS channel during voltage propagation (the default value is 0.5 v).           |
| <code>vpth</code>     | PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (the default value is -0.4 v).          |
| <code>inst</code>     | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                        |
| <code>xinst</code>    | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                     |
| <code>subckt</code>   | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                 |
| <code>xsubckt</code>  | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                  |
| <code>pwl_time</code> | If specified, all pwl sources are considered constant sources with a value equal to the voltage of the pwl source at <code>pwl_time</code> . Default is infinity. |

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|                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>vsrncodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrncodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these <code>vsrncodefile</code> node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrncodefile=["NV_FILE0"]</code>.</p> <p>Default is " [...] ".</p> |
| <code>depth</code>        | <p>Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level plus 3 sublevels. Default is 8.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <code>rpt_node</code>     | <p>Report node voltages. If set to <code>no</code>, no node voltages are reported. If set to <code>all</code>, all node voltages are reported. If set to <code>top</code>, voltages of only the top-level nodes are reported. If set to <code>selected</code>, voltages of only the specified nodes are reported. The report is written to a file named</p> <p><code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code>.</p> <p>Possible values are <code>no</code>, <code>all</code>, <code>top</code>, and <code>selected</code>. The default value is <code>no</code>.</p>                                                                                                                                                             |
| <code>error_limit</code>  | <p>Maximum number of errors to be reported. Default is 10000.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### Example

```
capv1 static_capv cond="v(1,2)>0
```

The above command will report the capacitor elements that fulfill the condition  $v(1,2) > 0$ . The following is an example of the report that is displayed in the Web browser:

## Static Capacitor Voltage Check Violations

### static\_capv: capv1

capv1 static\_capv cond="v(1,2)>0"

Violation Count: 1

#### Static Capacitor Voltage Check - Violation

| Title                 | Instance Name | Model Name | Sub Name | V1         | V2         |
|-----------------------|---------------|------------|----------|------------|------------|
| <a href="#">capv1</a> | c1            | capacitor  | -        | ( 0, 3.3 ) | ( 0, 3.3 ) |

## Static Diode Voltage Check

### Syntax

```
title static_diodev model=[m1 m2 ...] cond=<expression> vnth=<value> vpth=<value>
 <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1
 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> pwl_time=<value>
 vsrnodefile=[[subckt]...]<depth=n> <rpt_node=no|all|top|selected>
 error_limit=<value>
```

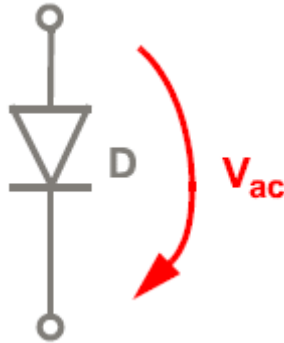
### Description

Reports diode elements fulfilling the conditional expression on device voltages.

Supported diode variables are:  $v(a,c)$ ,  $v(a)$ , and  $v(c)$ .

Supported operators are: +, -, \*, /, ==, !=, <, <=, >, >=, ||, &&, and !.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.



## Arguments

|                       |                                                                                                                                                                   |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>model</code>    | Diode device model names to be checked.                                                                                                                           |
| <code>cond</code>     | Condition to be checked (default is <code>none</code> ).                                                                                                          |
| <code>vnth</code>     | NMOS threshold voltage. This value is used to calculate the voltage drop across a NMOS channel during voltage propagation (the default value is 0.5 v).           |
| <code>vpth</code>     | PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (the default value is -0.4 v).          |
| <code>inst</code>     | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                        |
| <code>xinst</code>    | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                     |
| <code>subckt</code>   | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                 |
| <code>xsubckt</code>  | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                  |
| <code>pwl_time</code> | If specified, all pwl sources are considered constant sources with a value equal to the voltage of the pwl source at <code>pwl_time</code> . Default is infinity. |

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|                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>vsrncodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrncodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these <code>vsrncodefile</code> node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrncodefile=["NV_FILE0"]</code>.</p> <p>Default is " [...] ".</p> |
| <code>depth</code>        | <p>Hierarchy level (from top level) to be checked. <code>depth=3</code> reports errors on top level and three sublevels. Default is 8.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <code>rpt_node</code>     | <p>Report node voltages. If set to <code>no</code>, no node voltages are reported. If set to <code>all</code>, all node voltages are reported. If set to <code>top</code>, voltages of only the top-level nodes are reported. If set to <code>selected</code>, voltages of only the specified nodes are reported. The report is written to a file named</p> <p><code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code>.</p> <p>Possible values are <code>no</code>, <code>all</code>, <code>top</code>, and <code>selected</code>. The default value is <code>no</code>.</p>                                                                                                                                                             |
| <code>error_limit</code>  | <p>Maximum number of errors to be reported. Default is 10000.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### Example

```
dvl static_diodev model=["diode1"] cond="v(a,c)>0"
```

The above command will report the instances of `diode1` that fulfill the condition  $v(a, c) > 0$ . The following is an example of the report that is displayed in the Web browser:

## Static Diode Voltage Check Violations

### static\_diodev: dv1

```
dv1 static_diodev model=["diode1"] cond="v(a,c)>=0"
```

Violation Count: 2

#### Static Diode Voltage Check - Violation

| Title               | Instance Name | Model Name | Sub Name | Va               | Vc               |
|---------------------|---------------|------------|----------|------------------|------------------|
| <a href="#">dv1</a> | x1.d1         | diode1     | inv_esd  | ( 0.00 , 0.00 )  | ( -5.00 , 5.00 ) |
| <a href="#">dv1</a> | x1.d2         | diode1     | inv_esd  | ( -5.00 , 5.00 ) | ( 3.30 , 3.30 )  |

## Static Resistor Check

### Syntax

```
title static_resistor type=[range|distr|print] rmin=<value> rmax=<value>
error_limit=<value>
```

### Description

Reports all resistors within or outside the range `rmin` and `rmax`. Moreover, it also generates a distribution list of all resistors in the circuit.

If the parameter `type` is set to `range`, then all resistors outside the range of `rmin` and `rmax` will be reported.

If the parameter `type` is set to `print`, then all resistors between `rmin` and `rmax` will be reported. The resistor names can be sorted by clicking the *Device name* header.

If the parameter `type` is set to `distr` then a distribution report will be generated for all resistors. There are 12 bins that are:

-Inf - 0, 0 - 1m, 1m - 10m, 10m - 0.1, 0.1 - 1, 1 - 10, 10 - 100, 100 - 1k, 1k - 10k, 10k - 100k, 100k - 1Meg, and 1Meg - Inf



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However, if two or more consecutive bins are empty then they will merge into one bin, reducing the number of bins. The parameters `rmin`, `rmax` and `error_limit` are ignored when the parameter type is set to `distr`.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.

### Arguments

|                                                      |                                                                                                                     |
|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| <code>type=range distr</code><br><code> print</code> | Type of report requested.                                                                                           |
| <code>rmin</code>                                    | Lower bound of resistor value to be reported. Default is -1000G Ohm.                                                |
| <code>rmax</code>                                    | Upper bound of resistor value to be reported. Default is 1000G Ohm.                                                 |
| <code>error_limit</code>                             | Maximum number of errors to be reported when <code>type=print</code> or <code>type=range</code> . Default is 10000. |

### Example

```
chk1 static_resistor type=distr
```

The simulator generates a resistor value distribution report, as shown below.

## Static Resistor Check Violations

### static\_resistor: chk1

chk1 static\_resistor type=distr

Violation Count: 12

#### Static Resistor Check - Resistor Value Distribution

| Title                | Range           | Count |
|----------------------|-----------------|-------|
| <a href="#">chk1</a> | ( -Inf, 0 )     | 0     |
| <a href="#">chk1</a> | [ 0, 1 m )      | 1     |
| <a href="#">chk1</a> | [ 1 m, 10 m )   | 1     |
| <a href="#">chk1</a> | [ 10 m, 100 m ) | 1     |
| <a href="#">chk1</a> | [ 100 m, 1 )    | 1     |
| <a href="#">chk1</a> | [ 1 , 10 )      | 1     |
| <a href="#">chk1</a> | [ 10 , 100 )    | 1     |
| <a href="#">chk1</a> | [ 100 , 1 K )   | 1     |
| <a href="#">chk1</a> | [ 1 K, 10 K )   | 1     |
| <a href="#">chk1</a> | [ 10 K, 100 K ) | 1     |
| <a href="#">chk1</a> | [ 100 K, 1 M )  | 1     |
| <a href="#">chk1</a> | [ 1 M, Inf )    | 2     |

## Static Capacitor Check

### Syntax

```
title static_capacitor type=[range|distr|print] cmin=<value> cmax=<value>
 error_limit=<value>
```

### Description

Reports all capacitors within or outside the range `cmin` and `cmax`. Moreover, it also generates a distribution list of all capacitors in the circuit.

If the parameter `type` is set to `range`, then all capacitors outside the range of `cmin` and `cmax` will be reported.

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If the parameter type is set to `print`, then all capacitors between `cmin` and `cmax` will be reported. The capacitor names can be sorted by clicking the *Device name* header.

If the parameter type is set to `distr`, then a distribution report will be generated for all capacitors. There are 9 bins that are:

`-Inf - 0, 0 - 10a, 10a - 100a, 100a - 1f, 1f - 10f, 10f - 100f, 100f - 1p, 1p - 10p, 10p - Inf`

However, if two or more consecutive bins are empty then they will merge into one bin, reducing the number of bins. The parameters `cmin`, `cmax`, and `error_limit` are ignored when the parameter type is set to `distr`.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.

### Arguments

|                                                      |                                                                                                                                   |
|------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| <code>type=range distr</code><br><code> print</code> | Type of report requested.                                                                                                         |
| <code>cmin</code>                                    | Lower bound of capacitor value to be reported. Default is <code>-1F</code> .                                                      |
| <code>cmax</code>                                    | Upper bound of capacitor value to be reported. Default is <code>1F</code> .                                                       |
| <code>error_limit</code>                             | Maximum number of errors to be reported when <code>type=print</code> or <code>type=range</code> . Default is <code>10000</code> . |

### Example

```
chk1 static_capacitor type=distr
```

The simulator reports a capacitor distribution based on their value, as shown below.

## Static Capacitor Check Violations

### static\_capacitor: chk1

chk1 static\_capacitor type=distr

Violation Count: 9

#### Static Capacitor Check - Capacitor Value Distribution

| Title                | Range           | Count |
|----------------------|-----------------|-------|
| <a href="#">chk1</a> | ( -Inf, 0 )     | 0     |
| <a href="#">chk1</a> | [ 0, 10 a )     | 1     |
| <a href="#">chk1</a> | [ 10 a, 100 a ) | 1     |
| <a href="#">chk1</a> | [ 100 a, 1 f )  | 1     |
| <a href="#">chk1</a> | [ 1 f, 10 f )   | 1     |
| <a href="#">chk1</a> | [ 10 f, 100 f ) | 1     |
| <a href="#">chk1</a> | [ 100 f, 1 p )  | 1     |
| <a href="#">chk1</a> | [ 1 p, 10 p )   | 1     |
| <a href="#">chk1</a> | [ 10 p, Inf )   | 5     |

## Static ERC Check

### Syntax

```
title static_erc hotwell=[off|on] dangle=[off|all|no_top]
floatgate=[off|all|no_top|no_moscap|no_top_moscap|pode] <gate2power=off|on>
<gate2ground=on|off> floatbulk=[off|all|no_top <inst=[inst1 inst2...]>
vnth=<value> vpth=<value> vlth=<value> vhth=<value> pwl_time=<value>
vsrnodefile=[[subckt]...] <xinst=[xinst1 xinst2...]> <subckt=[subckt1
subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> error_limit=<value> <depth=n>
<rpt_node=no|all|top|selected>
```

### Description

Enables you to detect the following electrical design rule violations without running the simulation:

- MOSFET with bulk not hard-wired to power supply.

- Unconnected MOSFET gate.
- Unconnected MOSFET bulk.
- Dangling node.

The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.

### Arguments

|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>hotwell</code>     | Report MOSFET with bulk not connected to VDD or GND. Possible values are <code>off</code> and <code>on</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>dangle</code>      | Report dangling nodes. If set to <code>off</code> (default), dangling nodes are not checked. If set to <code>all</code> , all nodes are checked. If set to <code>no_top</code> , the top-level nodes are excluded from the check.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>floatgate</code>   | Report unconnected MOSFET gates. If set to <code>off</code> (default), no nodes are checked. If set to <code>all</code> , all nodes are checked. If set to <code>no_top</code> , top-level nodes are excluded from the check. If set to <code>no_moscap</code> , MOSCAP gates are excluded from the check. If set to <code>no_top_moscap</code> , all top-level nodes and the MOSCAP gates are excluded from the check. If set to <code>pode</code> , all <code>pode</code> devices whose gates are floating are reported as violations. Possible values are <code>off</code> , <code>all</code> , <code>no_top</code> , <code>no_moscap</code> , <code>no_top_moscap</code> , and <code>pode</code> . |
| <code>floatbulk</code>   | Report unconnected MOSFET bulk. If set to <code>off</code> (default), nodes are not checked. If set to <code>all</code> , all nodes are checked. If set to <code>no_top</code> , the top-level nodes are excluded from the check.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <code>gate2power</code>  | Reports PMOS with gate connected to ground and NMOS with gate connected to VDD. Possible values are <code>on</code> and <code>off</code> . The default value is <code>off</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>gate2ground</code> | Reports NMOS gate nodes connected to ground and PMOS gate nodes connected to VDD. The gate must be a <code>vsource</code> node. Possible values are <code>on</code> and <code>off</code> . The default value is <code>off</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

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|                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>rpt_node</code>     | <p>Report node voltages. If set to <code>no</code>, no node voltages are reported. If set to <code>all</code>, all node voltages are reported. If set to <code>top</code>, voltages of only the top-level nodes are reported. If set to <code>selected</code>, voltages of only the specified nodes are reported. The report is written to a file named <code>&lt;netlist_name&gt;.&lt;check_name&gt;.nv</code>.</p> <p>Possible values are <code>no</code>, <code>all</code>, <code>top</code>, and <code>selected</code>. The default value is <code>no</code>.</p>                                                                                                                                                                               |
| <code>vlth</code>         | <p>Voltage below <code>vlth</code> is considered GND. Applicable only with <code>hotwell</code>, <code>gate2ground</code>, and <code>gate2power</code>. Default is <code>0.2V</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <code>vhth</code>         | <p>Voltage above <code>vhth</code> is considered VDD. Applicable only with <code>hotwell</code>, <code>gate2ground</code>, and <code>gate2power</code>. Default value is <code>0.8V</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>vpth</code>         | <p>PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (the default value is <code>-0.4 v</code>).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>vnth</code>         | <p>NMOS threshold voltage. This value is used to calculate the voltage drop across a NMOS channel during voltage propagation (the default value is <code>0.5 v</code>).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <code>pwl_time</code>     | <p>If specified, all <code>pwl</code> sources are considered constant sources with a value equal to the voltage of the <code>pwl</code> source at <code>pwl_time</code>. Default is infinity.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <code>vsrncodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrncodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these <code>vsrncodefile</code> node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrncodefile=["NV_FILE0"]</code>.</p> <p>Default is <code>"[...]"</code>.</p> |
| <code>error_limit</code>  | <p>Maximum number of errors to be reported per check. Default is <code>10000</code>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <code>inst</code>         | <p>Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

|         |                                                                                                                        |
|---------|------------------------------------------------------------------------------------------------------------------------|
| xinst   | Subcircuit instances that are excluded from the circuit check.<br>Default is none.                                     |
| subckt  | Instances of the specified subcircuit to which the circuit checks<br>are applied. Default is subckt=*.                 |
| xsubckt | Instances of the specified subcircuit which are excluded from the<br>circuit checks. Default is none.                  |
| depth   | Hierarchy level (from top level) to be checked. depth=3 reports<br>errors on top level plus 3 sublevels. Default is 8. |

**Example**

```
chk1 static_erc floatgate=all
```

The above command reports all MOSFETs with a floating gate.

The following is an example of the report that is displayed in the Web browser:

Static ERC Check Violations

static\_erc: chk1

```
chk1 static_erc floatgate=all
```

Violation Count: 2

Static ERC Check - Floating Gate Violations

| Title                | Instance Name |
|----------------------|---------------|
| <a href="#">chk1</a> | MP1           |
| <a href="#">chk1</a> | Q1.MP1        |

Static RC Delay Check

**Syntax**

```
title static_rcdelay node=[n1 n2 ...] <detailed_path=[yes|no]>
fanoutmargin=[lower_margin higher_margin] cmin=<value> maxnrise=<value>
minnrise=<value> maxnfall=<value> minnfall=<value> maxtrise=<value>
```

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```
mintrise=<value> maxtfall=<value> mintfall=<value> <inst=[inst1 inst2...]>
<xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1
xsubckt2....]> <depth=n>
```

## Description

Reports nodes with excessive rise or fall times. Rise and fall times are based on estimation.

The `static_rcdelay` check analyzes only the fanout nodes. It does not check nodes that connect to MOSDIODEs or MOSCAPs. The check reports either the top worst case rise/fall times (`maxnrise`, `maxnfall`) or nodes with rise/fall times above the user-defined thresholds (`maxtrise`, `maxtfall`). In addition, the check reports the driving MOSFETs and the receiving MOSFET (gate connected to the analyzed node) for each node.

For postlayout netlist, the check supports only the backannotation (stitching) flow.

The results are reported into a file with the extension `static.xml`, which can be read with a Web browser.

## Arguments

|                       |                                                                                                   |
|-----------------------|---------------------------------------------------------------------------------------------------|
| <code>node</code>     | Nodes to which the check is applied. Default is none.                                             |
| <code>maxnrise</code> | Report the top number nodes with highest rise time. Default is none.                              |
| <code>minnrise</code> | Report the top number nodes with lowest rise time. Default is none.                               |
| <code>maxnfall</code> | Report the top number nodes with highest fall time. Default is none.                              |
| <code>minnfall</code> | Report the top number nodes with lowest fall time. Default is none.                               |
| <code>maxtrise</code> | Report only those node names with rise time higher than the specified value. Default is infinity. |
| <code>mintrise</code> | Report only those node names with rise time lower than the specified value. Default is none.      |
| <code>maxtfall</code> | Report only those node names with fall time higher than the specified value. Default is infinity. |
| <code>mintfall</code> | Report only those node names with fall time lower than the specified value. Default is none.      |



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|                            |                                                                                                                                                                                                                                               |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>inst</code>          | Subcircuit instances to which the circuit check is applied. Default is <code>inst=*</code>                                                                                                                                                    |
| <code>xinst</code>         | Subcircuit instances that are excluded from the circuit check. Default is <code>none</code> .                                                                                                                                                 |
| <code>subckt</code>        | Instances of the specified subcircuit to which the circuit checks are applied. Default is <code>subckt=*</code> .                                                                                                                             |
| <code>xsubckt</code>       | Instances of the specified subcircuit which are excluded from the circuit checks. Default is <code>none</code> .                                                                                                                              |
| <code>depth</code>         | Hierarchy level (starting from top, instance, or subcircuit scope) to be checked. Default is 8.                                                                                                                                               |
| <code>fanoutmargin</code>  | Relative fanout level (in ratio of VDD voltage) for which rise and fall time is measured. The range of values is <code>[0.01 0.99]</code> . The default range is <code>[0.1 0.9]</code> . Lower margin should be less than the higher margin. |
| <code>cmin</code>          | Node capacitance threshold. Only nodes with total capacitance higher than the specified value are reported. Default is <code>1e-14</code> .                                                                                                   |
| <code>detailed_path</code> | Report all possible (yes) or worst case (no) rise/fall time per node. Possible values are <code>yes</code> and <code>no</code> .                                                                                                              |

### Example

```
chk static_rcdelay node=[*] maxnrise=10 cmin=1e-14 detailed_path=no
```

The above command will estimate the RC delay for all nodes. It will report four tables, one table for each parameter. It will report the maximum (highest) two rise delays.

The following is an example of the report that is displayed in the Web browser:

## static\_rcdelay: chk

- chk static\_rcdelay node=["\*"] maxnrise=10 cmin=1e-14 detailed\_path=no
- Violation Count: 4

### Static RC Delay Check - Max Rise-time Delays

| Title               | Node Name | Delay(s)     | Receiver | Node Cap(F)  |
|---------------------|-----------|--------------|----------|--------------|
| <a href="#">chk</a> | E         | 1.217681e-09 | x_d2.mp2 | 2.029682e-13 |

### Drivers datas: size=2

| Driver   |
|----------|
| x_r1.mp2 |
| x_r1.mp1 |

## Static Subcircuit Port Voltage Check

### Syntax

```
title static_subcktport cond=<expression> vnth=<value> vpth=<value> subckt=<value>
 pw1_time=<value> vsrnodefile=[[subckt]...] error_limit=<value>
```

### Description

Reports instances of the user-specified `subckt` fulfilling the conditional expression on port voltages. Only one subcircuit is allowed per statement.

Voltages of a port can be referenced by the port name of a subcircuit. For example, consider the subcircuit definition `.subckt INV port_A port_B`. Here, supported port names are: `v(port_A)`, `v(port_B)` and `v(port_A,port_B)`.

Supported operators are: `+`, `-`, `*`, `/`, `==`, `!=`, `<`, `<=`, `>`, `>=`, `|`, `&&`, and `!`.

All design instances of the subcircuit, specified using `subckt` are checked.

The results are written to the `static.xml` file, which can be viewed in a Web browser.

## Arguments

|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>cond</code>        | Conditional expression to be fulfilled. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>vnth</code>        | NMOS threshold voltage. This value is used to calculate the voltage drop across an NMOS channel during voltage propagation (default value is $0.5 \text{ v}$ ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>vpth</code>        | PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation (default value is $-0.4 \text{ v}$ ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>pwl_time</code>    | If specified, all pwl sources are considered constant sources with a value equal to the voltage of the pwl source at <code>pwl_time</code> . Default is infinity.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <code>vsrnodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a <code>vsrnodefile</code> file with the <code>rpt_node</code> feature, then you can reuse these vsource node voltages.</p> <p>The subcircuit name and the related <code>NV_FILE</code> need to be specified in pairs. The node voltages from the <code>NV_FILE</code> are applied to the nodes inside the given subcircuit. If the first <code>NV_FILE</code> is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrnodefile=["NV_FILE0"]</code>.</p> <p>Default is <code>"[...]"</code>.</p> |
| <code>error_limit</code> | Maximum number of errors reported. Default is 10000.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <code>subckt</code>      | Instances of the specified subcircuit to which the check is applied. Wildcard is not supported. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

## Example

```
sp1 static_subcktport subckt="decand3_pre" cond="v(Z)>1.7"
```

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The above command will report all instances satisfying the condition  $v(Z) > 1.7$ . The following is an example of the report that is displayed in the Web browser:

### static\_subcktpport: sp1

- sp1 static\_subcktpport subckt="decand3\_pre" cond=" $v(Z) > 1.7$ "
- Violation Count: 16

#### Static Subckt Port Check - Violation

| Title               | Inst Name      | Key Sub-expressions | Operands Value    |
|---------------------|----------------|---------------------|-------------------|
| <a href="#">sp1</a> | XTOP.XPRE1.XI2 | $(v(Z) > 1.7)$      | $v(Z) = (0, 1.8)$ |
| <a href="#">sp1</a> | XTOP.XPRE1.XI7 | $(v(Z) > 1.7)$      | $v(Z) = (0, 1.8)$ |

## Static Stack Count

### ***Syntax***

```
title static_stack model=<expression> count=<value> <inst=[inst1 inst2...]>
 <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1
 xsubckt2....]> <depth=n> error_limit=<value>
```

### ***Description***

This check counts PMOS and NMOS transistor stacks and then reports stacks larger than specified count.

The results are written to the `static.xml` file, which can be viewed in a Web browser.

### ***Arguments***

Design check parameters

|                    |                                          |
|--------------------|------------------------------------------|
| <code>model</code> | MOSFET device model names to be checked. |
|--------------------|------------------------------------------|

Filtering parameters

|                    |                                                  |
|--------------------|--------------------------------------------------|
| <code>count</code> | Maximum number of permitted count. Default is 3. |
|--------------------|--------------------------------------------------|

|                          |                                                      |
|--------------------------|------------------------------------------------------|
| <code>error_limit</code> | Maximum number of errors reported. Default is 10000. |
|--------------------------|------------------------------------------------------|

Wildcard scoping

|                   |                                                                                                             |
|-------------------|-------------------------------------------------------------------------------------------------------------|
| <code>inst</code> | Subcircuit instances to which the check is applied. Default includes all instances ( <code>inst=*</code> ). |
|-------------------|-------------------------------------------------------------------------------------------------------------|

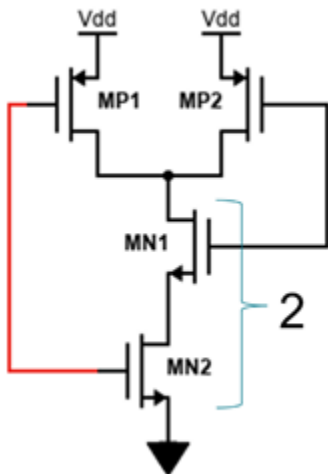
|                    |                                                                      |
|--------------------|----------------------------------------------------------------------|
| <code>xinst</code> | Subcircuit instances to be excluded from the check. Default is none. |
|--------------------|----------------------------------------------------------------------|

|                     |                                                                                                                                      |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <code>subckt</code> | The instances of the specified subcircuit to which the check is applied. Default includes all subcircuits ( <code>subckt=*</code> ). |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------|

|                      |                                                                                                  |
|----------------------|--------------------------------------------------------------------------------------------------|
| <code>xsubckt</code> | The instances of the specified subcircuits that are excluded from the check. Default is none.    |
| <code>depth</code>   | Hierarchy levels (starting from top, instance, or subcircuit scope) to be checked. Default is 8. |

### Example

Consider the following example design:



For this design, the following command checks stacks consisted of nch and reports if the stack count is more than 1:

```
chk2 static_stackcount=1 model=[nch]
```

The report is displayed in the Web browser, as shown below.

- `chk2 static_stack count=1 model=["nch"]`
- Violation Count: 1

Static Stack Check - Violation

| Title                | Count |
|----------------------|-------|
| <a href="#">chk2</a> | 2     |

Stack datas: size=2

| Instance Name |
|---------------|
| MN1           |
| MN2           |

Static Coupling Impact Check

Syntax

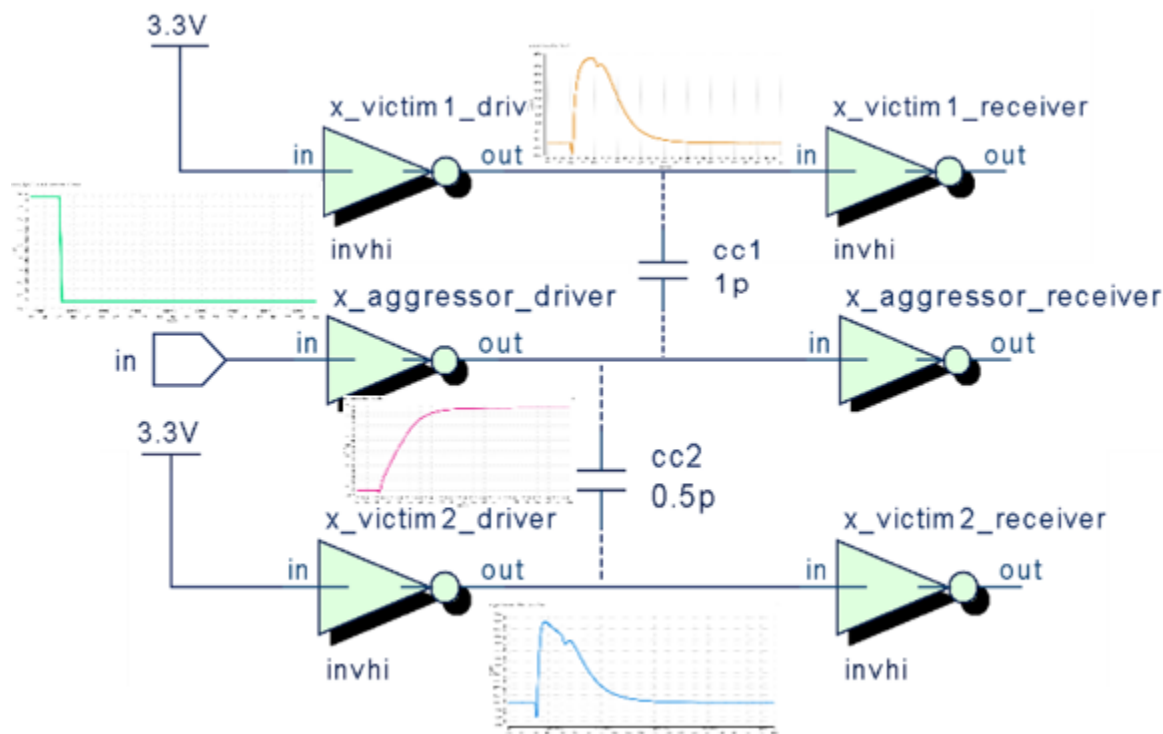
```
title static_coupling node=[n1 n2 ...] vnth=<value> vpth=<value>
 <inst=[inst1inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1
 subckt2...]> <xsubckt=[xsubckt1 xsubckt2...]> pwl_time=<value>
 <vsrctnodefile=[[subckt]...] depth=n> error_limit=<value>
```

Description

Evaluates the possible coupling effects in the circuit.

For each victim node, the check identifies its coupling impact from aggressor(s) by dividing the total charge of the aggressor with its node capacitance (including cc+gc+device cap). The charge of each aggressor is calculated by multiplying the voltage level of the coupling

aggressors (using Vmax for worst case analysis) with the coupling capacitance. In this check, only the capacitors written in netlist are counted.



The results are written to a file with the extension `static.xml`, which can be viewed with a Web browser.

## Arguments

|                          |                                                                                                                                               |
|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>        | Nodes to which the check is applied. Default is none.                                                                                         |
| <code>error_limit</code> | Maximum number of errors reported. Default is 100.                                                                                            |
| <code>vpth</code>        | PMOS threshold voltage. This value is used to calculate the voltage drop across a PMOS channel during voltage propagation. Default is -0.4 V. |
| <code>vnth</code>        | NMOS threshold voltage. This value is used to calculate the voltage drop across an NMOS channel during voltage propagation. Default is 0.5 V. |
| <code>pwl_time</code>    | Time for pwl source to be considered as constant vsource.                                                                                     |



## Spectre Classic Simulator, Spectre APS, Spectre X, Spectre XPS, Spectre FMC Analysis, and Legato Reliability Solution User Guide

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|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>        | Nodes to which the check is applied. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <code>vsrnodefile</code> | <p>Specifies the file from which node voltage are to be read to perform the check. If the node voltages for a given block are already available from a previous simulation and saved in a vsrnodefile file with the <code>rpt_node</code> feature, then you can reuse these vsource node voltages.</p> <p>The subcircuit name and the related NV_FILE need to be specified in pairs. The node voltages from the NV_FILE are applied to the nodes inside the given subcircuit. If the first NV_FILE is given without a subcircuit name, then it is applied to the top level. For example, <code>vsrnodefile=["NV_FILE0"]</code>.</p> <p>Default is " [ . . . ] ".</p> |
| <code>inst</code>        | Subcircuit instances to which the check is applied. Default includes all instances ( <code>inst=*</code> ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <code>xinst</code>       | Subcircuit instances to be excluded from the check. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>subckt</code>      | The instances of the specified subcircuit to which the check is applied. Default includes all subcircuits ( <code>subckt=*</code> ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>xsubckt</code>     | The instances of the specified subcircuits that are excluded from the check. Default is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <code>depth</code>       | Hierarchy levels (starting from top, instance, or subcircuit scope) to be checked. Default is 8.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

### Example

```
coup static_coupling node=[*]
```

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The above statement reports all victims that are impacted by aggressors. The following is an example of the report that is displayed in the Web browser:

### Static Coupling Impact Check - Violation

| Title                | Node Name | Node Cap(F)  | Node Min Voltage(V) | Node Max Voltage(V) | Coupling Impact |
|----------------------|-----------|--------------|---------------------|---------------------|-----------------|
| <a href="#">coup</a> | victim1   | 1.979802e-13 | 0.000000e+00        | 0.000000e+00        | 1.666834e+01    |

### Coupling\_node datas: size=1

| Coupling Node Name | Coupling Node Min Voltage(V) | Coupling Node Max Voltage(V) | Coupling Instance | Coupling Instance Cap(F) |
|--------------------|------------------------------|------------------------------|-------------------|--------------------------|
| aggressor          | 0.000000e+00                 | 3.300000e+00                 | cc1               | 1.000000e-12             |

This report has the following two sections:

- The first section displays the node name of the victim. Next, the node capacitance (with respect to ground) of the victim is shown. The min/max voltage columns display the possible voltage range for this node. The coupling impact is a gauge used to measure the coupling impact of aggressor(s) on the victim. The coupling impact is a relative term and does not have any physical meaning.
- The second section displays the list of aggressors. The min/max voltage columns display the possible voltage range for this node. The coupling instance name (and its capacitance) is the capacitor connected between the aggressor and the victim. This section can have multiple rows for multiple aggressors.

## Static PMOS to GND Count Check

### Syntax

```
title static_pmos2gnd node=[n1 n2 ...] count=<value> <inst=[inst1 inst2...]>
 <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1
 xsubckt2....]> <depth=n> error_limit=<value>
```

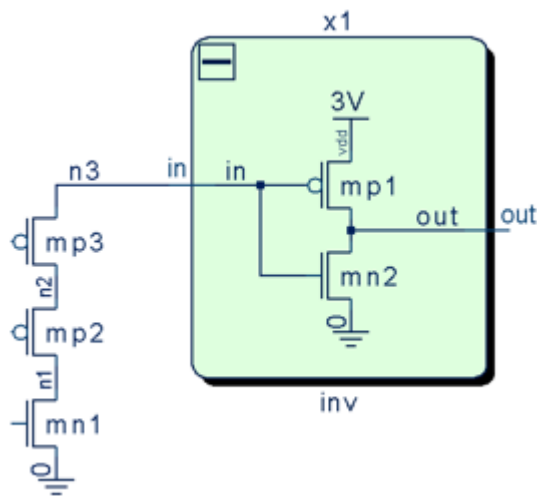
### Description

Counts unpaired PMOS in the discharging path from a fanout node to GND and reports paths having PMOS count greater than the specified count.

The check only analyzes the fanout nodes. It does not check the nodes connecting only to MOSDIODEs or MOSCAPs.

The check counts PMOS from a fanout node to gnd. It does not include PMOS in the count under the following conditions but does report them.

- it is connected to gnd
- it is connected parallel to NMOS as in a transmission gate



The results are written to the `static.xml` file, which can be viewed in a Web browser.

### Arguments

|                      |                                                                                                                                      |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>    | Nodes to which the check is applied. Default is none.                                                                                |
| <code>count</code>   | Maximum number of permitted NMOS. Default is 3.                                                                                      |
| <code>inst</code>    | Subcircuit instances to which the check is applied. Default includes all instances ( <code>inst=*</code> ).                          |
| <code>xinst</code>   | Subcircuit instances to be excluded from the check. Default is none.                                                                 |
| <code>subckt</code>  | The instances of the specified subcircuit to which the check is applied. Default includes all subcircuits ( <code>subckt=*</code> ). |
| <code>xsubckt</code> | The instances of the specified subcircuits that are excluded from the check. Default is none.                                        |

|             |                                                                                                  |
|-------------|--------------------------------------------------------------------------------------------------|
| depth       | Hierarchy levels (starting from top, instance, or subcircuit scope) to be checked. Default is 8. |
| error_limit | Maximum number of errors reported. Default is 10000.                                             |

Example

```
chk1 static_pmos2gnd node=[*] count=0
```

The above statement reports all paths from all fanout nodes having PMOS count greater than 0. The following is an example of the report that is displayed in the Web browser:

- `chk1 static_pmos2gnd node=["*"] count=0`
- Violation Count: 1

Static PMOS to gnd Count

| Title                | Node Name | Count |
|----------------------|-----------|-------|
| <a href="#">chk1</a> | n3        | 2     |

Drivers datas: size=3

| Driver |
|--------|
| mp3    |
| mp2    |
| mn1    |

It reports one path from fanout n3 to gnd. The number of PMOS found in this path is two. Note that mn1 is an NMOS therefore does not contribute in the count.

Static NMOS to VDD Count Check

Syntax

```
title static_nmos2vdd node=[n1 n2 ...] count=<value> <inst=[inst1 inst2...]>
 <xinst=[xinst1 xinst2...]> <subckt=[subckt1 subckt2....]> <xsubckt=[xsubckt1
 xsubckt2....]> <depth=n> error_limit=<value>
```

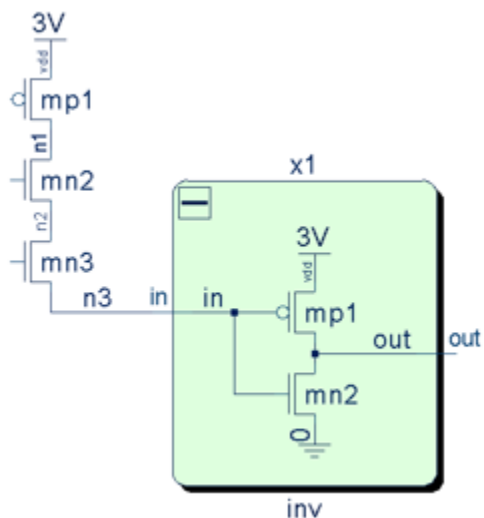
### Description

Counts unpaired NMOS in the charging path from a fanout node to VDD and reports paths having NMOS count greater than the specified count

The check only analyzes the fanout nodes. It does not check the nodes connecting only to MOSDIODEs or MOSCAPs.

The check counts NMOS from a fanout node to VDD. It does not include NMOS in the count under the following conditions but does report them.

- it is connected to vdd
- it is connected parallel to PMOS as in a transmission gate



The results are written to the `static.xml` file, which can be viewed in a Web browser.

## Arguments

|       |                                                                                                             |
|-------|-------------------------------------------------------------------------------------------------------------|
| node  | Nodes to which the check is applied. Default is none.                                                       |
| count | Maximum number of permitted NMOS. Default is 3.                                                             |
| inst  | Subcircuit instances to which the check is applied. Default includes all instances ( <code>inst=*</code> ). |
| xinst | Subcircuit instances to be excluded from the check. Default is none.                                        |

|             |                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------|
| subckt      | The instances of the specified subcircuit to which the check is applied. Default includes all subcircuits (subckt=*) |
| xsubckt     | The instances of the specified subcircuits that are excluded from the check. Default is none.                        |
| depth       | Hierarchy levels (starting from top, instance, or subcircuit scope) to be checked. Default is 8.                     |
| error_limit | Maximum number of errors reported. Default is 10000.                                                                 |

Example

```
chk1 static_nmos2vdd node=[*] count=1
```

The above statement reports all paths from all fanout nodes having NMOS count greater than 1. The following is an example of the report that is displayed in the Web browser:

- chk1 static\_nmos2vdd node=["\*"] count=1
- Violation Count: 1

Static NMOS to vdd Count

| Title                | Node Name | Count |
|----------------------|-----------|-------|
| <a href="#">chk1</a> | n3        | 2     |

Drivers datas: size=3

| Driver |
|--------|
| mn3    |
| mn2    |
| mp1    |

It reports one path from fanout n3 to vdd. The number of NMOS found in this path is two. Note that mp1 is a PMOS therefore does not contribute in the count.

## Static Highfanout Check

### Syntax

```
title static_highfanout node=[n1 n2 ...] upth=<value> downth=<value> rcut=<value>
 <inst=[inst1 inst2...]> <xinst=[xinst1 xinst2...]> <subckt=[subckt1
 subckt2....]> <xsubckt=[xsubckt1 xsubckt2....]> <depth=n> error_limit=<value>
```

### Description

The `static_highfanout` check detects MOSFETs that have a gate connected to a high fanout node. The check reports nodes that have a count greater than the specified count.

The results are written to the `static.xml` file, which can be viewed in a Web browser.

### Arguments

|                          |                                                                                                                                                                                |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>node</code>        | Nodes to which the check is applied. Default is none.                                                                                                                          |
| <code>upth</code>        | Defines the ratio of the width of PMOS (pull-up) and the loading of MOSFETs (with gate connection). The load of transmission gate is also considered. The default value is 10. |
| <code>downth</code>      | Defines the ratio of the width of NMOS (pull-down) and the loading of MOSFETs. The default value is 20.                                                                        |
| <code>rcut</code>        | Cuts the resistor having value greater than <code>rcut</code> . The default value is 1e6.                                                                                      |
| <code>error_limit</code> | Maximum number of errors reported. Default is 10000.                                                                                                                           |
| <code>inst</code>        | Subcircuit instances to which the check is applied. Default includes all instances ( <code>inst=*</code> ).                                                                    |
| <code>xinst</code>       | Subcircuit instances to be excluded from the check. Default is none.                                                                                                           |
| <code>subckt</code>      | The instances of the specified subcircuit to which the check is applied. Default includes all subcircuits ( <code>subckt=*</code> ).                                           |
| <code>xsubckt</code>     | The instances of the specified subcircuits that are excluded from the check. Default is none.                                                                                  |
| <code>depth</code>       | Hierarchy levels (starting from top, instance, or subcircuit scope) to be checked. Default is 8.                                                                               |

## Example

```
chk1 static_highfanout node=["*"] upth=10 downth=20
```

The above statement reports pMOSFETs whose loading-width to driving-width ratio is more than 10. In addition nMOSFETs whose loading-width to driving-width ratio is more than 20 are reported. The report includes the violation type, displaying if it is a pull-up violation, pull-down violation, or both.

The following is an example of the report that is displayed in the Web browser:

### Static Highfanout Check Violations

#### static\_highfanout: chk1

- chk1 static\_highfanout node=["\*"] upth=10 downth=20
- Violation Count: 3

#### Static Highfanout Node Check - Violation

| Title                | Node Name | UpDrivesWidth | DownDrivesWidth | LoadsWidth   | UpThreshold | DownThreshold | ViolationType |
|----------------------|-----------|---------------|-----------------|--------------|-------------|---------------|---------------|
| <a href="#">chk1</a> | x2.out    | 4.800000e-05  | 4.800000e-05    | 1.800000e-03 | 10          | 20            | up and down   |
| <a href="#">chk1</a> | x3.inn1   | 3.000000e-06  | 0.000000e+00    | 9.000000e-05 | 10          | 20            | up            |
| <a href="#">chk1</a> | x3.inn2   | 0.000000e+00  | 3.000000e-06    | 9.000000e-05 | 10          | 20            | down          |

## Workshop

A workshop or rapid adoption kit (RAK) is available that demonstrates the static and dynamic checks in Spectre. This RAK/workshop can be accessed from the following locations:

- Cadence support website <http://support.cadence.com>

Go to *Support Home > Resources > Rapid Adoption Kits > Virtuoso Custom IC and Sign-off Flow > Static and Dynamic Checks*

- SPECTRE installation

Go to `<SPECTRE_install_dir>/tools.lnx86/spectre/examples/SpectreCircuitChecks`



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## Postlayout Simulation

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This chapter consists of the following topics:

- Performance Improvement
- EMIR Analysis
- Parasitic Backannotation of DSPF/SPEF/DPF Files

## Performance Improvement

For postlayout designs with RC parasitics, the `+postlayout` option enables various performance technologies to speed up the simulation, including RC reduction, efficient coupling capacitor handling, DC algorithms optimized for large post-layout circuits, along with other advanced numerical techniques.

To turn on postlayout simulation technologies, use the following command-line options:

```
% spectre +aps +postlayout ...
% spectre +aps +postlayout=hpa ...
% spectre +aps +postlayout=upa ...
```

The `+postlayout` option delivers best simulation performance, with acceptable accuracy, for custom digital designs, memory designs, and analog/mixed-signal designs where high simulation precision is not required. `+postlayout=hpa` provides higher simulation precision for analog/mixed-signal designs. `+postlayout=upa` delivers the ultimate post-layout simulation accuracy, similar to `+postlayout=hpa`, but with RC reduction completely disabled.

Even though not recommended, you can use the `+rcnet_fmax=N` command-line option to adjust simulation accuracy associated with `+postlayout`. The unit for `N` is in GHz and the default value is 125. `N=25` is considered aggressive, whereas `N=250` is considered conservative. The `+rcnet_fmax` option not only controls RC reduction accuracy with any local RC net, but also defines the accuracy/performance trade-off of other non-reduction based techniques.

The `+postlayout` command-line option enables RC reduction because of which some parasitic RC nodes are reduced. Therefore, if you have specified `save` statements in the netlist to save all internal RC nodes, some of these nodes are not saved. To save these nodes, set the value of the `savefilter` option to `none` in the netlist, as shown below.

```
opt options savefilter=none
```

You can use the `preserve_inst` option to preserve instances from any component reduction and parasitic reduction, as shown in example below:

```
simulationOptions options preserve_inst=[inst1, inst2, ...]
```

`inst1` and `inst2` can be the instances of any device or subcircuit; they will not be reduced by APS, or the parasitic reduction technology.

**Note:** The `+parasitics` option is now obsolete and should not be used. You can use the `+postlayout=legacy` option to get the same behavior as `+parasitics`. In addition, you can use the `+postlayout=legacy_rf` option for RF designs, which provides the same functionality as the `+parasitics=rf` option. The `+postlayout=legacy` and `+postlayout=legacy_rf` options will be removed in a future release.

**Note:** The `+postlayout` command-line option is available only in Spectre® APS.

## **EMIR Analysis**

With Spectre® APS, and Spectre® X, Cadence delivers a powerful transistor-level EMIR solution. This dynamic power net and signal net EMIR capability uses a patented technology and is designed to provide high capacity and high performance EMIR analyses. Within the same flow, Spectre APS and Spectre X can be used for high accuracy EMIR analyses; while Spectre X provides higher capacity and performance. The Spectre EMIR solution provides a set of advanced features covering dynamic EMIR, static EMIR, point-to-point resistance analysis, power gate support, differential IR drop, design resistor EM calculation, macro model generation, black boxing, and what-if analysis. The flow is fully integrated into Cadence Virtuoso® ADE environment. Results of the analysis can be visualized with Voltus-Fi XL).

This section discusses the following:

- [Spectre EMIR Technology, Product, and Flow Overview](#) on page 808
- [Getting Started with Spectre EMIR Analysis](#) on page 813
- [Establishing an Accuracy Reference and Correlating EMIR Accuracy](#) on page 852
- [Optimizing EMIR Analysis for Accuracy and Performance](#) on page 857
- [Power Gate Support](#) on page 864
- [Handling the Complexity of DSPF/SPEF files](#) on page 865
- [Advanced Analyses](#) on page 871
- [Advanced EMIR Features](#) on page 880
- [Event Triggered EMIR Analysis](#) on page 888
- [Other Features](#) on page 888

## **Spectre EMIR Technology, Product, and Flow Overview**

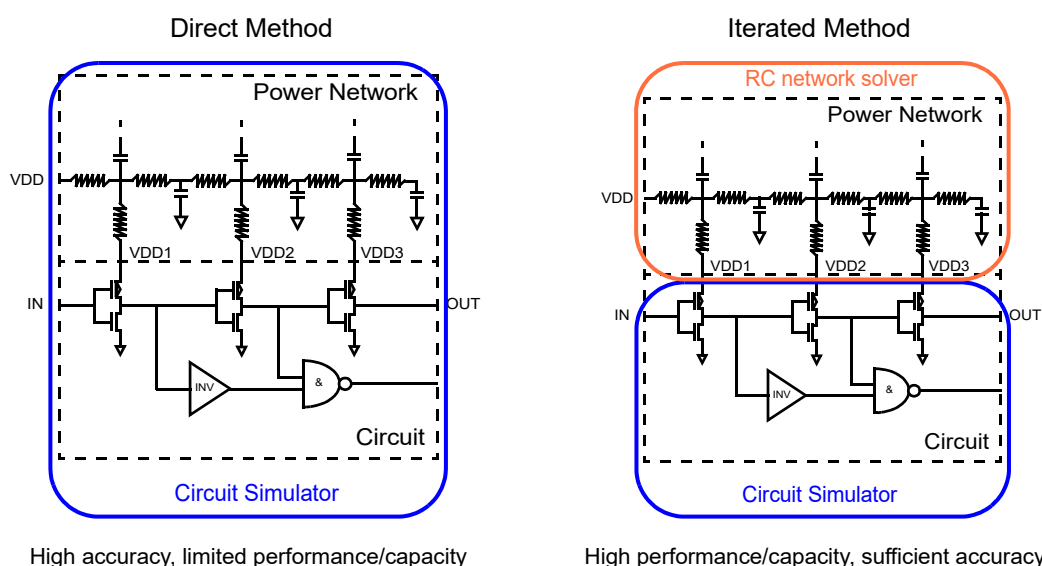
### **Technology Overview**

In an EMIR flow, a circuit is evaluated together with the parasitic resistor and capacitor network, which models the IR drop or the EM effect. There are two general approaches of solving such a problem:

- **Direct EMIR analysis** - When high accuracy is needed, a brute-force simulation of the entire system (circuit plus parasitic resistances and capacitances) can be performed to

accurately calculate the EMIR of any net. The EMIR simulation performance and capacity is subject to the limitation of the circuit simulator being used.

- **Iterated EMIR analysis** - In order to conduct EMIR simulation on circuits with much larger power and signal nets within a much shorter time, an alternative is to decouple the nonlinear circuit simulation from the linear RC net analysis. User can iterate the linear RC net analysis by modifying the layout, however, the nonlinear circuit simulation is performed only once. The decoupling of the linear RC nets from the nonlinear circuit is not mathematically equivalent to the original design and certain inaccuracy is introduced, however, the user receives the benefit of simulation performance and capacity.



For high accuracy EMIR analysis of small design blocks, or designs with smaller numbers of RC nets, the Spectre® APS and Spectre X based direct EMIR analysis is recommended.

To gain higher performance and higher capacity on medium-to-large designs, the iterated EMIR analysis method is recommended. Both Spectre APS and Spectre X support iterated EMIR analysis.

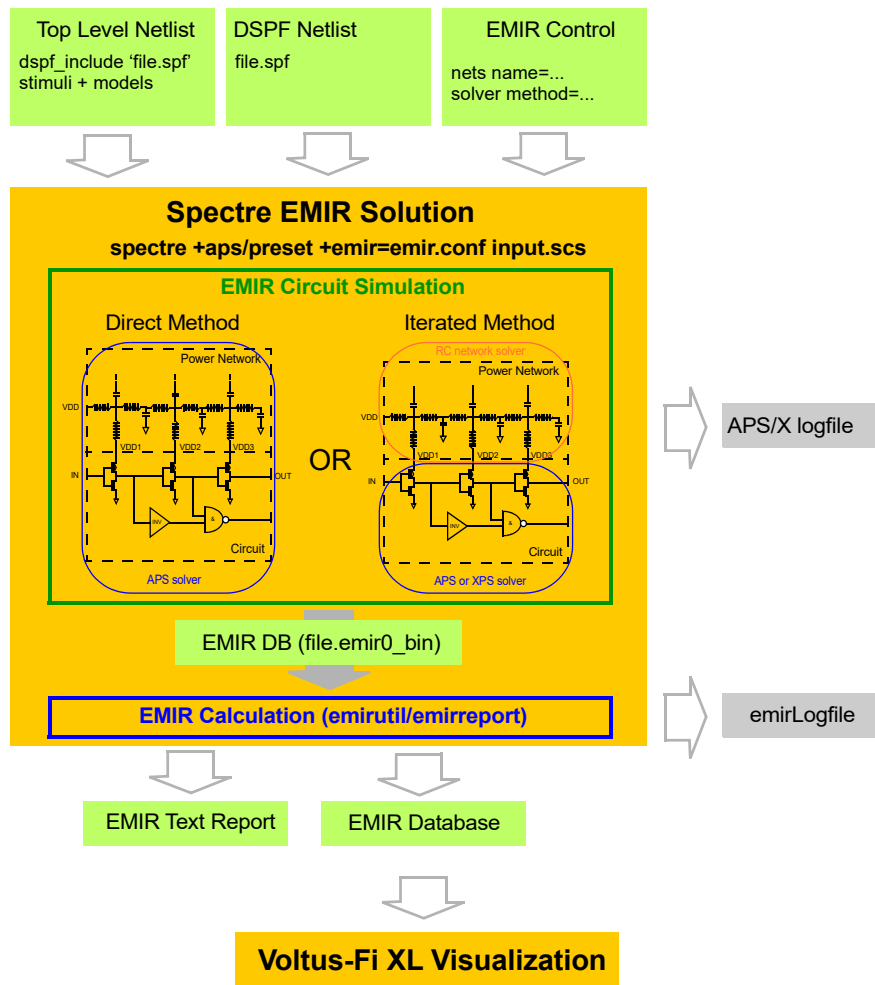
The Spectre EMIR flow requires a complete testbench that contains the DSPF files (with the parasitic and instance sections describing the circuit to be analyzed) stimuli, device models, and so on. The EMIR analysis can be applied to a transient or DC analysis.

The presence of a +emir option on the Spectre command line enables the EMIR analysis during circuit simulation. The details of EMIR analysis - type of analyses, nets to be analyzed, output to be created - are specified using an EMIR configuration file.

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Using either direct EMIR analysis or iterated EMIR analysis, the circuit simulation is performed first with various voltages and currents being calculated. Next, a standalone tool, `emirrreport/emirutil`, is called to post-process the simulation results and generate the IR and EM reports. By default, the post-processing step is invoked automatically.

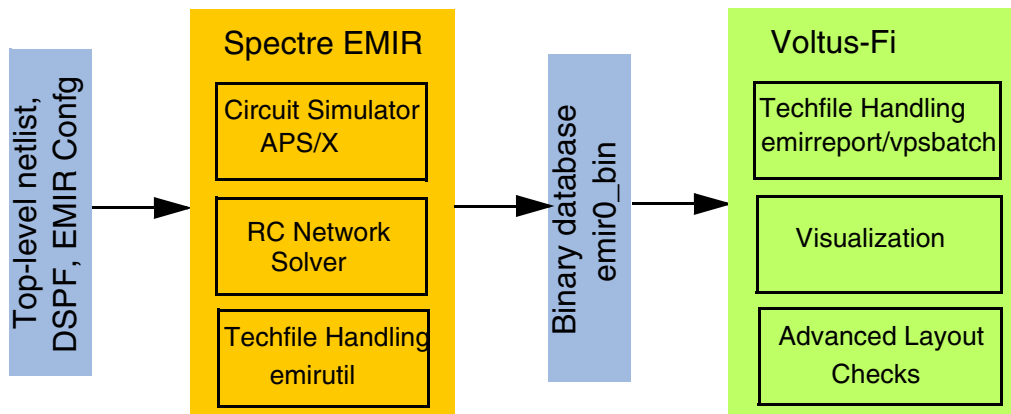
The output of the EMIR analysis is an EMIR text/html report, which lists the EM and/or IR information of all the nets requested. In addition, *Voltus-Fi XL* can be used to visualize the IR drop and EM current violations in Virtuoso Layout Editor.



Note that while the Spectre EMIR flow uses the DSPF representation of the designs, it is not relying on any post-layout back-annotation or "stitching" capability. The flow covers designs with power gates and package models.

## Product Overview and EMIR Flow

The EMIR product consists of the Spectre EMIR simulation and the *Voltus-Fi XL* visualization. The circuit and the RC network simulation are handled by Spectre EMIR. The result is stored in a binary database which contains the average, rms, max IR drop, and EM values. *Voltus-Fi XL* reads the information from the binary database, evaluates whether the currents are above the limits defined in the technology file, and visualizes the results in the layout.



Different utilities are responsible for creating the IR drop and EM text reports. For advanced node designs for which the technology file format is ICT or `qrctechfile`, the utility `emirreport` (or `vpsbatch`) is used to generate the text report. For older technology nodes which use `emdatafile` format, the utility `emirutil` is used to create the text reports.

## DSPF requirements

The Spectre EMIR flow is based on a DSPF representation of the analyzed design. The DSPF file is required to contain all electrical and geometric information needed for EMIR

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analysis. The following figure shows a representative DSPF netlist with all important information for EMIR being marked in color.

```
*|DSPF 1.5
*|DATE "Tue Sep 18 15:44:21 2012"
*|VENDOR "Cadence Design Systems"
*|PROGRAM "Cadence Extraction QRC"
*|VERSION "10.1 Linux 32 bit- (Thu Apr 14 12:02:04 PDT 2011)"
*|DESIGN "adc_sample_hold"
*|DIVIDER /
*|DELIMITER #
*|DeviceFingerDelim "@"
*|BUSBIT []
.GLOBAL
*
.SUBCKT adc_sample_hold outm outp SIDDQ VDD VSS bias100 hold hold_test inm
*
*Net Section
*|GROUND_NET VSS
*
*|NET VDD 8.09439e-14
*|P(VDD I 0 1.4100 103.0500)
*|I(MPM6#s MPM6 s X 0 34.1500 88.8500)
*|S(net0154#49 51.2355 82.8175)
*|S(net0154#50 51.2355 78.5785)

Rg3135 net0154#49 net0154#50 0.978231 $mt3 $L=4.239 $W=0.26 $X=51.235 $Y=80.6985

Rs3247 net0154#150 net0154#162 0.077778 $Viat $A=0.3528 $X=59.315 $Y=50.34
C5551 net58#104 VSS#155 5.63854e-17 $X=22.285 $Y=64.9885
...
*
*Instance Section
*
MNMO MNMO#d MNMO#g MNMO#s VSS gpd090_nmos2v L=0.28U W=3U AD=0.9P AS=0.54P PD=6.6U PS=3.36U
```

Important EMIR related information

- Subckt definition
- Layer name
- L/W of wire OR Area of via
- Coordinates (X,Y) of resistor origin
- MOSFET Instances

## EM Rule Support

EM rules are defined in DRM, and part of the technology files. The *Voltus-Fi XL*– Spectre EMIR solution supports the following technology file formats.

- ICT, ICT-EM (EM rules only)
- qrctechfile
- emdatafile

Advanced node technologies require special EM rules that are only supported in ICT/ICT-EM and qrctechfile format. Refer to the *Quantus QRC Techgen Reference Manual* for details.

emdatafile format is used for legacy technology nodes. In future, it is expected to be replaced by ICT and qrctechfile format.



Various Cadence EMIR tools support only subsets of these techfile formats (for example, Voltus does not support ICT file, but supports `ICT_em`). `ICT_em` is the only format supported by all Cadence EMIR technologies, Voltus, EAD, and Voltus-Fi L and XL.

## Getting Started with Spectre EMIR Analysis

To perform EMIR analysis, first create a complete simulation testbench with the DSPF files containing the postlayout data of the design. Specify the fingered devices in the `instance` section and the parasitic resistors and capacitors in the `net` section. Use the `dspf_include` statement to read the DSPF content, as shown below.

```
dspf_include "sram.spf" (Spectre syntax)
```

```
.dspf_include "sram.spf" (SPICE syntax)
```

`dspf_include` provides special features like port order adjustments, or handling of duplicated subcircuits, which are not available in `include/.include`. Therefore, do not use `include/.include` in the EMIR flow for including the DSPF file.

Large DSPF files may be split into multiple files, for example, `sram.dspf`, `sram.dspf.1`, `sram.dspf.2`, and so on. If the top-level DSPF file (`sram.dspf`) is included with the `dspf_include` statement, Spectre will search for any related file (`sram.dspf.1`, `sram.dspf.2`, ...) and read them automatically.

EMIR analysis can be applied to several subcircuits within the same design. Each block needs to be described with a DSPF file, and each DSPF file needs to be included with the `dspf_include` statement.

Setting up a correct postlayout simulation test bench is vital to successful EMIR analysis (see [Handling the Complexity of DSPF/SPEF files](#)).

Once the testbench is set up, you can perform a regular (non-EMIR) postlayout simulation with the `spectre` command to ensure that the testbench contains no error, and the circuit behavior is as expected.

```
% spectre ++aps=liberal input.scs //Spectre test bench
```

The Spectre command-line options can be used to adjust accuracy and performance. The command above initiates the simulation session with the `++aps` engine and `liberal` errpreset setting.

To perform the same simulation with EMIR analysis added, you need to create and include an EMIR control file with the `spectre` command, as shown below.

```
% spectre ++aps=liberal +emir=emir.conf input.scs //Spectre test bench
```

The EMIR analyses is enabled by using the `+emir` Spectre command-line option. All EMIR-related commands are defined in the EMIR control file.

### EMIR Control File

EMIR analysis is performed based on the first transient analysis statement in the netlist. An EMIR control file contains all of the settings and options that are relevant to an EMIR analysis. Some of the options that can be specified using the EMIR control file are: the names of the nets to be analyzed, the type of analyses to be performed, the EMIR analysis time window, choice of direct or iterated methods, settings for RC simulation, location of EM rule file, and so on.

The following sample control file describes EMIR analysis based on the `x1` instance. A maximum IR drop analysis is performed on nets `VDD` and `VSS`, while RMS-based EM analysis is performed on all nets inside the `x1` instance. The two-stage iterated method is used, and the current density limits for the EM report are referenced from file `./em_dir/40n_emfile.txt`. Only one subcircuit instance is allowed for EMIR analysis for a Spectre run.

### Example EMIR control file (emir.config)

```
net name=[X1.VDD X1.VSS] analysis=[vmax iavg]
net name=[X1.*] analysis=[irms]
solver method=iterated
emirutil techfile="./em_dir/40n_emfile.txt"
```

The EMIR control file supports the Spectre line continuation character `+` and comment-line characters `*` and `//`.

The following table summarizes the EMIR control file options:

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The following table summarizes the supported EMIR control file options:

| Keyword    | Option Set                                                                                       | Explanation                                                                                                                                                                                                                                                                                                                                                                                          | Default Value |
|------------|--------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| <b>net</b> | name=[instance1.net1<br>instance1.net2....]<br><br>or<br><br>name=[net1 net2...]<br>inst=[inst1] | Defines the nets for which the analysis is performed.<br><i>instance</i> defines the instance of the subcircuit containing the net. <i>net</i> defines the net name inside the subcircuit instance as it is defined in the DSPF *   NET definition. If the DSPF file is included at the top level, the instance name is not required. Wildcarding is supported for net names but not instance names. | none          |
|            | analysis=[imax iavg<br>iavgpos iavgneg iavgabs<br>irms vmax vavg]                                | peakEM, avgEM, avgEM for i>0, avgEM for i<0, avgabseM, rmseM, peakIR, avgIR. imax, iavg, iavgabs, irms, and vmax data are always written to the binary database independent of user settings.<br><br><b>Note:</b> If <i>Voltus-Fi</i> acpeak analysis is required, then imax and irms analyses need to be enabled in Spectre EMIR.<br><br>imax means<br>max(abs(current waveform))                   | iavg, vmax    |

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|  |                                                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |
|--|----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|  | <code>dut_inst=name</code>                                                                                                 | This option defines the instance name of the DSPF subcircuit (for example, <code>i0</code> ). It is required only if a name mapping is required between ADE net names (for example, <code>i0.i1.i2.net5</code> ) and DSPF names ( <code>i0.x1/xi2/net5</code> ). By default, ADE name is modified by adding a leading <code>x</code> and replacing <code>.</code> with <code>/</code> . The DSPF subcircuit instance name and the leaf-level net name are not impacted. You can use the option <code>spf</code><br><code>netxtorprefix=dspf_hier_inst_prefix</code><br><code>schematic_hier_inst_prefix</code> to customize the mapping. | none |
|  | <code>pwrgate=[I1.VDD I1.VDD_INT...]global=[I1.VDD]</code><br><br>or<br><br><code>inst=[I1] pwrgate=[VDD VDD_NT...]</code> | Enables power gate handling. You need to specify the power supply net driving the power gate ( <code>vsource</code> connected) and the internal power supply net driven by the powergate. If one power supply net drives multiple power gates, you need to specify one statement with all internal power supply nets. If none of the powergate nets is driven by <code>vsource</code> , then the <code>global</code> statement can be used to define the global net.                                                                                                                                                                     | none |
|  | <code>coupled_nets = [VDD VDD1 VDD2 VDD3]</code>                                                                           | Defines nets being coupled by design resistors and solved together. Requires the definition of the design resistor model:<br><code>eisopt</code><br><code>coupled_nets_model=[rmw 1]</code>                                                                                                                                                                                                                                                                                                                                                                                                                                              | none |

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|  |                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |             |
|--|---------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
|  | <p>analysis=[sigvmax<br/>sigvavg] reftype=[avg<br/>max min pin]<br/>[findsrc=yes no] [refnode<br/>=name] [vref=value]</p> | <p>analysis=sigvmax - max<br/>signal net IR drop.</p> <p>analysis=sigvavg - avg<br/>signal net IR drop.</p> <p>reftype=avg - reference<br/>voltage for IR drop is the<br/>average voltage of all subnodes<br/>at every time point. This is the<br/>default.</p> <p>reftype=max - reference<br/>voltage for IR drop is the<br/>maximum voltage of all<br/>subnodes at every time point.</p> <p>reftype=min - reference<br/>voltage for IR drop is the<br/>minimum voltage of all<br/>subnodes at every time point.</p> <p>reftype=pin findsrc=yes<br/>- Reference voltage of IR drop is<br/>taken from vsource, which is<br/>traced back from *P  node.</p> <p>reftype=pin findsrc=no -<br/>Reference voltage of IR drop is<br/>taken from *P  node.</p> <p>refnode - use the reference<br/>voltage from the specified<br/>reference node.</p> <p>vref - use the voltage value as<br/>reference and report the value<br/>as vmax and not as sigvmax in<br/>the report.</p> | <p>none</p> |
|--|---------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|

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|  |                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |      |
|--|----------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|  | analysis=[ipwc]<br>pwc_threshold=1e-6                                                  | Enables pulse-wise constant EM current calculation for violation visualization. The pwc_threshold option defines the current threshold for finding the start of the pulse. Any value below pwc_threshold (the default value is 1e-6) is considered as zero. The emirutil dump_pwc_info=1 2 option generates an ASCII report in the <name>.rpt.pwc file for debugging purpose only. dump_pwc_info =1 creates a compact report (default) while dump_pwc_info=2 creates a detailed PWC report. | none |
|  | net name=[vdd gnd]<br>analysis=iacpeak                                                 | ACPEAK analysis with shifting constant time window. Window size is defined by acpeak_tpeak, and shifting by acpeak_tpeak/acpeak_n. Iacpeak value for worst case window is reported.                                                                                                                                                                                                                                                                                                         | none |
|  | net name=[vdd gnd]<br>analysis=[iacpeak ipwc]<br>pwc_threshold=1e-6                    | Duty cycle analysis with varying time window, time windows defined by current value crossing pwc_threshold. Td and duty cycle for worst case window are reported.                                                                                                                                                                                                                                                                                                                           | none |
|  | net name=[vdd gnd]<br>analysis=[iacpeak ipwc]<br>tau=100p<br>td_current_threshold=1e-6 | Duty cycle analysis with constant time window (tau), time windows defined by current value crossing pwc_threshold. Td and duty cycle for worst case window are reported. Td isn't calculated when lmax<td_current_threshold (def. 1uA).                                                                                                                                                                                                                                                     |      |

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|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <pre> name [instance.net1...] r2r_refnet=VSS analysis=[r2rvmin] [r2rvmin_layer=mt1]r2rvmin_refnet_layer=[m2] r2rvmin_tap_inst=[MN1* MN2*] r2rvmin_refnet_tap_inst=[MN3* MN4*] r2rvmin_model=[pch...] r2rvmin_refnet_model=[nc h...] r2rvmin_bbox=[1.0 1.0 269.5 279.5] r2rvmin_refnet_bbox=[...] ] r2rvmin_node_report=[on  off] r2rvmin_rule_name=name r2rvmin_excl_layer=[m6] r2rvmin_refnet_excl_layer=[m9] r2rvmin_excl_tap_inst=[MN5] r2rvmin_refnet_excl_tap_inst=[MN6] r2rvmin_excl_model=[pch...] r2rvmin_refnet_excl_model=[pch...] r2rvmin_excl_bbox=[32.99 95.92 41.01 99.659] r2rvmin_refnet_excl_bbox=[...] </pre> | <p>Worst case differential (rail-to-rail) IR drop between the specified power supply node and the reference net written to the *.rpt.r2r file. If r2r_refnet is not specified, the ground node is automatically detected. At each time point, the sub node with the highest IR drop is selected for power and ground net and the differential voltage is calculated. The worst case differential IR drop over the EMIR time window is reported and the worst case power and ground waveforms are written to the waveform file. Optional scoping (combined with AND) includes layer names, tap device names, and tap device model names for both power supply node and refnet. A boundary box can be defined for power supply net and refnet.</p> <p>Optionally, a name can be assigned to each r2rvmin option.</p> <p>r2rvmin_node_report enables additional report of nodes and XY coordinates (default is off). Exclude statements supported for layers, tap device instances, models, and bounding boxes. All exclude statements allow you to specify file content. For example, r2rvmin_refnet_excl_tap_inst_file=refexcl.txt.</p> | <p>none</p> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|

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|               |                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |      |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|               | <pre>design_res_models=[name= rhim_m l=... w=... layer=...unit=... term=3] analysis=[iavg irms]  design_res_models=[resis tor] analysis=[iavg irms]</pre> | Specifies EM analyses for design resistors in the form of subcircuit resistor models (name=...) or resistor primitives (resistor). W and L are optional parameters for mapping of subcircuit resistor subcircuit parameters between DSPF and subcircuit model, unit for W/L, and term that defines the terminal at which the current should be evaluated. The default is one terminal.                                                                                                                                                                             | none |
|               | vref=value                                                                                                                                                | Defines the optional voltage reference value for v <sub>max</sub> and v <sub>avg</sub> analyses.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | none |
|               | include=file                                                                                                                                              | Specifies the file name with a list of net names.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | none |
|               | exclude=[netname1<br>netname2...]                                                                                                                         | Excludes the specified nets when name=[*] is used.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | none |
| <b>solver</b> | <pre>method=[auto direct iter ated profoundly iteronly   itereco iterated_split]</pre>                                                                    | <p>auto - direct for Spectre APS and Spectre X</p> <p>direct - forced direct method</p> <p>iterated - forced iterated method</p> <p>profoundly - iterated flow - circuit profile generation</p> <p>iteronly - iterated flow - RC network iteration (requires solver inputwf=iterated.emirta p.pwl)</p> <p>itereco - iterated flow - RC network iteration with What-If changes defined in the ECO file</p> <p>iterated_split - iterated flow - Same as iterated; however, it runs the first and second stages as separate processes to reduce peak memory usage</p> | auto |



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|  |                                                       |                                                                                                                                                                                                                                                                                                                                                                                                       |                   |
|--|-------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
|  | <code>speed= [ 1   2   3   4   5   6   7   8 ]</code> | <p>Defines the speed/accuracy trade-off for PN and SN RC network solver.</p> <p>1 - adaptive time step, highest accuracy, lowest speed</p> <p>5 - adaptive time step, lowest accuracy, highest speed</p> <p>6 - fixed time step with 2000 steps</p> <p>8 - fixed time step with 1000 steps</p>                                                                                                        | 5                 |
|  | <code>rcr=[only selected asis]</code>                 | <p>Defines EMIR RC reduction for the first stage of the iterated method.</p> <p><code>only</code> - use the Only database.</p> <p><code>selected</code> - use the selected RC reduction, if enabled.</p> <p><code>asis</code> - use the parser/solver RC reduction, if enabled.</p> <p>EMIR RC reduction is performed during parsing. Solver RC reduction, if enabled, is performed additionally.</p> | <code>only</code> |
|  | <code>rcr_netsize=value</code>                        | <p>Applies to <code>rcr_selected</code> only. All nets with value equal to or less than the specified resistor value are considered signal nets using conservative RC reduction. The signal net reduction method is defined by <code>rcr_small_net_method</code>. All nets having a value more than the specified resistor value are considered power nets.</p>                                       | 30000             |

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|  |                                                                                |                                                                                                                                                                                                                                                                                                                                                      |                    |
|--|--------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
|  | <code>rcr_huge_netsize=value</code>                                            | Differentiates between the large and huge power nets. The large power net reduction is defined by <code>rcr_big_net_method</code> while the huge power net reduction uses the <code>reff</code> method. By default, there is no huge power net.                                                                                                      | infinite           |
|  | <code>rcr_small_net_method=[conly reff rcr rsnap asis]</code>                  | Specifies the reduction method for signal nets. Possible values are <code>conly</code> , <code>reff</code> , <code>rcr</code> , <code>rsnap</code> , and <code>asis</code> .                                                                                                                                                                         | <code>rcr</code>   |
|  | <code>rcr_big_net_method=[conly reff rcr rcr_pwr rsnap rsnap_reff asis]</code> | Specifies the reduction method for large power nets. Possible values are <code>conly</code> , <code>reff</code> , <code>rcr</code> , <code>rcr_pwr</code> , <code>rsnap</code> , <code>rsnap_reff</code> , and <code>asis</code> .                                                                                                                   | <code>conly</code> |
|  | <code>rcr_net=[name1 name2...]</code>                                          | This option is applicable only when <code>rcr</code> is set to <code>selected</code> . All the specified nets are considered as signal nets. A conservative RC reduction is applied in the first stage. The reduction rate can be adjusted by using the solver option <code>rcr_fmax=value</code> (the default value is 20, and the unit is in GHz). | <code>none</code>  |
|  | <code>c_net=[name1 name2...]</code>                                            | This option is applicable only when <code>rcr</code> is set to <code>selected</code> . All the specified nets use <code>Conly</code> method in the first stage.                                                                                                                                                                                      | <code>none</code>  |

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|  |                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                             |      |
|--|----------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|  | <code>rcr_pwr_net[name1<br/>name2...]</code>                                                                                     | This option is applicable only when <code>rcr</code> is set to <code>selected</code> . All specified power nets use moderate RC reduction. The reduction rate can be adjusted by using the solver option <code>rcr_pwr_fmax=value</code> (the default value is 2, and the unit is in GHz).                                                                                                                                                                  | none |
|  | <code>reff_pwr_net=[name1<br/>name2...]</code>                                                                                   | This option is applicable only when <code>rcr</code> is set to <code>selected</code> . All specified power nets use Reff modeling between pin and tap nodes.                                                                                                                                                                                                                                                                                                | none |
|  | <code>rsnap_reff_pwr_net=[name1<br/>name2...]<br/>kept_layer=[layer1<br/>layer2...]<br/>snap_layer=[layer1<br/>layer2...]</code> | This option is applicable only when <code>rcr</code> is set to <code>selected</code> . All power nets specified use a combined Rsnap/Reff modeling between the pin and tap nodes. You need to define either the layers that need to be modeled with Rsnap/Reff (with <code>snap_layer</code> , all non-specified layers are kept), or the layers that should be kept (with <code>kept_layer</code> , all non-specified layers are modeled with Rsnap/Reff). | none |
|  | <code>asis_net=[name1 name2]</code>                                                                                              | Applies to <code>rcr=selected</code> only. All specified nets use the <code>asis</code> method.                                                                                                                                                                                                                                                                                                                                                             | none |

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|  |                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |      |
|--|------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|  | <code>global_pwr_net=[name1<br/>name2 ...]</code>                                                    | By default, IR drop is enabled only for DSPF subcircuit ports that are driven by a DC vsource. If a subcircuit port is not connected to a DC vsource, it can be defined as a power supply node using the <code>global_pwr_net</code> option and IR drop on this net can be calculated by specifying the <code>analysis=vmax</code> statement on this net. The IR drop reference value used is the maximum value of the voltage waveform at the specified port. This feature is only supported in iterated method. Wildcarding is not allowed. Once enabled, the net can be used in the <code>pwrgate</code> statement. | none |
|  | <code>ldo_net=[VDD_LDO]<br/>ldo_driver=[I1.X1/M1<br/>I1.X1/M2]<br/>ldo_vref=max avg min value</code> | Defines LDO net for LDO IR drop analysis. LDO MOSFET drivers need to be defined in <code>ldo_driver</code> . IR drop reference voltage can be the min, the max, or the average voltage of the <code>ldo_driver</code> nodes over the EMIR time window. Alternatively, the user can define a fixed reference value, <code>ldo_vref=1.1</code> . Instead of <code>ldo_drive</code> , the instance name of the LDO can be specified with <code>ldo_inst=[I1.X1]</code> . Wildcards are supported <code>ldo_drive</code> but not in <code>ldo_inst</code> .                                                                | none |

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|  |                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |       |
|--|--------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
|  | <code>preset=0   1   2</code>              | Specifies whether or not the solver should be optimized.<br><br>0- Does not optimize the solver<br><br>1 - Performs solver optimization for accuracy<br><br>2 - Performs solver optimization for performance                                                                                                                                                                                                                                                                                           | 1     |
|  | <code>tstep=value</code>                   | Change the solver to a fixed timestep specified by <i>value</i> . The unit is in seconds.                                                                                                                                                                                                                                                                                                                                                                                                              | none  |
|  | <code>min_tstep=value</code>               | Minimum time step for adaptive time step. The unit is in seconds.                                                                                                                                                                                                                                                                                                                                                                                                                                      | 1ps   |
|  | <code>maxiters=value</code>                | Defines the maximum iteration number in the transient stage of RC solver. Value 0 can be used for performance optimization.                                                                                                                                                                                                                                                                                                                                                                            | 100   |
|  | <code>rcsolve_multi_proc=[on   off]</code> | If set to <code>on</code> , enables parallel (forked) processes for second stage network solving. You can use the <code>+mt</code> command-line option to specify the maximum number of cores to use. Small-sized nets (< <code>rcsolve_1t_netsize</code> ) are solved first with eight forked single-thread processes. Medium-sized nets are solved next with two forked four-thread processes. Large nets (> <code>rcsolve_4t_netsize</code> ) are solved with one main process using eight threads. | off   |
|  | <code>rcsolve_1t_netsize=value</code>      | Specifies the small net threshold value for parallel (forked) processing of second stage network solving.                                                                                                                                                                                                                                                                                                                                                                                              | 10000 |

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|  |                                             |                                                                                                                                                                                                                                                                                                                          |           |
|--|---------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
|  | <code>rcsolve_4t_netsize=value</code>       | Specifies the large net threshold value for parallel (forked) processing of second stage network solving.                                                                                                                                                                                                                | unlimited |
|  | <code>ignore_tap=[name1 name2...]</code>    | Ignores the specified tap devices in dynamic, static EMIR, and SPGS. The specified tap devices are changed to subnodes and do not carry any current. In addition, they are not reported. It applies to only the second stage of the iterated method and is not supported in the direct method. Wildcarding is supported. | none      |
|  | <code>report_tapc=[off text]</code>         | Report the net and tap device capacitance values for nets being defined in the UTI command. The capacitance report is written to a file with extension <code>rpt_tapc</code> .                                                                                                                                           | off       |
|  | <code>concurrent_ratio=value</code>         | Defines the concurrent tap device handling. The <code>value</code> should be greater than or equal to 0 but less than or equal to 1.<br><br>1 - concurrent<br>0 - not concurrent                                                                                                                                         | 1         |
|  | <code>mosfet_subckt=[name1 name2...]</code> | Defines the subcircuits describing the complex powergate subcircuits. The first four terminals should connect to MOSFET d, g, s, b, and terminals 0 and 2 should connect to the global and virtual power nets.                                                                                                           | none      |
|  | <code>inputwf=file_name</code>              | Specifies the waveform file that contains the results from circuit simulation when <code>method=iteronly</code> is used.                                                                                                                                                                                                 | none      |

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|---------------|----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| <b>static</b> | <code>ifile=<i>filename</i></code>                                                     | Enables static EMIR analysis. The filename defines the subcircuit instance port currents. Static EMIR analysis cannot be combined with dynamic EMIR analysis.                                                                                                                                                    | none |
|               | <code>exclude=[net=[name1 name2] dev=[name1 name2]]</code>                             | Exclude the tap devices from static current distribution. A 0A current is assigned to the specified tap devices. Wildcarding is supported for both <code>exclude</code> and <code>dev</code> . For example:<br><br><code>exclude=[net=[I1.VDD] dev=[MPM3*]]</code> .                                             | none |
|               | <code>net=[name1] dev=[name1 name 2]<br/>current_scale=1.5</code>                      | Allows individual tap device current scaling after the currents were distributed. Dev and current_scale are required parameters. If net isn't defined then option is applied to all nets. Wildcarding is supported for net and dev. Example: <code>static net=[I1.VDD] dev=[MPM3* MNM1] current_scale=1.5</code> | none |
|               | <code>ldo_net=[I1.VDD_LDO]<br/>ldo_driver=[I1.X1/M1 I1.X1/M2] ldo_vref=1.0</code>      | Defines LDO net and LDO drivers for which IR drop is calculated.                                                                                                                                                                                                                                                 | none |
|               | <code>i_value = 1.1e-6<br/>net=[net1 net2] dev = [X1/X2/X5/*] model = [model_3]</code> | Defines individual device current assignment. Current assigned by i_value is considered to be part of total current defined in static_ifile.                                                                                                                                                                     | none |

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|  |                                                                                          |                                                                                                                                                                                                                                                                                |                    |
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|  | <code>i_scale = 1.1 net=[net1<br/>net2] dev = [X1/X2/X5/<br/>*] model = [model_3]</code> | Defines how the current is scaled for the given devices. First scaling is applied to W/L for all devices defined in <code>i_scale</code> . Second current distribution is performed based on W/L values. This approach doesn't change the total pin current being distributed. | <code>none</code>  |
|  | <code>current_scale_file=current_scale_file.txt</code>                                   | Supports tap device current scaling (above) through file definition. Content of current scaling file per line is: <code>net dev scaling_factor</code> , i.e. <code>I1.VDD MPM3* 1.5</code>                                                                                     | <code>false</code> |
|  | <code>report_tapi=[true   false]</code>                                                  | Enables the printing of individual tap device currents in static EMIR analysis. The current values are written to a file with the extension <code>rpt_tapi</code> .                                                                                                            | <code>false</code> |



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|                 |                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |      |
|-----------------|------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| <b>emirutil</b> | <code>techfile="emDataFile"</code> | <p>Specifies the EM rule file in the emdatafile, qrctechfile, or ICT file format.</p> <p>The EM rule file can be predefined in the configuration file using the <code>EMTECHFILE</code> environment variable, as shown below.</p> <pre>setenv EMTECHFILE="<i>&lt;path&gt;/emdatafile</i>"</pre> <p>It can also be defined in the <code>.cdsinit</code> file as follows:</p> <pre>envSetVal("spectre.envO pts" "emTechFile" string <i>&lt;path to the file&gt;</i></pre> <p>Case-insensitive layer names are supported for easier match between the DPSF file and emData file.</p> <p>The rule file defined in the configuration file has higher priority followed by the rule file specified in <code>.cdsinit</code>. The rule file specified using the environment variable has the least priority.</p> <p>Alternatively, you can use the <code>emdatafile="emDataFile"</code> option to specify the techfile in the emdata format, <code>qrctechfile="qrcTechFile"</code> to specify the QRC tech files, and <code>ictfile="ictfile"</code> to specify the file in ICT format.</p> | none |
|-----------------|------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|

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|  |                               |                                                                                                                                                                                                                                                                |      |
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|  | layermapfile="mapfile"        | Optional file that defines the mapping between the layer names in the DSPF file and the layer names in the technology file.                                                                                                                                    | none |
|  | EMOnlyICTFile="emOnlyICTfile" | Specifies the file containing only the EM rules. It is usually used in combination with qrcTechFile.                                                                                                                                                           | none |
|  | autorun=[true false]          | <p>true - run emirutil automatically after the solver to generate a text report.</p> <p>false - manually run emirutil.</p>                                                                                                                                     | true |
|  | report=[text layout html]     | <p>Defines the type of report created by emirutil.</p> <p>text - creates only the text report.</p> <p>layout - creates only the layout violation map.</p> <p>html - creates the report in html format.</p> <p><b>Note:</b> Multiple entries are supported.</p> | text |
|  | notation=[s e]                | <p>Notation for the text and html reports.</p> <p>e - engineering scale number (for example, 5.02m)</p> <p>s - scientific notation (for example, 5.02e-3)</p>                                                                                                  | e    |
|  | sort_by_net=yes no            | <p>Report IR and EM results per net, or all nets.</p> <p>yes - report EMIR results per net.</p> <p>no - combine EMIR results of all nets into one report.</p>                                                                                                  | yes  |

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|  |                                                                           |                                                                                                                                                                                                        |              |
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|  | <code>tap_model_report=yes no</code>                                      | Report the device model names for all tap devices in dynamic and static *.rpt_ir and *.spgs.                                                                                                           | no           |
|  | <code>filter_ir_percent=value</code>                                      | Defines the percentage of nodes being reported starting from the biggest IR drop. For example, <code>filter_ir_percent=5</code> reports the top 5% IR drop nodes in the violation map and text report. | no<br>filter |
|  | <code>filter_ir_threshold=value</code>                                    | Defines the IR voltage drop threshold for the node being reported. For example, <code>filter_ir_threshold=0.01</code> reports all nodes with IR drop above 0.01V.                                      | no<br>filter |
|  | <code>filter_em_threshold</code>                                          | The EM current for resistor is written only to the EM current text report if its RJ value ( <code>current_density/current_density_limit</code> ) is greater than the value specified.                  | none         |
|  | <code>warning_limit=[value<br/>warning_type1<br/>warning_type2...]</code> | Defines the maximum number of warnings per EMIR warning message.                                                                                                                                       | 50           |
|  | <code>geounit=value</code>                                                | Defines the scaling of all DSPF geometry parameters (W, L, X, Y). It applies only to the * NET section, and not to the instance section.                                                               | 1um          |

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|  |                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |     |
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|  | <code>geounit_wl=value</code> | <p>Defines the scaling of all DSPF geometry parameters <code>W</code> and <code>L</code>. The product of DSPF <code>W/L</code> * <code>geounit_wl</code> is equal to <code>W/L</code> in meters. It only applies to <code>*INET</code> section and not the instance section. <code>geounit_wl=1e-6</code> means <code>W</code> and <code>L</code> in DSPF are specified in <code>um</code>.<br/> <code>geounit_wl=1</code> means <code>W</code> and <code>L</code> in DSPF are specified in <code>m</code>. <code>W/L</code> in the binary database are always stored in <code>um</code>.</p>                                                                                                                                             | 1um |
|  | <code>geounit_xy=value</code> | <p>Defines the scaling of DSPF geometry parameters <code>X</code> and <code>Y</code>. It applies only to the <code>* NET</code> section, and not to the instance section.<br/> <code>geounit_xy=1e-6</code> means that the <code>X</code> and <code>Y</code> in the DSPF file are specified in <code>um</code>.<br/> <code>geounit_xy=1</code> means that the <code>X</code> and <code>Y</code> in the DSPF file are specified in <code>m</code>. <code>X/Y</code> in the binary database are always stored in <code>um</code>.</p> <p><b>Note:</b> If the <code>geounit_XY</code> and <code>geounit</code> options are specified together, the <code>geounit_XY</code> option takes precedence over the <code>geounit</code> option.</p> | 1um |

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|  |                                     |                                                                                                                                                                                                                                                                                    |        |
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|  | auto_detect_geounit<br>[true false] | emirutil generates an error message if the X, Y coordinates are outside the range of [-10cm 10cm] and the W, L values are outside the range of [1nm, 1mm]. If you intentionally want to keep the out-of-range values, set auto_detect_geounit to false to continue the simulation. | true   |
|  | violation_map=[failed all]          | Defines the EM violation map to be created.<br><br>failed - create map only for resistors with EM violation.<br><br>all - create map for all resistors                                                                                                                             | failed |
|  | via_count=[useR useArea]            | Defines the method used for calculating the via count.<br><br>useR - calculation based on via resistance (emdatafile_via_resistance/dspf_via_resistance).<br><br>useArea - calculation based on via area (dspf_via_area/emdatafile_via_area).                                      | useR   |
|  | idirn=[true false]                  | Prints the current direction in the EM report ( <i>Current Direction</i> column). For metal resistors, the current direction is printed. That is, <i>W</i> means that the current is flowing from east to west. For via resistors, the current direction from/to layer is printed. | false  |
|  | ir_in_em [true false]               | Reports the IR drop for each metal resistor/via in the EM current report ( <i>Max_ir</i> column).                                                                                                                                                                                  | false  |

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|             |                                                         |                                                                                                                                                                                                                                                                                                    |             |
|-------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
|             | <code>color_level=number</code>                         | Defines the number of colors displayed in the violation map. Default value is 10.                                                                                                                                                                                                                  | 10          |
|             | <code>iusercalc="file<br/>procedure"</code>             | Enables custom current calculation. The file contains the SKILL procedure, which contains the current calculation.                                                                                                                                                                                 | none        |
|             | <code>blech_path_report="file"</code>                   | Enables the printing of the blech length path for each metal layer that belongs to the net specified in the file.                                                                                                                                                                                  | none        |
|             | <code>invalid_res_width</code>                          | Ignores any resistor with $R \leq 0.001$ . and width $\geq \text{invalid\_res\_width}$ , when calculating the path length. In addition, these resistors are not reported in the EM report.                                                                                                         | 10u         |
|             | <code>recovery_factor=value</code>                      | Defines the recovery factor for iavg calculation with recovery factor. If specified, then $\text{iavg} = \max( \text{iavgpos} ,  \text{iavgneg} ) - \text{recovery\_factor} * \min( \text{iavgpos} ,  \text{iavgneg} )$ . If not specified, then $\text{iavg} = \text{iavgpos} + \text{iavgneg}$ . | none        |
| <b>time</b> | <code>window=[start1 stop1<br/>start2 stop2 ...]</code> | Time window to which the EMIR analysis is applied. It applies to all nets for which the analysis is defined. Multiple and overlapping windows are supported. An individual report is created for each time window. You can use different time windows for emirutil v/s Spectre simulation.         | [0<br>tend] |

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|  |                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |      |
|--|---------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|  | <pre> window=[start1 stop1 start2 stop2 ...] net=[net1 net2....] output=none </pre>                                                                     | <p>Black out window. The specified time windows are blacked out from the global EMIR time window. It applies only to the EMIR analysis for the specified nets.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | none |
|  | <pre> window=[start1 stop1 start2 stop2 ...] exclude [t1 t2 t3 t4] net=[net1 net2....] output=power filename="file" [analysis=avg] fmstage=[1 2] </pre> | <p>Creates average current report for static EMIR analysis. It reports the average port current for the specified nets for the active time window. The active time window is defined as <i>user-defined window</i> minus <i>exclude window</i>. The results are written to the specified file. If no file is specified, then a file with the extension <code>avgpwr</code> is created. The average current creation works independently of the dynamic EMIR feature.</p> <p>Average <math>A</math> for two active windows (<math>t1 \rightarrow t2</math>, <math>t3 \rightarrow t4</math>) is calculated as: <math>A = (A1 + A2) / (t2 - t1 + t4 - t3)</math>. <code>fmstage</code> specifies whether the current should be taken from the first stage (default) or the second stage of EMIR analysis.</p> | none |

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|               |                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |      |
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|               | <pre> window=[start1 stop1 start2 stop2 ...] exclude [t1 t2 t3 t4] net=[net1 net2....] output=power filename="file" [analysis=max] fmstage=[1 2] </pre> | <p>Creates the peak current report. It reports the peak port current and peak time for the specified nets for the active time window. The active time window is defined as <i>user-defined window</i> minus <i>exclude window</i>. The results are written to the specified file. If no file is specified, then a file with the extension <code>peakpwr</code> is created. <code>fmstage</code> specifies whether the current should be taken from the first stage (default) or the second stage of EMIR analysis.</p>                                        | none |
| <b>vprobe</b> | <pre> net=[net1 net2...] </pre>                                                                                                                         | <p>Enables voltage waveform printing of the selected nets (* NET in DSPF) for second stage iterated method. Waveforms can be printed only for nets for which IR drop or EM currents are analyzed. The waveform file is located in the <code>*.emirtap-tran</code> directory. Wildcards are supported. The format can be specified using <code>-format uwi -uwifmt &lt;format&gt;</code>.</p> <p><b>Note:</b> Waveform printing for direct method and first-stage iterated method can be enabled by using the regular <code>save/.probe</code> statements.</p> | none |



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|  |                                 |                                                                                                                                                                                                                    |                                                               |
|--|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
|  | scope=[netonly   taponly   all] | <p>The selected scope.</p> <p>netonly - save the net pin voltage waveform.</p> <p>taponly - save all tap node voltage waveforms.</p> <p>all - save voltage waveforms for net pin, all subnodes, and tap nodes.</p> | netonly. If include/exclude is used, then the default is all. |
|  | include=[pattern]               | Defines the names of subnodes and tap nodes to be included. Wildcards are supported.                                                                                                                               | *                                                             |
|  | exclude=[pattern]               | Defines names of subnodes and tap nodes to be excluded. Wildcards are supported.                                                                                                                                   | none                                                          |
|  | compression=[no   all]          | Enables waveform compression.                                                                                                                                                                                      | no                                                            |
|  | compreltol=value                | Defines the relative tolerance for waveform compression.                                                                                                                                                           | 1.00E-03                                                      |
|  | compvabstol=value               | Defines the absolute voltage tolerance for waveform compression.                                                                                                                                                   | 1.00E-06                                                      |

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|               |                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                               |
|---------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
| <b>iprobe</b> | net=[net1 net2...]          | <p>Enables current waveform printing of the selected nets (* NET in DSPF) for second stage iterated method. Waveforms can be printed only for nets for which IR drop or EM currents are analyzed. The waveform file is located in the *.emirtap-tran directory. Wildcards are supported. The format can be specified using -format uwi -uwifmt &lt;format&gt;.</p> <p><b>Note:</b> Waveform printing for direct method and first-stage iterated method can be enabled by using the regular save/.probe statements.</p> | none                                                          |
|               | scope=[netonly taponly all] | <p>The selected scope.</p> <p>netonly - save total pin current, and power gate current, if power gate exists.</p> <p>taponly - save all tap device currents.</p> <p>all - save pin currents, power gate currents, and all tap device currents.</p>                                                                                                                                                                                                                                                                     | netonly. If include/exclude is used, then the default is all. |
|               | include=[pattern]           | Defines names of the resistors to be included. Wildcards are supported.                                                                                                                                                                                                                                                                                                                                                                                                                                                | *                                                             |
|               | exclude=[pattern]           | Defines names of the resistors to be excluded. Wildcards are supported.                                                                                                                                                                                                                                                                                                                                                                                                                                                | none                                                          |
|               | compression=[no all]        | Enables waveform compression.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | no                                                            |
|               | compreltol=value            | Defines the relative tolerance for waveform compression.                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1.00E-03                                                      |

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|            |                                                      |                                                                                                                                                                                                                                                                                                                                       |          |
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|            | <code>compvabstol=value</code>                       | Defines the absolute current tolerance for waveform compression.                                                                                                                                                                                                                                                                      | 1.00E-06 |
| <b>spf</b> | <code>aliasterm="alias library_terminal name"</code> | Alias used when DSPF instance terminal names do not match the cell terminal name in the libraries.                                                                                                                                                                                                                                    | none     |
|            | <code>check=[on off]</code>                          | Enable (on) or disable (off) automatic spfchecker run for creating <code>spfxtorprefix</code> and <code>spfaliasterm</code> configuration settings for the iterated method. Spfchecker can also be enabled by setting the <code>MMSIM_SPF_CHECK</code> environment variable, as follows:<br><br><code>setenv MMSIM_SPF_CHECK 1</code> | off      |
|            | <code>rcr_report=[on off]</code>                     | Enable net-based Conly/RCR report. The report is written to a file with the extension <code>*.rpt_rcr</code> . The report generation can also be enabled by setting the <code>MMSIM_DSPF_RCR_REPORT</code> environment variable, as follows:<br><br><code>setenv MMSIM_DSPF_RCR_REPPORT 1</code>                                      | off      |

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|  |                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                           |
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|  | <code>patch_island=[no_patch skip_island patch_active patch_all]</code>                                                      | <p><code>no_patch</code>: skips any net that has an island.</p> <p><code>skip_island</code>: solves the net but ignores the island.</p> <p><code>patch_active</code>: patches only the islands with tap devices and skips the islands without tap devices.</p> <p><code>patch_all</code>: patches all islands.</p> <p>Patching is the creation of a random connection between the island and the main net with a resistor of 10kOhm; the resistor value can be set using <code>spf patch_island_rval=value</code>.</p> | <code>patch_active</code> |
|  | <code>ignore_pwr_gate_models=[model1...]</code><br><code>nets=[pwg_net1 pwg_net2...]</code><br><code>from_stage=[1 2]</code> | <p>All instances of the specified model are removed if their first and third terminals are connected to the specified nets.</p> <p><code>from_stage=1</code> (default) removes the element from the Spectre database and impacts the first and second stage.</p> <p><code>from_stage=2</code> keeps the instance in the first stage but removes it from the second stage. The net names must be specified in pairs (GPN/VPN or VPN/VPN) and may contain wildcards.</p>                                                 | <code>none+C85:F85</code> |
|  | <code>auto_detect_ignore_instances=value</code>                                                                              | <p>Enables EMIR iterated method to automatically remove elements that can be ignored. This option does not have any impact on the direct method</p>                                                                                                                                                                                                                                                                                                                                                                    | <code>none</code>         |

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|             |                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                          |       |
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|             | <code>ignore_instances=[instance names from DSPF instance_section]</code><br><code>from_stage=[0 1 2]</code> | The specified DSPF instance is removed from EMIR simulation. <code>from_stage =0</code> (default) removes the instance from the Spectre database and impacts the first and second stage. <code>from_stage=1</code> removes the instance from the Spectre database and the RC solver database. <code>from_stage=2</code> removes the instance from the RC solver database only. The instance names may contain wildcards. | none  |
| <b>spgs</b> | <code>net=[net1 net2...]</code>                                                                              | Enables the static power grid solver and defines the power nets to be analyzed.                                                                                                                                                                                                                                                                                                                                          | none  |
|             | <code>short_res_layer=[layer1 layer2....]</code>                                                             | Specifies the DSPF layer that needs to be shorted.                                                                                                                                                                                                                                                                                                                                                                       | none  |
|             | <code>no_short_res_layer=[layer1 layer2...]</code>                                                           | Specifies the DSPF layers that should not be shorted. All other layers are shorted.                                                                                                                                                                                                                                                                                                                                      | none  |
|             | <code>open_res_layer=[layer1 layer2...]</code>                                                               | Cuts the R on the specified layers (creating an open) and keeps the R on all other layers.                                                                                                                                                                                                                                                                                                                               | none  |
|             | <code>pwrgate=[powernet1 powernet2...]</code>                                                                | Specifies the power gates that need to be analyzed in the power grid solver.                                                                                                                                                                                                                                                                                                                                             | none  |
|             | <code>coupled_nets = [VDD VDD1]</code>                                                                       | Solve coupled nets together. Requires the definition of the design resistor model: <code>eisopt coupled_nets_model=[rmw1]</code> .                                                                                                                                                                                                                                                                                       | none  |
|             | <code>ldo_net=[I1.VDD_LDO]</code><br><code>ldo_driver=[X1/M1 X1/M2]</code><br><code>ldo_voltage=1.0</code>   | Defines Ldo net and LDO drivers for reff calculation.                                                                                                                                                                                                                                                                                                                                                                    | none  |
|             | <code>filter_moscap=true false</code>                                                                        | If set to <code>true</code> , tap nodes that connect to MOSFET devices are filtered out.                                                                                                                                                                                                                                                                                                                                 | FALSE |

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|  |                                                                                                                           |                                                                                                                  |          |
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|  | <code>max_rpt=value</code>                                                                                                | Report only the top value paths.                                                                                 | infinite |
|  | <code>filter_res_threshold</code>                                                                                         | Report only the paths that have the resistance value above the specified value.                                  | 0        |
|  | <code>rshort=value</code>                                                                                                 | Specifies that the resistors with <code>R&lt;rshort</code> need to be shorted during static power grid analysis. | 0        |
|  | <code>remove_dangle_res=true   false</code>                                                                               | Removes the dangling resistors.                                                                                  | FALSE    |
|  | <code>tap2sub net=&lt;net_name&gt;<br/>include=[&lt;tap_name&gt;<br/>exclude=[&lt;tap_name&gt;]</code>                    | Converts tap to subnodes.                                                                                        | none     |
|  | <code>tap2pin net=&lt;net_name&gt;<br/>include=[&lt;tap_name&gt;<br/>exclude=[&lt;tap_name&gt;]</code>                    | Converts tap to pin.                                                                                             | none     |
|  | <code>sub2tap net=&lt;net_name&gt;<br/>include=[&lt;node_name&gt;<br/>exclude=[&lt;node_name&gt;<br/>layer=[m1 m2]</code> | Converts subnode to tap.                                                                                         | none     |
|  | <code>sub2pin net=&lt;net_name&gt;<br/>include=[&lt;node_name&gt;<br/>exclude=[&lt;node_name&gt;]</code>                  | Converts subnode to pin.                                                                                         | none     |
|  | <code>tap2sub net=&lt;net_name&gt;<br/>include=[&lt;tap_name&gt;<br/>exclude=[&lt;tap_name&gt;]</code>                    | Converts tap to subnode                                                                                          | none     |
|  | <code>pin2sub net=&lt;net_name&gt;<br/>include=[&lt;pin_name&gt;<br/>exclude=[&lt;pin_name&gt;]</code>                    | Converts pin to subnode.                                                                                         | none     |
|  | <code>pin2tap net=&lt;net_name&gt;<br/>include=[&lt;pin_name&gt;<br/>exclude=[&lt;pin_name&gt;]</code>                    | Converts pin to tap.                                                                                             | none     |
|  | <code>shorted_nets=[VDD VVDD]</code>                                                                                      | Short two nets together on their *IP and perform SPGS on the combined net                                        | none     |

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|                  |                                 |                                                                                                                                                                                                           |              |
|------------------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
|                  | test_bench_less=1               | Enables the simplified SPGS flow only requiring DSPF file and subcircuit instance call or the top-level subcircuit (+top).                                                                                | 0            |
| <b>pwr_macro</b> | subckt=name<br>or<br>inst=name  | Creates power macro model for all instances of the specified subcircuit or for the specified subcircuit instance.                                                                                         | none         |
|                  | port=[name1 name2....]          | Specifies the subcircuit ports that are modeled. Wildcards are supported                                                                                                                                  | *            |
|                  | type=[max   avg   avgabs   rms] | Specifies the type of current to be measured for defining the created port DC source value. Multiple entries are supported.                                                                               | none         |
|                  | output=[subckt   table]         | Specifies the output to be generated.<br><br>subckt - generate the subcircuit macro model<br><br>table - generate a table with current and capacitance information<br><br>Multiple entries are supported. | subckt       |
|                  | outdir                          | Specifies the directory to which the macro models are written.                                                                                                                                            | raw          |
|                  | outname                         | Specifies the name for the created macro model files. The file extension is<br><i>.inst_name.subckt_name.type.</i>                                                                                        | netlist_name |

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|            |                      |                                                                                                                                                                                                                                                                   |      |
|------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|            | mode=0   1           | Specifies the type of macro model to be generated.<br><br>mode=1 creates the macro model with what-if branches for resolving potential KCL problems.<br><br>mode=0 creates the macro model with parallel resistor branch for addressing potential KCL violations. | 1    |
| <b>eco</b> | file="eco_file_name" | Enables What-If analysis and applies the changes defined in the eco_file_name. This option is supported when method=iterated or method=itereco.                                                                                                                   | none |

The EMIR control file supports the Spectre line continuation character +, and the comment lines start with character \* or string //.

### Checking the Progress of EMIR Analysis

As the simulation runs, Spectre sends messages to the screen and the simulation log file that show the progress of the simulation and provide statistical information. Following information may be significant to your EMIR analysis when you use the iterated method.

### *Hardware configuration and run-time machine loading*

In the beginning of a simulation session, Spectre prints the hardware configuration (physical memory, CPU core specification) and the run-time machine status (available memory, CPU core operating frequency, CPU loading). Since EMIR analysis often involves large-scale designs with gigabytes of data, it is important to ensure that there is sufficient memory available, with CPU operating at full speed (not in power saving mode), and the machine loading is light.

```
User: user1 Host: lnx-user1 HostID: CD0A1190 PID: 26141
Memory available: 10.2268 GB physical: 16.6236 GB
CPU Type: Intel(R) Xeon(R) CPU E5-1650 0 @ 3.20GHz
Processor PhysicalID CoreID Frequency Load
 0 0 0 3192.5 0.3
```



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|     |   |   |        |     |
|-----|---|---|--------|-----|
| 1   | 0 | 1 | 3192.5 | 0.2 |
| 2   | 0 | 2 | 3192.5 | 0.3 |
| ... |   |   |        |     |

### Reading the EMIR Control File

Spectre reads the EMIR control file before processing the circuit being simulated. All valid EMIR options are reported in the following section:

```
Reading EMIR configuration file: ../iterated.conf
~~~~~
EMIR Analysis Configuration
~~~~~
nets pwrgate = [i1.VDD i1.outp] analysis = [vmax]
nets name = [i1.VSS] analysis = [vmax]
nets name = [i1.*] analysis=[irms iavg]
spf aliasterm = "gpdk090_nmos2v 1=d 2=g 3=s"
...
emirutil techfile = emDataFile.txt
solver method = iterated
```

If one of the specified EMIR options is not displayed in the summary, check the related warnings, and correct the syntax.

### Processing the DSPF Files

Spectre processes the DSPF files and prepares a reduced circuit to be simulated. This often includes identifying the power nets and reducing them to only include parasitic capacitors, as well as identifying the signal nets and reducing the parasitic resistors and capacitors according to accuracy requirement.

```
Time for Processing DSPF file: CPU = 128.981 ms, elapsed = 60.8708 s (1m 0.9s).
Time accumulated: CPU = 167.974 ms, elapsed = 60.8709 s (1m 0.9s).
Peak resident memory used = 42 Mbytes.
```

```
Time for Creating Parasitic Database: CPU = 0 s, elapsed = 403.166 us.
Time accumulated: CPU = 170.973 ms, elapsed = 60.874 s (1m 0.9s).
Peak resident memory used = 42.1 Mbytes.
```

All coupling capacitors with  $C < 1e-16$  are grounded, while others are preserved. The `dspf_include` option `CapacitorSplitThreshold` can be used to adjust the value. Direct method and first stage iterated method do not simplify coupling caps. The second

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stage iterated method includes coupling caps in individual net solving. It biases the other terminal of the coupling cap with a voltage waveform.

### ***Running the Circuit Simulation to Produce Voltage Profiles***

At this point, with the simplification of power and signal nets, Spectre is ready to simulate the nonlinear circuit and produce voltage profiles needed for iterated EMIR analyses. This step is similar to a regular circuit simulation, where Spectre first parses the circuit, reports circuit inventory, initiates a DC analysis, and finishes the step with a transient analysis.

```
Creating probes for EMIR analysis: 36 voltage probes, 0 current probes
```

```
Time for setting up EMIR tap devices: CPU = 10.0 ms (0h 0m 0s), elapsed = 10.0 ms (0h 0m 0s).
```

```
Time for setting up EMIR analysis: CPU = 30.0 ms (0h 0m 0s), elapsed = 30.0 ms (0h 0m 0s).
```

```
Peak resident memory used = 0.95 Mbytes
```

```
...
```

```

```

```
Transient Analysis `transient1': time = (0 s -> 20 ns)
```

```

```

```
...
```

```
.....9.....8.....7.....6.....5.....4.....3.....2.....1.....0
```

```
Number of accepted tran steps = 918
```

```
Initial condition solution time: CPU = 175.973 ms, elapsed = 176.348 ms.
```

```
Intrinsic tran analysis time: CPU = 352.946 ms, elapsed = 354.783 ms.
```

```
Total time required for tran analysis `transient1': CPU = 531.918 ms, elapsed = 557.204 ms.
```

```
Time accumulated: CPU = 873.866 ms, elapsed = 62.0641 s (1m 2.1s).
```

```
Peak resident memory used = 65.2 Mbytes.
```

```
Creating EMIR waveform profile ../iterated.emirtap.pwl
```

```
Time for creating waveform database: CPU = 30.0 ms (0h 0m 0s), elapsed = 40.0 ms (0h 0m 0s).
```

The reported transient time and the accumulated time are important measures to be considered when optimizing performance. The voltage profiles of the tap devices (active devices connecting to the power and signal RC nets) are stored in the pwl files, and used as input for the second stage EMIR simulation.

This step of EMIR simulation is fully multi-threaded. It uses the number of cores defined by the `+mt` command-line option.

## ***Simulating the Parasitic RC Nets***

In the second stage of the iterated EMIR analysis, the power and signal nets are simulated together with the tap devices. During the simulation, the tap device terminal voltages over time is taken from the voltage profiles created in the first stage. In the second stage, nets are solved individually, except for coupled nets, which are solved together.

The RC network solver writes all IR drop voltage and EM current values to the binary database with the extension `emir0_bin`. Important log file content is written to the `EMIR PARASITICS ANNOTATION SUMMARY` section, which provides information on the nets and R/C elements processed. In addition, the number of solved time steps per net, and the elapsed time for the RC solving are essential when optimizing performance.

```

```

```
EMIR RC Analysis
```

```

```

```
Reading EMIR configuration file: ../iterated.emirtap.conf
```

```
~~~~~
```

```
EMIR Analysis Configuration
```

```
~~~~~
```

```
solver method = iteronly inputwf = ../iterated.emirtap.pwl
```

```
Maximum grounded vsource value = 2.5v
```

```
Searching and processing cross coupling capacitors in SPF file
```

```
/grid/cic/nsdpe-2/stefanw/emir/logfile/./adc_sample_hold.dspf
```

```
.....9.....8.....7.....6.....5.....4.....3.....2.....1.....0
```

```
Cross coupling capacitors found and processed: 0
```

```
Solving coupled nets "VDD outp": number of nodes = 594, time = (0n -> 20n)
```

```
.....9.....8.....7.....6.....5.....4.....3.....2.
.....1.....0
```

```
Total time required for EMIR RC analysis of coupled nets "VDD ... ": CPU = 480.0
ms (0h 0m 0s), elapsed = 240.0 ms (0h 0m 0s).
```

```
Completed transient analysis up to 100% at Tue Jan 12 03:53:44 2016
```

```
EMIR RC analysis accumulated time: CPU = 1.4 s (0h 0m 1s), elapsed = 1.0 s (0h
0m 1s).
```

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Peak resident memory used = 68.40 Mbytes.

~~~~~  
EMIR PARASITICS ANNOTATION SUMMARY  
~~~~~

|                            |        |                |      |
|----------------------------|--------|----------------|------|
| Nets:                      | parsed | 18 processed   | 18   |
| Cross coupling capacitors: | parsed | 0 processed    | 0    |
| Capacitors:                | parsed | 0 processed    | 0    |
| Resistors:                 | parsed | 3052 processed | 2933 |
| Nodes:                     | parsed | 2205 processed | 2205 |

Nets annotated with C-only: 0 Nets annotated with RC: 18

Detailed annotation report written in file "iterated.raw/iterated.emirtap.spfrpt"  
0 errors and 28 warnings(fixed errors)

```
 Message statistics
=====
Instance section detected 1
Small R/C excluded 96
Dangling R/C terminal 28
```

Notice from spectre.

EMIR binary file 'iterated.raw//iterated.emirtap.emir0\_bin' is generated  
(start = 0, stop = 2e-08)..

Number of nets solved = 18

Number of accepted time steps = 3148 (average 174.889 per net)

Number of rejected time steps = 187 (average 10.3889 per net)

...

Total time required for EMIR RC analysis: CPU = 1.4 s (0h 0m 1s), elapsed = 1.0 s (0h 0m 1s).

Peak resident memory used = 68.4 Mbytes

This step of the EMIR simulation is fully multi-threaded. It uses the number of cores defined by the `+mt` command-line option.

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After the EMIR data is available in the binary database, another step is performed to create the text reports for IR drop, EM currents, pin currents, and power gate information. The following output shows the related section in the log file (some content is only written to stdout):

```
Creating EMIR report, check './iterated.raw/iterated.emirtap.emirlog' for more information.
```

```
Time usage: elapsed: 150.0 ms (0h 0m 0s), CPU: 90.0 ms (0h 0m 0s)
```

```
Find PDB file (./logfile.emirtap.pdb)
```

```
Pin current report ./logfile.emirtap.rpt_pin created.
```

```
Power gate report ./logfile.emirtap.rpt_pwg created.
```

```
Completed processing EM/IR data up to:10 %
```

```
Completed processing EM/IR data up to:20 %
```

```
Completed processing EM/IR data up to:30 %
```

```
Completed processing EM/IR data up to:40 %
```

```
Completed processing EM/IR data up to:50 %
```

```
Completed processing EM/IR data up to:60 %
```

```
Completed processing EM/IR data up to:70 %
```

```
Completed processing EM/IR data up to:80 %
```

```
Completed processing EM/IR data up to:90 %
```

```
Completed processing EM/IR data up to:100 %
```

```
text IR report successfully generated.
```

```
text EM report successfully generated.
```

```
text PIN current report successfully generated.
```

```
text Power gate report successfully generated.
```

```
Note, found 4 warning messages, and 4 warnings printed.
```

**At the end of the simulation, Spectre reports the total simulation time and peak memory used.**

```
Aggregate audit (3:53:45 AM, Tue Jan 12, 2016):
```

```
Time used: CPU = 2.38 s, elapsed = 63.3 s (1m 3.3s), util. = 3.76%.
```

```
Time spent in licensing: elapsed = 60.1 s (1m 0.1s), percentage of total = 94.8%.
```

```
Peak memory used = 68.8 Mbytes.
```

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## Viewing EMIR Results

Spectre EMIR writes the IR voltage and EM current values to a binary database with the extension `emir0_bin`. In addition, it automatically calls the `emirreport` or `emirutil` binary for creating the text or html reports.

The textual/html IR drop report (file extension: `rpt_ir/rpt_ir.html`) lists the voltage drop per net (in the order of largest to smallest), and provides information about the time the maximum IR drop occurred, as well as the layer information and layer coordinates. An example section of an IR drop report is shown in the following figure:

```
VOLTAGE DROP RESULTS

BINARY FILE = aps.emir0_bin
RESULTS FILE CREATED = Mon May 7 23:07:51 2012
SIMULATOR = aps
USER SUPPLIED VALUES:
 RESULTS TYPE = TRANSIENT PEAK
 TRANSIENT START = 0
 TRANSIENT STOP = 4.2e-08
 NET NAME = VDD VSS

----- "VSS" NET: Vref=0V-----
max

VOLTAGE-DROP NETNAME TIME LAYER X Y
(V) (s) (um) (um)
2.405m VSS:F4608 42.000n NDIFF 17.028 22.518
2.361m VSS:F4510 42.000n NDIFF 19.832 24.695
2.358m VSS:F3473 1.325n NDIFF 16.268 25.770
2.297m VSS:F3432 40.325n NDIFF 15.652 25.770
```

The EM report (file extension: `rpt_em/rpt_em.html`) lists the pass/fail results for each resistor segment of a net, and provides information about the resistor name, layer, current, layer width, density (current divided by width), density limit, number of vias required, and the coordinates.

```
----- NET "AAAA" -----
rms

There is no resistor whose current density exceeds the limit.

%failed resistor layer current width pathlength density limit needed width/#vias X1 Y1 X2 Y2
(A) (um) (um) (A/um,A/via) (A/um,A/via) (um/#) (um) (um) (um) (um)
pass-100% r9 PC 167.395p 0.0370 2.381 4.524n 234.152u 0.00100 19.474 24.219 19.474 23.876
pass-100% r14 V1 9.99e-17 0.0720 0.152 9.99e-17 120.000u 1(1) 19.475 24.321 19.475 24.302
pass-100% r13 M2 6.97e-17 0.0800 0.152 8.72e-16 1.765m 0.0290 19.475 24.321 19.475 24.169
pass-100% r12 M1 1.93e-17 0.0800 0.140 2.41e-16 1.999m 0.0260 19.475 24.162 19.475 24.302
```

The EMIR text and html reports can also be created using an existing EMIR binary database using the following command:

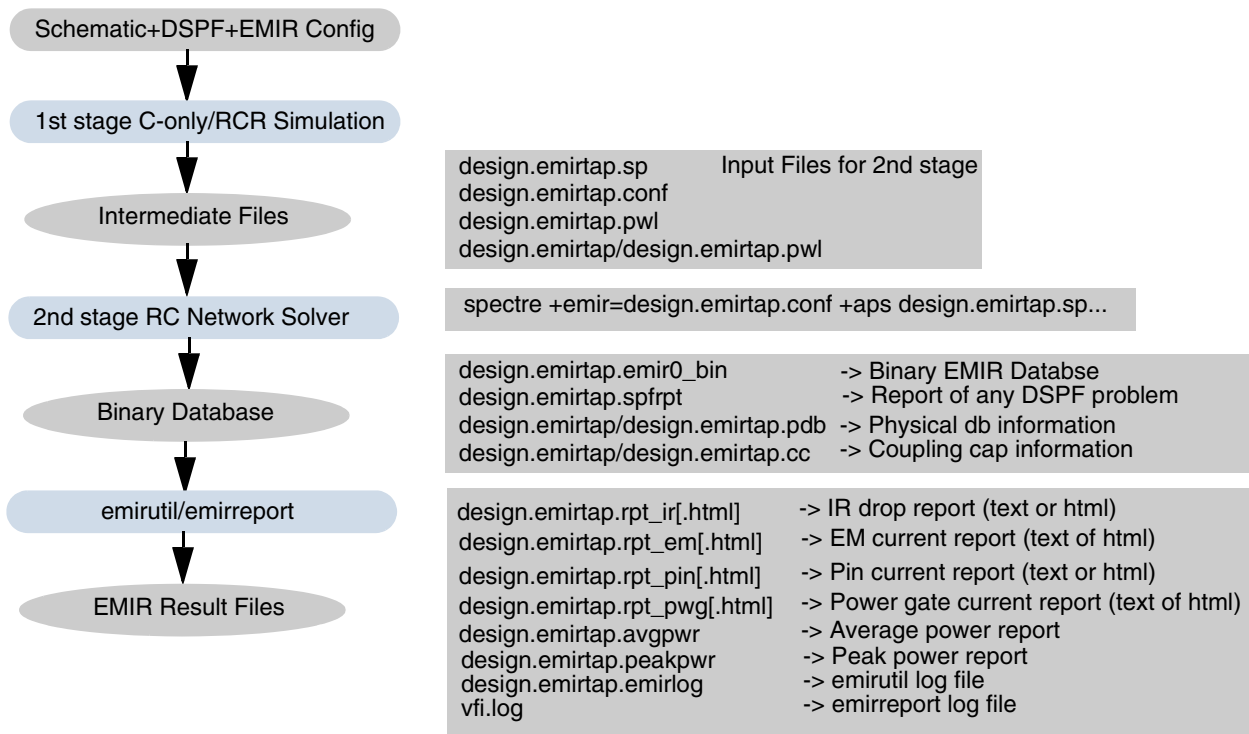
```
$ emirutil -db aps.emir0_bin -control emir.conf
```

For more information on `emirutil/vpsbatch` utility for creating the reports, and for the visualization of the EMIR analysis results in the layout, refer to the *Voltus-Fi* user manual.

If there are multiple `emir0_bin` files created by the same Spectre EMIR simulation, it is sufficient to specify only the first binary database file with the `-db` option. The utility automatically identifies all other binary database files created by the Spectre EMIR simulation.

Data Flow

The data flow of the iterated EMIR flow is shown in the following flowchart. The first stage EMIR circuit simulation creates the tap device voltage profiles which are stored in the `pwl` files, and used in the second stage. The second stage RC network solver writes all IR drop and EM current values to a binary database with the extension `emir0_bin`. This binary database is used by `emirutil/emirreport` for creating the text/html reports, and by *Voltus-Fi XL* to visualize the results in the layout.



All intermediate and output files are written into the Spectre output (raw) directory. Some files shown in the figure are only created when the related feature is enabled in the EMIR config file.

If multiple EMIR windows are used in the same EMIR simulation, a set of files is created for each EMIR time window. For example:

Time window 1: `emir0_bin`, `rpt_ir`, `rpt_em`, ...  
Time window 2: `emir1_bin`, `rpt_ir1`, `rpt_em1`, ...

The data flow for the APS direct method is the same except that the intermediate files are not created. Only the iterated method EMIR files have the `emirtap` file extension.

Direct method: `design.emir0_bin`, `design.rpt_ir`, `design.rpt_em`

Iterated method: `design.emirtap.emir0_bin`, `design.emirtap.rpt_ir`, `design.emirtap.rpt_em`

For large designs, the intermediate (`pwl`, `pdb`) and EMIR database files (`emir0_bin`) can be compressed by using the `eisopt zipfiles=2` option in the EMIR config file.

### Establishing an Accuracy Reference and Correlating EMIR Accuracy

To evaluate an EMIR solution and to select the appropriate level of accuracy and performance trade-off, it is important to establish a golden accuracy reference, and be able to correlate EMIR results compared to this reference.

#### Establishing an Accuracy Reference Using the APS Direct Method

For evaluating and optimizing the performance and accuracy of Spectre EMIR analysis results, a golden accuracy reference is required. It is recommended to select a representative small-to-medium sized design that can be simulated within reasonable time by using the APS direct method. APS direct method produces accurate EMIR golden accuracy. The following shows an example of APS direct method EMIR config:

```
net name=[X1.VDD X1.VSS] analysis=[vmax iavg]
net name=[X1.*] analysis=[irms]
solver method=direct
```

When correlating data between iterated and direct method, there is no need for including a technology file since only IR drop and EM current values are compared.

#### Correlating EMIR Accuracy

Once the iterated method is run on the same design, you can use the `emirutil` utility to compare the accuracy of iterated EMIR results with the golden APS direct EMIR results.

For example, the following command compares the IR drop results for the node `vdd` between the iterated and direct methods. All `vdd` tap points with more than 100mV and 1% of the maximum `vdd` IR drop are reported. The results are written to the file `test.erclog` in scientific notation.

```
emirutil -i iterated.rpt_ir -r direct.rpt_ir -o test -net "vdd"
 -ir_abstol 100e-6 -ir_reltol 0.01 -maxrpt all -notation s
```



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The following is an example of the comparison report:

### Top 5 ABS Error:

| No. | ABS Error | REL Error | Input Data | Ref Data | Name(net)     |
|-----|-----------|-----------|------------|----------|---------------|
| 1   | 798.000u  | 14.5%     | 4.698m     | 5.496m   | mc4#d (vdd)   |
| 2   | 789.000u  | 14.4%     | 4.698m     | 5.487m   | mc4#s (vdd)   |
| 3   | 781.000u  | 14.3%     | 4.698m     | 5.479m   | vdd#432 (vdd) |
| 4   | 770.000u  | 14.1%     | 4.698m     | 5.468m   | vdd#449 (vdd) |
| 5   | 770.000u  | 14.1%     | 4.698m     | 5.468m   | vdd#430 (vdd) |

Avg ABS Error: 237.135u  
95% Coverage: 583.000u  
ABS Err Below 356.650u: 644/1067(60.4%)

### Top 5 REL Error:

| No. | REL Error | ABS Error | Input Data | Ref Data | Name          |
|-----|-----------|-----------|------------|----------|---------------|
| 1   | 17.7%     | 636.000u  | 2.950m     | 3.586m   | mc4@1#s (vdd) |
| 2   | 17.7%     | 633.000u  | 2.950m     | 3.583m   | mc4@1#d (vdd) |
| 3   | 17.3%     | 618.000u  | 2.950m     | 3.568m   | vdd#22 (vdd)  |
| 4   | 17.3%     | 615.000u  | 2.950m     | 3.565m   | vdd#4 (vdd)   |
| 5   | 17%       | 606.000u  | 2.950m     | 3.556m   | vdd#23 (vdd)  |

Avg REL Error 4.93%  
95% Coverage: 13.9%  
REL Err Below 5.0%: 604/1067(56.6%)

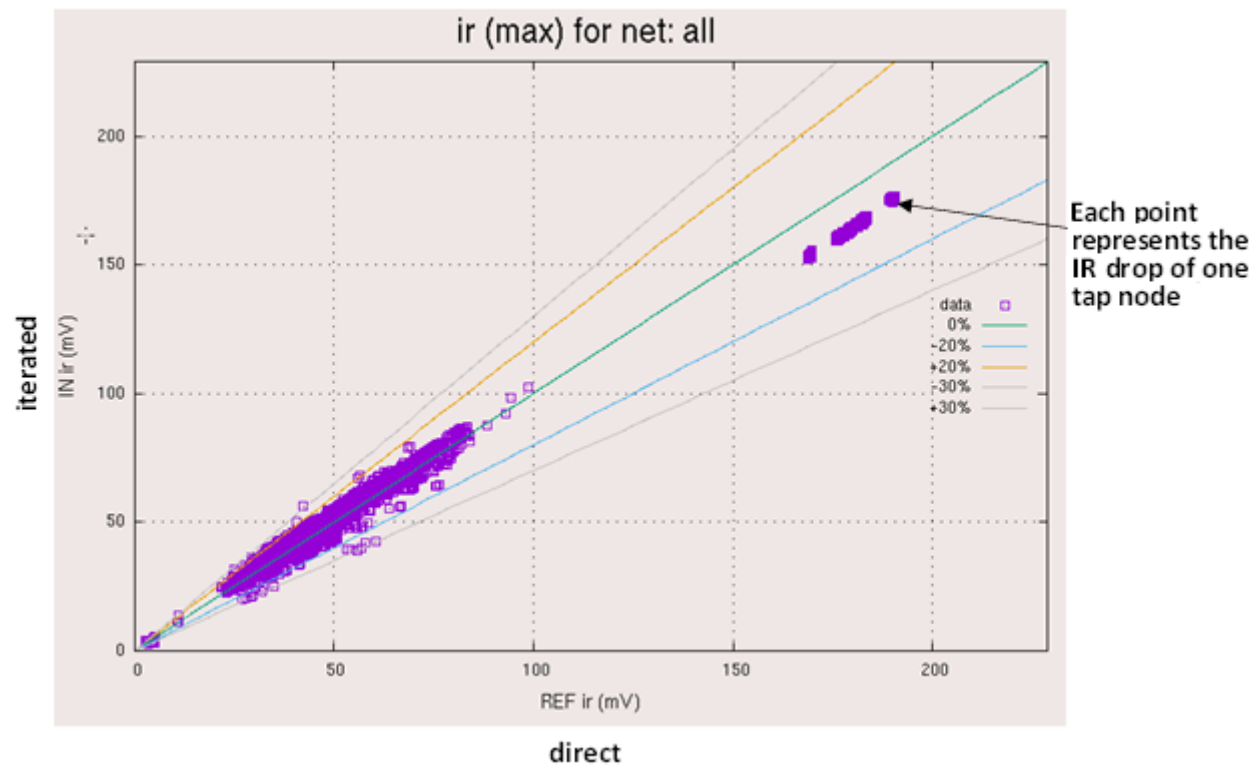
Alternatively, a GNUPLOT graph can be generated, as shown below:

```
emirutil -i input.emirtap.rpt_em -r input.rpt_em -net VDD -g
```

This command creates a GNUPLOT command file (that is, `out_VDD_em_max.plt`), and a gnuplot database file (that is, `out_VDD_em_max.dat`). The plot can be shown in GNUPLOT using the following command.

```
gnuplot -persist default_VDD_ir_avg.plt
```

The following gnuplot graph compares the IR drop for all nets of the design between iterated and direct method.



The following table describes the `emirutil` command-line options.

| Command-line Option                  | Description                                                                  |
|--------------------------------------|------------------------------------------------------------------------------|
| <code>-i input.emirtap.rpt_em</code> | Input file with EM or IR data (that is, the iterated method).                |
| <code>-r input.rpt_em</code>         | Reference file with reference to EM or IR data (that is, the direct method). |

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| Command-line Option                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>-g v-v   rele-v   abse-v</code> | <p>Create gnuplot script and database for gnuplot visualization.</p> <p><code>v-v</code> compares the input value with the reference value (default)</p> <p><code>rele-v</code> compares the relative error of the input with the reference value</p> <p><code>abse-v</code> - compares the absolute error of the input value with the reference value</p> <p>You can redirect the output to PNG, JPG, or PS files by using the <code>EMIRUTIL_GPLOT_OUT</code> environment variable as follows:</p> <pre>setenv EMIRUTIL_GPLOT_OUT png jpg ps</pre> |
| <code>-gdesp title_addition</code>    | Add additional information to the gnuplot graph title.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <code>-o EM_VSS</code>                | Define the output file name (for example, <code>EM_VSS.erclog</code> ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <code>-print_shell</code>             | If specified, also print the result in the command shell                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <code>-net "VDD_AVTR"</code>          | The nets to be analyzed. The default is <code>"*"</code> . Use <code>-net all</code> to create a single report for all nets.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <code>-comp_exclude "q[*]clk"</code>  | The nets to be excluded.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <code>-layer name</code>              | Layers to be analyzed. Default is <code>"*"</code> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <code>-ir_abstol value</code>         | The absolute cut-off value for the IR drop values to be compared. The default is 1 mV.                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <code>-em_abstol value</code>         | The absolute cut-off value for the EM current values to be compared. The default is 50 uA.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <code>-spgs_abstol value</code>       | The absolute cut-off value for effective resistors to be compared. The default value is 0.1 Ohm.                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <code>-ir_reltol value</code>         | The relative cut-off value for the IR drop values to be compared. The default is 33.3% of the maximum IR value per net.                                                                                                                                                                                                                                                                                                                                                                                                                              |

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| Command-line Option               | Description                                                                                                                                                                                                                                           |
|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>-em_reltol value</code>     | The relative cut-off value for the EM current values to be compared. The default is 0% of the maximum EM value per net.<br><br><b>Note:</b> Only tap points/resistors with value above the cut-off value and the relative cut-off value are reported. |
| <code>-spgs_reltol value</code>   | The relative cut-off value for effective resistors to be compared. Default is 0% of the max resistor value per net.                                                                                                                                   |
| <code>-maxrpt number</code>       | Report top numbers for absolute and relative errors, per specified nets. The default is 5. For a detailed report containing all tap points/resistors, use the option <code>-maxrpt all</code> .                                                       |
| <code>-notation s e</code>        | <code>e</code> is the engineering scale number. For example, 5.02m. This is the default.<br><br><code>s</code> is the scientific notation. For example, 5.02e-3.                                                                                      |
| <code>-c control.txt</code>       | Read the command-line options from the file <code>control.txt</code> .<br><br><b>Note:</b> The same syntax is used in the control file except that the dash (-) is not used.                                                                          |
| <code>-vref voltage irdrop</code> | Defines the reference for IR drop display.<br><br><code>voltage</code> - use node voltage as reference. This is the default.<br><br><code>irdrop</code> - use irdrop as reference.                                                                    |

All `emirutil` options can also be specified in a control file and included using the `-c` command-line option. The syntax in the control file does not require the dash.

The following is an example of specifying the `emirutil` options in a control file:

```
reference="/home/user/emir/direct/top2.rpt_ir"
input="/home/user/emir/iterated/top2.rpt_ir"
output=test
net="vdd avtr"
ir_abstol=1e-8
ir_reltol=0.01
maxrpt=all
notation=s
print_shell
```

The control file can be used with `emirutil`, as shown below.

```
emirutil -c control.txt
```

**Note:** The `emirutil` can be used not only to compare the direct EMIR analysis results with iterated EMIR analysis results, but also to compare the results of any two EMIR analyses.

The outcome of the correlation between the iterated and direct methods provides a good understanding of the iterated method accuracy.

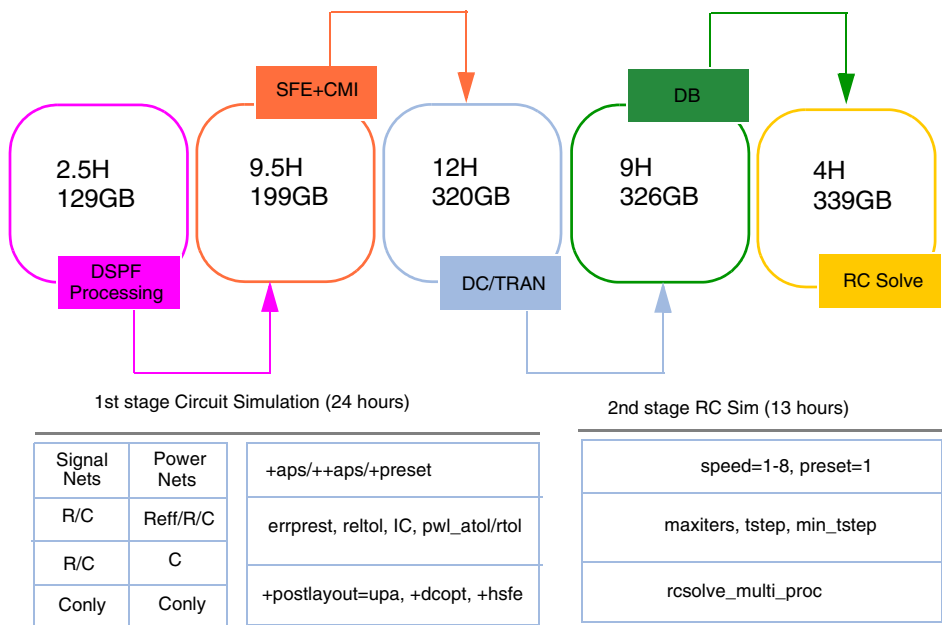
## Optimizing EMIR Analysis for Accuracy and Performance

### Understanding the Accuracy Impact and Performance Bottleneck

As discussed, the iterated method consists of a first stage circuit simulation with different simulation solver options (Spectre APS, Spectre X), and a second stage RC network solver analysis. Both stages can be optimized for accuracy and performance. The accuracy of the first stage can be improved by keeping some parasitics with the RC reduction option, in place of the default C-only simulation. Once the parasitics going into the first stage circuit simulation are decided, the performance and accuracy of the first stage circuit simulation is completely subject to the choice of simulation solver, and the solver accuracy setting (for example, `errpreset`, `++aps`, `+preset`, `+dcopt`, `+hsfe`). The accuracy and performance trade-off in the second stage is defined by the speed option. A higher value of the speed option means higher performance, and a lower value means higher accuracy. For most designs, the default `speed=5` provides the best accuracy/performance tradeoff.

The following figure shows the performance numbers for an individual EMIR analysis steps for a large representative design, and the options for trading between accuracy and performance.

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When optimizing performance, it is important to check whether it is the first stage or the second stage that dominates the overall performance. The elapsed time and time steps for each stage are reported in the Spectre log file, as shown below.

```
Number of accepted tran steps = 4590
~~~~~
Post-Transient Simulation Summary
~~~~~
Total time required for tran analysis `transient1': ..., elapsed = 12.8799 ks (3h 34m 40s)
Time accumulated: CPU = 62.375 ks (17h 19m 35s), elapsed = 21.7773 ks (6h 2m 57s).
Peak resident memory used = 60.3 Gbytes.
...
Finished EMIR transient analysis
Time usage: elapsed: 20.3 Ks (5h 39m 19s), CPU: 69.3 Ks (19h 16m 8s)

number of nets solved = 57
number of successful time steps = 114837 (average 2014.68 per net)
```

The number of time steps used in the second stage RC simulation should track the first stage circuit simulation to some extent.

### Performance and Accuracy Trade-Off in the First Stage Circuit Simulation

Since the first stage involves circuit simulation, all Spectre-related simulation options can be used for optimizing accuracy or performance. For very large digital and SRAM designs, use the following command-line options to obtain good performance in APS:

`++aps=liberal` - high performance APS solver with `errpreset=liberal`

`+hsfe` - hierarchical Spectre parser for improved parsing performance

`+dcopt=11` - high speed DC operating point calculation

`+postlayout=upa` - postlayout optimized simulation technology without RC reduction

Analog and mixed-signal designs typically require higher accuracy. The following options may provide good performance for such designs:

`++aps=moderate` - high performance APS solver with `errpreset=moderate`

`+dcopt` - high speed DC operating point calculation

`+postlayout=upa` - postlayout optimized simulation technology without RC reduction

Alternatively, Spectre X can be used with the equivalent `+preset` option. If Spectre X is used, then there is no need for specifying `+hsfe` or `+postlayout=upa`. The `+dcopt` option may still be used for optimizing the DC performance.

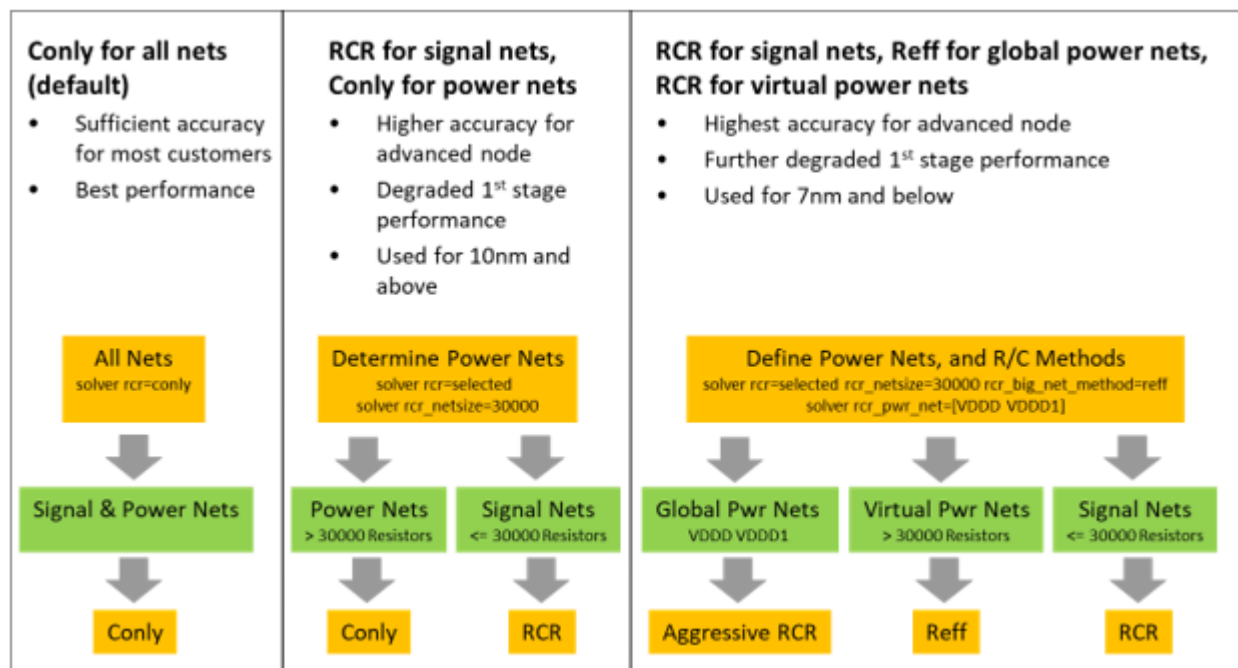
EMIR analysis can be accurate only if the circuit behaves correctly in first stage. Therefore, always check the first stage voltage waveforms for correct circuit behavior, before analyzing EMIR accuracy.

EMIR accuracy can be significantly improved by changing the first stage from the default C-only method to RC modeling methods. When this is needed, it is recommended to apply RC reduction to the signal nets and leave the power nets to be C-only. You can use the `rcr_netsize` option to define signal versus power nets. A typical value is `rcr_netsize=30000`, which means that all (power) nets with more than 30000 resistors are processed with C-only while all (signal) nets with less or equal 30000 resistors are processed with RC reduction. The default value of `rcr_netsize` is 30000.

The accuracy can be further improved by additionally using the RSNAP or Reff method for the power nets. However, this needs to be performed carefully because power nets can be huge and applying RCR may cause the degrade performance to be similar to the direct method. The recommended approach is to use RCR on the smaller global power nets, and Reff on the larger virtual power nets. This is a very conservative approach and is recommended only for advanced node designs.

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The following figure shows the three methods.



The first stage modeling method for the signal nets and power nets can be defined respectively using the options `rcr_small_net_method` and `rcr_big_net_method`. The advanced users may differentiate between the large and huge power nets by using the options `rcr_huge_netsize` (default is infinite). For huge nets, the Reff method is used.

Alternatively, there are options for assigning individual nets to the three categories of nets:

- Only nets: `solver c_net=[name 1 name2...]`
- RC reduced signal nets: `solver rcr_net=[name1 name2...]`
- Aggressive RC reduced power nets: `solver rcr_pwr_net=[name1 name2...]`
- Reff power nets: `solver reff_pwr_net=[name1 name2...]`
- Rsnap/Reff power nets: `solver rsnap_reff_pwr_net=[name1 name2]`

The name-based options support wildcard and have higher priority than the size-based `rcr_pwr_netsize` setting.

The accuracy of the RC reduction methods can be adjusted by setting the cut-off frequency.

- `rcr_fmax=value` - Cut-off frequency for the conservative signal net RC reduction (default is 20GHz)



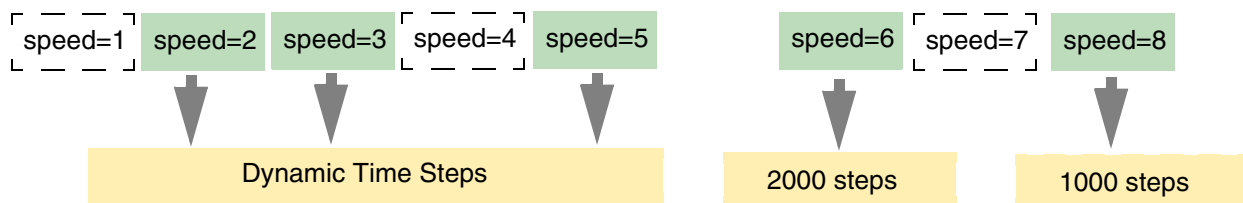
## Spectre Classic Simulator, Spectre APS, Spectre X, Spectre XPS, Spectre FMC Analysis, and Legato Reliability Solution User Guide

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- `rcr_pwr_fmax=value` - Cut-off frequency for the moderate power net RC reduction (default is 5GHz)

### Speeding Up Second Stage RC Simulation

The `speed` option defines the accuracy and performance of the second stage RC network solver. `speed=8` provides the highest performance while `speed=1` provides the highest accuracy. `speed=1-5` use adaptive time steps while `speed=6-8` use fixed time steps.



For most designs, the default `speed=5` provides the best accuracy/performance tradeoff. Only rare cases require you to adjust the `speed` option.

If (for debugging) a fixed time step is required, you can use the `tstep` option, as follows:

```
solver tstep=1p
```

Also, the RC network solving performance can be improved by using multiple (forked) processes in addition to the default multi-threaded processing. Multi-processing can be enabled with the following option:

```
solver rcsolve_multi_proc=on
```

When enabled, the total number of cores at any time is defined by the `+mt` Spectre command-line option. Small nets (`<rcsolve_1t_netsize`) are solved first with eight forked single-thread processes. Medium nets are solved next with two forked four thread processes. Big nets (`>rcsolve_4t_netsize`) are solved with one main process using eight threads.

The overall EMIR performance can be improved by pipelining the first and second stage EMIR solving. By default, the Spectre EMIR flow runs the first and second stages sequentially. However, if both the stages are the dominant parts of the overall EMIR simulation, the second stage solving can be started while the first stage is still running. In the pipelined approach, the second stage solving reads the partial results from the first stage, and calculates the related EMIR data while the first stage continues in the transient simulation. You should define the large time-consuming (power) nets as pipelined nets, while smaller nets can be solved with the regular method. The pipelined processing can be enabled with the following option.

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```
solver pipeline_nets = [net1 net2 ...]
```

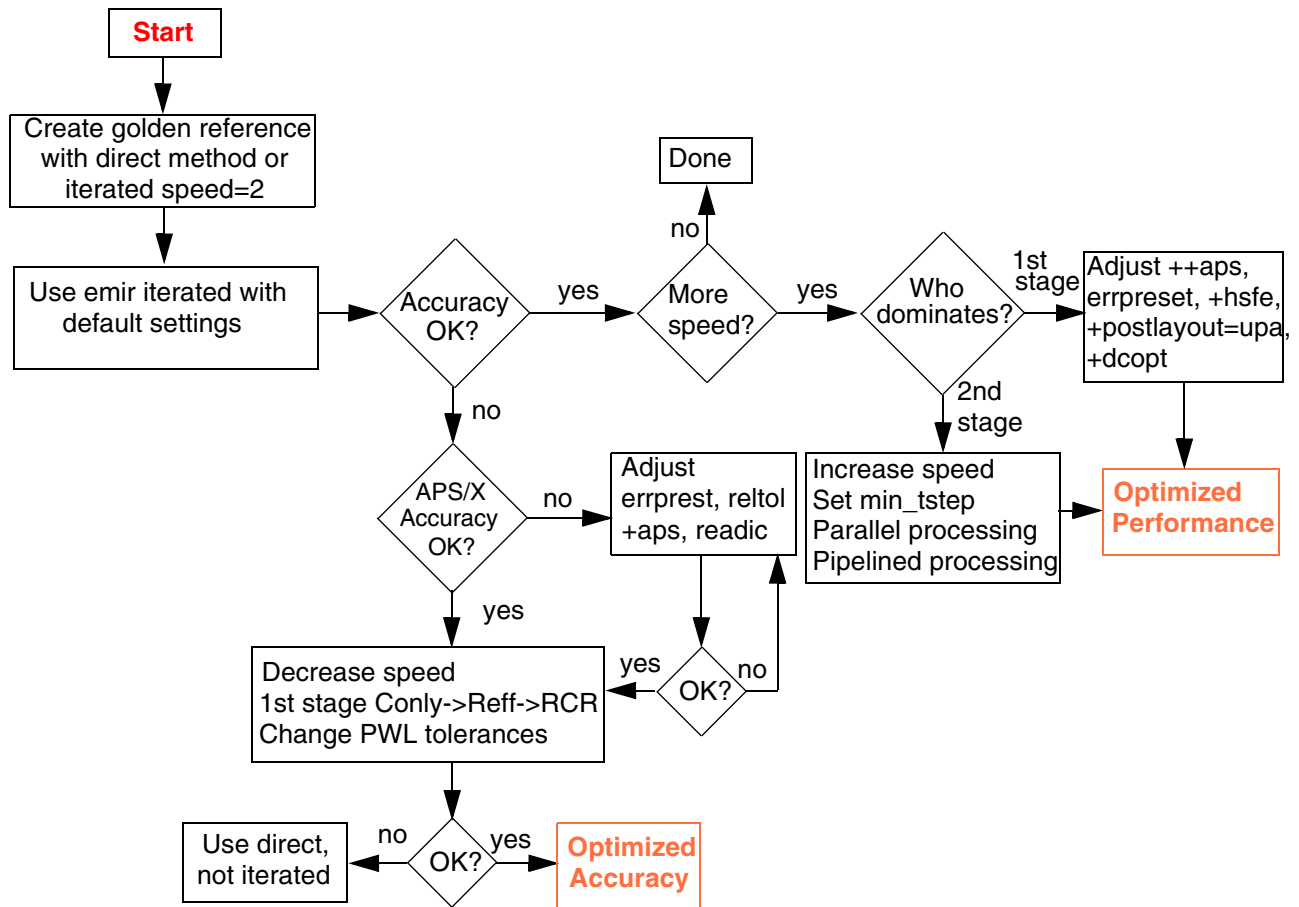
Pipelining is recommended when:

- Both first and second stages are both dominant parts of the overall EMIR simulation time
- Large net solving dominates the second stage solving
- Transient time and the EMIR time window are heavily overlapping

Spectre EMIR uses multiple processes when multi-processing and pipelining are enabled. Job distribution systems like `lsf`, `rsh`, and `nc` can be used to distribute EMIR subprocesses to a server farm.

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The following flowchart describes the overall flow about how to optimize the EMIR accuracy and performance:



## Highest performance settings:

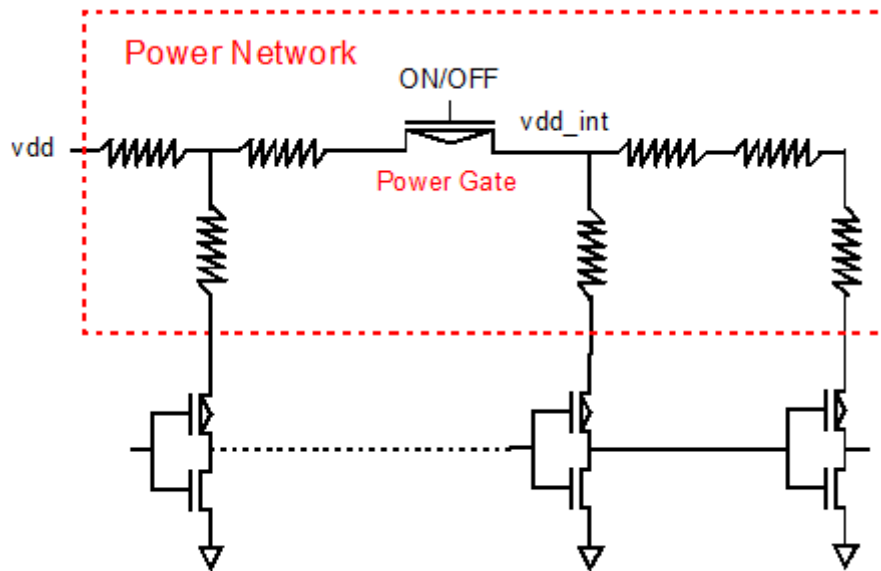
spectre ++aps=liberal, +dcopt=11, +hsfe, +postlayout=upa OR  
 spectre +preset=vx +dcopt=11  
 solver method=iterated speed=8  
 solver rcsolve\_multi\_proc=on

## High accuracy settings

spectre +aps=moderate +postlayout=upa OR  
 spectre +preset=mx  
 solver method=iterated rcr=selected

## Power Gate Support

Power networks may contain power gates (four-terminal MOSFET device) which enable or disable the power supply in the circuit. These power gates split the power supply RC network into two parts; the RC network driving the power gate, and the RC network being driven by the power gate. These nets are strongly coupled together and they should be simulated together in EMIR analysis.



To invoke power gating handling, add the power gate setting in the EMIR control file (`emir.config`), as shown below.

```
net pwrgate=[vdd vdd_int] analysis=[vmax]
```

Both, the global power supply net `vdd` driving the power gates, and the virtual internal power supply net `vdd_int` driven by the power gates, need to be specified in the `net` statement in any order. Wildcards are supported for internal power supply nets, but not for power supply nets. If one power supply net drives multiple power gates, one statement with all power supply nets needs to be defined, as shown below.

```
net pwrgate=[vdd vdd_int1 vdd_int2] analysis=[vmax]
```

The IR drop report includes both the power supply net in the usual report file name, for example, `input.rpt_ir` and the internal power supply net is reported in a file, such as `input.rpt_pwg` or `input.emirtap.rpt_pwg` for direct and iterated methods respectively. The IR drop for the virtual power net includes the voltage drop on the global power net, the voltage over the power gate, and the voltage drop on the virtual power net. EM analysis is performed as usual, if specified.

In addition, an important parameter `Ton` is also reported in the `.rpt_pwg` file. It reports the time taken to power-up the terminal of the internal power supply net to 95% of the power supply level (VDD).

**Note:** The parameter `Ton` can be infinity if the internal power supply level does not reach 95% of VDD.

Each `pwrgate` statement allows you to define only one global power node and the related virtual power nodes. If a design contains multiple global nodes with power gates and virtual nodes, then, for each of them, a separate `pwrgate` statement is required.

Serial power gate structures are supported. For such gate structures, not only the top-level power supply net and the internal supply net, but also the net between the serial power gates needs to be specified.

Complex power gate subcircuits are supported if the subcircuit terminals 0, 1, 2, 3 connect to the MOSFET terminals d, g, s, b, and if subcircuit terminals 0 and 2 connect to the global and virtual power nets. Other two-terminal devices are allowed in the subcircuit, but controlled elements and current sources inside the subcircuit are not supported. You may manually define the MOSFET subcircuit, as shown below.

```
solver mosfet_subckt=[subckt_name1 ...]
```

## Handling the Complexity of DSPF/SPEF files

### SPF Checker

The DSPF files are created with parasitic extraction tools like QRC. The content and format of a DSPF file is heavily dependent on the extraction tool and the settings. Very often, simulation problems occur due to problems in the DSPF file.

SPF Checker is a utility shipped as a part of MMSIM release which analyses a DSPF file, reports problems which may cause simulation problems, and creates an EMIR configuration file with the recommended mapping statements for EMIR analysis. In addition, it creates a configuration file for the Spectre DSPF parasitic backannotation flow (SPF).

The DSPF checker is a binary shipped with MMSIM under the location `.../lnx86/bin/spfchecker` . The following command line arguments are supported:

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```
spfchecker SPF_FILE_NAME[-detail <value>] [-message <value>] [-log LOG_FILE_NAME]
-c EMIR_CONF_NAME] [-ckt=subckt_name] [-ctl=filename] [+lorder licenseList]
-force -help
```

| Argument           | Description                                                                                                                                                |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| -dspf              | If the input is in DSPF format (default).                                                                                                                  |
| -spef              | If the input is in SPEF format.                                                                                                                            |
| -outdir <dir_name> | Set the output directory for the checker results. Default is .                                                                                             |
| -detail            | Report detailed information (statistics) for NETs whose subnodes are more than the value specified using -d. Default is 0.                                 |
| -message           | Set the maximum number of messages for each type of error. Default is 50.                                                                                  |
| -log name          | Set the checker log file name. If this argument is not specified, a file with the name <code>SPF_FILE_NAME.chklog</code> is created by default.            |
| -c name            | Create the EMIR configuration file. If this argument is not specified, a file with the name <code>SPF_FILE_NAME.emir_conf</code> is created by default.    |
| -opt name          | Create a back annotation option file. If this argument is not specified, a file with the name <code>SPF_FILE_NAME.stitch_opt</code> is created by default. |
| -ckt subckt        | Define the subcircuit scope. Default is the first subcircuit definition found.                                                                             |
| +lorder            | Specify the license checkout order. The default checkout order is <code>PRODUCT:MMSIM</code>                                                               |
| -fix name          | Fix the common connection errors and create a new DSPF file.                                                                                               |
| -dump_cc name      | Dump the cross coupling capacitors into the named file                                                                                                     |
| -dump_lvl level    | Set the level to dump the original coupling capacitors. Default is 0.                                                                                      |
| -force             | Overwrite the previous SPF checker results.                                                                                                                |
| -ctl file          | Exclude the parasitic resistors specified in the list. For example, ctl file: <code>spf_ignore_layers = [M1 M2]</code>                                     |

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| Argument | Description                                      |
|----------|--------------------------------------------------|
| -help    | Display help related to the SPF Checker utility. |

The SPF checker creates the following files:

- `test.spf.chklog` - Detailed SPF checker log file
- `test.spf.spfinfo` - DSPF element inventory
- `test.spf.emir_conf` - Recommended settings for EMIR config file
- `test.spf.stitch_opts` - Recommended (SPICE format) settings for DSPF back annotation

Before running any EMIR analyses, ensure that your DSPF file is clean. This can be achieved by running the `spfchecker` utility and by confirming that `spfchecker` does not report an error message in the `*chklog` file. Typical error messages in the `chklog` file are:

```
SPF-0003: 2 ERROR: NETs broken into pieces
SPF-0016: 6 ERROR:Instances with different connection from
 the NET Section
SPF-0019: 430 ERROR: NETs with sub-nodes not connecting to any
 parasitics
SPF-0028: 1 ERROR: Instance model terminal definition conflicts
SPF-0039: 3854807 ERROR: Layer is extracted as both via and metal layer
```

Simulating a DSPF file for which `spfchecker` reported errors may generate invalid EMIR simulation results. If `spfchecker` reports warnings and no errors, the DSPF file can be used in EMIR analysis.

Additionally, `spfchecker` prepares content for the EMIR config file into the `*.emir_conf` file. This content can either manually be copied into the EMIR config file, or included with an `include` statement:

```
include test.spf.emir_conf
```

## Port Order Handling

When setting up the EMIR simulation, you need to ensure that the subcircuit port order in the DSPF file matches the port order of the instance call in the top-level netlist. Very often there may be cases where the port order between the top-level instance call and the DSPF subcircuit do not match. For such cases, the following three solutions are available:

1. Manually change the port order of the instance call in the top-level netlist to match the port order in the DSPF subcircuit call.
2. When setting up the simulation in ADE, copy the port order from the DSPF file to the CDF `termOrder` of the related cell and switch the cell view of this cell to the DSPF file using the *Specify SPICE source File* option. The netlister uses the CDF `termOrder` and creates the same order in the instance call.
3. Reuse the instance call from the pre-layout schematic netlist, and read in the pre-layout schematic netlist to the DSPF file. In addition, use the `.dspf_include` command (instead of `.include`), which provides advanced functionality for port order mapping, as follows.

```
.dspf_include file.spf port_order=[spf|sch] extra_port=[true|false]
bus_delim="busdelim_schematic [busdelim_parasitic]"
case_sensitive=[true|false] selected_inst="X1" shortPins=[yes|no]
```

If you use `.dspf_include`, the following rules apply:

- a. By default, the subckt description is taken from the DSPF file independent on whether the same subckt description is available in the schematic netlist. If the same subckt is instantiated multiple times, and the subckt is defined in both, schematic netlist and DSPF, then the user can define which subckt definition to use in which instance.
  - `selected_inst="X1"` – Will use the DSPF subcircuit definition for instance X1 while all other instances will use the schematic subcircuit definition.
- b. Depending on the `port_order` option, the port order of the subcircuit definition is taken from the pre-layout schematic netlist or from the DSPF file subcircuit definition, as shown below.
  - `port_order=sch` – (Default). The port order is taken from schematic subcircuit definition. The same port number and names are required. If the schematic subcircuit definition is not available, a warning is issued in the log file, and DSPF port order is used.
  - `port_order=spf` – The port order is taken from the DSPF subcircuit definition.



- c. By default, the extra ports in the DSPF or schematic subcircuit definition cause the simulation to stop. However, the `extra_port` option enables a special handling of extra subcircuit ports.
- `extra_port=false` – (Default) The port number in the schematic and the DSPF file needs to be the same. If not, the simulation will stop.
  - `extra_port=true` – The extra ports in the DSPF subcircuit call are changed to internal nodes. In addition, the extra ports in the schematic subcircuit definition are connected to nodes with the same name in the DSPF netlist, otherwise, they will be floating. A report is issued in the log file containing information on the subcircuit ports that do not match and how to handle them.
- d. The `bus_delim` option enables you to map the bus delimiter between the schematic and DSPF/SPEF files. This option defines the bus delimiter in the schematic netlist, and optionally the bus delimiter in the DSPF file. By default, the bus delimiter of the DSPF file is automatically taken from the DSPF file header (that is, `*|BUSBIT []` or `*|BUS_DELIMITER []`). If the bus delimiter is not defined in the parasitic file header, you need to specify it in the `dspf_include bus_delim` statement. If both are specified, then the parasitic file bus delimiter is taken from the `dspf_include bus_delim` option.
- `bus_delim="<>"` – `A<1>` is mapped to `A_1` in the DSPF file, if the bus delimiter in the DSPF file header is `_`.
  - `bus_delim="@ []"` – `A@1` is mapped to `A[1]` in the DSPF file.
- e. By default, the DSPF file is considered case insensitive (`case_sensitive=false`). You can set the `case_sensitive` option to `true` to make the DSPF file case sensitive. You can use the `duplicate_subckt=warn|ignore` option to use the last definition.
- f. By default, Spectre uses the subcircuit definition for all instances of a subcircuit from the DSPF file even if it is also defined in the schematic. If a subcircuit is instantiated multiple times, you can specify the instances for which the subcircuit definition is to be used from the DSPF file. For all other instances, the definition is used from the schematic.
- For example, if `selected_inst="X1 X2"`, Spectre uses the subcircuit definition for instances X1 and X2 from the DSPF file. For other instances, it uses the definition from the schematic.
- Note:** Spectre does not support multiple definitions of a subcircuit in multiple DSPF files. If a subcircuit is defined in multiple DSPF files, Spectre returns an error.
- g. If the same subcircuit is defined multiple times in one or multiple DSPF files, the simulation stops.

- h.** If the net contains multiple \*I P split pins and if +emir is used on the command line, the extra pins are shorted to the primary pin because when +emir is used, shortPins is automatically set to yes. In the following example, pin VDD%1 and VDD%2 are shorted to primary pin VDD:

```
*|NET VDD
*|P VDD
*|P VDD%1
*|P VDD%2
```

When +emir is not used on the command line, shortPins is set to no and the pins are not shorted.

The following table lists the differences between include and dspf\_include:

| Scenario                                                                                  | include/.include                                                                                                                                                                                                | dspf_include/.dspf_include                                                                                 |
|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| Same subcircuit definition in the schematic netlist and DSPF file                         | Default: Error out<br>Use<br>duplicate_subckt=warn<br>  ignore to use the last definition<br><br>Subcircuit content from the schematic or DSPF is taken depending on the order of the definition in the netlist | Subcircuit content from DSPF is taken independent of the order of the subcircuit definition in the netlist |
| Port order does not match between the instance call and the DSPF subcircuit definition    | Port order needs to be manually adjusted                                                                                                                                                                        | The port_order option can be used to automatically adjust the port order                                   |
| Port number in DSPF does not match the port number in the schematic netlist instance call | Extra ports need to be removed manually                                                                                                                                                                         | The extra_port option can be used to automatically handle extra ports.                                     |
| Multiple DSPF files are included with the same subcircuit definition                      | Default: Error out<br>Use the<br>duplicate_subckt= warn<br>  ignore to use the last subcircuit definition                                                                                                       | Default: Error out<br><br><b>Note:</b> Duplicated DSPF subcircuit definition is not supported.             |

| Scenario                                                                                                        | include/.include                 | dspf_include/.dspf_include                                                                                                                                  |
|-----------------------------------------------------------------------------------------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>*   NET contains multiple pins</p> <p>*   NET VDD</p> <p>*   P VDD</p> <p>*   P VDD%1</p> <p>*   P VDD%2</p> | Pins need to be shorted manually | <p>Pins are automatically shorted.</p> <p>Pin VDD%1 and VDD%2 are automatically shorted to pin VDD.</p> <p>Pins are not shorted when +emir is not used.</p> |

Additionally, `dspf_include` reads all the DSPF lines starting with \* (\*|NET, \*|I, \*|P, \*|S), while `include` considers all related lines as comments. This enables `dspf_include` to fix the connectivity of broken nets, which cannot be done with `include`.

## SPEF Netlist Support

The Spectre EMIR solution also supports SPEF postlayout netlists. Unlike the DSPF files, the SPEF netlist always contains the combination of a schematic netlist with the active devices and the SPEF netlist with the parasitic element information. Mismatches on the subcircuit instance names related to leading X's are automatically detected and resolved. Use the `spef_include` statement to include an SPEF file in the schematic netlist, as shown below.

```
spef_include "example.spef" inst="I0" (Spectre Syntax)
.spef_include "example.spef" inst="I0" (SPICE Syntax)
```

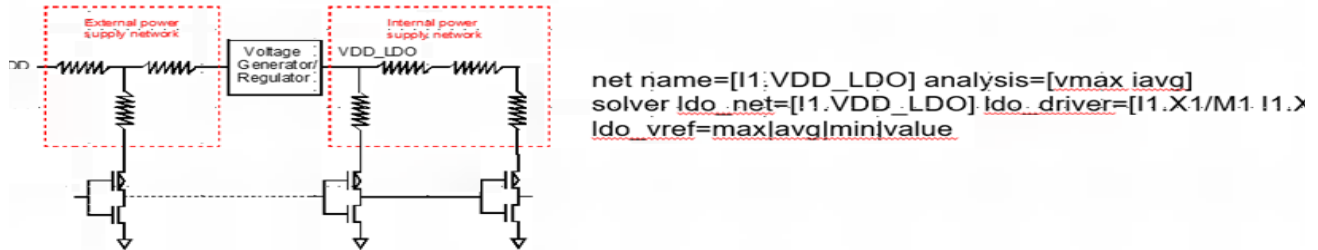
The SPEF flow uses the same EMIR control file as in the DSPF flow. You also need to specify the control file on the Spectre command line with the `+emir=emir.config` statement.

## Advanced Analyses

### Voltage Generator (LDO) IR Drop Analysis

IR drop analysis (analysis=[vmax vavg]) is typically applied to power nets, they are driven by voltage sources which provides a constant reference voltage over the EMIR window. Nevertheless, designs may have internal generators or regulators. For the generator driven nets an IR drop analysis may be important. These nets behave like signal nets since their voltage value is changing over time.

The Spectre EMIR LDO feature enables the user to perform IR drop analysis on LDO nets like the VDD\_LDO in the following graphic.



The LDO feature is enabled with the `ldo_net` solver option in the EMIR config file. It works in dynamic, and static EMIR, as well as in SPGS.

## Dynamic LDO IR Drop Analysis

In dynamic EMIR the net `VDD_LDO` is handled like any signal net. Nevertheless, there is an IR drop report created. Based on the users setting the IR drop reference voltage can be the min, the max, or the average voltage of the `ldo_driver` nodes over the EMIR time window. Alternatively, the user can define a fixed reference value, i.e. `ldo_vref=1.1`.

```
net name=[I1.VDD_LDO] analysis=[vmax iavg]
solver ldo_net=[I1.VDD_LDO] ldo_driver=[I1.X1/M1 I1.X1/M2]
ldo_vref=max|avg|min|value
```

Instead of defining the individual `ldo_driver` MOSFET devices, the user may define the LDO MOSFET instance name, i.e. `ldo_inst=[I1.X1]`. In that case all MOSFET's with `I1.X1` in instance name are considered LDO driver MOSFET devices. While the `ldo_driver` option supports wildcarding on the name inside DSPF, the `ldo_inst` doesn't support wildcarding.

## Static LDO IR Drop Analysis

In static EMIR the `ldo_driver` nodes are shorted together and connected to a `vsources` with the voltage value defined in `ldo_vref`.

```
net name=[I1.VDD_LDO] analysis=[vmax iavg]
static ldo_net=[I1.VDD_LDO] ldo_driver=[I1.X1/M1 I1.X1/M2] ldo_vref=1.0
```

The static EMIR current distribution for this net is same as for any other power net. The static current for the `VDD_LDO` net needs to be defined in the "static ifile".

```
I1 VDD_LDO 0.02
```

It is distributed to all tap devices but not the ldo\_driver devices (I1.X1/M1 and I1.X1/M2). If VDD\_LDO has a \*IP, then no current will be assigned to this pin and no loading from this pin will be considered in the static EMIR analysis.

### SPGS LDO Handling

In SPGS the ldo\_driver nodes are shorted together and used as \*IP. If there are other \*IP on the VDD\_LDO net, then they are changed to subnodes (\*IS).

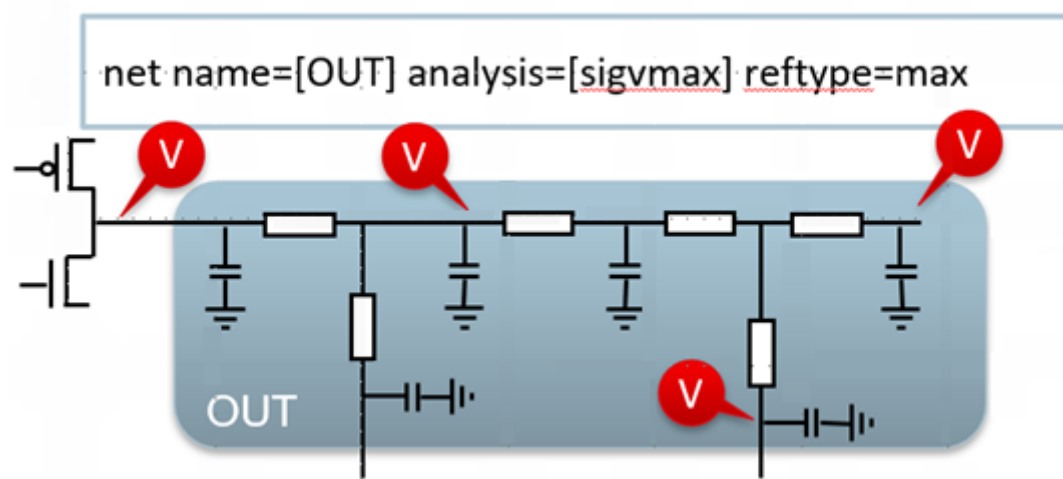
```
spgs ldo_net=[I1.VDD_LDO] ldo_driver=[X1/M1 X1/M2] ldo_voltage=1.0
```

The SPGS reff value for all tap devices is calculated in reference to shorted ldo\_driver nodes. The voltage value used for the reff calculation is defined by the ldo\_voltage option. Instead of the ldo\_voltage the option ldo\_vref may be used.

### Signal Net IR Drop Analysis

With the introduction of the LDO IR drop analysis, the signal net IR drop analysis has become less important. The main question you need to ask is, what is the value of calculating IR drop for a signal net, when there is no clearly defined voltage reference since all node voltages are changing at all times. Furthermore, since the number of signal nets is typically large, the feature will cause the creation of lots of IR drop data which may not be needed or may be challenging to read.

The signal net IR drop analysis is enabled with the `vmax` or `vavg` analysis statement.



Different methods for defining the reference voltage are supported:

The following are supported for defining the reference voltage:

- `reftype=max` - Use the maximum voltage of all nodes at each time point.
- `reftype=avg` - Use the average voltage over all nodes at each time point (default).
- `reftype=pin findsrc=true` - For the given nets, use the `vsource` connected to \* | P node.
- `reftype=pin findsrc=false` - For the given nets, use the \* | P node as the reference, and not `vsource`.
- `refnode=name` - Use the specified sub node of \* | NET as reference.
- `vref=value` - Use the specified voltage as reference.

When using `reftype=max` for a net with three subnodes: `net1:1` (1V), `net1:2` (2V), and `net1:3` (3V), the detected reference voltage will be 3V, and the IR drop calculated will be 2V for `net1:1`, 1V for `net1:2`, and 0V for `net1:3`. When using `reftype=avg` the reference voltage will be 2V, and the IR drop calculated will be 1V for `net1:1`, 0V for `net1:2`, and -1V for `net1:3`.

The signal net IR drop analysis is automatically changed to a regular IR drop analysis (`vmax`), if `vref=value` is specified, or if the net (during the EMIR time window) is driven by a constant voltage source.

### Design Resistor EM Current Analysis

By default, the EM current analysis is only performed on parasitic resistors defined in the RC net section of the DSPF file. If required, Spectre EMIR solution allows the EM analysis to be performed for design resistors in the DSPF instance section, as shown below. This analysis can be applied to primitive resistor elements, or resistors defined with subcircuit definitions.

```
net design_res_models=[resistor] analysis=[iavg] (primitive resistor)
net design_res_models=[name=rhim] analysis=[iavg] (resistor subckt rhim)
```

For design resistors, the parameters `$l`, `$w`, and `$lvl` are expected to be defined for primitive resistor calls, and `l` and `w` for subcircuit resistor calls in the DSPF instance section. When the parameter names are inconsistent in the DSPF file, name mapping rules can be specified in the EMIR configuration file, as shown below.

```
net design_res_models=[name=rhim_m l=lr w=wr] analysis=[iavg]
```

Layer information and units for `l` and `w` can be defined in the EMIR configuration file, as shown below.

```
net design_res_models=[name=rhim_m layer=mt1 unit=1] analysis=[iavg]
```

The product of design resistor `W/L * unit` defines W/L in meter. The default value of `unit` is 1.

The EM results related to design resistor are reported in the `design.rpt_em` file, as shown below.

| ----- NET "_CDNS_MMSIM_DESIGN_RESISTOR" ----- |          |                |          |       |            |         |        |        |             |         |        |         |      |
|-----------------------------------------------|----------|----------------|----------|-------|------------|---------|--------|--------|-------------|---------|--------|---------|------|
| avg                                           | %failed  | resistor layer | current  | width | pathLength | density | limit  | needed | width/#vias | X1      | Y1     | X2      | Y2   |
| resistance                                    |          |                | (A)      | (um)  | (um)       | (A/um)  | (A/um) | (um/#) |             | (um)    | (um)   | (um)    | (um) |
| (ohm                                          |          |                |          |       |            |         |        |        |             |         |        |         |      |
| pass-95.39%                                   | 10.R3035 | mt1            | 367.651u | 7.25  | 61.600     | 50.701u | 1.110m | 0.33   | 47.070      | -65.510 | 47.070 | -65.510 | 884  |

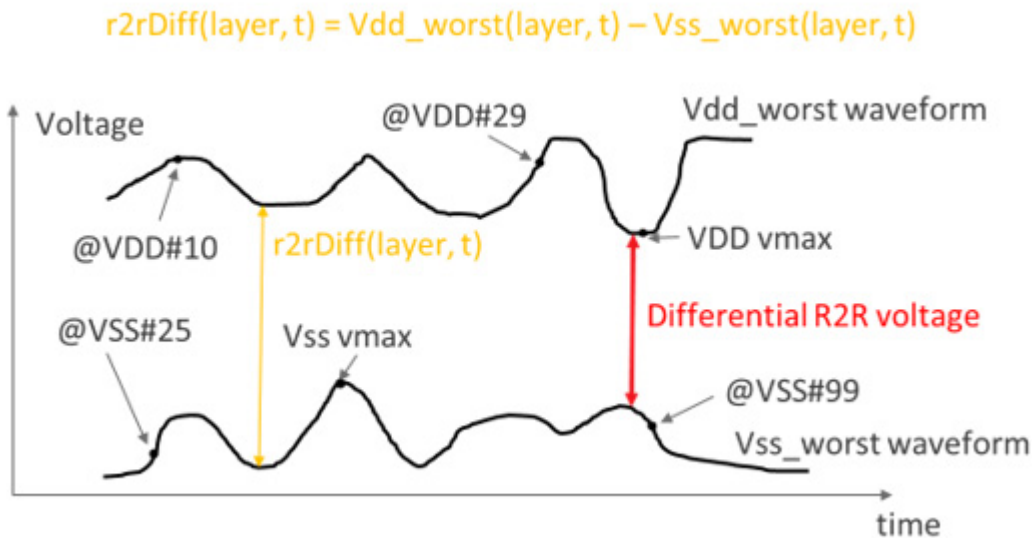
If the layer name is not specified, but a resistor model name is defined, then the resistor model name is reported as the layer name.

By default, Spectre EMIR evaluates the current on the first terminal of the design resistor. However, you can define the index of the design resistor terminal you want the current to be evaluated at, as shown below.

```
net design_res_models=[name=rhim_m term=3] analysis=[iavg]
```

Differential (Rail-to-Rail) IR Drop Analysis

The differential IR drop feature allows you to identify the worst-case IR drop between the specified power supply and the ground node. At each time point, it calculates the worst IR drop over all the power supply sub nodes, and the worst IR drop over all the ground sub nodes. At each time point, it also calculates and reports the worst case rail-to-rail voltage for the given EMIR time window.



The differential IR drop analysis is enabled with the `analysis=r2rvmin` option. Multiple power supply nodes can be specified. If the ground node is not specified in the `r2r_refnet` statement, Spectre automatically detects the global ground node.

```
net name=[VDD] r2r_refnet=VSS analysis=[r2rvmin]
```

The following is an example of a differential IR drop report:

| POWER-GROUND MINIMUM VOLTAGE RESULT             |                      |              |            |
|-------------------------------------------------|----------------------|--------------|------------|
| VERSION = 390                                   |                      |              |            |
| BINARY FILE = ../diff_irdrop.emirtap.emir0_bin  |                      |              |            |
| RESULTS FILE CREATED = Sat Dec 19 03:16:49 2015 |                      |              |            |
| USER SUPPLIED VALUES:                           |                      |              |            |
| RESULTS TYPE                                    | =                    |              |            |
| TRANSIENT START                                 | = 1.76e-09           |              |            |
| TRANSIENT STOP                                  | = 2.111e-09          |              |            |
| Power_net_name                                  | R2rvmin_value<br>(V) | R2rvmin@time | Layer_name |
| VDD                                             | 857.333m             | 581.859p     | N/A        |
| OR                                              |                      |              |            |
| VDD                                             | 857.568m             | 581.859p     | m1_a       |

The `r2rvmin` feature allows you to apply the analysis only to selected layers, selected tap devices, tap devices of a user-defined model, and selected bounding boxes. Combinations are supported and combined with the AND behavior. Excluding tap nodes based on their layer, model, or instance information is also supported. To differentiate between multiple `r2rvmin` reports, you can apply the rule names to each `r2rvmin` statement (`r2rvmin_rule_name`). Refer to the `r2rvmin` option in the table under the [EMIR Control File](#) section for more information. The differential (rail-to-rail) IR drop analysis is only supported in the direct method.

## Static EMIR Analysis

Static EMIR analysis enables you to evaluate IR drop and EM currents based on the specified current consumptions for subcircuit instances without running a transient or DC simulation. The specified currents are distributed to the tap devices based on the width and length ratios of devices in the design. The IR drop and EM current analysis is performed based on the current at each tap device.

To enable static EMIR analysis, you need to use the `static ifile` option in the EMIR configuration file, as shown below.



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```
net name=[I1.VDD I1.VSS] analysis=[vavg iavg]
static ifile="static_currents.txt"
```

For static EMIR analysis, `vmax` and `vavg` for IR drop and `imax`, `irms`, and `iavg` values for EM currents remain the same, and therefore, just one can be selected in the statement.

The subcircuit instance currents are defined (in A) in the `static_currents.txt` file with the subcircuit instance name, subcircuit port name, and the current flowing in the port. This current is distributed to all MOSFET tap devices. No current distribution is done for non-MOSFET tap devices. In that case, these devices are excluded from the block-level based current distribution. The following is an example of the file:

```
I1 VDD 0.001
I1.I2 VDD 0.005
I1.I2/I3 VDD 0.000001
I1.I2.I3/I4 VDD 0.000005
I1 VSS -0.005
I1.MPM1@19 VDD 0 //exclude tap device from current assignment
I1.MPM3@15 VDD 0.0001 //define tap device current,exclude from current
 assignment
x0.QQ0 VSS 0.1 b //define current for non-MOSFET device and terminal
```

The accuracy of static EMIR analysis strongly depends on the detailed current information provided in `static_ifile`. Therefore, it is highly recommended to provide the current consumption for every subcircuit instance.

The results of static EMIR analysis are written to the same IR drop and EM current text reports, and into the same EM binary database as dynamic EMIR analysis.

**Note:** Only one of static or dynamic EMIR analysis can be performed from the same simulation session, and not both. When you run an static EMIR analysis, all other Spectre analyses, such as `dc` and `tran` are ignored.

Static EMIR analysis can also be applied to designs with power gates. For this, you need to specify the `pwrgate` option, as follows:

```
net name=[I1.VDD] analysis=[vavg iavg]
static ifile="static_currents.txt"
net pwrgate=[I1.VDD I1.VDD_INT] analysis=[vavg iavg]
```

You need to specify the power gate current in the `static_currents.txt` file, as shown below.

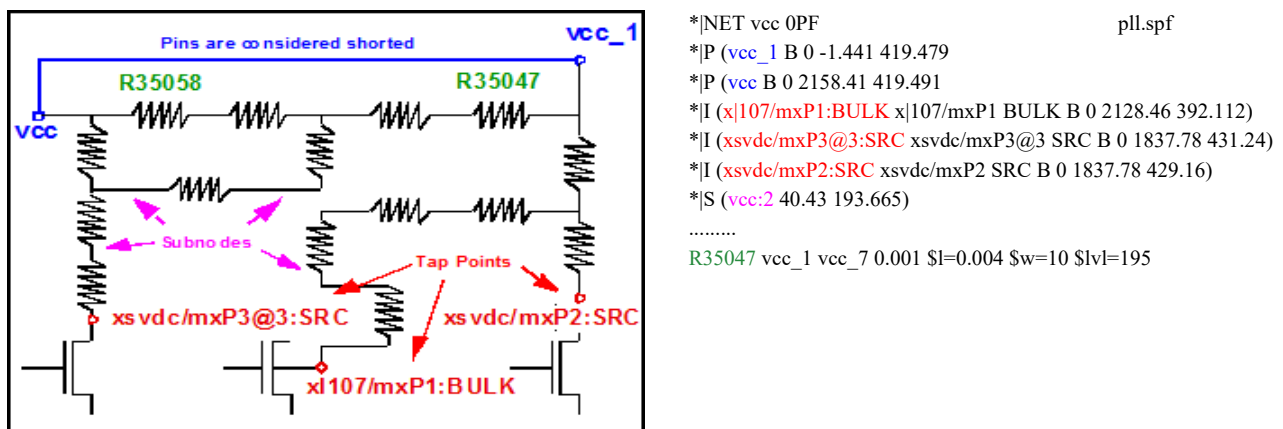
```
I1 VDD 0.001
I1 VDD_INT 0.0005
```

The static EMIR current file for the top-level EMIR subcircuit can be generated while running a dynamic EMIR analysis by using the `output=power` option in the time window statement.

## Static Power Grid Solver

Static Power Grid Solver (SPGS) can be used to calculate pin-to-tap resistances based on the description of a DSPF file and the options set in a EMIR configuration file. The resistances calculated by SPGS are electrically-equivalent resistances, and not the summation of resistors. The calculation assumes that all pins are connected together to form a global pin. After calculation, the resistance between the global pin and all taps is generated and listed based on the significance of their values.

The definition of pin, subnodes, and tap nodes is given in the DSPF file, as shown below:



The static EMIR analysis is enabled with the `spgs net=...` statement in the EMIR configuration file. The net statement defines the power nets to be analyzed.

```

spgs net=[i1.vcc i1.vss]
spgs pwrgate = [i1.vcc i1.outp]
spgs maxrpt=200
spgs filter_res_threshold=50

```

If the power net contains a power gate, then the `pwrgate` option needs to be specified. You can optionally use the `rshort` option to short the resistors in the power net based on their resistor value. In addition, the report can be limited to the top 200 paths, and any path with less than 50 Ohms can be filtered out.

The SPGS flow requires the DSPF file to be included in the Spectre input file with the `dspf_include` statement, as shown below.

```
dspf_include "pll.spf"
```

The power nets need to be connected to the voltage sources, and the device models need to be defined for the devices in the instance section in the DSPF file. The SPGS feature is run as in the regular EMIR flow, as follows.

```
spectre +aps input.scs +emir=spgs.conf
```

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The SPGS report provides a list of pin-to-tap node resistors ordered from highest to lowest. The W/L column either show the MOSFET W/L ratio or the NFIN/L ratio.

| Count | R         | W/L   | (x:y)      | (x:y) in GDSII | name            |
|-------|-----------|-------|------------|----------------|-----------------|
| #1    | 1920.2579 | 5.00  | (1440:366) | (1440:366)     | xI107/mxP1:BULK |
| #2    | 1577.1482 | 10.00 | (1440:476) | (1440:476)     | xsvdc/mxP3@3    |
| #3    | 1353.6123 | 4.00  | (1440:509) | (1440:509)     | xsvdc/mxP2:SRC  |

**Note:** It is recommended to run the SPGS feature separately and not together with any other EMIR analysis.

SPGS also supports the conversion between pin, tap node, and sub node. The following statements convert tap node MPM3@44:s of net I1.vdd to a pin, and sub node VDD:5 to a tap node.

```
spgs tap2pin net=[i1.vdd] include=[MPM3@44:s]
spgs sub2tap net=[i1.vdd] include=[VDD:5]
```

All conversion options are described in the EMIR configuration file option table. The conversion options are processed incrementally. This enables you to first move all tap nodes to subnodes, and to move nodes of interest back to tap nodes.

```
spgs tap2sub net=[i1.VSS] include=[VSS:*]
spgs sub2tap net=[i1.VSS] include=[VSS:82305002 VSS:63148225]
```

SPGS can be applied to signal nets. If the signal net contains a pin definition (\* | P), then the effective resistance is calculated starting from the pin. If the signal net does not contain any pin definition, then the resistance calculation is started from the first tap device connection (\* | I) for this net in the DSPF file. The conversion options also apply to signal nets.

By default, the SPGS flow requires the full EMIR simulation setup including the DSPF file, device models, stimuli, and power supply definitions. A higher performance simplified SPGS flow is available which just requires the DSPF file in addition to either an instance call of the DSPF subcircuit, or a +top option using the DSPF subcircuit name. The simplified flow does not require any device models, stimuli, or power supply definitions. It can be enabled with the following option:

```
spgs test_bench_less=1
```

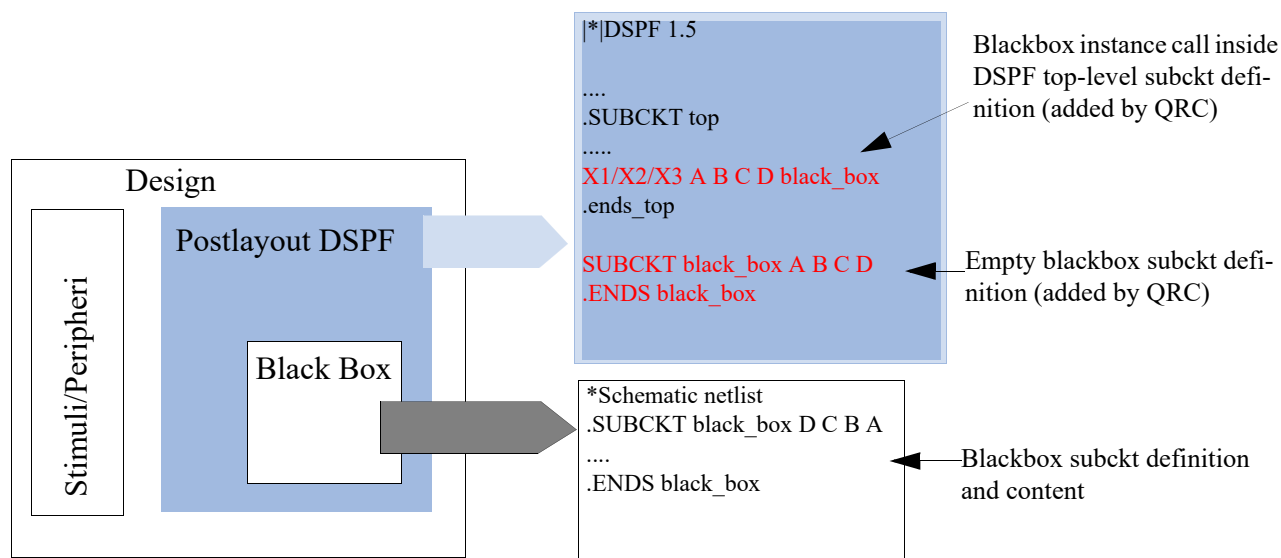
**Note:** The simplified SPGS flow has the limitation that it cannot be applied to designs with power gates. For such requirements, you need to use the full SPGS flow.

By default, the SPGS flow solves nets in parallel (`emirutil rcsolve_multi_proc=on`). Individual nets are solved, either with single thread (small nets), or with multi-thread (large nets).

## Advanced EMIR Features

### Blackbox Handling

The Spectre EMIR flow supports the blackbox approach, which allows the exclusion of blocks from parasitic extraction and EMIR analysis. These blocks are represented in the simulation with a pre-layout netlist, and have only an instance call and an empty subcircuit definition in the DSPF netlist.



Blackbox handling is enabled by specifying the subcircuit name after the `blackbox` keyword in the `dspf_include` statement, as shown below.

```
.dspf_include "top.spf" ... blackbox="black_box"
```

For the blackbox subcircuit instances, Spectre takes the port order from the DSPF subcircuit definition, and the content from the schematic (`blackbox`) subcircuit definition. This behavior is fixed. The `port_order` option of the `dspf_include` statement has no impact on the blackbox port order.

**Note:** You can specify multiple subcircuits. The `extra_port` option also applies to the blackbox subcircuit ports.

## Creating Power Macro Models

Spectre supports the creation of power macro models that can be used in the Spectre EMIR blackbox simulation flow. These macro models describe the subcircuit port current consumption and capacitive load. They are created in Spectre language and use the subcircuit definition. The macro model creation can be enabled either in a non-EMIR Spectre simulation, or in an Spectre EMIR simulation. Both dc and tran analyses are supported.

To create macro models, use the `pwr_macro` statement, as follows:

```
pwr_macro subckt=top port=[vdd X<0>] type=[avg rms] outdir=macrodir mode=1
pwr_macro inst=i1 port=[*] type=[max] outname=macro output=[subckt table]
window=[10n 20n 80n 100n]
```

Where:

`subckt` - specifies that the macro model is created for all instances of this subcircuit.

`inst` - specifies that the macro model is created for the specified subcircuit instance.

`port` - specifies the subcircuit ports that are modeled. Wildcards are supported.

`type` - specifies the type of current measurement for defining the created port current DC source value. Supported values are `max`, `avg`, `avgabs`, and `rms`. Multiple entries are supported.

`output` - specifies the output to be created. If you specify `output=subckt`, then the subcircuit macro model is created. This is the default. If you specify `output=table`, then a port current/capacitance table is created.

`outdir` - specifies the output directory name (relative to simulation directory).

`outname` - specifies the macro model file name. The file has an extension `.inst_name.subckt_name.type`

`mode` - `mode=1` creates the macro model with what/if for separate pull and push currents. This is the default. `mode=0` creates the macro model with parallel resistors.

`window` - defines the time window for which the macro model is created. Multiple time windows are supported. One model is created for each time window. The first window has no additional extension. The second window uses 1 as additional extension, the third window uses 2, and so on. For example, `*.1.avg`, `*.2.avg`, and so on.

To create a power macro model in a regular (non-EMIR) Spectre simulation, the `pwr_macro` statements need to be defined in a configuration file which is read with the Spectre `+pwr_macro` command-line option. This flow also works in the Spectre EMIR flow.

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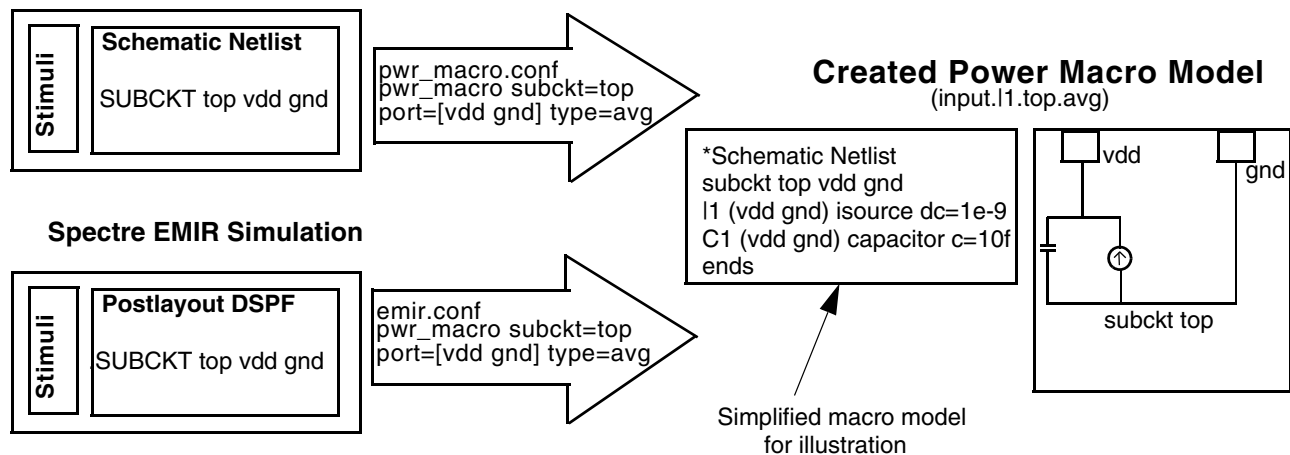
```
spectre +aps +pwr_macro=pwr_macro.conf input.ckt
```

In addition, you can create the macro model in a Spectre EMIR simulation as part of EMIR configuration. In this case, the `pwr_macro` statements need to be defined in the EMIR configuration file which is included with the `+emir` command-line option.

```
spectre +aps +emir=emir.conf input.ckt
```

The following figure illustrates the macro modeling generation flow. Note that the figure shows only a simplified version of the model.

## Spectre non-EMIR Simulation (OR)



The created macro table model is written to a file for which the extension consists of the instance name, the subcircuit name, and the type of analysis of the subcircuit block. If multiple analyses are specified, multiple macro model files are created. For example, for a macro model for instance `I1` of subcircuit `adc_sample_hold`, based on average current, the extension `.I1.adc_sample_hold.avg` will be used.

Macro models are generated in a regular (non-EMIR) simulation, direct EMIR analysis, and also in the first and second stages (extra `emirtap` in extension) of the iterated EMIR analysis.

The macro model created is slightly more complex than what is shown in the simplified figure above. Since the model is later used together with other macro models in a full chip simulation, there may be a problem that some of these models feed currents into the same net, but the sum of the currents does not satisfy Kirchhoff's law. To resolve such problems, the `mode=1` macro model contains if/else sections that allow you to enable either driving (push) or driven (pull) currents. The following example shows a `mode=1` macro model for a subcircuit for which `vdd` and `gnd` have been extracted:

```
// TITLE: Port Current Macro Model with Push and Pull Mode for subckt
adc_sample_hold
```

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```
simulator lang=spectre
// BB_MACRO_TOP PARAMETER DEFINITION
// 0 ... consider push and pull currents, may cause potential KCL problems
// 1 ... consider pull currents only (positive port current value)
// 2 ... consider push currents only (negative port current value)
// R_BB_MACRO_TOP defines internal serial resistor
// parameters bb_macro_top=0 r_bb_macro_top=10
subckt adc_sample_hold outm outp SIDDQ VDD VSS \
 bias100 hold hold_test inm inm_test inp \
 inp_test sample sample_test
parameters bb_macro=bb_macro_top r_bb_macro=r_bb_macro_top
wrongValue paramtest errorif=(bb_macro != 0 && bb_macro != 1 && bb_macro != 2)
message="Unvalid bb_macro parameter value, valid values: 0, 1, 2"
// SIMULATION OF PULL AND PUSH PORT CURRENTS
if (bb_macro==0) {
 Rport0 (VDD VDD_int) resistor r=r_bb_macro
 Iport0 (VDD_int 0) isource dc=0.00153621
 Cport0 (VDD 0) capacitor c=8.39577e-12
 Rport1 (VSS VSS_int) resistor r=r_bb_macro
 Iport1 (VSS_int 0) isource dc=-0.00160214
 Cport1 (VSS 0) capacitor c=1.14779e-12

// SIMULATION OF PULL PORT CURRENTS ONLY
} elseif (bb_macro==1) {
 Rport0 (VDD VDD_int) resistor r=r_bb_macro
 Iport0 (VDD_int 0) isource dc=0.00153621
 Cport0 (VDD 0) capacitor c=8.39577e-12
 Rport1 (VSS VSS_int) resistor r=r_bb_macro
 Vport1 (VSS_int 0) vsource dc=0

// SIMULATION OF PUSH PORT CURRENTS ONLY
} elseif (bb_macro==2) {
 Rport0 (VDD VDD_int) resistor r=r_bb_macro
 Vport0 (VDD_int 0) vsource dc=0
 Rport1 (VSS VSS_int) resistor r=r_bb_macro
 Iport1 (VSS_int 0) isource dc=-0.00160214
 Cport1 (VSS 0) capacitor c=1.14779e-12
}
ends adc_sample_hold
```

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You can specify the option `bb_macro_top` in your top-level netlist, and also specify which macro model mode to use. If `bb_macro_top` is set to 0, all macro model port currents are activated. If `bb_macro_top` is set to 1, only pull currents are modeled. If `bb_macro_top` is set to 2, only push currents are considered. In addition, the value of serial resistor `r_bb_macro_top` for the current and voltage sources in the macro model needs to be defined at the top level.

The alternative `mode=0` macro model overcomes the potential KCL problem by adding a parallel resistor. The value of the parallel resistor and the voltage are extracted from the simulation during which the model is generated. The following example shows the `mode=0` macro model for the same subcircuit.

```
simulator lang=spectre
pwr_macro_opt options preserve_subckt=[adc_sample_hold]
subckt adc_sample_hold outm outp SIDDQ VDD VSS \
 bias100 hold hold_test inm inm_test inp \
 inp_test sample sample_test
parameters vavg_VDD=2.5 rmacro_VDD=32.8738
Iport0 (VDD 0) isource dc=0.0015325 - vavg_VDD/rmacro_VDD
Cport0 (VDD 0) capacitor c=8.39538e-12
Rport0 (VDD 0) resistor r=rmacro_VDD
parameters vavg_VSS=0 rmacro_VSS=216.051
Iport1 (VSS 0) isource dc=-0.00158744 - vavg_VSS/rmacro_VSS
Cport1 (VSS 0) capacitor c=1.14816e-12
Rport1 (VSS 0) resistor r=rmacro_VSS
ends adc_sample_hold
```

In addition to the macro models, you can also generate a table with port current and capacitance values. The values are written to a file with the extension `rpt_pwr_macro`.

-----INST: "I1" SUBCKT "adc\_sample\_hold"-----

| Port | I <sub>max</sub> (A) | I <sub>avg</sub> (A) | I <sub>avgabs</sub> (A) | I <sub>rms</sub> (A) | C <sub>max</sub> (F) | C <sub>avg</sub> (F) | C <sub>avgabs</sub> (F) | C <sub>rms</sub> (F) |
|------|----------------------|----------------------|-------------------------|----------------------|----------------------|----------------------|-------------------------|----------------------|
| VDD  | 0.00315119           | 0.00285237           | 0.00285237              | 0.00285231           | 8.55353e-12          | 8.54216e-12          | 8.542162e-12            | 8.54216e-12          |
| VSS  | -0.00364904          | -0.00299747          | 0.00299747              | 0.00301076           | 1.38952e-12          | 1.38169e-12          | 1.38169e-12             | 1.38169e-12          |
| ...  |                      |                      |                         |                      |                      |                      |                         |                      |

If the above table exists from a previous simulation, and the table contains all ports of the extracted subcircuit, you can use the following script to create a power macro model using the information from the table:

```
tbl2macro test.rpt_pwr_macro -inst I2.I1 -type avg -outdir test_pwr_macro
tbl2macro test.rpt_pwr_macro -subckt bus_nand -type avg rms
```



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The script is available in the SPECTRE installation (`.../tools.lnx86/bin/tbl2macro`), and can be used as follows:

```
tbl2macro <rpt_pwr_macro> [options]
```

`-h` - Print the help page

`-inst <inst_name>` - Name of the instance (OR)

`-subckt <subckt_name>` - Name of the subcircuit

`-out <out_dir>` - Name of the output directory name (default is .)

`-type <list>` -- List of max, avg, avgabs, and rms (default is all)

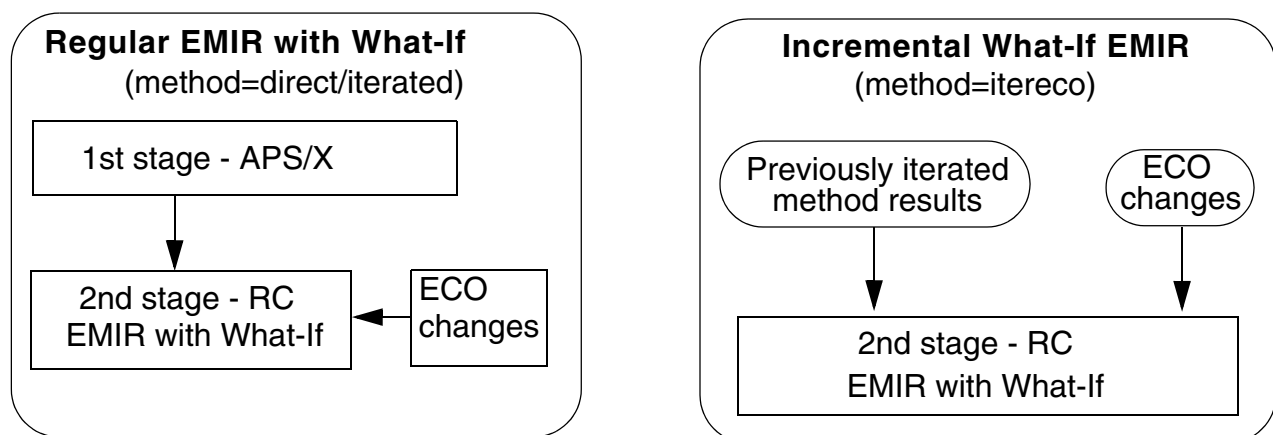
`-fmt <spice|spectre>` -- Output format (default is spectre)

`-mode <0|1>` - 0 means parallel resistor model, and 1 means what/if push-and-pull model (default is 1)

### What-If EMIR Analysis

The What-If analysis enables you to analyze the impact of the potential layout changes without the need for implementing these changes in the layout, and to re-extract the DSPF file. These changes are also called ECO changes.

The What-If flow is supported in the regular EMIR flow using the direct or iterated method. There is also an incremental iterated flow that uses the `itereco` method. This flow reuses the circuit simulation results from a previous iterated mode EMIR analysis and reruns just the second stage EMIR analysis.



The What-If changes are defined in an ECO file which is included in the EMIR configuration file. All ECO changes are relative to the original DSPF content. In one What-If simulation, all changes defined in the ECO file are applied together at once, and then analyzed together in the second stage of the EMIR analysis.

Multiple incremental ECO runs are supported. For each run, the changes defined in the ECO file are applied to the original DSPF content. Changes from the previous ECO runs are not considered. In the incremental What-If analysis, only the nets with the ECO changes are analyzed.

All ECO changes for a specific What-If run are defined in one ECO file which is included in the EMIR configuration file. The following ECO commands are supported.

- `add_pin net=<net_name> name=[node1 node2 ...]`
- `add_pin net=<net_name> layer=[dspf_layer_name]`
- `delete_pin net=<net_name> name=[node1 node2 ...]`
- `add_cap net=<net_name> cap=[node1 cvalue1 node2 cvalue2 ...]`
- `add_res net=<net_name> node=<node1 node2> r=<rvalue> (optional: $L, $W, $A, $N,$lv1)`
- `delete_res net=<net_name> name=<resistor1 resistor2 ...>`
- `scale_res net=<net_name> name=<resistor1 resistor2 ... > scale=<scalefactor>`

Here:

`net_name` is the name of the net as defined in DSPF \*|`net` statement. Wildcard is not supported.

`node1 node2 ...` are the names of pin, sub, or tap nodes. Wildcard is not supported.

`cvalue1 cvalue2..` are the values of the capacitance to be added. You can use a negative value for reducing net capacitance. The value is a floating number.

`rvalue` is the value of the resistor to be added. The value is a floating number

`resistor1 resistor2...` are the instance names of the resistors to be deleted or scaled.

`scalefactor` is the scaling factor. The value is a floating number

`dspf_layer_name` specifies that the nodes of all resistors on the specified layer are changed to pins.

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The following is an example of an `emir.co` file:

```
add_pin net=[VDD] name=[VDD#9]
del_res net=[bias1] name=[Rj3652]
scale_res net=[VDD] name=[Rg1 Rg2 Rg3 Rg4] scale=0.5
delete_res net=[VDD] name=[Rg5]
add_res net=[VDD] node=[VDD#80 VDD#81] r=10 $l=10.0 $w=0.25 $lvl=mt1
add_cap net=[VDD] cap=[VDD#80 10e-15 VDD#81 5e-15]
```

When performing a regular iterated method EMIR analysis with What-If, the only change required in the EMIR configuration file is the reference to the ECO file, as shown below.

```
solver method=iterated
eco file="emir.eco"
```

The following statements need to be defined in the EMIR configuration file to enable an incremental What-If EMIR analysis.

```
solver method=itereco inputwf="./input.emirtap.pwl"
eco file="emir.eco"
```

In an incremental EMIR analysis, Spectre loads the following database files from the previous EMIR simulation: `<netlist>.emirtap.pdb`, `<netlist>.emirtap.cc`, `<netlist>.emirtap.pdb_2`, and `<netlist>.emirtap.pwl`. You need to ensure that these files are available in the same directory as the `<netlist>.emirtap.pwl` file that you define in the solver statement.

All ECO changes are summarized in the `ECO SUMMARY` section of the Spectre log file. The What-If EMIR flow generates exactly the same text and binary database output as any other Spectre EMIR simulation. The only difference is that the result file names of the incremental What-If analyses use the filename of the ECO file as prefix. For example, if the ECO file name is `emir.eco`, then the EM current text report file will be named `emir.eco.input.rpt_em`.

The Spectre What-If EMIR flow also supports a pin location file for changing subnodes to pins. This special flow is important when all subnodes in a user-specified layout area should be changed to pins. The following statements can be used in the ECO file for defining the pin location files:

```
add_pin net=VDD loc_file=pinloc loc_threshold=0.1
add_pin net=VSS loc_file=pinloc_vss loc_threshold=0.1
```

The `net` statement defines the DSPF net to which the pin location file is applied to, while the `loc_threshold`  $\Delta$  (unit  $\mu\text{m}$ , default value 0.1) defines the area in which all subnodes are changed to pin. The area is defined with:  $x - \Delta < x < x + \Delta$ ,  $y - \Delta < y < y + \Delta$ .

The pin location files define the x and y coordinates, the layer name, and whether the type is POWER or GROUND. Following is an example of the pin location file for power net VDD:

```
#<pad_name> <X_loc> <Y_loc> <metal name-DEF> <POWER or GROUND>
VDD:2 30.0 103.0 mt3 POWER
```

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```
VDD:3 20.2150 94.2250 mt1 POWER
```

Following is an example of the pin location file for the ground net VSS:

```
#<pad_name> <X_loc> <Y_loc> <metal name-DEF> <POWER or GROUND>
VSS:2 15.6000 27.9600 mt1 GROUND
```

Alternatively, all subnodes inside a bounding box may be changed to pins. This can be done by using the following option:

```
add_pin net=VDD bbox=[lx ly ux uy] layer=[dspf_layer_name]
```

For example:

```
add_pin net=I1.VDD bbox=[20 80 22 86] layer=[mt1]
```

An incremental pin addition is also supported. From a reference node  $[x, y]$  incrementally add/subtract  $\Delta x / \Delta y$ , check for any sub node on the grid within the proximity, and change the identified sub node to a pin. If no reference node is defined, all pins are used as reference node.

```
add_pin net=VDD layer=metal5 ref_node=[x y] h_x=value h_y=value
proxim_abstol=value
```

For example:

```
add_pin net=inm layer=mt3 ref_node=[105.0 105.0] h_x=8.0 h_y=-6.0 proxim_abstol=1
```

## Event Triggered EMIR Analysis

Spectre EMIR enables you to control the EMIR time windows in the second stage of iterated method by first stage events. A measure statement may be used to define the first stage events, as shown below.

```
.meas tran blkout3 when v(TEST_INP)='vhi/2.0' td=30n fall=1
.meas tran blkout4 param='blkout3+20n'
```

The created events can be used to define the time windows in the EMIR config file, as shown below.

```
time window=[@blkout3 @blkout4] net=[I101.VDD] output=none
```

If an event is used but not available at the time of evaluation, Spectre EMIR generates an error and the simulation is stopped.

## Other Features

- EMIR analysis is performed not only for transient but also for operating point and DC analysis. All measures (for example, avg, rms, and max) are analyzed the same way as in the transient EMIR analysis. This is available for both Spectre APS direct and Spectre

APS iterated methods. If EMIR analysis is applied to a combined DC and transient analysis, it is applied to both.

- Probing of parasitic element currents, and parasitic node voltages is supported.
- Negative resistors in the power and signal nets are properly handled without shorting or removing them.
- `alter` and `altergroup` statements are supported when using the direct method. For each `alter` and `altergroup` statements, the EMIR analysis is invoked automatically and generates EMIR reports named `input_tran1.rpt_ir`, `input_tran2.rpt_ir` and so on.
- The EMIR flow supports temperature-dependent resistor definitions (TC1, TC2) in the DSPF file

```
RRM14 a#1 a#12 0.516195 TC1=0.00265 TC2=-2.641e-07 ...
```

The effective resistor value is calculated using the following equation:

$$R = R_{NOM} * (1 + TC1 * (TEMP - TNOM) + TC2 * (TEMP - TNOM) (TEMP - TNOM))$$

If TNOM is defined in the DSPF file header with the following statement

```
*|GLOBAL_TEMPERATURE 27
```

then TNOM is taken from the DSPF file, otherwise TNOM is taken from the Spectre netlist. TEMP is taken either from `dspf_include` statement

```
dspf_include "./test.dspf" temp=100
```

or from the TEMP statement in the Spectre netlist.

The DSPF TNOM and the `dspf_include` TEMP statement impact only the effective DSPF resistor calculation. They do not affect any other Spectre temperature dependency.

- The EMIR flow supports simple triple resistor DSPF definitions.

Example:

```
*|NET C1_B 'C1*3.93132e-15+C2*3.86269e-15+C3*4.17145e-15' CA1 C1_B 0
'C1*1.97013e-16+C2*1.90427e-16+C3*2.08892e-16' $lv1=2 Ro 1 1 C1_B:81 C1_B:82
'C1*63.220882+C2*74.936630+C3*53.778004' $M2 $L=5.569 $W=0.06
```

**Note:** Only the above format is support. More complex equations are not supported.

The parameters C1, C2 and C3 need to be defined on the `dspf_include` line. They cannot be defined in the regular Spectre netlist.

```
dspf_include "./test.dspf" param="C1=1 C2=0 C3=0"
```

- The EMIR flow supports temperature-dependent EM rules. It reads the circuit temperature from the netlist statement, and applies it to the EM rules.

- ❑ `temperature` is a predefined keyword in the `emData` file. It may be used in equations to represent the circuit temperature.
  - ❑ If `temperature` is defined in the `emData` file, and it does not match the `temperature` (`temp` value) in the netlist, an error message is generated.
  - ❑ If `temperature` is not defined in the `emData` file, the tool uses the temperature defined in the netlist.
- The Spectre EMIR flow can handle inductor elements in both direct and iterated methods. Direct method supports all inductor elements. In iterated method, design inductors are handled in the first stage; inductors inside subcircuit tap devices are handled using their current waveforms from the first stage, package inductors connecting to DSPF subcircuit ports are solved together with the net in the second stage solver, and parasitic inductors (not typical for DSPF) are handled by the second stage solver.

## **Spectre EMIR Analysis Using Voltus-XFi**

Voltus-XFi Custom Power Integrity Solution is used for transistor-level power and signal integrity analysis, which includes multi-mode simulation for EM and IR analysis. This solution combines Cadence® Quantus™ RC extraction, Spectre EMIR simulation, and Voltus-XFi visualization in the Cadence Virtuoso® platform. This combination of products simplifies the use model of the flow by using a common setup for all the tools. You do not have to run the flow in separate steps.

The Spectre EMIR Voltus-XFi solution provides two major enhancements over Spectre EMIR Voltus-Fi:

- Simplified use model for the iteration method
- Enhanced distribution of EMIR analysis

### **Simplified Use Model for the Iteration Method**

The Spectre EMIR setup with Voltus-Fi requires you to set up options in the first and second stages of the iteration method to optimize the accuracy and performance of simulation.

However, in the Spectre EMIR Voltus-XFi solution, the `+emirpreset` command-line option simplifies the EMIR use model. This option predefines all first- and second-stage EMIR settings. This technology works only with the Spectre X solver.

Similar to the Spectre X technology, the value of the `+emirpreset` option can be `cx`, `ax`, `mx`, `lx`, and `vx`, where `cx` is the most conservative setting and `vx` is the setting for highest performance.

```
spectre +preset=ax +emirpreset=mx input.scs +emir=iterated.conf
```

The `+emirpreset` option internally sets the `solver rcr` and `solver rcsolve_multi_proc` settings. Therefore, when `+emirpreset` is set to enable the solution, Spectre ignores the following settings specified in the EMIR config file:

```
solver rcr=...
solver rcsolve_multi_proc=...
```

**Note:** Advanced users can set individual EMIR solver settings in the EMIR config file and give preference to them over `+emirpreset` by using the `-emirpreset_override` option on the Spectre command line, as shown below.

```
spectre +preset=ax +emirpreset=mx input.scs +emir=iterated.conf
-emirpreset_override
```

When running the direct EMIR method, as shown below, the use model, performance, and accuracy of Spectre EMIR Voltus-XFi solution is same as that of Spectre EMIR Voltus-Fi.

```
spectre +preset=ax input.scs +emir=direct.conf
```

## Enhanced Distribution of EMIR Analysis

In the second stage of the iterated EMIR simulation, typically a few large power nets and a large set of smaller signal nets are solved individually.

The Spectre EMIR Voltus-XFi solution provides an enhanced mechanism to distribute RC net solving to multiple computers. This feature is based on the XPDB database solution. It optimizes the performance in the second stage.

To enable distribution of net solving to multiple computers:

1. Create the XPDB database by using the `-dump_xpdb` option of the `spfchecker` command.

The following example creates the `adc_sample_hold.dspf.xpdb` file:

```
spfchecker -dump_xpdb adc_sample_hold.dspf
```

2. Specify that you need to use the XPDB database created in step 1.

You can do this in two ways:

- ❑ Run Spectre by using the `+xpdb` command-line option to enable the use of the `.xpdb` file.

```
spectre +aps +xpdb adc_sample_hold.scs +emir=adc_sample_hold.conf
```

- ❑ Use the `dspf_include` command to include the XPDB database.

```
dspf_include "adc_sample_hold.dspf.xpdb"
```

If you use the `dspf_include` command, you do not need to specify the `+xpdb` in the command line.

3. (Optional) Use the `+mp` and `+mt` command-line options to specify the number of processes and the number of cores per job. The individual RC net solving processes are managed by a scheduler that is launched by the master process.

```
spectre +mp=N +mt=M +preset=ax +emirpreset=mx input.scs +emir=iterated.conf +xpdb
```

The following example distributes jobs using `rsh` to run 4 processes with 16 threads each on `hostA` and `hostB`:

```
spectre +mp=rsh +mt=16 +hosts "hostA:1 hostB:2" +preset=ax ...
```

The main process on `hostA` is not defined because it is automatically assigned.



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You can distribute jobs on an LSF farm by using the `bsub` command, as shown below.

```
"bsub -n 16 <other_bsub_params> "spectre +mp=4 +mt=16 +preset=ax ..."
```

## **Parasitic Backannotation of DSPF/SPEF/DPF Files**

This section covers the following topics:

- [Postlayout Simulation Methodologies](#) on page 894
- [Control Options for Parasitic Backannotation Flow](#) on page 896
- [Parasitic Backannotation Report](#) on page 921
- [Some Common Error and Warning Messages Related to Parasitic Backannotation](#) on page 922

### **Postlayout Simulation Methodologies**

In general, there are three postlayout simulation methodologies:

- **Flat RC Netlist File**

A flat netlist containing a large number of elements and devices. For example, the netlist from Quantus QRC extracted view, which is often used in ADE.

- **Hierarchical RC Netlist File**

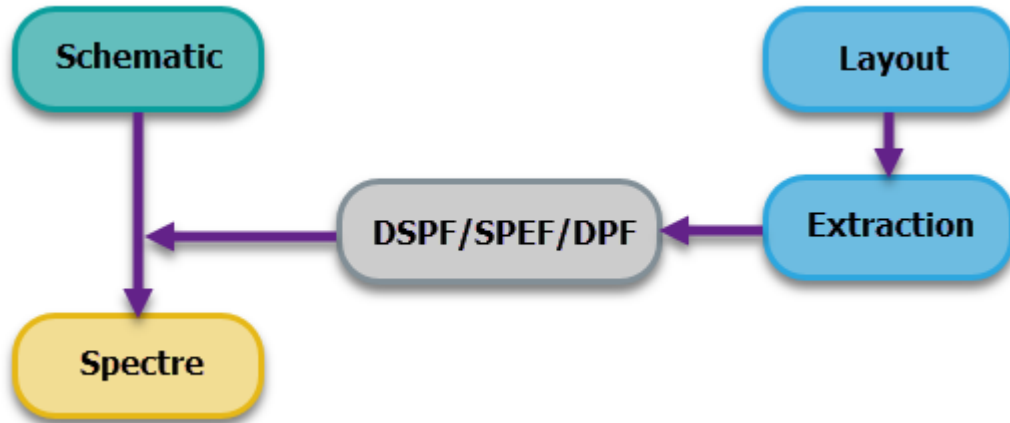
A netlist file that contains a hierarchy of extracted subcircuits.

- **Backannotation of Parasitic Files**

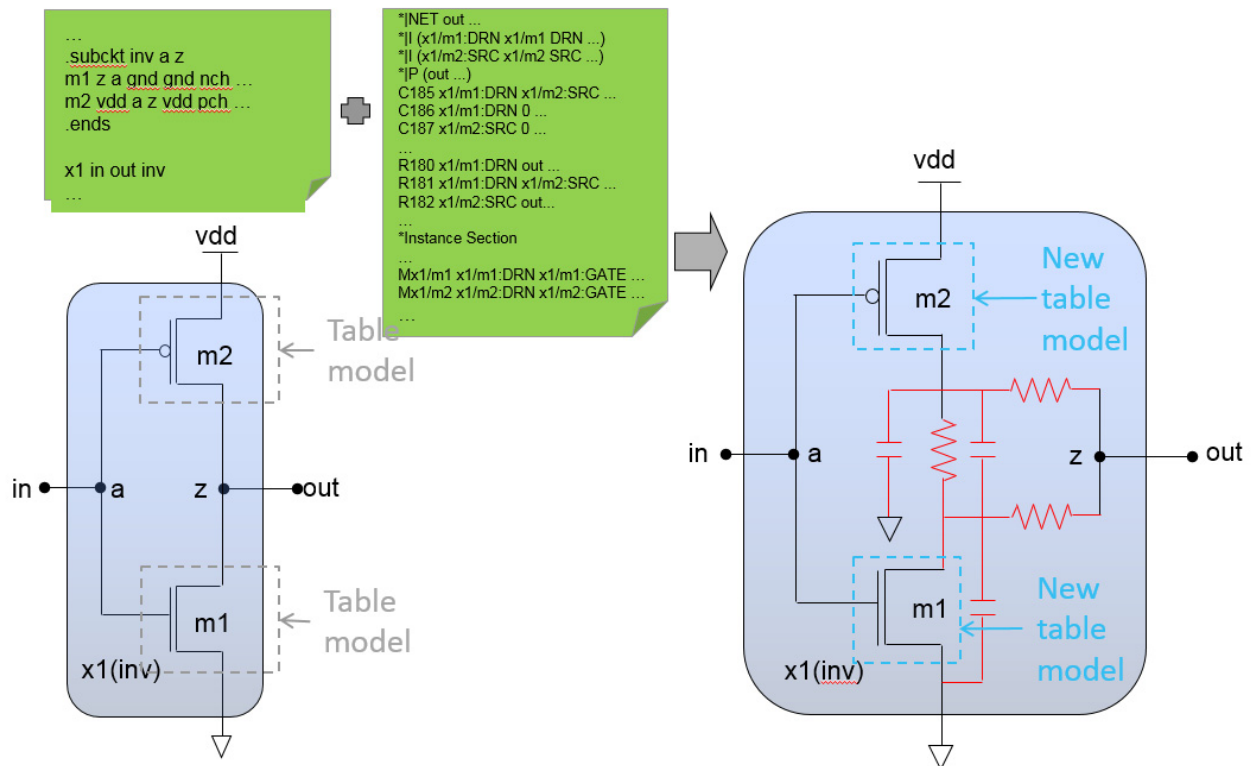
DSPF/SPEF/DPF files containing parasitic information. This methodology combines the parasitic information with the pre-layout netlist through backannotation. It enables Spectre to automatically plug in the parasitic elements during simulation. Compared to the flat and hierarchical RC netlist methodologies, the backannotation methodology has the following benefits:

- ☐ It provides the ability to reuse the pre-layout simulation test-bench. There is no need to change the test-bench setup, save Ocean measurements, and so on.
- ☐ It can perform What-if analysis using selective backannotation.

The following figure shows the backannotation flow:



## Parasitic Backannotation - Concept



The simulation database is built upon the pre-layout netlist, as shown in the left of the figure. The parasitics from the parasitic files (DSPF/SPEF/DPF) are backannotated into the database, as shown in the right. The hierarchy and the net names from the pre-layout netlist are retained, and the device models are regenerated according to device parasitic information (DPF/Instance Section from the SPF). The nodes are backannotated with R and C from the SPEF/SPF `Net` section.

### Control Options for Parasitic Backannotation Flow

The control options for the parasitic backannotation flow can be grouped under four categories:

- [Parasitic File Loading Options](#) on page 899
- [Parsing Options Used in Backannotation](#) on page 902
- [Selective Backannotation Options](#) on page 913
- [Backannotation Message Control Options](#) on page 918

**Note:** Unlike traditional simulation options, wherein if the same option is specified multiple times, the last one takes precedence, most backannotation options, when specified multiple times, accumulate the assigned values.

The following table provides a summary of the options:

| Category                       | Option Name | Syntax                | Description                                                                   |
|--------------------------------|-------------|-----------------------|-------------------------------------------------------------------------------|
| Parasitic File Loading Options | dpf         | dpf="scope filename"  | Specifies the name and scope of the DPF file that needs to be backannotated.  |
|                                | spf         | spf="scope filename"  | Specifies the name and scope of the SPF file that needs to be backannotated.  |
|                                | spef        | spef="scope filename" | Specifies the name and scope of the SPEF file that needs to be backannotated. |

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| Category               | Option Name        | Syntax                                                                                                             | Description                                                                                                                                                                                                    |
|------------------------|--------------------|--------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Parsing Options</b> | spfswapterm        | spfswapterm="terminal1 terminal2 subcktname"                                                                       | Specifies the terminals of the subcircuit macro-model that can be swapped.                                                                                                                                     |
|                        | spfxtorprefix      | spfxtorprefix="substring [replacement_substring]"                                                                  | Specifies the prefix for the device and net names in the DSPF/SPEF/DPF file.                                                                                                                                   |
|                        | spfaliasterm       | spfaliasterm="model   subckt prelayout_term1=spf_alias1 prelayout_term2=spf_alias2 ... prelayout_termN=spf_aliasN" | Specifies an alias for the terminal names of devices. This option is useful when the terminal names of devices in the DSPF/SPEF/DPF files are different from those in the simulation model library.            |
|                        | speftriplet        | speftriplet=1   2   3                                                                                              | Specifies which value from the triplet should be used for backannotation in the SPEF file. This option is effective only when the values in the SPEF file are represented as triplets. The default value is 2. |
|                        | spfrcr             | spfrcr=0   1                                                                                                       | Specifies whether RC reduction in parasitic backannotation should be enabled. The default value is 1.                                                                                                          |
|                        | spfrcrfmax         | spfrcrfmax=value                                                                                                   | Defines the maximum frequency for RC reduction performed during parasitic backannotation. The unit is in GHz. The default value is 25.                                                                         |
|                        | spfinstancesection | spfinstancesection=0   1                                                                                           | Controls the device parameter backannotation from the instance section of the DSPF file. The default value is 1.                                                                                               |

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| Category | Option Name            | Syntax                                           | Description                                                                                                                                                                                                                                                        |
|----------|------------------------|--------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          | spfbusdelim            | spfbusdelim="schematic_busdelim [DSPF_busdelim]" | Allows to map the bus delimiter between schematic and DSPF, SPEF, and cap file. The option defines the bus delimiter in the schematic netlist, and optionally the bus delimiter in the DSPF file. The default value is the bus delimiter taken from the DSPF file. |
|          | spfshortpin            | spfshortpin=yes no                               | Enables or disables the shorting of pins (* P) for the same net (* NET). The default value is yes.                                                                                                                                                                 |
|          | spfscale               | spfscale=value                                   | Sets the scaling factor of all instances in the parasitic file. The default value is 1.                                                                                                                                                                            |
|          | spfcaponly             | spfcaponly=0 1                                   | Specifies whether only capacitors should be backannotated (C-only stitching). The default value is 0.                                                                                                                                                              |
|          | spfreppin              | spfreppin=0 1 2 3                                | Specifies whether to choose the first instance pin, last instance pin, first instance pin after sorting, or the last instance pin after sorting as the representative node. The default value is 0.                                                                |
|          | spfrepgate             | spfrepgate=1                                     | Picks the first gate pin as representative node. If no gate pin exists, pin selection follows spfreppin. Default is 0 and pin selection follows spfreppin.<br><br>It can be used together with spfreppin, and has higher priority.                                 |
|          | sim_opt_probe_spf_node | sim_opt_probe_spf_node=0 1 2 3 4                 | Controls the probing of backannotated nodes. The default value is 0.                                                                                                                                                                                               |
|          | sim_opt_spf_probe_mode | sim_opt_spf_probe_mode=0 1                       | Controls the probe name for the SPF node.                                                                                                                                                                                                                          |
|          | spfhierdelim           | spfhierdelim=char                                | Changes the spf hierarchical delimiter. The default value is the hierarchical delimiter taken from the DSPF file header.                                                                                                                                           |
|          | dpfprefix              | dpfprefix="m r d x"                              | Backannotates all devices with M (mosfet), R (resistor), D (diode), and instance X.                                                                                                                                                                                |
|          |                        |                                                  |                                                                                                                                                                                                                                                                    |

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| Category                                      | Option Name        | Syntax                                          | Description                                                                                                                                                             |
|-----------------------------------------------|--------------------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Selective Backannotation Options</b>       | spfcnet            | spfcnet=[netname 1 netname2..]                  | Backannotates the total capacitance of the specified nets.                                                                                                              |
|                                               | spfcnetfile        | spfcnetfile=filename                            | Backannotates the total capacitance of the net specified in the given text file, which contains a list of C-only backannotated nets.                                    |
|                                               | spfrcnet           | spfrcnet=[netname 1 netname2..]                 | Specifies the name of the net to be backannotated with parasitic resistors and capacitors.                                                                              |
|                                               | spfrcnetfile       | spfrcnetfile=filename                           | Specifies a text file containing a list of RC backannotated nets.                                                                                                       |
|                                               | spfnetcmin         | spfnetcmin=value                                | Selects the nets for backannotation using the value of their total node capacitance.                                                                                    |
|                                               | spfskipnet         | spfskipnet=[netname 1 netname2..]               | Specifies the nets that need to be skipped for backannotation.                                                                                                          |
|                                               | spfskipnetfile     | spfskipnetfile=filename                         | Specifies the file containing a list of nets that need to be skipped for backannotation.                                                                                |
| <b>Backannotation Control Message Options</b> | spfmglimit         | spfmglimit='number [STITCH-ID_1] [STITCH-ID_2]' | Sets the maximum number of messages (message limit) for a specified message category identifier (STITCH-ID) to be printed in the .spfrpt file. The default value is 50. |
|                                               | spfprintlargercnet | spfprintlargercnet=value                        | Sets the threshold for large RC nets by specifying the number of resistors and capacitors in one net.                                                                   |

## Parasitic File Loading Options

- dpf
- spf
- spef

### *dpf*

### Syntax

#### *Spectre format*

name options dpf="scope filename"

## *SPICE format*

```
.options dpf="scope filename"
```

## Description

Specifies the DPF file that is to be backannotated and its scope. If you specify this option multiple times, all specified settings are considered.

## Arguments

|              |                                                                                                                                                                                                                                                                         |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>scope</i> | Specifies a subcircuit or an instance. When a subcircuit is specified, the DPF file is backannotated with all the instances of that subcircuit. When an instance is specified, the DPF file is backannotated with the specified instance only. Wildcards are supported. |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

|                 |                                                                                                                                                                                                                         |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>filename</i> | Specifies the name of the DPF file. Multiple DPF files can be specified for backannotation by using the option multiple times. If you specify a DSPF file, only the instance section of the DSPF file is backannotated. |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Example

### *Spectre format*

```
opt1 options dpf="X1.XPLL PLL.dpf" dpf="X1.XMEM mem.dpf"
```

### *SPICE format*

```
.options dpf="X1.XPLL PLL.dpf" dpf="X1.XMEM mem.dpf"
```

tells the simulator that the `PLL.dpf` file is to be backannotated into the `X1.XPLL` instance and `mem.dpf` file is to be backannotated into the `X1.XMEM` instance.

## *spf*

## Syntax

### *Spectre format*

```
name options spf="scope filename"
```

### *SPICE format*

```
.options spf="scope filename"
```



## Description

This option specifies the DSPF file that is to be backannotated and its scope. If you specify this option multiple times, all specified settings are considered.

## Arguments

|                 |                                                                                                                                                                                                                                                                       |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>scope</i>    | Specifies a subcircuit or an instance. When a subcircuit is specified, the DSPF file is backannotated to all the instances of that subcircuit. When an instance is specified, the DSPF file is backannotated to the specified instance only. Wildcards are supported. |
| <i>filename</i> | Specifies the name of the DSPF file. Multiple DSPF files can be specified for backannotation by using the option multiple times.                                                                                                                                      |

## Example

### *Spectre format*

```
opt1 options spf="mem mem.dspf"
```

### *SPICE format*

```
.options spf="mem mem.dspf"
```

tells the simulator to stitch `mem.dspf` to subcircuit `mem`.

## ***spef***

## Syntax

### *Spectre format*

```
name options spef=" scope filename"
```

### *SPICE format*

```
.options spef=" scope filename"
```

## Description

Specifies the SPEF file that is to be backannotated and its scope. If you specify this option multiple times, all specified settings are considered.

## Arguments

|                 |                                                                                                                                                                                                                                                  |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>scope</i>    | Specifies the subcircuit or instance name. When a subcircuit is specified, the SPEF file is backannotated to all the instances of that subcircuit. When an instance is specified, the SPEF file is backannotated to the specified instance only. |
| <i>filename</i> | Specifies the name of the SPEF file. Multiple SPEF files can be specified for backannotation by using the option multiple times.                                                                                                                 |

## Example

### *Spectre format*

```
opt1 options spef="adc a.spef"
```

### *SPICE format*

```
.options spef="adc a.spef"
```

tells the simulator to stitch `a.spef` to the subcircuit `adc`.

## ***Parsing Options Used in Backannotation***

- spfswapterm
- spfxtorprefix
- spfaliasterm
- speftriplet
- spfrcr
- spfrcrfmax
- spfinstancesection
- spfbusdelim
- spfshortpin
- spfscale
- spfcaponly

- [spfreppin](#)
- [sim\\_opt\\_probe\\_spf\\_node](#)
- [sim\\_opt\\_spf\\_probe\\_mode](#)
- [spfhierdelim](#)
- [dpfprefix](#)

## ***spfswapterm***

### **Syntax**

#### *Spectre format*

```
name options spfswapterm="terminal1 terminal2 subcktname"
```

#### *SPICE format*

```
.options spfswapterm="terminal1 terminal2 subcktname".
```

Specifies the terminals of a subcircuit macro-model that can be swapped. In general, this is needed when devices are modeled by subcircuits. If you specify this option multiple times, all specified settings are considered.

### **Example**

#### *Spectre format*

```
opt1 options spfswapterm= "n1 n2 nch_mac"
```

#### *SPICE format*

```
.options spfswapterm= "n1 n2 nch_mac"
```

tells the simulator that terminals `n1` and `n2` of subcircuit `nch_mac` can be swapped.

## ***spfxtorprefix***

### **Syntax**

#### *Spectre syntax*

```
name options spfxtorprefix="substring [replacement_substring]"
```

#### *SPICE syntax*

```
.options spfxtorprefix="substring [replacement_substring]"
```

## Description

Specifies the prefix for the device and net names in the DSPF/SPEF/DPF file. The device names in the pre-layout netlist and the DSPF/SPEF file often do not match, and this option can be used to match them. If you specify this option multiple times, all specified settings are considered.

## Example

### *Spectre syntax*

```
opt1 options spfxtorprefix="XM X"
```

### *SPICE syntax*

```
.options spfxtorprefix="XM X"
```

Considering that XX1/XM1 exists in the pre-layout netlist but the corresponding device name in the DSPF file is XM1/XM1, the above setting changes XM to X for successful backannotation.

## *spfaliasterm*

## Syntax

### *Spectre format*

```
name options spfaliasterm="model|subckt prelayout_term1=spf_alias1
 prelayout_term2=spf_alias2 ... prelayout_termN=spf_aliasN"
```

### *SPICE syntax*

```
.options spfaliasterm="model|subckt prelayout_term1=spf_alias1
 prelayout_term2=spf_alias2 ... prelayout_termN=spf_aliasN"
```

## Description

Specifies an alias for the terminal names of devices. This option is useful when the terminal names of devices in DSPF/SPEF/DPF files are different from those in the simulation model library. The terminal names of devices can be different in technology nodes that use subcircuits to model devices. If you specify this option multiple times, all specified settings are considered.

## Example

### *Spectre format*

```
opt1 options spfaliasterm="nfet_mac n1=D n2=G n3=S n4=B"
```

## *SPICE format*

```
.options spfaliasterm="nfet_mac n1=D n2=G n3=S n4=B"
```

tells the simulator that in subcircuit `nfet_mac`, terminal `n1` corresponds to terminal `D` in the DSPF file. Similarly, terminal `n1` corresponds to terminal `G`, terminal `n3` corresponds to terminal `S`, and terminal `n4` corresponds to terminal `B`.

## ***speftriplet***

### **Syntax**

#### *Spectre format*

```
name options speftriplet=1|2|3
```

#### *SPICE format*

```
.options speftriplet=1|2|3
```

### **Description**

Specifies which value out of the triplet should be used for backannotation in the SPEF file. This option is effective only when the values in the SPEF file are represented as triplets (for example, `0.325:0.41:0.495`). The default value is 2, which means that the second value will be used.

### **Example**

#### *Spectre format*

```
name options speftriplet=1
```

#### *SPICE format*

```
.options speftriplet=1
```

tells the simulator to choose the first value for backannotation from the triplet in the SPEF file.

## ***spfrcr***

### **Syntax**

#### *Spectre syntax*

```
name options spfrcr = 0 | 1
```

#### *SPICE syntax*

```
.options spfrcr = 0 | 1
```

## Description

Specifies whether RC reduction in parasitic backannotation be enabled. The default value is 1, which enables RC reduction. When `spfrcr` is set to 0, RC reduction is disabled. This options works independently of the `+parasitics` option.

## Example

### *Spectre syntax*

```
opt1 options spfrcr = 0
```

### *SPICE syntax*

```
.options spfrcr = 0
```

tells the simulator to disable RC reduction during parasitic backannotation.

## ***spfrcrfmax***

## Syntax

### *Spectre syntax*

```
name options spfrcrfmax = value
```

### *SPICE syntax*

```
.options spfrcrfmax = value
```

## Description

Defines the maximum frequency for RC reduction performed during parasitic backannotation. The unit is in GHz and the default value is 25GHz.

## Example

### *Spectre syntax*

```
opt1 options spfrcrfmax=10
```

### *SPICE syntax*

```
.options spfrcrfmax=10
```

The above statement sets the maximum frequency for parasitic backannotation RC reduction to 10GHz.

## ***spinstancesection***

### **Syntax**

#### *Spectre Syntax*

```
name options spinstancesection = 0 | 1
```

#### *SPICE syntax*

```
.options spinstancesection = 0 | 1
```

### **Description**

Controls the device parameter backannotation from the instance section of the DSPF file. If `spinstancesection` is turned off (0), the instance section is ignored in backannotation. Default is on (1).

### **Example**

#### *Spectre syntax*

```
opt1 options spinstancesection=0
```

#### *SPICE syntax*

```
.options spinstancesection=0
```

The above statement disables the backannotation of the DSPF instance section device parameters.

## ***spbusdelim***

### **Syntax**

#### *Spectre syntax*

```
name options spbusdelim="schematic_busdelim [DSPF_busdelim]"
```

#### *SPICE syntax*

```
.options spbusdelim="schematic_busdelim [DSPF_busdelim]"
```

### **Description**

Allows to map the bus delimiter between schematic and DSPF, SPEF, and cap file. The option defines the bus delimiter in the schematic netlist, and optionally the bus delimiter in the DSPF file.

By default, the bus delimiter of the DSPF file is taken from the DSPF file header (that is, \*|BUSBIT [], \*|BUS\_BIT [], or \*|BUS\_DELIMITER []).

If the bus delimiter is not defined in the parasitic file header, you need specify it by using the `spfbusdelim` option in schematic netlist.

## Example 1

### *Spectre syntax*

```
opt1 options spfbusdelim="<>"
```

### *SPICE syntax*

```
.options spfbusdelim="<>"
```

A<1> is mapped to A\_1 in the DSPF file, if the bus delimiter in the DSPF file is \_.

## Example 2

### *Spectre syntax*

```
opt1 options spfbusdelim="@ []"
```

### *SPICE syntax*

```
.options spfbusdelim="@ []"
```

A@1 is mapped to A[1] in the DSPF file.

## *spfshortpin*

### Syntax

#### *Spectre syntax*

```
name options spfshortpin=yes|no
```

#### *SPICE syntax*

```
.option spfshortpin=yes|no
```

### Description

Enables or disables the shorting of pins (\*|P) for same net (\*|NET). If the value of `spfshortpin` is set to `yes`, all \*|P pins in the same net section are shorted. If the value is set to `no`, then pins are not shorted.

## Example

```
opt1 options spfshortpin=no
```



## ***spfscale***

### **Syntax**

#### *Spectre syntax*

```
name options spfscale=value
```

#### *SPICE syntax*

```
.options spfscale=value
```

### **Description**

Specifies the scaling factor of all instances in the parasitic file. The default value is 1.

### **Example**

Consider that the MOSFET width is defined as  $w=2$  in the DSPF file.

#### *Spectre format*

```
opt1 options spfscale=1u
```

#### *SPICE syntax*

```
.options spfscale=1u
```

Scales the width of the MOSFET to 2u.

## ***spfcaponly***

### **Syntax**

#### *Spectre syntax*

```
name options spfcaponly=0|1
```

#### *SPICE syntax*

```
.options spfcaponly=0|1
```

### **Description**

Specifies whether only capacitors need to be backannotated (C-only stitching). The default value is 0 (both R and C are backannotated).

### **Example**

## *Spectre format*

```
opt1 options spfcaponly=1
```

## *SPICE syntax*

```
.options spfcaponly=1
```

Tells the simulator to backannotate capacitors only and discard the parasitic resistors.

## ***spfreppin***

### **Syntax**

#### *Spectre syntax*

```
name options spfreppin=0|1|2|3
```

#### *SPICE syntax*

```
.options spfreppin=0|1|2|3
```

### **Description**

Specifies whether to choose the first instance pin, last instance pin, first instance pin after sorting, or the last instance pin after sorting as the representative node. Default is 0, which means that the first instance pin is chosen as the representative mode.

### **Example**

#### *Spectre format*

```
opt1 options spfreppin=1
```

#### *SPICE syntax*

```
.options spfreppin=1
```

Tells the simulator to choose the last instance pin as the representative mode.

## ***sim\_opt\_probe\_spf\_node***

### **Syntax**

#### *Spectre syntax*

```
name options sim_opt_probe_spf_node=0|1|2|3|4
```

#### *SPICE syntax*

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```
.options sim_opt_probe_spf_node=0|1|2|3|4
```

## Description

Controls the probing of backannotated nodes. This option is supported only in Spectre XPS.

- 0 - Do not probe backannotated nodes. This is the default.
- 1 - Probe the instance pins of the SPF net.
- 2 - Probe all instance pins internal nodes of the SPF net.
- 3 - Probe the instance pins of all device gates
- 4 - Probe the instance pins of the primary device gate (skip finger devices)

## Examples

### *Spectre format*

```
opt1 options sim_opt_probe_spf_node=1
```

### *SPICE syntax*

```
.options sim_opt_probe_spf_node=1
```

tells the simulator to probe the instance pin of the SPF net.

## ***sim\_opt\_spf\_probe\_mode***

## Syntax

### *Spectre syntax*

```
name options sim_opt_spf_probe_mode=0|1
```

### *SPICE syntax*

```
.options sim_opt_spf_probe_mode=0|1
```

## Description

Controls the probe name of spf nodes. This option is supported only in Spectre XPS.

- 0 - Flattened node name in `<net_name>#<flatten_nodename>` format.
- 1 - Hierarchical node name following the net. This is default.

## Examples

## *Spectre format*

```
opt1 options sim_opt_spf_probe_mode=1
```

## *SPICE syntax*

```
.options sim_opt_spf_probe_mode=1
```

Tells the simulator to probe signals in format `<net_name>#<flatten_nodename>`. For example, `net074#xi0/xi0/xgi1/mna:g`.

## ***spfhierdelim***

### **Syntax**

#### *Spectre syntax*

```
name options spfhierdelim=char
```

#### *SPICE syntax*

```
.options spfhierdelim=char
```

### **Description**

Specifies the hierarchical delimiter to be used in the SPF file. The default value is ".".

### **Example**

#### *Spectre format*

```
opt1 options spfhierdelim=/'
```

#### *SPICE syntax*

```
.options spfhierdelim=/'
```

Tells the simulator to use / as the hierarchical delimiter in the SPF file.

## ***dpfprefix***

### **Syntax**

#### *Spectre syntax*

```
name options dpfprefix=char
```

#### *SPICE syntax*

```
.options dpfprefix=char
```

## Description

Backannotates the instances with the leading character(s) specified by this option. The default value is ".".

## Example

### *Spectre format*

```
opt1 options dpfprefix="m x"
```

### *SPICE syntax*

```
.options dpfprefix="m x"
```

Tells the simulator to only backannotate the instances with leading char *m* or *x*.

## Selective Backannotation Options

- spfcnet
- spfcnetfile
- spfrcnet
- spfrcnetfile
- spfnetcmin
- spfskipnet
- spfskipnetfile

## *spfcnet*

## Syntax

### *Spectre Syntax*

```
name options spfcnet=netname
```

### *SPICE syntax*

```
.options spfcnet=netname
```

## Description

Backannotates the total capacitance of the specified net. All other parasitic components such as parasitic resistors that are associated with this net are ignored. The complete hierarchical

net names should be specified. If you specify this option multiple times, all specified settings are considered.

Backannotation attaches only one grounded capacitor with value computed by the total capacitance (defined in `*NET` statement in the DSPF file) subtracted by the total capacitance of all cross-coupling capacitors of this net. All terminals of cross-coupling capacitors which are connected to the subnodes of the specified net are reconnected to the node of the net, and their values are subtracted from the total capacitance.

### Example

#### *Spectre format*

```
opt1 options spfcnet=X1.netA spfcnet=netB
```

#### *SPICE format*

```
.options spfcnet=X1.netA spfcnet=netB
```

tells the simulator to stitch only the total lumped capacitance to nets `X1.netA` and `netB`.

### ***spfcnetfile***

### Syntax

#### *Spectre syntax*

```
name options spfcnetfile=filename
```

#### *SPICE syntax*

```
.options spfcnetfile=filename
```

### Description

Specifies a text file, which contains a list of C-only backannotated nets. The format of the text file requires you to specify one net per line. This option stitches the lumped capacitance to the nets specified in the text file, similar to the `spfcnet` option. Only one file name can be specified per option. If you specify this option multiple times, all specified values are considered.

### Example

#### *Spectre format*

```
opt1 options spfcnetfile=nets.text
```

#### *SPICE syntax*

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```
.options spfrcnetfile=nets.text
```

Considering that the file `nets.text` contains:

```
netA
netB
netC
```

tells the simulator to stitch lumped total capacitance to `netA`, `netB`, and `netC`.

## ***spfrcnet***

### **Syntax**

#### *Spectre syntax*

```
name options spfrcnet=netname
```

#### *SPICE syntax*

```
.options spfrcnet=netname
```

### **Description**

Specifies the name of the net to be backannotated with parasitic resistors and capacitors. The other nets are backannotated with lumped total capacitances. Wildcards are supported and you can specify as many nets as needed. Full hierarchical net names are required.

### **Example**

#### *Spectre syntax*

```
opt1 options spfrcnet=netA
```

#### *SPICE syntax*

```
.options spfrcnet=netA
```

tells the simulator to stitch `netA` with parasitic resistors and capacitors. Also, if is the only `spfrcnet` option specified, backannotate other nets with lumped total capacitance.

## ***spfrcnetfile***

### **Syntax**

#### *Spectre syntax*

```
name options spfrcnetfile="filename"
```

## *SPICE syntax*

```
options spfrcnetfile="filename"
```

## **Description**

Specifies a text file, which contains a list of RC backannotated nets. The format of the text file requires you to specify one net per line. The net names specified in the file are backannotated with parasitic resistors and capacitors, similar to the `spfrcnet` option. The other nets are backannotated with lumped total capacitances. Only one file name can be specified per option.

## **Example**

### *Spectre syntax*

```
opt1 options spfrcnetfile=nets.text
```

### *SPICE syntax*

```
.options spfrcnetfile=nets.text
```

`nets.text` file contains:

```
netA
```

```
netB
```

```
netC
```

tells the simulator to stitch resistance and capacitance to nets `netA`, `netB` and `netC`, and stitch only capacitance to all other nets.

## ***spfnetcmin***

## **Syntax**

### *Spectre syntax*

```
name options spfnetcmin=value
```

### *SPICE syntax*

```
.options spfnetcmin=value
```

## **Description**

Selects the nets for backannotation using the value of their total node capacitance. If a net's total node capacitance exceeds the `spfnetcmin` value, all the parasitics associated with the net are backannotated correctly; otherwise, only the total capacitance is added to the net node.



## Example

### *Spectre syntax*

```
opt1 options spfnetcmin=1.0e-16.
```

### *SPICE syntax*

```
options spfnetcmin=1.0e-16.
```

tells the simulator to stitch resistance and capacitance on the nets whose total capacitance is more than  $1.0e-16$ , and only capacitance for the nets whose total capacitance is less than  $1.0e-16$ .

## ***spfskipnet***

## Syntax

### *Spectre syntax*

```
name options spfskipnet=netname
```

### *SPICE syntax*

```
.options spfskipnet=netname
```

## Description

Specifies the nets that are to be skipped for backannotation, that is, none of the parasitic components of the nets are backannotated. Wildcards are supported. If you specify this option multiple times, all specified settings are considered.

## Example

### *Spectre syntax*

```
opt1 options spfskipnet=X1.nodeA
```

### *SPICE syntax*

```
.options spfskipnet=X1.nodeA
```

tells the simulator to skip backannotation of net `X1.nodeA`.

## ***spfskipnetfile***

## Syntax

### *Spectre format*

```
name options spfskipnetfile=filename
```

## *SPICE format*

```
options spfskipnetfile=filename
```

## Description

Specifies a text file, which contains the list of nets to be skipped for backannotation. The format of the text file requires you to specify one net per line. Only one file name can be specified per option setting.

## Example

### *Spectre format*

```
opt1 options spfskipnetfile=nets.text
```

### *SPICE format*

```
.options spfskipnetfile=nets.text
```

Considering `nets.text` file contains:

```
netA
netB
netC
```

tells the simulator to skip nets `netA`, `netB` and `netC` for backannotation.

## ***Backannotation Message Control Options***

- `spfmglimit`
- `spfprintlargercnet`

### ***spfmglimit***

## Syntax

### *Spectre syntax*

```
name options spfmglimit='number STITCH-ID_1 STITCH-ID_2'
```

### *SPICE syntax*

```
.options spfmglimit='number STITCH-ID_1 STITCH-ID_2'
```

## Description

Sets the maximum number of messages (message limit) for a specified message category identifier (*STITCH-ID*) to be printed in the `.spfrpt` file. When a *STITCH-ID* is not specified, the software assigns the maximum message number limit to all message categories. If you do not specify a *number*, the software assigns the maximum limit of 50 (default) messages for each message category.

### Examples

#### *Spectre format*

```
opt1 options spfmsglimit="10 STITCH-0010"
```

#### *SPICE syntax*

```
.options spfmsglimit="10 STITCH-0010"
```

tells the simulator to print no more than 10 messages for the *STITCH-0010* message category. For the other message categories, the default maximum limit of 50 messages will apply.

#### *Spectre syntax*

```
opt1 options spfmsglimit="1000000"
opt2 options spfmsglimit="5 STITCH-0020"
```

#### *SPICE syntax*

```
.options spfmsglimit="1000000"
.options spfmsglimit="5 STITCH-0020"
```

tells the simulator to print no more than 1000000 messages for all message categories except *STITCH\_0020* for which no more than 5 messages will be printed.

### ***spfprintlargercnet***

### Syntax

#### *Spectre format*

```
name options spfprintlargercnet=value
```

#### *SPICE format*

```
.options spfprintlargercnet=value
```

### Description

Sets the threshold for large RC nets by specifying the number of resistors and capacitors in one net. Spectre XPS writes the large RC net statistics information in the log file.

## Examples

### *Spectre format*

```
opt1 options spfprintlargercnet=100
```

### *SPICE format*

```
.options spfprintlargercnet=100
```

Spectre XPS reports the large RC nets in the log file, as shown below.

```
Nets with number of RC > 100
```

```
=====
123 out
261 x1.mid
132 in
3828 x1.vddp
.....
```

In the report, the first column is the sum of the number of resistors and capacitors, and the second column is the name of RC net.

## ***Frequently Asked Question***

### **Why are the expanded ground capacitors more than the parsed ground capacitors?**

During backannotation, certain cross-coupling capacitors are grounded and these capacitors are counted in the category of expanded ground capacitors. During backannotation, cross-coupling capacitors are grounded if:

- several cross-coupling capacitors attached to net A have no corresponding nets for their second terminal. In this case, all cross-coupling capacitors are lumped to ground as one grounded capacitor. Therefore, expanded grounded capacitors are more than those parsed.
- net A is erroneous. In this case, all parsed capacitors are discarded and one grounded total capacitor is expanded.
- a net is backannotated with C-only. In this case, no capacitors are parsed but one total grounded capacitor is expanded.

## Parasitic Backannotation Report

The Spectre log file contains a section PARASITIC BACK-ANNOTATION SUMMARY that displays the following information:

```

PARASITIC BACK-ANNOTATION SUMMARY:
File: "decoder.dpf"
File: "decoder.spf"

 Nets parsed 1089
 annotated RC 1081 (99.2%)
 annotated C-only 0 (0.0%)
 annotated spfcnet 2 (0.2%)
 skipped spfskipnet 4 (0.4%)

 CrossCaps| parsed 0
 annotated 0 (0.0%)
 grounded 0 (0.0%)

 C in RC nets parsed 12949
 annotated 12949 (100%)
 R in RC nets parsed 25662
 annotated 25662 (100%)

 Instances parsed 2761
 annotated 1860 (67.4%)
 skipped 901 (32.6%)

1 errors and 0 warnings (fixed errors)are issued (see file
"test_stitch_report.xps.spfrpt")

Message Statistics
=====
Node not found 1
Instance section detected 1
Skipped net due to filtering 5

```

Description of the fields in the report is given below.

| Field            | Description                     |
|------------------|---------------------------------|
| Nets parsed 1089 | Number of nets in the SPF file. |

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|                             |                                                                                                    |
|-----------------------------|----------------------------------------------------------------------------------------------------|
| annotated RC 1081 (99.2%)   | Number of nets that are annotated with R and C.                                                    |
| annotated C-only 0 (0.0%)   | Number of nets that are annotated with C only.                                                     |
| annotated spfcnet 2 (0.2%)  | Number of nets specified using the <code>spfcnet</code> option.                                    |
| skipped spfskipnet 4 (0.4%) | Number of nets specified using the <code>spfskipnet</code> option.                                 |
| CrossCaps parsed 0          | Number of coupling caps in the SPF file.                                                           |
| annotated 0 (0.0%)          | Number of coupling caps annotated successfully.                                                    |
| grounded 0 (0.0%)           | Number of coupling caps that are grounded for some reason (for example, one terminal is floating). |
| Instances parsed 2761       | Number of instances in the Instance section                                                        |
| annotated 1860 (67.4%)      | Number of instances backannotated.                                                                 |
| skipped 901 (32.6%)         | Number of instances skipped.                                                                       |

Errors and warning messages can be located in the stitching report file `.xps.spfrpt`.

### Some Common Error and Warning Messages Related to Parasitic Backannotation

#### **ERROR (STITCH-0000)(:12): Node xio.xb1.n3 not found. Net is not expanded.**

This error message is generated when the net name does not match the pre-layout name or the node does not exist.

To fix the net mismatch issue, use the `spfxtorprefix` option.

#### **WARNING (STITCH-0039)(:49): Net x1.mid is skipped due to filtering**

This message is generated when nets are skipped using the `spfskipnet` option.

For better performance, ensure that the total capacitance of the nets specified using the `spfskipnet` option is backannotated.

#### **WARNING (STITCH-0011)(:32): Only total cap is attached to net net19.**

This message is generated when C-only backannotation is enabled. For better performance, ensure that the total capacitance of the nets specified using the `spfcnet` option is backannotated.

**WARNING(STITCH-0084)(:13): Cross-coupling capacitor "c12 (1.3e-17)" is lumped to ground (first node not found in the file scope).**

This message is generated when one net of the coupling cap is not found in pre-layout.

**WARNING(STITCH-0039)(:79): Net net46 is skipped because has zero C-only value**

This message is generated when the `NET` section does not have parasitic capacitance defined.

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# Encryption

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Encryption allows you to protect your proprietary parameters, subcircuits, models, and netlists, and release your libraries to your customers without revealing sensitive information. Your customers can run simulations in the Spectre<sup>®</sup> circuit simulator with the encrypted netlists – the Spectre circuit simulator does not print any data inside the encrypted blocks. Messages about the encrypted portions of your circuit are suppressed.

You can encrypt netlists that are in the Spectre and Berkeley SPICE formats.

You cannot use encryption if you are using the Spectre Compiled-Model Interface (CMI).

This chapter covers the following topics:

- [“New key for Encryption”](#) on page 926.
- [“Encrypting a Netlist”](#) on page 927
- [“Encrypted Information During Simulation”](#) on page 933.

## **New key for Encryption**

Starting with the SPECTRE19.1 release, Spectre uses a new key ( $k-4$ ) as default. You can use the  $k-3$  option to invoke the old key. The following table lists the usage of the key in the SPECTRE18.1 ISR8 and SPECTRE19.1 releases.

|                             | <b>Old Key</b> | <b>New Key</b> |
|-----------------------------|----------------|----------------|
| <b>SPECTRE18.1<br/>ISR8</b> | default        | $k-4$          |
| <b>SPECTRE19.1</b>          | $k-3$          | default        |

## Encrypting a Netlist

To encrypt a netlist,

1. Open the netlist you want to encrypt in a text editor.
2. Type `PROTeCt` above the data you want to protect. The capital letters indicate the shortest legal abbreviation, so you achieve the same affect by typing `prote` or `protec` for example.
3. Type `UNPROTeCt` after the last line of the data you want to protect. The capital letters indicate the shortest legal abbreviation, so you achieve the same affect by typing `unprote` or `unprotec` for example.

You must use the `protect` and `unprotect` keywords in pairs.

4. Save the netlist.
5. In a terminal window, type

```
spectre_encrypt [-i input_file] [-o output_file] [-all] [-key 1|2|3|4]
```

where

|                    |                                                                                                                                                                                                                                                                                             |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>input_file</i>  | The path and name of the netlist to be encrypted. If you do not specify the input file, the netlist from standard input is encrypted.                                                                                                                                                       |
| <i>output_file</i> | The path and name of a file to hold the encrypted netlist. The extension that you use for <i>output_file</i> must be the same extension used on <i>input_file</i> .<br>If you do not specify the output file, the encrypted netlist is displayed as standard output in the terminal window. |
| <code>-all</code>  | Encrypts the entire netlist, ignoring the <code>protect</code> and <code>unprotect</code> keywords.                                                                                                                                                                                         |
| <code>-key</code>  | By default, the netlist encrypted in SPECTRE19.1 release onwards cannot be decrypted using earlier versions.                                                                                                                                                                                |

The Spectre circuit simulator uses the SSL CRYPTO library to encrypt your netlist.

**Note:** `spectre_encrypt` does not require any license, however, it checks for the existence of any of the 32500, *Virtuoso\_Multi\_mode\_Simulation*, *Virtuoso\_Spectre*, *Virtuoso\_Spectre\_XL*, or *Virtuoso\_Spectre\_GXL* licenses. If any of these licenses is not available, it generates an error.

The `protect` and `unprotect` keywords are replaced with `pragma` statements in the output netlist. The `pragma` statements contain important information about encryption such as the method used, the key name, and the beginning and end of the encrypted block. The Spectre circuit simulator uses this information while decrypting the netlist. Hence it is important that you do not modify any `pragma` statement or the encrypted text between the `pragma` statements in the output file.



To view a demonstration on encrypting a Spectre netlist, see [\*Protecting Proprietary Information in a Spectre Netlist\*](#) video.

**Note:** Access to this video will depend on the availability of a web browser and a Cadence Online Support account.

## What You can Encrypt

You can encrypt signals, netlist and subcircuit parameters, files, devices, and model cards. You can use multiple pairs of `protect`, `unprotect` to encrypt different portions of your netlist. The content inside the `protect`, `unprotect` block is encrypted and the content outside this block remains the same as the original netlist.

### Encrypting a File

You can encrypt a file by adding `protect` at the beginning and `unprotect` at the end of the file.

### Encrypting Subcircuits

As described in the following sections, you can encrypt an entire subcircuit, part of a subcircuit, or multiple subcircuit blocks.

#### *Encrypting an Entire Subcircuit*

To encrypt an entire subcircuit, place `protect` before the `subckt` and `unprotect` after the `ends` statement. This encrypts the subcircuit name as well as the I/O pins. Since the interfaces are not readable after encryption, Cadence recommends that you add some information on how the interface works outside the protected block so that your users can create Composer symbols for simulation.

All flattened primitive devices expanded from a protected subcircuit are also protected.

## Example

### Original Netlist

```
* subckt name :inv, I/O pins:2
* parameters wi, le
protect
subckt inv out in
parameters wi=1u le=3u
mp1 mid in vd vd pmos w=wi l=le
mn1 mid in 0 0 nmos w=wi l=le
r1 mid out resistor r=2k
model pmos bsim3v3 type=p tnom=27.0
tox=2.9e-09
model nmos bsim3v3 type=n tnom=27.0
tox=2.8e-09
ends
unprotect

* open latch module
subckt latch q qbar clk d
...
```

### Encrypted Netlist

```
* subckt name :inv, I/O pins:2
* parameters wi, le
//pragma protect begin_protected
//pragma protect data_method = AES
//pragma protect data_keyowner = Cadence
Design Systems.
//pragma protect data_keyname = CDS_KEY
//pragma protect data_keyversion = 4
//pragma protect data_block
fajdfejwrADFASDfdhfhjadfahd
QERWfdjau77r42jagadfhjkuer
jdfejwrADFASDfdhfhjad
jdfejwrADFASDfdhfhjad
//pragma protect end_protected

* open latch module
subckt latch q qbar clk d
...
```

### ***Encrypting a Subcircuit without Interfaces***

To encrypt the contents of a subcircuit leaving its name and I/O pins public, place `protect` after `subckt` and `unprotect` before `ends`.

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## Example

### Original Netlist

```
subckt inv out in
protect
parameters wi=1u le=3u
mp1 mid in vd vd pmos w=wi l=le
mn1 mid in 0 0 nmos w=wi l=le
r1 mid out resistor r=2k
model pmos bsim3v3 type=p tnom=27.0
tox=2.9e-09
model nmos bsim3v3 type=n tnom=27.0
tox=2.8e-09
unprotect
ends

* open latch module
subckt latch q qbar clk d
...
```

### Encrypted Netlist

```
subckt inv out in
//pragma protect begin_protected
//pragma protect data_method = AES
//pragma protect data_keyowner = Cadence
Design Systems.
//pragma protect data_keyname = CDS_KEY
//pragma protect data_keyversion = 4
//pragma protect data_block
fajdfejwrADFASDfdhfhjadfahd
QERWfdjau77r42jagadfhjkuer
//pragma protect end_protected
ends

* open latch module
subckt latch q qbar clk d
...
```

## ***Encrypting Portions of a Subcircuit or Multiple Subcircuits***

You can use multiple pairs of `protect` and `unprotect` in a subcircuit to protect portions of it. See the example below.

## Example

### Original Netlist

```
subckt inv out in
parameters wi=1u le=3u
protect
mp1 mid in vd vd pmos w=wi l=le
mn1 mid in 0 0 nmos w=wi l=le
unprotect
r1 mid out resistor r=2k
protect
model pmos bsim3v3 type=p tnom=27.0
tox=2.9e-09
model nmos bsim3v3 type=n tnom=27.0
tox=2.8e-09
unprotect
ends inv
...
```

### Encrypted Netlist

```
subckt inv out
parameters wi=1u le=3u
global vd
//pragma protect begin_protected
//pragma protect data_method = RC5
//pragma protect data_keyowner= Cadence Design
Systems.
//pragma protect data_keyname = CDS_KEY
//pragma protect data_block
QERWfdjau77r42jagadfhjkuer
//pragma protect end_protected
r1 mid out 2k
//pragma protect begin_protected
etu45j6jgfly5po765t8tnji5j5i76k
// pragma protect end_protected
ends inv
...
```

If you have multiple subcircuits in your netlist, you can encrypt them by using multiple pairs of `protect` and `unprotect` as shown in the example above.

## Encrypting a Model Card

You can encrypt one or more model cards with a pair of `protect` and `unprotect` keywords. The keywords do not have to be within or outside the model card. Even if you encrypt only a portion of the model card, the entire model card is protected during simulation. In case there are no parameters within a protected block, the Spectre circuit simulator displays a warning message, but still encrypts the model card.

### Example 1

In the following example, the encryption keywords are around the model card definition. The model name and all parameters are encrypted.

## Original Netlist

```
* The 1st model name is pmos, type is p
* The 2nd model name is nmos, type is n
subckt inv out in
parameters wi=1u le=3u
mp1 mid in vd vd pmos w=wi l=le
mn1 mid in 0 0 nmos w=wi l=le
ends inv
protect
model pmos bsim3v3 type=p tnom=27.0
tox=2.9e-09
model nmos bsim3v3 type=n tnom=27.0
tox=2.8e-09
unprotect
```

## Encrypted Netlist

```
* The 1st model name is pmos, type is p
* The 2nd model name is nmos, type is n
subckt inv out in
parameters wi=1u le=3u
mp1 mid in vd vd pmos w=wi l=le
mn1 mid in 0 0 nmos w=wi l=le
ends inv
//pragma protect begin_protected
//pragma protect data_method = AES
//pragma protect data_keyowner = Cadence
Design Systems.
//pragma protect data_keyname = CDS_KEY
//pragma protect data_keyversion = 4
//pragma protect data_block
QERWfdjau77r42jagadfhjkuer
//pragma protect end_protected
```

## Example 2

In the following example, the `protect` keyword is within the model card definition, leaving a number of parameters outside the protection block. The model name and parameters outside



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the protection block remain public, but the whole model is protected for message and parameter output during simulation.

## Original Netlist

```
model pmos bsim3v3 type=p tnom=27.0
tox=2.9e-09
protect
Nch=2.498E+17 Tox=27.0 tox=2.9e-09
Xj=1.00000E-07
+Lint=9.36e-8 Wint=1.47e-7
+Vth0=.6322 K1=.756 K2=-3.83e-2
+Dvt2=-9.17e-2 Nlx=3.52291E-08
Dwg=-6.0E-09 Dwb=-3.56E-09
+Cit=1.622527E-04 Cdsc=-2.147181E-05
unprotect
```

## Encrypted Netlist

```
model pmos bsim3v3 type=p tnom=27.0
tox=2.9e-09
//pragma protect begin_protected
//pragma protect data_method = AES
//pragma protect data_keyowner = Cadence
Design Systems.
//pragma protect data_keyname = CDS_KEY
//pragma protect data_keyversion = 4
//pragma protect data_block
fajdfejwrADFASDfdhfdjadfahd
//pragma protect end_protected
```

## Encrypting an Include File

If there is an include file in the encrypted portion of your netlist, you must encrypt it separately.

## Encrypted Information During Simulation

When you simulate an encrypted netlist, all warnings, error messages, and `info` statements about the encrypted portions of your netlist are suppressed.

**Note:** Spectre cannot parse an encrypted file when C preprocessor (CPP) is enabled. Therefore, do not use the `-E`, `-D`, and `-U` options in the file, since these options enable CPP. In addition, wildcards are not supported in CPP.

The following sections describe how the Spectre circuit simulator handles the encrypted portions of your netlist.

## Protected Device

A device is encrypted if any of the following conditions are met:

- It is a primitive and inside a protected block.
- It is an instance of a subcircuit. The instance is not in a protected block, but the subcircuit is protected. Here is an example:

```
X1 in out INV
subckt INV (in out)
protect
mp1 vdd in vdd pmos W=1.0e-6 L=1.0e-6
mn1 out in 0 0 nmos W=1.0e-6 L=1.0e-6
unprotect
ends INV
```

In the flattened netlist, devices X1/mp1 and X1/mn1 are protected.

- It is an instance of a subcircuit, and the instance is in a protected block. Whether the subcircuit is protected or not, all the flattened primitive devices from that hierarchical level are protected. An example is given below.

```
protect
X1 in out INV
unprotect
subckt INV (in out)
mp1 vdd in vdd pmos W=1.0e-6 L=1.0e-6
mn1 out in 0 0 nmos W=1.0e-6 L=1.0e-6
ends INV
```

In the flattened netlist, devices X1/mp1 and X1/mn1 are protected.

For a device meeting any of the above criteria, its name and instance parameters are protected. The instance parameters of a protected device cannot be modified through an `alter` statement, but the protected device can be replaced through an `altergroup` statement. Information about a protected device is filtered out in all analyses outputs.

Encrypted devices are not included in the circuit inventory.

## Protected Node

A node contained exclusively within a protected block is protected, and its name and value is not displayed in the output file. If you request an `ic` file or restart a simulation, protected nodes are displayed in encrypted format in the `ic`, checking point, and restart output files.

## Protected Global and Netlist Parameters

Global and netlist parameters defined inside a protected block are encrypted. However, you can alter or sweep a protected parameter. All device instance and model parameters dependent on the altered parameter are updated even if the device or model is protected.

## **Protected Subcircuit Parameters**

Subcircuit parameters are protected if they appear exclusively within a protected block. All devices or model cards that refer to encrypted parameters must be in a protected block to protect the parameter values. If protected parameters are referred to by an unprotected device or model card, the parameter values are printed in the info statements for this device or model card.

You can alter or sweep a protected subcircuit parameter. All device instance and model parameters dependent on the altered parameter are updated even if the device or model is protected.

## **Protected Model Parameters**

For a model card inside a protected block (where the `protect` keyword appears before the `model` statement), the model card and all model parameters are encrypted. If you place `protect` after the model definition and leave some parameters outside a protection block, only parameters inside the protection block are encrypted. During simulation, all parameters inside the model card are encrypted since encryption is done on the basis of the model card, not individual parameters. Warning messages and *info* statements for all model parameters and values of a protected model card are suppressed.

Even if the model name is protected, you can instantiate primitives using that model. You cannot alter or sweep protected model parameters, but you can replace a protected model through an `altergroup` statement.

## **Multiple Name Spaces**

Names of parameters, subcircuits, models, and devices that appear exclusively within protected blocks are encrypted. However, identical names appearing outside the protected blocks are bound to their encrypted counterparts. Hence, Cadence recommends that you give unique names to the parameters, subcircuits, models, and devices you want to protect.

## **Displaying Messages Generated From an Encrypted Block**

By default, messages generated from an encrypted block are not displayed in the Spectre log file. You can use the `simulator visible=messages` and `simulator visible=none` keywords to show or hide messages that are generated from an encrypted block.

Consider the following example:

```
simulator lang=spectre
```

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```
parameters c1=1p c2=2p c10=c1+c2
parameters res=10k
protect
simulator visible=messages
r1 1 0 resistor r=res
simulator visible=none
c1 1 0 capacitor c=c10
unprotect
run dc
spectre2 options currents=all
```

In the above example, `r1` and `c1` are specified in a protected block and both have errors. However, because `r1` has been specified using the keyword `simulator visible=messages`, the message related to `r1` will be displayed in the Spectre log file. On the other hand, the message related to `c1` will not be displayed in the log file because it has been specified using the keyword `simulator visible=none`.

**Note:** Currently, this feature is applicable only to SFE messages.

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## Time-Saving Techniques

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In this chapter, you will learn about different methods to reduce simulation time. This chapter discusses the following topics:

- [Specifying Efficient Starting Points](#) on page 938
- [Reducing the Number of Simulation Runs](#) on page 938
- [Adjusting Speed and Accuracy](#) on page 938
- [Saving Time by Starting Analyses from Previous Solutions](#) on page 938
- [Saving Time by Specifying State Information](#) on page 939
- [Saving Time by Modifying Parameters during a Simulation](#) on page 944
- [Saving Time by Selecting a Continuation Method](#) on page 947

## Specifying Efficient Starting Points

The Spectre® circuit simulator arrives at a solution for a simulation by calculating successively more accurate estimates of the final result. You can increase simulation speed by providing information that the Spectre simulator uses to increase the accuracy of the initial solution estimate. There are three ways to provide a good starting point for a simulation:

- Start analyses from previous solutions
- Specify initial conditions for components and nodes
- Specify solution estimates with nodesets

## Reducing the Number of Simulation Runs

With the Spectre simulator, you can run many analyses (including analyses of the same type) in a single simulation. With other SPICE-like simulators, you might require multiple simulations to complete the same tasks. In a single simulation run, you can run a set of Spectre analyses; modify the component, temperature, or `options` parameters; and then run additional analyses with the new parameters.

## Adjusting Speed and Accuracy

You can use the `errpreset` parameter to increase the speed of transient analyses, but this speed increase requires some sacrifice of accuracy.

## Saving Time by Starting Analyses from Previous Solutions

A solution for one analysis can be an appropriate starting point for the next analysis. For example, if a DC analysis precedes a transient analysis, you can use the DC solution as the first guess for the initial point in the transient analysis solution. There are two Spectre analysis parameters that let you start analyses from previous solutions. They are available for most Spectre analyses.

- The `restart` parameter

If you set this parameter to `restart=no` in an analysis statement, the Spectre simulator uses the DC solution of the previous analysis as an initial guess for the following analysis.

- The `prevoppoint` parameter

If you set this parameter to `prevoppoint=yes` in an analysis statement, the Spectre simulator does not compute or recompute the operating point. Instead, it uses the operating point computed by the previous analysis.

## **Saving Time by Specifying State Information**

The Spectre simulator lets you provide state information (the current or last-known status or condition of a process, transaction, or setting) to the DC and transient analyses. You can specify two kinds of state information:

- **Initial conditions**

The `ic` statement lets you specify values for the starting point of a transient analysis. The values you can specify are voltages on nodes and capacitors, and currents on inductors.

- **Nodesets**

Nodesets are estimates of the solution you provide for the DC or transient analyses. Nodesets usually act only as aids in speeding convergence, but if a circuit has more than one solution, as with a latch, nodesets can bias the solution to the one closest to the nodeset values.

## **Setting Initial Conditions for All Transient Analyses**

You can specify initial conditions that apply to all transient analyses in a simulation or to a single transient analysis. The `ic` statement and the `ic` parameter described in this section set initial conditions for all transient analyses in the netlist. In general, you use the `ic` parameter of individual components to specify initial conditions for those components, and you use the `ic` statement to specify initial conditions for nodes. You can specify initial conditions for inductors with either method. Specifying `cmin` for a transient analysis does not satisfy the condition that a node has a capacitive path to ground.

**Note:** Do not confuse the `ic` parameter for individual components with the `ic` parameter of the transient analysis. The latter lets you select from among different initial conditions specifications for a given transient analysis.

## **Specifying Initial Conditions for Components**

You can specify initial conditions in the instance statements of capacitors, inductors, and windings for magnetic cores. The `ic` parameter specifies initial voltage values for capacitors and current values for inductors and windings. In the following example, the initial condition voltage on capacitor `Cap13` is set to two volts:

```
Cap13 11 9 capacitor c=10n ic=2
```

## Specifying Initial Conditions for Nodes

You use the `ic` statement to specify initial conditions for nodes or initial currents for inductors. The nodes can be inside a subcircuit or internal nodes to a component.

The following is the format for the `ic` statement:

```
ic signalName=value ...
```

The format for specifying signals with the `ic` statement is similar to that used by the `save` statement. This method is described in detail in [“Saving Main Circuit Signals”](#) on page 255. Consult this discussion if you need further clarification about the following example.

```
ic Voff=0 X3.7=2.5 M1:int_d=3.5 L1:l=1u
```

This example sets the following initial conditions:

- The voltage of node `Voff` is set to 0.
- Node 7 of subcircuit `X3` is set to 2.5 V.
- The internal drain node of component `M1` is set to 3.5 V. (See the following table for more information about specifying internal nodes.)
- The current for inductor `L1` is set to 1μ.

Specifying initial node voltages requires some additional discussion. The following table tells you the internal voltages you can specify with different components.

| Component                     | Internal Node Specifications |
|-------------------------------|------------------------------|
| BJT                           | int_c, int_b, int_e          |
| BSIM                          | int_d, int_s                 |
| MOSFET                        | int_d, int_s                 |
| GaAs MESFET                   | int_d, int_s, int_g          |
| JFET                          | int_d, int_s, int_g, int_b   |
| Winding for Magnetic Core     | int_Rw                       |
| Magnetic Core with Hysteresis | flux                         |



## Supplying Solution Estimates to Increase Speed

You use the `nodeset` statement to supply estimates of solutions that aid convergence or bias the simulation towards a given solution. You can use nodesets for all DC and initial transient analysis solutions in the netlist. The `nodeset` statement has the following format:

```
nodeset signalName=value...
```

Values you can supply with the `nodeset` statement include voltages on topological nodes, including internal nodes, and currents through voltage sources, inductors, switches, transformers, N-ports, and transmission lines.

The format for specifying signals with the `nodeset` statement is similar to that used by the `save` statement. This method is described in detail in [“Saving Main Circuit Signals”](#) on page 255. Consult this discussion if you need further clarification about the following example.

```
nodeset Voff=0 X3.7=2.5 M1:int_d=3.5 L1:l=1u
```

This example sets the following solution estimates:

- The voltage of node `Voff` is set to 0.
- Node 7 of subcircuit `X3` is set to 2.5 V.
- The internal drain node of component `M1` is set to 3.5 V. (See the table in the [ic statements](#) section of this chapter for more information about specifying internal nodes.)
- The current for inductor `L1` is set to 1μ.

## Specifying State Information for Individual Analyses

You can specify state information for individual analyses in two ways:

- You can use the `ic` parameter of the transient analysis to choose which previous specifications are used.
- You can create a state file that is read by an individual analysis.

## Choosing Which Initial Conditions Specifications Are Used for a Transient Analysis

The `ic` parameter in the transient analysis lets you select among several options for which initial conditions to use. You can choose the following settings:

| Parameter Setting | Action Taken                                                                                                                                                                 |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>dc</code>   | Initial conditions specifiers are ignored, and the existing DC solution is used.                                                                                             |
| <code>node</code> | The <code>ic</code> statements are used, and the <code>ic</code> parameter settings on the capacitors and inductors are ignored.                                             |
| <code>dev</code>  | The <code>ic</code> parameter settings on the capacitors and inductors are used, and the <code>ic</code> statements are ignored.                                             |
| <code>all</code>  | Both the <code>ic</code> statements and the <code>ic</code> parameters are used. If specifications conflict, <code>ic</code> parameters override <code>ic</code> statements. |

## Specifying State Information with State Files

You can also specify initial conditions and estimate solutions by creating a state file that is read by the appropriate analysis. You can create a state file in two ways:

- You can instruct the Spectre simulator to create a state file in a previous analysis for future use.
- You can create a state file manually in a text editor.

## Telling the Spectre Simulator to Create a State File

You can instruct the Spectre simulator to create a state file from either the initial point or the final point in an analysis. To write a state file from the initial point in an analysis, use the `write` parameter. To write a state file from the final point, use the `writefinal` parameter. Each of the following two examples writes a state file named `ua741.dc`. The first example writes the state file from the initial point in the DC sweep, and the second example writes the state file from the final point in the DC sweep.

```
Drift dc param=temp start=0 stop=50.0 step=1 readns="ua741.dc" write="ua741.dc"
Drift dc param=temp start=0 stop=50.0 step=1 readns="ua741.dc"
writefinal="ua741.dc"
```

## Creating a State File Manually

The syntax for creating a state file in a text editor is simple. Each line contains a signal name and a signal value. Anything after a pound sign (#) is ignored as a comment. The following is an example of a simple state file:

```
State file generated by Spectre from circuit file 'wilson'
during 'stepresponse' at 5:39:38 PM, Jan 21, 1992.
1 .588793510612534
2 1.17406247989272
3 14.9900516233357
pwr 15
vcc:p -9.9483766642647e-06
```

## Reading State Files

To read a state file as an initial condition, use the `readic` transient analysis parameter. To read a state file as a nodeset, use the `readns` parameter. This example reads the file `intCond` as initial conditions:

```
DoTran z12 tran start=0 stop=0.003 \
 step=0.00015 maxstep=6e-06 readic="intCond"
```

This second example reads the file `soluEst` as a nodeset.

```
DoTran z12 tran start=0 stop=0.003 \
 step=0.00015 maxstep=6e-06 readns="soluEst"
```

## Special Uses for State Files

State files can be useful for the following reasons:

- You can save state files and use them in later simulations. For example, you can save the solution at the final point of a transient analysis and then continue the analysis in a later simulation by using the state file as the starting point for another transient analysis.
- You can use state files to create automatic updates of initial conditions and nodesets.

The following example demonstrates the usefulness of state files:

```
altTemp alter param=temp value=0
Drift dc param=temp start=0 stop=50.0 step=1 readns="ua741.dc0" write="ua741.dc
XferVsTemp xf param=temp start=0 stop=50 step=1 probe=Rload freq=1kHz \
 readns="ua741.dc0"
```

The first analysis computes the DC solution at  $T=0^{\circ}\text{C}$ , saves it to a file called `ua741.dc0`, and then sweeps the temperature to  $T=50^{\circ}\text{C}$ . The transfer function analysis (`xf`) resets the temperature to zero. Because of the temperature change, the DC solution must be recomputed. Without the use of state files, this computation might slow the simulation because the only available estimate of the DC solution would be that computed at  $T=50^{\circ}\text{C}$ , the

final point in the DC sweep. However, by using a state file to preserve the initial DC solution at  $T=0^{\circ}\text{C}$ , you can enable the Spectre simulator to compute the new DC solution quickly. The computation is fast because the Spectre simulator can use the DC solution computed at  $T=0^{\circ}\text{C}$  to estimate the new solution. You can also make future simulations of this circuit start quickly by using the state file to estimate the DC solution. Even if you have altered a circuit, it is usually faster to start the DC analysis from a previous solution than to start from the beginning.

## **Saving Time by Modifying Parameters during a Simulation**

The Spectre simulator lets you place specifications in the netlist to modify parameters and then resimulate. This lets you accomplish tasks with a single Spectre run that might require multiple runs with another simulator. To change parameter settings during a run, you use the following Spectre control statements:

### ■ The `alter` statement

You use this statement to change the parameters of circuits, subcircuits, and individual models or components. You also use it to change the following `options` statement temperature parameters and scaling factors:

- ☐ `temp`
- ☐ `tnom`
- ☐ `scale`
- ☐ `scalem`

You can use the `altergroup` statement to specify device, model, and netlist parameter statements that you want to change the values of with analyses.

### ■ The `set` statement

Except for temperature parameters and scaling factors, you use the `set` statement to modify any `options` statement parameters you set at the beginning of the netlist. The new settings apply to all analyses that follow the `set` statement in the netlist.

The `alter` and `set` statements are queued up with analysis statements and are processed in order.

## Changing Circuit or Component Parameter Values

You modify parameters for devices, models, circuit, and subcircuit parameters during a simulation with the `alter` statement. The modifications apply to all analyses that follow the `alter` statement in your netlist until you request another parameter modification.

### Changing Parameter Values for Components

To change a parameter value for a component device or model, you specify the device or model name, the parameter name, and the new parameter value in the `alter` statement. You can modify only one parameter with each `alter` statement, but you can put any number of `alter` statements in a netlist. The following example demonstrates `alter` statement syntax:

```
SetMag alter dev=Vt1 param=mag value=1
```

- `SetMag` is the unique netlist name for this `alter` statement. (Like many Spectre statements, each `alter` statement must have a unique name.)
- The keyword `alter` is the primitive name for the `alter` statement.
- `dev=Vt1` identifies `Vt1` as the netlist name for the component statement you want to modify. You identify an instance statement with `dev` and a `model` statement with `mod`. When you use the `alter` statement to modify a circuit parameter, you leave both `dev` and `mod` unspecified.
- `param=mag` identifies `mag` as the parameter you are modifying. If you omit this parameter, the Spectre simulator uses the first parameter listed for each component in the Spectre online help as the default.
- `value=1` identifies `1` as the new value for the `mag` parameter. If you leave `value` unspecified, it is set to the default for the parameter.

### Changing Parameter Values for Models

To change a parameter value for model files with the `altergroup` statement, you list the device, model, and circuit parameter statements as you do in the main netlist. Within an `alter` group, each model is first defaulted and then the model parameters are updated. You cannot nest `alter` groups. You cannot change from a model to a model group and vice versa. The following example demonstrates `altergroup` statement syntax:

```
ag1 altergroup {
 parameters p1=1
 model myres resistor r1=1e3 af=p1
 model mybsim bsim3v3 lmax=p1 lmin=3.5e-7
}
```

## Further Examples of Changing Component Parameter Values

This example changes the `is` parameter of a model named `SH3` to the value `1e-15`:

```
modify2 alter mod=SH3 param=is value=1e-15
```

The following examples show how to use the `param` default in an `alter` statement. The first parameter listed for resistors in the Spectre online help (`spectre -h`) is the default. For resistors, this is the resistance parameter `r`.

Consequently, if `R1` is a resistor, the following two `alter` statements are equivalent:

```
change1 alter dev=R1 param=r value=50
change1 alter dev=R1 value=50
```

## Changing Parameter Values for Circuits

When you change a circuit parameter, you use the same syntax as when you change a device or model parameter except that you do not enter a `dev` or a `mod` parameter.

This example changes the ambient temperature to `0°C`:

```
change2 alter param=temp value=0
```

The following table describes the circuit parameters you can change with the `alter` statement:

---

| Parameter           | Description                                              |
|---------------------|----------------------------------------------------------|
| <code>temp</code>   | Ambient temperature                                      |
| <code>tnom</code>   | Default measurement temperature for component parameters |
| <code>scalem</code> | Component model scaling factor                           |
| <code>scale</code>  | Component instance scaling factor                        |

---

**Note:** If you change `temp` or `tnom` using an `alter` statement, all expressions with `temp` or `tnom` are reevaluated.

## Modifying Initial Settings of the State of the Simulator

You can change the initial settings for the state of the simulator by placing a `set` statement in the netlist. The `set` statement is similar to the `options` statement that sets the state of

the simulator, but it is queued with the analysis statements in the order you place them in the netlist.

You use the `set` statement to change previous `options` or `set` statement specifications. The modifications apply to all analyses that follow the `set` statement in the netlist until you request another parameter modification. The `set` and `options` statements have many identical parameters, but the `set` statement cannot modify all `options` statement parameters. The parameter listings in the Spectre online help (`spectre -h`) tell you which parameters you can reset with the `set` statement.

### Formatting the `set` Statement

The following example demonstrates the `set` statement syntax. This example turns off several annotation parameters.

```
Quiet set narrate=no error=no info=no
```

- `Quiet` is the unique name you give to the `set` statement.
- The keyword `set` is the primitive name for the `set` statement.
- `narrate`, `error`, and `info` are the parameters you are changing.

**Note:** If you want to change `temp` or `tnom`, use the `alter` statement.

## Saving Time by Selecting a Continuation Method

The Spectre simulator normally starts with an initial estimate and then tries to find the solution for a circuit using the Newton-Raphson method. If this attempt fails, the Spectre simulator automatically tries several continuation methods to find a solution and tells you which method was successful. Continuation methods modify the circuit so that the solution is easy to compute and then gradually change the circuit back to its original form. Continuation methods are robust, but they are slower than the Newton-Raphson method.

If you need to modify and resimulate a circuit that was solved with a continuation method, you probably want to save simulation time by directly selecting the continuation method you know was previously successful.

You select the continuation method with the `homotopy` parameter of the `set` or `options` statements. In addition to the default setting, `all`, other settings are possible for this parameter: `gmin` stepping (`gmin`), source stepping (`source`), the pseudotransient method (`ptran`), and damped pseudotransient method (`dptran`), . You can also prevent the use of continuation methods by setting the `homotopy` parameter to `none`.





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## Managing Files

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This chapter discusses the following topics:

- [About Spectre Filename Specification](#) on page 950
- [Creating Filenames That Help You Manage Data](#) on page 950

## About Spectre Filename Specification

Many analysis statements require a filename as a parameter value for the input or output of data. It is often easier to keep track of output files if these filename parameter values are related to some other filename, typically the input filename.

The Spectre® circuit simulator's filename specification features help you manage your data by letting you systematically specify or modify filenames. With the Spectre simulator, you can easily identify data from multiple simulation runs or from single runs containing repeated similar analyses. You can modify input filenames so that you can easily identify the output file from a specific simulation or analysis. You can also construct output filenames in ways that prevent accidental overwriting of data.

## Creating Filenames That Help You Manage Data

The Spectre simulator helps you keep track of simulation data by letting you create filenames that are variants of input filenames. For example, with Spectre, you can

- Identify simulation data by date, time, process ID, or other defining characteristics in the results filenames
- Keep multiple circuits in a single directory without having subsequent simulations overwrite previous results

To do this, you set environment variables so that output filenames are automatically different variants of input filenames.

- Construct filenames at run time

This is convenient if your input data comes from several files. For example, you can use an `include` statement to insert several different circuit files into main input files that each contain analyses. Each circuit file can also be used with several stimulus files. To prevent confusion, you can create filenames at run time for the stimulus files that associate them with the appropriate main input files.

In this section, you will learn how to use the various Spectre features for creating filenames.

### Creating Filenames by Modifying Input Filenames

The Spectre simulator gives you predefined percent codes you can put in your filenames. These predefined codes let you construct filenames that add defining characteristics, such as date or time, to input filenames. You specify predefined percent codes with a percent character (%) followed by an uppercase letter. The uppercase letter tells the Spectre simulator

how to construct the filename. You can use percent codes in environment variables, in `spectre` command parameters, or in your netlist—wherever you need to specify filenames for simulation results.

For example, `%C` is the predefined percent code for the name of the input circuit file. If your circuit file is named `opamp1` and you place the following `-raw` setting for your UNIX environment variable

```
setenv SPECTRE_DEFAULTS "-raw %C.raw"
```

the Spectre simulator sends simulation results to the directory named `opamp1.raw`.

### Description of Spectre Predefined Percent Codes

These are the percent code that can help you organize your simulation data:

- |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>%A</code> | <code>%A</code> is replaced by the name of the current analysis that is running.<br><br>If it is specified in a device statement, it is expanded to a blank string because there is no current analysis.                                                                                                                                                                                                                                                                                           |
| <code>%B</code> | <code>%B</code> is replaced by <code>64bit</code> for 64-bit version of the software.                                                                                                                                                                                                                                                                                                                                                                                                              |
| <code>%C</code> | <code>%C</code> is replaced by the input circuit filename, as it is used in the command line. If the circuit filename is <code>opamp1</code> , the specification <code>%C.raw</code> generates a file named <code>opamp1.raw</code> .<br><br>When the Spectre simulator does not know the name of the input file, as when the circuit is read from the standard input (from a pipe or from a redirected file), the Spectre simulator substitutes the name <code>stdin</code> for <code>%C</code> . |
| <code>%D</code> | <code>%D</code> is replaced by the date when the program started. For example, the specification <code>%D.opamp1</code> might generate a file named <code>94-09-19.opamp1</code> .<br><br>The date is in year-month-day format. All leading zeros are included. This format generates filenames that you can sort alphabetically into chronological order.                                                                                                                                         |
| <code>%F</code> | <code>%F</code> is replaced by the completed analysis name. For example, if you have file named <code>mc1-005_dc1</code> , the specification <code>spectre_%F.dc</code> will expand to <code>spectre_mc1-005_dc1.dc</code> .                                                                                                                                                                                                                                                                       |
| <code>%H</code> | <code>%H</code> is replaced by the host name (network name) of the system on which the Spectre simulator is running.                                                                                                                                                                                                                                                                                                                                                                               |
| <code>%M</code> | <code>%M</code> is replaced by the current CMIVersion.                                                                                                                                                                                                                                                                                                                                                                                                                                             |

|    |                                                                                                                                                                                                                                                                                                                         |
|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| %P | <p>%P is replaced by the process ID.</p> <p>The process ID is a unique integer assigned to the Spectre process by the operating system.</p>                                                                                                                                                                             |
| %S | <p>%S is replaced by the simulator name. For example, the specification %S.opamp1 might generate a file named <code>spectre.opamp1</code>.</p> <p>If you use a different name or a symbolic link with a different name to access a copy of the executable program, the new name becomes the program name.</p>           |
| %T | <p>%T is replaced by the time when the program started. For example, the specification %T.opamp1 might generate a file named <code>14:44:07.opamp1</code>.</p> <p>Time is in 24-hour format, and all leading zeros are included. This format generates filenames that sort alphabetically into chronological order.</p> |
| %V | <p>%V is replaced by the simulator version string. For example, the specification <code>out_%V.raw</code> might generate a file named <code>out_1.0.2.raw</code>.</p>                                                                                                                                                   |
| %I | <p>%I is replaced by the installation directory.</p>                                                                                                                                                                                                                                                                    |
| %O | <p>%I is replaced by the operating platform.</p>                                                                                                                                                                                                                                                                        |
| %U | <p>%U is replaced by the username.</p>                                                                                                                                                                                                                                                                                  |
| %% | <p>This specifies the % character by itself.</p> <p>This option lets you use percent characters in filenames. Two percent characters (%%) in a filename specification produce a single percent character in the filename, which is not interpreted as a percent code indicator.</p>                                     |

The predefined percent codes feature does not perform recursive substitutions. For example, if you have an input file named `A%SD.xyz` and you create an output file with the percent code designation `%C.raw`, the Spectre simulator creates the output file `A%SDxyz.raw`. The Spectre simulator does not substitute the simulator name for %S in this case.

## Customizing Percent Codes

You can define your own percent codes or redefine existing codes with the `+%<X>` option of the `spectre` command. Names of customized percent codes can be any single uppercase or lowercase letter. You can define percent codes in two ways:

- You can define percent codes for a single simulation by typing this option into the command line with the `spectre` command at the start of the simulation.
- You can specify the customized percent code as a default by typing the `spectre` command into the `SPECTRE_DEFAULTS` environment variables.

For example, if you type in the following instruction at the command line

```
spectre +%E opamp1 test3
```

the Spectre simulator runs a simulation for circuit `test3`. During this simulation, the Spectre simulator substitutes the name `opamp1` for any `%E` it finds in results filename specifications.

You undefine customized percent codes with the `-%<X> spectre` command option. For example, if you customize percent codes with the `SPECTRE_DEFAULTS` environment variable, you might want to undefine them for a given simulation run. To do this, you include the `-%<X>` command line option in the `spectre` command that starts the simulation. Undefined percent codes return to predefined values. If an undefined percent code has no predefined value, it is treated like an empty string.

### Creating Filenames from Parts of Input Filenames

Colon modifiers (`:x`) create filenames from parts of input filenames. You can use colon modifiers with all percent codes except the `%%` code.

For example, if you apply `%C:r.raw` to the input filename `opamp.ckt`

- `%C` is the input filename (`opamp.ckt`)
- `:r` is the root of the input filename (`opamp`)
- `.raw` is the new filename extension

The result is the output filename `opamp.raw`. In this example, (`:r`) is the colon modifier.

### Definitions of Colon Modifiers

The Spectre simulator recognizes the following colon modifiers:

---

| Modifier        | Description                                                                        |
|-----------------|------------------------------------------------------------------------------------|
| <code>:r</code> | Signifies the root (base name) of the given path for the file                      |
| <code>:e</code> | Signifies the extension for the given path of the file                             |
| <code>:h</code> | Signifies the head of the given path for any portion of the file before the last / |
| <code>:t</code> | Signifies the tail of the given path for any portion of the file after the last /  |

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| Modifier | Description                                                                                                                                                       |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| : :      | Signifies the ( :) character itself; use two consecutive colons ( : : ) to place a single colon in an output filename that is not read as a percent code modifier |

Any character except a modifier after a colon ( :) signals the end of modifications. The Spectre simulator appends both the colon and the character to the filename.

The Spectre simulator applies a chain of colon modifiers in the sequence you specify them. For example, if you apply %C:e.%C:r:t to the input filename `/circuits/opamp.ckt`

%C:e is the extension (ckt) of the input filename

%C:r is the root (`/circuits/opamp`) of the input filename

:t is the tail of the input filename after the last / (`opamp.ckt`)

The result is the output filename `ckt.opamp`.

**Note:** If the input filename does not contain a slash and a period, the modifiers :t and :r return the whole filename, and the modifier :h returns a period.

### Examples of Colon Modifier Use

The following table shows the various filenames you can generate from an input filename (%C) of `/users/maxwell/circuits/opamp.ckt`:

| Colon Modifier | Comments                                                                       | Output Filename Result                          |
|----------------|--------------------------------------------------------------------------------|-------------------------------------------------|
| %C             | Input filename                                                                 | <code>/users/maxwell/circuits/opamp.ckt</code>  |
| %C:r           | Root of the input filename                                                     | <code>/users/maxwell/circuits/opamp</code>      |
| %C:e           | Extension of the input filename                                                | <code>ckt</code>                                |
| %C:h           | Head of the input filename                                                     | <code>/users/maxwell/circuits</code>            |
| %C:t           | Tail of the input filename                                                     | <code>opamp.ckt</code>                          |
| %C::           | Second colon is appended to the input filename and the end of the modification | <code>/users/maxwell/circuits/opamp.ckt:</code> |

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| Colon Modifier | Comments                                                                                                                                             | Output Filename Result |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|
| %C:h:h         | The head of %C:h (such a recursive use of :h might be useful if you want to direct your output to a different directory from that of the input file) | /users/maxwell         |
| %C:t:r         | The root of %C:t                                                                                                                                     | opamp                  |
| %C:r:t         | The tail of %C:r                                                                                                                                     | opamp                  |
| /tmp%C:t:r.raw | The suffix .raw is appended to the root of %C:t, and the full path is altered to put opamp.raw in the /tmp file.                                     | /tmp/opamp.raw         |
| %C:e.%C:r:t    | Extension of %C followed by the tail of %C:r                                                                                                         | ckt.opamp              |





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## Identifying Problems and Troubleshooting

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This chapter discusses the following topics:

- [Error Conditions](#) on page 958
- [Spectre Warning Messages](#) on page 960
- [Customizing Error and Warning Messages](#) on page 966
- [Controlling Program-Generated Messages](#) on page 977
- [Correcting Convergence Problems](#) on page 978
- [Correcting Accuracy Problems](#) on page 981
- [Packaging a Test Case for Shipment to Cadence](#) on page 982

## Error Conditions

Error conditions terminate a Spectre® circuit simulator run. If you receive any of the messages described in this section, you must fix the problem and rerun the simulation.

### Invalid Parameter Values That Terminate the Program

If you enter a parameter that causes the Spectre simulator to stop or puts a model in an invalid region, such as giving  $z0=0$  to a transmission line, the Spectre simulator sends you a message like this one and exits.

```
Error from spectre during hierarchy flattening.
t11: Value of 'z0' should be nonzero.
spectre terminated prematurely due to fatal error.
```

To run the simulation, you must change the parameter to an acceptable value.

### Singular Matrices

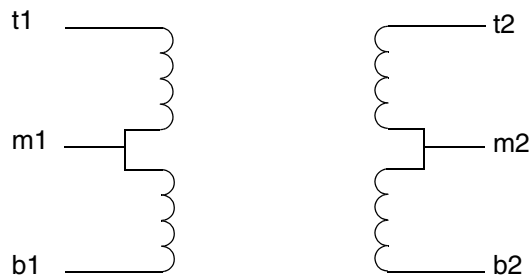
If you receive an error message that says a matrix is singular, your netlist contains either a floating node which is causing the problem or a loop of zero resistance branches, for example, a loop of voltage sources or inductors. The following procedures might help you find the problem:

- Check the `options` statement in your netlist to ensure that `topcheck=full` in at least one statement. The topology checker normally helps you identify singular matrix problems, but it cannot do so if it is disabled.
- If the error message appears only for particular components or circuit parameters or only for particular voltages or currents, try one of the following procedures:
  - ❑ Set `gmin=1e-12` (the default value).
  - ❑ If you are working with simplified semiconductor models, try using more complex models.

A CMOS (complementary metal oxide semiconductor) inverter whose model parameters have infinite output impedance in saturation demonstrates the usefulness of these techniques. When either the N- or P-type device is in the ohmic region, the solution is unique. However, when both devices are saturated, there is a range of output voltages that all satisfy Kirchhoff's Current Law. In this situation, the Newton-Raphson method forms a linearized circuit that is singular for that iteration.

- Check ideal transformers, N-ports, or transmission lines for floating nodes or loops of zero-resistance branches and modify the circuit to eliminate them.

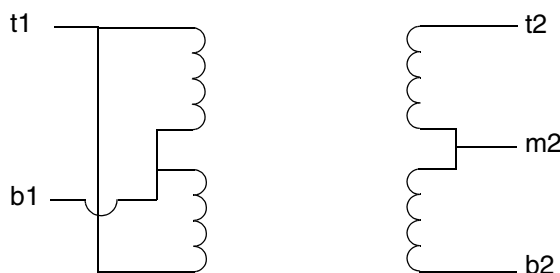
For example, consider this center-tapped transformer:



```
subckt ct_xfmr (t1 b1 t2 m2 b2)
 Tt t1 m1 t2 m2 transformer n1=2
 Tb m1 b1 m2 b2 transformer n1=2
end ct_xfmr
```

If you use this transformer and leave the center-tap terminal ( $m2$ ) floating, the Spectre simulator notifies you of a singular matrix. Because both  $m1$  and  $m2$  are floating, the DC solution is not unique.

If you choose a different topology for the transformer, like the one in the following example, you can avoid the problem.



```
subckt ct_xfmr (t1 b1 t2 m2 b2)
 Tt t1 b1 t2 m2 transformer n1=2
 Tb t1 b1 m2 b2 transformer n1=2
end ct_xfmr
```

Circuits that contain ideal transformers, N-ports, or transmission lines can have floating nodes or loops of zero-resistance branches because the topology checker cannot adequately verify these components. Finding these currents is difficult because all these components act like ideal transformers at DC. When you look into one port of a

transformer, you can see either a short or an open circuit, depending on what you see looking out of the other port.

### Internal Error Messages

If the Spectre simulator detects an internal error, it displays a message like one of the following:

```
Internal error detected by spectre. Please see http://support.cadence.com/wps/mypoc/cos?uri=deeplinkmin:COSHome for Customer Support contact information.
```

```
Error detected in file 'file.c' at line 101.
```

```
Internal error detected by spectre. Please see http://support.cadence.com/wps/mypoc/cos?uri=deeplinkmin:COSHome for Customer Support contact information.
```

```
Arithmetic exception.
```

Cadence can help you find solutions to these problems. If you get one of these messages, call Cadence Customer Support or contact a Cadence application engineer.

### Time Is Not Strictly Increasing

PWL takes a wave parameter that accepts time/value pairs. If the time value does not increase, the Spectre simulator displays the following message:

```
Error found in spectre during initial setup.
```

```
v10:time is not strictly increasing in waveform.
```

Check the PWL component to fix this error.

### Spectre Warning Messages

Warning messages tell you about conditions that might cause invalid results. Unlike error messages, warnings do not stop a simulation. When you receive a warning message, you must decide whether the particular condition creates a problem for your simulation. This section describes some common Spectre warning messages. It also tells you how to modify parameters to correct conditions that might produce invalid simulation results.

The Spectre simulator often prints warnings and notices that are eventually determined to be “uninteresting,” and there is a natural tendency after a while to ignore them. We recommend that you carefully study them the first few times you simulate a particular circuit and whenever the simulator gives you unexpected results.

## **P-N Junction Warning Messages**

Almost every semiconductor device includes at least one p-n junction. Normally, these p-n junctions are biased in a particular operating region. Three types of warning messages are available for each p-n junction, one for exceeding a maximum current, one for exceeding a melting current, and one for exceeding a breakdown voltage.

### **Explosion Region Warnings**

```
Warning from spectre at dc = 191 mA during DC analysis 'srcSweep'.
mos_mod: The bulk-drain junction current exceeds 'imelt'.
The results computed by Spectre are now incorrect because the junction
current model has been linearized.
```

Or

```
xram.d3247: The junction is melting (increase imax)
```

The Spectre simulator provides two parameters, `imax` and `imelt`, that limit the current across a PN junction. These parameters aid convergence and prevent numerical overflow. The junction characteristics of the device are assumed to be accurately modeled for current up to `imax`. If `imax` is exceeded during iterations, the linear model is substituted until the current drops below `imax` or until convergence is achieved. If convergence is achieved with the current exceeding `imax`, the results are inaccurate, and Spectre prints a warning similar to the first one above.

The `imelt` parameter is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. By default it is set to the value of `imax`. When any component of the junction current exceeds `imelt`, Spectre issues a warning and again the results become inaccurate. The junction current is linearized above the value of `imelt` to prevent arithmetic exceptions.

Both these parameters have current density counterparts, `jmax` and `jmelt`, that you can specify if you want the absolute current values to depend on the device area.

### **Melting Current Warnings**

A separate model parameter, `imelt`, is used as a limit warning for the junction current. This parameter can be set to the maximum current rating of the device. When any component of the junction current exceeds `imelt`, Spectre issues a warning and the results become inaccurate. The junction current is linearized above the value of `imelt` to prevent arithmetic exception, with the exponential term replaced by a linear equation at `imelt`.

## Breakdown Region Warnings

Messages like the following are breakdown region warnings:

```
D2: Breakdown voltage exceeded.
```

```
Q1: The collector-substrate voltage exceeded breakdown voltage.
```

The warning message identifies the relevant component name (D2 and Q1) and the affected junction.

The Spectre simulator issues breakdown region warnings only when you specify conditions for them. For information on setting parameters to identify a breakdown region, see [“Customizing Error and Warning Messages”](#) on page 332.

## Missing Diode Would Be Forward-Biased

```
Warning from spectre at time = 501.778 ns during transient analysis tran_to_1u.
```

```
i1.q0: Missing collector-substrate diode would be forward biased.
```

```
Notice from spectre at time = 510.1688 ns during transient analysis tran_to_1u.
```

```
i1.q0: Missing collector-substrate diode returns to normal bias condition.
```

Most p-n junctions in semiconductor models include both a resistive (the diode) and a capacitive (the junction capacitance) model. If the diode reverse saturation current is set to zero, the resistive part of the junction is turned off, and the Spectre simulator assumes that the resistive portion of the junction does not exist (but the junction capacitance may still be present). In this case, if the voltage across the missing diode is larger than  $10 * V_t$  (where  $V_t$  is the thermal voltage), Spectre will issue a warning message telling you that the junction, which is missing, will be forward biased. A follow-up notice is issued if, and when, the device returns to a normal bias condition.

## Tolerances Might Be Set Too Tight

When you simulate high-voltage or high-current circuits, the default tolerances might be tight enough to make convergence difficult or impossible. If you get a “Tolerances might be set too tight” message, try relaxing tolerances by increasing the value of `reltol`, `iabstol`, and `vabstol`.

## Parameter Is Unusually Large or Small

The Spectre simulator checks the parameter values to see if they are within a normal range of expected values. This check can catch data entry errors or identify situations that can cause the Spectre simulator to have difficulties simulating the circuit.

The “Parameter is unusually large or small” message issues a notice about a parameter value. The message looks like one of the following:

```
NPNbjt: 'rb' has the unusually small value of 1mOhms.
PNPbjt: 'tf' has the unusually large value of 1Gs.
OA1.Q16 of ua741: 'region' has the unusual value of rev.
```

If you receive such a message, check the parameter. If the unusual parameter value is correct, you can ignore this message.

The limits settings that generate these warning messages are soft limits, as opposed to hard limits settings. Hard limits stop a simulation if they are violated. the Spectre simulator has automatic soft limits on a few parameter values. However, you can override these limits or specify your own limits for parameters that do not have automatic limits. For more information, see [“Customizing Error and Warning Messages”](#) on page 332.

### gmin Is Large Enough to Noticeably Affect the DC Solution

```
Warning detected by spectre during DC analysis oppoint.
Gmin=1pS is large enough to noticeably affect the DC solution.
```

By default, the Spectre simulator (and SPICE) adds a very small conductance of  $10^{-12}$  siemens called `gmin` across nonlinear devices. This conductance prevents nodes from floating if the nonlinear devices are turned off. By default, `GMIN=1e-12 Siemens`. The `gmin` parameter usually has a minimal effect on circuit behavior. However, some circuits, such as charge storage circuits are very sensitive to the small currents that flow through `gmin`.

You see a message such as the one given above if the current flowing through the `gmin` conductors, when treated as an error current, does not meet the `gmin` criteria. That is, the message is displayed if the current that enters any node from all attached `gmin` conductors is larger than either `iabstol` or `reltol` multiplied by the sum of the absolute value of the individual currents that enter the node.

If your circuit is not sensitive to small leakage currents, you can ignore this message. If your circuit is sensitive to these currents, reduce the `gmin` value or set it to zero.

### Minimum Timestep Used

If this problem occurs, the analysis continues, and a warning message is displayed at each time point that does not meet the convergence criteria. In the Spectre simulator, this is very rare, but it does occur. Occasionally, this needs to be remedied to get the correct solution.

1. Make sure devices have junction and overlap capacitance specified.
2. Increase `maxiters`, but do not go higher than 200.

3. Change to the `gear2` or `gear2only` method of integration.
4. Reduce other occurrences of the local truncation error cutting the timestep. Increase `lteratio` and increase the absolute error tolerances `vabstol` and `iabstol`. Do not go too high with any of these.
5. Combine 2, 3, and 4 and set `cmin` to prevent instantaneous change at every node in the circuit.
6. Relax `reltol` in combination with 5.

### Syntax Errors

Warning from spectre in indab\_7 during circuit read-in:

```
na300.scs" 27: `c11': Encountered statement in Spectre format while in Spice language mode. This will not be supported in a future release.
```

The Spectre parser is dual mode and accepts both the Spectre native language and documented Spice2G6. The default for the Spectre simulator is SPICE. If you include a file written in Spectre native syntax, you must either specify simulator `lang=spectre` or name the file with a `.scs` suffix. After Spectre processes the file, it reverts to the default mode. It is illegal to include Spectre syntax in the SPICE mode or vice versa.

For the MOS instance line given below:

```
M1 1 2 0 0 NCH W= 10u L= 2u
```

Spectre displays the following warning:

```
m1: Encountered statement in Spectre format while in SPICE language mode. This will not be supported in a future release.
```

Since the instance statement is valid in both languages, you can ignore this warning.

### Topology Messages

Notice from spectre during topology check.

Only one connection to the following node:

```
4
```

```
No DC path from node `4' to ground, Gmin installed to provide path.
```

The Spectre topology checker identifies floating nodes and automatically inserts a `gmin` resistor (1e12 Ohms) to prevent a non-isolated solution. The Spectre simulator then displays a message telling you what it did.



## Model Parameter Values Clamped

Warning from spectre during initial setup.

```
n: The value of `vj(pb)' at T = 25 C is 50e-03 V, which is too small.
```

```
Clamped to 0.1 V.
```

```
n: The value of `vj(pb)' at T = 27 C is 41.7617e-03 V, which is too small.
```

```
Clamped to 0.1 V.
```

The Spectre simulator clamps model parameter values to prevent numerical difficulties during simulation. When clamping is completed, Spectre displays a message indicating that it is using clamped values. There is no way to disable these clamps.

## Invalid Parameter Warnings

Warning from spectre during circuit read-in.

```
`pchmod': `tox' is not a valid parameter for `bsim4' models.
```

```
`pchmod': `nch' is not a valid parameter for `bsim4' models.
```

This type of warning is issued any time you specify an invalid parameter in a model definition. The models included with Spectre have predefined model parameters. For more information, see `spectre -h`.

Only these predefined parameters can be used within a model definition. The Spectre circuit simulator issues similar warnings for invalid instance and subcircuit parameters.

## Redefine Primitives Messages

Warning from spectre in `q2' during circuit read-in.

```
"redefPrim.scs" 6: `q2.resistor' redefines the primitive named `resistor
```

Spectre displays this message if you define a model or subcircuit with the same name as a built-in primitive device.

The following message tells you that the local definition will override the built-in definition:

```
model resistor bjt
```

```
q1 1 2 3 resistor
```

q1 is considered a bjt device rather than a resistor.

## Initial Condition Messages

Notice from spectre during IC analysis, during transient analysis 'tran1'.

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Initial condition computed for node 2 is in error by 755.152 uV. To reduce error in computed initial conditions, decrease `rforce`. However, setting rforce too small may result in convergence difficulties or in the matrix becoming singular.

The Spectre simulator sets initial conditions on a node by attaching a voltage source through a resistor. The default value of this resistor is 1, but you can control the value through the options parameter `rforce`. This notice indicates that the initial condition calculated for this node is about 755uV from the value specified in the netlist. You can lower the value of `rforce` to bring the voltage values into agreement in one of the following ways:

- Through the Analog Options window in the Analog Design Environment.
- Inserting an options statement in the netlist. An example is given below:

```
myOptions options rforce=1m
```

### Output Messages

Notice from spectre during transient analysis 'tran1'.  
No outputs found. Loosening output filter criterion to 'lvlpub'.

If you set `save=selected`, the Spectre simulator saves the voltages in the save statement. If the save statement does not contain any voltage values, Spectre issues the above warning and changes the `save` option default to `lvlpub`. This saves all node voltages.

### Log File Messages

Warning from Spectre during generation of log file.  
`opt1 options warning_limit=number warning_id = [message_type_1 message_type_2]`

For example,

```
opt1 options warning_limit=3 warning_id = [SFE-30 CMI-2151]
```

IN the statement, 3 is the number of messages allowed for printing in log file for each message type defined in `warning_id`.

SFE-30 and CMI-2151 are the user-defined message types for printing in the log file.

## Customizing Error and Warning Messages

You can customize the Spectre error and warning messages to some extent to fit the needs of a simulation. This section tells you about these customization options.

## Selecting Limits for Parameter Value Warning Messages

You can accept Cadence default soft limits that determine when you receive warning messages about parameter values, or you can enter your own limits. You can also control which parameters the Spectre simulator checks. This section gives you instructions for all.

### Accepting Cadence Range Limits Defaults

The most convenient option for deciding which warning messages you receive is to accept Cadence Range Limits Defaults. The Cadence defaults are located in `your_install_dir/tools/spectre/etc/limits/range.lmts`, and you can examine them to see if they meet your needs. You can enter Cadence defaults with the `SPECTRE_DEFAULTS` environment variable in your shell initialization file (such as `.profile` or `.cshrc`). The entry in your shell initialization file looks like the following:

```
setenv SPECTRE_DEFAULTS "+param $HOME/tools/dfII/etc/
spectre/range.lmts"
```

With this entry in the shell initialization file, the Spectre simulator reads parameter limits from `your_install_dir/tools/spectre/etc/limits/range.lmts`.

You can override a `SPECTRE_DEFAULTS` setting with the `param` option of the `spectre` command. Specifying `+param` as a command line argument overrides `+param` in `SPECTRE_DEFAULTS` and tells the Spectre simulator to read range limits from the file you specify. Specifying `-param` tells the Spectre simulator to ignore the `+param` given in `SPECTRE_DEFAULTS` without giving the Spectre simulator a new location to find range limits.

**Note:** For more information about Spectre defaults, see the [Spectre Circuit Simulator Reference](#) manual and “Customizing Percent Codes” on page 318.

### Creating a Parameter Range Limits File

In some circumstances, you might want to set your own parameter limits for warning messages. This might be the case, for example, if you are maintaining your own sets of model libraries. If you want to choose your own parameter limits for warnings, you must use a text editor to create a parameter range limits file.

A parameter range limits file requires the following syntax. Fields enclosed by single brackets (`[]`) are optional.

```
[ComponentKeyword] [model] [LowerLimit <[=]]
[[]Param[]] <[=] UpperLimit]
```

Observe the following syntax rules for a parameter limits file:

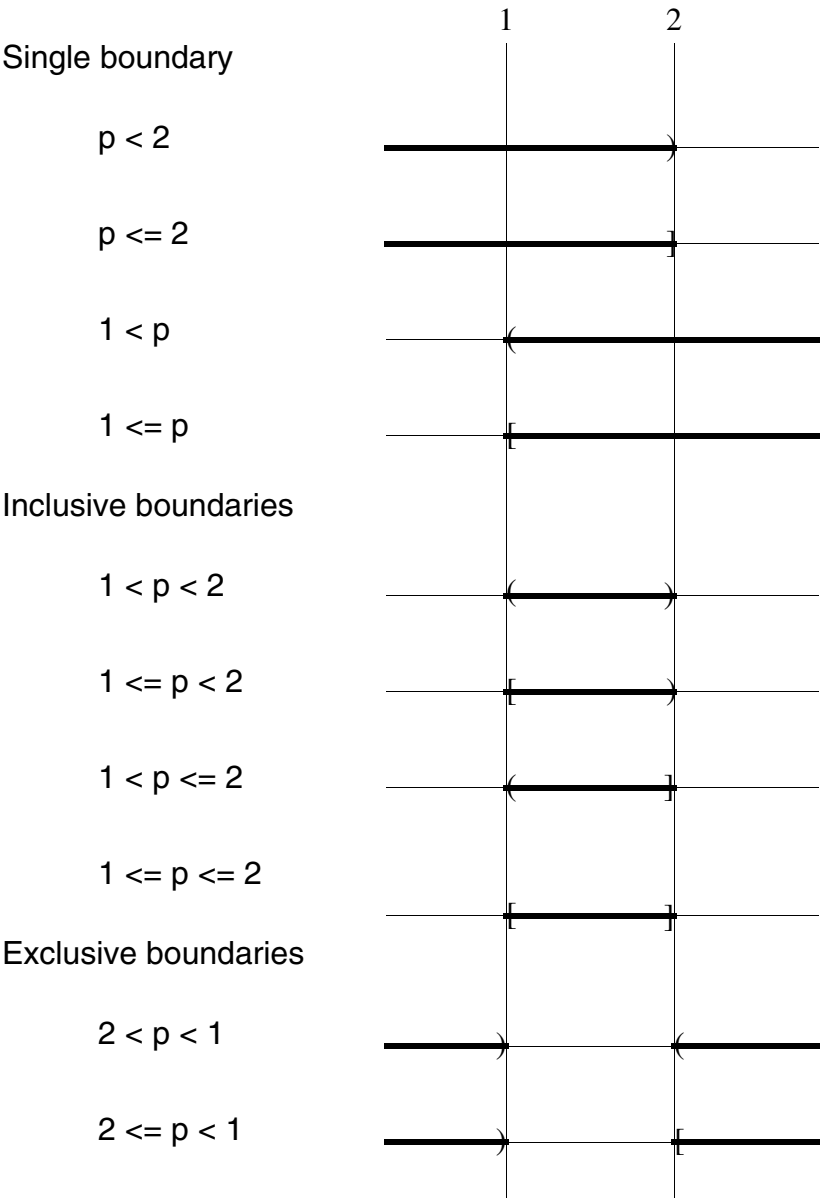
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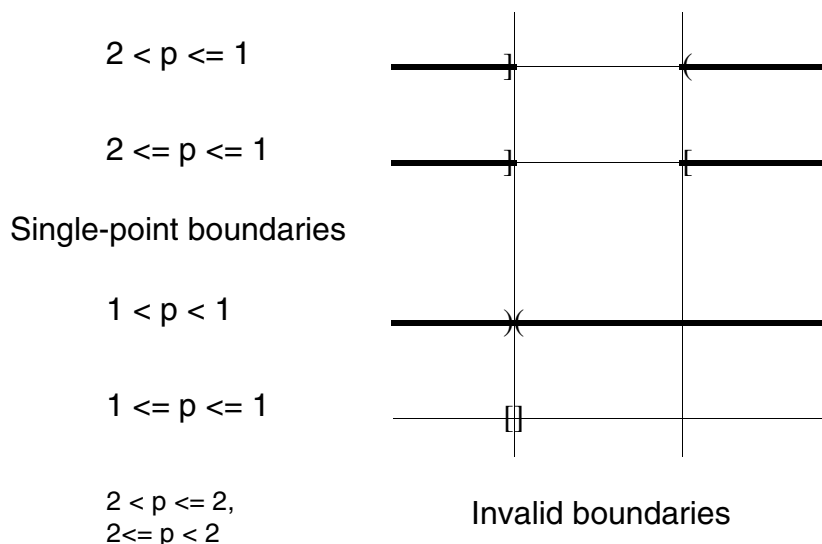
- You can specify limits for input, output, or operating-point parameters for either component instances or models. You can also specify limits for analysis parameters.
- You must specify the limits for each parameter on a single line.
- You can specify open bounds using angle brackets (<) or closed bounds using an angle bracket with an equal sign (<=). If you specify closed bounds, there can be no space between < and =.
- You can specify inclusive or exclusive ranges. If you specify exclusive ranges, the upper limit must be smaller than the lower limit.

The diagram on the following pages shows you the proper formats for range specifications.

Examples of Range Limits Specifications



## Examples of Range Limits Specifications (*continued*)



- The component keyword must be a Spectre name, not a name used for SPICE compatibility. For example, use `mos3` rather than `mos`.
- If you specify more than one parameter limit for a component, you need to specify the component keyword only once. The Spectre simulator assumes the keyword is unchanged from the previous parameter unless you specify a new component keyword.
- If you give a parameter limit more than once, your last instructions override previous limits.
- If you mention a parameter but give it no limits, all limits are disabled for that parameter.
- You can specify limits for integer, real, or enumerated parameters. Enumerated parameters are those that take only predefined values (such as `yes` or `no` and `all` or `none`).

To specify limits on enumerated parameters, use the index of the enumeration in the limits declaration for that parameter. To find the index of a parameter of component `name`, see the parameter listings for the component `name` in the Spectre online help (`spectre -h`) and count the enumerations in the limits declaration starting from zero.

For example, to specify that the BJT operating-point parameter `region` should not be `rev` (reversed), look for the `region` parameter in the parameter listings for the BJT component. The `region` parameter is described as follows:

`region=fwd`      Estimated operating region. Possible values are `off`, `fwd`, `rev`, or `sat`.

For this parameter, `off` has index 0, `fwd` has index 1, `rev` has index 2, and `sat` has index 3. To specify a limit that notifies you if any BJT is reversed, use either of the following specifications:

```
2 < region < 2
```

or

```
3 <= region <= 1
```

- You must give the keyword `model` when you place limits on model parameters. If you do not give the keyword `model`, the limits are applied to instance parameters.
- You can indicate upper or lower limits for the absolute value of a parameter with the vertical line character (`|vto|`).

For example,

```
resistor 0.1 < |r| < 1M
```

specifies that the absolute value of `r` should be greater than 0.1 ohm and less than 1 megohm. There can be no spaces between the absolute value symbols and the parameter name.

- You currently cannot place limits on vector parameters.
- You can write parameter limits using Spectre native-mode scale factors. For example, you can write the limit

```
f <= 1.0e6
```

as

```
f <= 1M
```

### Example of a Parameter Range Limits File

This example shows a parameter limits file with correct syntax.

```
mos3 0.5u <= 1 <= 100u
 0.5u <= w
 0 < as <= 1e-8
 0 < ad <= 1e
```

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```
model |vto| <= 3
```

You can find the parameter names (*l*, *w*, *as*, *ad*, *vto*) and component keywords (*mos3*) in the parameter listings in the Spectre online help (`spectre -h`). This example instructs the Spectre simulator to accept without warnings *mos3* components for these conditions:

- If channel length is more than or equal to 0.5  $\mu\text{m}$ , or less than or equal to 100  $\mu\text{m}$
- If channel width is greater than or equal to 0.5  $\mu\text{m}$
- If the area of source diffusion is greater than 0, or less or equal to  $1\text{e-}8\text{ m}^2$
- If the area of drain diffusion is greater than 0, or less or equal to  $1\text{e-}8\text{ m}^2$
- If the *mos3* model parameter *vto* (the threshold voltage at zero body bias) has an absolute value less than or equal to 3

### Entering a Parameter Range Limits File

You can enter a parameter range limits file in two ways:

- Type the `+param <filename>` option of the `spectre` command from the command line or place it in an environment variable. *<filename>* is the name of the parameter range limits file. In the following example, *limits3* is the range limits file for this simulation of *test.circuit*.

```
spectre +param limits3 test.circuit
```

- Read the parameter limits file from within another file by putting an `include` statement with a syntax like the following example in your netlist.

```
include "filename"
```

*filename* is the name you give to the range limits file.

You can nest `include` statements. The only limit on depth is that imposed by the operating system on the number of files that can be open simultaneously in the Spectre simulator.

Paths you specify in filenames refer to the directory that contains the current file, not to the directory in which the Spectre simulator was started. For example, suppose your directory tree is set up as follows

```
design1/ckt1
design1/param.lmts
design1/resistor.lmts
design2/ckt2
design2/param.lmts
design2/resistor.lmts
```



and you run the Spectre simulator in `design1` with the following `spectre` command:

```
spectre +param ../design2/param.lmts ckt1
```

If the file `design1/param.lmts` contains the line

```
include "resistor.lmts"
```

the Spectre simulator reads in the `design2/resistor.lmts` file, but not the `design1/resistor.lmts` file.

### Requesting Breakdown Region Warnings for Transistors

If you want warning messages about the breakdown regions of transistors, you must set the appropriate parameters for each component when you identify the component with an `instance` or `model` statement. For most transistors, you set the `bvj` parameter.

For BJTs, you must set three parameters: `bvbe`, `bvbc`, and `bvsub`. These are breakdown parameters for the base-emitter, the base-collector, and the substrate junctions.

Diodes are also exceptions because you can set both the `bvj` and `bv` parameters. You need two different parameters for the diode breakdown voltage because of the Zener breakdown model in the diode. When you use the diode as a Zener diode, it is purposely biased in the breakdown region, and you do not want to be warned about the Zener breakdown. By specifying the `bv` parameter, you tell the Spectre simulator to implement the Zener diode model at `bv`.

### Telling Spectre to Perform Additional Checks of Parameter Values

You can perform a `check` analysis at any point in a simulation to be sure that the values of component parameters are reasonable. You can perform checks on input, output, or operating-point parameters. The Spectre simulator checks parameter values against parameter soft limits. To use the `check` analysis, you must also enter the `+param` command line argument with the `spectre` command to specify a file that contains the soft limits.

The following example illustrates the syntax of the `check` statement. It tells the Spectre simulator to check the parameter values for instance statements.

```
ParamChk check what=inst
```

- `ParamChk` is your unique name for this `check` statement.
- The keyword `check` is the component keyword for the statement.
- The `what` parameter tells the Spectre simulator which parameters to check.

The `what` parameter of the `check` statement gives you the following options:

| Option                | Action                                                               |
|-----------------------|----------------------------------------------------------------------|
| <code>none</code>     | Disables parameter checking.                                         |
| <code>models</code>   | Checks input parameters for all models only.                         |
| <code>inst</code>     | Checks input parameters for all instances only.                      |
| <code>input</code>    | Checks input parameters for all models and all instances.            |
| <code>output</code>   | Checks output parameters for all models and all instances.           |
| <code>all</code>      | Checks input and output parameters for all models and all instances. |
| <code>oppooint</code> | Checks operating-point parameters for all models and all instances.  |

### Selecting Limits for Operating Region Warnings

The Spectre simulator lets you specify forbidden operating regions for transistors. If a transistor operates in a forbidden operating region, the Spectre simulator sends you a warning message. This feature is available for BJTs, MOSFETs, JFETs, and GaAs MESFETs.

### Specifying Forbidden Operating Regions for Transistors

You specify a forbidden operating region in a transistor with the `alarm` parameter. The `alarm` parameter gives you the following options:

| Option              | Description                                                                          |
|---------------------|--------------------------------------------------------------------------------------|
| <code>none</code>   | The default condition with no warnings issued.                                       |
| <code>off</code>    | Warns if the transistor is turned off.                                               |
| <code>triode</code> | Warns if the transistor operates in the triode region (available for MOSFETs).       |
| <code>sat</code>    | Warns if the transistor operates in the saturation region.                           |
| <code>subth</code>  | Warns if the transistor operates in the subthreshold region (available for MOSFETs). |
| <code>fwd</code>    | Warns if the transistor is forward-biased (available for BJTs).                      |

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| Option | Description                                |
|--------|--------------------------------------------|
| rev    | Warns if the transistor is reverse-biased. |

For example, to be sure that a group of MOSFETs always operates in the saturation region, you enter this `model` statement:

```
model mos_example nmos alarm=off alarm=triode
 alarm=subth
```

Each of the three `alarm` parameters in this example identifies a forbidden operating condition. Operating the device anywhere except in the saturation region triggers a warning. The warning looks like the following:

```
Warning detected by spectre during transient analysis 'timesweep'.
M1: Device operated in the triode region.
```

### Defining BJT Operating Regions

The Spectre simulator provides two parameters, `vbefwd` and `vbcfwd`, that let you specify the boundaries between BJT operating regions. The default value for each parameter is 0.2 volts.

The following table shows you the criteria the Spectre simulator uses to determine BJT operating regions.

| Region     | Bias Conditions                               |
|------------|-----------------------------------------------|
| off        | $V_{be} \leq vbefwd$ and $V_{bc} \leq vbcfwd$ |
| saturation | $V_{be} > vbefwd$ and $V_{bc} > vbcfwd$       |
| forward    | $V_{be} > vbefwd$ and $V_{bc} \leq vbcfwd$    |
| reverse    | $V_{be} \leq vbefwd$ and $V_{bc} > vbcfwd$    |

### Range Checking on Subcircuit Parameters

You can test the value of subcircuit parameters with the `paramtest` component. If the parameters meet your testing criteria, you can print an informational message, print a warning, or print an error message and terminate the program.

## Formatting the paramtest Component

The `paramtest` component has the following format:

*Name* `paramtest` *parameter=value...*

- *Name* is your unique name for this `paramtest` component.
- The keyword `paramtest` is the component keyword for the component.
- The parameters specify the tests that are applied to the parameters, the action taken if parameters satisfy the test conditions, and the text of the message that is printed when parameters satisfy the test conditions.

## Rules and Guidelines to Remember

- If you specify more than one test, the conditional action is taken if any test passes.
- If you use the `paramtest` component without specifying test conditions, the specified actions are taken, and the message is printed unconditionally. This option is useful for using the `paramtest` component with the `if` statement. The `paramtest` instruction can be followed whenever a given `if` statement option is executed.

## The paramtest Options

The following table explains the possible `paramtest` options.

| Parameter             | Instruction                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>printif</code>  | Informational message is printed if test condition is satisfied.                                                                                                                                                                                                                                                                                                                                                                                                |
| <code>warnif</code>   | Warning is printed if test condition is satisfied.                                                                                                                                                                                                                                                                                                                                                                                                              |
| <code>errorif</code>  | Program quits and error message is printed if testing condition is satisfied.                                                                                                                                                                                                                                                                                                                                                                                   |
| <code>message</code>  | Parameter value is the message text.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <code>severity</code> | You set this parameter when you use <code>paramtest</code> without a test condition. It specifies the type of message printed and the action to be taken, if any. The possible values are <code>debug</code> , <code>status</code> , <code>warning</code> , <code>error</code> , and <code>fatal</code> . If you specify <code>error</code> , the current analysis quits with an error message. If you specify <code>fatal</code> , the whole simulation stops. |

## A paramtest Example

This example uses three consecutive `paramtest` statements to check the values of four parameters—`l`, `w`, `ls`, and `ld`. If a parameter value satisfies a test condition, one of three different warning messages is printed:

```
TooShort paramtest warnif=(l < 1um) \
 message="Channel length for nmos must be greater than 1u."
TooThin paramtest warnif=(w < 1um) \
 message="Channel width for nmos must be greater than 1u."
TooNarrow paramtest warnif=(ls < 1um) warnif=(ld < 1um) \
 message="Strip width for nmos must be greater than 1u."
```

## Controlling Program-Generated Messages

The Spectre simulator normally sends error, warning, and informational messages to the screen. To prevent confusion, the Spectre simulator limits the amount of material it sends to the screen. You can, however, get a more complete printout of messages if you send the messages to a log file that you can generate with the `spectre` command or in a `SPECTRE_DEFAULTS` environment variable.

## Specifying Log File Options

You can choose from among the following command line options:

- |                                |                                                                                                                                                                                                    |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>+log &lt;file&gt;</code> | The Spectre simulator sends all messages to a log file as well as printing to the screen. You specify the name for the file. You can use <code>+l</code> as an abbreviation of <code>+log</code> . |
| <code>=log &lt;file&gt;</code> | The Spectre simulator sends all messages to a log file but does not print to the screen. You specify the name for the file. You can use <code>=l</code> as an abbreviation of <code>=log</code> .  |
| <code>-log</code>              | The Spectre simulator does not create a log file. You can use <code>-l</code> as an abbreviation of <code>-log</code> . This is the default option.                                                |

## Command Line Example

The following entry on the command line runs a simulation for circuit `smps.circuit` and sends all messages to a log file named `smps.logfile`:

```
spectre =log smps.logfile smps.circuit
```

## Setting Environment Variables

If you specify log file options in a `SPECTRE_DEFAULTS` environment variable, you might want to name log files according to some system that helps you keep track of log files from different simulations. Spectre predefined percent codes are useful for this. The following example uses the predefined percent code `%C` to create log filenames based on the input filename. If you run a simulation for `smps.circuit`, the Spectre simulator creates a log file named `smps.circuit.logfile`. You place the `SPECTRE_DEFAULTS` environment variable in the `.cshrc` or `.profile` files.

```
setenv SPECTRE_DEFAULTS "=log %C.logfile"
```

For more information about predefined percent codes and the `SPECTRE_DEFAULTS` environment variable, see [Chapter 13, “Managing Files.”](#)

## Suppressing Messages

There are also `spectre` command options that let you print or suppress error, warning, or informational messages:

|                       |                                       |
|-----------------------|---------------------------------------|
| <code>+error</code>   | Prints error messages                 |
| <code>-error</code>   | Does not print error messages         |
| <code>+warning</code> | Prints warning messages               |
| <code>-warning</code> | Does not print warning messages       |
| <code>+info</code>    | Prints informational messages         |
| <code>-info</code>    | Does not print informational messages |

As a default, the Spectre simulator prints all these messages.

## Correcting Convergence Problems

In this section, you will learn about procedures that can help you if a simulation does not converge.

### Correcting DC Convergence Problems

If you have DC convergence problems, these suggestions might help you. Simple solutions generally precede more radical or complex measures in the list.

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- Evaluate and resolve any warning or error messages.
- Check for circuit connection errors. Check to see that the polarity and value are correct for independent sources. Check to see if the polarity and multiplier are correct for controlled sources.
- Try all of the homotopy methods (`gmin`, `source`, `ptran`, and `dptran`). These are tried by default.
- Check for an incorrect estimated operating region. The default estimated operating region in the Spectre simulator is on in the forward region for all devices. If there are a reasonable number of devices that are really off, set them off in the schematic. For a large number of devices, this might not be practical.
- Check for extremely high gain circuits with nonlinearities and feedback. The convergence criteria are applied to all nodes in the circuit. The output of the gain block meets Kirchhoff's Current Law and  $\delta(\text{reltol} \cdot V)$  about 1 part in  $10^3$  by default. Because of the gain, the input must move by this value divided by the gain. If the gain is high (for example,  $10^8$ ), the input must move less than 1 part in  $10^{11}$ . This is an extremely small motion from iteration to iteration that might not be achievable. If the gain is even higher, the numerical resolution of the machine might be approached. About 15 digits of resolution is available in a 64-bit floating-point number. In this case, the gain needs to be reduced.

**Note:** In this case, one node (the output) controls convergence, and all the other nodes are more accurate than the convergence criteria by itself would predict. This is typical for most circuits.

- Enable the topology checker (set `topcheck=full` on the `options` statement) and pay attention to any warnings.
- Increase `maxiters` for the DC analysis.
- If you have convergence problems during a DC sweep, reduce the step size.
- Check for unusual parameter values using the parameter range checker (add `+param param-limits-file` to the `spectre` command line arguments) and pay attention to any warnings.

Print out the minimum and maximum parameter values by placing an `info` statement in the netlist. Make sure that the values for the instance, model, output, temperature-dependent, and (if possible) operating-point parameters are reasonable.

- Avoid using very small floating resistors, particularly small parasitic resistors in semiconductors. Use voltage sources or `iprobe`s to measure currents instead. Small floating resistors connected to high impedance nodes can cause convergence difficulties. `rbm` in the bipolar model is especially troublesome.

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- If the `minr` model parameter is set, make certain it is set to 1 mOhm or larger.
- Use realistic device models. Make sure that all component parameters are reasonable, particularly nonlinear device model parameters.
- Increase the value of `gmin` with the `options` statement.
- Loosen tolerances, particularly absolute tolerances such as `iabstol` (on the `options` statement).
- Simplify the nonlinear component models. Try to avoid regions in the model that might cause convergence problems.
- When you have a solution, write it to a nodeset file using the `write` parameter. When you run the simulation again, read the solution back in using the `readns` parameter in the `dc` statement.
- If this is not the first analysis, the solution from the previous analysis might be an inadequate solution estimate because it differs too much from the solution for the current analysis. If this is so, set `restart=yes`.
- If you have an estimate of the solution, use nodeset statements or a nodeset file to set as many nodes as possible.
- If using nodesets or initial conditions causes convergence difficulties, try increasing `rforce` with the `options` statement.
- If you are simulating a bipolar analog circuit, make sure the region parameters on all transistors and diodes are set correctly.
- If the analysis fails at an extreme temperature but succeeds at room temperature, try adding a DC analysis that sweeps temperature. Start at room temperature, sweep to the extreme temperature, and write the last solution to a nodeset file.
- Use numeric pivoting in the sparse matrix factorization. Set `pivotdc=yes` with the `options` statement. Sometimes you must also increase the pivot threshold to between 0.1 to 0.5 by resetting the `pivrel` parameter with the `options` statement.
- Divide the circuit into pieces and simulate them individually. Make sure that results for a part alone are close to results for that part combined with the rest of the circuit. Use the results to create nodesets for the whole circuit.
- Try replacing the DC analysis with a transient analysis. Modify all the independent sources to start at zero and ramp to the independent source DC values. Run the transient analysis well beyond the time when all the sources have reached their final values. Write the final point to a nodeset file.

You can make this transient analysis more efficient with one of the following procedures:



- ❑ Set the integration method to backward-Euler (`method=euler`).
- ❑ Loosen the local truncation error criteria by increasing `lteratio` to 50 or more.

Occasionally, an oscillator in the circuit causes the transient analysis to terminate or work very slowly.

### Correcting Transient Analysis Convergence Problems

You can use two approaches to eliminate transient analysis convergence problems. The first strategy is to reduce the effect of discontinuities in nonlinear capacitors. The second method is to eliminate discontinuous jumps in the solution. Try the following suggestions if you have difficulty with transient analysis convergence:

- Use a complete set of parasitic capacitors on nonlinear devices to avoid jumps in the solution waveforms. Specify nonzero source and drain areas on MOS models.
- Use the `cmin` parameter to install a small capacitor from every node in the circuit to ground. This usually eliminates any jumps in the solution.
- If you can identify a nonlinear capacitance that might have a discontinuity, simplify the nonlinear capacitor model. If you cannot actually simplify the model, modifying it might help convergence.
- As a last resort, relax the tolerance values for the `lteratio` or `reltol` parameters and widen transitions in the stimulus waveforms.

### Correcting Accuracy Problems

If you need greater accuracy from a Spectre simulation, the most common solution is to tighten the `reltol` parameter of the `options` or `set` statements. In addition, be sure that the absolute tolerance parameters, `vabstol` and `iabstol`, are set to appropriate values. If tightening `reltol` does not help or if it greatly slows the simulation, try the additional suggestions in the following sections.

### Suggestions for Improving DC Analysis Accuracy

- Be sure there are no errors in the circuit. Use the computed DC solution and the operating point to debug the circuit. Check the topology, the component parameters, the models, and the power supplies.
- Be sure you are using appropriate models and that the model parameters are consistent and correct.

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- If the circuit might have more than one solution, use `nodeset` statements to influence the Spectre simulator to compute the solution you want.
- Be sure that `gmin` is not influencing the solution. If possible, set `gmin` to 0 (in an `options` or `set` statement).

### Suggestions for Improving Transient Analysis Accuracy

- Verify that the circuit biased up properly. If it did not, there might be a problem in the topology, the models, or the power supplies.
- Be sure you are using appropriate models and that the model parameters are consistent and correct. Check the operating point of each device.
- Set the transient analysis parameter `errpreset` to `conservative`.
- If there is a charge conservation problem, use only charge-conserving models if you are not already doing so. Then tighten `reltol` to increase accuracy. (With the Spectre simulator, only customer-installed models might not be charge conserving.)
- Be sure that `gmin` is not influencing the solution. If possible, set `gmin` to 0 (in an `options` or `set` statement).
- If a solution exhibits point-to-point ringing, set the integration method in the transient analysis to Gear's second-order backward-difference formula (`method=gear2only`).
- If a low-loss resonator exhibits too much loss, set the integration method in the transient analysis to the trapezoidal rule (`method=traponly`).
- If the initial conditions used by the Spectre simulator are not the same as the ones you specified, decrease the `rforce` parameter in the `options` or `set` statements until the initial conditions are correct.
- If the Spectre simulator does not accurately follow the turn-on transient of an oscillator, set the `maxstep` parameter of the transient analysis to one-tenth the size of the expected period of oscillation or less.

### Packaging a Test Case for Shipment to Cadence

The `mmsimpack` utility, shipped with the SPECTRE release, enables you to create a compressed tar file containing all input files required for a test case. If a test case needs to be sent to Cadence for discussing and resolving Spectre simulation problems, the utility can be used to create the required file set, and to ship the case to Cadence.

To create a compressed tar file, perform the following steps:

1. Run a regular Spectre simulation to create a Spectre log file which reports all the files being read during parsing. Since, for this job, only the parsing is of relevance, the transient time may be shorted to accelerate the process.
2. Use the `mmsimpack` utility to create the compressed tar file, as follows:

```
% mmsimpack logfile -pack <packdir> [-filter <filter_file>]
```

Where

`pack <packdir>` specifies the directory where you want to save the packed netlist.

`-filter <filter_file>` (Optional) is a user-defined filter. The files that match the pattern in the filter file are not packed. The format of `filter_file` should be a regular expression.

`-copy_only` (Optional) Copy only the input netlist files and do not replace the absolute path in the netlist. This can reduce the `mmsimpack` runtime, however, the netlist might not run at another location because of the path issue.

`-h` displays the help information.

### Example

```
% spectre +aps mult16.scs +log mult16.out
% mmsimpack mult16.out -pack packngo
```

The above example will create a file called `SendMe.tar.gz` in the directory `packngo`. The `SendMe.tar.gz` file contains all the files required for running Spectre on the `mult16.scs` test case.



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## Example Circuits

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This appendix contains example netlists for testing the BSIM3v3 standard model.

- [Notes on the BSIM3v3 Model](#) on page 986
- [Spectre Syntax](#) on page 986
- [SPICE BSIM 3v3 Model](#) on page 986
- [Spectre BSIM 3v3 Model](#) on page 987
- [Ring Oscillator Spectre Deck for Inverter Ring with No Fanouts \(inverter\\_ring.sp\)](#) on page 987
- [Ring Oscillator Spectre Deck for Two-Input NAND Ring with No Fanouts \(nand2\\_ring.sp\)](#) on page 989
- [Ring Oscillator Spectre Deck for Three-Input NAND Ring with No Fanouts \(nand3\\_ring.sp\)](#) on page 990
- [Ring Oscillator Spectre Deck for Two-Input NOR Ring with No Fanouts \(nor2\\_ring.sp\)](#) on page 992
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- [Opamp Circuit \(opamp.cir\)](#) on page 995
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- [Modified Open-Loop Opamp \(openloop1.sp\)](#) on page 996
- [Example Model Directory \(q35d4h5.modsp\)](#) on page 996

## Notes on the BSIM3v3 Model

The Spectre® circuit simulator supports the standard BSIM 3v3 MOS model (both BSIM 3v3.1 and BSIM 3v3.2) as published by the University of California at Berkeley. Further information about this model can be obtained by using Spectre's online help by typing `spectre -h bsim3v3` at the command line or by consulting the BSIM3 home page at

[www-device.eecs.berkeley.edu/~bsim3/index.html](http://www-device.eecs.berkeley.edu/~bsim3/index.html)

Spectre does not add proprietary parameters to its implementation of the standard model.

## Spectre Syntax

Notes explaining Spectre syntax are included as comments throughout the example netlists.

The Spectre circuit simulator reads Spice2G6 input along with its own native format. The model card can therefore be specified in either format. Below is an example of each. Note that the valid parameter list does not change, only the primitive name, level designation, and version/type parameters.

Beginning with the 4.4.3 release, the Spectre simulator is compatible with SPICE input language beyond documented SPICE2G6. Contact your local Cadence representative for more details.

## SPICE BSIM 3v3 Model

```
*model = bsim3v3
*Berkeley Spice Compatibility
*Lmin= .35 Lmax= 20 Wmin= .6 Wmax= 20
.model N1 NMOS
+Level=11
+Tnom=27.0
+Nch=2.498E+17 Tox=9E-09 Xj=1.00000E-07
+Lint=9.36e-8 Wint=1.47e-7
+Vth0=.6322 K1=.756 K2=-3.83e-2 K3=-2.612
+Dvt0=2.812 Dvt1=0.462 Dvt2=-9.17e-2
+Nlx=3.52291E-08 W0= 1.163e-6 K3b= 2.233
+Vsats=86301.58 Ua=6.47e-9 Ub=4.23e-18 Uc=-4.706281E-11
+Rdsw=650 U0=388.3203 wr=1
+A0=.3496967 Ags=.1
+B0=0.546 B1= 1
+Dwg=-6.0E-09 Dw=-3.56E-09 Prwb=-.213
+Keta=-3.605872E-02 A1=2.778747E-02 A2=.9
+Voff=-6.735529E-02 NFactor=1.139926 Cit=1.622527E-04
+Cdsc=-2.147181E-05 Cdscb= 0
+Dvt0w=0 Dvt1w=0 Dvt2w=0
+Cdscd=0 Prwg=0
+Eta0=1.0281729E-02 Etab=-5.042203E-03
+Dsub=.31871233
```

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---

```
+Pclm=1.114846 Pdiblc1=2.45357E-03 Pdiblc2=6.406289E-03
+Drout=.31871233 Pscbe1=5000000 Pscbe2=5E-09 Pdiblc3=-.234
+Pvag=0 delta=0.01
+Wl=0 Ww=-1.420242E-09 Wwl = 0
+Wln=0 Wwn=.2613948 Ll=1.300902E-10
+Lw=0 Lwl=0 Lln=.316394 Lwn=0
+kt1=-.3 kt2=-.051
+At=22400
+Ute=-1.48
+Ua1=3.31E-10 Ub1=2.61E-19 Uc1=-3.42e-10
+Kt1l=0 Prt=764.3
```

## Spectre BSIM 3v3 Model

```
*Berkeley Spice Compatibility
*Lmin= .35 Lmax= 20 Wmin= .6 Wmax= 20
simulator lang=spectre
model nch bsim3v3
+version=3.1
+type=n
+tnom=27.0
+nch=2.498E+17 tox=9E-09 xj=1.00000E-07
+lint=9.36e-8 wint=1.47e-7
+vth0=.6322 k1=.756 k2=-3.83e-2 k3=-2.612
+dvt0=2.812 dvt1=0.462 dvt2=-9.17e-2
+n1x=3.52291E-08 w0= 1.163e-6 k3b= 2.233
+vsat=86301.58 ua=6.47e-9 ub=4.23e-18 uc=-4.706281e-11
+rdsw=650 u0=388.3203 wr=1
+a0=.3496967 ags=.1
+b0=0.546 b1= 1
+dwg=-6.0e-09 dwb=-3.56e-09 prwb=-.213
+keta=-3.605872e-02 a1=2.778747e-02 a2=.9
+voff=-6.735529e-02 nfactor=1.139926 cit=1.622527e-04
+cdsc=-2.147181e-05 cdsch= 0
+dvt0w=0 dvt1w=0 dvt2w=0
+cdscd=0 prwg=0
+eta0=1.0281729e-02 etab=-5.042203e-03
+dsb=.31871233
+pclm=1.114846 pdiblc1=2.45357e-03 pdiblc2=6.406289e-03
+drout=.31871233 pscbe1=5000000 pscbe2=5e-09 pdiblc3=-.234
+pvag=0 delta=0.01
+wl=0 ww=-1.420242e-09 wwl = 0
+wln=0 wwn=.2613948 ll=1.300902e-10
+lw=0 lwl=0 lln=.316394 lwn=0
+kt1=-.3 kt2=-.051
+at=22400
+ute=-1.48
+ua1=3.31e-10 ub1=2.61e-19 uc1=-3.42e-10
+kt1l=0 prt=764.3
```

## Ring Oscillator Spectre Deck for Inverter Ring with No Fanouts (inverter\_ring.sp)

This example uses Spectre syntax.

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---

```
// Ring oscillator Spectre deck for INVERTER ring with no fanouts.
simulator lang=spectre
global 0 gnd vdd vss

aliasGnd (gnd 0) vsource type=dc dc=0

// Spectre options to be used
SetOption1 options iabstol=1.00n audit=full temp=25

MyAcct1 info what=inst extremes=yes
MyAcct2 info what=models extremes=yes
MyAcct3 info what=input extremes=yes
MyAcct5 info what=terminals extremes=yes
MyAcct6 info what=oppooint extremes=yes

// Next section is the subckt for inv
subckt inv (nq a)
m1 (nq a vdd vdd) p l=0.35u w=2.60u ad=1.90p pd=6.66u as=1.90p ps=6.66u
m2 (vss a nq vss) n l=0.35u w=1.10u ad=0.80p pd=3.66u as=0.80p ps=3.66u

// Interconnect Caps for inv
c0 (a vdd) capacitor c=1.0824323e-15
c1 (a nq) capacitor c=3.0044e-16
c2 (nq vss) capacitor c=5.00186e-16
c3 (nq vdd) capacitor c=6.913993e-16
c4 (a vss) capacitor c=8.5372566e-16
ends

// Begin top level circuit definition
xinv1 (1 90) inv
xinv2 (2 1) inv
xinv3 (3 2) inv
xinv4 (4 3) inv
xinv5 (5 4) inv
xinv6 (6 5) inv
xinv7 (7 6) inv
xinv8 (8 7) inv
xinv9 (9 8) inv
xinv10 (10 9) inv
xinv11 (11 10) inv
xinv12 (12 11) inv
xinv13 (13 12) inv
xinv14 (14 13) inv
xinv15 (15 14) inv
xinv16 (16 15) inv
xinv17 (90 16) inv

// Next couple of lines sets variables for vdd and vss.
parameters vdd_S1=3.3
parameters vss_S1=0.0
vdd_I1 (vdd gnd) vsource dc=vdd_S1
vss_I1 (vss gnd) vsource dc=vss_S1

// Set initial conditions:
ic 2=0 4=0 6=0 8=0 10=0

// Next line makes the call to the model
// NOTE: The user may utilize the '.lib' syntax with Spectre's +spp
// command line option if they are using Spectre 4.43 or greater.
// There is also a Spectre native syntax for equivalent
// functionality. It is shown in q35d4h5.modsp.

include "q35d4h5.modsp" section=tt
```



```
// Analysis Statement
tempOption options temp=25
typ_tran tran step=0.010n stop=35n

alter_ss altergroup {
include "q35d4h5.modsp" section=ss
parameters vdd_S1=3.0
}

alterTempTo100 alter param=temp value=100
ss_tran tran step=0.010n stop=35n

alter_ff altergroup {
include "q35d4h5.modsp" section=ff
parameters vdd_S1=3.3
}

alterTempTo0 alter param=temp value=0
ff_tran tran step=0.010n stop=35n
```

## Ring Oscillator Spectre Deck for Two-Input NAND Ring with No Fanouts (nand2\_ring.sp)

This example uses Spectre syntax.

```
// Ring oscillator Spectre deck for 2-Input NAND ring with no fanouts.
simulator lang=spectre
global 0 gnd vdd vss

aliasGnd (gnd 0) vsource type=dc dc=0

// Spectre options to be used
SetOption1 options iabstol=1.00n audit=full

MyAcct1 info what=inst extremes=yes
MyAcct2 info what=models extremes=yes
MyAcct3 info what=input extremes=yes
MyAcct5 info what=terminals extremes=yes
MyAcct6 info what=oppooint extremes=yes

// Next section is the subckt for na2 *****
subckt na2 (nq a)
m1 (nq a vdd vdd) p l=0.35u w=2.70u ad=1.03p pd=3.46u as=1.98p ps=6.86u
m2 (nq vdd vdd vdd) p l=0.35u w=2.70u ad=1.03p pd=3.46u as=1.98p ps=6.86u
m3 (vss a 6 vss) n l=0.35u w=1.70u ad=1.25p pd=4.86u as=0.18p ps=1.91u
m4 (nq vdd 6 vss) n l=0.35u w=1.70u ad=1.25p pd=4.86u as=0.18p ps=1.91u
c0 (a vdd) capacitor c=1.0512057e-15
c1 (a nq) capacitor c=7.308e-17
c2 (vdd vss) capacitor c=6.12359e-16
c3 (nq vss) capacitor c=5.175377e-16
c4 (nq vdd) capacitor c=1.1668172e-15
c5 (a vss) capacitor c=9.530671e-16
ends

// Begin top-level circuit definition
xna21 (1 90) na2
xna22 (2 1) na2
xna23 (3 2) na2
xna24 (4 3) na2
xna25 (5 4) na2
```

```
xna26 (6 5) na2
xna27 (7 6) na2
xna28 (8 7) na2
xna29 (9 8) na2
xna210 (10 9) na2
xna211 (11 10) na2
xna212 (12 11) na2
xna213 (13 12) na2
xna214 (14 13) na2
xna215 (15 14) na2
xna216 (16 15) na2
xna217 (90 16) na2

// Next couple of lines sets variables for vdd and vss.
parameters vdd_S1=3.3
parameters vss_S1=0.0
vdd_I1 (vdd gnd) vsource dc=vdd_S1
vss_I1 (vss gnd) vsource dc=vss_S1

// Next line initializes nodes within ring
ic 2=0 4=0 6=0 8=0 10=0

include "q35d4h5.modsp" section=tt

// Next line defines transient steps and total simulation time
tempOption options temp=25
tt_tran tran step=0.010n stop=35n

alter_ss altergroup {
include "q35d4h5.modsp" section=ss
parameters vdd_S1=3.0
}

alterTempTo100 alter param=temp value=100
ss_tran tran step=0.010n stop=35n

alter_ff altergroup {
include "q35d4h5.modsp" section=ss
parameters vdd_S1=3.3
}

alterTempTo0 alter param=temp value=0
ff_tran tran step=0.010n stop=35n
```

## **Ring Oscillator Spectre Deck for Three-Input NAND Ring with No Fanouts (nand3\_ring.sp)**

This example uses Spectre syntax.

```
// Ring oscillator Spectre deck for 3-Input NAND ring with no fanouts.
simulator lang=spectre
global 0 gnd vdd vss

aliasGnd (gnd 0) vsource type=dc dc=0

// Simulator options to use
SetOption1 options iabstol=1.00n audit=full

MyAcct1 info what=inst extremes=yes
MyAcct2 info what=models extremes=yes
```

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---

```
MyAcct3 info what=input extremes=yes
MyAcct5 info what=terminals extremes=yes
MyAcct6 info what=oppooint extremes=yes

// Next section is the subckt for na3p1
subckt na3p1 (nq a)
m1 (nq a vdd vdd) p l=0.35u w=2.90u ad=1.10p pd=3.66u as=2.12p ps=7.26u
m2 (nq vdd vdd vdd) p l=0.35u w=2.90u ad=1.10p pd=3.66u as=1.10p ps=3.66u
m3 (nq vdd vdd vdd) p l=0.35u w=2.90u ad=2.12p pd=7.26u as=1.10p ps=3.66u
m4 (vss a 7 vss) n l=0.35u w=2.40u ad=1.75p pd=6.26u as=0.25p ps=2.61u
m5 (7 vdd 8 vss) n l=0.35u w=2.40u ad=0.25p pd=2.61u as=0.25p ps=2.61u
m6 (nq vdd 8 vss) n l=0.35u w=2.40u ad=1.75p pd=6.26u as=0.25p ps=2.61u
c0 (8 vdd) capacitor c=1.341e-17
c1 (vdd vss) capacitor c=9.9445302e-16
c2 (nq vss) capacitor c=6.287e-16
c3 (nq vdd) capacitor c=2.0719818e-15
c4 (a vss) capacitor c=5.3760487e-16
c5 (a vdd) capacitor c=1.2446956e-15
c6 (a nq) capacitor c=7.308e-17
c7 (7 vdd) capacitor c=2.0115e-17
ends

// Begin top level circuit definition
xna3p11 (1 90) na3p1
xna3p12 (2 1) na3p1
xna3p13 (3 2) na3p1
xna3p14 (4 3) na3p1
xna3p15 (5 4) na3p1
xna3p16 (6 5) na3p1
xna3p17 (7 6) na3p1
xna3p18 (8 7) na3p1
xna3p19 (9 8) na3p1
xna3p110 (10 9) na3p1
xna3p111 (11 10) na3p1
xna3p112 (12 11) na3p1
xna3p113 (13 12) na3p1
xna3p114 (14 13) na3p1
xna3p115 (15 14) na3p1
xna3p116 (16 15) na3p1
xna3p117 (90 16) na3p1

// Next couple of lines sets variables for vdd and vss.
parameters vdd_S1=3.3
parameters vss_S1=0.0
vdd_I1 (vdd gnd) vsource dc=vdd_S1
vss_I1 (vss gnd) vsource dc=vss_S1

// Next line initializes nodes within ring
ic 2=0 4=0 6=0 8=0 10=0

include "q35d4h5.modsp" section=tt

// Transient analysis card
tempOption options temp=25
typ_tran tran step=0.010n stop=35n
alter_ss altergroup {
include "q35d4h5.modsp" section=ss
parameters vdd_S1=3.0
}
```

```
alterTempTo100 alter param=temp value=100
ss_tran tran step=0.010n stop=35n

myAlter2 altergroup {
include "q35d4h5.modsp" section=ff
parameters vdd_S1=3.3
}

alterTempTo0 alter param=temp value=0
ff_tran tran step=0.010n stop=35n
```

## Ring Oscillator Spectre Deck for Two-Input NOR Ring with No Fanouts (nor2\_ring.sp)

This example uses Spectre syntax.

```
// Ring oscillator Spectre deck for 2-Input NOR ring with no fanouts.
simulator lang=spectre
global 0 gnd vdd vss

aliasGnd (gnd 0) vsource type=dc dc=0

// Spectre options
SetOption1 options iabstol=1.00n audit=full

MyAcct1 info what=inst extremes=yes
MyAcct2 info what=models extremes=yes
MyAcct3 info what=input extremes=yes
MyAcct5 info what=terminals extremes=yes
MyAcct6 info what=oppooint extremes=yes

// Next section is the subckt for no2
subckt no2 (nq a)
m1 (vdd a 6 vdd) p l=0.35u w=4.80u ad=3.50p pd=11.06u as=0.50p ps=5.01u
m2 (nq vss 6 vdd) p l=0.35u w=4.80u ad=3.50p pd=11.06u as=0.50p ps=5.01u
m3 (vss a nq vss) n l=0.35u w=1.20u ad=0.88p pd=3.86u as=0.46p ps=1.96u
m4 (vss vss nq vss) n l=0.35u w=1.20u ad=0.88p pd=3.86u as=0.46p ps=1.96u
c0 (a vdd) capacitor c=6.3676066e-16
c1 (a nq) capacitor c=5.3592e-17
c2 (vdd vss) capacitor c=5.39538e-16
c3 (nq vss) capacitor c=8.780327e-16
c4 (nq vdd) capacitor c=5.577428e-16
c5 (a vss) capacitor c=1.1100392e-15
ends

// begin top level circuit definition
xno21 (1 90) no2
xno22 (2 1) no2
xno23 (3 2) no2
xno24 (4 3) no2
xno25 (5 4) no2
xno26 (6 5) no2
xno27 (7 6) no2
xno28 (8 7) no2
xno29 (9 8) no2
xno210 (10 9) no2
xno211 (11 10) no2
xno212 (12 11) no2
xno213 (13 12) no2
xno214 (14 13) no2
```

```
xno215 (15 14) no2
xno216 (16 15) no2
xno217 (90 16) no2

// Next couple of lines sets variables for vdd and vss.
parameters vdd_S1=3.3
parameters vss_S1=0.0
vdd_I1 (vdd gnd) vsource dc=vdd_S1
vss_I1 (vss gnd) vsource dc=vss_S1

// Next line initializes nodes within ring.
ic 2=0 4=0 6=0 8=0 10=0

include "q35d4h5.modsp" section=tt

// Analysis
tempOption options temp=25
tt_tran tran step=0.010n stop=35n

ss_alter altergroup {
include "q35d4h5.modsp" section=ss
parameters vdd_S1=3.0
}

alterTempTo100 alter param=temp value=100
ss_tran tran step=0.010n stop=35n

ff_alter altergroup {
include "q35d4h5.modsp" section=ff
parameters vdd_S1=3.3
}

alterTempTo0 alter param=temp value=0
ff_tran tran step=0.010n stop=35n
```

## Ring Oscillator Spectre Deck for Three-Input NOR Ring with No Fanouts (nor3\_ring.sp)

This example uses Spectre syntax.

```
// Ring oscillator spectre deck for 3-Input NOR ring with no fanouts.
simulator lang=spectre
global 0 gnd vdd vss
aliasGnd (gnd 0) vsource type=dc dc=0

// Spectre options
SetOption1 options iabstol=1.00n audit=full rforce=1 temp=25

MyAcct1 info what=inst extremes=yes
MyAcct2 info what=models extremes=yes
MyAcct3 info what=input extremes=yes
MyAcct5 info what=terminals extremes=yes
MyAcct6 info what=oppooint extremes=yes

// Next section is the subckt for no3
subckt no3 (nq a)
m1 (vdd a 7 vdd) p l=0.35u w=3.60u ad=2.63p pd=8.66u as=0.38p ps=3.81u
m2 (7 vss 8 vdd) p l=0.35u w=3.60u ad=0.38p pd=3.81u as=0.38p ps=3.81u
m3 (nq vss 8 vdd) p l=0.35u w=3.60u ad=1.37p pd=4.36u as=0.38p ps=3.81u
m4 (nq vss 9 vdd) p l=0.35u w=3.60u ad=1.37p pd=4.36u as=0.38p ps=3.81u
m5 (9 vss 10 vdd) p l=0.35u w=3.60u ad=0.38p pd=3.81u as=0.38p ps=3.81u
m6 (vdd a 10 vdd) p l=0.35u w=3.60u ad=2.63p pd=8.66u as=0.38p ps=3.81u
```

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```
m7 (vss a nq vss) n l=0.35u w=1.40u ad=1.02p pd=4.26u as=0.53p ps=2.16u
m8 (vss vss nq vss) n l=0.35u w=1.40u ad=0.53p pd=2.16u as=0.53p ps=2.16u
m9 (vss vss nq vss) n l=0.35u w=1.40u ad=0.53p pd=2.16u as=1.02p ps=4.26u
c1 (9 nq) capacitor c=3.7995e-17
c2 (vdd vss) capacitor c=1.3996057e-15
c3 (nq vss) capacitor c=3.1546797e-15
c4 (nq vdd) capacitor c=5.5551875e-16
c5 (a vss) capacitor c=1.2907233e-15
c6 (a vdd) capacitor c=2.1779808e-15
c7 (10 nq) capacitor c=2.0115e-17
c8 (a nq) capacitor c=5.233362e-16
ends

// Begin top-level circuit definition
xno31 (1 90) no3
xno32 (2 1) no3
xno33 (3 2) no3
xno34 (4 3) no3
xno35 (5 4) no3
xno36 (6 5) no3
xno37 (7 6) no3
xno38 (8 7) no3
xno39 (9 8) no3
xno310 (10 9) no3
xno311 (11 10) no3
xno312 (12 11) no3
xno313 (13 12) no3
xno314 (14 13) no3
xno315 (15 14) no3
xno316 (16 15) no3
xno317 (90 16) no3

// Next couple of lines sets variables for vdd and vss.
parameters vdd_S1=3.3
parameters vss_S1=0.0
vdd_I1 (vdd gnd) vsource dc=vdd_S1
vss_I1 (vss gnd) vsource dc=vss_S1

// Next line initializes nodes within ring
ic 2=0 4=0 6=0 8=0 10=0

include "q35d4h5.modsp" section=tt

// Analysis
tempOption options temp=25
typ_tran tran step=0.010n stop=35n

alter_ss altergroup {
include "q35d4h5.modsp" section=ss
parameters vdd_S1=3.0
}

alterTempTo100 alter param=temp value=100
ss_tran tran step=0.010n stop=35n

alter_ff altergroup {
include "q35d4h5.modsp" section=ff
parameters vdd_S1=3.3
}

alterTempTo0 alter param=temp value=0
ff_tran tran step=0.010n stop=35n
```

## Opamp Circuit (opamp.cir)

This example uses Spectre's SPICE syntax.

```
.subckt opamp 1 2 6 8 9
m1 4 2 3 3 nch w=43u l=10u ad=0.3n as=0.3n pd=50u ps=50u
m2 5 1 3 3 nch w=43u l=10u ad=0.3n as=0.3n pd=50u ps=50u
m3 4 4 8 8 pch w=10u l=10u ad=0.3n as=0.3n pd=20u ps=20u
m4 5 4 8 8 pch w=10u l=10u ad=0.3n as=0.3n pd=20u ps=20u
m5 3 7 9 9 nch w=38u l=10u ad=0.3n as=0.3n pd=40u ps=40u
m6 6 5 8 8 pch w=344u l=10u ad=1.3n as=1.3n pd=350u ps=350u
m7 6 7 9 9 nch w=652u l=10u ad=2.3n as=2.3n pd=660u ps=660u
m8 7 7 9 9 nch w=38u l=10u ad=0.3n as=0.3n pd=40u ps=40u
cc 5 6 4.4p
ibias 8 7 8.8u
.ends opamp
```

## Opamp Circuit 2 (opamp1.cir)

This example uses Spectre's SPICE syntax.

```
.subckt opamp 1 2 6 8 9
m1 4 2 3 3 nch w=20u l=0.5u ad=0.3n as=0.3n pd=50u ps=50u
m2 5 1 3 3 nch w=20u l=0.5u ad=0.3n as=0.3n pd=50u ps=50u
m3 4 4 8 8 pch w=20u l=0.5u ad=0.3n as=0.3n pd=20u ps=20u
m4 5 4 8 8 pch w=20u l=0.5u ad=0.3n as=0.3n pd=20u ps=20u
m5 3 7 9 9 nch w=20u l=0.5u ad=0.3n as=0.3n pd=40u ps=40u
m6 6 5 8 8 pch w=20u l=0.5u ad=1.3n as=1.3n pd=350u ps=350u
m7 6 7 9 9 nch w=20u l=0.5u ad=2.3n as=2.3n pd=660u ps=660u
m8 7 7 9 9 nch w=20u l=0.5u ad=0.3n as=0.3n pd=40u ps=40u
cc 5 6 4.4p
ibias 8 7 8.8u
.ends opamp
```

## Original Open-Loop Opamp (openloop.sp)

```
* Allen & Holmberg, p. 438 - Original Open Loop OpAmp Configuration
vinp 1 0 dc 0 ac 1.0
vdd 4 0 dc 5.0
vss 0 5 dc 5.0
vinm 2 0 dc 0
cl 3 0 20p
x1 1 2 3 4 5 opamp
** Bring in opamp subcircuit
include "opamp.cir"
** Bring in models here
.model nch bsim3v3
.model pch bsim3v3 type=p
.op
simulator lang = spectre
tf (3 0) xf save=lvlpub nestlvl=1 start=1 stop=1K dec=20
simulator lang = spice
.dc vinp -0.005 0.005 100u
.print dc v(3)
```

```
.ac dec 10 1 10MEG
.print ac vdb(3) vp(3)
.end
```

## Modified Open-Loop Opamp (openloop1.sp)

```
* Allen & Holmberg, p. 438 - Modified Open Loop OpAmp Configuration
vinp 1 0 dc 0 ac 1.0
vdd 4 0 dc 5.0
vss 0 5 dc 5.0
vinm 2 0 dc 0
cl 3 0 20p
x1 1 2 3 4 5 opamp
** Bring in opamp subcircuit
include "opamp1.cir"
** Bring in models here
.model nch bsim3v3
.model pch bsim3v3 type=p
.op
simulator lang = spectre
tf (3 0) xf save=lvlpub nestlvl=1 start=1 stop=1K dec=20
simulator lang = spice
.dc vinp -0.10 0.10 10u
.print dc v(3)
.ac dec 10 1 10MEG
.print ac vdb(3) vp(3)
.end
```

## Example Model Directory (q35d4h5.modsp)

```
//example model directory
simulator lang = spectre

library mosmodels
section tt
model n bsim3v3 tox=1.194e-08
model p bsim3v3 type=p tox=7.4e-09
endsection

section ss
model n bsim3v3 tox=1.242e-08
model p bsim3v3 type=p tox=7.724e-09
endsection

section ff
model n bsim3v3 tox=1.1544e-08
model p bsim3v3 type=p tox=7.148e-09
endsection
endlibrary
```



---

## Using Compiled-Model Interface

---

The Spectre® circuit simulator supports dynamic loading of device models. This feature allows you to dynamically load device primitives (stored in shared objects) at run time. This is useful for developing and distributing models.

### Installing Compiled-Model Interface (CMI)

CMI is now shipped with Spectre. The installation is done as a manual step after the Spectre product installation.

To install CMI, run the `cmiExtract` script located in the following directory:

`your_install_dir/tools.<platform>/spectre/bin`

You must have a valid Spectre CMI license to run this script. You are prompted to specify a directory in which the CMI hierarchy is to be installed, with the default being

`your_install_dir/tools.<platform>/.`

Once the extraction script is complete, the CMI hierarchy can be found in the directory `spectrecmi` in the specified location. The README files are in the `spectrecmi` directory and the CMI manual, `cmiprint.pdf`, is in `spectrecmi/doc/`. See the CMI manual, Compiled-Model Interface Reference for information on how to proceed.

### Configuration File

The Spectre circuit simulator can be configured to load a specific set of shared objects based on the content of a set of configuration files. The default CMI configuration file is shown below.

```
; The default search path is
; your_install_dir/tools.<platform>/spectre/lib/cmi/%M
; This file is automatically generated.
; Any changes made to it will not be saved.

load libinfineon_sh.so
load libphilips_sh.so
load libphilips_o_sh.so
```

```
load libsparam_sh.so
load libstmodels.so
```

The CMI file allows legal UNIX file paths and Spectre predefined percent codes. For more information on predefined percent codes, see [Description of Spectre Predefined Percent Codes](#) on page 951.

## Configuration File Format

The following commands can be used in the configuration file:

| Command | Action                                                           |
|---------|------------------------------------------------------------------|
| setpath | Specifies the search path.                                       |
| prepend | Adds a path before the current search path.                      |
| append  | Adds a path after the current search path.                       |
| load    | Adds a shared object to the list of shared objects to load.      |
| unload  | Removes a shared object from the list of shared objects to load. |

The following examples show the syntax for these commands.

### ***To specify a search path:***

```
setpath path [path2 ...path N]
```

#### **Example 1:**

```
setpath $HOME/cds/15.1/tools.%O/spectre/lib/%B/cmi/%M
```

#### **Example 2:**

```
setpath ($HOME/myLib/cmi/%M $HOME/cds/15.1/tools.%O/spectre/lib/%B/cmi/%M)
```

where %O is expanded to the platform name and %B is expanded to 64bit for the 64-bit version of the software.

### ***To prepend a path:***

```
prepend path [path 2 ... path N]
```

#### **Example 1:**

```
prepend $HOME/myLib/cmi/%M
```

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### Example 2:

```
prepend ($HOME/myLib/cmi/%M $HOME/cds/15.1/tools.%O/spectre/lib/%B/cmi/%M)
```

### **To append a path:**

```
append path [path2 ... path N]
```

### Example 1:

```
append $HOME/myLib/cmi/%M
```

### Example 2:

```
append ($HOME/myLib/cmi/%M $HOME/expLib/cmi/%M)
```

The default search path is the path to the directory that contains Spectre shared objects: `$CDS_ROOT/tools.<platform>/spectre/lib/cmi/CMIVersion`.

### **To load a shared object:**

```
load [path/] soname.ext
```

### Example 1:

```
load libnortel.so
```

### Example 2:

```
load $HOME/myLib/cmi/%M/libmydevice.so
```

### **To unload a shared object:**

```
unload [path/] soname.ext.version
```

### Example 1:

```
unload libsiemens.so.1
```

### Example 2:

```
unload $HOME/myLib/cmi/%M/libmydevice.so
```

The name of the shared object file includes an extension and can also have a version number. The path to the shared object is optional. If you do not specify the path, the Spectre simulator uses the search path from the current configuration file.

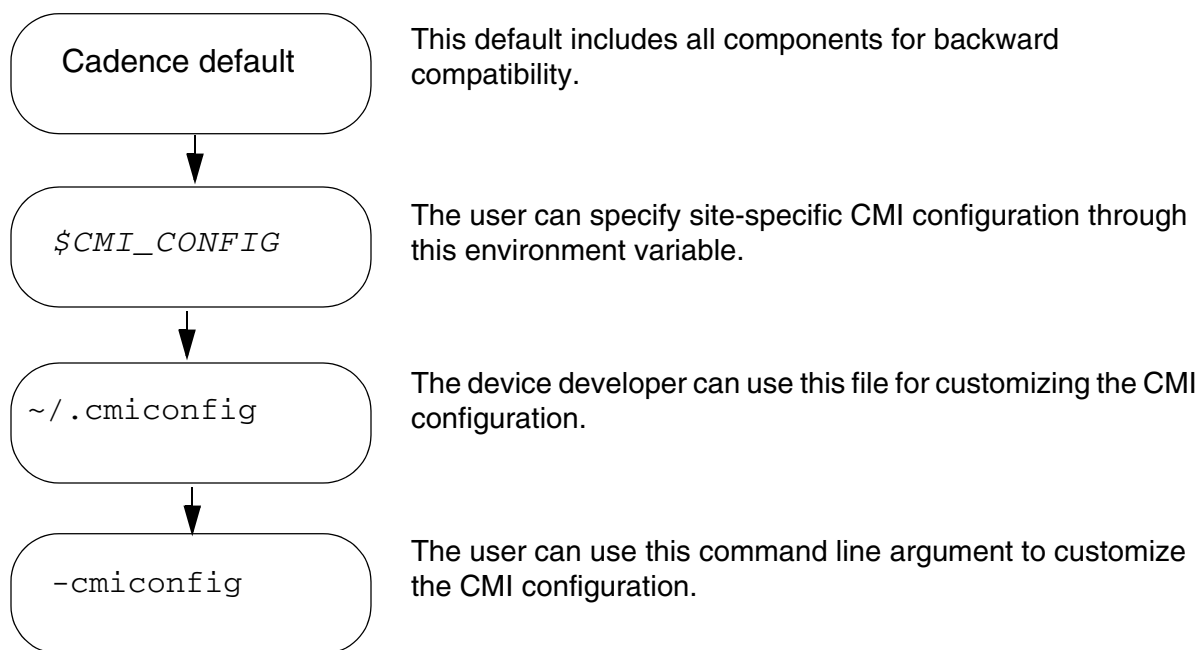
A line that begins with a semicolon is a comment and is ignored. Empty lines are allowed and are ignored.

## Precedence for the CMI Configuration File

The Spectre simulator reads configuration files in the following order:

- The default Cadence CMI configuration file
- The configuration file specified by the value of the `$CMI_CONFIG` environment variable
- The file `$HOME/.cmiconfig`, if it exists
- The CMI configuration file specified in the `-cmiconfig` argument

Each configuration file modifies the previous configuration.



## Configuration File Example

This section contains examples that show how configuration files can be used to customize the list of shared objects that the Spectre circuit simulator loads at run time. The default configuration file includes `libinfineon_sh.so`, `libstmodels_sh.so`, `libphilips_sh.so`, `libphilips_o_sh.so`, and `libsparam_sh.so`.

If you need only the ST models, you can create a configuration file called `site_cmi_config` that loads only `libstmodels.so` by unloading the other three shared objects:

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---

```
;default search path is $CDS_ROOT/tools/spectre/lib/cmi/%M
;only libstmodels for this site
;this file is called site_cmi_config
unload libinfineon_sh.so
unload libphilips_sh.so
unload libphilips_o_sh.so
unload libsparm_sh.s0
```

When the environment variable `$CMI_CONFIG` is set to `site_cmi_config`, only `libstmodels.so` is loaded.

A model developer can create a file `$HOME/myLib/libmybjt.so` consisting of the BJT model under development. To check the results of the BJT under development in `libmybjt.so` with the BJT503 models in `libphilips_sh.so`, the developer can create a CMI configuration file in the home directory as follows:

```
;this is $HOME/.cmiconfig file
;I want to include libphilips.so released by Cadence so that
;I can check my BJT with BJT503.
load libphilips_sh.so
;I also want to include my BJT model from libmybjt.so
append $HOME/myLib
load libmybjt.so
```

## CMI Versioning

The version format for CMI is *major.minor*. The value of *major* is increased when there are major changes that require CMI developers to recompile their components.

Type `spectre -cmiversion` to display the current CMI version.

The Spectre circuit simulator checks for CMI version compatibility for each shared object as well as for each primitive. This ensures that

- A shared object is compiled with the latest version of CMI
- The source code for each device primitive is up to date

**Note:** A primitive can be installed only once. Different versions of the same primitive cannot be used.

## Checking the CMI Shared Library

Spectre provides a utility `cmicheck` that enables you to check your CMI libraries before using them. The `cmicheck` utility is located in the `<your_install_directory>/bin` directory and can be used as follows:

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```
% spectre +cmicheck[=summary] -cmiconfig <path>
```

or

```
% spectre +cmicheck=all -cmiconfig <path>
```

`spectre +cmicheck=summary` displays the following output on your screen:

- Number of CMI shared libraries
- Shared library
- Timestamp
- Platform
- CMI Version
- Defined Primitives

In addition to the above information, `spectre +cmicheck=all`, displays information related to each primitive including model and instance parameters.

---

## Netlist Compiled Functions (NCF)

---

The Spectre circuit simulator now allows a netlist expression to call functions that are loaded from a Dynamic Link Library (DLL). With this functionality, you can create your own functions in C or C++, for example, taking advantage of the features of these languages and overcoming the restrictions of the netlist user-defined function.

### Loading a Plug-in

A plug-in can be loaded using either the `-plugin` command-line option or the `CDS_MMSIM_PLUGINS` environment variable. Both approaches allow the use of embedded environment variables, `%` modifiers and tilde expansion. A list of plug-ins can be provided using `CDS_MMSIM_PLUGINS`. Elements of the list are separated by whitespace or semicolons.

```
% spectre -plugin ~/plugins/%O/libmyplugin_sh.so mytest.scs +log %C:r.out
```

or

```
% setenv CDS_MMSIM_PLUGINS "~/plugins/%O/libmyplugin_sh.so"
```

```
% spectre mytest.scs +log %C:r.out
```

Commonly used `%` modifiers are

- `%I`: MMSIM installation hierarchy
- `%O`: Platform specified, equivalent to the result of `cds_plat`
- `%B`: A 32-bit executable replaces this with an empty string. A 64-bit executable expands this to the string `64bit`.

### Using a NCF in a Spectre Netlist

A NCF is called in a Spectre netlist just like any built-in mathematical function or user-defined function is called. There is no special syntax required to use a NCF once its plug-in has been

successfully loaded by Spectre. In the following example, `safe_sqrt( x )` is a simple NCF that evaluates the following code

```
if (x < 0.0)
 return 0.0;
else
 return sqrt(x);
```

In the Spectre netlist, this is called as follows

```
parameters w=1u y=safe_sqrt(w)
```

It could also be called on any instance or model parameter expression. There are some restrictions on the use of NCF functions.

- A NCF cannot be used in a behavioral source if an argument to the NCF is non-constant, i.e. a reference to a node voltage, device current, etc.

```
r1 1 0 resistor r=add(1.0, 2.0)*1k // Used correctly
b1 1 0 bsource i=v(1)/(add(1.0, 2.0)*1k) // Used correctly
b1 1 0 bsource i=add(v(1), 0)/1k // Error, cannot compute d(i)/d(v(1))
```

- A NCF cannot be used in a post-processing statement, such as a `save`, `.PRINT`, `.PROBE` or `.MEASURE`.

## Creating a Plug-in

You must include the `ncf.h` file to provide declarations of all functions and variables used in the plug-in.

The plug-in must contain the `ncfinstall` function, which must include a call to the `ncfSetDefaultVersion` version. This function informs the application the version of the NCF interface that the following NCF functions support. If the call to this function fails, the application prints an error message, and ignores all subsequent NCF calls from this plug-in.

A sample plug-in is given below.

```
#include <math.h>
#include "plugins/ncf.h"

double
foo(ncfHandle_t handle, int argc, double argv[])
{
 /* return result; */
}

void
```



```
ncfInstall(void)
{
 ncfHandle_t func = 0L;
 if (ncfSetDefaultVersion(NCF_VERSION_1) == ncfFalse)
 return;

 /* Create and register the function "foo" */
 func = ncfCreateFunction("foo");
 ncfRegisterFunction(func);
}
```

Assuming that *SPECTRE\_INSTALL* is the root of the SPECTRE installation, the path to the *ncf.h* file is

```
${SPECTRE_INSTALL}/tools/mmsim/include/plugins
```

When adding this path to the compile line using the *-I* option, you can add the path to the *mmsim/include* directory, rather the path to the *plug-ins* directory, as follows:

```
% gcc -fPIC -I${MMSIM_INSTALL}/tools/mmsim/include -o myplugin.o -c myplugin.c
```

No Cadence libraries need to be linked to the final plug-in DLL, however it is normally necessary to link in the math library. To create the plug-in, all object files should be compiled with the appropriate PIC option and then linked together into the DLL. The following example uses *gcc* to create the shared library.

```
% gcc -shared -o libmyplugin_sh.so myplugin.o -lm
% cp libmyplugin_sh.so ~/plugins/`cds_plat`
```

## Installing a NCF

To create a NCF, you must first call the function *ncfCreateFunction*. The only argument is the name of the NCF as it will be called from the netlist. The return value is a handle to the NCF object, a *ncfHandle\_t*. If the call to *ncfCreateFunction* fails, a value of *0L* is returned. You must then register the NCF with the application by calling *ncfRegisterFunction*. The only argument passed to this function is the previously created handle.

```
ncfHandle_t func = ncfCreateFunction("foo");
ncfRegisterFunction(func);
```

In the above example, the NCF *foo* is created and registered with the application. By default the NCF has the following attributes.

- It takes one scalar real argument which has pass-by-value semantics.

- Its return value is a real scalar.
- The name of the function as called from the netlist is `foo`.
- Since the developer has not provided a compiled function, the application searches the plug-in for an exported symbol with the name `foo`, and assumes that symbol is the function to be executed when the NCF is called.

## Modifying the Default Behavior of a NCF

While the default behavior of the NCF can be sufficient, this may not be the case. For example, the NCF may take more than one argument, the name of the compiled function is different than the name of the NCF, or the compiled function is not exported from the plug-in. The following functions can be used to modify the default behavior of the NCF.

### **`ncfSetNumArgs( ncfHandle_t, int, int )`**

This function takes three arguments. The first is a handle to the NCF being modified. The next two are the minimum and maximum number of arguments, respectively.

```
ncfSetNumArgs(func, 2, 2);
ncfSetNumArgs(func, 2, 10);
```

In the first example above, the NCF `func` accepts two arguments. If the call to this NCF from the netlist has a different number of arguments, the parser will error out immediately. In the second example, the NCF can have any number of arguments from a minimum of two to a maximum of ten.

### **`ncfSetDLLFunctionV1( ncfHandle_t, ncfFunctionV1Ptr_t )`**

If the you do not specify a compiled function for a particular NCF, the application searches the plug-in for a function with the same name as the NCF. If such a symbol does not exist or it exists but does not have global scope (in C this would indicate that it has static linkage), then an error message is printed and the application exits.

The function `ncfSetDLLFunctionV1` can be used to specify the compiled function to be called when an NCF is evaluated. The `V1` suffix indicates that the function conforms to the `NCF_VERSION_1` interface. The first argument is a handle to the NCF being modified. The second argument is a pointer to the actual compiled function. For the `NCF_VERSION_1` interface, the compiled function takes three arguments. The first is a handle to the function registered NCF, the second is the number of arguments in the netlist call, and the third is an

array of double values. Each value corresponds to a value from the netlist call. The signature of the compiled function is

```
double (*ncfFunctionV1Ptr_t) (ncfHandle_t handle, int argc, double argv[]);
```

A simple example of the use of `ncfSetDLLFunctionV1` is as follows

```
#include <math.h>
#include "plugins/ncf.h"

/* A simple function to add two arguments. */
static
double add(ncfHandle_t handle, int argc, double argv[])
{
 return argv[0] + argv[1];
}

void
ncfInstall(void)
{
 ncfHandle_t func = 0L;
 if (ncfSetDefaultVersion(NCF_VERSION_1) == ncfFalse)
 return;

 func = ncfCreateFunction("add");
 ncfSetNumArgs(func, 2, 2);

 /* The call to ncfSetDLLFunctionV1 is required since 'add'
 * is defined above to have static linkage, hence it cannot be
 * seen by the application loading the plugin. */
 ncfSetDLLFunctionV1(func, &add);

 ncfRegisterFunction(func);

 return;
}
```

## Attaching Arbitrary Data to a NCF

You may wish to attach extra data to a NCF. This data can be attached during the creation of the NCF and then retrieved during function evaluation, using the provided `ncfHandle_t` argument. This feature is normally used to allow multiple NCFs to share a common for implementation or to provide a interposer type functionality.

```
ncfSetData(ncfHandle_t, ncfData_t)
ncfData_t ncfGetData(ncfHandle_t)
```

These functions set and get data on a previously created NCF. In the following example, two NCF, `add` and `sub`, are registered with the application, but they share a common compiled function implementation, `add_or_sub`. The compiled function uses the `ncfGetData` function to get the data associated with the supplied `ncfHandle_t`. If the data is `+1`, the supplied arguments are added: if the data is `-1`, the supplied arguments are subtracted. When

the NCF's are being created, you use the `ncfSetData` function to set data on each `ncfHandle_t`.

```
#include <math.h>
#include "plugins/ncf.h"

static
double add_or_sub(ncfHandle_t handle, int argc, double argv[])
{
 ncfData_t data = ncfGetData(handle);
 if (data == +1)
 return argv[0] + argv[1];
 else if (data == -1)
 return argv[0] - argv[1];
 else
 return 0.0;
}

void
ncfInstall(void)
{
 ncfHandle_t func = 0L;
 if (ncfSetDefaultVersion(NCF_VERSION_1) == ncfFalse)
 return;

 func = ncfCreateFunction("add");
 ncfSetNumArgs(func, 2, 2);
 ncfSetDLLFunctionV1(func, &add_or_sub);
 ncfSetData(func, +1);
 ncfRegisterFunction(func);

 func = ncfCreateFunction("sub");
 ncfSetNumArgs(func, 2, 2);
 ncfSetDLLFunctionV1(func, &add_or_sub);
 ncfSetData(func, -1);
 ncfRegisterFunction(func);
}
```

---

## Digital Vector File Format

---

This chapter describes how to perform vector checks and apply stimuli according to digital vectors using the Spectre circuit simulator. To process digital vector file formats, the following statement needs to be specified in the netlist file:

### Spectre Syntax

```
vec_include "vector_filename" [HLCheck=0|1] [autostop=yes|no]
[insensitive=yes|no]
```

### SPICE Syntax

```
.vec "vector_filename" [HLCheck=0|1] [autostop=true|false] [insensitive=yes|no]
```

**Note:** A period (.) is required when using SPICE language syntax (for example, .vec).

### Description

HLCheck is a special flag that you need to set to generate the vector output check for H and L states of input signals. Bidirectional and output signals always check H and L states and are unaffected by the HLCheck flag. Normally, you do not need to use the HLCheck flag unless it is necessary to check if input signals are shorted in the netlist file. The output resistance of H and L states for input signals can be specified by the hlz statement.

Each vec card can specify only one vector file. If a netlist file needs to include multiple vector files, multiple vec cards can be used. For example, if a netlist file needs to include three vector files, then it needs to use three vec cards.

#### Spectre Syntax:

```
Card 1: vec_include "file1.vec"
Card 2: vec_include "file2.vec"
Card 3: vec_include "file3.vec"
```

#### SPICE Syntax:

```
Card 1: .vec "file1.vec"
Card 2: .vec "file2.vec"
```

Card 3: .vec "file3.vec"

## Arguments

|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>vector_filename</code>    | The filename of the digital vector file                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <code>HLCheck = 0   1</code>    | Special flag which turns on checking for the H and L states for input signals (default = 0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <code>autostop=yes no</code>    | <ul style="list-style-type: none"><li>■ <b>no</b> tells the Spectre to use the end time from the <code>.tran</code> or <code>tran</code> statement (default).</li><li>■ <b>yes</b> tells Spectre to use the last specified time point in the vector file as the end time. If multiple <code>.vec</code> files are specified, and <code>autostop=true</code> is in one or all <code>.vec</code> statements, the simulator takes the longest time point available in the <code>.vec</code> files and uses it as the end time.</li></ul> <p><b>Note:</b> The <code>autostop</code> argument can also be used when loading <code>.vcd</code> and <code>.evcd</code> files.</p> |
| <code>insensitive=yes no</code> | Specifies whether the vector file content is considered case sensitive or insensitive. The default value is <code>yes</code> . For example, if you are in Spectre mode and a vector file is case sensitive, then use <code>insensitive=no</code> .                                                                                                                                                                                                                                                                                                                                                                                                                         |

## Example

### Spectre Syntax:

```
vec_include "vec1.vec" autostop=yes
```

### SPICE Syntax:

```
.vec "vec1.vec" autostop=yes
```

tells Spectre to replace the end time with the time from the `vec1.vec` file (that is, the time from the `vec1.vec` file is used as the transient simulation end time).

The digital vector file is described in detail in the following sections:

- [General Definition](#) on page 1011
- [Options for Digital Vector](#) on page 1013
- [Vector Patterns](#) on page 1016

- [Signal Characteristics](#) on page 1033
- [Tabular Data](#) on page 1054
- [Vector Signal States](#) on page 1055
- [Example of a Digital Vector File](#) on page 1056
- [Frequently Asked Questions](#) on page 1057

## General Definition

### Comment Line

A comment line begins with a semicolon ‘;’.

### Continuous Line

A continuous line is indicated by a plus sign ‘+’.

The maximum length of a line is 1024 characters. If a card is longer than 1024 characters, you need to use the continuous line for the card.



#### *Tip*

For a long identifier (for example, a 1280-bit vector bus) that cannot fit on a single line, use the back slash \ sign after the last bit. Do not use a space between the last bit and the \ sign. The other way to continue a line is by using a plus sign (+) sign at the beginning of the line. If you use a + sign, the continuous vector is treated as another vector bus.

### Signal Mask

A signal mask can be used to specify the effective range of the current statement in a vector file (statement applies to specific signals). Spectre matches the signals according to the signal definition order in the `radix`, `vname`, and `io` statements. For the corresponding signal, a value of 1 indicates the statement is valid and a value of 0 indicates the statement is ignored. Based on the size of the vector specified in the `radix` statement, the signal mask value can range from 0 to 1 for 1bit, 0 to 3 for 2bit, 0 to 7 for 3bit, and 0 to 9 or A to F for 4bit.

### Example

```
radix 1 2 2 4
io i i i o
vname EN A[1:0] B[1:0] P[3:0]
```

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---

```
tunit ns
trise 1
tfall 1
vih 2.5
vil 0.0
vol 0.25
voh 2.25
vih 1.8 1 0 0 0
vih 3.3 0 0 3 0
trise 0.5 0 1 2 0
chk_window -1 5 1 0 0 0 F
```

The above example contains a single bit vector `EN`, and multiple bit vectors `A`, `B`, `P`. The mapping between the vectors and analog signals are as follows:

```
A[1:0] ==> A1 A0
A[[1:0]] ==> A[1] A[0]
```

When you specify a mask value to a 2-bit vector it expands as follows:

```
A[1:0] -> A1 A0
1 -> 0 1
3 -> 1 1
```

For a 4-bit vector:

```
P[3:0] -> P3 P2 P1 P0
1 -> 0 0 0 1
F -> 1 1 1 1
```

In above example, the global value of `vih` is 2.5V. With masks, `vih` is set to 1.8V for signal `EN`, and 3.3V for `B1` and `B0`. Other signals use the global value of 2.5V.

The `chk_window` statement specifies a window for vector checking. Spectre only checks the signal states within this window. The signal states outside the window are ignored. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all output vectors. The first parameter is `start_time` and defines the window, which starts at time `vec_time-start_time`. The second parameter is `end_time` and defines the window, which ends at time `vec_time+end_time`. In this example, the `start_time` is negative which means the checking window starts 1ns after vector time.

For more information about the statements used in this example, refer to [“Vector Patterns”](#) on page 1016 and [“Signal Characteristics”](#) on page 1033.



## Options for Digital Vector

In this section, options for digital vector format are introduced.

**Note:** These options are defined in netlist and not in the vector file.

Spectre supports the following vector checks (such as x state and z state) using the `options` statement:

- [vector\\_chk\\_zstate](#) on page 1014
- [vector\\_chk\\_xstate](#) on page 1015

## **vector\_chk\_zstate**

### ***Spectre Syntax***

```
Opt options vector_chk_zstate=0|1
```

### ***SPICE Syntax***

```
.option vector_chk_zstate=0|1
```

### **Description**

If set to 1, performs z state check. If the value is set to 0, z state checking is ignored. While performing z state checking, if the expected output is z, while the real output is not z state, the vector check generates an error in the *netlist.vecerr* report. The `vector_chk_zstate` statement is supported only in Spectre XPS S mode.

**Note:** The Z state definition is consistent with the [dyn\\_highz](#) circuit check. For example, if  $v_{th} < v_{gs} < \text{breakdown voltage}$ , the MOSFET is considered to be working either in triode region or saturation region and is considered as conducting, otherwise it is considered in z state.

## **vector\_chk\_xstate**

### ***Spectre Syntax***

Opt options vector\_chk\_xstate=0|1|2

### ***SPICE Syntax***

.option vector\_chk\_xstate=0|1|2

### **Description**

If set to 1, x state check is performed and node voltage between `vol` and `voh` is considered as x state. If set to 2, x state check is performed and node with multi-drive (more than one conducting path to drive the node) is considered as x state. It means that the logic value of such node may be uncertain in digital simulation. For `vector_chk_xstate=2`, the node value is not checked. If set to 0, the x state check is not performed.

## **Vector Patterns**

In this section, vector patterns (such as signal sizes, directions, names, and check windows) are defined. Spectre supports the following digital vector pattern statements:

- [radix](#) on page 1017
- [sig\\_type](#) on page 1018
- [io](#) on page 1019
- [vname](#) on page 1020
- [hier](#) on page 1022
- [tunit](#) on page 1023
- [chk\\_ignore](#) on page 1024
- [chk\\_window](#) on page 1025
- [enable](#) on page 1029
- [period](#) on page 1031
- [mask](#) on page 1032

## radix

```
radix vector1_size1 vector2_size2 ...vector_sizeN
```

### Description

Specifies the size (in bits) of the vector. This statement must be located before any other statements, and can only be specified once. Valid vector sizes include 1 (binary), 2, 3 (octal), or 4 (hexadecimal).



#### Tip

If the `radix` of the vector is larger than 1, the name of this vector specified in `vname` must be indexed as `[msb:lsb]` or `[lsb:msb]`. If the `radix` is 4, the `vname` can use names such as `name[3:0]` and `name[0:3]`.

### Examples

The following example

```
radix 2 2 4
```

contains three vectors: Two 2-bit vectors and one 4-bit vector.

**Note:** The examples presented in the rest of this chapter follow this format.

In the next example

```
radix 2 11 1111
```

also contains three vectors, two 2-bit vectors and one 4-bit vector, but in a different format.

## sig\_type

sig\_type L | R

### Description

The `sig_type` statement defines the signal type. It can be `L` (logic) or `R` (real). The `R` (real) type signal can be defined as input or output. If a signal is defined as two different `sig_type`, it can be defined twice as output signal. This feature allows you to create two output check windows for the same signal, as logic value and real number value.

### Example

```
radix 1 1 1
vname vout vout vin
io o o i
sig_type r l l
tunit 10ns
chk_window -10 30 1 period=100 first=5 duration=2 reltol=0.1 abstol=0.01 ; duration
is 2*10ns=20ns, reltol is 10% and abstol is 10mV.
; data
0 0 01
100 1.2 10 ; For signal 'vout', it is expected high in logic value and
1.2V in real value
200 1.3 10 ; The expected real value of signal 'vout' is 1.3V, still
high as logic value
```

## io

```
io type1 type2 ...typeN
```

### Description

The `io` statement defines the type of vector. It can be the `i` (input), `o` (output), or `b` (bidirectional), or `u` (unused) type. If the vector type is `u`, it will always be converted to the value specified in `val`. If this statement is specified more than once, the last value is used.

### Notes

- Use the `enable` statement to specify the control signal for the bidirectional vector (`b`). If this specified control signal is not found, Spectre issues an error.
- If the control signal of the bidirectional vector is not specified by the `enable` statement, Spectre treats it as an input signal.

### Example

```
radix 2 2 4
io i i o
```

The first and second vectors are input vectors, and the third vector is an output vector.

## vname

*vname name1 name2 ... nameN*

### Description

The `vname` statement assigns a name to each vector. For a single bit vector, it can have the following naming format: `Va`, `Va[0:0]`, or `Va[[0:0]]`. For multiple bit vectors, the naming formats include: `Va[2:0]`, `Va[[2:0]]`, `Va[0:2]`, or `Va[[0:2]]`. Each naming format is given a different resulting name. If multiple brackets are used, then the following rule is applied:

- The outer brackets define the bus notation. They are kept as bus delimiter in the signal name.
- The inner brackets define the range of the bus signal. They are not used as part of the signal name.

If the `vname` statement is specified more than once, the last value is used.

Hierarchical signal names are also supported by `vname`. That is, you can apply vector stimuli or perform a vector check on the internal signals of instances. When mapping hierarchical signal names, the default delimiter is a period (.). You can change the value of the delimiter using the `hier_delimiter` option in the analog netlist file (see [Specifying Hierarchical Delimiters](#) on page 585). The `hier` statement can be used to enable or disable this option.

**Table D-1 vname Vector Names**

| Naming Format                       | Resulting Names                                                                                                   |
|-------------------------------------|-------------------------------------------------------------------------------------------------------------------|
| <code>Va[2:0]</code>                | <code>Va2</code> , <code>Va1</code> , <code>Va0</code>                                                            |
| <code>Va[[2:0]]</code>              | <code>Va[2]</code> , <code>Va[1]</code> , <code>Va[0]</code>                                                      |
| <code>Va[0:2]</code>                | <code>Va0</code> , <code>Va1</code> , <code>Va2</code>                                                            |
| <code>Va[[0:2]]</code>              | <code>Va[0]</code> , <code>Va[1]</code> , <code>Va[2]</code>                                                      |
| <code>Va&lt;1:0&gt;</code>          | <code>Va1</code> , <code>Va0</code>                                                                               |
| <code>Va &lt;[1:0]&gt;</code>       | <code>Va&lt;1&gt;</code> , <code>Va&lt;0&gt;</code>                                                               |
| <code>Va [ &lt;1:0&gt; ]</code>     | <code>Va[1]</code> , <code>Va[0]</code>                                                                           |
| <code>Va &lt;&lt;1:0&gt;&gt;</code> | <code>Va&lt;1&gt;</code> , <code>Va&lt;0&gt;</code>                                                               |
| <code>X1.Va[0:2]</code>             | Internal signals <code>Va0</code> , <code>Va1</code> , and <code>Va2</code> of instance <code>X1</code>           |
| <code>TOP.X1.Va[[0:2]]</code>       | Internal signals <code>Va[0]</code> , <code>Va[1]</code> , and <code>Va[2]</code> of instance <code>TOP.X1</code> |





## Tip

If the radix of the vector is larger than 1, the name of the vector specified in `vname` must be indexed as `[msb:lsb]` or `[lsb:msb]`. If `radix` is 4, `vname` can use names such as `name[3:0]` and `name[0:3]`.

## Examples

In the following example

```
radix 2 2 4
io i i i
vname va[1:0] vb[[1:0]] vc[[0:3]]
```

tells Spectre that the voltage sources in the first vector are named `va1` and `va0`. Voltage sources in the second vector are connected to `vb[1]` and `vb[0]`. The third vector has voltage sources with the names `vc[0]`, `vc[1]`, `vc[2]`, and `vc[3]`.

In the next example

```
radix 2 2 4
io i i o
vname X1.va[1:0] X2.vb[[1:0]] X1.X3.vc<[0:3]>
hier 1
```

tells the simulator the voltage sources in the first vector are mapped to internal signals `va1` and `va0` of instance `X1`. Voltage sources in the second vector are connected to `v[1]` and `vb[0]` of instance `X2`. The third vector defines the output vector check for signals `vc<0>`, `vc<1>`, `vc<2>`, and `vc<3>` of instance `X1.X3`.

## hier

```
hier 0|1
```

## Description

This option is used to specify whether or not the hierarchical signal name mapping feature is enabled. If `hier` is set to 0, the hierarchical delimiter (for example, signal period or `.`) is considered to be part of the signal name. The default value is 1 (hierarchical signal name mapping enabled). If this statement is specified more than once, the last value is used.

## Example

```
radix 2
io i
hier 0
vname X1.va[1:0]
```

tells Spectre to connect the voltage sources with the `X1.va1` and `X1.va0` signals located in the top level of the analog netlist file.

## tunit

`tunit time_unit`

### Description

Sets the time unit for all time related variables. The time unit can be one of the following: `fs` (femto-second), `ps` (pico-second), `ns` (nano-second), `us` (micro-second), and `ms` (milli-second). The default time unit is 1 ns. If this statement is specified more than once, the last value is used.

### Example

```
tunit 1.5ns
```

## chk\_ignore

```
chk_ignore start_time end_time [mask1 mask2 ... maskN]
```

### Description

The `chk_ignore` statement specifies a window for ignoring output vector checks. A mask can be provided to specify which vector and bit to apply. If the mask is not specified, the setting applies to all output vectors. The `start_time` and `end_time` arguments must be specified. To define multiple time windows for ignoring output vector checks, use multiple `chk_ignore` statements.

### Arguments

|                         |                                                                                                                                                                                                                     |
|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>start_time</code> | Defines the start time for the window used to ignore the output vector checks (use <u>tunit</u> to define the <code>start_time</code> units).                                                                       |
| <code>end_time</code>   | Defines the end time for the window used to ignore the output vector checks (use <u>tunit</u> to define the <code>end_time</code> units). You can use <code>end_time=-1</code> to ignore the entire transient time. |

### Example

```
tunit 1n
chk_ignore 0 100 0F30 ; 0F30 is a signal mask
chk_ignore 3e+2 500 0F30
chk_ignore 0 -1 F000 ; F000 is a signal mask
```

tells Spectre to ignore the output vector check for signals specified by the mask `0F30` in the time windows 0 ns to 100 ns and 300 ns to 500 ns, and to ignore the entire transient time for the signals specified by the mask `F000`.

## chk\_window

```
chk_window start_time end_time steady [period=const [first=const]] [mask1 mask2 ... maskN] [duration=duration] [abstol=voltage] [reltol=value]
```

### Description

The `chk_window` statement specifies a window for vector checking. Spectre only checks the signal states within this window. The signal states outside the window are ignored. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all output vectors. The checks occur at every time point specified in the vector file or as defined by the `period` and `first` arguments.

Setting the `period` argument activates periodic window checking. If `period` is not defined, the `first` argument is ignored by the simulator.

### Notes

- To activate periodic window checking, you need to include the "period=" and "first=" keywords.
- Parameters and expressions are supported for the `start_time`, `end_time`, `period`, and `first` arguments (see [“Examples”](#) on page 1026 for more information about parameters and expressions syntax).

### Arguments

|                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>start_time</code>     | Defines the window start time at which the window starts at time <code>vec_time-start_time</code> . If the <code>period</code> argument is defined, <code>vec_time</code> is the first time point defined by the <code>first</code> argument, and the vector checks are repeated according to the value of <code>period</code> . If the <code>period</code> argument is not defined, <code>vec_time</code> is the time point defined in the vector file. |
| <code>end_time</code>       | Defines the window end time at which the window ends at time <code>vec_time+end_time</code> .                                                                                                                                                                                                                                                                                                                                                            |
| <code>steady = 0   1</code> | Can be set to 0 or 1. If set to 0, then the vector check passes as long as the signal has reached the desired state once. If set to 1, then the signal remains in the desired state for the entire window period to pass the vector check.                                                                                                                                                                                                               |
| <code>period</code>         | Activates periodic window checking and defines its time period.                                                                                                                                                                                                                                                                                                                                                                                          |

|                       |                                                                                                                                                                                                                                                                                               |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>first</code>    | Defines the first check point for periodic window checking (only valid when the <code>period</code> argument is also defined).                                                                                                                                                                |
| <code>duration</code> | Works with <code>steady=0</code> . If any time point of transient results exceeds the tolerance, the accumulation of duration is reset. For <code>steady=1</code> , it means the signal needs to be within the tolerance for the whole check window; <code>duration</code> itself is ignored. |
| <code>abstol</code>   | Defines the absolute tolerance for the real value.                                                                                                                                                                                                                                            |
| <code>reltol</code>   | Defines the relative tolerance for the real value.                                                                                                                                                                                                                                            |

**Note:** The combined error tolerance is given by:

$$\text{Error\_tol} = \text{abstol} + \text{expected\_value} * \text{reltol}$$

Normally, it is recommended that the length of the check window is less than the data period. This means that for one time window, the expected value does not change. Spectre XPS has been enhanced to separate the check window when the expected data value changes. As a result, two values are supported now, and it is still valid for real number in the vector. Changing the values more than twice in a check window is not supported.

For example, the following is not supported:

The check window is 100ns. However, for every 10ns, the output of vector real number changes.

Here, you need to change the length of `check_window` too, for example to 10ns.

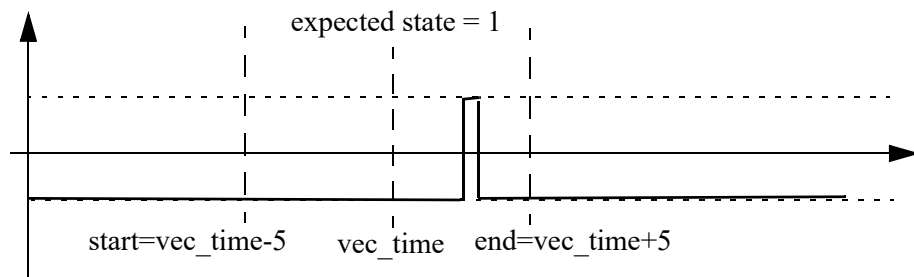
### Examples

The following example

```
chk_window 5 5 0
```

tells Spectre to set the steady state to 0, so the waveform passes the vector check (see [Figure D-1](#) on page 1027).

**Figure D-1 Vector Check with `chk_window` Steady State Set to 0**

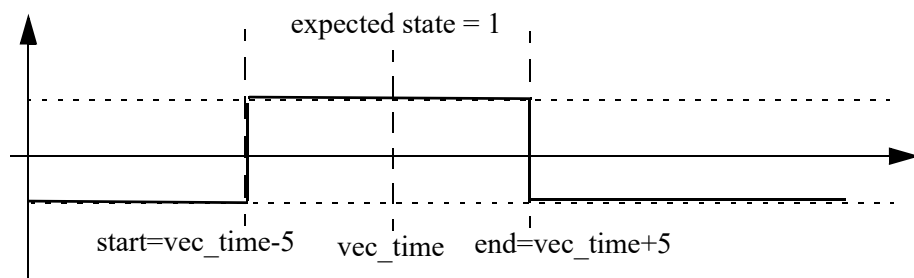


In the next example

```
chk_window 5 5 1
```

tells Spectre to set the steady state to 1, which means the signal needs to stay at state 1 for the whole window period to pass the vector check, as shown in [Figure D-2](#) on page 1027. If the signal is as shown in [Figure D-1](#) on page 1027, the vector check fails.

**Figure D-2 Vector Check with `chk_window` Steady State Set to 1**



In the next example

```
radix 1 1 1 1
vname ph1 d q qb
io i i o o
tunit 10ns
chk_window -10 30 1 period=100 first=5 0 0 1 0
```

tells Spectre to activate periodic window check for signal `q`. The vector check points start at 50 ns and repeat every 1 us.

In the next example

```
chk_window -10 30 1 first=5 0 0 1 0
```

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tells Spectre to ignore the `first` argument because a valid `period` argument has not been specified.

In the next example

```
tunit 1ns
param myfadd(x,y)='x + y'
param mystartt=1.5 mystopt='(myfadd(mystartt, 50.5))'
chk_window mystartt mystopt 1
```

tells Spectre to set the steady state to 1, the start time for `chk_window` to 1.5 ns, and the end time to 52 n (this example shows the `chk_window` parameters and expressions syntax).

In the following example:

```
radix 1 1 1 1 1
vname ph1 d q qb q_real
sig_type 1 1 1 1 r
io i i o o o
tunit 10ns
chk_window -10 30 1 period=100 first=5 duration=2 reltol=0.1 abstol=0.01 ; duration
is 2*10ns=20ns, reltol is 10% and abstol is 10mV.

; data
0 0000 0
100 1110 1.2 ; the expected value is 1.2V, so 1.2±(1.2*10%+0.01) (1.2-
0.13)V~(1.2+0.13)V is a pass.
200 1110 1.3 ; the expected value is 1.3V, so 1.3±(1.3*10%+0.01) (1.3-
0.14)V~(1.3+0.14)V is a pass.
```



## enable

```
enable 'enable_signal_expr' [mask1 mask2 ... maskN]
```

### Description

The `enable` statement connects the enable signal, or enable signal expression, to the bidirectional vector. The resulting value 1 (H) enables the output signal. The controlled bidirectional signal is regarded as an input for other values.

You can provide a mask to specify to which vector and bit the enable signal expression applies. If the mask is not specified, the setting applies to all bidirectional vectors. Also, if this statement is specified more than once, the last value is used.

The enable signal can be used in a vector or an analog netlist file. When an enable signal is used in an analog netlist file, it can also be defined as an output signal for a vector check or only used as an enable signal. The `avoh` and `avol` statements can be used to define the logic high and low voltage thresholds for the analog signal.

**Note:** The enable signal cannot be defined as a bidirectional signal.

Bit-wise logic operators are supported in an enable signal expression: `&` (AND), `|` (OR), `^` (XOR), and `~` (NOT). Additional operators can be created using a combination of the supported operators. The order of processing for the logic operators is NOT > AND > OR, XOR (OR and XOR are processed at the same time). You can use parentheses `()` around the operators to change the processing order.

**Note:** You need to use single quotation marks `' '` for enable signal expressions.

### Examples

The following example

```
radix 1 1 1 1
io i i b o
vname en in bi out
enable en 0 0 1 0
```

tells Spectre to set `en` as the enable signal for `bi`, and when `en` is in 1 (or H) state, `bi` becomes the output signal. When `en` is in 0 (or L, X, U) state, `bi` changes to the input signal. When `en` is in Z state, the `bi` (input and output) signal also changes to Z state.

In the next example

```
radix 1 1 1
```

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---

```
io i b o
vname en bi out
enable ~en 0 1 0
```

tells Spectre to set `en` as the enable signal for `bi`. Unlike the [first example](#), this enable signal name contains a `~` sign, which reverses the state to control the bidirectional signal. Now when the enable signal is in 1 (or H) state, the `bi` becomes an input signal.

In the next example

```
radix 1 1 1
io b b o
vname bi_1 bi_2 out
enable ana_en1 0 1 0
enable `(ana_en1 | X1.ana_en2) & out' 1 0 0
```

tells Spectre that the `ana_en1` and `X1.ana_en2` enable signals originate in the analog netlist file, and `X1.ana_en2` is a hierarchical signal. Although the `out` signal is used as an enable signal, the simulator still performs a vector check.

## period

`period time`

### Description

The `period` statement is used to specify the time interval for tabular data, so that the absolute time is not needed.

If `period` is not specified, then the absolute time must be specified in the tabular data. If it is specified more than once, the last value is used.

### Example

`period 10.0`

tells Spectre that the signal period is 10 ns and the absolute time points are unnecessary.

## mask

```
mask mask_name mask_pattern
mask mask_name name1 name2 ... nameN
```

## Description

The mask statement defines the mask name to represent a user-defined mask pattern.

The statement starts with the keyword `mask`, followed by a mask name and the mask pattern. The mask pattern can be specified using either the values or the signal names. If the signal nodes are used to describe the mask pattern, a logic 1 is set to each signal node at the corresponding column location. Any unspecified column defaults to logic 0.

## Arguments

|                               |                                                                                                       |
|-------------------------------|-------------------------------------------------------------------------------------------------------|
| <code>mask_name</code>        | Defines the name of the user-specified mask.                                                          |
| <code>mask_pattern</code>     | Defines the bit pattern for the mask.                                                                 |
| <code>name1 name2, ...</code> | Defines the signal names being part of the pattern. Bus signals are supported in the name definition. |

## Example

```
signal n1 n2 n3 n4 bus<[0:3]>
radix 1111 4
mask mask1 0101
mask mask2 n1 n2
mask mask3 bus<[0:3]>
trise 0.05
trise 0.1 mask1
tfall 0.08
tfall 0.15 mask2
tfall 0.2 mask3
```

In the above example `mask1` is assigned pattern `0101` which enables signals `n2` and `n4`. `mask2` contains signal `n1` and `n2`. `trise=100ps` is assigned to signal `n2` and `n4`, while all other signals use a `trise` of `50ps`. `tfall=150ps` is assigned to signal `n1` and `n2` and `tfall=200ps` is assigned to bus signal `bus<0>`, `bus<1>`, `bus<2>`, `bus<3>`, and `bus<4>`, while all other signals use `80ps`.

## Signal Characteristics

In this section, signal characteristics containing various attributes for input or output signals (such as delay, rise or fall time, voltage thresholds for logic low and high, and driving ability) are defined. For most of these statements, the mask can be used to apply the specified characteristics to the corresponding signals. The statements are organized into three groups:

- [Timing](#) on page 1034
- [Voltage Threshold](#) on page 1041
- [Driving Ability](#) on page 1050

**Note:** In the following examples for time-related statements, the time unit is 1 ns if the statement is not specified with tunit.

## Timing

Timing characteristics of input or output signals (such as delay, rise time, and fall time) can be specified using the following statements. The values of these statements can be positive or negative. For the delay timing characteristics, the negative value is used to advance the signals by a specified time. For the rise and fall timing characteristics, the negative value is the same as the positive one.

- [idelay](#) on page 1035
- [odelay](#) on page 1036
- [tdelay](#) on page 1037
- [slope](#) on page 1038
- [tfall](#) on page 1039
- [trise](#) on page 1040

**Note:** Spectre checks whether the values of the `trise`, `tfall`, and `slope` statements are reasonable (warning message is issued when the defined value is too small or large).

## idelay

```
idelay time_value [mask1 ... maskN]
```

### Description

The `idelay` statement specifies the delay time for the corresponding input signal. If a bidirectional signal is specified, this applies only to the input stage of the bidirectional signal. The default value is 0.0, if `idelay` or `tdelay` is not set.

### Example

```
idelay 5.0
```

tells Spectre to delay all input signals by 5 ns, whereas

```
idelay -5.0
```

tells Spectre to advance all input signals by 5 ns.

## odelay

```
odelay time_value [mask1 ... maskN]
```

### Description

The `odelay` statement specifies the time delay for the corresponding output signal. If a bidirectional signal is specified, this applies only to the output stage of the bidirectional signal. The default value is 0.0, if `odelay` or `tdelay` is not set.

### Example

```
odelay 5
```

tells Spectre to delay all output signals by 5 ns, whereas

```
odelay -5.0
```

tells the simulator to advance all output signals by 5 ns.



## tdelay

`tdelay time [mask1 mask2 ... maskN]`

### Description

The `tdelay` statement specifies the delay time for corresponding vectors. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all vectors (input, output, and bidirectional).

If `tdelay` is not specified, the default value is 0.0. If this statement is specified more than once, the last value is used for the active mask. This statement can also overrule the value previously set by the `idelay` or `odelay` statements.

### Examples

```
tdelay 5.0
```

tells Spectre to advance all signals by 5 ns.

```
tdelay -5.5 3 0 F
```

tells Spectre to advance all signals, specified with a mask, by 5.5 ns.

## slope

```
slope time [mask1 mask2 ... maskN]
```

### Description

The `slope` statement sets the input vectors rise and fall time. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

If this statement is not specified, then the default value of 0.1 ns is used. If this statement is specified more than once, the last value is used for the active mask. This statement can also overrule the value previously set by the `trise` or `tfall` statements.

### Examples

```
slope 0.05
```

or

```
vname va[1:0] vb[[1:0]] vc[[0:3]]
io i i o
slope .025 1 3 5
```

The least significant bit, `va0`, of the first input vector and the two bits, `vb[1]` and `vb[0]`, of the second input vector have a `trise` and `tfall` of 0.025 ns. The third vector is an output vector (specified in the `io` statement), so it is not affected by the `slope` statement.

## tfall

```
tfall time [mask1 mask2 ...maskN]
```

### Description

The `tfall` statement specifies the falling time of the input vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

The value from the `slope` statement is used, if `tfall` is not specified. If this statement is specified more than once, the last value is used for the active mask. This statement can also overrule the value previously set by the `slope` statement.

### Examples

The following example

```
tfall 0.05
```

tells Spectre that all input vectors have a fall time of 0.05 ns.

In the next example

```
vname va[1:0] vb[[1:0]] vc[[0:3]]
tfall 0.1 0 2 0
```

the most significant bit, `vb[1]`, of the second input vector has a fall time of 0.1 ns. The fall time of `vb[0]` and other input vectors remains the same.

## trise

```
trise time [mask1 mask2 ...maskN]
```

### Description

The `trise` statement specifies the rise time of the input vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

If `trise` is not specified, the value from the `slope` statement is used. If this statement is specified more than once, the last value is used for the active mask. This statement can also overrule the value previously set by the `slope` statement.

### Examples

The following example

```
trise 0.1
```

or

```
trise -0.1
```

tells Spectre that all input vectors have a rise time of 0.1 ns.

In the next example

```
vname va[1:0] vb[[1:0]] vc[[0:3]]
trise 0.1 0 3 0
```

the two bits of the second input vector has a rise time of 0.1 ns and the `trise` of the other input vector remains the same.

## **Voltage Threshold**

When converting input vectors to stimuli or performing an output vector check, the voltage threshold for logic low and high can be specified using the following statements:

- vih on page 1042
- vil on page 1043
- voh on page 1044
- vol on page 1045
- avoh on page 1046
- avol on page 1047
- vref on page 1048
- vth on page 1049

## **vih**

`vih voltage [mask1 mask2 ...maskN]`

### **Description**

The `vih` statement specifies the logic high voltage of the input vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

If `vih` is not specified, the default voltage is 3.3. If this statement is specified more than once, the last value is used for the active mask.

### **Examples**

`vih 5.0`

or

`vih 5.5 3 1 0`

## **vil**

```
vil voltage [mask1 mask2 ... maskN]
```

### **Description**

The `vil` statement specifies the logic low voltage of the input vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

If `vil` is not specified, the default voltage is 0.0. If this statement is specified more than once, the last value is used for the active mask.

### **Examples**

```
vil 0.25
```

or

```
vil 0.5 3 0 0
```

## voh

*voh voltage [mask1 mask2 ... maskN]*

### Description

The `voh` statement specifies the logic high voltage of the output vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all output vectors.

If `voh` is not specified, the default voltage is 3.3. If this statement is specified more than once, the last value is used for the active mask.

### Examples

```
voh 5.0
```

or

```
voh 5.5 0 0 F
```



## vol

`vol voltage [mask1 mask2 ... maskN]`

### Description

The `vol` statement specifies the logic low voltage of the output vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all output vectors.

If `vol` is not specified, the default voltage is 0.0. If this statement is specified more than once, the last value is used for the active mask.

### Example

```
vol = 0.05
voh = 1
```

tells Spectre to interpret all output signals with values below 0.05 V as 0, print all signals above 1 V as 1, and all signals between 0.05 V and 1 V are U.

## avoh

```
avoh voltage [signal_name1 signal_name2 ... signal_nameN]
```

### Description

The `avoh` statement specifies the logic high voltage of the signal from the analog netlist file, which is not defined in the `radix`, `vname`, or `io` statements. You can provide signal names to specify the valid scope for `avoh` (wildcards are supported). A period ( `.` ) can be used as the hierarchical delimiter to specify the hierarchical signal. If a signal name is not used, the setting applies to all analog signals used in the vector file.

**Note:** A mask cannot be used to specify which vector and bit to apply to the signal (different behavior from other vector format statements).

### Example

```
avoh = 1 ana_en* X1.Enanble
```

tells Spectre that analog signals `ana_en*` and `X1.Enanble` have a logic high voltage of 1.0.

## avol

```
avol voltage [signal_name1 signal_name2 ... signal_nameN]
```

### Description

The `avol` statement specifies the logic low voltage of the signal from the analog netlist file, which is not defined in the `radix`, `vname` or `io` statements. You can provide signal names to specify the valid scope for `avol` (wildcards are supported). A period (.) can be used as the hierarchical delimiter to specify the hierarchical signal. If a signal name is not used, the setting applies to all analog signals used in the vector file.

**Note:** A mask cannot be used to specify which vector and bit to apply to the signal (different behavior from other vector format statements).

### Example

```
avol = 0.5 ana_en* X1.Enable
```

tells Spectre that analog signals `ana_en*` and `X1.Enable` have a logic low voltage of 0.5.

## vref

```
vref node_name [mask1 mask2 ... maskN]
```

### Description

The `vref` statement sets the reference node of the input vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

If `vref` is not specified, the default value is 0 (that is, the ground). If this statement is specified more than once, the last value is used for the active mask.

### Examples

The following example

```
vref 0
```

tells Spectre to set the negative node of the vector source to ground.

In the next example

```
vref vss
```

tells the simulator to set the negative node of the vector source to `vss`.

**Note:** Spectre only supports reference node to ground. References to other nodes causes the simulator to issue error messages.

## vth

*vth voltage [mask1 mask2 ... maskN]*

### Description

The `vth` statement sets the threshold voltage of the output vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all output vectors.

If `vth` is not specified, the default value is 1.65. If this statement is specified more than once, the last value is used for the active mask.

### Examples

```
vth 2.5
```

or

```
vth 2.7 0 0 8
```

## **Driving Ability**

For input stimuli, the output resistance of vector sources can affect Spectre simulation results. To specify the driving ability of vector sources, use the following statements:

- hlz on page 1051
- outz on page 1052
- triz on page 1053

## hlz

`hlz resistance [mask1 mask2 ... maskN]`

### Description

The `hlz` statement specifies the output resistance for the corresponding input vector, but unlike `outz`, this output resistance only applies to the H and L states of the vector. This resistance overwrites the resistance for the H and L states set by `outz`.

You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

If `hlz` is not specified, the default value follows `outz`. If `hlz` is set to 0, Spectre uses 0.01 instead. If this statement is specified more than once, the last value is used for the active mask.

### Examples

`hlz 1meg`

or

`hlz 4.7k 2 2 0`

## outz

`outz resistance [mask1 mask2 ... maskN]`

### Description

The `outz` statement specifies the output resistance for the corresponding input vector. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

If `outz` is not specified, the default value is 0.01. If `outz` is set to 0, the default value is used. If this statement is specified more than once, the last value is used for the active mask.

### Examples

`outz 1meg`

or

`outz 5.5meg 2 2 0`



## triz

```
triz resistance [mask1 mask2 ... maskN]
```

## Description

The `triz` statement specifies the output impedance when the corresponding input vectors are in tri-state. You can provide a mask to specify which vector and bit to apply. If the mask is not specified, the setting applies to all input vectors.

If `triz` is not specified, the default value is 1,000 Meg. If `triz` is set to 0, Spectre uses 0.01 instead. Also, if this statement is specified more than once, the last value is used for the active mask.

## Examples

```
triz 2000meg
```

or

```
triz 550meg 2 2 0
```

## Tabular Data

This section describes the values of signals at specified times (absolute or period time modes). For periodic signals, it is unnecessary to specify the absolute time at each time point. The `period` statement can be used to specify the signal period.

### Absolute Time Mode

The period is not specified.

```
Time1 vector1_value1 vector2_value1 vector3_value1
Time2 vector1_value2 vector2_value2 vector3_value2
...
TimeN vector1_valueN vector2_valueN vector3_valueN
```

### Period Time Mode

The period is specified.

```
vector1_value1 vector2_value1 vector3_value1
vector1_value2 vector2_value2 vector3_value2
...
vector1_valueN vector2_valueN vector3_valueN
```

`vector_value` can be 0-9, A-F, Z, X, L, H, or U, and is dependent on how `radix` is set.

### Description

Tabular data is used to describe the waveform of voltage sources.

### Examples

```
; format: time vector
0 000101010
10 011010101
20 000101010
```

or

```
; format: vector
00101010
11010101
00101010
```

**Note:** This example assumes the period has been set by `period 10.0`.

or

```
; format: time vector
10 02A
20 315
30 02A
```

## Valid Values

The valid values in tabular data depend on the `radix` statement setting.

**Table D-2 Tabular Data Valid Values**

| Value Specified in <code>radix</code> Statement | Valid Value |
|-------------------------------------------------|-------------|
| 1                                               | 0, 1        |
| 2                                               | 0-3         |
| 3                                               | 0-7         |
| 4                                               | 0-9, A-F    |

The values specified in the table above are converted into 0 and 1 states by Spectre. The simulator also accepts L, H, Z, X, and U values when `radix=1`.

## Vector Signal States

### Input

Spectre accepts the following signal states for input vector signals.

**Table D-3 Input Vector Signal States**

| Signal State | Description                |
|--------------|----------------------------|
| 0            | Drive to ZERO (GND)        |
| 1            | Drive to ONE (VDD)         |
| Z, z         | Floating to high-impedance |
| X, x         | Drive to ZERO (GND)        |

**Table D-3 Input Vector Signal States, *continued***

| Signal State | Description                     |
|--------------|---------------------------------|
| L, l         | Resistively drive to ZERO (GND) |
| H, h         | Resistively drive to ONE (VDD)  |
| U, u         | Drive to ZERO (GND)             |

The resistance values of **L** and **H** are set by the **hlz** statement, and the impedance value of **Z** is set by the **triz** statement.

## Output

Spectre accepts the following signal states for output vector signals.

**Table D-4 Output Vector Signal States**

| Signal State | Description              |
|--------------|--------------------------|
| 0            | Expects ZERO             |
| 1            | Expects ONE              |
| Z, z         | Accepts any signal state |
| X, x         | Accepts any signal state |
| U, u         | Accepts any signal state |

## Example of a Digital Vector File

This is a basic digital vector file that shows how each Spectre statement is used.

```
; radix specifies the number of bit of the vector.
radix 2 2 4
; io defines the vector as an input or output vector.
io i i o
; vname assigns the name to the vector.
vname A[1:0] B[1:0] P[3:0]
; tunit sets the time unit.
tunit ns
; trise specifies the rise time of each input vector.
trise 1
```

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```
; tfall specifies the fall time of each input vector.
tfall 1
; vih specifies the logic high voltage of each input vector.
vih 2.5
; vil specifies the logic low voltage of each input vector
vil 0.0
; voh specifies the logic high voltage of each output vector
voh 2.0
; vol specifies the logic low voltage of each output vector
vol 0.5
0 0 0 x
200 3 3 x
400 1 2 0
600 2 1 9
800 3 1 2
1000 1 3 2
1200 2 2 3
1400 3 2 3
1600 2 3 4
1800 0 0 6
2000 0 0 7
```

## Frequently Asked Questions

### Can I replace the bidirectional signal with an input and output vector?

Bidirectional signals can be divided into two columns, one for an input vector and the other for an output vector (the enable signal is no longer needed). The same `vname` and signal name is used for the input and output vectors.

For the input stage, the value of the output vector must be `x` or `z` (output vector check is not performed). For the output stage, the value of the input vectors must be `z` or `z` (no stimulus for this signal). For example:

```
radix 1 1 1 1
io i o i o
vname DI DO DQ DQ
tunit ns
0 0 1 0 x
100 1 0 1 x
200 0 1 0 x
```

```
300 0 0 z 1
400 1 1 z 0
500 0 0 z 1
```

## How do I verify the input stimuli?

Use `.probe tran v(*) depth=1` to probe the top-level signals and then check the waveform outputs with the Virtuoso Visualization and Analysis or SimVision viewers.

**Note:** The signal names are case sensitive.

Review the log file to check if the signals defined in the digital vector file match those defined in the analog netlist file.

- When the signal is defined in the vector file, but not in the analog netlist file, a warning message appears stating that the VCD or VEC file is not defined in the netlist file.
- When the input signal is used in the analog netlist file, but does not match the one located in the vector file, check the list of dangling nodes or no DC path to ground in the log file.

## How do I verify the vector check?

A `<netlistName>_<tranName>.veclog` file is generated at the location specified by Spectre `option-raw` statement if there are any vector checks. A `<netlistName>_<tranName>.vecerr` file is also generated when errors occur during the vector check. Refer to these two files for detailed information about the vector check. Here, `<netlistName>` is the name of the netlist and `<tranName>` is the name of the transient analysis.

When the signal is defined in the vector file, but not in the analog netlist file, the simulator issues a warning message in the log file that states the signal node is missing from the netlist file.

---

## Verilog Value Change Dump Stimuli

---

This chapter introduces the Verilog<sup>®</sup> value change dump (VCD) and extended VCD (EVCD) file formats, as used in the Spectre<sup>®</sup> circuit simulator, and provides illustrations to explain the signal information file.

The VCD file (ASCII format) contains information about value changes for selected variables in the circuit design. Spectre supports two types of VCD files:

- **Four-state** – represents variable changes in 0, 1, x (unknown or “not needed”) and z (tri-state) without providing strength information and port direction
- **Extended** – represents variable changes in all states and provides strength information and port direction

For more information about EVCD file format, refer to [“Enhanced VCD Commands”](#) on page 1104.

## Processing the Value Change Dump File

To process VCD or EVCD files in Spectre, the following statements need to be specified in the netlist file:

### Spectre Syntax

```
vcd_include "vcd_filename" "signal_info_filename" [autostop=yes|no]
 [insensitive=yes|no]
```

### SPICE Syntax

```
.vcd "vcd_filename" "signal_info_filename" [autostop=yes|no]
 [insensitive=yes|no]
```

or

### Spectre Syntax

```
evcd_include "evcd_filename" "signal_info_filename" [autostop=yes|no]
 [insensitive=yes|no]
```

## SPICE Syntax

```
.evcd "evcd_filename" "signal_info_filename" [autostop=yes|no]
 [insensitive=yes|no]
```

**Note:** A period (.) is required when using SPICE language syntax (for example, .vcd or .evcd).

Spectre replaces the end time in the .tran or tran statement with the time specified in the .vcd/.evcd file when autostop=yes (default is no). If no is specified, the simulation time specified in the .tran or tran statement remains unchanged. For more information on autostop, refer to the Transient Analysis (tran) section in the *Spectre Circuit Simulator Reference manual*.

Each vcd or evcd statement can only specify one VCD or EVCD file. If a netlist file needs to include multiple VCD or EVCD files, multiple vcd or evcd statements must be used. For example, if a netlist file contains three VCD files, it needs three vcd statements (use the same netlist file format for EVCD files).

### Spectre Syntax:

```
Statement 1: vcd_include "file1.vcd" "file1.signal"
Statement 2: vcd_include "file2.vcd" "file2.signal"
Statement 3: vcd_include "file3.vcd" "file3.signal"
```

### SPICE Syntax:

```
Statement 1: .vcd "file1.vcd" "file1.signal"
Statement 2: .vcd "file2.vcd" "file2.signal"
Statement 3: .vcd "file3.vcd" "file3.signal"
```

**Note:** A netlist file can include multiple VEC, VCD, and ECVD files.

VCD and EVCD formats are widely used in digital circuit design and contain different kinds of information for transistor level simulation. You need to provide signal information, such as timing characteristics, voltage threshold, and driving ability of input signals for each VCD or EVCD file. Since VCD and EVCD formats are compatible, Spectre can share the same signal information file.

By default, Spectre handles the VCD and EVCD file content as case insensitive (insensitive=yes). Case sensitivity can be set using the insensitive=no option.

## VCD Commands

- [VCD File Format](#) on page 1061
- [Definition Commands](#) on page 1062



- [Data Commands](#) on page 1072

## VCD File Format

### Continuous Line

The continuous line symbol is the back slash (\) sign and is rarely used in the VCD file. The beginning of a card is indicated by the `$command` keyword (for example, `.$var`), and ends with the `$end` keyword. If an identifier is longer than 1024 characters, and does not fit into a single line, the \ sign must be used to continue the line.

### \$comment

```
$comment comments $end
```

### *Description*

Comments need to be enclosed within the `$comment` and `$end` commands.

### *Example*

```
$comment
This is a test line.
$end
```

## Definition Commands

In the definition section, the VCD command keywords used to indicate the start of a card begin with a dollar (\$) sign. VCD definition commands include: `$comment`, `$date`, `$enddefinitions`, `$scope`, `$timescale`, `$upscope`, `$var`, and `$version`. The end of a card is marked with an `$end` keyword. Multiple lines can be placed between the `$command` and `$end` commands.

Spectre supports the following VCD definition section commands:

- [\\$date](#) on page 1063
- [\\$enddefinitions](#) on page 1064
- [\\$scope](#) on page 1065
- [\\$timescale](#) on page 1066
- [\\$upscope](#) on page 1068
- [\\$var](#) on page 1069
- [\\$version](#) on page 1071

## **\$date**

```
$date date $end
```

## **Description**

The `$date` command is used to specify the date of the VCD file created. Spectre accepts this command card, but does not process it.

## **Example**

```
$date May 7, 2001 $end
```

## **\$enddefinitions**

```
$enddefinitions $end
```

### **Description**

The `$enddefinitions` command indicates where the definition section of the VCD file ends. This command card tells Spectre to treat the rest of the VCD file as the data section. If this command card is missing, Spectre parses the data section incorrectly and issues an error message.

### **Example**

```
$enddefinitions $end
```

## \$scope

```
$scope [scope_type] [scope_name] $end
```

### Description

The `$scope` command card switches from the current circuit level to a lower circuit level in the design hierarchy.

### Example

```
$scope module module1 $end
```

It is important to note:

- Spectre ignores `scope_type`, but the command must still be specified to maintain consistency with standard VCD format.
- A matching `$upscope` card must be specified in the VCD file definition section to switch the scope back to the current scope.

## \$timescale

```
$timescale [number] [time_unit_prefix] $end
```

### Description

The `$timescale` command is used to specify the time scale. This time scale applies to all time values in the VCD file, and to its signal information file. The default time is 1 ns.

### Arguments

*number*

A positive double number

*time\_unit\_prefix*

The unit prefix. The following unit prefix symbols can be applied to any numerical quantities:

- $a = A = 1.0\text{e-}18$
- $F = f = 1.0\text{e-}15$
- $G = g = 1.0\text{e}9$
- $K = k = 1.0\text{e}3$
- $M = m = 1.0\text{e-}3$
- $N = n = 1.0\text{e-}9$
- $P = p = 1.0\text{e-}12$
- $T = t = 1.0\text{e}12$
- $U = u = 1.0\text{e-}6$
- $X = x = \text{MEG} = \text{meg} = 1.0\text{e}6$
- $Y = y = 1.0\text{e-}24$
- $Z = z = 1.0\text{e-}21$

### Example

```
$timescale 1 ns $end
```

or

```
$timescale 1ns $end
```

produces the same result, telling Spectre to set the time scale to 1 ns.

## \$upscope

```
$upscope $end
```

### Description

The `$upscope` command card switches from the current circuit level to an upper circuit level in the design hierarchy.

### Example

```
$upscope $end
```

**Note:** This card must be used after the `$scope` card to switch the scope back to the top scope.



## \$var

```
$var [var_type] [size] [identifier] [reference] $end
```

or

```
$var [var_type] [size] [identifier] [reference] [index_range] $end
```

## Description

The `$var` command defines the bus to be dumped into the data section.

## Arguments

|                    |                                                                                                                                                                                                                             |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>var_type</i>    | The bus type (Spectre ignores this information)                                                                                                                                                                             |
| <i>size</i>        | Number of bits in this bus specified as a decimal number                                                                                                                                                                    |
| <i>identifier</i>  | The identifier used in the data section; it can be a or a combination of printable ASCII characters                                                                                                                         |
| <i>reference</i>   | The name of the bus                                                                                                                                                                                                         |
| <i>index_range</i> | The index range of the bus in the following formats: <ul style="list-style-type: none"><li>■ [MSI:LSI]</li><li>■ [LSI:MSI]</li><li>■ [index] if the size is 1</li></ul> <b>Note:</b> MSI, LSI, and index must be an integer |

**Note:** If the size is larger than 1, and the *index\_range* is not specified, Spectre assigns an *index\_range* of [size-1:0].

The name of the bit is a combination of the reference and the index.

## Examples

In the following example

```
$var reg 4 % regA [0:3] $end
```

the names of the four bits in bus `regA` are `regA[0]`, `regA[1]`, `regA[2]`, and `regA[3]`. The netlist file referencing these VCD sources must match these names.

In the next example

```
$var reg 1 & b [0] $end
```

the name of the bit is `b[0]`. The card defined a bit, not a bus, as a size of 1.

In the next example

```
$var reg 1 & c $end
```

the name of the bit is `c`.

In the next example

```
$var reg 4 % regA $end
```

the names of the four bits in bus `regA` are `regA[3]`, `regA[2]`, `regA[1]`, and `regA[0]`. The netlist file referencing these VCD sources must match the names.

## **\$version**

```
$version version $end
```

## **Description**

The `$version` command is used to specify the version of the VCD file created. Spectre accepts this command card, but does not process it.

## **Example**

```
$version spectre B2001.2.10 $end
```

## Data Commands

In the VCD data section, a time point that starts with a number (#) sign (for example, #100) indicates the beginning of a new card. This card continues until it reads the line before the next card (cards can have multiple lines). It can also contain data values and a command block. A command block begins with one of the following command keywords, `$comment` or `$time_value`, and ends with `$end`.

### data

#### Description

Data is divided into two types that each have their own format:

- Bus data
- Bit data

The bus data is for buses defined by `$var`, with a size greater than one. The bit data applies to the bus defined by `$var`, with a size equal to one. The bus data format is *Bvalue bus\_identifier* whereas the bit data format is *value bus\_identifier*.

#### Examples

In the following example

```
b0101 %
```

the bus with identifier `%` (defined by `$var`) has a binary value of 0101.

In the next example

```
1&
```

the one bit bus with identifier `&` (defined by `$var`) has a binary value of 1.

The valid characters for specifying the value are: 0, 1, x, X, z, and Z. Of these characters, x and X are treated as 0 for the input signal, and do not need a vector check for the output signal. The z and Z characters are treated as floating to high-impedance for the input signal, and do not need a vector check for the output signal.

### time\_value

```
#time_value
```

## Description

Each time value (point) is the beginning of a card in the data section.

## Example

#100

Time value is equal to 100 time units (time unit is defined by \$timescale).

## Signal Information File

**Note:** The information in this section is applicable to both VCD and EVCD formats.

The signal directions are specified in the signal information file. To input signals, Spectre applies stimuli to the simulation. The values of the output signals are used to perform a vector check against the simulation results, and vector errors are generated if mismatches occur. The enable signals are required to control the bi-directional signal behavior as input or output signals. All other signals in the VCD or EVCD file, not specified in the signal information file, are ignored by the simulator (warning messages are issued for these signals, based on the scopes specified in the signal information file).

The time scale of the time related cards in the signal information file are controlled by the `$timescale` card in the VCD file. For example, if `$timescale` is set to 1 ns and `.tdelay` to 2, a delay of (2 \* 1ns) occurs.

The signal name in the signal information file can be specified by using the bus name or a wildcard. The signal name specified in the VCD file is in bus/bit format. [Table E-1](#) on page 1074 provides examples.

**Table E-1 Signal Name in VCD File Corresponds to Signal Information File**

| VCD File         | Signal Information File |
|------------------|-------------------------|
| P[0] ... P[15]   | P[0:15]                 |
| P[0] ... P[15]   | P[*]                    |
| Q[63:32] Q[31:0] | Q[63:0]                 |

The example in [Table E-2](#) on page 1074 shows an incorrect naming format.

**Table E-2 Incorrect Naming Format in Signal Information File**

| VCD File | Signal Information File |
|----------|-------------------------|
| A[0:15]  | A[0:7] A[8:15]          |

**Note:** By default, Spectre creates flat mapping between the VCD and analog netlist files (the `.hier` statement can be used to switch to hierarchical name mapping to precisely match signals).

## **Signal Information File Format**

### **Comment Line**

A comment line begins with asterisk (\*) or dollar (\$) signs.

### **Continuous Line**

A continuous line is indicated by a plus (+) sign.

The maximum length of a line is 1024 characters. If a card is longer than 1024 characters, you need to use the continuous line for the card.

To process VCD and EVCD formats, the following signal characteristics need to be defined in the signal information file:

- Signal Matches on page 1076
- Signal Timing on page 1088
- Voltage Threshold on page 1094
- Driving Ability on page 1099

## **Signal Matches**

In this section, the following statements define the signal matches between the VCD and analog netlist files, signal directions, and output vector check.

- [.alias](#) on page 1077
- [.scope](#) on page 1079
- [.in](#) on page 1080
- [.out](#) on page 1081
- [.bi](#) on page 1082
- [.chk\\_ignore](#) on page 1084
- [.chkwindow](#) on page 1085



**.alias**

`.alias target_busname alias_name`

**Description**

The `.alias` statement is used to modify the name of the signal bus in the VCD/EVCD file to match the signal name in the netlist file.

By default, Spectre maps the bus delimiter from "`*[*]`" in VCD file to "`*<*>`" in the analog netlist. For example, the default setting is as follows:

`.alias *[*] *<*>`

You can use the following alias statement to alias the VCD signal `top.hier1.hier2.*[*]` to SPICE top level `*<*>`:

`.alias top.hier1.hier2.*[*] *<*>`

**Note:** For more information on using the `.alias` statement in hierarchical signal name mapping, refer to [“Hierarchical Signal Name Mapping”](#) on page 1100.

**Examples**

The following example

`.alias *[*] *[*]`

tells Spectre to keep square brackets as the bus limiter in an analog netlist. This `.alias` statement is required because `*[*]` is mapped to `*<*>` by default (see [Table E-3](#) on page 1077).

**Table E-3 .alias \*[\*] [\*] Names**

| Bus Name              | Signal Name                                 |
|-----------------------|---------------------------------------------|
| <code>a[0:3]</code>   | <code>a[0], a[1], a[2], a[3]</code>         |
| <code>vec[3:0]</code> | <code>vec[3], vec[2], vec[1], vec[0]</code> |

In the next example

`.alias sig_*[*] vec_*<*>`

tells the simulator to change the square brackets to angular brackets (see [Table E-4](#) on page 1078).

**Table E-4 .alias sig\_\*[\*] vec\_\*<\*> Names**

| Bus Name      | Signal Name                                        |
|---------------|----------------------------------------------------|
| sig_1[0:3]    | vec_1<0>, vec_1<1>, vec_1<2>, vec_1<3>             |
| sig_bus1[3:0] | vec_bus1<3>, vec_bus1<2>, ve_bus1c<1>, vec_bus1<0> |

In the next example

```
.alias sig_* vec_*
```

tells the simulator to change the prefix of the signal names from `sig_` to `vec_` (see [Table E-5](#) on page 1078).

**Table E-5 .alias sig\_\* vec\_\* Names**

| Bus Name | Signal Name |
|----------|-------------|
| sig_1    | vec_1       |
| sig_2    | vec_2       |

## **.scope**

```
.scope scope_name1 [scope_name2 ... scope_nameN]
```

### **Description**

The `.scope` statement specifies the target scope located in the definition section of the VCD file. Only the signals defined in the specified scope are processed. Multiple `.scope` statements in a signal information file are supported.

### **Arguments**

*scope\_name*      The name of the scope specified in the VCD file by the `$scope` card.

**Note:** Each scope name causes Spectre to process the signals located in the specified scope, but not the signals located in its parent or child scopes.

### **Example**

```
.scope module1 module2
```

tells Spectre to process the signal located in scope `module1` and `module2`.

## **.in**

```
.in signal_name1 signal_name2 ... signal_nameN
```

### **Description**

The `.in` statement defines the specified bus as the input bus.

### **Arguments**

*name*        The name of the bus specified in the VCD file

### **Example**

VCD file:

```
$var reg 4 % b [0:3] $end
$var reg 1 * a $end
$var reg 1 & c [4] $end
$var reg 4 % d [0:3] $end
```

Signal information file:

```
.in b[0:3] a c[4] d[*]
```

Defines `b[0:3]`, `a`, `c[4]`, and `d[0:3]` as the input signals.

## **.out**

```
.out signal_name1 signal_name2 ... signal_nameN
```

### **Description**

The `.out` statement defines the specified bus as the output bus.

### **Arguments**

*name*        The name of the bus specified in the VCD file

### **Example**

In the VCD File:

```
$var reg 4 % b [0:3] $end
$var reg 1 * a $end
$var reg 1 & c [4] $end
$var reg 4 % d [0:3] $end
```

In the signal information file

```
.out b[0:3] a c[4] d[*]
```

Defines `b[0:3]`, `a`, `c[4]`, and `d[0:3]` as the output signal.

## .bi

```
.bi 'enable_signal_expr' signal_name1 signal_name2 ... signal_nameN
```

### Description

The `.bi` statement defines the specified bus as the bidirectional bus.

The enable signal can be from a VCD/EVCD or an analog netlist file. When an enable signal is from an analog netlist file, it can also be defined as an output signal for a vector check or only used as an enable signal. If a VCD signal is used as an enable signal, it must be declared an input using the `.in` statement and located in the VCD file. Different from enable statements in the vector file, the logic voltage threshold of an analog enable signal is defined by the `.voh` and `.vol` statements.

**Note:** The enable signal cannot be defined as a bidirectional signal.

The `.alias` statement can be used to perform name mapping for the enable signal. In hierarchical signal name mapping (`.hier 1`), a hierarchical structure for the analog netlist file is supported for the enable signal. A period (.) can be used as the hierarchical delimiter to specify the hierarchical signal, and the hierarchical delimiter can be mapped to other delimiters by the `.alias` statement.

Bit-wise logic operators are supported in an enable signal expression: `&` (AND), `|` (OR), `^` (XOR), and `~` (NOT). Additional operators can be created using a combination of the supported operators. The order of processing for the logic operators is NOT > AND > OR, XOR (OR and XOR are processed at the same time). You can use parentheses ( ) around the operators to change the processing order.

### Arguments

|                                   |                                                                                                                   |
|-----------------------------------|-------------------------------------------------------------------------------------------------------------------|
| <code>'enable_signal_expr'</code> | The expression for the enable signals. The bidirectional bus switches to output mode only when its value is high. |
|-----------------------------------|-------------------------------------------------------------------------------------------------------------------|

**Note:** You need to use single quotation marks `' '` for enable signal expressions.

|                          |                                                     |
|--------------------------|-----------------------------------------------------|
| <code>signal_name</code> | The name of the bus specified in the VCD/EVCD file. |
|--------------------------|-----------------------------------------------------|

### Examples

The following example

VCD file:

```
$var reg 4 % b [0:3] $end
$var reg 1 & en $end
```

Signal information file:

```
.bi en b[0:3]
```

defines `b[0:3]` as the bidirectional signal, which is controlled by the `en` signal. When `en` is high, `b[0:3]` becomes the output signal.

In the next example

VCD file:

```
$var reg 4 * myBi [0:3] $end
$var reg 1 # en $end
```

Signal information file:

```
bi ~en myBi[0:3]
```

defines `myBi[0:3]` as the bidirectional signal, which is controlled by the `en` signal. The enable signal is appended with a tilde (~) sign, so unlike the first example, the `en` is now high, `myBi[0:3]` becomes the input signal, and vice versa.

In the next example

VCD file:

```
$var reg 4 * myBi_1 [0:3] $end
$var reg 1 # en $end
```

Signal information file:

```
.hier 1
.bi 'en & (ana_en1 ^ X1.ana_en2)' myBi_1[0:3]
.voh 1.5 ana_en* X1.ana_en*
.vol 0.8 ana_en* X1.ana_en*
```

defines `myBi_1[0:3]` as the bidirectional signal, which is controlled by the expression `'en & (ana_en1 ^ X1.ana_en2)'`. When the value of the expression is high, `myBi_1[0:3]` becomes the input signal, and vice versa. The `.voh` and `.vol` statements define the logic voltage threshold of the two analog enable signals.

## .chk\_ignore

```
.chk_ignore start_time end_time [signal_name1 ... signal_nameN]
```

### Description

The `.chk_ignore` statement specifies a window used to ignore output vector checks for a VCD file. You can provide the signal names in order to apply this statement locally. In addition to hierarchical mapping, the hierarchical structure is also given in the signal names. The `start_time` and `end_time` arguments must be specified. To define multiple time windows for ignoring output vector checks, use multiple `chk_ignore` statements.

### Arguments

|                         |                                                                                                                                                                                                                                         |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>start_time</code> | Defines the start time for the window used to ignore the output vector checks (use the <a href="#">\$timescale</a> card in the VCD file to set the time scale).                                                                         |
| <code>end_time</code>   | Defines the end time for the window used to ignore the output vector checks. You can use <code>end_time=-1</code> to ignore the entire transient time (use the <a href="#">\$timescale</a> card in the VCD file to set the time scale). |

### Example

VCD file:

```
$timescale 1ns $end
```

Signal information file:

```
.hier 1
.chk_ignore 0 100 X1.out1 Top.digital.pout[*]
.chk_ignore 300 500 X1.out1 Top.digital.pout[*]
.chk_ignore 0 -1 out[*]
```

tells Spectre to ignore the output vector check for signals `X1.out1` and `Top.digital.pout[*]` in the time windows 0 ns to 100 ns and 300 ns to 500 ns, and to ignore the entire transient time for the signal `out[*]`.



## .chkwindow

```
.chkwindow start_time end_time steady [period=const [first=const]] [signal_name1
... signal_nameN]
```

### Description

The `.chkwindow` statement specifies a window for output vector checking. Spectre only checks the signal states within this window. The signal states outside the window are ignored. The checks occur at every time point specified in the VCD/EVCD file or as defined by the `period` and `first` arguments.

Setting the `period` argument activates periodic window checking. If `period` is not defined, the `first` argument is ignored by the simulator.

**Note:** To activate periodic window checking, you need to include the "period=" and "first=" keywords.

### Arguments

|                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>start_time</code>     | Defines the window start time at which the window starts at time <code>vec_time-start_time</code> . If the <code>period</code> argument is defined, <code>vec_time</code> is the first time point defined by the <code>first</code> argument, and the vector checks are repeated according to the value of <code>period</code> . If the <code>period</code> argument is not defined, <code>vec_time</code> is the time point defined in the VCD/EVCD file. |
| <code>end_time</code>       | Defines the window end time at which the window ends at time <code>vec_time+end_time</code> .                                                                                                                                                                                                                                                                                                                                                              |
| <code>steady = 0   1</code> | If set to 0, then the vector check passes as long as the signal has reached the desired state once. If set to 1, then the signal remains in the desired state for the entire window period to pass the vector check.                                                                                                                                                                                                                                       |
| <code>period</code>         | Activates periodic window checking and defines its time period.                                                                                                                                                                                                                                                                                                                                                                                            |
| <code>first</code>          | Defines the first check point for periodic window checking (only valid when the <code>period</code> argument is also defined).                                                                                                                                                                                                                                                                                                                             |

### Examples

In the following example

VCD file:

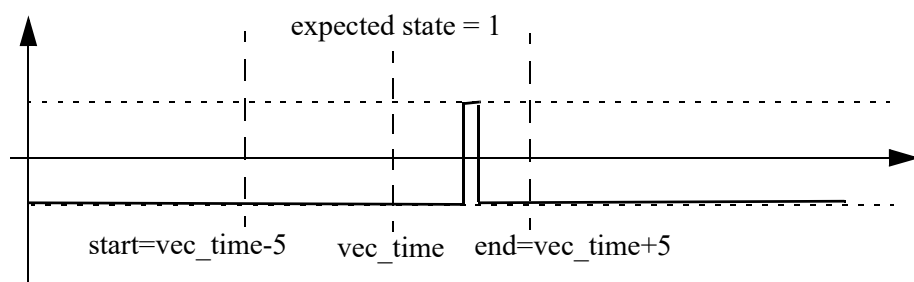
```
$timescale 1ns $end
```

Signal information file:

```
.chkwindow 5 5 0
```

The `.chkwindow` statement is set to 0, so the waveform passes the vector check (see [Figure E-1](#) on page 1086).

**Figure E-1 Vector Check with `.chkwindow` Set to 0**



In the next example

VCD file:

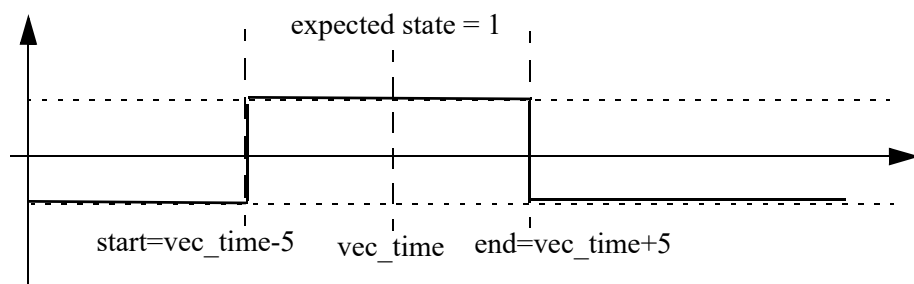
```
$timescale 1ns $end
```

Signal information file:

```
.chkwindow 5 5 1
```

The `.chkwindow` statement is set to 1 and the signal remains at that state for the entire window period, in order to pass the vector check (see [Figure E-2](#) on page 1086). If the signal matches [Figure E-1](#) on page 1086, the vector check fails.

**Figure E-2 Vector Check with `.chkwindow` Set to 1**



In the next example

VCD file:

```
$timescale 100ps $end
```

Signal information file:

```
.chkwindow 5 5 1 period=100 first=20 p[*] out_*
```

tells the simulator to activate periodic window checking for signals `p[*]` and `out_*`. The vector check points start at 2 ns and repeats every 10 ns.

In the next example

```
.hier 1
```

```
.chkwindow 5 5 1 first=20 X1.Xana.p[*] X1.Xdigital.Xcore.out_*
```

tells the simulator to ignore the `first` argument because a valid `period` argument has not been specified. The other arguments are used in the simulation.

## **Signal Timing**

The signal timing characteristics (delay, rise and fall time) are defined in this section.

- [.idelay](#) on page 1089
- [.odelay](#) on page 1090
- [.tdelay](#) on page 1091
- [.tfall](#) on page 1092
- [.trise](#) on page 1093

**Note:** Spectre checks whether the values of the `.trise` and `.tfall` statements are reasonable (warning message is issued when the defined value is too small or large).

## **.idelay**

```
.idelay time_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.idelay` statement specifies the delay time for the corresponding input signals. If a bidirectional signal is specified, this only applies to the input stage of the bidirectional signal. The default value is 0.0, if `.idelay` and `.tdelay` are not set.

### **Example**

In the following example

VCD file:

```
$timescale 1ns $end
```

Signal information file:

```
.idelay 5
```

All input signals have a time delay of 5 ns.

In the next example

VCD file:

```
$timescale 100 ps $end
```

Signal information file:

```
.hier 1
.scope Xtop.XI1
.in a[0:3] b
.tdelay 0.1 Xtop.XI1.a* Xtop.XI1.b
```

The `Xtop.XI1.a[0:3]` and `Xtop.XI1.b` input signals have a delay time of 10 ps.

## **.odelay**

```
.odelay time_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.odelay` statement specifies the delay time for the corresponding output signals. If a bidirectional signal is specified, this only applies to the output stage of the bidirectional signal. The default value is 0.0, if `.odelay` and `.tdelay` are not set.

### **Example**

VCD file:

```
$timescale 1ns $end
```

Signal information file:

```
.odelay 5
```

All output signals have a time delay of 5 ns.

## **.tdelay**

```
.tdelay time_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.tdelay` statement specifies the delay time for the corresponding input, output, and bidirectional signals. The default value is 0.0, if `.tdelay`, `.idelay`, and `.odelay` are not specified.

### **Example**

VCD file:

```
$timescale 1ns $end
```

Signal information file:

```
.tdelay 5
```

All signals have a time delay of 5 ns.

## **.tfall**

```
.tfall time_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.tfall` statement specifies the fall time of the input signal. If `.tfall` is not specified, the default value is 0.1 n.

**Note:** The range of voltage level change for *time\_value* is 0-100%.

### **Examples**

In the following example

VCD file:

```
$timescale 1 ns $end
```

Signal information file:

```
.tfall 0.1
```

all input signals have a fall time of 0.1 ns.

In the next example

VCD file:

```
$timescale 1 ns $end
```

Signal information file:

```
.in a[0:3] b
.tfall 0.1 a[0:3] b
```

input signals `a[0:3]` and `b` have a fall time of 0.1 ns.



## **.trise**

```
.trise time_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.trise` statement specifies the rise time of the input signal. If `.trise` is not specified, the default value is 0.1 n.

**Note:** The range of voltage level change for `time_value` is 0-100%.

### **Examples**

In the following example

VCD file:

```
$timescale 1 ns $end
```

Signal information file:

```
.trise 0.1
```

all input signals have a rise time of 0.1 ns.

In the next example

VCD file:

```
$timescale 1 ns $end
```

Signal information file:

```
.in a[0:3] b
.trise 0.1 a[0:3] b
```

input signals `a[0:3]` and `b` have a rise time of 0.1 ns.

## **Voltage Threshold**

As digital vector format, the voltage threshold for logic low and high can be specified using the following statements to convert the input vectors to stimuli or to perform an output vector check.

- [.vih](#) on page 1095
- [.vil](#) on page 1096
- [.voh](#) on page 1097
- [.vol](#) on page 1098

## **.vih**

```
.vih voltage_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.vih` statement specifies the logic high voltage of the input signal. If `.vih` is not specified, the default voltage is 3.3.

You can also use a parameter name to specify the voltage. For example:

```
.vih pwr_vdd
```

The `.vih` statement also supports global and local specifications as well as expressions, as shown below.

```
.vih pwr_vdd
.vih pwr_vdd_cpu_sram r*cpu_sram[*]
.vih pwr_vdd *.08
```

### **Examples**

In the following example

```
.vih 5.0
```

tells Spectre all input signals have a logic high voltage of 5.0.

In the next example

```
.in a[0:3] b
.vih 5.0 a[*] b
```

tells the simulator input signals `a[0:3]` and `b` have a logic high voltage of 5.0.

## **.vil**

```
.vil voltage_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.vil` statement specifies the logic low voltage of the input signal. If `.vil` is not specified, the default voltage is 0.0.

Like `.vih`, `.vil` also support parameters, global and local specifications, and expressions.

### **Examples**

In the following example

```
.vil 1.0
```

tells Spectre all input signals have a logic low voltage of 1.0.

In the next example

```
.in a[0:3] b
.vil 1.0 a[0:3] b
```

tells the simulator input signals `a[0:3]` and `b` have a logic low voltage of 1.0.

## **.voh**

```
.voh voltage_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.voh` statement specifies the logic high voltage of signals defined as outputs and signals from the analog netlist file that are used in the signal information file. If `.voh` is not specified, the default voltage is 3.3.

Like `.vih`, `.voh` also support parameters, global and local specifications, and expressions.

### **Examples**

In the following example

```
.voh 5.0
```

tells Spectre that all output signals have a logic high voltage of 5.0.

In the next example

```
.out out[0:3] outA
.voh 5.0 out[*] outA
```

tells the simulator output signals `out[0:3]` and `outA` have a logic high voltage of 5.0.

## **.vol**

```
.vol voltage_value [signal_name1 ... signal_nameN]
```

### **Description**

The `.vol` statement specifies the logic low voltage of signals defined as outputs and signals from the analog netlist file that are used in the signal information file. If `.vol` is not specified, the default voltage is 0.0.

Like `.vih`, `.vol` also support parameters, global and local specifications, and expressions.

### **Examples**

In the following example

```
.vol 1.0
```

tells Spectre that all output signals have a logic low voltage of 1.0.

In the next example

```
.out out[0:3] outA
.vol 1.0 out[0:3] outA
```

tells the simulator output signals `out[*]` and `outA` have a logic low voltage of 1.0.

## **Driving Ability**

For input stimuli, the output resistance of VCD/EVCD sources can affect Spectre results. To specify the driving ability of VCD/EVCD sources, use the following statements:

### **.outz**

```
.outz resistance [signal_name1 ... signal_nameN]
```

### **Description**

The `.outz` statement specifies the output resistance for corresponding input signals. If `.outz` is not specified, the default value is 0.01.

### **Example**

```
.outz 1meg
```

All input signals have an output resistance of 1 Megaohm.

### **.triz**

```
.triz resistance [signal_name1 ... signal_nameN]
```

### **Description**

The `.triz` statement specifies the output impedance when the corresponding input signals are in tri-state. If `.triz` is not specified, the default value is 1,000 Meg.

### **Example**

```
.triz 500meg
```

All input signals have an output impedance of 500 Megaohms.

## **Hierarchical Signal Name Mapping**

Hierarchical signal name mapping can be used to precisely match signals between the VCD and analog netlist files, and is defined by Spectre `hier` statement:

```
.hier 0 | 1
```

### **Description**

The `.hier` statement is used to specify hierarchical names in both the VCD and analog netlist files.

### **Arguments**

|                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>hier</code> | <p>If <code>hier=0</code>, Spectre creates flat mapping between the VCD and analog netlist files (default). To maintain backward compatibility, the hierarchical delimiter is regarded as part of the signal name.</p> <p>If <code>hier=1</code>, the simulator applies the hierarchical names to the VCD and analog netlist files. The VCD file stimuli are no longer limited to the top level of the analog netlist file. In the VCD info file, the complete hierarchical structure needs to be added to the <code>.scope</code> statement (the hierarchical signals in the analog netlist file are mapped according to the information provided by the <code>.alias</code> statement).</p> |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

The key differences between flat and hierarchical mapping include:

- To match hierarchical signals in the VCD file, the complete hierarchical structure needs to be specified in the `.scope`, `.alias`, and `.chkwindow` statements, as well as in the signal characteristic statements. For flat mapping, only the signal names are needed.
- For hierarchical signal name mapping, the statements to define the port direction of the signal are related to the `.scope` statement, which includes the `.in`, `.out`, and `.bi` statements. When using flat mapping, the multiple scopes defined by the `.scope` statement are regarded as set. Spectre searches all of the scopes to perform a signal match and outputs an error message when the same signal name is defined in more than one VCD scope.
- The hierarchical structure of the analog netlist file is specified by the `.alias` statement when performing hierarchical mapping.



## Enhanced Statements

### *.scope and .in/.out/.bi*

When using Spectre to apply hierarchical names to the VCD/EVCD and analog netlist files (`.hier 1`), the hierarchical structure in the VCD/EVCD file must be clearly defined with the `.scope` statement. The `.in`, `.out`, and `.bi` statements are used to define the signal name in the specified `.scope` statement and cannot contain the hierarchical structure. For the `.bi` statement, the enable signal needs to contain the hierarchical path because the signal may belong to a different scope.

The VCD/EVCD signal info file supports multiple `.scope` statements. The effective scope of each `.scope` statement is affected by the other statements, requiring the `.in`, `.out`, and `.bi` statements to be in the correct location.

## Examples

In the VCD file:

```
$scope module top $end
$scope module digital $end
$var reg 1 ! din_1 $end
$var reg 1 " en $end
$scope module drv $end
$var reg 1 ! mid[1] $end
$var reg 1 " inout $end
$upscope $end
$upscope $end
$upscope $end
```

In the VCD info file:

```
.hier 1
.scope top.digital
* The effective scope is top.digital
.in din_1 en
* The scope top.digital is ended by the next .scope statement
.scope top.digital.drv
* The effective scope is changed to top.digital.drv
.out mid[*]
.bi top.digital.en inout
```

## **.alias**

```
.alias targ_signame alias_signame
```

The hierarchical structures that are defined in the `.scope` statement are used only for the VCD/EVCD file, so the `.alias` statement is needed to map the signals to the lower circuit levels of the analog netlist file.

**Note:** If multiple `.alias` statements define the mapping relationship for a signal, the last `.alias` statement is used by the simulator, and the other statements are overwritten.

## **Arguments**

|                            |                                                                                                                                                                                                                                             |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>targ_signame</code>  | Specifies the hierarchical signal names (VCD/EVCD format) that are already defined in the <code>.scope</code> statement and <code>.in/.out/.bi</code> statements. The hierarchical delimiter is represented by a period ( <code>.</code> ). |
| <code>alias_signame</code> | Specifies the hierarchical signal names of the analog netlist file. The <code>hier_delimiter</code> option defines the hierarchical delimiter.                                                                                              |

## **Examples**

In the following example

```
.alias TOP.module1.in1 X1.in1
.scope Top.module1
.in in1
```

tells Spectre to map the `TOP.module1.in1` defined in the `.scope` and `.in/.out/.bi` statements to the signal `in1` of instance `X1` in the analog netlist file.

In the next example

```
.alias [*] *<*>
.alias Top.module1.sig_*[*] X1.vec_*<*>
.scope Top.module1
.out sig_[0:15]
.scope digital_block
.in datain[*]
```

tells the simulator for the `Top.module1.sig_[0:15]` signals, the second `.alias` statement overwrites the first `.alias` statement and maps the signals to `X1.vec_<0>`, ... `X1.vec_<15>`. Since only the first `.alias` statement matches the `digital_block.datain[*]` signals, they are mapped to `digital_block.datain<*>` of the analog netlist file.

In the next example

■ Analog netlist file:

```
Opt options hier_delimiter = %
```

■ VCD/EVCD info file:

```
.alias TOP.module1.sig_[*] X1%Xdrv%vec_<*>
.scope Top.module1
.out sig_*
```

**Note:** The hierarchical delimiter for the analog netlist file is percent (%), not period (.).

## ***Hierarchical Signal Names***

For hierarchical mapping, the signal names in the `.alias` and `.chkwindow` statements, as well as in the signal characteristic statements, must have the hierarchical structure in the VCD file.

## **Examples**

```
.hier 1
.chkwindow -1 5 1 Top.X1.out*
.vih 1.2 X1.in[*]
.vol 0.2 X1.dout1 Xdig.X2.dout1
.tfall 0.2 Xana.X1.in* Xdig.din*
.outz 100 X1.in[*]
```

## Enhanced VCD Commands

Since the EVCD and VCD formats are similar, only the key EVCD format differences will be discussed in this section:

- [Signal Strength Levels](#) on page 1104
- [Value Change Data Syntax](#) on page 1104
- [Port Direction and Value Mapping](#) on page 1106

### Signal Strength Levels

Verilog HDL allows scalar net signal values to have a full range of unknown values, and different levels of strength or combinations of levels of strength. For logic operation, multiple-level logic strength modeling resolves combinations of signals into known or unknown values, allowing the behavior of hardware to be represented with improved accuracy.

EVCD signal strength can be defined by eight values, ranging from 0 (weakest) to 7 (strongest). The most commonly used values are 0 and 6. For example, for logic value 0

```
<0_strength_component> =6 , <1_strength_component> =0
```

and for logic value 1

```
<0_strength_component> =0 , <1_strength_component> =6
```

**Note:** Logic strength levels are not defined in VCD files because only four states are supported.

Spectre ignores the strength information (minimal impact on most CMOS circuit designs). If you want to preserve driver strength during simulation, specify `.outz` in the signal information file for specific signals with different output resistances.

For more information about logic strength modeling, refer to *IEEE Std 1364-2001*.

### Value Change Data Syntax

The EVCD `data` command is different from the one used with VCD because the EVCD version can provide strength information and additional signal states.

#### **data**

```
p[port_value] [0_strength_component] [1_strength_component] [identifier_code]
```

## Description

The value change section shows the actual value changes at each simulation time increment. Only variables that change value during a time increment are listed. In the EVCD file, strength information and a larger number of value states with port direction are presented in the value change section. The arguments for the EVCD `data` command are listed below.

## Arguments

|                             |                                                                                                                                                                                                   |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>p</i>                    | Key character that indicates a port.<br><br><b>Note:</b> There is no space between <i>p</i> and <i>port_value</i> .                                                                               |
| <i>port_value</i>           | State character which contains information about driving direction and the value of the port. The state characters are described in “Port Direction and Value Mapping” on page 1106 (see tables). |
| <i>0_strength_component</i> | One of the eight Verilog strength values indicating the <code>strength0</code> component of the value (Spectre ignores this value).                                                               |
| <i>1_strength_component</i> | One of the eight Verilog strength values indicating the <code>strength1</code> component of the value (Spectre ignores this value).                                                               |
| <i>identifier_code</i>      | The identifier code for the port, which is defined in the <code>\$var</code> construct for the port.                                                                                              |

## Examples

The following example

```
pU 0 7 <0
```

tells Spectre that one bit bus with identifier `<0` (defined by `$var`) has a binary value of `U`, and the strength of 0 component is 0 and the strength of 1 component is 7.

In the next example

```
pCCC 667 667 !
```

tells the simulator the bus with identifier `!` (defined by `$var`) has a binary value of `CCC`, and the strength of 0 component is 667 and the strength of 1 component is 667. There is more than one driver on this port and the resolved value is `CCC`.

## Port Direction and Value Mapping

The port value in the EVCD file contains port direction information, which helps Spectre distinguish some of the `x` states, apply stimuli for input signals, or perform a vector check for output signals.

**Note:** To generate the EVCD file, the port directions of the circuit simulated by Spectre need to be consistent with the port directions of the device under test (DUT).

### input Direction

Given an DUT and a test fixture, the driving direction is `input` if the text fixture drivers are driving a non-tristate value and the drivers inside the DUT are tri-state. The resolved value is mapped in Table E-6.

When reading the mapping information in the following tables, it is important to note:

- Declared `in` and declared `out` indicates the signal is defined as `input` and `output` in the signal information file. The term `active` implies the drivers are in a non-tristate condition.
- Because the conflicting states of the signal value are converted to `x` in the VCD file, they are regarded as “not needed” and Spectre does not perform a vector check when the signals are specified as `output`.
- Combining the port direction for the signal value in the EVCD file and the specified direction in the signal information file, Spectre can distinguish the `input` and `output` values of a signal and perform a vector check when it is specified as `output` in the signal information file.

**Table E-6 input Value Mapping**

| Port Value | Declared<br><code>in</code> | Declared<br><code>out</code> | Declared <code>bi</code><br>Enable = 0 | Declared <code>bi</code><br>Enable = 1 | Mapped VCD Value                                                                           |
|------------|-----------------------------|------------------------------|----------------------------------------|----------------------------------------|--------------------------------------------------------------------------------------------|
| D          | 0 input                     | No check                     | 0 input                                | No check                               | Low – only one active driver to the port                                                   |
| d          | 0 input                     | No check                     | 0 input                                | No check                               | Low – two or more active drivers to the port (may be conflicts, yet resolved value is low) |
| U          | 1 input                     | No check                     | 1 input                                | No check                               | High – only one active driver to the port                                                  |

**Table E-6** input Value Mapping, *continued*

| Port Value | Declared in | Declared out | Declared bi Enable = 0 | Declared bi Enable = 1 | Mapped VCD Value                                                                             |
|------------|-------------|--------------|------------------------|------------------------|----------------------------------------------------------------------------------------------|
| u          | 1 input     | No check     | 1 input                | No check               | High – two or more active drivers to the port (may be conflicts, yet resolved value is high) |
| N          | x input     | No check     | x input                | No check               | Unknown (not needed)                                                                         |
| n          | x input     | No check     | x input                | No check               | Unknown (not needed)                                                                         |
| Z          | z input     | No check     | z input                | No check               | Tri-state                                                                                    |

### output Direction

The driving direction is `output` if the driving value from drivers inside the DUT is non-tristate, but the value driven by the drivers in the test fixture is tri-state. The resolved value is mapped in Table E-7.

**Table E-7** output Value Mapping

| Port Value | Declared in | Declared out | Declared bi Enable = 0 | Declared bi Enable = 1 | Mapped VCD Value                                                                           |
|------------|-------------|--------------|------------------------|------------------------|--------------------------------------------------------------------------------------------|
| L          | z input     | Check 0      | z input                | Check 0                | Low – only one active driver to the port                                                   |
| l          | z input     | Check 0      | z input                | Check 0                | Low – two or more active drivers to the port (may be conflicts, yet resolved value is low) |
| H          | z input     | Check 1      | z input                | Check 1                | High – only one active driver to the port                                                  |

**Table E-7** output Value Mapping, *continued*

| Port Value | Declared<br>in | Declared<br>out | Declared bi<br>Enable = 0 | Declared bi<br>Enable = 1 | Mapped VCD Value                                                                             |
|------------|----------------|-----------------|---------------------------|---------------------------|----------------------------------------------------------------------------------------------|
| h          | z input        | Check 1         | z input                   | Check 1                   | High – two or more active drivers to the port (may be conflicts, yet resolved value is high) |
| X          | z input        | No check        | z input                   | No check                  | Unknown (not needed)                                                                         |
| T          | z input        | No check        | z input                   | No check                  | Tri-state                                                                                    |

### unknown Direction

The driving direction is `unknown` if both the drivers in the test fixture and DUT are driving a non-tristate value. The resolved value is mapped in Table [E-8](#).

**Table E-8** unknown Value Mapping

| Port Value | Declared<br>in | Declared<br>out | Declared bi<br>Enable = 0 | Declared bi<br>Enable = 1 | Mapped VCD Value            |
|------------|----------------|-----------------|---------------------------|---------------------------|-----------------------------|
| 0          | 0 input        | Check 0         | 0 input                   | Check 0                   | Low (input=0 and output=0)  |
| 1          | 1 input        | Check 1         | 1 input                   | Check1                    | High (input=1 and output=1) |
| ?          | x input        | No check        | x input                   | No check                  | x (input=x and output=x)    |
| A          | 0 input        | Check 1         | 0 input                   | Check 1                   | x (input=0 and output=1)    |
| a          | 0 input        | No check        | 0 input                   | No check                  | x (input=0 and output=x)    |
| B          | 1 input        | Check 0         | 1 input                   | Check 0                   | x (input=1 and output=0)    |
| b          | 1 input        | No check        | 1 input                   | No check                  | x (input=1 and output=x)    |



**Table E-8** unknown Value Mapping, *continued*

| Port Value | Declared in | Declared out | Declared bi Enable = 0 | Declared bi Enable = 1 | Mapped VCD Value                 |
|------------|-------------|--------------|------------------------|------------------------|----------------------------------|
| C          | x input     | Check 0      | x input                | Check 0                | x (input=x and output=0)         |
| c          | x input     | Check 1      | x input                | Check 1                | x (input=x and output=1)         |
| F, f       | z input     | No check     | z input                | No check               | Tri-state (input=z and output=z) |

## Enhanced VCD Format Example

The following is an example of EVCD file format.

```

$date
Jul 11, 2004 15:42:26
$end
$version
TOOL: ncsim 05.00-p001
$end
$timescale
1 ns
$end
$scope module board $end
$scope module counter $end
$var port [3:0] ! value $end
$var port 1 clock $end
$var port 1 # fifteen $end
$var port 1 $ altFifteen $end
$upscope $end
$upscope $end
$enddefinitions $end
#0
$dumpports
pXXXX 6666 6666 !
pN 6 6 "
pX 6 6 #
pX 6 6 $
$end

```

```
#5
pU 0 6 "
#10
pLLLL 6666 0000 !
pL 6 0 #
pL 6 0 $
#50
pD 6 0 "
...
```

## Frequently Asked Questions

- [Is it necessary to modify the VCD/EVCD file to match the signals?](#) on page 1110
- [How can I verify the input stimuli?](#) on page 1110
- [How do I verify the output vector check?](#) on page 1111
- [Why should I use hierarchical signal name mapping?](#) on page 1111
- [What is the difference between CPU and user time?](#) on page 1111

### Is it necessary to modify the VCD/EVCD file to match the signals?

You can adjust the signal information file to match signals in the VCD/EVCD file with those in the netlist file, and leave the VCD/EVCD file unchanged. Spectre only needs the scopes specified in the `.scope` statement and ignores the other scopes (the simulator also ignores the parent or child scope of the specified scope). The `.alias` statement can be used to map the signal names between the VCD/EVCD and circuit netlist files.

### How can I verify the input stimuli?

As digital vector format, first probe the signals in the top-level using `.probe tran v(*) depth=1` and check the waveform outputs with the Virtuoso Visualization and Analysis or SimVision viewers.

**Note:** The signal names are case sensitive.

Review the log file to check if the signals defined in the digital vector file match those defined in the analog netlist file.

- If the signal is in the specified scope of VCD/EVCD, but not in the VCD info file, a warning message appears.

- If the signal is in the specified scope of VCD/EVCD and in the VCD info file, but not in the analog netlist file, a warning message appears.
- If the signal is in the analog netlist file, but does not match the one in VCD/EVCD, check the list of dangling nodes or no DC path to the ground.

### How do I verify the output vector check?

A `<netlistName>_<tranName>.veclog` file is generated at the location specified by Spectre `option-raw` statement if there are any vector checks. A `<netlistName>_<tranName>.vecerr` file is also generated when errors occur during the vector check. Refer to these two files for detailed information about the vector check. Here, `<netlistName>` refers to the name of the netlist and `<tranName>` refers to the name of the transient analysis.

When the signal is defined in both the VCD/EVCD files and the VCD info file, but not in the analog netlist file, the simulator issues a warning message.

### Why should I use hierarchical signal name mapping?

Flat signal name mapping works for most situations, but suffers from the following limitations:

- Only the signals in the top level can be mapped to the VCD file (analog netlist file).
- When multiple `.scope` statements are used in a digital VCD file, Spectre treats them as a single set and searches for signals (as defined in the `.in`, `.out`, and `.bi` statements) in all of the `.scope` statements. An error occurs when a signal with the same name appears in more than one `.scope` statement.

Hierarchical signal name mapping is able to overcome these limitations, allowing you to map signals to the lower levels of the analog netlist file and to use multiple `.scope` statements (see [“Enhanced Statements”](#) on page 1101 for more information about `.scope` statements).

### What is the difference between CPU and user time?

#### Description

- **CPU time** is the time the central processing unit (CPU) spends running the user program
- **User time** is the user and system times combined (that is, the total time needed to provide system service to the user program)

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When running a simulation, Spectre stores the elapsed CPU and user time information in the STDOUT (standard output) or log file. The estimated completion time is based on linear interpolation of the user time from the start of the simulation. To view such information in STDOUT, set `annotated=estimated` in the `tran` statement.

**Note:** The elapsed user time can be less than the elapsed CPU time.

### Example

```
tran: time = 3.303 us (82.6 %), step = 9.036 ps (226 u%)
cpu = 957402.0 s, elapsed = 190995.8 s, steps = 144244, mem = 45959.8 MB
estimated completion time: 10:12:07
```