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Virtuoso Layout Suite EXL Reference

Product Version IC23.1
November 2023

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Contents

Introduction to Virtuoso Layout Suite EXL

Virtuoso® Layout Suite EXL (Layout EXL) is the most advanced editing environment in the Virtuoso Layout Suite, providing access to the first electrically- and simulation-driven layout design environment available in the electronic chip design industry.

The Layout EXL cockpit offers full access to all the Layout XL functionality in addition to providing access to all the functionality that was accessible under Layout EAD in previous releases. The Layout EXL cockpit is also the default cockpit for all advanced nodes features supported in the ICADVM20.1 release, such as concurrent layout team design, design planning, and interactive simulation driven routing.

Layout EXL is also the required base platform for all 5nm designs, the Virtuoso RF solution, the Virtuoso Photonics Solution, and for a new set of in-design technologies to facilitate advanced design planning and congestion analysis. Some of these capabilities have feature-specific license requirements in addition to the base Layout EXL license.

Layout EXL is required to edit any design that uses 5nm process technology or which includes specific design data generated by any of the technologies mentioned above. Designs containing such data must be edited only in Layout EXL to maintain compliance and to ensure that the design remains correct by construction at all times.

Consequently, when you open such designs from the Library Manager, CIW, or schematic or layout window menus, the design opens in Layout EXL automatically. The same applies to any design that was previously saved using Layout EXL.

Related Topics

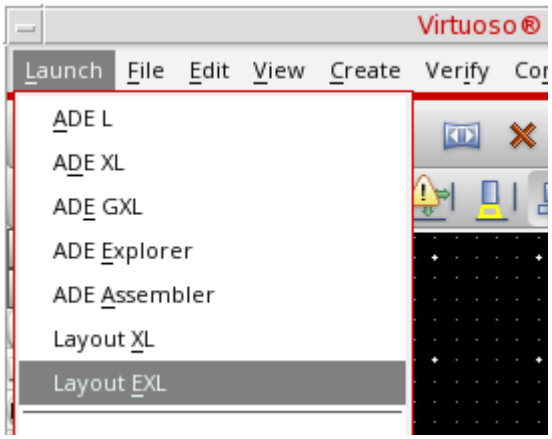
Launching Virtuoso Layout Suite EXL

Virtuoso Layout Suite EXL Features and Flows

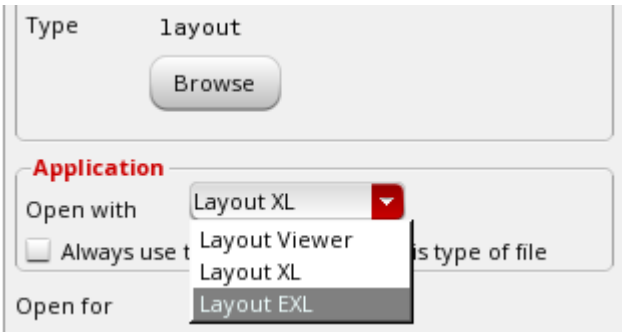
Launching Virtuoso Layout Suite EXL

To manually launch Layout EXL, do one of the following:

- From a Schematics XL or Layout XL window, choose *Launch – Layout EXL*.



- Use the Open File form from a Schematics XL or Layout XL window and choose *Layout EXL* from the *Open with* drop-down list.



Opening a design in Layout EXL automatically checks out a `Virtuoso_Layout_Suite_EXL` license, which remains checked out until either:

- All the layout windows in the Virtuoso session are closed. (The license remains checked out regardless of whether any of the open layout windows are using EXL features or not.)
- The Virtuoso session itself is ended.

You cannot open a design containing Layout EXL data in Layout XL. You can, however, view a Layout EXL design using the Layout Viewer application.

Related Topics

Virtuoso Layout Suite EXL Features and Flows

Virtuoso Layout Suite EXL Features and Flows

The features and flows available in Layout EXL are summarized below, along with instructions on how to enable each feature in the Layout EXL window and a link to more detailed information.

- **Electrically Aware Design**

  The electrically aware design (EAD) flow lets you capture the current data from design simulations, extract and visualize RC parasitics as you edit the layout, perform EM checks, and fix violations. You can further extract parasitics from a partial or complete layout and rerun simulations to check if the output specifications are met.

  You can access the electrically aware design functionality both from the *EAD* menu (which is automatically installed when you launch Layout EXL) and in the *EAD* workspace, available from the drop-down list in the toolbar.

- **Simulation Driven Routing**

  The simulation driven routing (SDR) capability elevates Virtuoso from an electrically aware design environment to a simulation driven design environment. It addresses many of the electromigration and parasitic challenges of critical circuits and advanced-node designs, offering the layout designer an innovative and predictable flow to help meet current density constraints, significantly reduce sign-off times, and improve productivity and design reliability.

  You can access the simulation driven routing functionality from the *SDR Toolbar*, which is installed automatically when you launch Layout EXL.

- **Virtuoso Concurrent Layout Editing**

  Virtuoso Concurrent Layout is a layout editing environment that lets multiple designers work concurrently on different parts of the same top cellview within Virtuoso. This increases the overall productivity of the layout design team by allowing them to work on different aspects of a single design in parallel.

  To access the feature, choose the *Concurrent_Layout* workspace from the drop-down list in the toolbar.

- **Design Planning and Analysis**

  The advanced design planning and analysis feature provides hierarchical generation capabilities supported in an innovative layout-place-route solution for both advanced and mature node designs. The design planning and analysis feature supports informed planning decisions earlier in the design cycle, which are based on real-time congestion analysis data provided by the fully integrated Congestion Analysis assistant.

  To access the feature, choose the *Design_Planning* workspace from the drop-down list in the toolbar.

- **Congestion Analysis**

  The Congestion Analysis assistant facilitates the quick and accurate modeling of routing congestion to help improve floorplanning, optimize pin generation and placement, and reduce overall die size. The feature lets you extract, display, and analyze routing congestion both visually and statistically, and offers sophisticated tools facilitating the targeted optimization of routing paths for critical nets and net groups.

  To open the assistant, choose the *Congestion_Analysis* workspace from the drop-down list in the toolbar.

- **Virtuoso Automated Device Placement and Routing Flow**

  The Virtuoso automated device placement and routing flow comprises a series of tasks to generate automatically placed and routed layouts. The flow enables you to quickly generate placed and routed layouts that are constraint compliant and LVS correct, and follow DRCs as captured in the Virtuoso technology file. The layouts also incorporate base layer fill, as typically required in advanced nodes. These layouts can be used to extract parasitics for re-simulation to identify issues early on, without waiting for the final sign-off, and can be easily modified and updated to generate the final layout for sign-off.

  To access the functionality, open the *Auto P&R* assistant that is automatically available in the Layout EXL environment.

The following features have feature-licensing requirements in addition to requiring Layout EXL platform and the `Virtuoso_Layout_Suite_EXL` license as a base. Check the feature documentation for more details.

- **Virtuoso RF Solution**

  The Virtuoso RF solution allows ICs to be imported from different technologies and into a single package design, enabling package designers to assemble and simulate the package on a single platform.

To access the RF solution, set the `Virtuoso_RF_Option` shell environment variable before you launch Virtuoso. You cannot open a package layout in Layout EXL unless this environment variable is set.

■ Virtuoso Photonics Solution

The Virtuoso Photonics solution supports an Electronic-Photonic Design Environment (EPDA) framework that allows integration and implementation of electrical and optical signals using a single design framework.

If you already have access to the Virtuoso Studio design environment, you can invoke the additional Photonics capabilities supported in Virtuoso by using the `Virtuoso_Photonics Option` (VPO) license. The VPO license can be accessed by setting the shell environment variables:

```
setenv Virtuoso_Photonics_Option t
```

If you do not already have a dedicated license to access the Virtuoso Studio design environment, you can check out the `Virtuoso_Photonics_Platform` (VPP) license by setting the shell environment variable:

```
setenv Virtuoso_Photonics_Platform t
```

Related Topics

Virtuoso Layout Viewer

Virtuoso Electrically Aware Design Flow

Virtuoso Simulation Driven Interactive Routing Flow

Getting Started with Virtuoso Concurrent Layout

Virtuoso Design Planning and Analysis

Running Congestion Analysis

Virtuoso RF Solution

Virtuoso Photonics Solution