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Virtuoso RF Solution Guide

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Contents

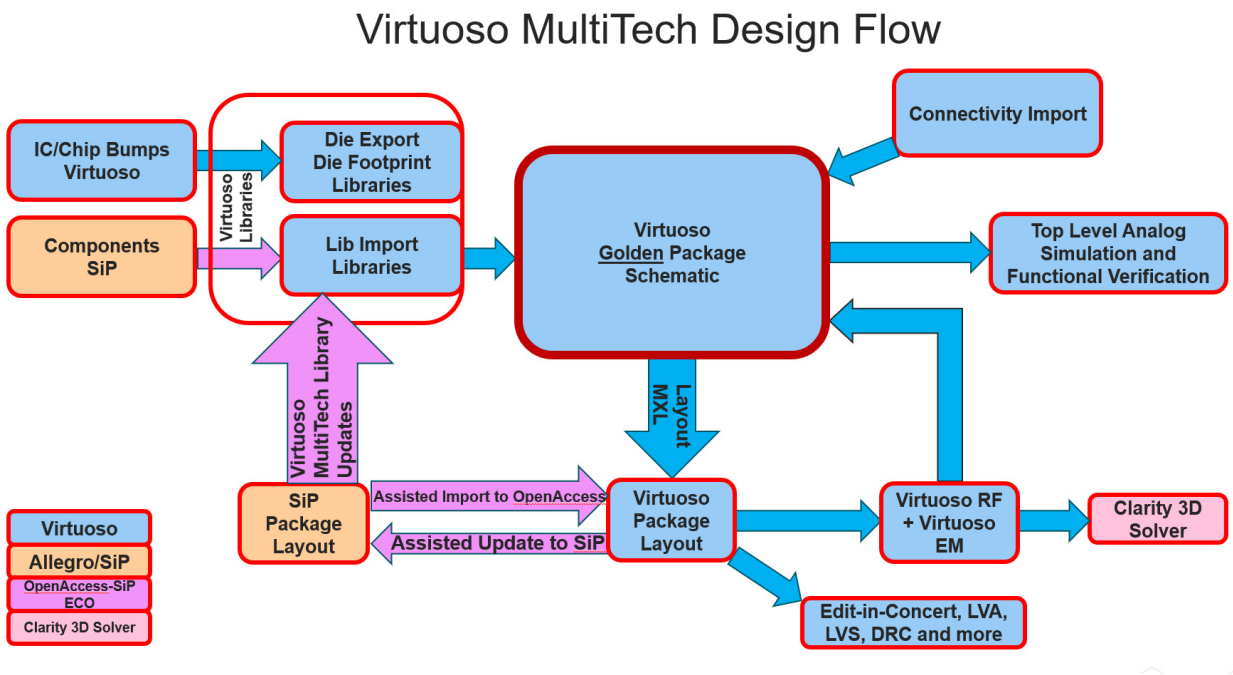
1

Introduction to Virtuoso RF Solution

The Virtuoso Multi-Technology Solution has enabled designers to create packages in Virtuoso by adding package design capabilities to the existing capabilities of Virtuoso. With the Virtuoso RF Solution, the Virtuoso Multi-Technology Solution is leveraged for RF module designers who want to edit, simulate, extract, and backannotate in Virtuoso. The rapid increase in design complexity and heterogeneous integration is driving the need to do simultaneous design in the package and die. This simultaneous, but often disjointed, development flows of the package and die increase the chance of design failure. The Virtuoso Multi-Technology Solution has been developed to allow the package and die designs to evolve simultaneously and Edit-in-Concert with one another within Virtuoso. Layout versus Schematic (LVS) integrity can be maintained during logic and placement changes in the package and die. In addition, the Virtuoso RF Solution gives package layout designers productivity-enhancing features to run a variety of EM solvers integrated into Virtuoso. Designers can fine-tune portions of the system by extracting and simulating circuit paths and context around the circuit paths.

In low frequency and less demanding environments, IC (Die) designs are relatively unaffected by the package context in which they were used. The IC (or die) in-package behavior is typically in line with standalone simulation results. Packages are now expanding from a single IC to multiple ICs with interconnects and discrete components required by the ICs to function. The PCB may contain several packages with associated interconnects and more discrete components. When the IC behavior is measured, housed inside a package and mounted on a PCB, there is a visible deviation compared to the standalone simulated characteristics of

the IC. This deviation is more pronounced at higher frequencies and/or more demanding EM environments. To identify and eliminate such errors at an early design stage and prior to tape-out, it is essential to have a familiar design and simulation environment, which auto-enables the IC or package designer to simulate the IC in context of the entire PCB, package system, and the parasitics. The methodology just described has a two-fold impact: it allows an optimization of the design of the package and PCB in the context of IC, and in certain cases might require redesigning the IC itself. The entire control lies with the IC or package designer, who is in a much better position to minimize design iterations.



The Virtuoso RF Solution in the Virtuoso environment allows ICs to be imported from different technologies and assembled in a package schematic. At times, the IC and package designer work in isolation and make changes to the schematic. The LVS checks, simulations, and EM simulations play an important role in synchronizing and consolidating the changes in the package layout. Flows in the Virtuoso RF Solution enable the package designers to assemble and simulate the package on one platform.

Related Topics

License Requirements of Virtuoso RF Solution

Schematic/Layout Views in the Virtuoso RF Solution/Virtuoso MultiTech Environment

License Requirements of Virtuoso RF Solution

The following are the licensed products needed for Virtuoso MultiTech Framework:

Virtuoso Electromagnetic Solver Assistant

Virtuoso Layout Suite MXL

EMX_Solver

Clarity 3D Solver

Virtuoso System Design Solution - RF Module Layout

Virtuoso Schematic Editor XL plus

(Option1) For SiP Layout editing with Virtuoso Layout Suite

Virtuoso Layout Suite MXL

OR

Virtuoso Layout Suite EXL + Virtuoso_MultiTech_Framework (95022)

(Option2) For SiP Layout editing with Allegro Package Designer Plus

Allegro Package Designer Plus and SiP Layout Option

Important

It is recommended to set up the PCB hierarchy path before IC and Sigrity hierarchy paths to ensure that the Virtuoso System Design, Virtuoso MultiTech Framework, Virtuoso RF Solution, and Virtuoso Electromagnetic flow works smoothly.

```
set path = ( $MMSIMHIER/tools.lnx86/bin $PCBHIER/tools/bin $ICHIER/tools/bin
$ICHIER/tools/dfII/bin $SIGRITY_EDA_DIR/tools/bin )
```

For more information on licensing, see *Virtuoso Software Licensing and Configuration Guide*.

Related Topics

Introduction to Virtuoso RF Solution

Schematic/Layout Views in the Virtuoso RF Solution/Virtuoso MultiTech Environment

Schematic/Layout Views in the Virtuoso RF Solution/ Virtuoso MultiTech Environment

The handling of the schematic and layout views in the Virtuoso RF Solution/Virtuoso MultiTech environment depends on specific policies as shown. Virtuoso MultiTech schematic or layout are created in a library that has `fabricType` = `package`, `module`, or `board`.

Virtuoso Environment	Opened Through	Virtuoso MultiTech Schematic	Virtuoso MultiTech Layout
Layout MXL	-Library Manager (Right-click the view – ***Open***) -CIW History (list of recently opened cellviews)	Opens in Schematics XL and it cannot be switched to the L tier.	Opens in Layout MXL and it cannot be switched to the EXL tier.
	-Library Manager (Right-click the view – ***Open With***) -CIW (***File*** – ***Open***)	Opens in the XL tier because Schematics XL is the only application listed.	Layout Viewer and Layout MXL are the available options and it cannot be switched to the EXL tier.
Layout MXL not available	-Library Manager (Right-click the view – ***Open***) -CIW History (list of recently opened cellviews)	Opens in Schematic XL and it cannot be switched to the L tier.	Displays an error message that the cellview cannot be opened.
	-Library Manager (Right-click the view – ***Open With***) -CIW (***File*** – ***Open***)	Opens in the XL tier because Schematics XL is the only application listed.	

Note: Virtuoso MultiTech schematic and Virtuoso RF Solution layouts cannot be opened in IC6.1.8. An error message is displayed. You can open Virtuoso System Design Platform schematics and layouts only in IC6.1.8. To open the Virtuoso System Design Platform schematics and layouts in Virtuoso Studio IC23.1, contact your Cadence Customer Support representative.

Related Topics

License Requirements of Virtuoso RF Solution

Introduction to Virtuoso RF Solution

2

Flows in Virtuoso RF Solution

There are many flows and sub-flows in the Virtuoso RF Solution, which involve various products such as, Cadence EMX® Planar 3D Solver, Clarity 3D Solver, Cadence Quantus™ Extraction Solution, and Allegro Package Designer Plus SiP Layout Option. You are recommended to follow the basic use model described below to create package layouts in Virtuoso and simulate IC in context of the package:

1. Import the technology information, libraries, and ICs before creating the schematic and layout. This task is performed by the librarian of the project, who enables the environment for creating the package schematic and layout.
2. Create a package schematic by instantiating SMD instances, die or IC instances, and transmission lines, creating attachments and connecting them to the package connectors, and simulating the schematic.
3. Create a package layout by generating a layout from source, creating bond wires, bump attachments, embedded dies, and die stacks, and creating voids using dynamic shapes. Edit-in-Concert by opening layouts from multiple fabrics simultaneously represented as various tabs in Virtuoso layout. Thereafter, perform interactive routing, EM analysis, and post-layout simulation. Additionally, create the extracted schematic using S-parameters from Clarity, EMX, and AXIEM.
4. Perform the connectivity, LVS, DRD, and DRC checks on the layout after importing from Allegro.
5. Export the package layout to the SiP layout by using the Allegro® translators. Place parts in SiP and route in the package layout and incrementally update the Virtuoso layout from SiP.

Related Topics

Virtuoso RFIC EMX Quantus Flow

Virtuoso RF Schematic-Driven Flow

Virtuoso RF Library Import Flow

Virtuoso RF ECO Flow

Virtuoso Integrity 3D-IC Flow

Virtuoso Schematic Editor Driven SiP Layout Flow

Virtuoso Stacked Silicon Solution Flow

SiP to Virtuoso Layout Assisted Import and Export Flows

Multi-Technology Enablement Flow

Virtuoso Schematic Editor Driven Layout MXL Flow

SiP Layout Option to Virtuoso Schematic Editor Flow

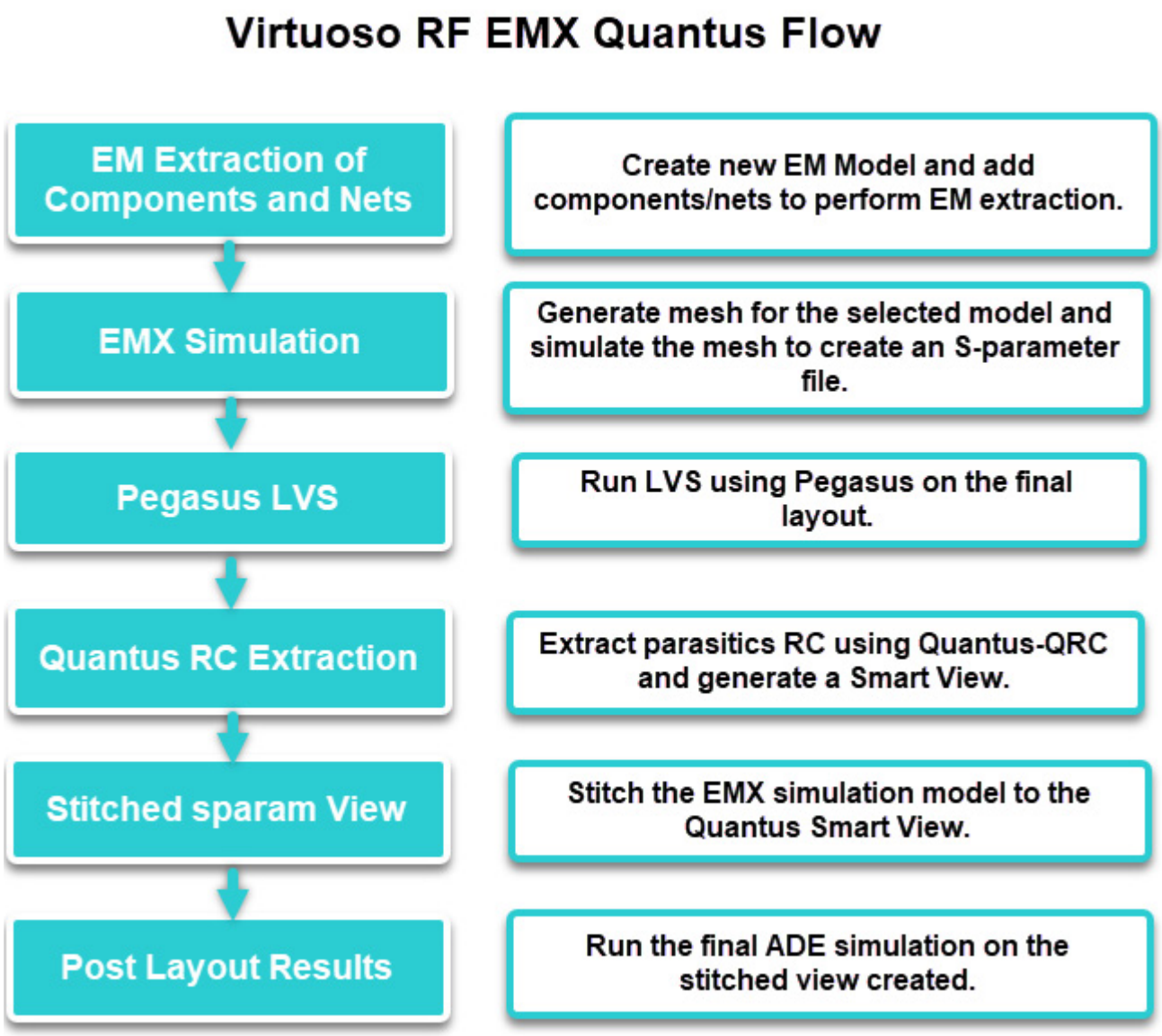
Virtuoso RFIC EMX Quantus Flow

The Cadence EMX Planar 3D Solver is an electromagnetic simulator for high-frequency, RF, and mixed-signal integrated circuits. It allows designers to accurately and efficiently simulate large RF circuit blocks, characterize the behavior of passive components, and analyze the parasitics due to interconnect. The EMX Planar 3D Solver offers complete automation coupled with high speed and accuracy. The EMX Planar 3D Solver is integrated with the Cadence Virtuoso custom IC design platform and Cadence Spectre models.

The Cadence Quantus Extraction Solution is the industry's most trusted sign-off parasitic extraction tool and is a leader in 3nm design adoptions and tapeouts. As a unified tool, the Quantus solution supports both cell-level and transistor-level extractions during design implementation and signoff. It is an integral component of the in-design methodology with the Virtuoso Studio. Quantus Extraction Solution lets you perform post-layout parasitic extraction of resistive, capacitive, and inductive effects in designed devices and wiring interconnects of digital, analog, and RF designs.

Using the Virtuoso RF Solution in the Virtuoso RFIC EMX Quantus flow, an RFIC designer can take advantage of several different EM simulation techniques to meet her requirements. Quantus solution supports several output formats, such as SPICE, transistor-level DSPF, or Quantus Smart View. Smart View is the enhanced version of extracted view output showing significant improvements with respect to runtime, memory usage, and netlist size. To combine

EM extraction of RF critical parts with Quantus parasitic extraction, use the Electromagnetic Solver Assistant in Layout EXL as the cockpit for defining your EM model.



Related Topics

Virtuoso RF Schematic-Driven Flow

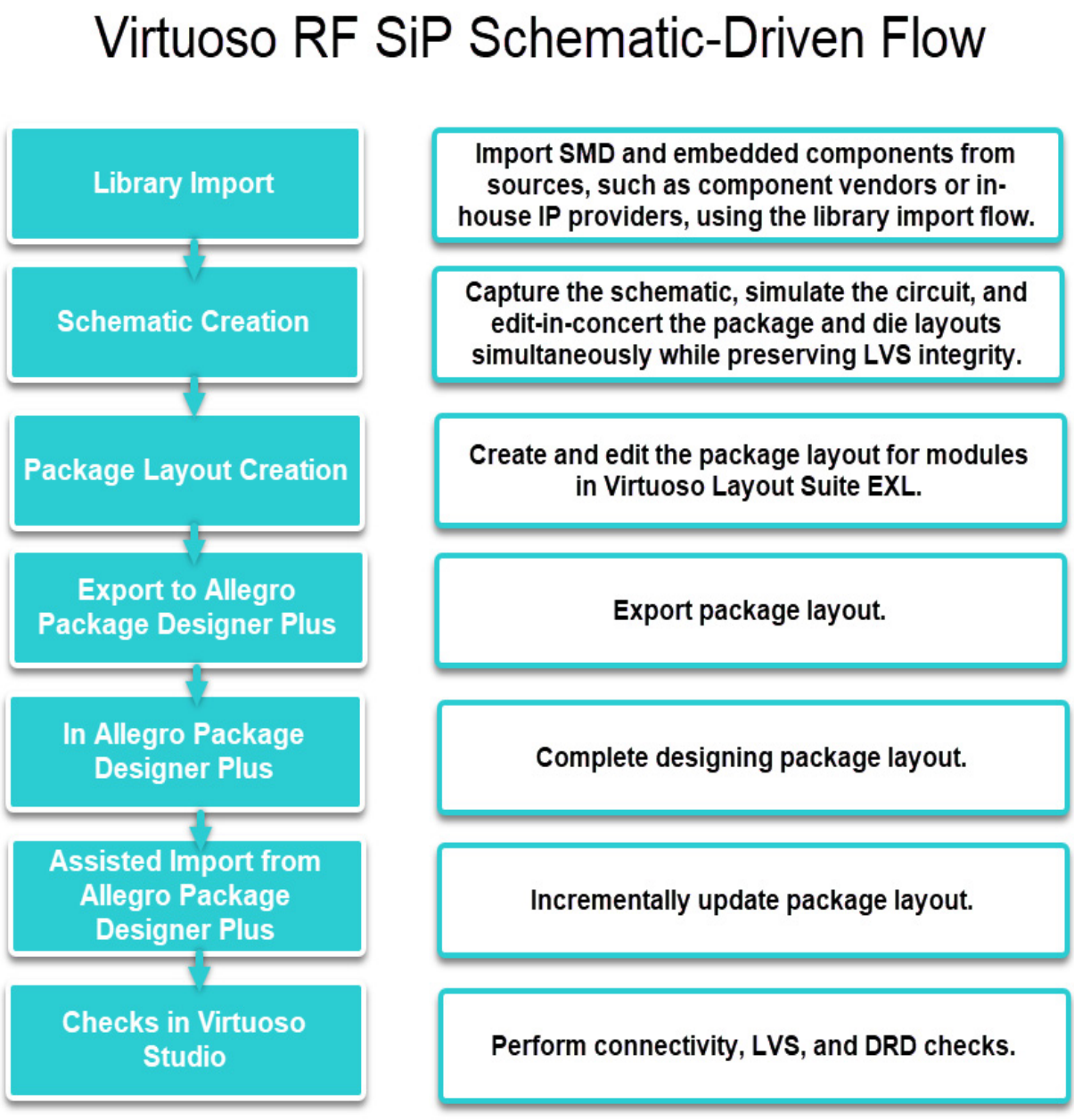
Virtuoso RF Library Import Flow

Virtuoso RF Schematic-Driven Flow

The Virtuoso RF Solution uses the Layout XL *Generate All From Source* (GFS) command and LVS capabilities in Virtuoso to fill the verification void present in many current design flows. In a typical Virtuoso RF Schematic-Driven flow, you export a die symbol from Virtuoso Layout Suite MXL (Layout MXL) to create a die symbol and an annotated abstract. This symbol can be used in conjunction with components sourced from different vendors or in-house libraries to create a package schematic in Virtuoso Schematic Editor. The schematic can be used as a connectivity reference to create a package layout using GFS. The package layout can be edited using package editing capabilities that allow the native creation and manipulation of packaging world concepts, such as curved shapes, voiding planes, and mechanical drill holes.

The package layout can be verified using a high accuracy 3D extractor, such as Clarity 3D Solver. Logic changes to the schematic and LVS checks while editing the layout allow the layout to be LVS clean through the design creation and editing process. At any point in the layout editing process, the design can be exported to the Allegro platform for further editing and imported back into the Virtuoso Studio. The round trip allows the connectivity reference in the Virtuoso schematic to guide the resolution of any connectivity conflicts between the

Allegro edited layout and the schematic. The layout can be exported to Allegro Package Designer Plus to finalize the layout for manufacturing.



The flow involves various tools, such as Allegro, Sigrity™, Virtuoso Schematic Editor, Virtuoso ADE Explorer, Virtuoso ADE Assembler, Design Data Translators, and Virtuoso Visualization and Analysis XL.

Related Topics

Virtuoso MultiTech Framework

Virtuoso RF Library Import Flow

Virtuoso Schematic Editor

Virtuoso ADE Explorer

Virtuoso ADE Explorer

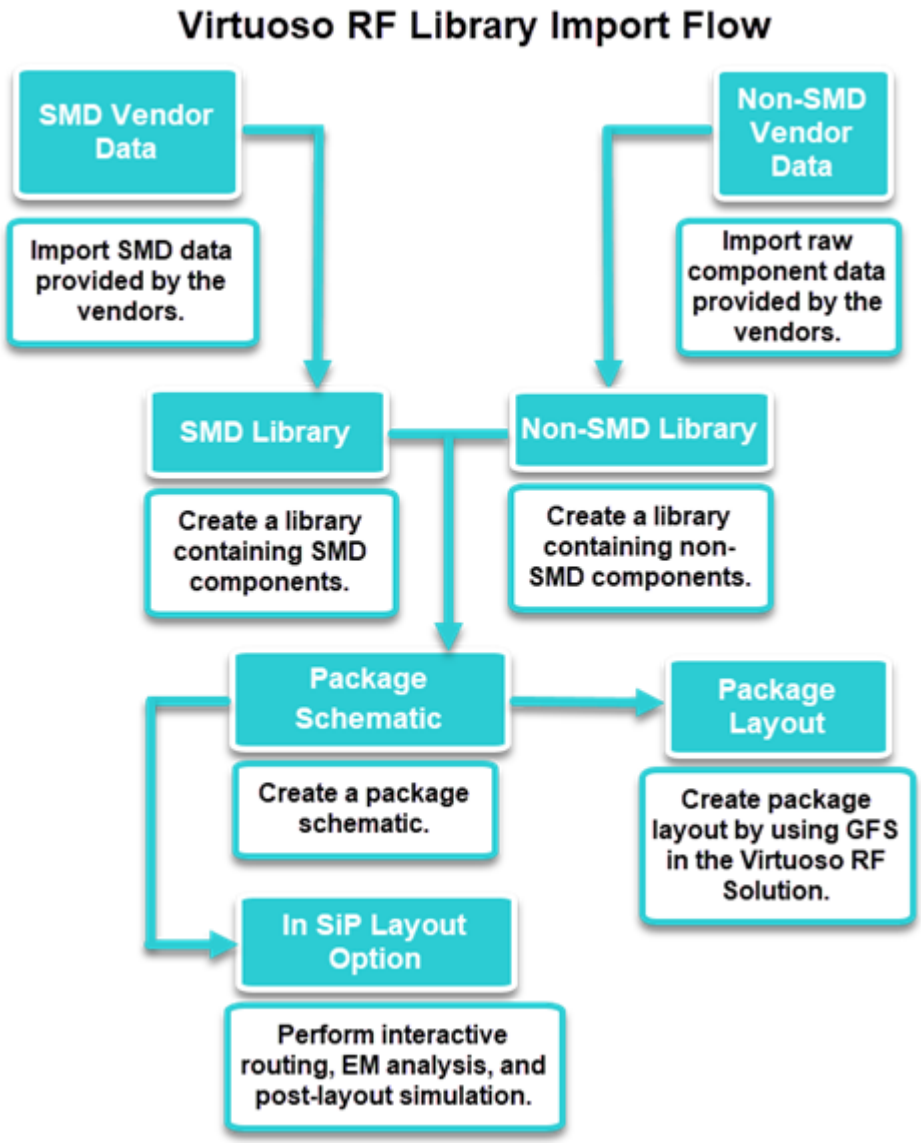
Design Data Translators

Virtuoso Visualization and Analysis XL

Virtuoso RF Library Import Flow

Library import is a crucial starting point of the Virtuoso RF Solution. The sub-tasks in this part of the flow are managed by the librarian. The flow enables you to use the raw component data

provided by the vendors and convert them into parts (cells) that can be used in packaging and simulation views in Virtuoso.



The S-Parameter or SPICE model files for devices from vendors do not have the required header information apart from some information about the port assignment. Each model represents the device under a different operational condition and so, in addition to the model files, the vendor also supplies a CSV file that contains details about each of these parts, such as part number, simulation frequency range, phase balance, and so on for the corresponding model.

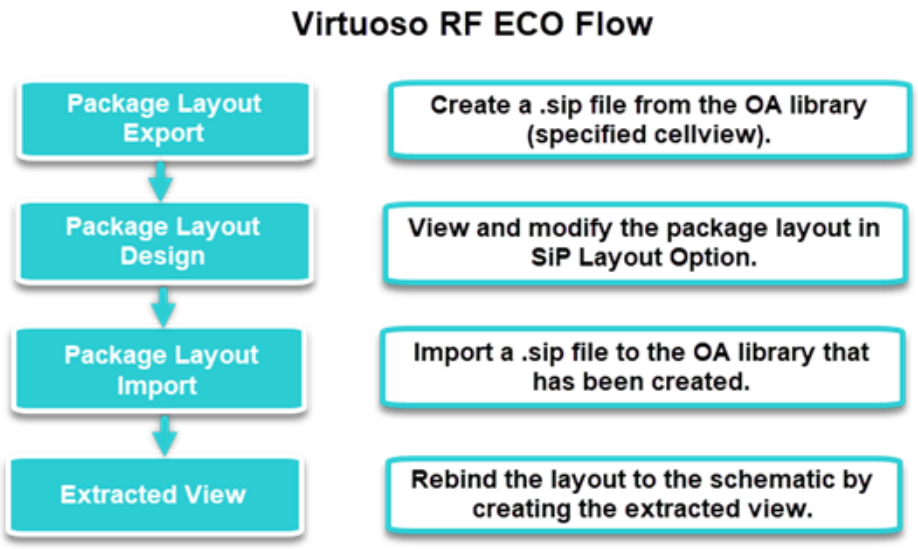
To create parts by using the model and CSV files for a given device, a model import wizard is used in this flow. It allows you to create the part table from CSV shared by the vendor to ensure that the part table, which includes all the part variants, is available for packaging in Virtuoso.

Related Topic

Managing Unified Libraries

Virtuoso RF ECO Flow

The ECO flow involves exchanging the package layout between the Virtuoso Studio and SiP Layout Option to complete designing the package layout before sending for manufacturing. Use Allegro translators for creating technology file and importing libraries from the Allegro Package Designer Plus. Package designers place and route parts in the SiP layout. Subsequently, the layout is imported into Virtuoso and verification checks are done.



Related Topics

Technology File

Library Import

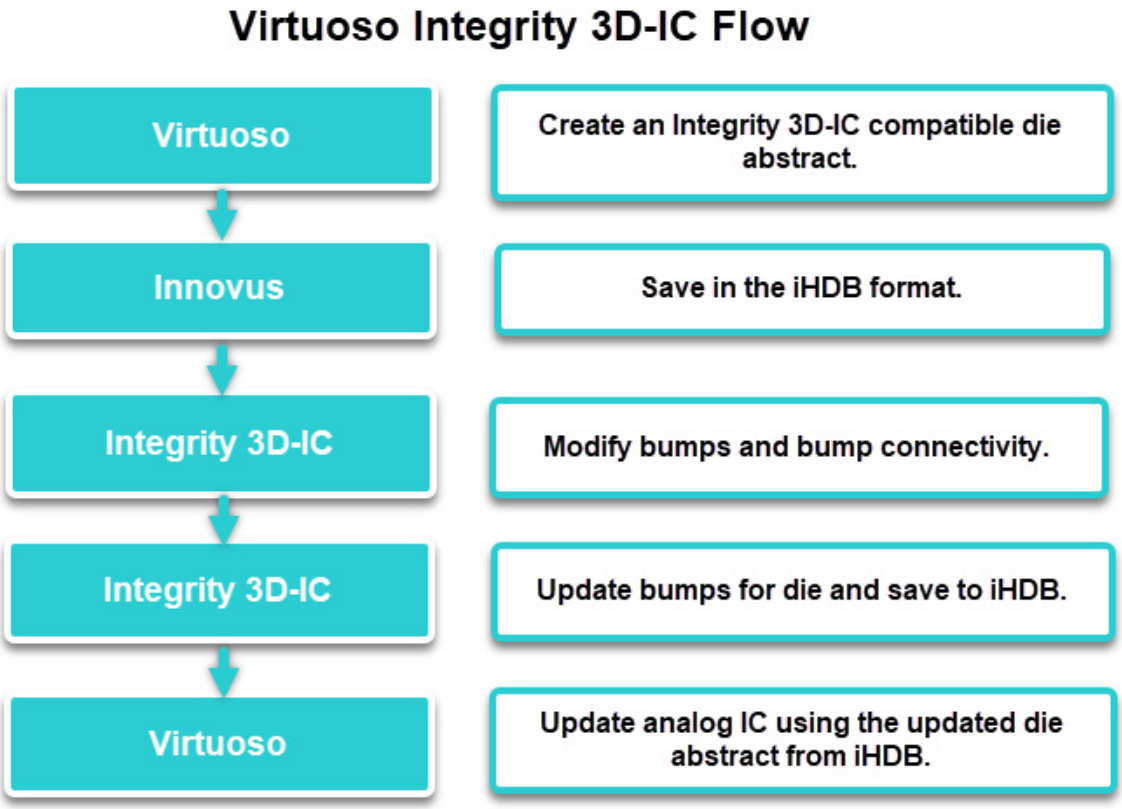
Virtuoso Integrity 3D-IC Flow

The Integrity™ 3D-IC platform enables 3D design planning, implementation, and system analysis.

Three-dimensional IC stacking often has analog ICs that are designed in Virtuoso but the bump planning and interaction with other ICs or interposers is done in Integrity 3D-IC. For the Virtuoso Integrity 3D-IC flow, an analog IC in Virtuoso is the starting point. The bump information is passed from Virtuoso through the Integrity hierarchical database (iHDB) to Integrity 3D-IC. Bumps are modified in Integrity 3D-IC and the modified bump information is passed back through iHDB to Virtuoso. To transfer the bump information across various platforms, a die layout is reduced to a smaller die abstract, which contains only the bump information and the die boundary.

It is important that the bumps, pads, or IOs are always in sync when designing a 3D-IC system. Both the analog IC designer working in the Virtuoso environment and a system designer working on the Integrity platform must be able to transfer data seamlessly to achieve

the system bump planning.The flow ensures that the changes made by an IC designer are correctly reflected in Integrity 3D-IC and vice-versa.



Related Topics

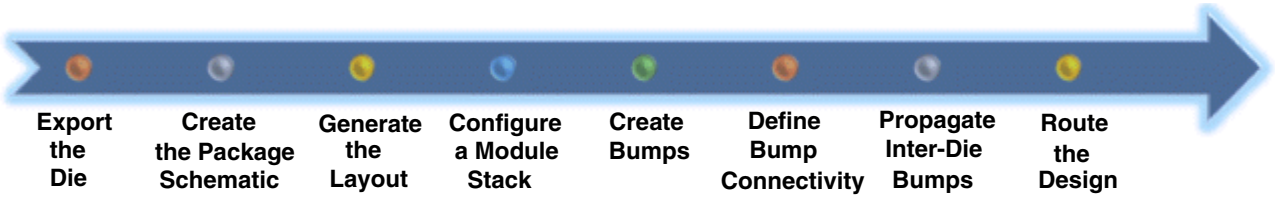
Creating and Verifying Integrity 3D-IC Compatible Die Abstracts

Exporting Dies

sameTechnologyAbstract

Virtuoso Stacked Silicon Solution Flow

Virtuoso Stacked Silicon Solution flow provides the required interface and options to design compact, stacked ICs. The following diagram depicts the overall Virtuoso Stacked Silicon solution flow.



In this flow, you can instantiate a die footprint in the package layout from a package library. The input from the package library includes a cellview that contains a layout, schematic, and symbol view. The output is a die footprint that is represented as a cellview and includes an abstract, a TILP, a schematic, and a symbol view.

The symbols of dies obtained from die export need to be arranged in a package schematic. A package schematic contains the IC and package portions of the design, which are represented, designed, and verified within a single environment.

Once the package layout has been generated from the package schematic, you can arrange the generated instances in the layout canvas and define the stack settings. Subsequently, you can create bumps and TSVs for the flip-chip dies, define connectivity for the bumps by assigning each bump to a net, and propagate the bump information to the dies on which the original die would be vertically stacked. Propagating helps align bumps in the two stacked dies.

Routing the design automatically or interactively by using a suitable router can be done at the end.

Related Topics

Creating a Package Schematic

Generating a Layout

Configuring a Stack

Creating Bumps and TSVs

Assigning Connectivity between Bumps

Propagating Bumps

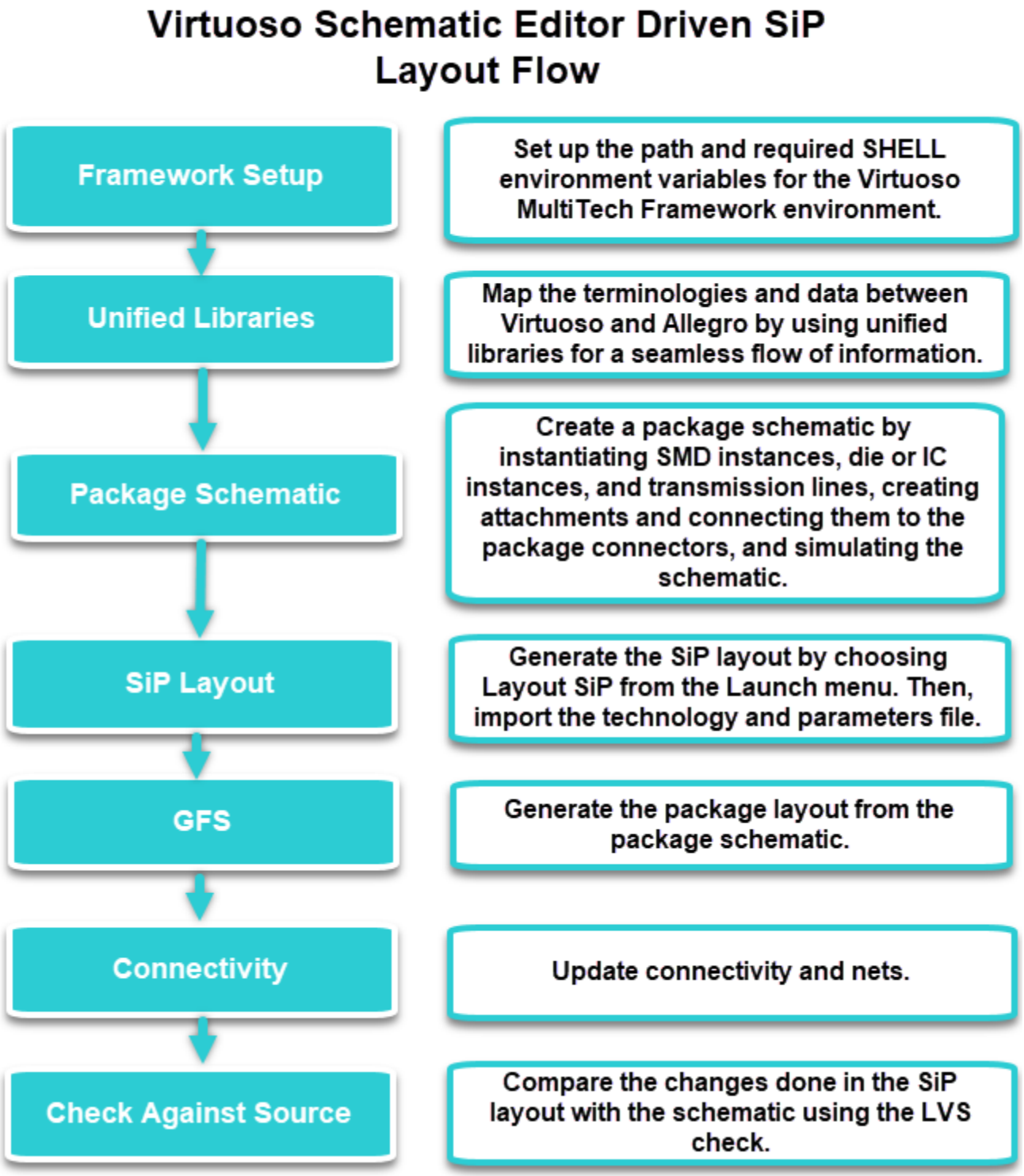
Virtuoso Interposer Router

Performing Interactive Routing

Virtuoso Schematic Editor Driven SiP Layout Flow

Cadence SiP Layout Option has many features for package and module implementation alongside a complete complement of constraint-driven verification and automation tools to complete the implementation. Artwork and manufacturing activities must be performed in SiP Layout Option. Teams that do day-to-day module and package design in SiP Layout Option can enjoy benefits from using a Virtuoso Schematic Editor driven flow without changing their use model. In addition, it provides the ability to mix high-accuracy extraction models with ideal models and simulate the design along with the testbench in Spectre. Unified libraries let you

map the terminologies and data between Virtuoso and Allegro for a seamless flow of information.



Related Topics

Virtuoso MultiTech Framework Setup

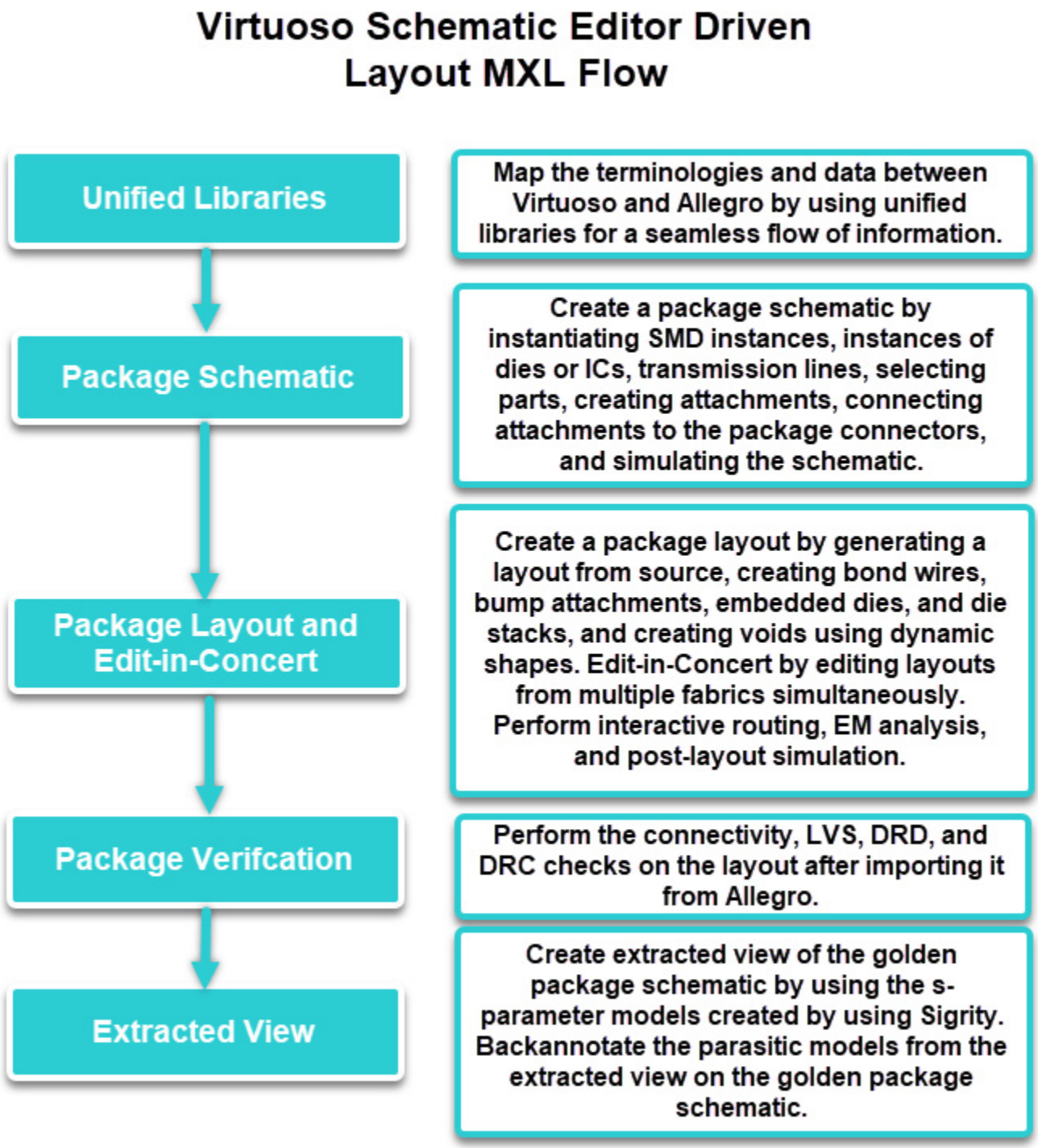
Views in the Unified Library

Types of Libraries for Creating Unified Libraries

Virtuoso Schematic Editor Driven Layout MXL Flow

Teams that are used to the Virtuoso Studio can benefit from this flow. This flow enables the package designers to assemble and simulate the package on one platform. You can create a package layout by generating a layout from source and creating bond wires, bump attachments, die embedding, die stacks, and voids using dynamic shapes. Layouts from multiple fabrics are co-designed simultaneously. You can perform interactive routing and EM analysis using Clarity 3D Solver or EMX Solver. Additionally, the extracted view, which is created using S-parameter models, is annotated back to the golden package schematic.

The following diagram depicts the overall flow.



Related Topics

Creating a Package Schematic

Creating Package Layout

Edit-in-Concert

Verify the Package

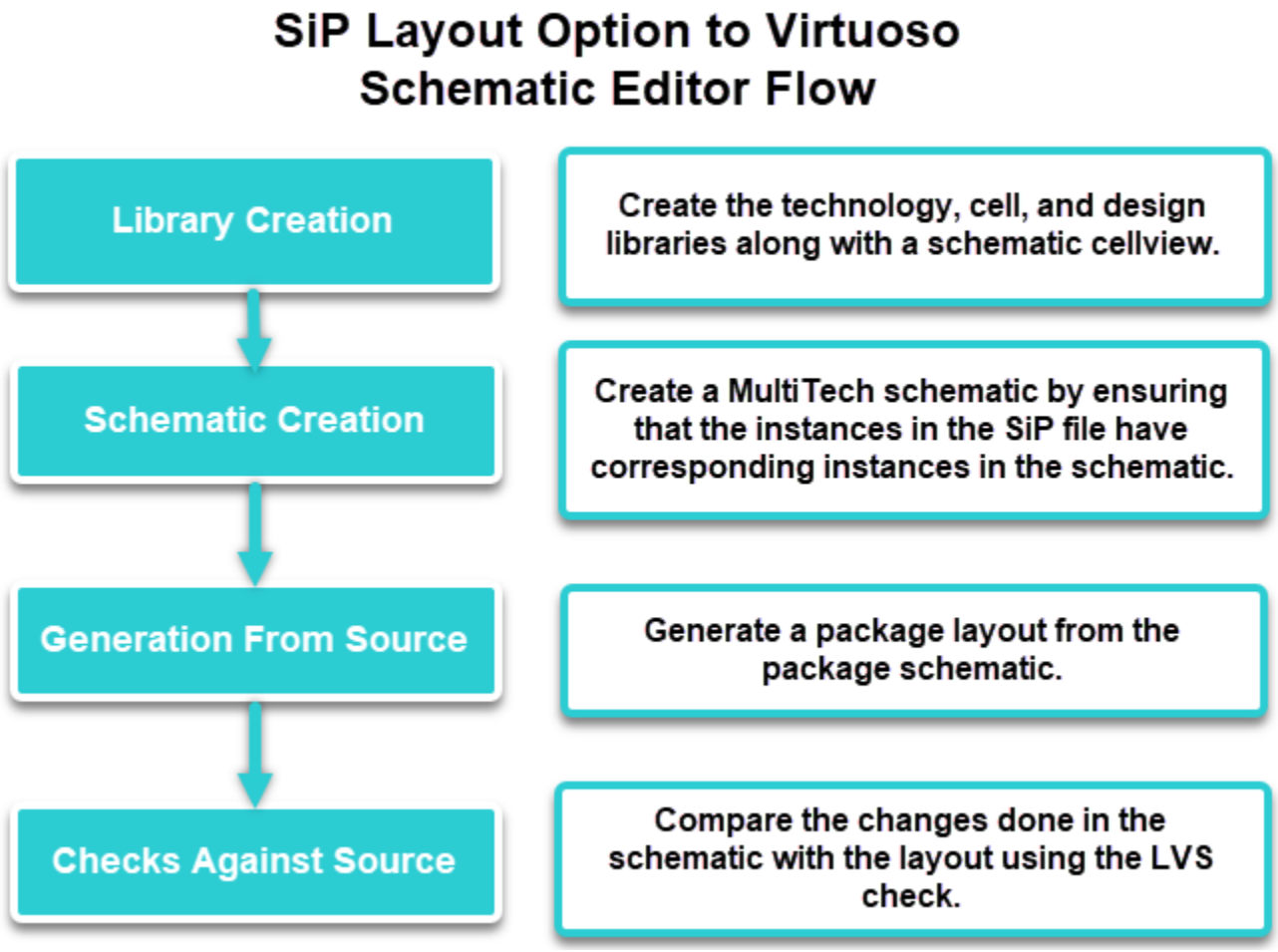
Performing 3D Electromagnetic Simulation

Creating an Extracted View

SiP Layout Option to Virtuoso Schematic Editor Flow

When creating a schematic in the Virtuoso RF solution from a SiP file, you can inherit all the netlist information already described in the SiP file instead of recreating them from scratch. You can use this schematic view to run the connectivity-driven flow in the Virtuoso RF solution, EM extraction, and simulation flows.

The following diagram depicts the overall flow.



Related Topics

Creating a Schematic Layout from a SiP File

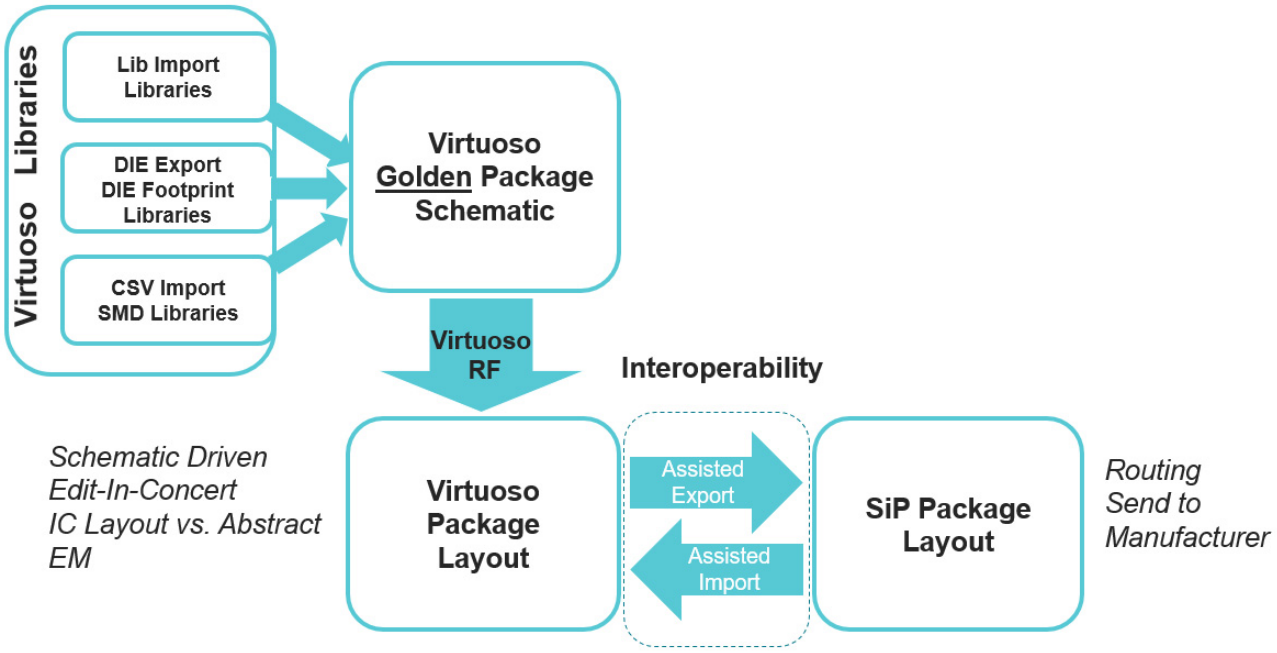
Create MultiTech Schematic Form

SiP to Virtuoso Layout Assisted Import and Export Flows

The assisted import flow is used to import changes made in a SiP file and merge them with an existing library in the Virtuoso RF Solution. The flow provides an environment to review an incoming SiP file for layers, vias, new or modified instances, placement, routing, mapping with the golden schematic, and comparison of IC layout with IC abstract. The Virtuoso libraries are updated with the changes from the SiP file. You must also verify the SiP file against the golden schematic.

The assisted export flow helps ensure the seamless interoperability between Virtuoso and Allegro to avoid losing data during file transfers. This flow is more suitable for ECOs. The type of edits supported for updating a SiP layout include routing, placement, connectivity, die pin edits, die abstract re-mastering or renumbering, and SMD creation. Some of the edits, such as die or BGA creation, scribe, shrink, and thermal expansion are not supported for updates in a SiP file.

The following diagram depicts the overall flow.



Related Topics

Updating a Virtuoso Layout From a SiP File

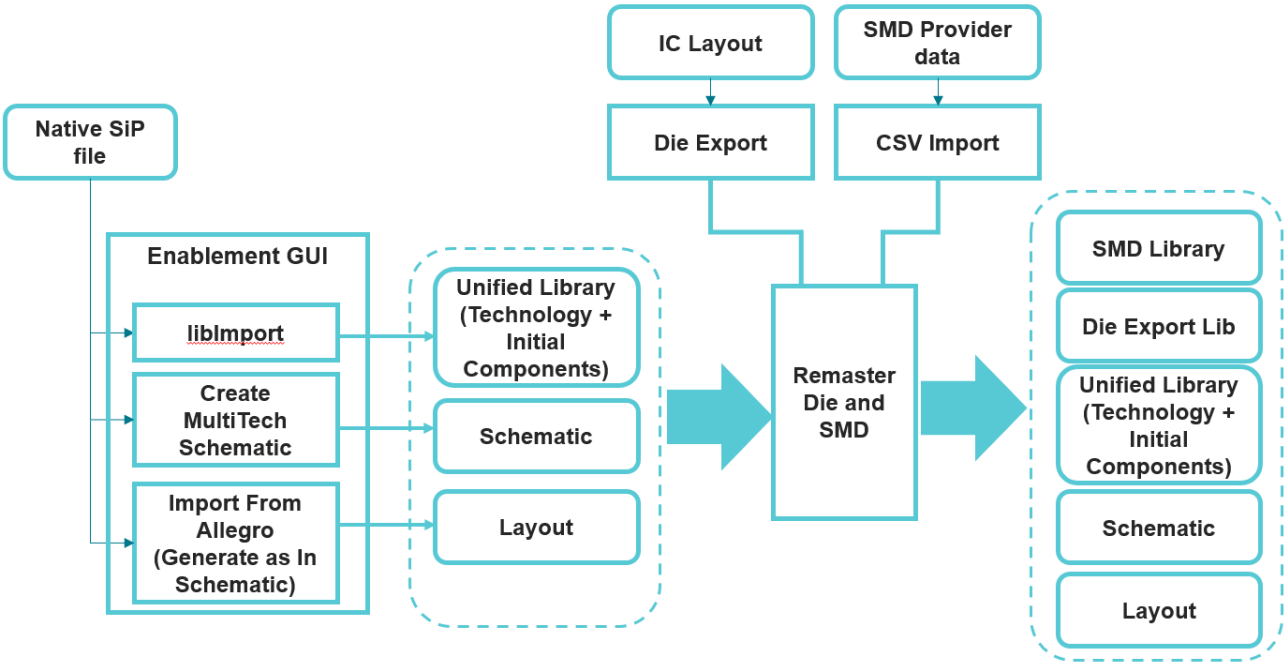
Allegro Design Layout Importer Form

Virtuoso Layout to SiP with Assisted Export

Export Design Update Form

Multi-Technology Enablement Flow

The enablement flow stitches together the libimport, multi-technology schematic creation, and layout import from Allegro process in a single step. The initial Virtuoso RF Solution database is made of a unified library containing the technology and other cells, a schematic view based on the SiP file content and connectivity, and a layout view in sync with the schematic. This design database created from a native SiP file is the starting point for the Virtuoso Schematic Editor Driven SiP Layout Flow.



Related Topics

Initial SiP File to Virtuoso RF Solution Database

Virtuoso Multi Technology Enablement Form

3

Introduction to Packaging

Virtuoso RF Solution enhances the capability of Virtuoso to create packages. Packaging involves translating the logical design (schematic) captured into a physical design ready for placement and routing using Layout MXL. You can create or modify package layouts in the presence of the package constraints. The package components can be placed and routed in Layout MXL. You can also edit shapes.

Packaging-Related Terminology

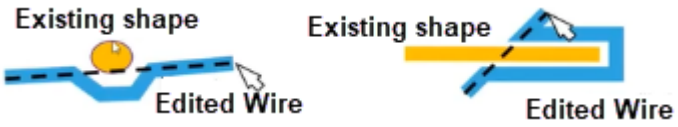
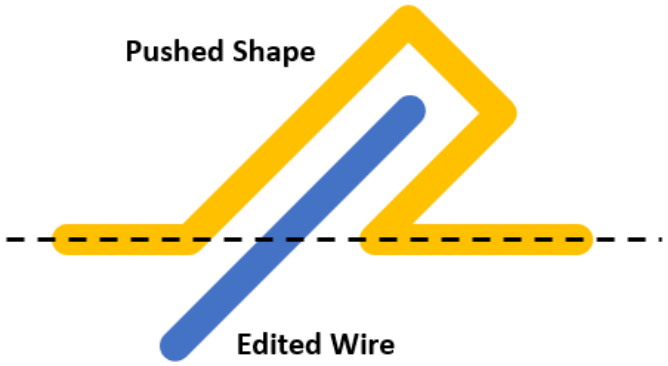
It is important to know a few packaging-related key terms.

Package Terminology	Definitions
Package	A physical symbol designated as the Drawing Type package in the Symbol Editor. Typically used as the database element for components that have electrical connectivity. Stored as a library element with an extension of `.psm`. A package contains the padstacks, labels, outline, TILPs, and so on. It visually represents the component in Layout MXL. Note that a single package may consist of a symbol or multiple logical symbols.
SMD (Surface Mounted Device)	A technology using surface-mounted components that have pins glued to the surface of a design. Designs that contain SMDs can have components at the top and bottom.
Embedded Component	Embedded technology plays an active role in shrinking interconnect path between components and reducing the transmission loss. Embedded components could be Active Devices (ADs) or Passive Devices (PDs). Embedding components leads to reduction of connection points, external pads, number of through holes, and lead length so that circuit board integrity can be improved and parasitic inductance of printed circuit can be decreased.

Package Terminology	Definitions
Transmission Line	An electric conductor exhibiting series inductance and shunt capacitance distributed along its length and logically divided into chunks. A signal must charge up each chunk or inductance and capacitance before it is passed along to the next chunk, therefore, reducing the propagation velocity.
Heterogeneous Integration	Heterogeneous integration is about integrating components with different functionalities and thicknesses, or could be available in the market as pre-packaged components with solder terminations, such as BGA, CSP, in the inner layer of PCBs as assembled components. Using packaging technology to integrate dissimilar chips with different functions instead of integrating all the functions into a single chip and going for finer feature size achieves this.
Die, Die pad, Die Stack	Die is an unpackaged chip. Die pad is a metal contact on the die of an IC that is used to make electrical connections between the IC and the component (also called I/O pad or die pin. For flip-chip, they are called solder bumps, while for wire bound ICs they may be called bond wire pads). In IC tool terminology, wire bonded ICs are often referred to as bond pads. Die stack is a vertical stack of dies consisting of one or more dies, spacers, and interposers.
Bond wire, Bond finger	A wire (usually gold) that connects a die pad to its respective bond finger on the component substrate or to another die pad on another die. A metal pad on the outer layer of component substrate to which a bond wire will be attached to form an electrical connection between the component and die.
Flip Chip	An unpackaged integrated circuit that connects to a hybrid circuit by means of solder bumps on its faces that correspond to its pin-outs.
Silicon Substrate	The silicon "wafer" onto and into which the IC circuitry is placed.

Package Terminology	Definitions
BGA, LGA	Ball grid array (BGA) is a type of die component whose pins are solder balls arranged in a grid pattern. Land grid array (LGA) is a a type of die component with a rectangular grid of solder balls on the underside of a package.
Interposers	A substrate with a single conductor layer that is used in the manufacture of a die stack to support the die connectivity. It provides the capability to wire bound dies whose die pad positions create the wire-bound lateral spans that are beyond the physical limits of a wire-bounding machine.
Vias	An opening in a dielectric layer that connects adjacent conductor layers. A via is a plated-through hole with ETCH/CONDUCTOR on every ETCH/CONDUCTOR subclass. Vias make it possible to route a single connection through more than one ETCH/CONDUCTOR subclass. Also called a feedthrough.
Padstack	A list of all data for each pad definition in the design drawing; each pin and via refers to a padstack for size, shape, and drill information.
Cut Shapes, Drill Holes	Cut shapes is about trimming the conductive planes in the PCB into separate electrical pieces. Drill holes are important for multilayer PCB. These holes are used for electrical connection between each layers and fix or position the components.
Technology Independence	The ability to be used in any design and accept user-preferred units, constraint and parameter values, and user properties on any platform.
TILP	Technology Independent Layout Pcells (TILPs) are created from the die symbols, which have been created from exporting the die. TILPs are added to the libraries from importing into the package layout.
Planes	A conductive layer in the cross-section editor designated as layer type "plane". These layers are typically used to create shapes for the purpose of Power and GND distribution. These layers exist within the component substrate that routes the signals and distributes the power from the die to the host PCB.

Package Terminology	Definitions
Voiding Shape	A void is generated for dynamic shapes when a change is made that affects the shape connectivity. It insulates the signal shapes from other shapes, such as power and ground. Voiding associated with the rectangular pads maintains a more consistent minimum clearance to the pad boundary. It improves the copper shape flow between the adjacent rectangular pads.
IC and Package Shape Interface	IC and package interconnect, which is through bond wires or IO pads.
Significance of Ground and Power Planes in Packages	Ground and power plane is also a shape in package. The package traces are long and they behave like transmission lines. Therefore, there is a need to provide a return path for it. On the other hand, IC traces are short so no planes are needed for return path. Power planes reduce the impedance of the power net which, in turn, reduces the voltage drop.
Stackup	The arrangement of copper layers and insulating layers that make up a PCB prior to the board layout design. While a layer stack-up allows you to get more circuitry on a single board through the various PCB board layers, the structure of PCB stack-up design has many other advantages: ■ Minimize the circuit's vulnerability to external noise as well as minimize radiation, reduce impedance, and crosstalk concerns on high-speed PCB layouts. ■ Balance the need for low-cost, efficient manufacturing methods with concerns about signal integrity issues ■ Enhance the electromagnetic compatibility of the design as well.
WLP	Wafer-level packaging (WLP) is the technology of packaging an IC that is the part of the wafer itself. It involves attaching the top and bottom outer layers of packaging and the solder bumps to ICs on the wafer, and then dicing the wafer. All packaging and interconnection must be fabricated on the wafer prior to dicing.

Package Terminology	Definitions
Hug	A mode in which the edited wire avoids moving the existing shapes and respects `minSpacing` value set between the wire and the existing shapes. 
Shove	A mode in which an edited wire pushes the non-static shapes when it is extending and respects `minSpacing` values set between the wire and the existing shapes. 

Package Definition

The package is an advanced environment for the physical layout of printed circuit boards (PCB). You can place and route a design, generate the output, and documentation necessary information for its manufacture. Layout Suite MXL allows design considerations to be automatically incorporated into the physical design.

In a typical package layout, you can place SMD Pcells corresponding to schematic components and T-line Pcells as a topology. The package layout views are placed with flight-lines to allow guided placement. For routing and placement in a package layout, abutment of RF-connect for RF routing, placement of GND/VCC shapes, addition of guides to place landing pads equidistant from each other, movement of other pads when one of them is moved, and placement of power rings for power pads is done.

Components of a Package

Virtuoso RF Solution is a complete physical design and manufacturing verification solution for complex Virtuoso-based package design, including die bump array/BGA integration refinement using die abstracts. It supports all the popular package interconnect and assembly methodologies and provides comprehensive constraint-driven layout of the package substrate.

This topic presents an overview of the component design and die-to-I/O routing. Design technology for packages varies. Depending on certain needs, substrates can be laminate-based (organic), ceramic, thin film (silicon), or a combination of materials. These needs may be based on cost, performance, signal, and thermal considerations.

Two important package components are, Land Grid Array (LGA) and BGA (Ball Grid Array). These are an array of chip connections, using surface-mount technology, in the form of solder balls.

Related Topics

Bumps (IO pads)

Through Silicon Vias (TSVs)

Silicon Interposers

Padstacks

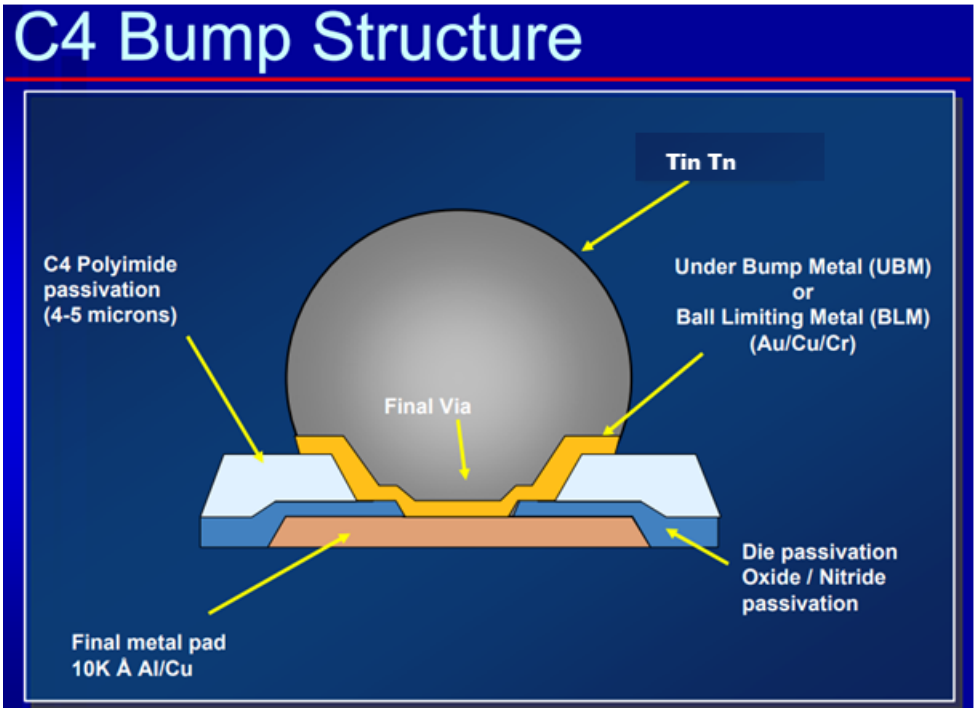
Stackup Information in Substrate

Wafer-Level Packaging

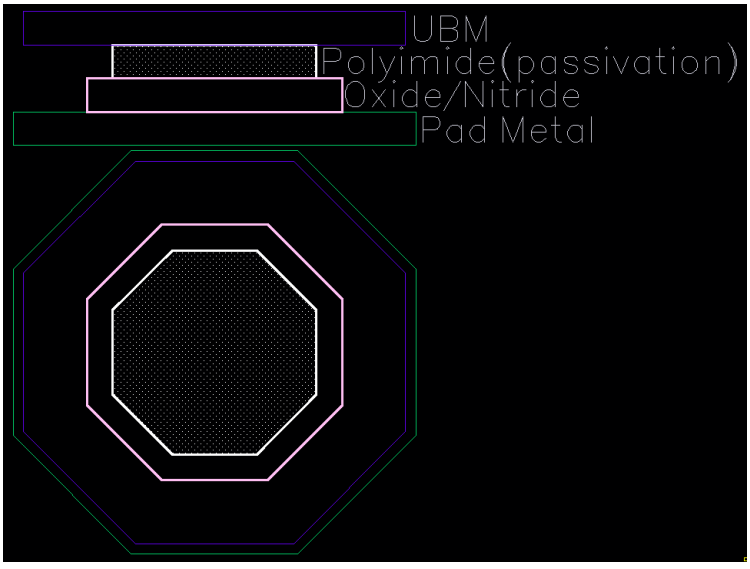
Bumps (IO pads)

To connect the dies, solder balls are placed on the top metal layer or on the backside metal layer. These solder balls and the metal pads beneath them are called bumps (IO Pads). Aligned IO pads between dies are called micro bumps or landing pads.

Cross-die signals and power travel to adjacent dies through micro bumps. IO pads between a die and the package substrate are called flip-chip bumps. These are the solder joints on the IC. Look at the following bump cell to know about its components.



This is a typical bump cell found in a PDK along with the cross-section.



Related Topics

Through Silicon Vias (TSVs)

Silicon Interposers

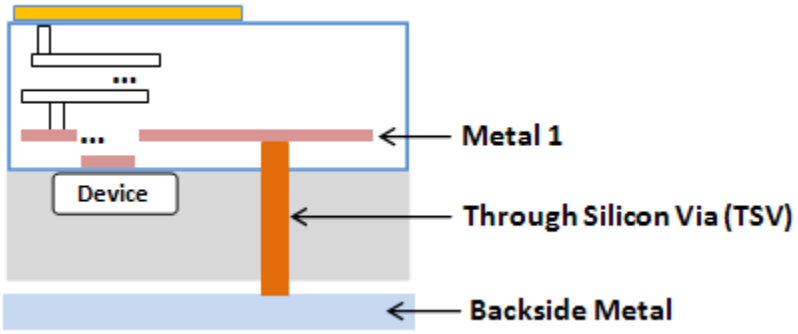
Padstacks

Stackup Information in Substrate

Wafer-Level Packaging

Through Silicon Vias (TSVs)

TSVs are copper vias with diameters ranging between 1 and 30 microns that pass through a silicon substrate.The top cap layer of a TSV is the first normal routing layer, Metal1, and the bottom cap layer of TSV is the backside metal layer. Therefore, TSVs enable signal propagation and power delivery between the top metal layer and the backside metal layer.



Related Topics

Bumps (IO pads)

Silicon Interposers

Padstacks

Stackup Information in Substrate

Wafer-Level Packaging

Silicon Interposers

Silicon interposers are electrical routing channels that help establish much finer die-to-die interconnections, thereby increasing the performance and reducing the power consumption. Silicon interposers are dies that can include TSVs to provide connections from the upper metal layers to additional backside metal layers. Also, for minimizing differences in thermal expansion and contraction because the materials are similar.

Related Topics

Bumps (IO pads)

Through Silicon Vias (TSVs)

Padstacks

Stackup Information in Substrate

Wafer-Level Packaging

Padstacks

Each symbol pin in a design must have a padstack associated with it. The padstack describes how the symbol pin connects to each layer in the design.

A padstack is a file that contains the following information for each layer:

- Pad size and shape
- Drill size and drill display figure

A padstack also describes the following information for the TOP and BOTTOM layers:

- Soldermask
- Pastemask
- Filmmask

A padstack can also contain Numerical Control (NC) drill data, which the layout editor uses to create drill drawings.

Related Topics

Bumps (IO pads)

Through Silicon Vias (TSVs)

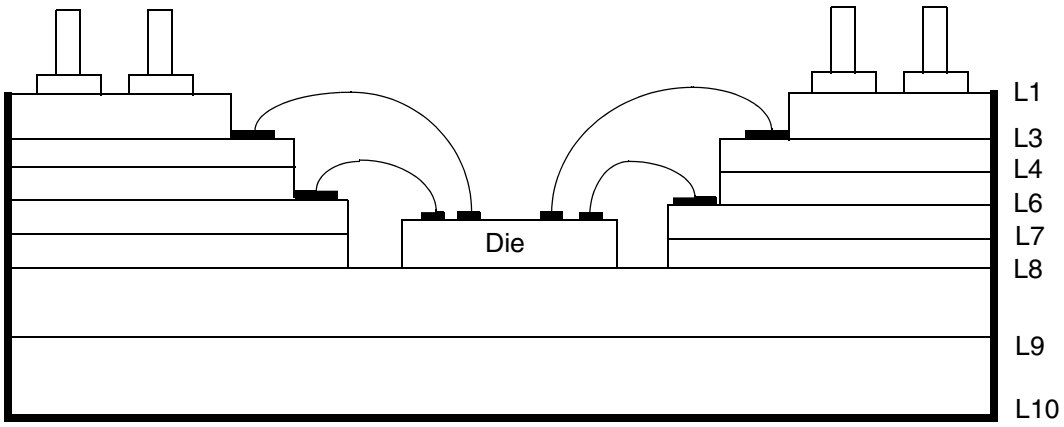
Silicon Interposers

Stackup Information in Substrate

Wafer-Level Packaging

Stackup Information in Substrate

The stackup information defines all the layers in the substrate that will be manufactured. This includes conductive layers, dielectric layers, paste layers, bond wires, pads, and shield planes.



The information necessary to complete an accurate stackup includes material, layer type, name, thickness, dielectric constant, and electrical conductivity.

The stackup of a component is important, not only for the physical characteristics, but also for electrical and thermal characteristics. With proper stackup construction, electrical and thermal simulations can provide a more accurate analysis of behavior. Without it, results become skeptical at best.

The stackup also provides the z-axis aspect of the electrical design, allowing for accurate positioning of conductive trace layers, power/ground layers, bond wire information, I/O pin position, and z-axis connections between trace layers or to a power or ground plane.

Information required for stackup modeling includes:

- Layer
  - Location
  - Material
  - Type (conductive, dielectric, shield)
  - Identifier or name
  - Thickness
- Electrical conductivity
- Dielectric constant

Layer Thickness

The overall thickness of the component is usually known and should be specified within the mechanical detailed information. Thickness is based on the number of layers required for the design. For example, a component may require 8 layers: 2 routing and 6 power/ground. The total thickness is the thickness of the 9 dielectric layers plus 8 layers of conductive material.

Individual layer thicknesses can be derived from the manufacturing data supplied by the foundry. You enter thickness data when you define the layer stackup.

Layer Materials

You should, at this point, know which materials to use for each of the conductive and dielectric layers. Material type is important to define the electrical characteristics of the component. You define these characteristics by specifying the electrical conductivity, and dielectric constant. However, you should obtain the exact specifications for the material through the manufacturing foundry, check them against the ECAD tool-generated values, and tune them to the manufacturing specification.

Layer Type

You specify a layer type to define the purpose the layer serves in the component design. Dielectric, conductive, plane, and bond wire are the most commonly used layer types, however, your design may require others. The significance of the layer type to the ECAD system is to specify effects (shield planes, design rule checking, and manufacturing output) for signal analysis.

Related Topics

Bumps (IO pads)

Through Silicon Vias (TSVs)

Silicon Interposers

Padstacks

Wafer-Level Packaging

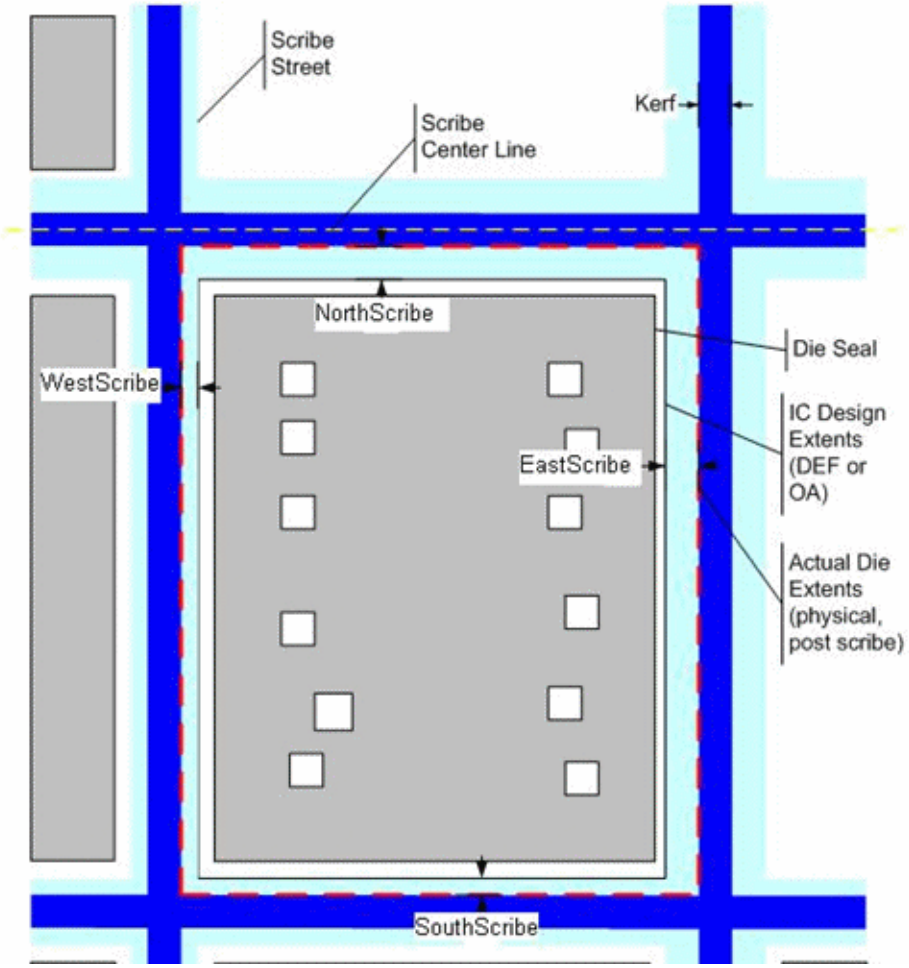
Technology File Packaging Definitions

analysisAttributes

Wafer-Level Packaging

During manufacturing, dies are generally created in batches where many dies are created on one wafer board. When the dies are laid out on the wafer, a space is left between each die boundary so that the scriber can cut the individual dies. This space (scribe area) is wide enough for the saw blade to pass through without affecting the components on the die. When

a saw cuts, it removes a channel on the material it is cutting. The figure below shows the scribe area between dies on a wafer board.



Previously, when you created an Edit-in-Concert die in an IC tool (or imported the die), its physical extents were based on the design extents from the IC design tool, not the actual physical qualities of the die. Yet, you need to consider these actual physical extents when placing dies in a component substrate layout. You must use them for any measurement, clearance, assembly, or placement rule checks that you perform in the component substrate design. This is particularly important in situations, such as measuring the clearance between the 3D path of a bond wire and the edge of the die, or the distance between closely-spaced components. If you do not use the actual die size (including the scribe area), you may place components too closely together in the layout design and, at the time of manufacturing, that will conflict with the placement of other components.

Related Topics

Bumps (IO pads)

Through Silicon Vias (TSVs)

Silicon Interposers

Padstacks

Stackup Information in Substrate

Phases of Package Creation

This topic describes the framework required to create packages.

Template Files

Providing stackup information results in more accurate thermal and signal analysis, design rule checking, and ready-to-manufacture routing. Once completed, stackup information can often be stored in an ASCII file format (template file) that is recognized by the ECAD system.

Template files store a wealth of information that can then be reused on other similar designs to reduce setup time and effort.

Related Topics

Constraint Definition

Placement

Thermal Analysis

Die-to-Component I/O Net Assignment

Routing Concerns

Voiding and Connectivity

Constraint Definition

With the physical modeling of the component substrate complete, the next phase is to set up constraints.

Constraints fall into two categories: physical and electrical. Physical constraints are driven by manufacturing guidelines, though electrical rules may impact the physical rules. For example, an electrical rule may be a 50-ohm line impedance that translates into a 4-mil trace width. Electrical rules are engineering-driven and are imposed to ensure signal quality and overall component performance.

Physical Constraints

Physical constraints can be further broken down into two categories: Physical (Line and Via sizes) and Spacing (Line, Via, Pad, and shape spacings). Again, most of the physical rules are driven by manufacturing specifications, though some latitude may be given depending on the foundry.

You can also assign physical constraints to specific nets or groups of nets (net classes). Net classes allow you to specify different line widths, via sizes, and element-to-element spacing to the entire group or to a specific area layer of the component substrate.

Electrical Constraints

Electrical constraints can be divided into two categories that are commonly lumped together: delay and distortion (D&D). Delay refers to the interconnect delays introduced by the physical layout, typically in terms of nanoseconds (ns). Distortion refers to sources of noise caused by the physical layout, such as undershoot or crosstalk. Distortion is measured in millivolts (mV).

You should divide signals in the layout into unique net classes based on performance requirements, for example, clocks and buses. Each constraint set would have its own noise budget and, therefore, corresponding distortion (overshoot, undershoot, crosstalk, and so on) constraints. For each net class, you also define timing constraints, such as delay and matched delay. In addition to defining electrical constraints, you should define any thermal constraints.

Template Files for Constraints

The effort involved in setting up all of the required constraints in a design may seem cumbersome and time consuming. Technology files allow you to dump out an ASCII representation of all defined constraints, which you can then import into other designs.

Technology files include:

- Net classes
- Physical constraints
- Electrical constraints
- Stackup Information
- Design size, units, and origin
- Special attributes and properties created within the design

Although every design has some unique requirements, template files can minimize the constraint definition effort by allowing you to modify an existing data file rather than starting a new file.

Related Topics

Placement

Thermal Analysis

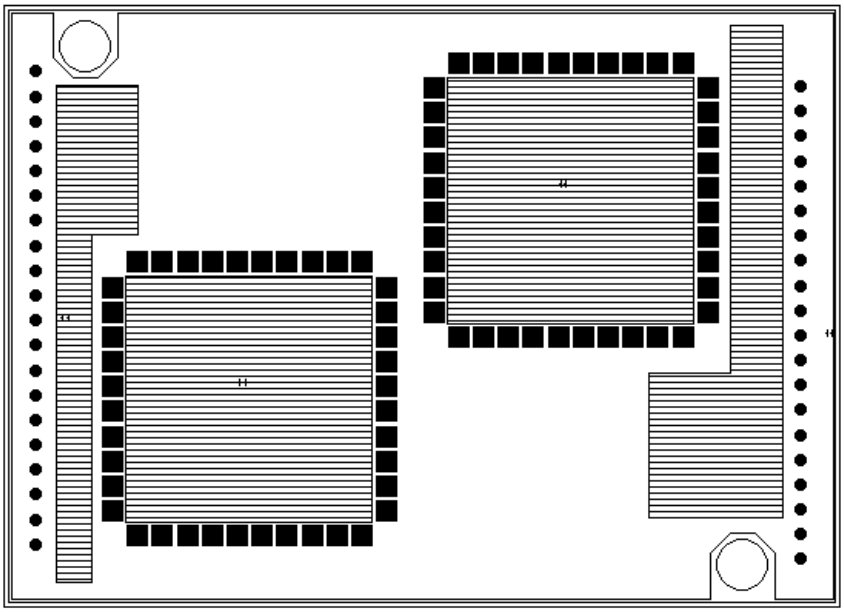
Die-to-Component I/O Net Assignment

Routing Concerns

Voiding and Connectivity

Placement

This phase is for defining the locations of the design elements with respect to the package. While there may be only a few elements to place, this can be difficult because of geometric restrictions of the substrate, such as cavities or geometric centering between all of the component I/Os.



If the component has multiple die, some latitude may be given to the designer for placement. In this situation, the designer is responsible for optimizing for die-to-die interconnect while at the same time optimizing for die-to-component fanout routing.

Die-to-Die Placement

For die-to-die placement optimization, the designer should attempt to minimize crossing of signals between die and the number of signals that pass through another die to reach its destination. To accomplish this, you should attempt to rotate dies, align dies that interconnect with each other, and place dies relatively close to each other to optimize the routing real estate. In most cases, however, component designers do not have much freedom in die rotation and placement. Therefore, if you cannot achieve optimized routing with imposed placement, it is best to consult with the logic and manufacturing engineers before making changes.

Die-to-Component Placement

For die-to-component placement optimization, die should be placed as close to the geometric center of the component as possible. If multiple dies are used, each die that connects to the component should be placed so that the die's I/O is on the outside edges, close to the component edge, and no obstructions exist between the die and the component I/O.

You should carefully place signals that require performance constraints, such as delay or crosstalk, or require special routing. Acknowledging these requirements allows for optimized real estate to handle discrete components.

Related Topics

Constraint Definition

Thermal Analysis

Die-to-Component I/O Net Assignment

Routing Concerns

Voiding and Connectivity

Thermal Analysis

Once you have placed components and defined constraints and stackup, you can perform thermal analysis. In this phase, you use thermal analysis to predict the junction and case temperatures within the component being designed. Through thermal analysis, you can quickly identify component temperatures that violate constraint criteria.

You can rectify thermal violations by applying one or more of the following corrective measures:

- Modify die placement, if multiples are being used
- Add plane layers to the stackup
- Use alternative substrate materials
- Add thermal vias
- Add heat sinks
- Experiment with alternative boundary conditions (estimate performance under various environmental conditions)

You can apply these measures in multiple “what-if” scenarios to arrive at an optimal solution.

Related Topics

Constraint Definition

Placement

Die-to-Component I/O Net Assignment

Routing Concerns

Voiding and Connectivity

Die-to-Component I/O Net Assignment

At this phase of component design, the only logic in the design database is the die and, in the case of FCMs, the die-to-die interconnect. This provides for efficient component design because die-to-component logic can be optimized only after you have defined the component description and placement. Without either piece, component I/O assignment becomes a blind exercise that results in poor interconnect efficiency.

With only die logic defined, you can optimize I/O assignment for routing and performance with minimization of interconnect length and logic criss-crossing.

Priority Nets

Prior to signal pin assignment, you should identify critical signals as priority connections. Depending on performance requirements, these signals may need to be the “shortest possible distance” to the component I/O, in which case manual pin assignment may be required. Many ECAD systems allow you to attach a special attribute to a net that requires a priority connection.

Pin Assignment

The first step in optimizing pin assignment is to determine which component I/Os feed power and ground connections. Most companies preassign pins in a netlist. The power/ground pin assignment determines the remaining available component pins that can be used for signal assignment. Of course, there must be enough I/O pins remaining to accommodate the number of signal I/Os.

Related Topics

Constraint Definition

Placement

Thermal Analysis

Routing Concerns

Voiding and Connectivity

Routing Concerns

Although the signal may require the shortest possible assignment, you must also consider routing. If the resulting shortest assignment results in connectivity crossing, you may need an additional routing layer. If an additional layer is not possible (or desired), you should make an assignment that selects the closest component I/O that also minimizes any signal crossing.

For general component I/O assignment, a utility should be available that scans both the die and the component I/O, take into consideration power, ground, and priority signals, and develop an optimized die-to-component netlist. Optimization should be based on overall

routing capability of the component. For multiple dies, this process may be incremental. During each step, you select the die I/O of one or more dies and direct the assignment to a specific location of the component. Otherwise, poor assignment may result.

Related Topics

Constraint Definition

Placement

Thermal Analysis

Die-to-Component I/O Net Assignment

Voiding and Connectivity

Voiding and Connectivity

Voiding helps designers route on the ground/power planes by insulating signal nets automatically. You need to specify the ground/power planes to provide reference planes for transmission lines. In addition, it reduces the impedance of the power/ground supply network and EM noise.

The signals going through ground/power planes are also required to route between signal layers separated by the planes.

Die-to-Component Interconnect

Die-to-Component interconnect involves fanning out all of the die-to-component interconnections and routing to the destination component pin. Depending on the technology being implemented, this routing may take on different forms:

- Routing patterns for Quad Flat Packs (QFP) and Pin Grid Arrays (PGA) are typically a triangular fanout pattern from the bond wire pads coupled with an “any angle” connection to the component pin.
- Routing patterns for Ball Grid Arrays (BGA) are typically an intricate weaving of traces through the flip-chip pin locations to an edge pattern of vias coupled with an intricate pattern into BGA ball locations.
- Routing patterns are a result of an optimized usage of routing real estate, resulting in the minimum number of routing layers.

Interactive routing is more suited for intricate routing patterns.

ECAD systems offer a host of interactive routing capabilities that you can use to semi-automatically build fanout patterns and then complete with “any angle” routing.

Through graphical representations of connectivity lines and online design rule checking, routing efficiency is easily realized as manufacturing concerns are minimized.

Die to Die Interconnect

When routing among dies, you must identify critical signals (clock, high speed buses) and route them first. Once you have routed critical signals, you can run signal analysis. Then, model the actual routed traces. You can use the new interconnect delays to verify that the timing budget has been met. Finally, you can edit the routed traces to reach the desired level of signal integrity for the critical signals.

You must specify manufacturing rules prior to routing. These rules include:

- Spacing (by layer, if applicable)
- Line widths
- Line impedance
- Legal via selection
- Blind and buried via spacing
- Min/Max stagger size

Power and Ground Vias

You must also route *power* and *ground* via connections. Depending on the type of design, you may route them before or after you route the signals. You must consider the via type (blind, buried, through) and the specific plane to which they attach.

Related Topics

Constraint Definition

Placement

Thermal Analysis

4

Import Libraries and ICs

The OA technology model has been enhanced to support package layouts. This technology data can either be imported directly from Allegro or loaded through the Virtuoso technology file. In addition, vendor and customer component libraries can be imported and used in Virtuoso RF while creating and verifying the package schematic and layout.

Technology File

The Virtuoso technology database is provided by the foundry (for IC fabrics) or the Outsourced Semiconductor Assembly and Test (OSAT) for package fabrics. Typically, the technology rules provided by OSAT houses are in the form of manuals that must be transcribed to Virtuoso technology file constructs that are subsequently loaded into Virtuoso.

The Virtuoso technology model has been extended and adapted to cover new constructs that are specific to the packaging world.

A simpler alternative to create a technology database using a hand-written technology file is to import the technology from an existing Allegro `.sip` or `.mcm` file that has been built using the same or a similar technology.

When importing information into a library where data exists, you have the options for updating the technology database while importing information from an existing `.sip`/`.mcm`/`.brd` file.

Related Topics

Import Technology File

Update Technology File

Constructs in the Technology File

Die Export

You can instantiate die footprints of ICs in the package layout from package library. IC/die footprint is the cellview in Virtuoso representing an IC design that includes the layout, schematic, and symbol. Exported die is the cellview that represents the footprint of the Die/IC/package, which will be instantiated in the package design. It contains an abstract, TILP, schematic, and symbol view. IO cell is also instantiated in the die/IC layout to represent its external connectivity.

During die export, the IC/die footprint is handed over to the package designer. By exporting the die, you can create technology-independent abstraction, which enables Edit-in-Concert, layout versus abstract (LVA) checks, and cross-fabric simulation using die schematic and model-based simulation for dies.

Related Topics

Die Export Preparation

Exporting Dies

Die Audit Overview

The audit functionality is a checker utility that reports all errors or warnings for an export die function on an IC layout before actually exporting a die. You can click *Module – Compliance Audit* to open the Virtuoso RF Compliance Audit form. During the audit, you are provided the same environment or settings as while running actual die export functionality to ensure that the same issues can be found and fixed earlier in the cycle. Related Topics

Die Audit

5

Package Schematic Creation

The package schematic contains the symbols of SMDs from SiP and the die symbol obtained from die export. It can contain more components, such as LGA, embedded components, and Transmission Lines (TLines). The package schematic contains the IC and package portions of the design that are represented, designed, and verified within a single environment. It eliminates the tedious and error prone process of maintaining multiple schematic databases. It lets you Edit-in-Concert the package and IC in the design flow. For example, you can explore the possibility of implementing a selected passive component of the IC, verify the performance by running a simulation, and decide about how best to implement the component. In some cases, a network of passive components may be better implemented across the boundary of the die placed on a package. This is true for RF modules, where the optimum design of filtering and matching networks often leverages components on both the die and in the package substrate.

To ensure that the top-level package design is derived from a package technology, create a package schematic inside a library where the technology library has the `package`, `module`, or `board` fabric. For example, a library created by importing a design from Allegro.

The Virtuoso RF Solution provides a library that contains the symbol view, simulation view, and OA layout view for TLines. You can instantiate the symbol views and capture connectivity in the package schematic. Tline components are derived from rfTlineLib, which is a library of wideband-accurate transmission line models in multi-conductor microstrip and stripline configurations.

Related Topics

Instantiating BGA Instances

Instantiating IC Instances

Creating TLines Instances

Instantiating TLine Instances

6

Package Layout Creation

Package layout is generated from the package schematic for editing the package layout. To complete the physical layout, use GFS to generate the layout. If there are flip chip attachments, use the appropriate instance properties to place the components on the top or bottom of the substrate with the correct orientation. Connect balls to IO pads through curved paths by using flight lines and connectivity/DRC markers in the Annotation Browser. You need to fix shorts on signals with power and ground planes by creating dynamic shapes and performing voiding. The synchronized edits in the die abstract and layout are covered in the Edit-in-Concert topic.

Note: Module fabrics are treated the same way as package fabrics. Therefore, the commands in the *Module* menu are available to cellviews with package and module fabrics.

Generate from Source

The package layout is generated from the package schematic using the existing Generate from Source (GFS) functionality to place the components appropriately.

During GFS, each layout instance, net, and terminal is created. Individual components in the schematic are represented as the TILP instances that contain type specific information of their function and parameters, such as rotation, mirrored, flipped, and so on, which control the re-layering and geometry of the shapes contained within the components.

The GFS process creates a single level of layout hierarchy. This layout hierarchy may bind to a different schematic hierarchy - the binder component in the Virtuoso RF Solution maintains the correspondence between objects in the schematic and layout hierarchies.

Related Topics

Generating a Layout

Update Binding Information

Dies in Virtuoso RF Solution

7

Edit-in-Concert

The Edit-in-Concert feature lets you view and edit die packages and their corresponding die layouts synchronously. It enables the IC designers and package designers, who are cross-geographically located and work on different platforms, update the designs (die or package) using the abstract files that do not require synchronous or concurrent operation of the tools. For example, when a layout engineer creates a die layout and a package engineer creates the corresponding die package.

- In die layouts, device placement is driven by factors such as the internal blocks of the design, routing of the layout, and the power requirements of the layout.
- In die packages, device placement is determined by factors such as the final alignment with the package BGA, the minimum bond wire lengths, and the usage of passive elements in the package.

You can use Edit-in-Concert to view and edit the board, package, and layout synchronously. Edit-in-Concert lets you:

- Visualize the IC in the context of the package and see where a change to one die impacts the design of the other.
- Ensure that the combination of die layout and the die package meets all design requirements, while minimizing the overall cost of production.

Edit-in-Concert mode can be launched from package, module, and board layouts. To switch to Edit-in-Concert mode, with a package or board die open, choose *Module – Edit-in-Concert*. The package and die layouts associated with the die footprint instances in the board or package die are displayed on subsequent tabs.

View-in-concert mode allows designers with limited permissions to view package and IC representations alongside each other, similar to edit-in-concert mode. This functionality is used by designers to analyze their focus sections of an IC in the context of the package and view the package routing near it. The other items in the *Module* menu are enabled or disabled based on the read or write permissions of a cellview. The *View-In-Concert* menu item is visible only when the cellview is opened in read-only mode.

Related Topics

Generating a Layout

Update Binding Information

Launch Edit-in-Concert Mode

Modify in Edit-in-Concert Mode

View-in-Concert Mode

8

Stacked Modules Management

Stacked modules are the basic building blocks of modern micro-electronic systems. Miniaturization of devices, for example cellular devices and medical devices, led to an increased demand for compact integrated circuit (IC) integration without any impact on device performance. To achieve compaction, IC dies are stacked and bonded. Stacking dies increases the available surface area on a package. Also, the electrical connections between stacked ICs are stronger than those on regular ICs.

A stacked module is a circuit that is integrated vertically with two or more dies that are stacked, aligned, and bonded using bumps. In conventional ICs, dies are connected using bumps or bonding pads on one side of the chip. In stacked modules, re-distributed layers (RDLs) are generated at the back of the chip. Bumps can be placed on both sides of the chip. Through-silicon vias (TSVs), through-package vias (TPVs), bumps, and silicon interposers help establish interconnections between dies.

Related Topics

Virtuoso Stacked Silicon Solution Flow

Stacked Modules

Benefits of Implementing Stacked Modules

Components of a Stacked Module

Stacked Module Assemblies

Virtuoso Stacked Silicon Solution Flow

Configuring a Stack

Die Operations

A stacked module comprises dies that are integrated vertically, aligned, and bonded using bumps. Bump management tasks are an integral part of the Virtuoso Stacked Silicon solution. Bump management tasks can be categorized into die operations and inter-die operations. Die operations are performed on individual dies and inter-die operations impact two or more dies.

In Virtuoso, bump management tasks can be run only when the design is open in Edit-In-Concert mode. In this mode, die commands are available from the tabs corresponding to individual dies and inter-die commands are available from the package or container tab.

Related Topics

Creating Bumps and TSVs

Assigning Connectivity between Bumps

Unassigning Bump Connectivity

Deleting Unassigned Bumps

Moving Pins to Bumps

Updating Bumps to the Abstract View

Saving Bumps to File

Creating Bumps from File

9

Verify the Package

The connectivity, LVS, and DRD checks are being done on the layout. When the package layout is modified, you need to verify that the connectivity of the physical implementation is valid. Markers are created to indicate opens and shorts present in the layout. Batch and interactive DRD checks can work with both curvilinear and regular shapes in a package layout. The DRD checker can be used to verify for the constraint violations in a package layout. Both connectivity extractor and DRD checker take into account void shapes.

Verifying that a design is correct is often the most difficult and yet also the most important aspect of designing a package layout. Additionally, routing paths should be adjusted iteratively until the package is optimized for all constraints. The number of layers depends on power levels and complexity.

Related Topic

Checking Layout

Cross-Fabric Checks Run

Checking Layout Against Schematic

Performing Cross-Fabric Checks

Extracting the Connectivity

Performing DRD Checks

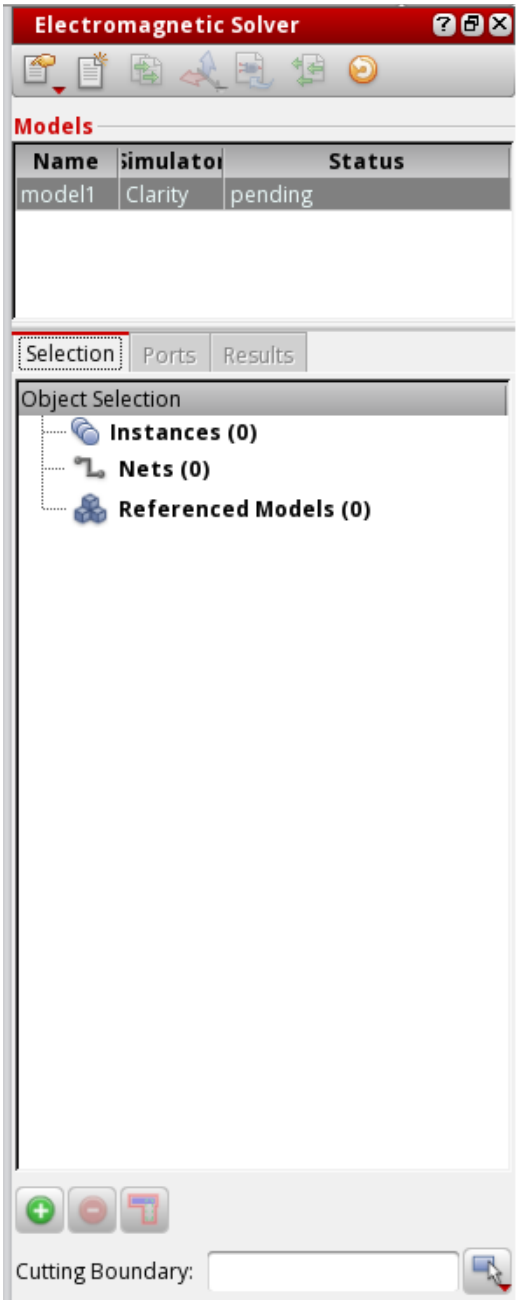
Supported DRD Constraints and Checks

10

3D Electromagnetic Simulation

Clarity and EMX are integrated as the extraction engines into the Electromagnetic Solver in Layout MXL. They let you create models by using Sigrity 2019 from the layout. Solvers can

simulate a metal structure in full 3D and find its RF behavior for many different frequencies. The result is a matrix of S-Parameters that is read by Spectre to achieve accurate simulations.



In general, models consist of nets and instances. IC models contain a process stack read from the ICT file.

On the other hand, package models contain a process stack read from techDB. Vias in package are exported as padstacks to the solver. The flip chip bumps and BGA balls are automatically created during EM simulation.

Types of EM Solvers in Virtuoso RF Solution

The Electromagnetic Solver assistant in Virtuoso Layout MXL provides an interface to create 3D models for passive devices in the layout view by using Sigrity. You can choose one of the following four solvers to run extraction and create S-parameters:

- **Clarity**: Uses a three-dimensional (3D), full-wave, finite element method (FEM) Clarity 3D Solver that uses the industry-leading parallelization technology to ensure that both meshing and frequency sweeping can be partitioned and parallelized across as many computers, computer configurations, and cores as are available.
- **EMX**: Uses a planar 3D solver to simulate high-frequency, RF, and mixed-signal integrated circuits. It allows designers to accurately and efficiently simulate large RF circuit blocks, characterize the behavior of passive components, and analyze the parasitics due to interconnect.

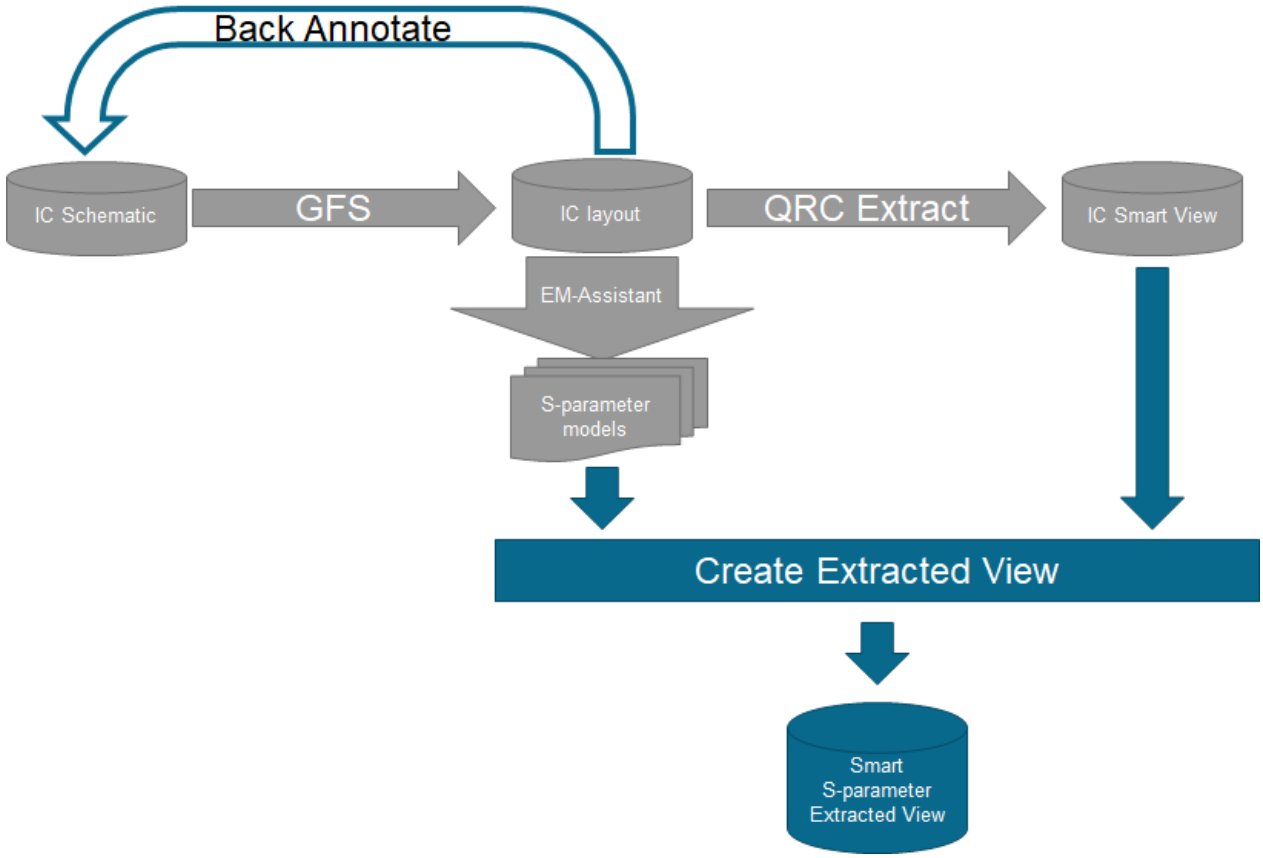
Related Topic

Electromagnetic Solver Assistant

Extracted Views Creation

Extracted cellview is created post the EM simulation where the nets and instances that are part of the model are replaced with an n-port instance. n-port is a schematic symbol that has the same number of ports as the S-Parameter matrix and points to the Touchstone file on the

disk. The stitched models in the extracted view are highlighted in the schematic during backannotation.



Important

The extracted views can be created for hierarchical and cross-fabric models.

Extracted View Creation From the Schematic

While creating an extracted view from a schematic, you can use only the flat IC schematic design and the single-device model for creating the extracted view. The database size becomes large due to fractured net segments and instances of parasitic devices.

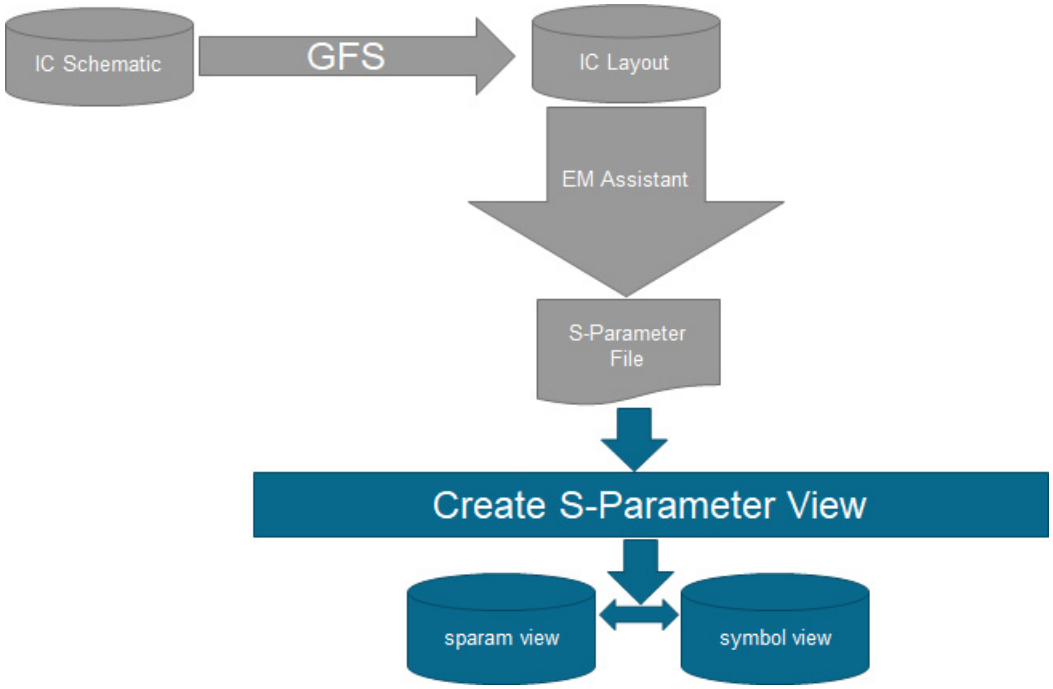
Extracted View Creation From Smart View

Creating a Smart View is better than creating an extracted view from schematic. It provides an efficient data model supported by OpenAccess Database consisting of layout OA database (`layout.oa`) and parasitic information database (`detailed_rc.oa`).

The Smart View is created with Quantus QRC.

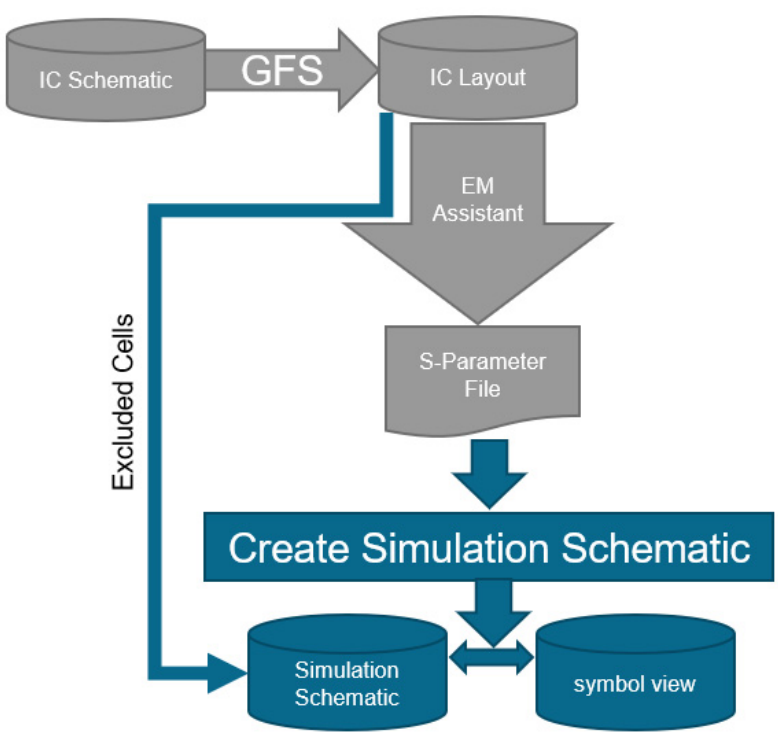
Extracted Views Creation From Full Cellviews

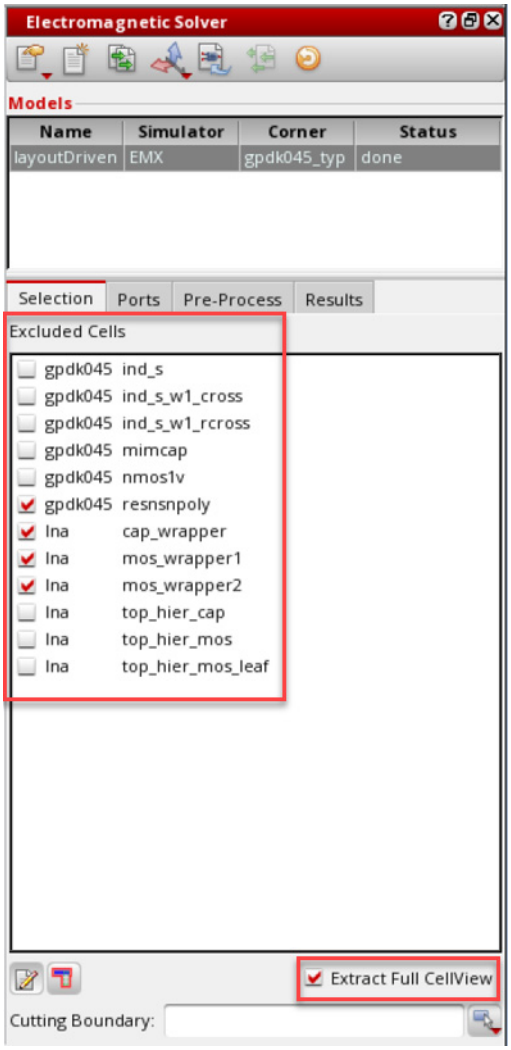
In this flow, the entire layout is extracted to an s-parameter cellview. This cellview can be selected for netlisting in the Hierarchy Editor. There is no separate extracted view and no stitching is needed because the entire layout is extracted. This is primarily a layout-driven flow.



You do not need to specify instances or nets. Select the *Extract Full CellView* check box to extract the entire cellview. You can exclude some cells from the layout by selecting from the

Excluded Cells list. In this case, an n-port schematic is automatically created that contains the excluded cells.





Related Topic

Smart View Output

Full Cellview Extraction

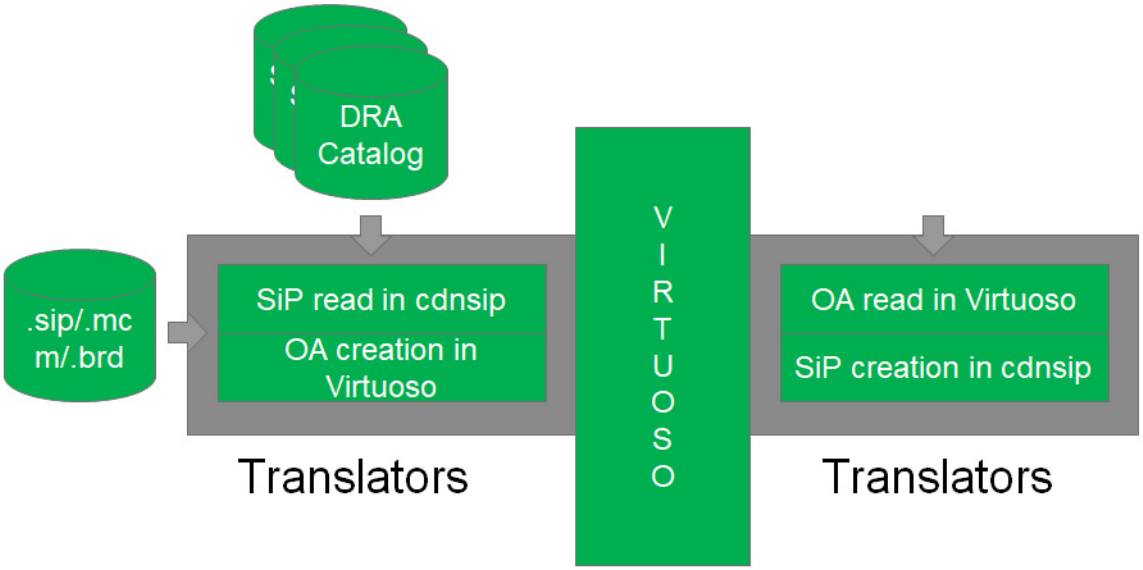
11

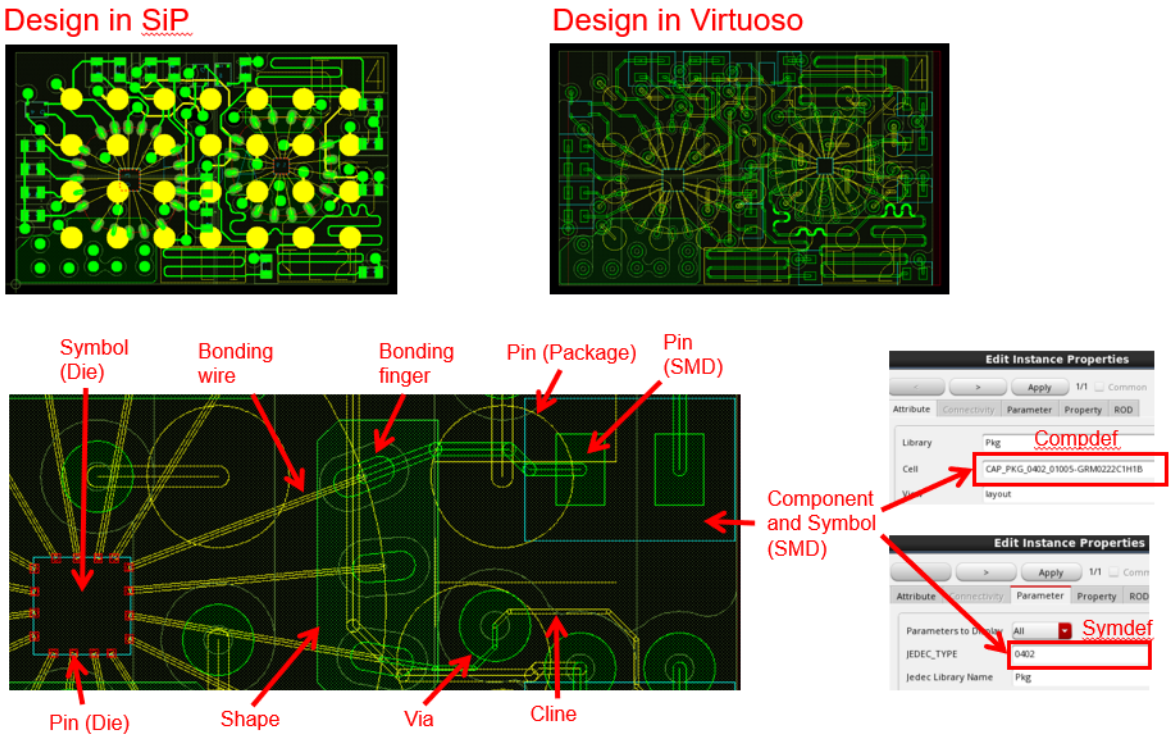
Interoperability with SiP

The Virtuoso RF Solution is a schematic driven package layout flow in Virtuoso that provides the capability to finish the package in Allegro. Therefore, interoperability with Allegro for package design should be robust to support seamless data transfer. The data models in Allegro and Virtuoso have significant differences and the gap needs to be bridged. The Allegro translators are invoked from Virtuoso and require a license for the SPB tools based on the type of the input or output database.

Due to the differences in the underlying SiP and OA databases, the object representations in SiP and OA are sometimes not entirely equivalent. Once the object has been translated from SiP to OA, it might not restore to its original SiP representation from the OA representation. Consequently, the translation of a SiP design to OA and back to SiP might be different from

the original one. However, the physical layouts created from the two design representations are equivalent from the manufacturing and analysis point of view up to a certain tolerance.





The following SPB layout design tools are involved in the export and import of the layout information:

- `.sip` file from Cadence SiP Layout (SiP)
- `.mcm` file from Allegro Package Designer (APD)
- `.brd` file from Allegro PCB Designer (Allegro)

Related Topic

Allegro Translators

Export Package Layout

Complete the Package Layout

Importing the Package Layout

Rebinding the Layout to a Schematic